MASTER OF SCIENCE THESIS

A Precision RC-locked Oscillator

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November 15, 2010

NXP founded by Philips

Electronic Instrumentation Laboratory

TU Delft

Delft University of Technology

A Precision RC-locked Oscillator

MASTER OF SCIENCE THESIS

For obtaining the degree of Master of Science in Electrical Engineering
at Delft University of Technology

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November 15, 2010

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Abstract

In this thesis, the development and implementation of a new precision RC-locked oscillator topology suitable for wireless sensor networks (WSNs) is described.

The objective of this thesis was to investigate the performance of the proposed topology and to compare this with the state-of-the-art in terms of accuracy and power consumption.

The new oscillator was implemented in a 0.16 μm CMOS process. Despite a few bugs, the prototype was sufficiently functional to be tested. It achieved a frequency inaccuracy of $\pm 0.9\%$ (3σ based on 12 samples) from -40^{o}C to 125^{o}C, consuming 37 μW power. The achieved performance is comparable to the state-of-the-art, for a wider temperature range and for significantly more samples.

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Chapter 1

Introduction

As IC technology improves, it becomes cheaper, its feature sizes shrink and it is possible to benefit from larger scale applications. For example, while only 12.4 million people had cellular phone subscriptions in the early 90s, within two decades, this communication network had expanded to include approximately 4.6 billion people [1]. In the near future, considering this speed in technological development, it will not be surprising to live in smart buildings that become aware of their residents and automatically adjust the living environment for maximum comfort, or to see doctors monitoring the healthcare of the patients from their screens and intervening with a simple mouse click [2]. Answers to all these and similar needs may come from wireless sensor networks (WSNs). WSNs consist of a large number of energy-autonomous nodes. Each node senses several physical parameters, such as temperature and light intensity, and transmits the acquired information through the network until it is collected by a central data sink.

As a WSN node becomes more functional, its circuit-level density increases as well as its power consumption. Considering that the lifetime of a sensor node depends on its battery and that the replacement of a battery is often impractical, ultra low power (e.g. below 100 µW) architectures have to be realized [3].

In addition to the low power requirement, WSN nodes must be cheap and small. A substantial fraction of the cost and size of a WSN node is determined by IC packaging costs and off-chip components, respectively. Both cost and size can be significantly reduced if the number of off-chip components is reduced. Crystal oscillators are common off-chip electronic components which are often used as frequency references [4]. Therefore, the frequency

reference[1] must be fully integrated in the same standard IC technology as the rest of the electronics.

The main function of the integrated frequency reference in a WSN node is to facilitate RF communication. An accurate frequency is needed to appropriately select the portion of the RF spectrum that is used for inter-node communication. Moreover, accurate time information is needed to synchronize each node with the rest of the network, and to shut down the node when it is not needed. A high-accuracy time reference results in accurate synchronization, a lower duty-cycle and consequently lower power consumption. However, integrated frequency references typically suffer from reduced accuracy. Designing a reference with sufficient accuracy within a limited power budget is a challenging task.

State-of-the-art WSN topologies require CMOS frequency references with accuracy in the order of 1% and power consumption lower than 50 µW over a wide range of temperature [16].

In chapter 2, possible implementations of fully integrated frequency references are presented. As an alternative, a new frequency reference is introduced in chapter 3. The circuit level implementation of the new frequency reference is described in chapter 4 and, finally in chapter 5, the measurement results are presented. The thesis ends with some conclusions.

[1]The expressions “oscillator” and “frequency reference” are interchangeable.

Chapter 2

Fully Integrated Frequency References

As mentioned in chapter 1, a WSN node requires a fully integrated frequency reference that consumes low power (50 µW), is moderately accurate (in the order of 1%) over a wide temperature range, and which can be realized in standard CMOS technology. Fully integrated frequency references can be categorized as: Feedback [5, 7], relaxation [18] and locked [6, 8, 9, 10, 16] oscillators. In the following sections, the operating principles and important design issues of these oscillators are briefly described.

2.1 Feedback Oscillators

In feedback oscillators, a feedback system is established and the oscillation condition is satisfied by Barkhausen criterion. Therefore, the oscillation signal has a sinusoidal waveform. LC-based, Wienbridge and ring oscillators are commonly implemented feedback oscillators. In the following part, the principles and the accuracy limitations of LC-based [5] and wienbridge [7] oscillators are summarized.

2.1.1 LC-based reference

The block diagram of a typical LC-based reference is shown in figure 2.1.1. This reference consists of two main parts: a resonant tank and an active circuit. The resonant tank includes an inductor and a capacitor. The active circuit compensates for the losses of the tank and sustains the oscillation. The oscillation condition is satisfied when the active circuit compensates for the losses of the tank and the phase shift across the tank is zero. It is desired

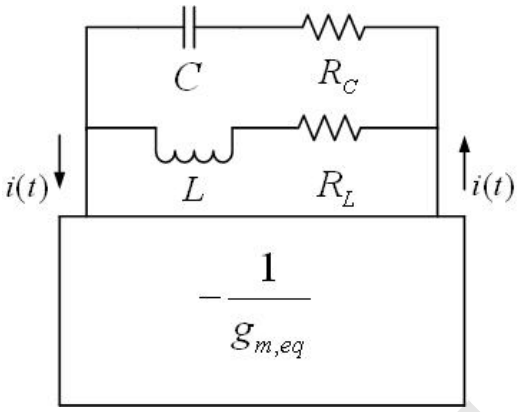

Figure 2.1.1: Block diagram of LC-based reference

that the oscillation frequency is only determined by inductor and capacitor values. The resistive losses of the inductor limit its quality factor and as a result such losses can be the dominant source of inaccuracy. An important consequence of having low inductor quality factor is relatively high power consumption. The active circuit has to compensate for the losses of the tank and so as the losses increase the active part requires higher g_m values, or simply, more power. In literature [5], a new passive temperature-compensation technique is demonstrated where a lossy capacitance is deliberately introduced to cancel the loss in the coil. This passive compensation technique significantly reduces the power consumption and the noise compared to the use of active compensation circuitry. An accuracy of ±300 ppm is reached in the temperature range from 0 ^{o}C to +70 ^{o}C. However, the power consumption of the frequency reference is around 4 mW, which is too high for use in WSNs.

2.1.2 Wienbridge oscillator

The Wienbridge oscillator is an example of a feedback oscillator that consists of an amplifier and a RC feedback network as shown in figure 2.1.2. The transfer function of this feedback network is written as in equation (2.1.1):

$$H(s) = \frac{R.C.s}{R^2.C^2.s^2 + 3.R.C.s + 1} \tag{2.1.1}$$

The Barkhausen criterion requires using an amplifier with a non-inverting gain of 3 and zero phase shift. The resistors R_1 and R_2 are used to adjust the gain of the amplifier to 3.

The oscillation frequency can be expressed as:

$$f_{out} = \frac{1}{2.\pi.R.C} \tag{2.1.2}$$

where R and C are the values of the resistors and capacitors used in the feedback network.

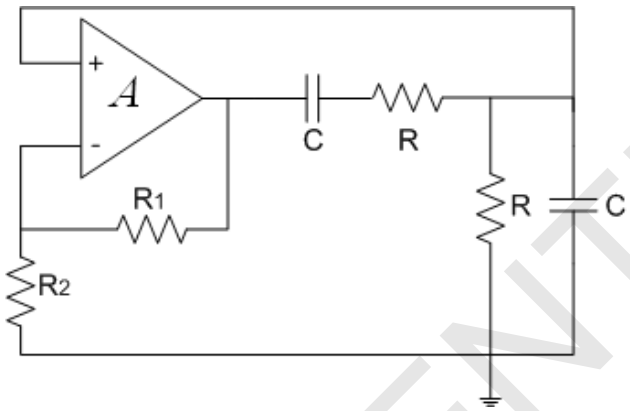

Figure 2.1.2: Block diagram of Wienbridge oscillator [7]

As can be seen from equation (2.1.2), ideally the frequency is determined by the resistor (R) and capacitor (C) values in the feedback network. However, in practice, the non-idealities of the opamp (e.g. its finite output resistance and phase shift at the oscillation frequency) affects the frequency. In addition, even though it is not shown in figure 2.1.2, the output signal of the opamp has to be limited by an amplitude regulator and this circuit also strongly affect the temperature coefficient of the output frequency [7]. To reduce these effects, gain boosting and current bleeding techniques are used at the expense of power consumption. In [7], a temperature coefficient of 86 ppm /^{o}C (from 0 ^{o}C to +100 ^{o}C), -172 dB (at 100 kHz) FoM phase noise and 66 µW power consumption is reported. This oscillator can be used in WSN applications. However, its power consumption is still somewhat higher than desired (50 µW).

2.2 Relaxation oscillator

A relaxation oscillator is an oscillator based upon the iteration of charging and discharging a capacitor. The conventional topology is shown in figure 2.2.1. The oscillation takes place as follows: 1: While the capacitor, C, is charged by the current, I_1, the voltage V_{osc} rises; 2: If $V_{osc} > V_{high}$, the

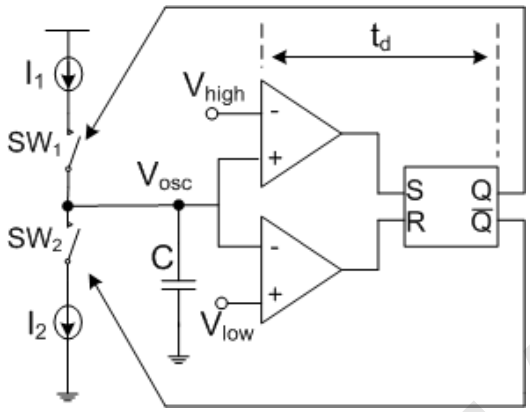

Figure 2.2.1: Conventional Relaxation Oscillator

comparator sets SR-FF, closes the switch SW_1 and changes the state of the oscillator into discharging phase; 3: V_{osc} falls while C is discharged by I_2; 4: If $V_{osc} < V_{high}$, other comparator resets SR-FF, closes the switch SW_2 and the state returns to charging phase.

The main issues of this oscillator are as follows: 1: The variation of comparator's delay t_d results in frequency variation with voltage and temperature; 2: The aging of the current sources degrade the accuracy of the slope of V_{osc} and varies frequency; 3: The flicker noise of the current sources degrade the accumulated jitter. A simple solution to obtain an accurate oscillation is to nullify t_d, however, this approach requires consuming huge power in the comparators so that it is not a low power approach. In literature [18], voltage averaging feedback (VAF) concept is introduced to overcome this trade-off. The topology is shown in figure 2.2.2. It consists of a relaxation oscillator with resistor, R, and capacitor, C, and an active integrator for VAF. The oscillation takes place as follows: 1: Assume the switches SW_1 and SW_2 are close, and SW_3 and SW_4 are open, so V_{osc1} and V_{osc2} are grounded; 2: SW_1 is open, SW_3 is close, V_{osc1} starts to rise up to V_{dd} and this signal is transmitted to the integrator via transmission gate; 3: V_{osc} is filtered out by the integrator to become V_c; 4: If V_{osc1} exceeds V_c, the SR-FF toggles the states of the switches, then, V_{osc2} starts to rise up to V_{dd} while V_{osc1} is grounded. The relaxation oscillator part is considered as a voltage-controlled oscillator with a control signal V_c. At the steady-state, the DC value of V_{osc} is equal to V_{ref} so that there is no charge accumulated by the integration capacitor, C, so that V_c stabilizes and the oscillation is locked.

In [18], it is proved that the oscillation frequency is just defined by a time constant RC and V_{ref}/V_{dd}. Since V_{ref} is a function of V_{dd}, the oscillation frequency is immune to supply variations. The variation of the comparator

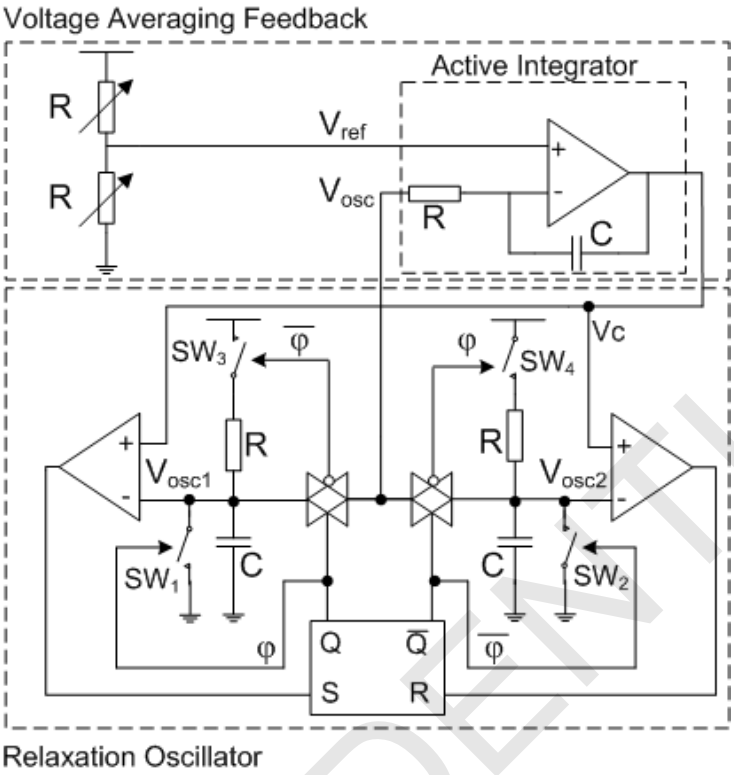

Figure 2.2.2: A relaxation oscillator with power averaging feedback

delays has little effect on the frequency, because, the feedback system automatically adjusts V_c to keep the equilibrium condition. Therefore, VAF has a negative-feedback effect. Another advantage of the topology is that the low offset frequency part of phase noise of the relaxation oscillator is suppressed by this effect. In [18], 23 ppm /^{o}C accuracy (from -40 ^{o}C to +125 ^{o}C), -146 dB (at 100 kHz) FoM phase noise and 45 μW power consumption is reported. This oscillator can be used in WSNs.

2.3 Locked Oscillators

In a locked oscillator, a voltage/current that is proportional to the output frequency of a VCO is produced by a converter block and its output is compared to a reference voltage/current that is proportional to an RC or thermal delay. An integrator drives the VCO on the base of the result of the comparison. The simplified block diagram of a locked oscillator is shown in figure 2.3.1. The frequency accuracy is determined by the precision in the conversion between time and voltage/current and in the mechanism used to

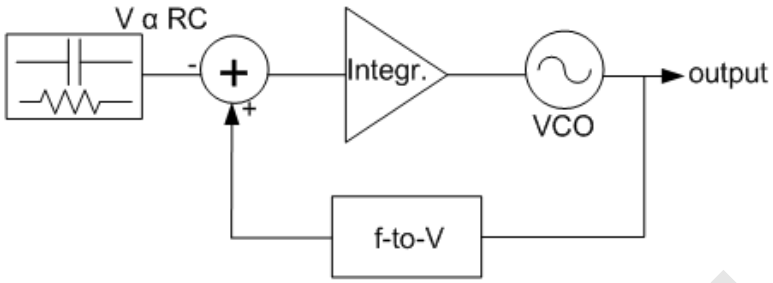

Figure 2.3.1: The block diagram of a locked oscillator

produce a voltage/current proportional to the resistor and capacitor. Different techniques can be employed to implement such blocks but the use of any additional circuit can spoil the frequency accuracy, compared to simpler architectures as it will be shown in the following examples. The main advantage is that even though a VCO is used in the system, the frequency accuracy of the reference only depends on the accuracy of the passive components. In this way, for example the jitter performance of the VCO is decoupled from the accuracy of whole reference.

In the following part, the principles and the accuracy limitations of two different implementations in [8] and [9] are summarized.

2.3.1 Electro-thermal filter (ETF) based reference

An electro-thermal filter (ETF) is a system whose inputs and outputs are electrical but in which the filtering takes place in the thermal domain. The block diagram of an ETF is shown in figure 2.3.2. It consists of a heater and a temperature sensor. The filter's input is the electrical power that drives the heater and turns into heat. The heat propagates through the silicon substrate and generates temperature gradients. The temperature gradients are then converted back to the electrical domain by the temperature sensor [10].

The block diagram of the ETF-based frequency reference is shown in figure 2.3.3. This is an example of a locked oscillator. An oscillator is locked to the propagation delay through the silicon, so that its period is proportional to the time taken by the heat wave to travel from the heater to the temperature sensor. The phase - frequency characteristic of the ETF then defines the oscillation frequency which can be written as[1]:

[1]This formula only applies for the point-heater point-sensor ETF.

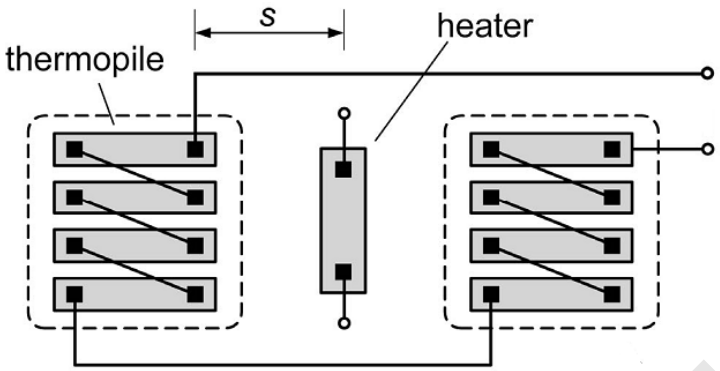

Figure 2.3.2: The block diagram of an ETF

$$f \propto \frac{D\phi_{ref}^2}{\pi s^2} \tag{2.3.1}$$

where ϕ_{ref} is the phase of the transfer function, D is the thermal diffusivity of the silicon and s is the the distance between the heater and the temperature sensor.

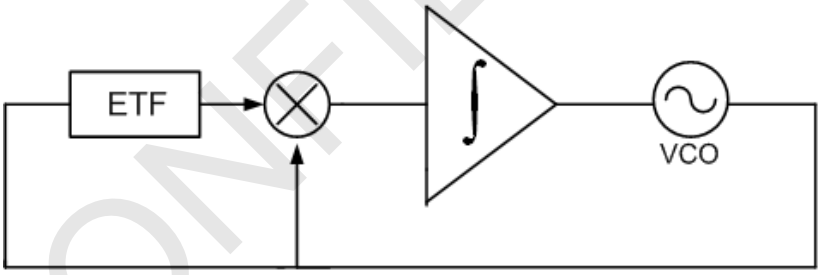

Figure 2.3.3: The block diagram of ETF-based frequency reference

The accuracy of the ETF-based frequency reference is limited by the accuracy of the thermal diffusivity of the silicon, D and the distance between the heater and the temperature sensor, s. The spread of D is practically zero in modern CMOS technologies and is therefore negligible. Therefore, the dominant source of error is the spread of s, which is determined by the lithographic accuracy of the process. The relative error $\triangle s/s$ can be reduced by increasing s, however increasing the distance degrades the signal-to-noise ratio of the filter output and hence the noise performance of the oscillator. Increasing the heater's power dissipation can compensate for this

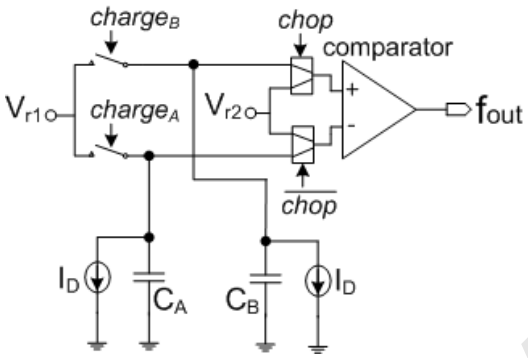

Figure 2.3.4: The block diagram of mobility-based frequency reference

effect. Technology scaling will also downscale the power consumption while keeping the accuracy and the amplitude of the filter output signal. However, even after scaling the ETF proposed in [11] from 0.7 μm CMOS to 65 nm CMOS, the heater power would only scale down from 2.5 mW to around 250 μW which is still too high for WSNs. In [11], $\pm$0.1% (from -55 ^{o}C to +125 ^{o}C) frequency inaccuracy, 312 ps (rms) period jitter and 7.8 mW power consumption is reported.

2.3.2 Mobility-based reference

A mobility-based reference is based on a current-controlled oscillator, in which the current is proportional to the charge mobility [16]. The block diagram of the system is shown in figure 2.3.4. It consists of a current reference, I_D, two capacitors C_A and C_B and a comparator.

I_D is used to linearly discharge C_A and C_B which are alternatively precharged to V_{r1}. When the voltage on the discharging capacitor drops below V_{r2}, the output of the comparator switches and the linear discharge of the other capacitor starts immediately.

The frequency of the oscillation is determined as:

$$f_{out} = \mu_n k \frac{C_{ox}\frac{W}{L}}{C} . \frac{V_R^2}{V_{r1} - V_{r2}} \tag{2.3.2}$$

where μ_n is the electron mobility, $C = C_A = C_B$, C_{ox} is the gate capacitance per unit area, V_R is the reference voltage, W and L are the width and the length, respectively, of a transistor used to generate I_D.

The offset of the comparator is an important source of error, because, it modifies the reference voltage, V_{r2} and alters the switching time of the comparator's output. The two multiplexers at the input of the comparator

are driven by the signal *chop* to mitigate this effect. In [16], frequency spread of ±1.1% (3σ) (from -22 ^{o}C to +85 ^{o}C), 52 ns (rms) period jitter, 0.1% relative jitter (after one second) and 41 µW power consumption is reported. This oscillator can be used to generate a reference frequency accurate enough for WSNs and the architecture is both low-voltage and low-power, as required by autonomous sensor nodes.

2.3.3 Frequency-to-voltage conversion-based locked loop

The block diagram of the oscillator designed in [8] is given in figure 2.3.5. The output of the VCO is converted into voltage by a frequency-to-voltage converter and this voltage is compared with a reference voltage (V_{ref}). The difference between two voltages is integrated and fed back to the input of the VCO.

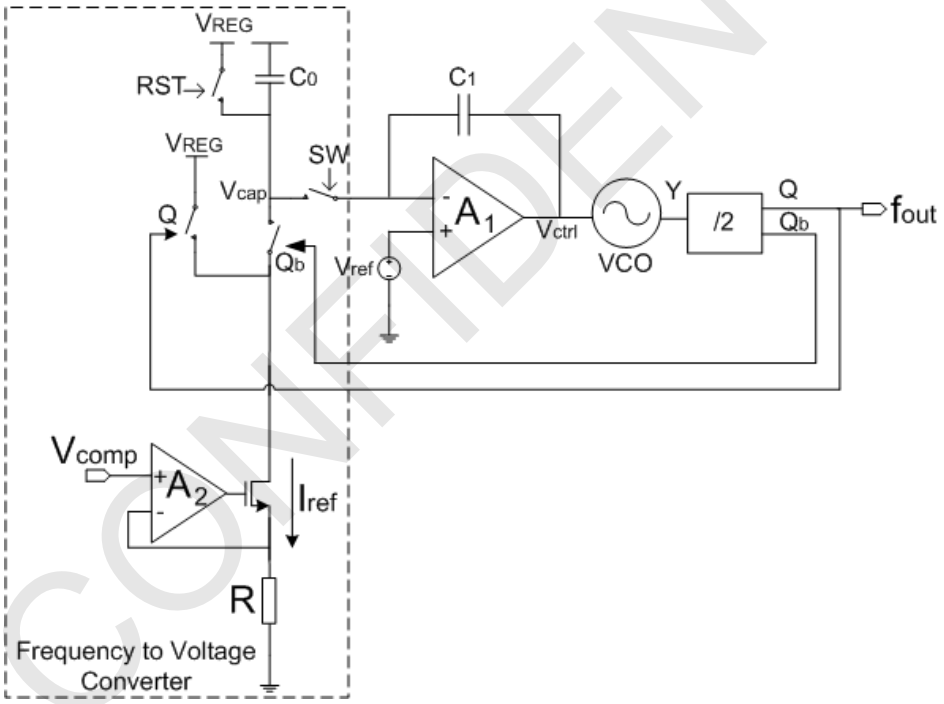

Figure 2.3.5: The block diagram of the frequency-to-voltage conversion based locked loop [8]

The operation of the circuit may be explained by dividing the operation into three different states which are resetting (RST), conversion and switching (SW). The timing diagram is shown in figure 2.3.6. During the reset phase, RST = 1, V_{cap} becomes equal to V_{REG}, the regulated supply volt-

age. The conversion phase starts when signal Q which is the output of the frequency divider is equal to 0. In this phase, the capacitor C_0 is charged by a constant current (I_{ref}) which is obtained by the help of an amplifier, source follower and integrated resistors. Therefore, the V_{cap} voltage level decreases. Next, during the switching phase, SW = 1, the charging action of the capacitor C_0 stops and the available V_{cap} voltage is compared to V_{ref} through the switched capacitor loop filter. The charge difference on C_0, due to the voltage difference between V_{ref} and V_{cap}, is transferred to C_1 and V_{ctrl} voltage is changed. As the V_{ctrl} changes, the oscillation frequency (f_{out}) is adapted. Due to the negative feedback, V_{cap} reaches V_{ref} at the steady state and the desired frequency is achieved.

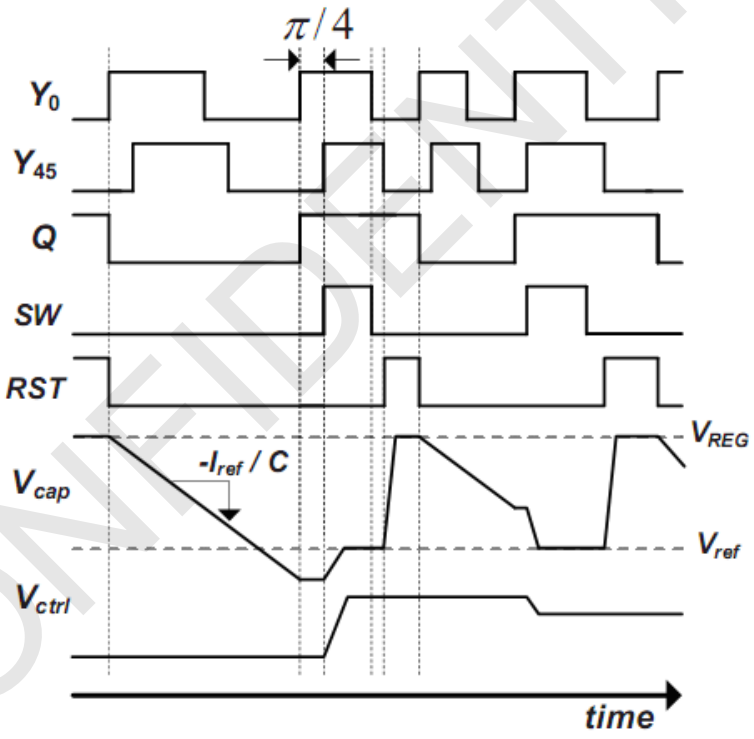

Figure 2.3.6: The timing diagram of the system shown in figure 2.3.5

The resulting frequency can be written as:

$$f_{out} = \frac{3.V_{comp}}{2.R.C_0.V_{REG}} \tag{2.3.3}$$

As can be seen from equation (2.3.3), ideally the frequency is determined by R, C_0, V_{REG} and V_{comp}. The regulator voltage is relatively process and

temperature independent, because it is obtained from a bandgap voltage reference. V_{comp} is derived from V_{REG} and as such it is also process and temperature independent. The V_{comp} is obtained using a linear temperature compensation circuit in order to obtain same temperature dependency of R, so that the temperature dependency of V_{comp} and R is cancelled. Therefore, the output frequency is only sensitive to the process variations of R and C_o and the temperature variations of C_o.

As in the case of Wienbridge oscillator, the amplifier is the critical part of the design. The amplifier A_1 will introduce an offset voltage ($\triangle V_{ref}$) and cause a frequency error at the steady state. The input referred offset voltage of A_2 causes an offset ($\triangle I_{ref}$) in I_{ref}. Since I_{ref} is interacting with the frequency determining elements, $\triangle I_{ref}$ causes frequency error, as well. Therefore, the offset of both amplifiers may be an important source of error. In [8], 67 ppm /^{o}C accuracy (from -20^{o}C to +100^{o}C) and 80 µW power consumption is reported. This oscillator can be used in WSN applications. However, the power consumption is still somewhat higher than desired (50 µW).

2.3.4 Frequency-to-current conversion-based locked loop

The block diagram of the oscillator described in [9] is given in figure 2.3.7. The principle of the oscillator may be summarized as follows: The output of the VCO is converted into current domain by a frequency-to-current converter, compared with a reference current (I_{ref}) by a current comparator and the output of the current comparator (V_{ctrl}) controls the VCO frequency (f_{out}).

As in the case of the frequency reference explained in section 2.3.3, I_{ref} is obtained by fixing one end of the resistors to a reference voltage (V_{bias}) with an amplifier and source follower. The frequency-to-current converter has a similar structure, but instead of using a real resistor, a switched-capacitor resistor that consists of a capacitor, C_s and two switches, S_1 and S_2 are used. The switches are driven by the oscillation pulses from the VCO. The overall structure operates as a resistor with a resistance of $(C_s.f_{out})^{-1}$. Since V_{bias} is used to generate both I_{ref} and I_{out}, the output frequency is independent of V_{bias}.

The resulting frequency can be written as:

$$f_{out} = \frac{1}{(R_P + R_N).C_S} \tag{2.3.4}$$

As it is seen from equation (2.3.4), the frequency is determined by the resistors ,$(R_P + R_N)$ and capacitor, C_S values.

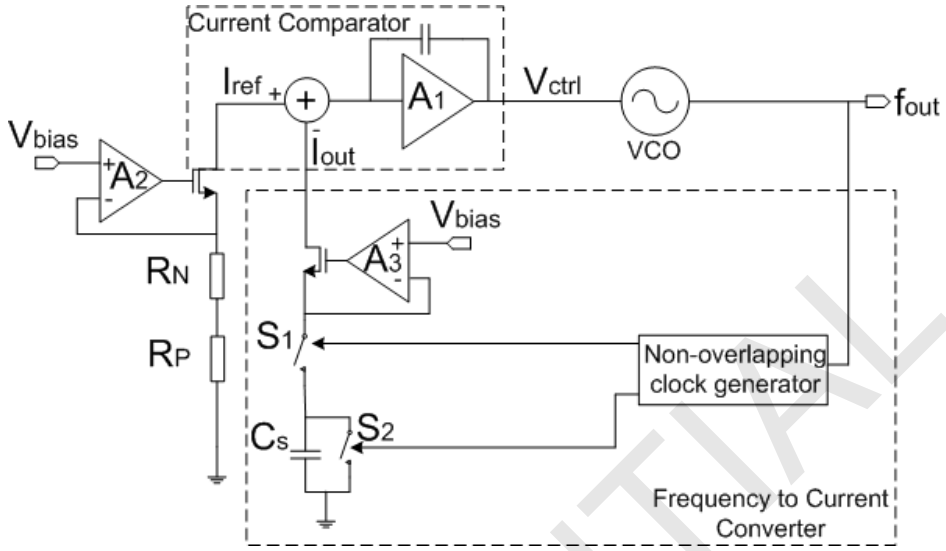

Figure 2.3.7: The block diagram of the frequency-to-current conversion based locked loop [9]

Like the frequency reference in section 2.3.3, the offsets of the amplifiers A_2 and A_3 are important aspects of the design. The input referred offset voltage of A_2 causes a deviation in the reference current ($\triangle I_{ref}$) and that of A_3 causes the current offset ($\triangle I_{out}$). Both offset currents cause the deviation of the output frequency. Therefore, using an amplifier for each of the frequency determining elements is not efficient in term of both accuracy and power. In [9], 90 ppm /^{o}C accuracy (from -20 ^{o}C to +100 ^{o}C), -96 dBc/Hz (at 1 MHz) phase noise and 180 µW power consumption is reported. This oscillator can be used in WSN applications. However, the power consumption is higher than desired (50 µW).

2.4 Benchmark

The benchmark of the oscillators [5, 6, 7, 8, 9, 16, 18] is shown in table 2.1.

2.5 Conclusion

In this chapter, the operating principles and the frequency accuracy limitations of the oscillators in [5], [6] ,[7], [8], [9], [16] and [18] are discussed. The performances of these oscillators are summarized in section 2.4.

In section 1, it was mentioned that the state-of-the-art WSN topology

Literature	[5]	[6]	[16]	[7]	[18]	[8]	[9]
Frequency	24 MHz	1.6 MHz	0.1 MHz	6 MHz	2 MHz	10 MHz	30 MHz
Supply voltage [V]	3.3	5	1.2	1.2	1.8	1.2	1.8
Power	4 mW	7.8 mW	41 µW	66 µW	45 µW	80 µW	180 µW
Area [mm^2]	0.81	6.75	0.11	0.03	0.04	0.22	0.08
Process	0.13 µm RF CMOS	0.7 µm CMOS	65 nm CMOS	65 nm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Variation with temp. [%]	± 0.56 0 ∼ 70^{o}C	± 0.1 -55∼125^{o}C	± 1.1 (3σ) -20∼80^{o}C	± 0.88 (σ) 0 ∼ 100^{o}C	± 0.75 ± 0.19* -40∼ 125^{o}C	± 0.4 -20∼100^{o}C	-0.7 / +0.5 -20∼100^{o}C
Samples measured over temp.	32	16	11	1	1	1	1
Temp. coeff. [ppm /^{o}C]	± 80	± 11.2	± 220 (3σ)	86	92	67	90
Phase noise [dBc/Hz]	-155 (@10 kHz)	N.A.	N.A.	-96 (@100 kHz)	-90 (@100 kHz)	N.A.	-96 (@1 MHz)
Period jitter	N.A.	312 ps	52 ns (rms)	N.A.	N.A.	N.A.	N.A.
Process sensitivity	N.A.	N.A.	7% (3σ) 11 samples	0.8%(σ) 6 samples	N.A.	N.A.	2.7% (σ) 20 samples

Table 2.1: Performances of state-of-the-art frequency references

* This performance could be obtained if the decoder would work properly.

requires a frequency reference which consumes less than 50 µW, has an accuracy in the order of 1% over a wide range of temperature and occupies low chip area. The power consumption of the oscillators in [5] and [6] is in the order of mWs and therefore they are not suitable for this application. The rest of the oscillators' performances appear to be suited for WSN. However, in [7], [8], [9] and [18] the reported frequency accuracies belong to only 1 sample, which does not provide any statistical information. Besides, the power consumption of [7], [8] and [9] are above the desired level. In [16], the power consumption is low enough, however there is still headroom for further improvement.

In the following chapter, a new frequency reference topology is introduced and its performance is investigated. With the new topology, a performance better than the ones listed in table 2.1 is targeted in terms of power and accuracy.

Chapter 3

A New RC-based Frequency Reference

3.1 Specifications

As described in chapter 1, the main requirements of the frequency reference for a WSN node are low power consumption and moderate frequency accuracy. Based on the work in [17], targeted specifications are derived for the new frequency reference and summarized in table 3.1.

The frequency accuracy specification is clarified with the help of figure 3.1.1. For simplicity, temperature compensation is not implemented and the 3σ spread of the oscillation frequency in the extreme temperatures is targeted to be less than 0.2%, after trimming at room temperature.

Specification	Values
Temperature Range	-55 ^{o}C to 125 ^{o}C
Power Dissipation	$<$ 50 µW
Frequency Inaccuracy	$\pm$0.2% (3σ)
Output Frequency	250 kHz
Temperature Coefficient	$<$ 80 ppm /^{o}C
Initial Accuracy / Trimmed Accuracy (@27 ^{o}C)	$\pm$20% / $\pm$0.05%
Process Node	0.16 µm CMOS
Supply Voltage	1.2 V, 1.8 V
Additional	Trimming (Pin Programming)

Table 3.1: The target specifications of the new RC-based frequency reference

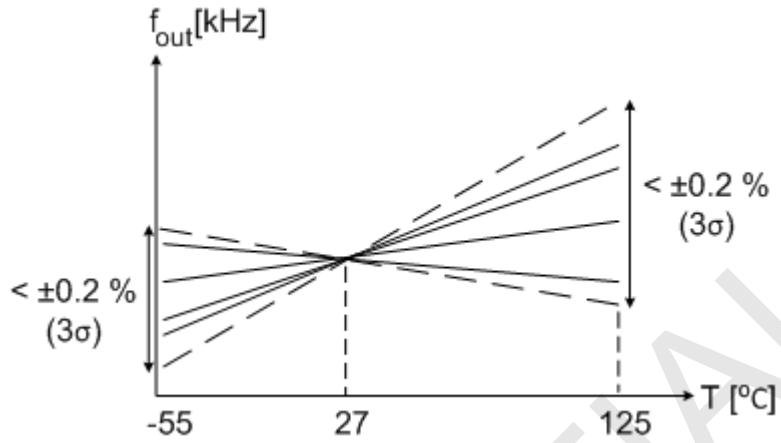

Figure 3.1.1: The frequency accuracy specification

3.2 The Proposed Topology

The proposed RC-based frequency reference topology can be seen in figure 3.2.1. The proposed topology is composed of an RC network, which is shown as H(f), a mixer, an integrator, a VCO and a frequency divider.

The operation of the building blocks in figure 3.2.1 can be summarized as follows: the RC network is used to obtain a phase shift between its input and output (φ), the mixer acts like a phase detector, generating an output signal based on the phase difference between its inputs, the integrator integrates the output of the mixer and the VCO tunes its output frequency (f_{out}) using the output signal of the integrator. At the steady state, where $\varphi = \pi/4$, the negative feedback forces the input of the integrator to be equal to zero and then the RC network fixes the frequency.

From the structural and operational point of view, the proposed system is very similar to the ETF-based frequency reference explained in section 2.3.1. In an ETF-based reference, the ETF is used as the frequency-determining component by means of its fixed frequency/phase characteristic. In the proposed topology, an RC network replaces the ETF.

The loop in figure 3.2.1 can be further analyzed using a mathematical approach. Assuming that the output of the frequency divider is $A_1.\cos(\omega.t)$, the output of the RC network can be written as $A_2.\cos(\omega.t+\varphi)$. The output of the mixer (V_{mix}) is calculated as:

$$V_{mix} = A_1.cos(\omega.t+\varphi) \times A_2.cos(\omega.t) \tag{3.2.1}$$

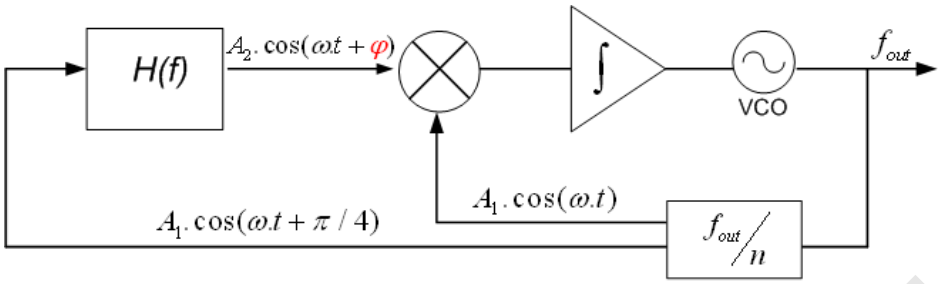

Figure 3.2.1: The proposed RC based frequency reference topology

$$V_{mix} = \frac{A_1.A_2.[cos(2.\omega.t+\varphi)+cos(\varphi)]}{2} \tag{3.2.2}$$

Initially considering that $\varphi = 0$, then due to the DC term, which is $cos(\varphi)/2$, the integrator's output will start to change. Once φ settles to $\pi/2$, the DC term will disappear because $cos(\varphi) = 0$ for $\varphi = \pi/2$. Since in equation (3.2.2), only a sinusoidal signal remains which is at the double frequency of the oscillation, the average value of the V_{mix} is zero which means that the integrator's average output signal remains constant. Since this signal is the control voltage of the VCO, the frequency output of the VCO is locked. Therefore, the oscillation condition of the loop is that the phase difference of the two input signals of the mixer to be equal to $\pi/2$. This phase difference can partially be obtained from the filter and the frequency divider. For example, in the case of using a first order filter, $\pi/2$ phase shift can only be obtained at infinite frequency. Therefore, $\pi/4$ phase shift can be obtained from the frequency divider and the remaining $\pi/4$ phase shift can be obtained from the RC filter. This means that the RC filter fixes the oscillation frequency to the frequency at which it exhibits a phase shift of $\pi/4$.

3.3 The Architectural Selection

Considering the theory explained in section 3.2, several varieties of the RC networks in figure 3.2.1 can be employed. A passive mixer (shown in figure 3.3.1) is chosen due to power considerations and a 1^{st} order RC network is chosen for simplicity. However, employing such a filter requires the use of a frequency divider as explained in section 3.2.

Possible topologies are shown in figure 3.3.2, 3.3.3 and 3.3.4. After reviewing the advantages and disadvantages of each topology, the most appropriate one is selected for further analysis and implementation.

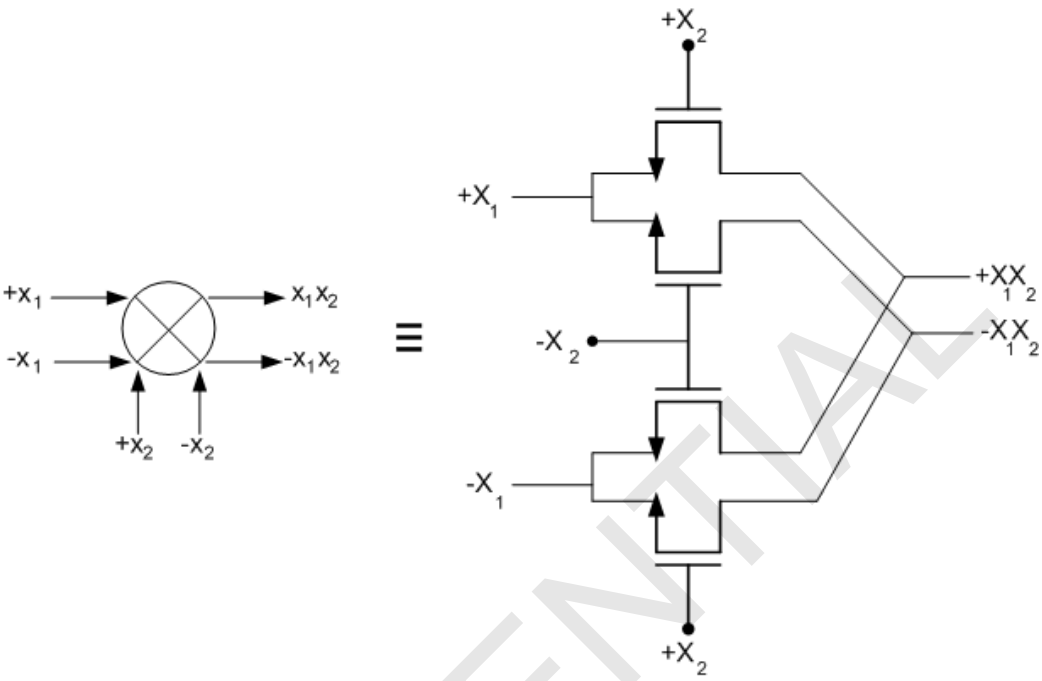

Figure 3.3.1: A differential passive mixer

In figure 3.3.2, the RC network provides an output signal in voltage domain. This signal is multiplied by the reference signal and integrated by an RC integrator.

In figure 3.3.3, the RC network provides an output signal in current domain. This signal is multiplied by the reference signal and integrated by the integrator capacitor.

In figure 3.3.4, the RC network provides an output signal in voltage domain. The voltage domain signal is converted to current domain by means of using a g_m stage. The output of the g_m stage is multiplied by the reference signal and integrated by the integrator capacitor.

Comparing the topologies in figure 3.3.2, 3.3.3 and 3.3.4, the one in figure 3.3.4 is the worst choice. First, using an additional g_m stage is not a power efficient solution. Second, using a g_m stage causes additional frequency error due to its phase shift. The main difference between the figure 3.3.2 and 3.3.3 is that, in figure 3.3.2 an RC integrator is employed and the voltage-to-current conversion of the signal is operated by the integrator resistor R_{int}, while in figure 3.3.3 this conversion is operated by the RC network itself. The disadvantage of the topology in figure 3.3.2 is that R_{int} alters the effective resistance of the filter and so alters the oscillation frequency. In addition, the mixer has to handle a considerable voltage swing which depends on the

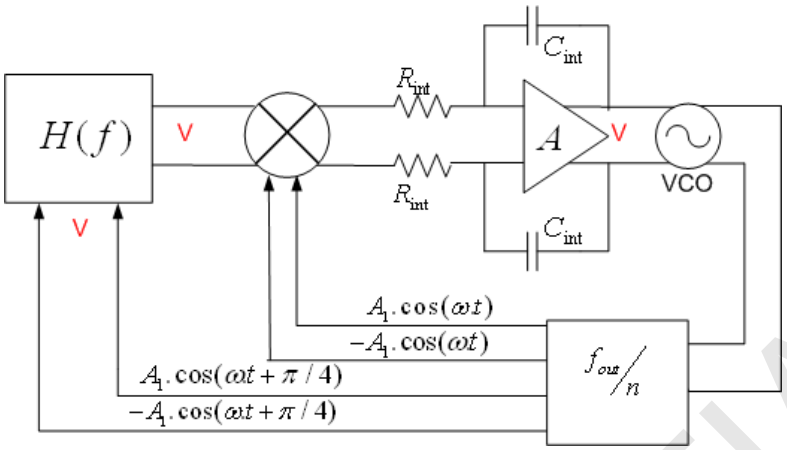

Figure 3.3.2: The First Possible Topology

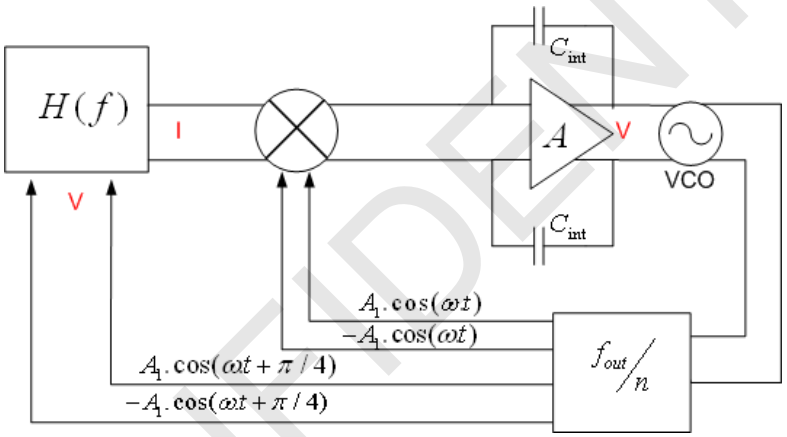

Figure 3.3.3: The Second Possible Topology

filter resistance. In figure 3.3.3, the mixer is directly located at the input of the integrator, i.e. which is ideally the virtual ground node. This provides a more stable mixer operation since the signal amplitude is small at this location.

3.4 Oscillation Frequency

Due to the advantages explained in section 3.3, the topology shown in figure 3.3.3 is simulated using the 1^{st} order RC filter shown in figure 3.4.1.

In order to calculate the oscillation frequency, it is important to remember that the average value of the signal at the input of the integrator is zero at steady-state due to the negative feedback loop as described in section

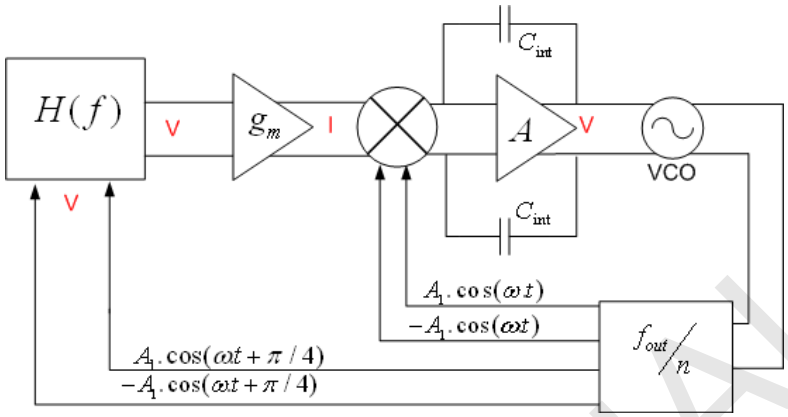

Figure 3.3.4: The Third Possible Topology

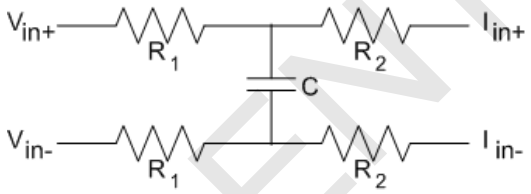

Figure 3.4.1: A 1^{st} order RC filter

3.2. The integrator input signal is shown in figure 3.4.2. Considering the oscillation condition, the area under one oscillation period should be equal to zero on average. This results in the following equation:

$$f_{out} = \frac{0.926}{2.\pi.R.C} \tag{3.4.1}$$

where C is the capacitor in the filter, R is the equivalent resistor, which is $(R_1 \| R_2)$.

A detailed calculation of the oscillation frequency is shown in appendix A.1. The frequency can be observed from the waveform of the integrated current in figure 3.4.2. Due to the mixing action, the frequency is doubled as explained in section 3.2.

As explained in section 3.2, in the case of using the 1^{st} order filter, the loop locks at the frequency where there is a $\pi/4$ phase shift in the filter. Since the phase of the 1^{st} order filter is shifted by $\pi/4$ in the -3 dB frequency, the oscillation frequency is estimated as $1/2\pi$RC. However, the calculation shown in appendix A.1 provides an accurate estimation.

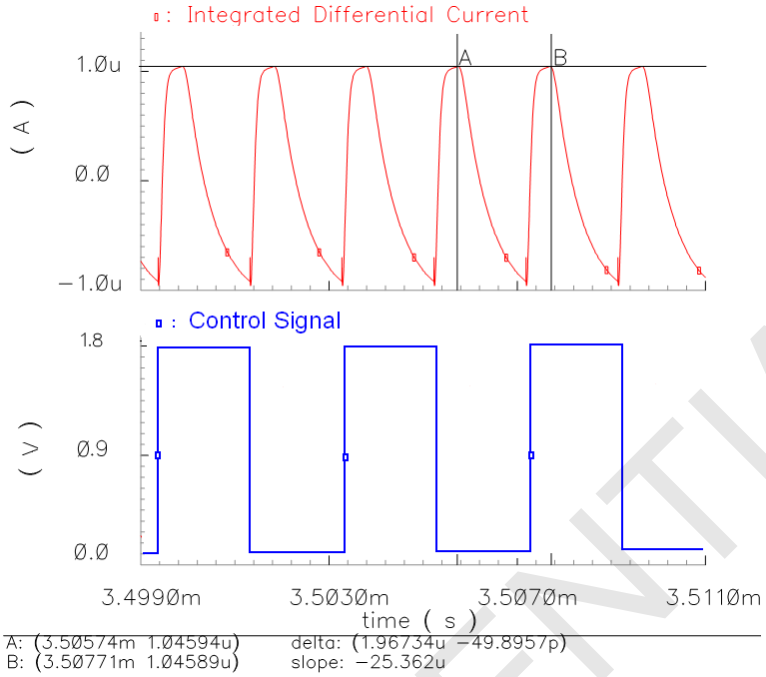

Figure 3.4.2: The signal waveform at the integrator input

3.5 Source of Errors

In this section, using the topology in figure 3.3.3 and the RC network in figure 3.4.1, the oscillation frequency error due to the following building blocks are investigated: the RC network, the mixer, the integrator opamp and the frequency divider.

3.5.1 The RC network

In 0.16 μm technology, the integrated resistors and capacitors are expected to deviate approximately $\pm 20\%$. Therefore, in order to obtain the same reference frequency from all of the fabricated chips, at least one of those circuit elements has to be trimmed. After trimming, the frequency is expected to deviate by temperature only due to the temperature coefficients of the resistor and capacitor.

The phase-frequency graph that is shown in figure 3.5.1 belongs to the network in figure 3.4.1 where $R_1 = 30$ kΩ, $R_2 = 1$ MΩ and $C = 10$ pF . The slope of the curve shown in figure 3.5.1 is a parameter that is used to convert any phase error into frequency error. This information is used in section 4.3. The corner frequency of the filter, where $\pi/4$ phase shift is obtained, is

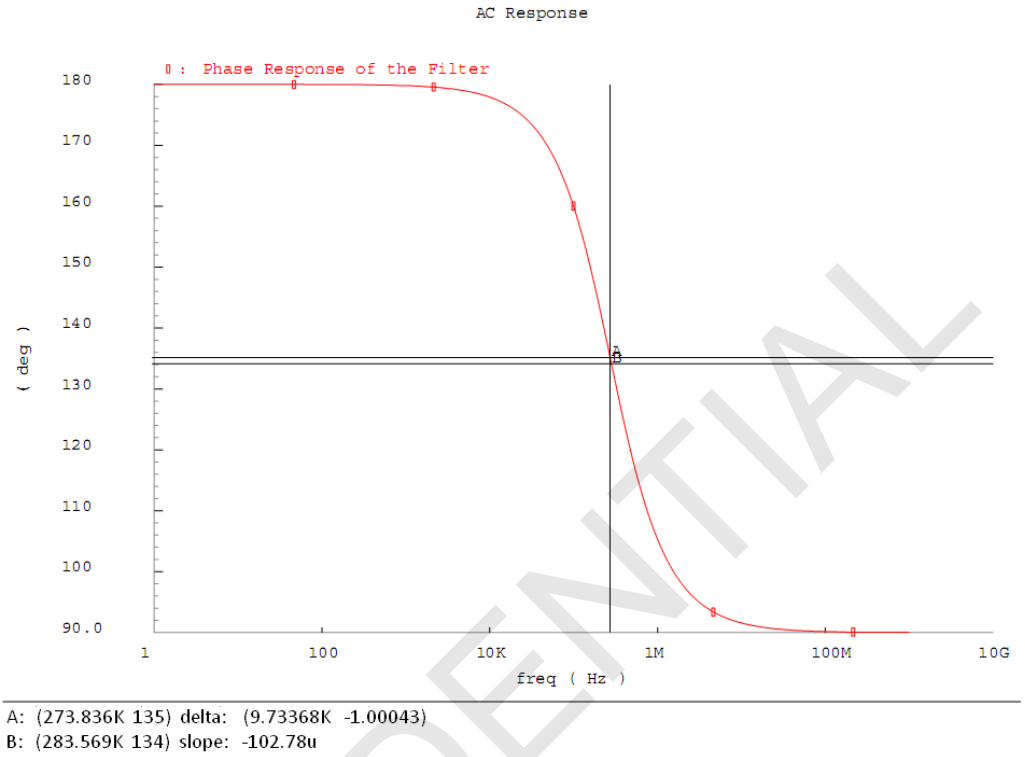

Figure 3.5.1: Phase-frequency response of a 1st order RC filter

approximately 273 kHz. As explained in section 3.2, the loop is locked at the frequency that gives $\pi/4$ phase shift in the filter. However, as analyzed in section 3.4, a factor of approximately 0.926 times of this frequency is expected from the oscillation, which is approximately 253 kHz.

3.5.2 The mixer

The on resistance and the mismatch of the mixer transistors are the two main error sources that cause a frequency deviation. On resistance of the mixer is added in series to the resistor in the RC network, affecting the transfer function of the filter and consequently the output frequency. Even though the filter needs to be trimmed due to the reasons explained in the previous section, the temperature coefficient of the on resistance is much more than that of the filter elements. Since the system is differential, due to the mismatch of the mixer transistors, the charge injection mismatch acts as an offset current in the system. This offset current is integrated by the integrator and causes frequency deviation, as well. In system level simulations, the effect

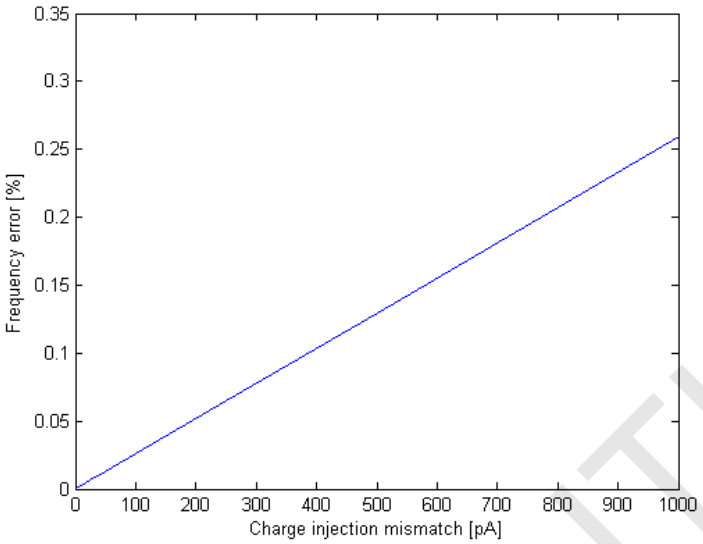

Figure 3.5.2: Frequency deviation vs charge injection mismatch

of the charge injection is simulated by injecting a DC current from one of the integrator inputs. The results are shown in figure 3.5.2.

In chapter 4, both effects are analyzed, and the frequency deviation due to both error sources will be minimized.

3.5.3 Integrator opamp

The offset and the limited gain of the integrator are two of the main error sources that cause a deviation in the frequency reference.

The effect of the offset can be explained in the simplified block diagram in figure 3.5.3, where H(f) is the transfer function of the RC network, V_{os} is the input referred offset voltage of the opamp, V_{bias} is the bias voltage of the opamp input. In the case of V_{os}=0 the current flowing through the branches are I_1 and -I_1. However due to the offset voltage an error current ($\triangle$I) is generated. The generated error current is integrated by the integrator and deviates the control voltage of the oscillator and consequently the frequency. The relation between the offset voltage and the frequency deviation is analyzed in appendix A.2. From the analysis, it is concluded that the frequency error is directly related to the ratio of the offset voltage and the filter driver voltage, rather than the absolute value of the offset voltage ($\triangle f \propto V_{os}/V_{dd}$). The frequency error due to the offset voltage is shown in figure A.2. The filter driver voltage is considered as 1.2 V.

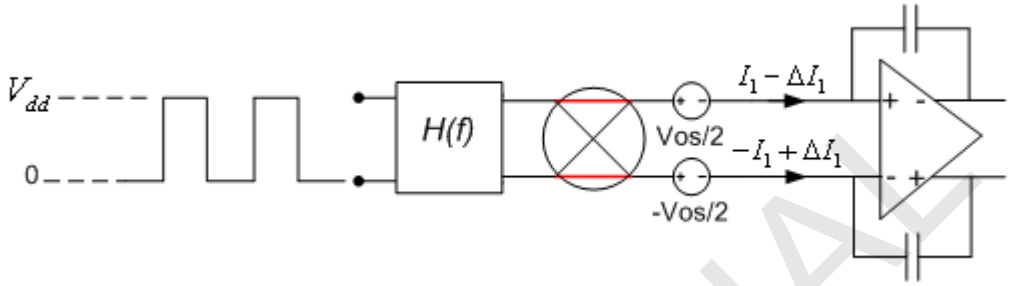

Figure 3.5.3: The effect of the offset voltage

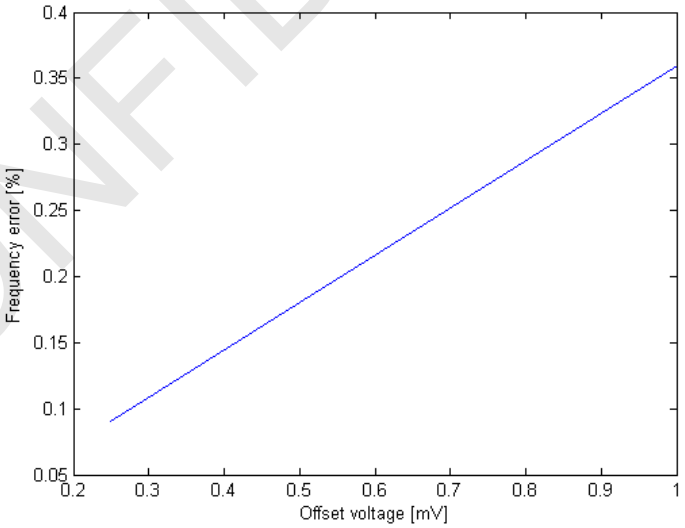

Figure 3.5.4: Frequency error due to offset voltage of the opamp

The effect of the open loop DC gain of the integrator can be analyzed as follows: considering that the loop is stable and the differential output signal of the integrator is 1 V, employing a 60 dB integrator opamp means to have 1 mV differential input signal. Therefore, using 60 dB integrator is expected to have the same effect of having an integrator opamp with 1 mV input referred offset voltage.

As mentioned in section 3.2, the oscillation frequency is locked when the DC term, which is the output of the mixer is integrated by the integrator. Since the integrator is not ideal, the second order harmonic which is shown in equation (3.2.2) will only partially be filtered out by the integrator capacitor. Therefore, there is a residual ripple that makes the oscillation frequency fluctuate. This fluctuation is aimed to be around one tenth of the targeted frequency accuracy which is around 0.03%.

3.5.4 Frequency divider

The frequency divider is used to generate a $\pi/4$ degree phase difference between the outputs of the divider and any mismatch in the circuitry manifests itselft as a phase error. This phase error is converted into frequency error by the transfer function shown in figure 3.5.1. In a first order filter, 1^o phase error gives 9.73 kHz frequency error. Considering that the oscillation period is 4 μs, if the mismatch is 1 ns, this gives 0.09^o phase difference and 0.87 kHz frequency error which is 0.34%. In the digital circuits, the 3σ error spread, e.g. both temperature and process, can be expected up to 50% of 1 ns. Therefore, after trimming 0.17% frequency error can be expected.

3.6 Initial Budget

Considering the error sources investigated in this chapter, an initial error budget that is shown in table 3.2 is prepared. In the error budget, the opamp offset is kept as the dominant source.

Contributors	Value	Frequency error [%]
Opamp offset	200 μV	0.074
Opamp gain	80 dB	0.035
Mixer charge injection	100 pA	0.026
Divider mismatch	0.05 ns	0.017
	Total	0.15

Table 3.2: Initial error budget

Chapter 4

Implementation

In the previous chapter, a new locked oscillator topology, its building blocks and non-idealities are introduced and based on the non-idealities an initial error budget is sketched. In this chapter, these building blocks are designed and analyzed in more details.

4.1 RC Network

4.1.1 Integrated Resistors and Capacitors

In 0.16 μm CMOS process, N+Active, N-well and N-poly resistors are available. However, N+Active and N-well resistors are not preferred because of their high-voltage-dependent temperature coefficients. The advantage of using N-poly resistor is its small 1^{st} and 2^{nd} order temperature coefficients. An N-poly resistor has a negative 1^{st} order and a positive 2^{nd} order temperature coefficient. The temperature behavior of a 60 kΩ N-poly resistor has been simulated and it is shown in figure 4.1.1. It has an average temperature coefficient of -90 ppm/^{o}C. In literature ([7, 9]), the temperature coefficient of an N-poly resistor is compensated by putting it in series with a P-poly resistor. However, P-poly resistor is not available.

In this process, metal-insulator-metal (MIM), fringe and MOS capacitors are commonly used integrated capacitors, since the others require extra process steps. MOS capacitor is not preferred because of it has a high temperature coefficient and its value is strongly process dependent. Among the remaining two alternatives, fringe capacitor is preferred because of its symmetric structure. A fringe capacitor consists of stacked finger-shaped metal areas and takes advantage of the capacitance between the fingers [14]. Since the capacitance seen from the both plates of the capacitor is the same, using

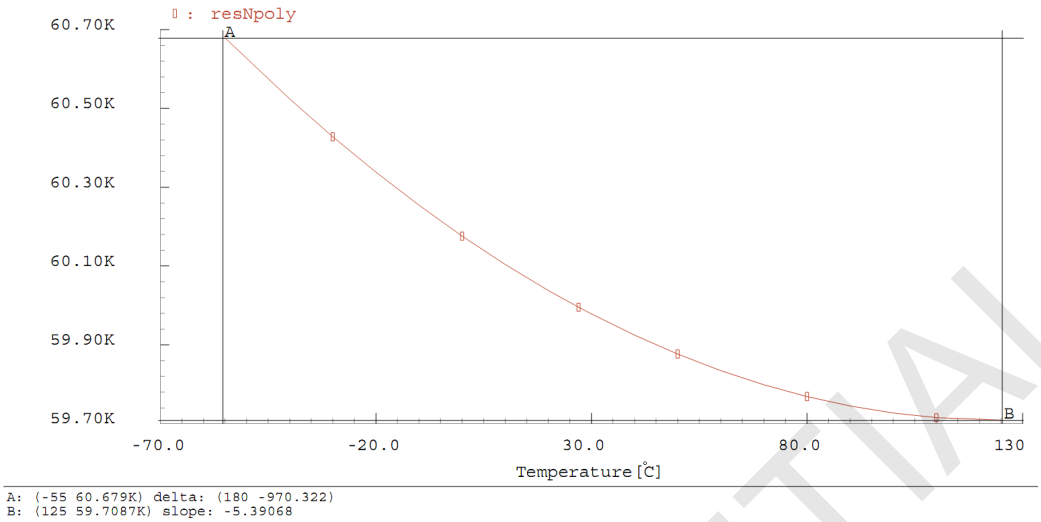

Figure 4.1.1: The variation of 60 kΩ resistor as a function of temperature

one fringe capacitor is sufficient in a first order filter, as it is shown in figure 3.4.1. Besides, since 0.16 μm CMOS process provides 6-metal layers, the capacitance per unit area is comparable to that of the MIM capacitors which are widely used in the literature [7, 8, 9]. The temperature behavior of a 10 pF fringe capacitor has been simulated and it is shown in figure 4.1.2. A fringe capacitor has an average temperature coefficient of +60 ppm/^{o}C. Its positive temperature coefficient is useful to compensate the that of the N-poly resistor. The corner frequency (f_{corner}=1/RC) of a low pass filter, that consists of a fringe capacitor and a N-poly resistor, is plotted as a function of temperature in figure 4.1.3. The average temperature coefficient of the frequency is +32 ppm/^{o}C.

4.1.2 Topology Selection

The proposed RC network topology is shown in figure 4.1.4. In this topology the frequency is determined by $(R_1 \parallel R_2)C$. The main filter capacitor (C) should be chosen in the order of 1 pF not to be dominated by the parasitic capacitances. In order to keep the oscillation frequency at the desired level (250 kHz) the filter resistance should be chosen in the order of 10 kΩ. However, using such a small resistor causes the output signal amplitude to be in the order of 0.1 mA, considering that the input voltage is 1.2 V. The output signal of the filter is integrated by the integrator and controls the output frequency of the VCO. Therefore, any fluctuation in the control signal of the VCO is turned into fluctuations in the output frequency. Using R_2 in

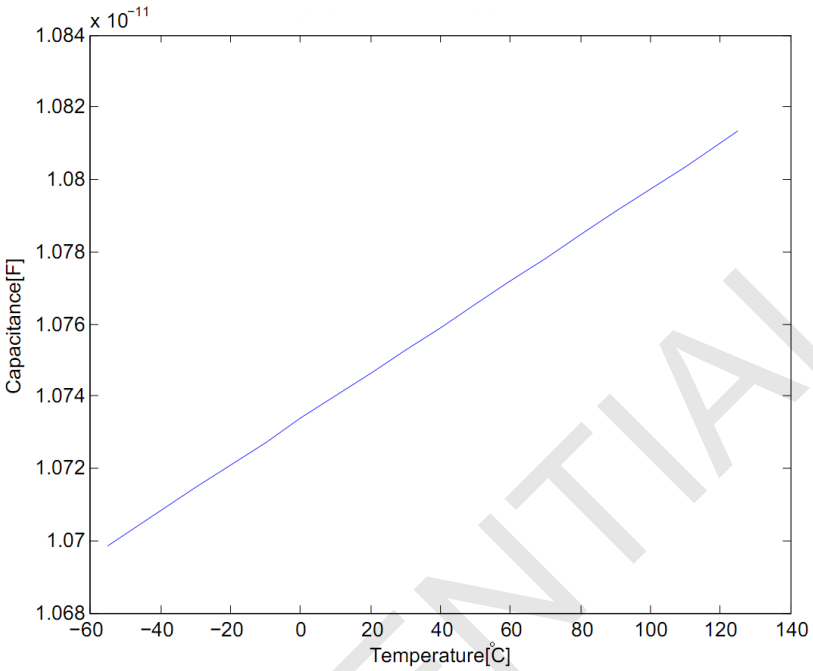

Figure 4.1.2: The variation of 10 pF capacitor as a function of temperature

the filter helps to set the ripple amplitude of the signal that controls the VCO. Considering that R_1 is much smaller than R_2, R_2 does not have much influence on the frequency and therefore does not need to be trimmed.

Due to the process spread, all the values of the filter elements and consequently the frequency are expected to drift from the desired level. By trimming some of the elements at room temperature, the frequency is set back to the desired level. According to the calculations shown in appendix A.3, considering only the process spread of the poly resistor and fringe capacitor, to obtain a frequency resolution of ±0.05%, 10 bit trimming is required. To make the trimming structure simpler, both R_1 and C_1 are trimmed at room temperature. R_1 is used for the coarse and C_1 for the fine tuning of the filter. To ensure that the coarse tuning steps are overlapping as shown in figure 4.1.5, totally 13 bits are used. Overlapping of the coarse steps is necessary to ensure that the frequency range is covered totally. For the coarse tuning, a 5 bit resistor trimming, and for the fine tuning a 8 bit capacitor trimming is used. The reason of restricting the capacitor trimming by 8 bits is to use unit capacitors that are not very sensitive to parasitics and to limit the silicon area occupied by the filter. As shown in section 4.7, the filter area is mainly consumed by the trimmable capacitors and it is almost the one third of the total chip area. The total system has a wide (±50%) tuning

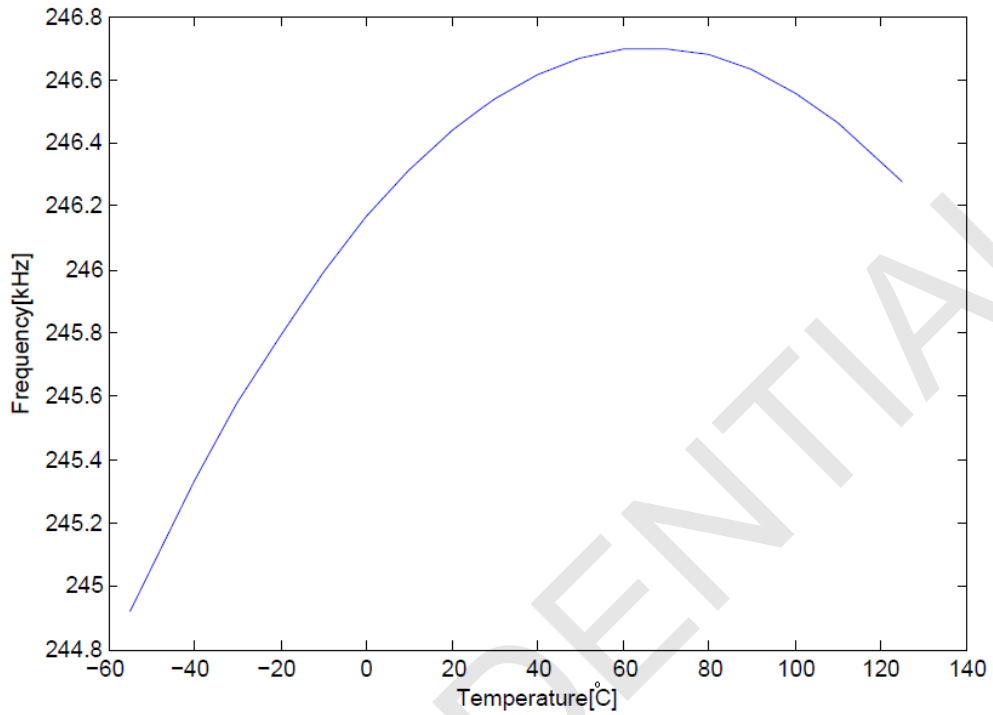

Figure 4.1.3: The variation of the corner frequency of a 1^{st} order RC filter

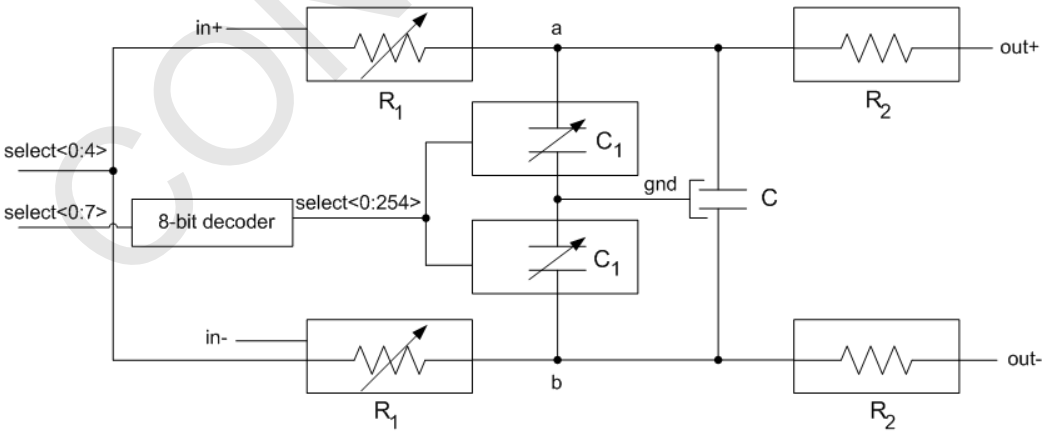

Figure 4.1.4: The proposed RC network topology

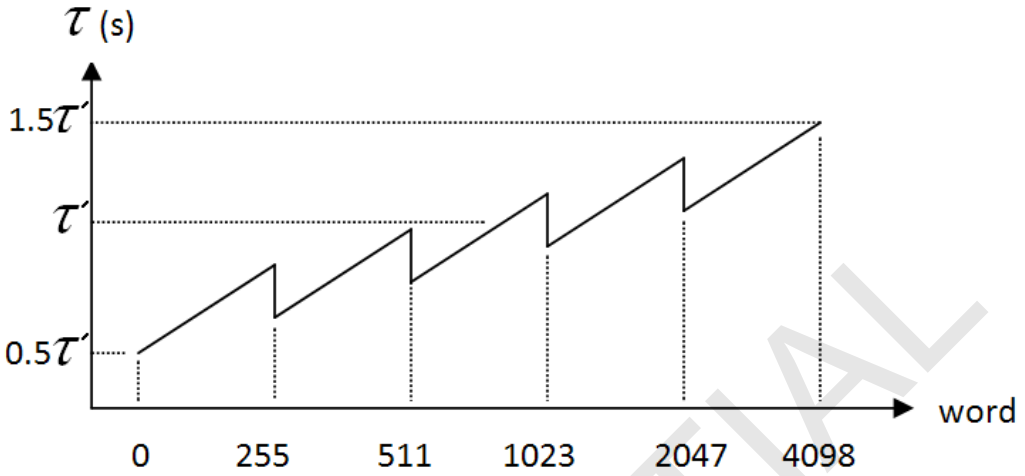

Figure 4.1.5: The trimming strategy of the RC network

range as shown in figure 4.1.5.

The trimmable capacitor (C_1) is shown in figure 4.1.6. It consists of 255 unit capacitors and transistors. One plate of the capacitor is connected to the signal paths, a or b, and the other one is connected to the drain of the transistor MN. Select signal is used to activate the capacitors by means of turning on and off the transistors.

The trimmable resistor (R_1) is shown in figure 4.1.7. As mentioned before, 5 bits are used for the coarse tuning of the filter. Therefore, in addition to the main resistor (R), 5 more branches that consist of unit resistors (R_u) are employed. The three-state buffer in figure 4.1.8 drives the filter. A three-state buffer is a buffer with an additional enable signal. If the enable signal is high, the input signal is observed at the output. If the enable signal is low, the output of the buffer becomes high impedance. Before the output stage of the three-state buffer, two D-flip-flops (D-FFs) are used. The reason for using these flip-flops (FFs) is to synchronize the signal that is coming from the output of the frequency divider. By means of synchronization, the delay contribution of the three-state buffer, which causes the oscillation frequency to deviate as described in section 3.5.4, is mostly eliminated. The output stage of the three-state buffer is sized such that the frequency error introduced due to the limited on-resistance is minimized. The resistance and capacitance values that are used in this design are shown in table 4.1.

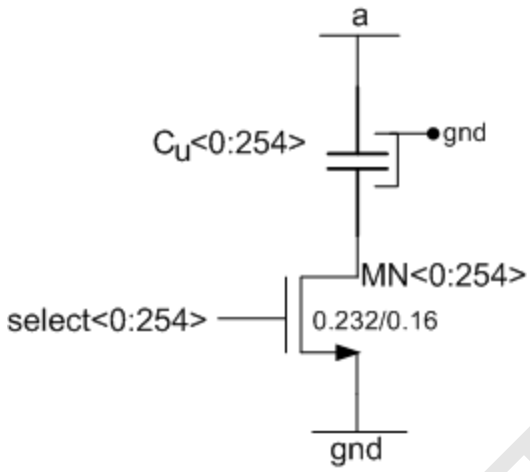

Figure 4.1.6: Trimmable fringe capacitors

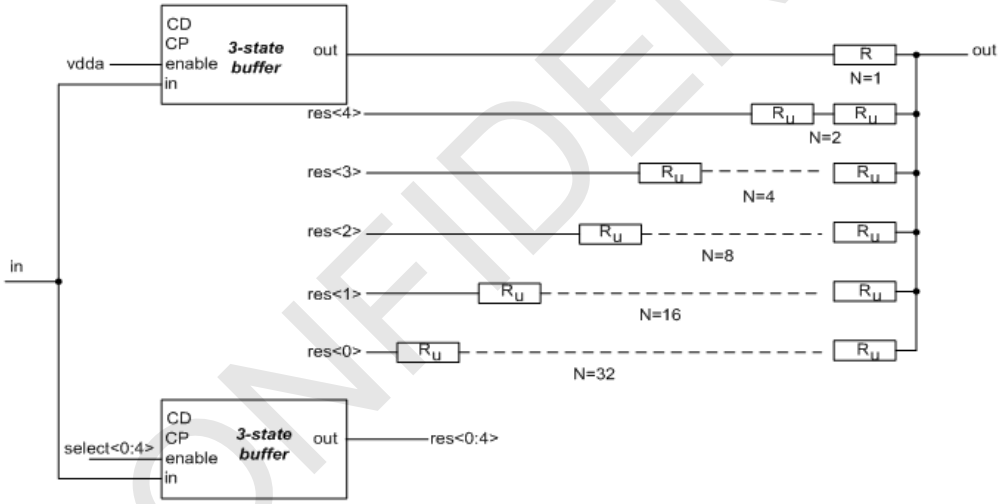

Figure 4.1.7: Trimmable resistor R_1 with reference to figure 4.1.4

Filter Elements		Values
R_1	R	30 kΩ
	R_u	30 kΩ
R_2		1 MΩ
C		10 pF
C_u		5.5 fF

Table 4.1: The resistor and capacitor values

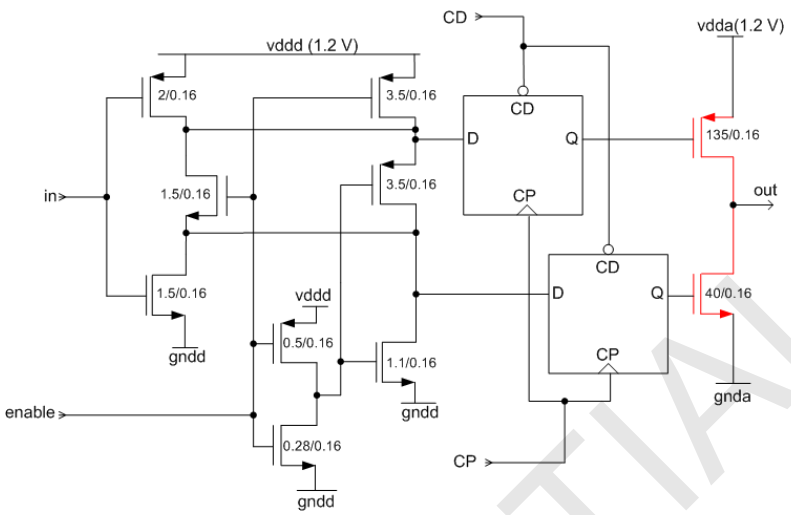

Figure 4.1.8: A synchronized 3-state-buffer

4.2 Mixer

The implemented mixer is shown in figure 4.2.1. $+x_1$ and $-x_1$ are the inputs, $+x_2$ and $-x_2$ are the control signals, $+x_1x_2$ and $-x_1x_2$ are the outputs of the mixer. The inputs of the mixer are connected to the output of the RC filter. The control signals are driven by the output stage of the frequency divider. The outputs are connected to the differential input pair of the integrator opamp.

4.2.1 Switching Non-idealities

An ideal switch behaves as follows: when it is open, the impedance is infinite and when it is closed, the impedance is zero. Furthermore, there is no delay between the driving signal and the switching action. In reality a CMOS switch has a non-infinite impedance R_{off} when it is off and non-zero R_{on} impedance when it is on. Since the $+x_1$ and $-x_1$ are the output signals of the RC filter, as the current flows through the MOS switches, the R_{on} is added in series to the filter resistance. Therefore, the effective filter resistance is affected and the oscillation frequency is shifted. The on resistance of a MOS switch is calculated from the equation (4.2.1).

$$R_{on} = \frac{1}{(V_{gs} - V_t).\beta} \tag{4.2.1}$$

with,

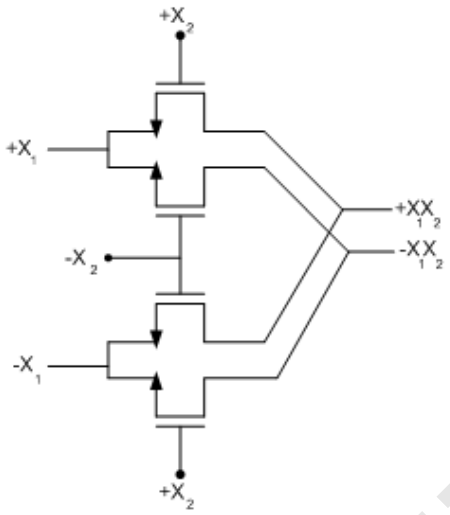

Figure 4.2.1: Implemented differential mixer

$$\beta = \mu.C_{ox}.\frac{W}{L} \tag{4.2.2}$$

where μ is the mobility, C_{ox} is the gate oxide capacitance per unit area, W is the width and L is the length of the transistor.

From equations (4.2.1) and (4.2.2), to minimize the on resistance of the switch, the aspect ratio of the transistor and the overdrive voltage should be maximized. Therefore, usually the minimum channel length transistors are used as switches. Besides, since the electron mobility of the NMOS transistors are higher than the hole mobility of PMOS transistors, on resistance of an NMOS switch is smaller than a PMOS switch that has the same dimensions. For a minimum size switch in a 0.16 μm process, simulations show that as V_{gs} decreases, R_{on} increases accordingly as expected from equation (4.2.1).

Secondly, there is a time delay between the control signals, $+x_2$ and $-x_2$, and the switching action mainly due to the relatively big capacitances of the control signal lines. To avoid the time differences between the lines, the layout should be done such that the lengths are as equal as possible. The other issue is the charge injection. The charge injection is mainly caused by two phenomena: parasitic capacitive feed-through and the redistribution of channel charge. When the switches are on, finite amount of charge is held in the channel. This charge can be expressed for a NMOS switch as:

$$q_{inj} = (V_{gs} - V_t).W.L.C_{ox} \tag{4.2.3}$$

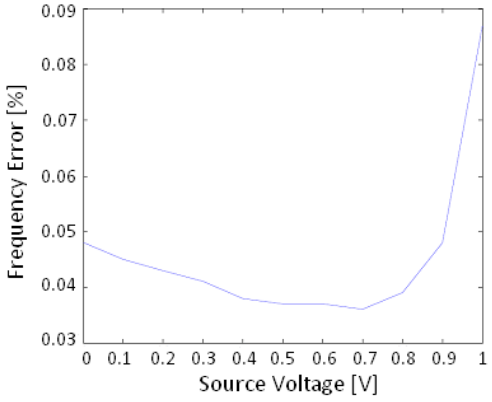

Figure 4.2.2: Source voltage vs frequency error

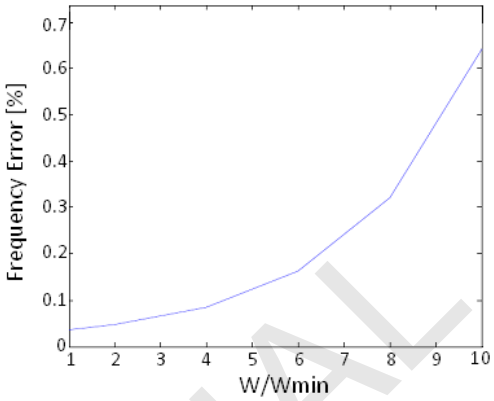

Figure 4.2.3: W/W$_{min}$ values vs frequency error

For a minimum size switch in a 0.16 μm process, the values that can be found are W = 0.232μm, L = 0.16μm, V$_t$ = 0.49 V, V$_{gs}$ = 1.8 V and C$_{ox}$ = 12.12 fF/μm^2 which leads to q$_{inj}$ = 0.59 fC.

This charge flows partially through both drain and source of the device when the switch is turned off. The relation between the injected current and charge is written as:

$$I_{inj} = q_{inj}.f_{clk} \tag{4.2.4}$$

where f$_{clk}$ is the frequency of the control signal.

Equation (4.2.4) implies that, as the clock frequency increases the charge injection effect becomes more dominant. Since the system is differential, only the differential charge injection or charge injection mismatches have an effect. When equation (4.2.3) is investigated, it can be concluded that W, L, C$_{ox}$ and V$_t$ mismatch leads to channel charge mismatch. Since the charge injection of a MOS transistor is proportional to the area, the minimum size switches are the best choice to minimize channel charge injection. Using dummy switches result in more charge injection mismatch, because the main switch will then be larger than minimum size [15].

To optimize the total error due to the charge injection mismatch and the on resistance, there are two design parameters: W and the source voltage V$_s$. The total frequency deviation due to both R$_{on}$ and the charge injection mismatch for different V$_s$ values are shown in figure 4.2.2. For this simulation, the minimum size switches are used (W = 0.232 μm, L = 0.16 μm). For the charge injection mismatch, 10% mismatch between the switches is assumed.

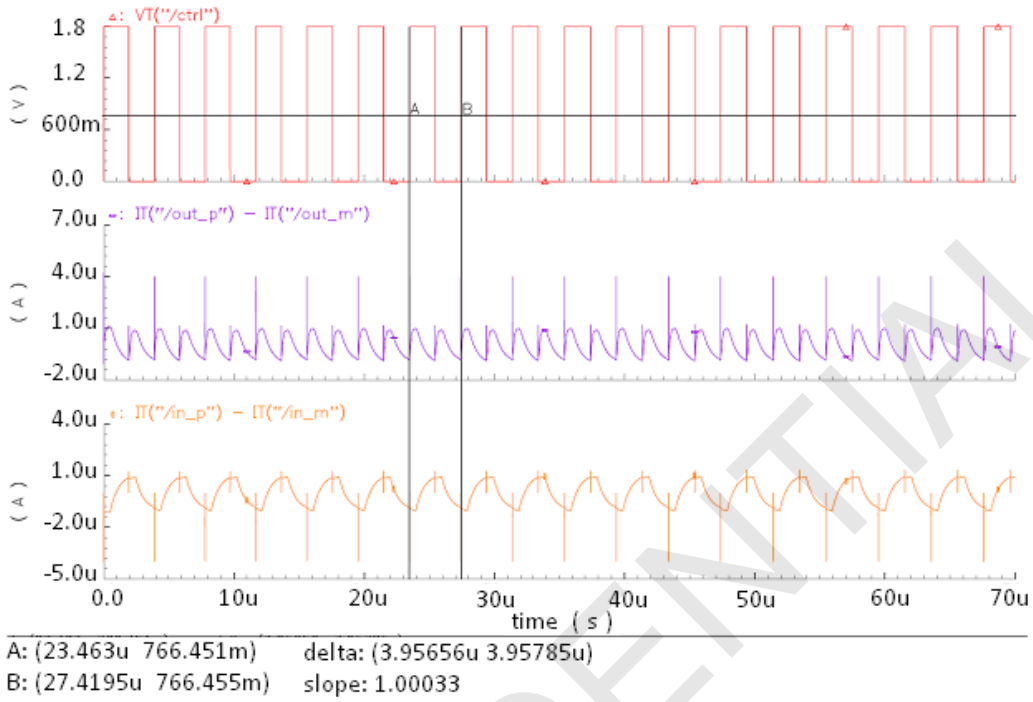

Figure 4.2.4: The transient response of the mixer

As seen from figure 4.2.2, choosing $V_s = 0.6$ V is nearly optimal solution. For $V_s = 0.6$ V, the frequency errors due to on resistance and charge injection mismatch for different W values are calculated and the total frequency errors are plotted in figure 4.2.3. The results are also verified by the simulations.

It can be concluded from figure 4.2.3 that choosing $W/W_{min} = 1$ gives the best compromise between the charge injection mismatch and on resistance of the switch. The frequency error expected from the mixer is 0.035%.

4.2.2 Simulations

The transient response of the mixer can be observed in figure 4.2.4. The transient response of the differential input and output signals of the mixer and the control signal are plotted. From figure 4.2.4, it is observed that while the differential input signal and the control signal have the same frequency, the differential output signal has the double frequency of the input signal.

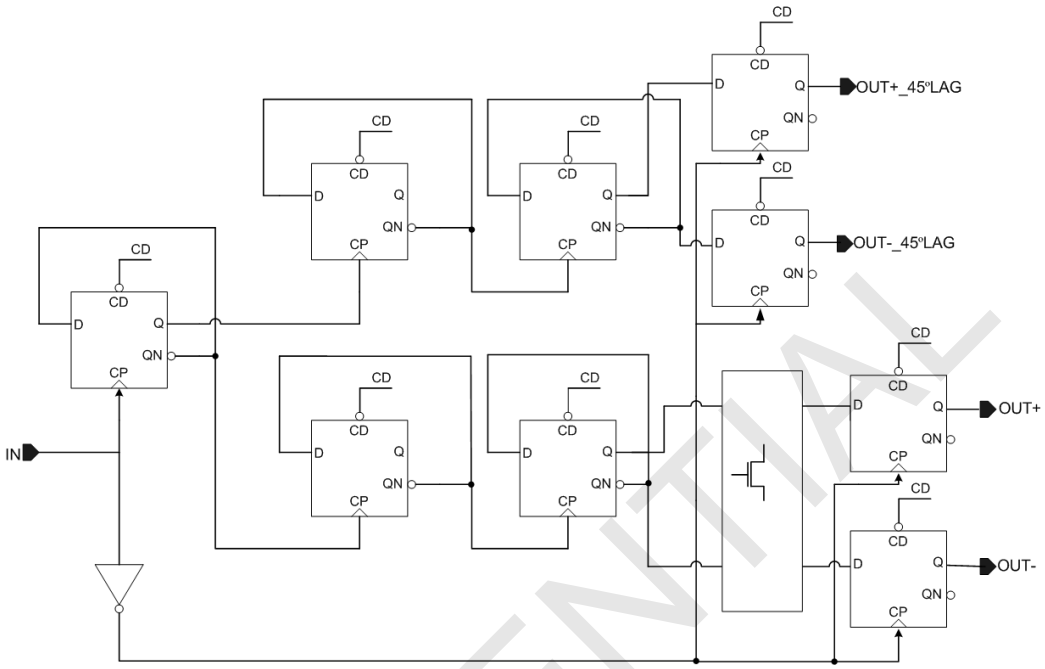

Figure 4.3.1: Frequency divider

4.3 Frequency Divider

As described in section 4.1, a frequency divider is required. The frequency divider is shown in figure 4.3.1 which generates a $\pi/4$ degree phase-shifted clock signal. To do this, the input frequency is divided by 8 by a chain of three D-FFs. Each D-FF divides the frequency by 2 and the last stage is used for synchronization. The outputs called "$OUT+\_45LAG$" and "$OUT-\_45LAG$" are the differential inputs of the mixer and "$OUT+$" and "$OUT-$" are the differential input of the three-state buffers.

Thanks to the synchronization with D-FF, the propagation delay mismatch of the D-FFs and of the connection lines and the additional propagation delay of the three-state buffers are cancelled. In table 4.2, it is observed that using synchronization provides approximately 10x improvement.

4.3.1 Simulations

The time domain simulations of the frequency divider shown is shown in figure 4.3.2. The frequency error due to the mismatches of the D-FFs are extracted from the time domain simulations is shown in figure 4.3.2. From the simulations, $\pi/4$ degree phase-shift between the output signals is observed.

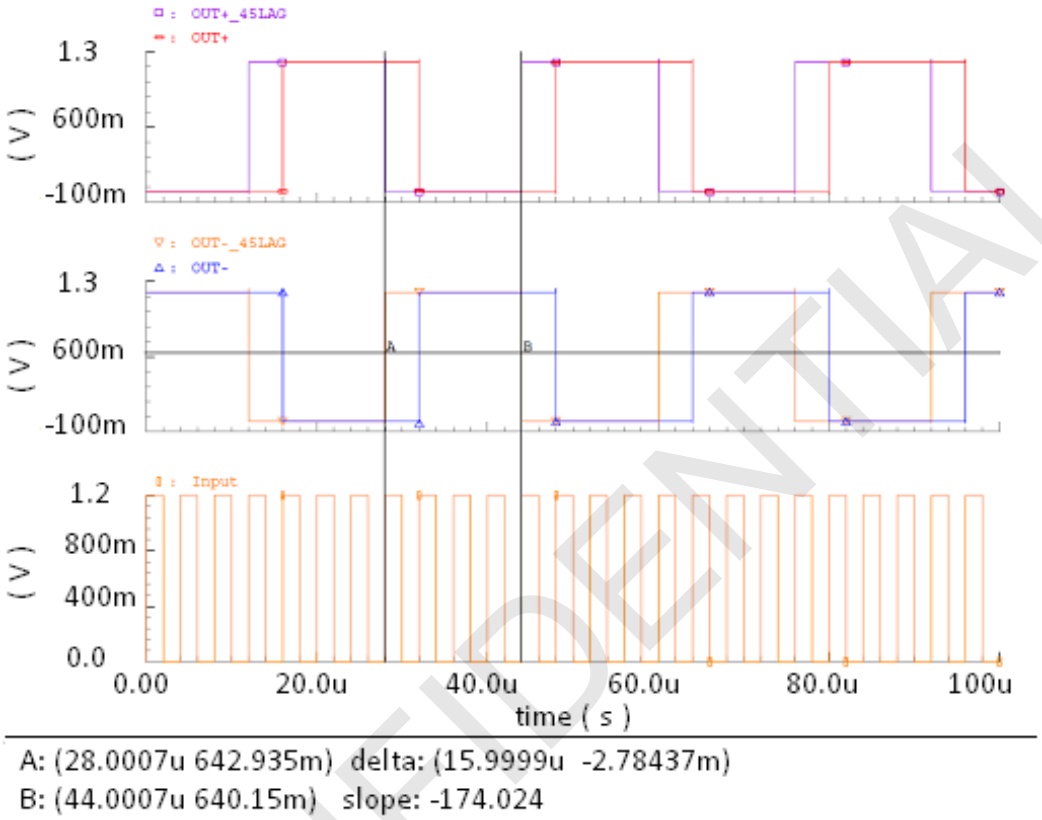

Figure 4.3.2: The timing diagram of the frequency divider

Temperature [^{o}C]	-55	27	125
3σ frequency error *without* synchronization [%]	0.063	0.064	0.068
3σ frequency error *with* synchronization [%]	0.0065	0.0066	0.007

Table 4.2: The frequency error (3σ) before and after synchronization

4.4 VCO

The function of the VCO is to provide the required oscillation frequency that is fixed by the RC filter. For this purpose, an existing relaxation oscillator has been adapted [16].

As shown in figure 4.4.1, the oscillator consists of a differental-to-single-ended converter, two current mirrors M_{15}- $M_A$and M_{15}- M_B, two capacitors C_A and C_B, a comparator and logic block. The drain current of M_{15} is mirrored to M_A and M_B. The capacitors, C_A and C_B, are alternatively precharged to V_{cap} and then linearly discharged by M_A and M_B. When the voltage on the discharging capacitor drops below V_{ref}, the output of the comparator switches and the linear discharge of the other capacitor starts immediately, while the recharge is delayed. The delay ensures that non-idealities of the comparator do not affect the slope of the discharge at the crossing of V_{ref} and it is not critical, as it does not influence the period T_{osc}. The delay signal and the signals driving the switches are generated by a digital circuit.

The frequency of the VCO is given by:

$$f_{osc} = \frac{(I + \Delta I)}{2C_{A,B}(V_{cap} - V_{ref})} \tag{4.4.1}$$

where V_{ref} and V_{cap} are reference voltages, C_A and C_B are the MOS capacitor operating in inversion, I is the current provided by M_4, ΔI is the current provided due to differential input voltage and the g_m of the differential-to-single-ended converter.

The main modification is designing a circuit that converts the differential input signal, which is the output of the integrator, into the circuit used in the relaxation oscillator to charge and discharge the capacitors. The designed circuit is shown in figure 4.4.2. The difference in the input voltages is converted to current by the differential pair $M_{9,10}$ and mirrored by transistors $M_{11,12}$, $M_{5,6}$ and $M_{13,14}$. The output current is taken from the drain of M_6 and M_{14}. This stage sets the gain of the VCO, which is a function of the g_m of the input pair. Transistor M_4 adds a constant current (1.4 μA) which keeps the free running frequency of the VCO around 1.8 MHz by means of charging the MOS capacitors C_A and C_B which are approximately 0.9 pF.

In section 3.5.3, it is explained that a ripple signal at the double frequency of the oscillation frequency is generated by the mixer and filtered out by the integrator. Since the output of the integrator is the control signal of the VCO, the residual ripple in the control signal causes a fluctuation at the output frequency. To reduce this effect, the input pair is degenerated by the

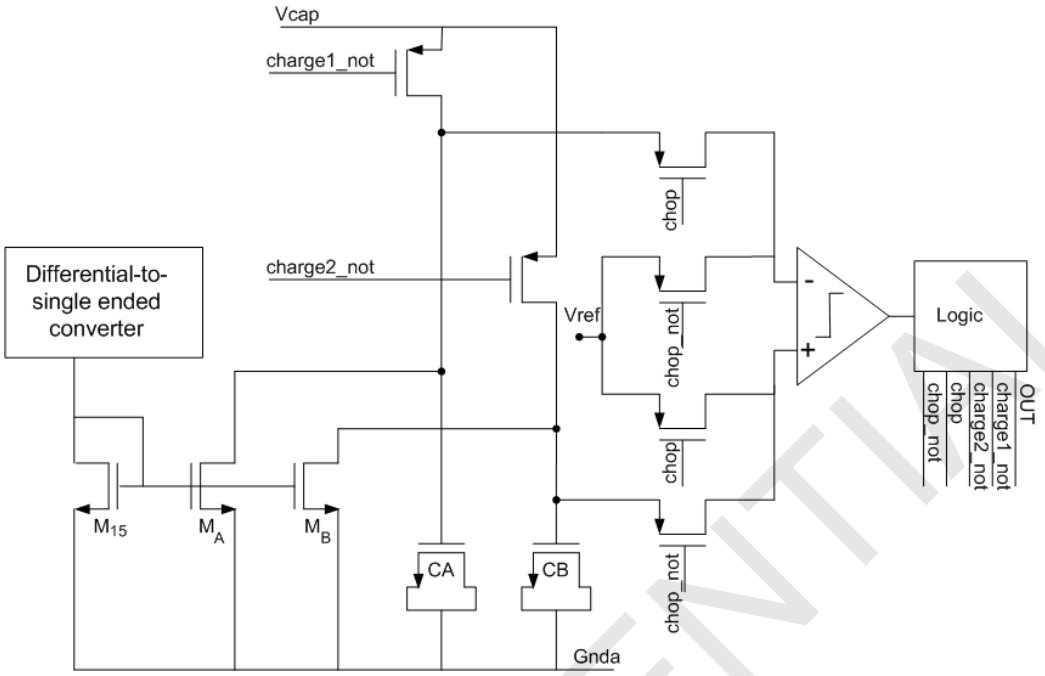

Figure 4.4.1: The topology of the relaxation oscillator

transistors M_7 and M_8. The degenerated input pair has an effective g_m of 0.1 μS and provides 5 dB filtering.

4.4.1 Simulations

The frequency variation at the output of the VCO for different control voltages, due to the temperature and process variations is shown in figure 4.4.3. The variation is mainly due to the variation of the MOS capacitor and the g_m of the input pair. The free running frequency of the VCO is 228 kHz. Therefore, as observed from figure 4.4.3, in order to ensure that the VCO is able to provide the sufficient oscillation frequency to lock the loop, the integrator opamp should have ± 0.9 V output swing. The signal waveforms at the gate of the MOS capacitors M_A and M_B is shown in figure 4.4.4.

The effect of the residual ripple can be observed from figure 4.4.5. The frequency ripple due to this signal is ±0.036%. To reduce the frequency ripple to this level, 50 pF integration capacitor is used.

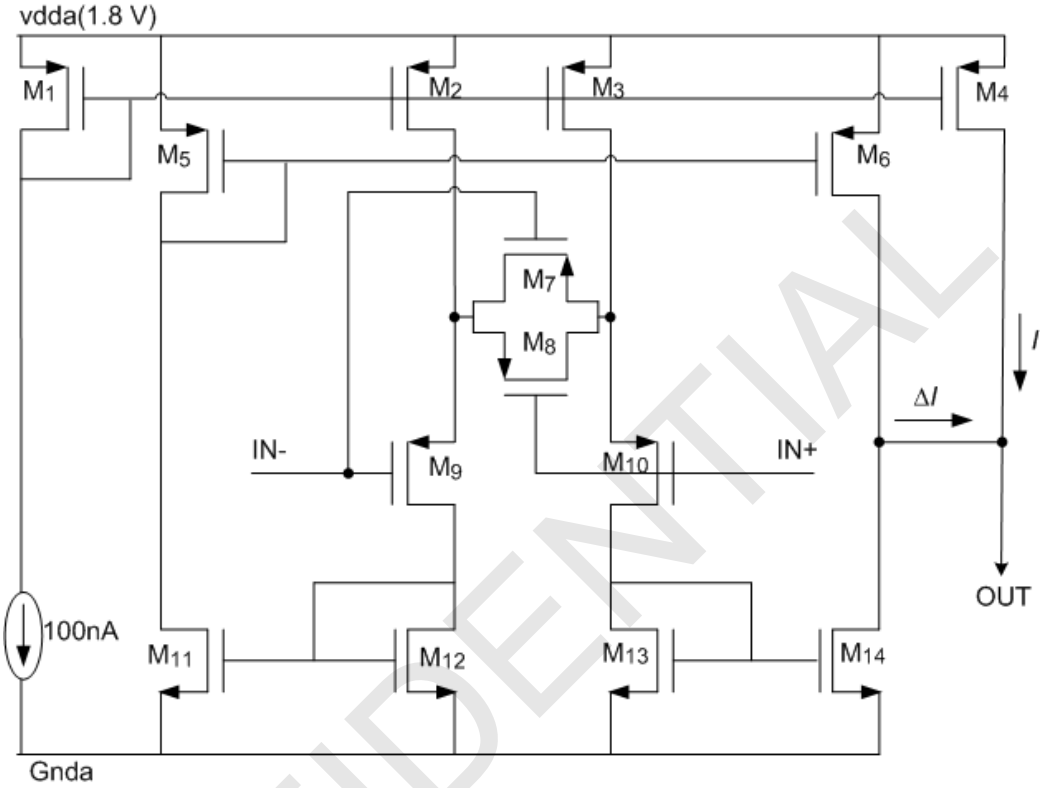

Figure 4.4.2: Differential-to-single-ended converter

MOSFET	W [μm]	L [μm]	I_{DS} [μA]	g_m [μS]
M_1	1.5	5	0.1	1.4
$M_{2,3}$	1.5[2]	5	0.2	2.8
M_4	1.5[14]	5	1.4	19.8
$M_{5,6}$	0.5	20	0.1	0.5
$M_{7,8}$	0.25	40	0	0
$M_{9,10}$	0.25[2]	10	0.2	0.9
$M_{11,14}$	0.3	20	0.1	0.8
$M_{12,13}$	0.3[2]	20	0.2	1.6

Table 4.3: Transistor dimensioning of the differential-to-single-ended converter

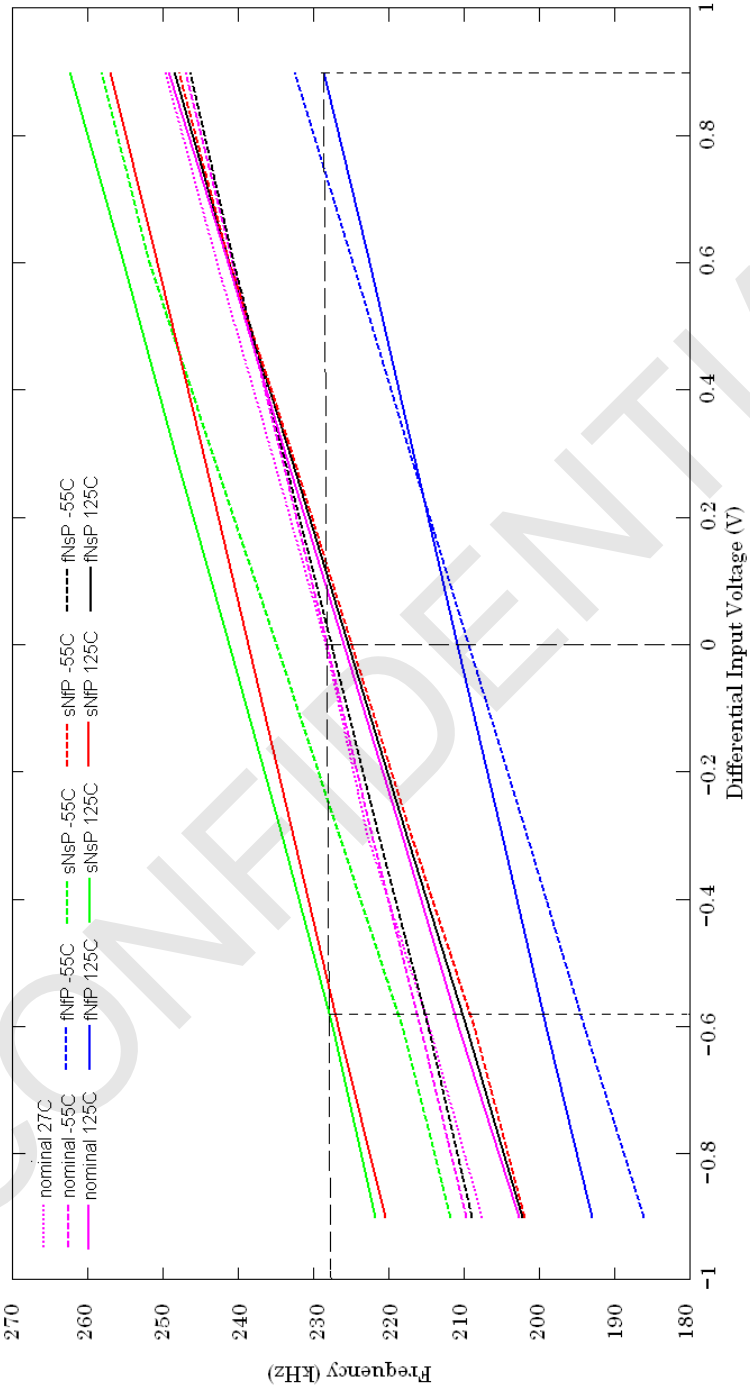

Figure 4.4.3: VCO frequency under various input voltages

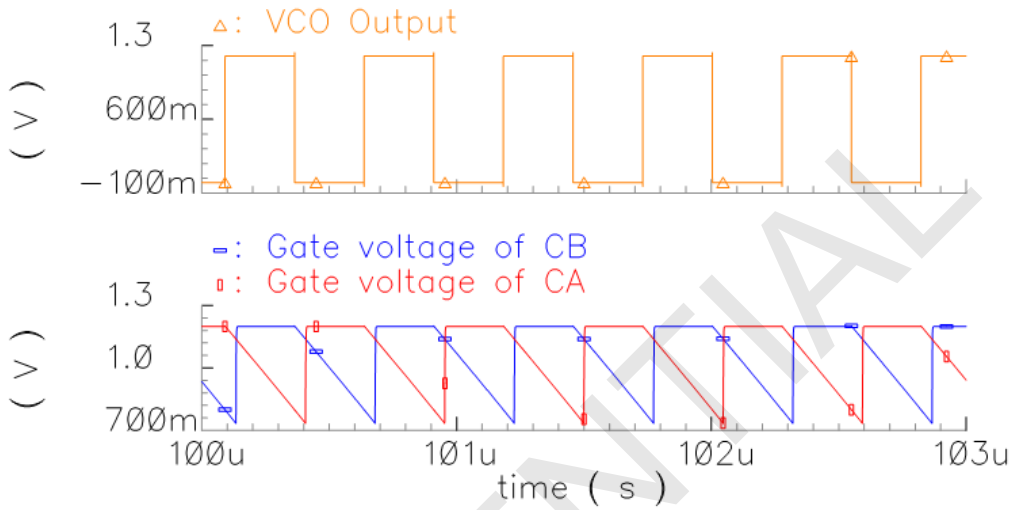

Figure 4.4.4: The signal waveforms of the main nodes of the VCO

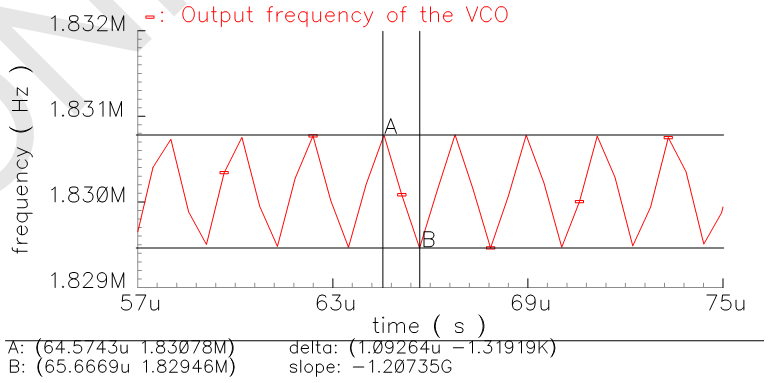

Figure 4.4.5: Output frequency ripple of the VCO under nominal conditions

4.5 Integrator

4.5.1 Design

In section 4.4, it is shown that due to the process and temperature variations of the VCO, the output stage of the opamp should have a ±0.9 V output swing. In section 3.5, it is mentioned that the opamp should have 80 dB gain and maximum 200 μV offset at all process corners. In section 4.2, it is emphasized that to minimize the frequency error due to mixer, the input transistors of the opamp should be biased at 0.6 V. All these requirements can be met using a well-known folded cascode opamp that employs a PMOS input transistor. The topology that is used in this design is shown in figure 4.5.1.

Since the opamp is fully differential, the output voltage must be controlled by a CMFB circuit. For this purpose, a set of two long-tail pairs are used. The long tail-pairs M_{22}, M_{23} and M_{24}, M_{25} are connected with their gates between the desired common mode voltage level (V_{CMFB}) and each of the output terminals V_{out+} and V_{out-}. The sum of the output currents of the transistors M_{23} and M_{24} controls the common-mode output voltage through M_{27}, M_{18} and M_{19}. To improve the stability of the CMFB circuit, the current sink transistors of the opamp is separated into two branches [12].

As mentioned in section 3.5, the most important design specification is the offset. Therefore, it is useful to analyze how to reduce the offset voltage of a folded cascode using the equation (4.5.1) [15]:

$$V_{os} = \triangle V_{T(8,9)} + g_{m(10,11)}\frac{\triangle V_{T(10,11)}}{g_{m(8,9)}} + g_{m(16,17)}\frac{\triangle V_{T(16,17)}}{g_{m(8,9)}} + g_{m(18,19)}\frac{\triangle V_{T(18,19)}}{g_{m(8,9)}} + \frac{I_{(8,9)}}{g_{m(8,9)}}\left(\frac{\triangle \beta_{(8,9)}}{\beta_{(8,9)}} + \frac{\triangle \beta_{(10,11)}}{\beta_{(10,11)}} + \frac{\triangle \beta_{(16,17)}}{\beta_{(16,17)}} + \frac{\triangle \beta_{(18,19)}}{\beta_{(18,19)}}\right) \quad (4.5.1)$$

where ΔV_T and$\triangle\beta$ are the differences in threshold voltages and transconductance factors of the indicated transistors respectively. From equation (4.5.1), it is concluded that the offset can be minimized by designing the input pair M_8 and M_9 with the highest possible g_m for a given bias current, which can be achieved by biasing them in weak inversion region. To obtain an optimal offset the transconductance of the current sink transistors M_{16}, M_{17}, M_{18}, M_{19} and current source transistors M_{10}, M_{11} should be reduced, meaning that they should work in strong inversion.

By appropriately sizing the transistors without using excessive area, an offset of about 1 mV (3σ) is achieved. In simulations, the input referred offset is measured in a feedback loop using an auxiliary amplifier that has

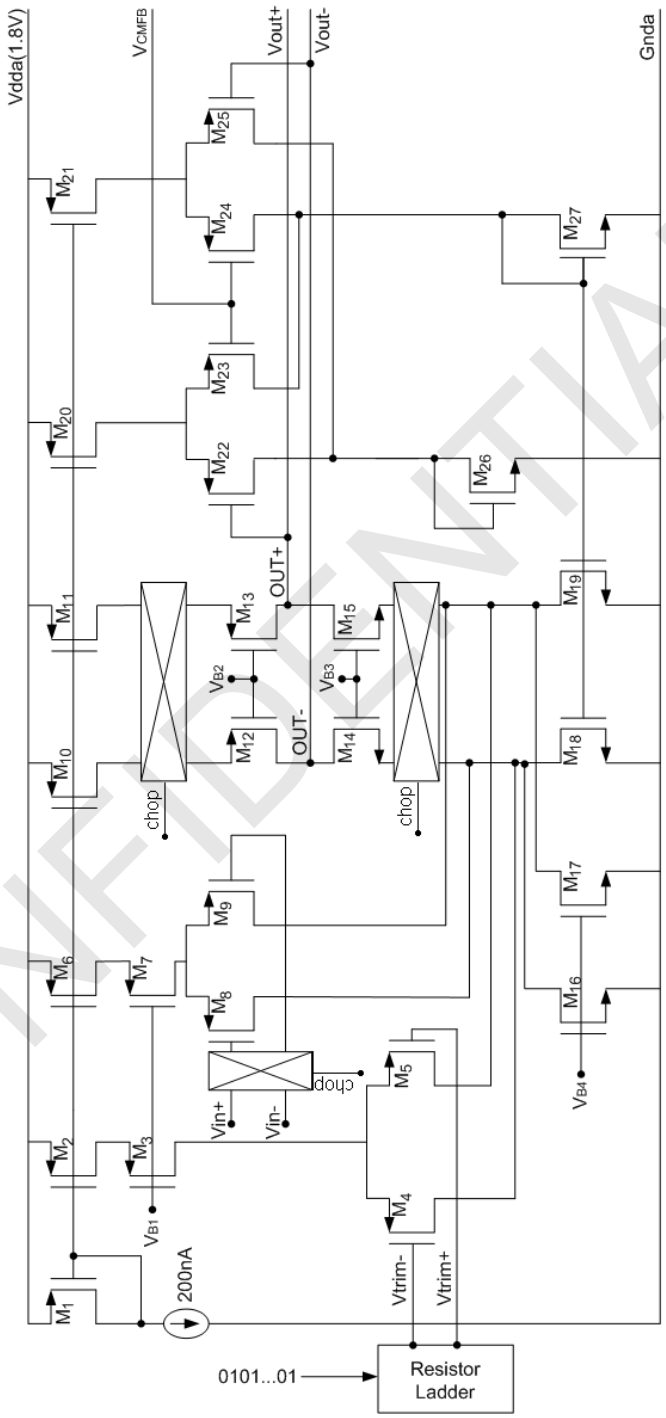

Figure 4.5.1: Fully Differential Folded Cascode Opamp

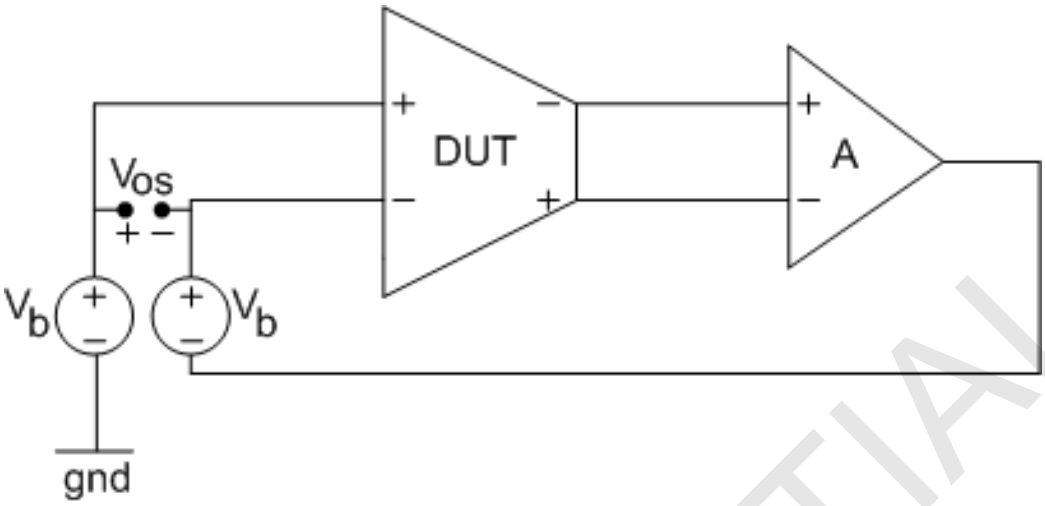

Figure 4.5.2: Offset measurement setup

a very high gain, as shown in figure 4.5.2 [13]. In order to achieve 200μV offset, additional trimming consisting of an auxiliary input pair and a resistor ladder structure is used. The auxiliary input pair is connected to the folding node, where the main input pair is also connected. The input voltage of the auxiliary input pair is provided by the resistor ladder as shown in figure 4.5.3. The relation between the transconductances of auxiliary and the main input pair is shown in equation (4.5.2). Since before trimming the input referred offset voltage is 1 mV, the resistor ladder must provide a voltage up to 10 mV to compensate for the opamp offset. In the resistor ladder, two 1.2 MΩ and forty 0.5 kΩ resistors are used. The step of the ladder is 0.5 mV which gives an average 50 µV offset resolution. The steps are selected by turning on/off the transistors in each branch.

This method only allows obtaining positive voltages which are used to cancel the negative offset. To be able to cancel the positive offset, the polarity of the offset is changed. This is achieved by placing the choppers, which have the same topology shown in figure 4.2.1, in the opamp.

$$g_{m,aux} = \frac{g_{m,main}}{10} \tag{4.5.2}$$

The comparison of the offset voltages before and after trimming is shown in table 4.4.

Due to a design error while mirroring the current from the bandgap reference, the DC gain of the opamp is around 10 dB below the desired value in fnsp and fnfp corners at 125 ^{o}C. This is approximately 0.03%. The opamp is not working in the *snsp* process corner.

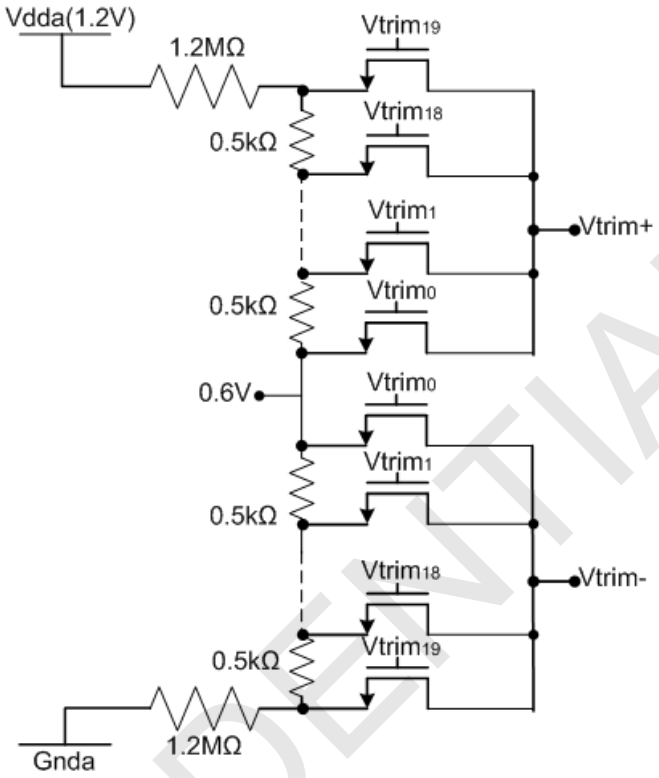

Figure 4.5.3: Offset trimming structure

Temperature [^{o}C]	-55	27	125
3σ offset voltage $before$ trimming	990 μV	960 μV	970 μV
3σ offset voltage $after$ trimming	145 μV	50 μV	175 μV

Table 4.4: Input referred offset voltage before and after trimming

Process Corners	DC Gain [dB]		
	-55^oC	27^oC	125^oC
fnfp	95.1	82.4	68.2
fnsp	95.4	76.4	67.3
snfp	97.5	94.5	83.6
snsp	-	-	-
nominal	95	92	75

Figure 4.5.4: DC gain of the opamp at different process corners and temperatures

MOSFET	W [μm]	L [μm]	I_{DS} [μA]	g_m [μS]
M_1	1.5	8	0.19	1.8
M_2	1.5[2]	8	0.38	3.5
M_3	0.5[2]	1.6	0.38	4.2
$M_{4,5}$	10[2]	4	0.19	4.8
M_6	1.5[20]	8	3.8	35.8
M_7	5[2]	1.6	3.8	43.3
$M_{8,9}$	25[8]	4	1.9	48
$M_{10,11}$	1.5[20]	8	1	8.9
$M_{12,13}$	5	3	1	11.2
$M_{14,15}$	1.4	3	1	12.1
$M_{16,17}$	1.9[6]	30	1.1	13.2
$M_{18,19}$	1.9[9]	30	1.9	21.4
CMFB Circuit				
$M_{20,21}$	1.5[4]	8	0.76	7.1
$M_{22,23,24,25}$	0.5	1	0.38	4.3
$M_{26,27}$	1.9[4]	30	0.76	8.9

Table 4.5: Important parameters of the opamp transistors

4.5.2 Transistor Dimensioning

The sizes, drain currents and transconductances of the transistors designed in figure 4.5.1 is shown in table 4.5.

4.6 Final Budget

The final error budget and the power budget of the system is shown in table 4.6 and 4.7, respectively. The total frequency error of the system is expected to be 0.27% with a power consumption of 35.3 μW. The final budget is larger from the intial budget shown in table 3.2. Because, the offset of the opamp is reduced to 25 μV below the target, which decreased the error; the on resistance of the mixer and the lower gain of the opamp increased the error. In addition, the input capacitance of the filter driver brings an additional 0.08% frequency error.

Error Contributors	Frequency Error [%]
Offset of the integrator opamp	0.064
Finite gain of the integrator opamp	0.063
Filter driver delay	0.08
Mixer effects	0.035
Filter driver resistance	0.023
Delay mismatch	0.0065
Total	**0.27**

Table 4.6: Error budget of the system

System Blocks	Power Consumption [μW]
VCO	20.1
Integrator opamp	13
Filter driver	1.3
Offset trimming ladder	0.6
Divider	0.27
Total	**35.3**

Table 4.7: Power budget of the system

4.7 Layout

The layout of the chip is shown in figure 4.7.1 and each block of the system is highlighted. The area of each block is listed in table 4.8. Main circuitry consumes 0.573 mm^2 and the remaining area is occupied by the decoupling capacitors.

System blocks	Area [mm^2]	System blocks	Area [mm^2]
Integrator capacitors	0.205	Opamp	0.014
RC Filter	0.197	Divider	0.009
VCO	0.023	Trimming ladder	0.003
Biasing	0.021	Mixer	4.8×10^{-5}
		Total	**0.573**

Table 4.8: The silicon area consumed by each block of the system

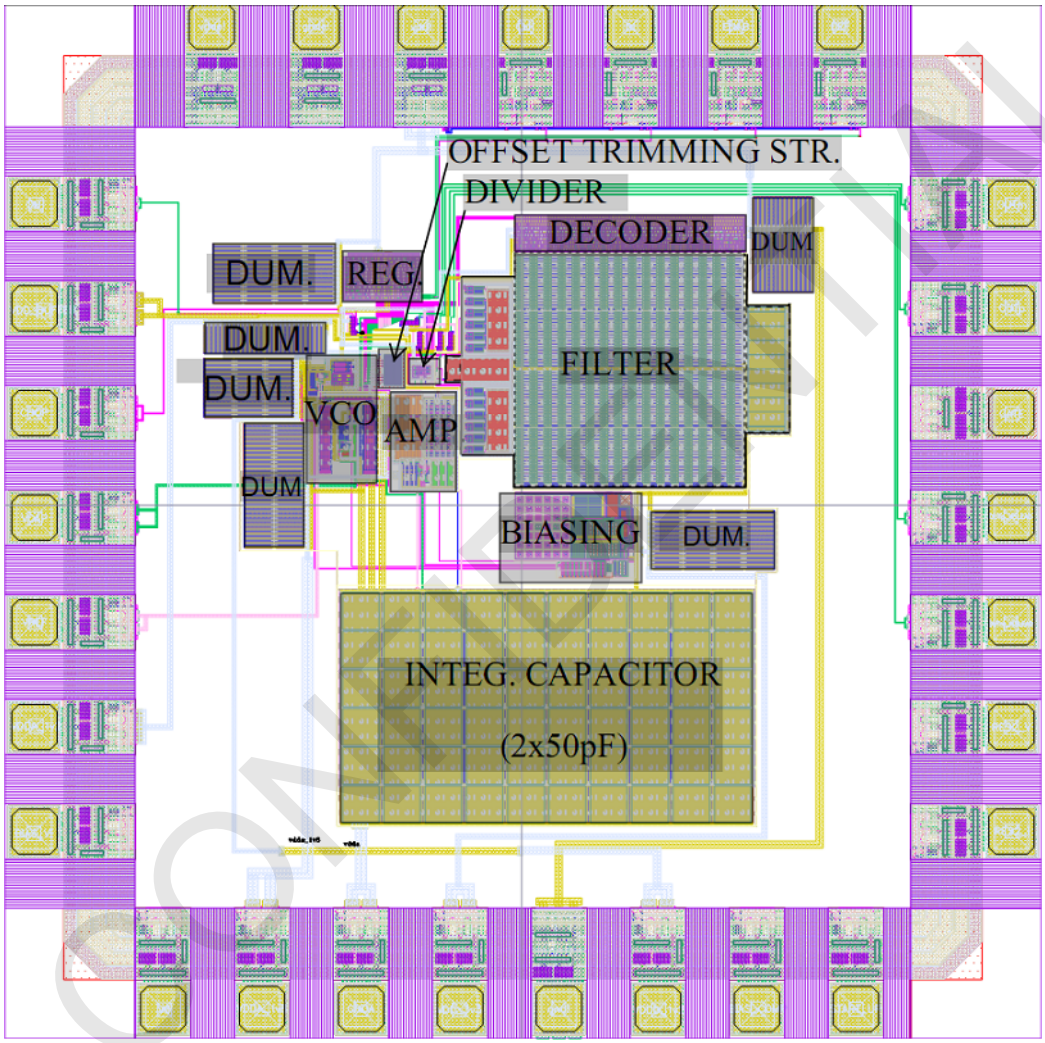

Figure 4.7.1: Layout of the chip

Chapter 5

Measurement

5.1 Measurement Setup

The functionality and the performance of the presented system are tested by measuring the output frequency of 12 chips at different temperatures. The measurement setup is shown in figure 5.1.1. This setup consists of the following components:

- A printed circuit board (PCB1) that is shown in figure 5.1.3 holds 4 test chips (DUT), relays and a decoder that are used to select these chips, relay driving integrated circuits (ICs) and a multiplexer to get the output signal from the selected chip.

- A PCB (PCB2) that is shown in figure 5.1.2 has two optocouplers to isolate the noisy signals supplied from the parallel port of the PC. These signals are the clock signal, enable signal of the decoder and select signals of the chips.

- An oven that is capable of changing the temperature between -55^{o}C and 125^{o}C. A calibrated Pt100 resistance is used to change the temperature accurately. It is placed inside an aluminum block on which PCB1 is mounted.

- A Keithley multimeter is used to measure the Pt100 resistance and the output frequency of the chips.

- Power supplies (only one shown below) provide 1.2 and 1.8 V analog and digital supplies for the chip, 3.3 V supply for the decoder and optocouplers and 5 V for the relay driving ICs in the PCBs.

- A PC running Labview controls the oven temperature and all the instruments mentioned above through RS 232 and GPIB buses, respectively. The values of the resistors, capacitors and the offset voltage of the integrator opamp can be adjusted by the Labview interface. The captured data is stored in the PC for further analysis.

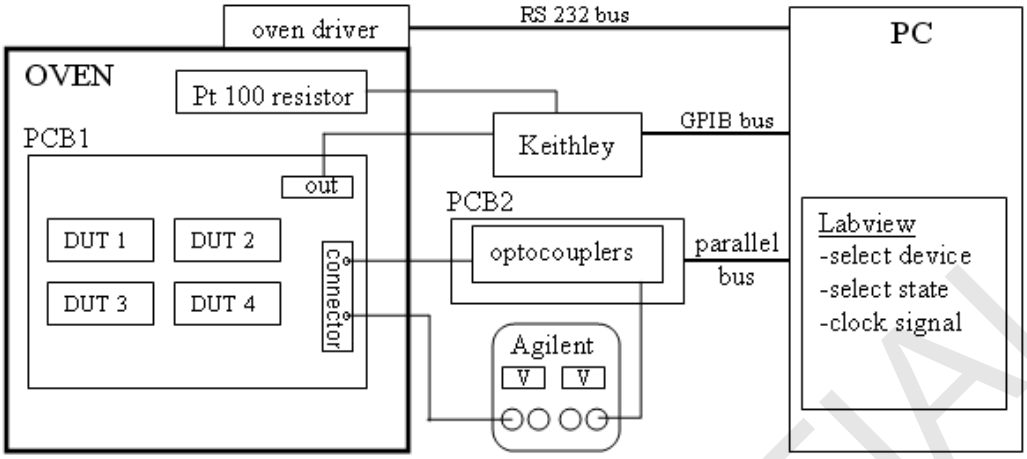

Figure 5.1.1: Block diagram of the entire measurement setup

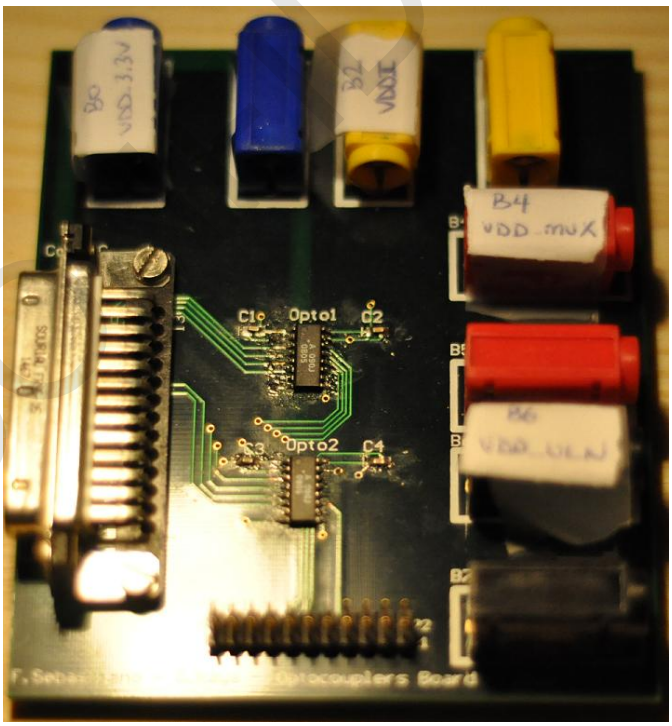

Figure 5.1.2: The picture of the optocoupler board

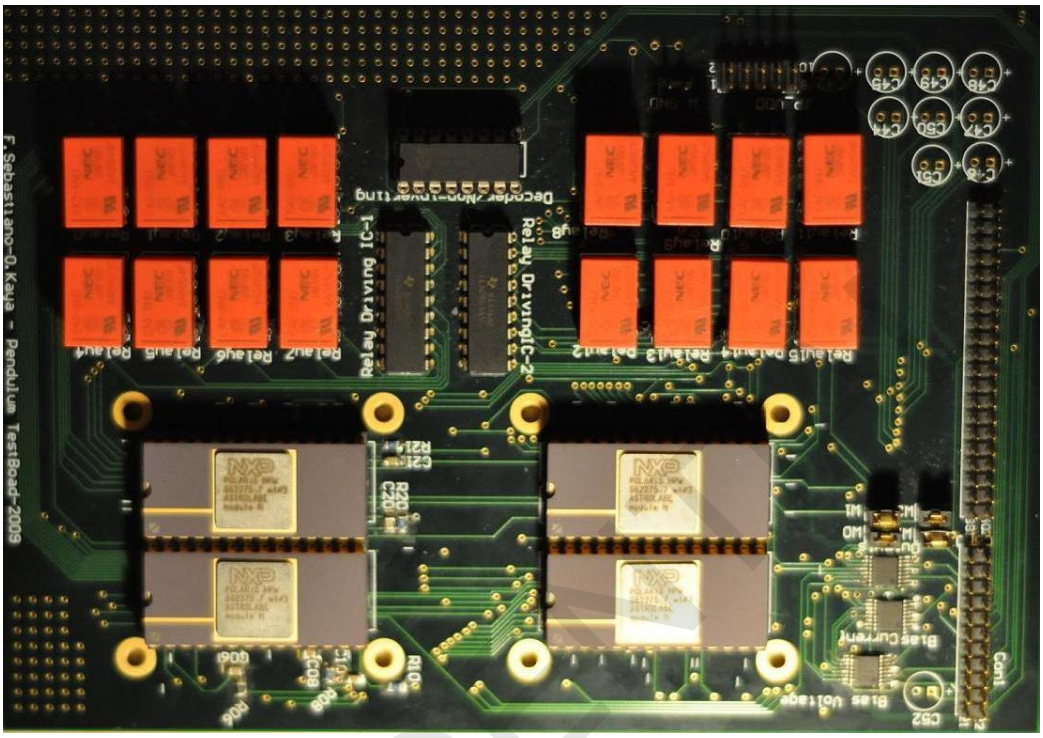

Figure 5.1.3: The picture of the test board

5.2 Measurement Results

5.2.1 Characterization of the RC Network

In section 4.1, it was explained that the oscillation frequency is determined by the resistor and capacitor values in the RC filter. These passive components need to be trimmed due to the process spread. The trimmable resistor (R_1) and the capacitor (C_1) can be trimmed by 5 and 8-bits network and are used for the coarse and fine tuning of the output frequency, respectively.

The frequency outputs of 12 samples as a function of resistor trimming steps are shown in figure 5.2.1. As observed from the figure, at the initial and final steps of the trimming, output frequencies saturate. This is due to the limited frequency range of the VCO. As seen from figure 4.4.3, the oscillation frequency range of the VCO is around 40 kHz. The measurement results also confirm the simulation results.

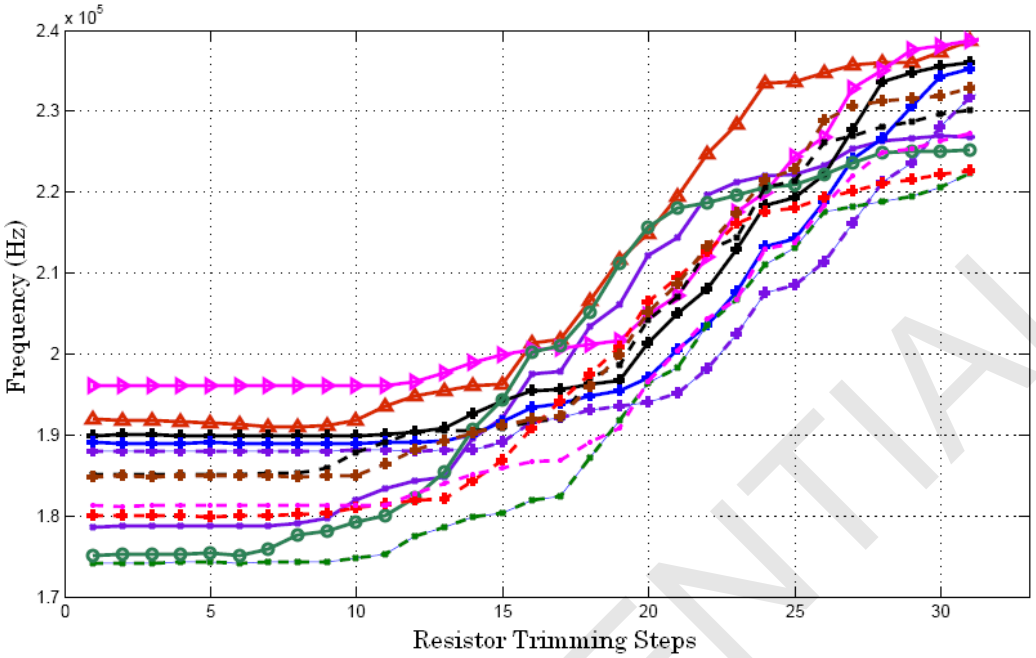

Figure 5.2.1: Frequency outputs of 12 samples as a function of resistor trimming steps

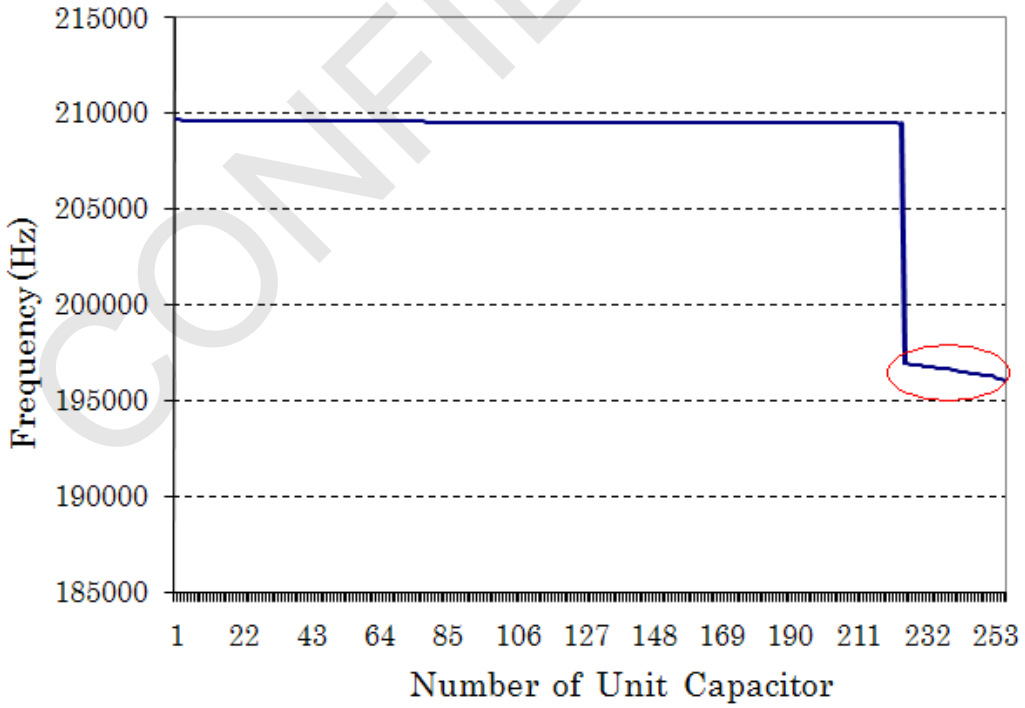

Figure 5.2.2: Frequency variation as a function of capacitor trimming steps

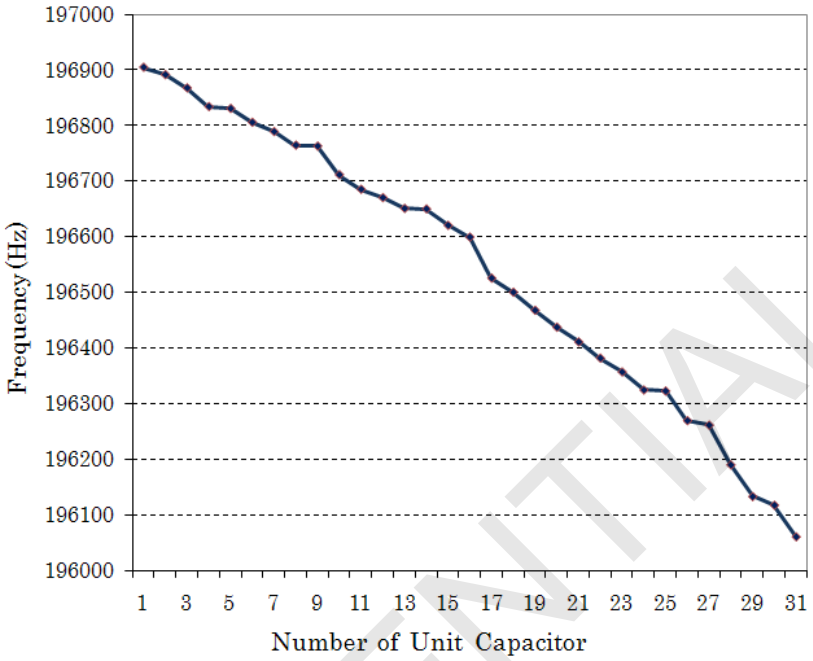

Figure 5.2.3: Frequency variation as a function of first 31 steps of the capacitor trimming structure

The output frequency as a function of the capacitor trimming steps is shown in figure 5.2.2. As the number of unit capacitors are activated, the oscillation frequency should decrease. However, the decoder works only partially. This problem stems from the verilog code of the decoder. The functional part of the capacitor trimming structure is shown in figure 5.2.3. At each step, the frequency decreases approximately 0.035%. Theoretically, the filter is designed to obtain 0.05% resolution which is close to the measurement result. In addition, the behavior of the curve is not absolutely monotonic. This can be due to the parasitic capacitors and their mismatch.

The output frequency of 20 samples are measured using the same settings for trimmable capacitor and resistor. The histogram of the measurement result is shown in figure 5.2.4. The standard deviation of the histogram is 5.2%. According to [14], both N-poly resistors and fringe capacitors may experience 16% process variation. This refers up to 32% frequency variation. The measurement results are better than expected. This is probably due to measuring samples from the same batch.

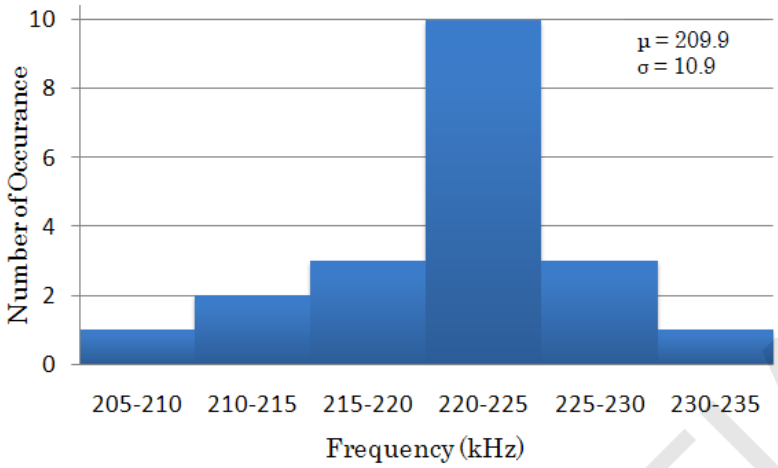

Figure 5.2.4: Frequency output of 20 samples

5.2.2 Offset Measurements

In section 3.5.3, it is shown that the offset of the integrator opamp is the dominant source of error and therefore needs to be trimmed to reduce it below 200 μV.

To evaluate the offset, the change at the output frequency is observed for different trimming voltages when the state of the chopper (see figure 4.5.1) is changed from chop=1 to chop=0. For 12 samples, this change is plotted in figure 4.4. Ideally, if the offset voltage is zero, changing the state of the chopper does not cause any change in frequency. For the trimming setting, where the output frequency does not change represents the offset voltage. Since the g_m value of the main input stage is 10 times higher than the auxilary stage where the trimming voltage is applied, the offset voltages are 10 times smaller than trimming voltages.

The offsets of the samples are shown in figure 5.2.6. Due to missing chopper at the output of the offset trimming structure, the trimming structure can only compensate the negative offsets. Therefore, out of 12 samples, the offset voltage of 3 samples can be totally removed. For 9 samples, the offset voltage is found by extrapolating the curves in figure 5.2.5. 6 of them has below 200 μV and 3 samples has around 400 μV offset voltages.

The average of the 12 curves is shown in figure 5.2.6. From this figure, a systematic offset voltage of 95 μV is observed. This can be due to measuring insufficient number of samples.

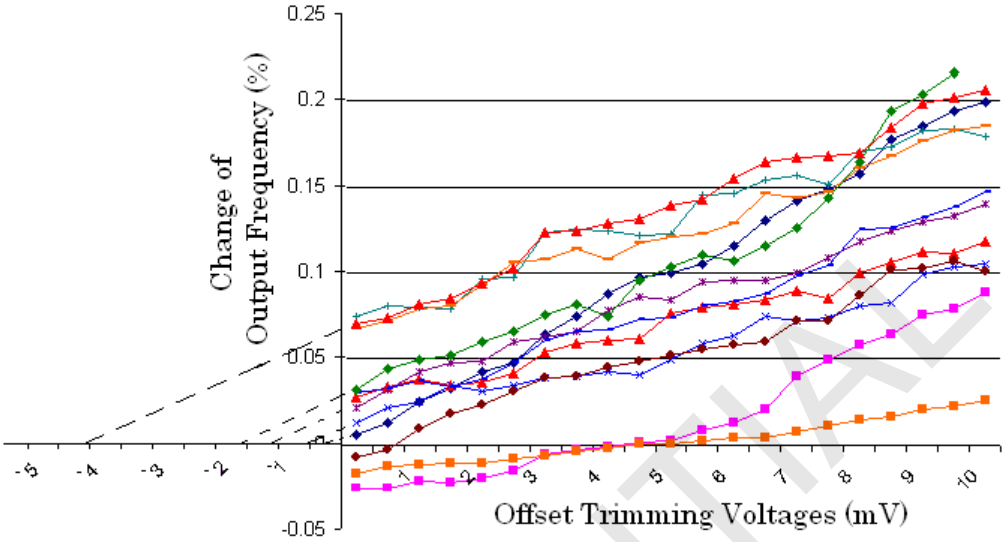

Figure 5.2.5: Input referred offset voltage of integrator opamp for 12 samples

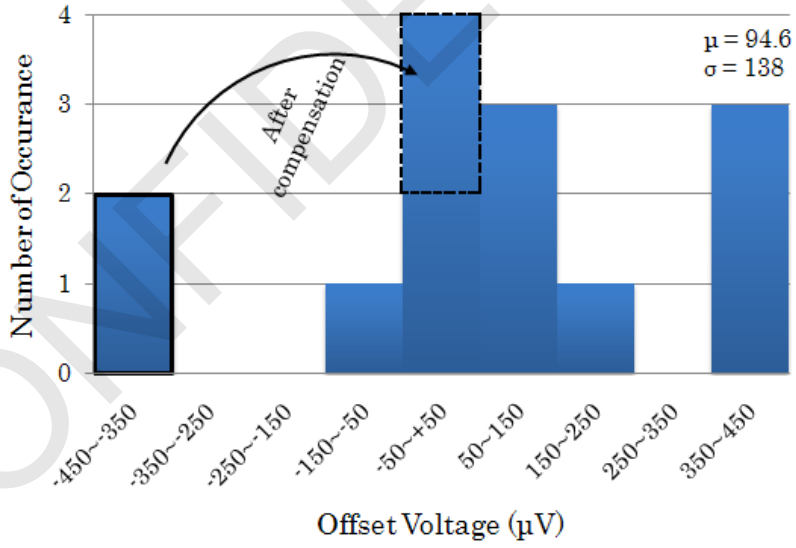

Figure 5.2.6: The offset voltages of 12 samples

5.2.3 Power Consumption

The power consumed from the power supplies of the chip is presented in table 5.1. The total power consumption of the chip is 37.2 μW, excluding the output buffers and biasing.

Supply [V]	Type	System Blocks	Power Consumption [μW]
1.2	Analog	Filter Driver	1.32
1.8	Analog	Opamp + Converter	18.9
1.2	Digital	VCO	16.7
1.8	Digital	Freq. Divider	0.32
		Total	**37.2**

Table 5.1: The current consumption of the chip

5.2.4 Jitter Measurements

Since the aim of this chip was to investigate the feasibility of the proposed concept, it was optimized for accuracy and low power consumption. However, jitter is an important design aspect of any frequency reference, as well.

The term "jitter" is a broadly used term that refers to frequency instability of oscillators, as observed in the time domain [20]. When specifying jitter however, a more strict definition is needed. In circuit design literature, the jitter of an oscillator is often specified as the period jitter, long-term jitter and relative jitter.

Period jitter is specified by the normalised one-period time error and often expressed in parts per million. The long-term jitter is the accumulated jitter over a certain number of periods. Relative jitter is defined as the standard deviation of jitter divided by elapsed time; its value for a time period of the order of one second is an important parameter for time references used in WSN, since it limits duty-cycle of the receiver when synchronization is performed over a time scale of seconds [17].

The measured period jitter of the output signal is 22 ns (rms) which is 0.46% of the oscillation period. Long-term jitter measurements for the output frequency of 1.8 MHz are reported in figure 5.2.7. The relative jitter is less than 200 ppm for a time period of miliseconds. This is a great improvement compared to the reported data (around 1000 ppm) in [16]. This improvement is thanks to the negative feedback effect of the loop.

5.2.5 Oven Measurements

12 samples from one batch are measured over the military temperature range (-55^{o}C to +125^{o}C) using a temperature controlled oven, with an accuracy in the order of 0.1^{o}C. The output frequency of each sample as a function of temperature is shown in figure 5.2.8. After one-point calibration, the frequency spread with respect to average frequency is computed from figure 5.2.8 and shown in figure 5.2.9. It is below 0.9% (3σ) over the range from

-40°C to +125°C.

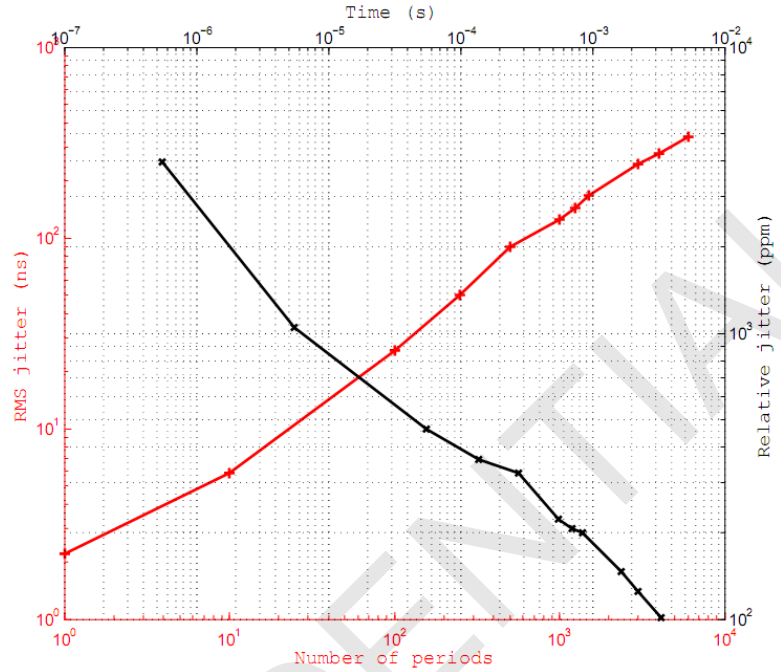

Figure 5.2.7: Measured long-term jitter vs. time

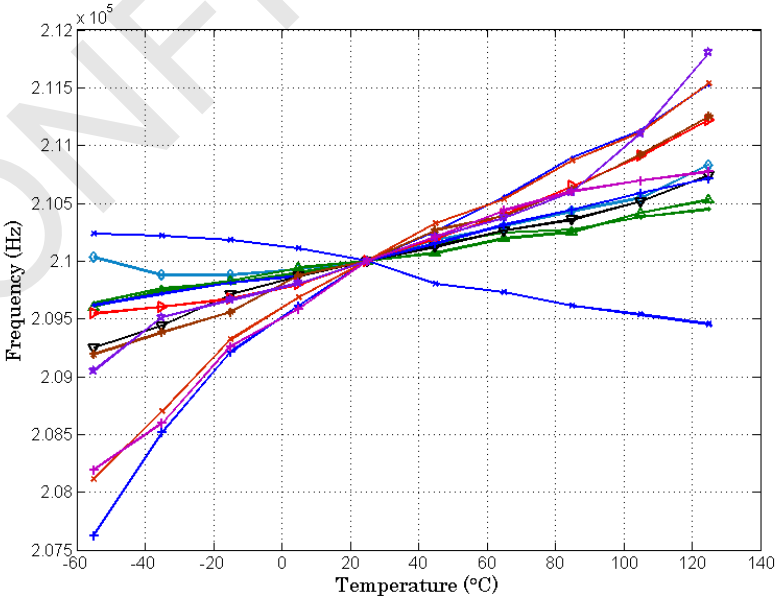

Figure 5.2.8: Output frequency measurements on 12 samples

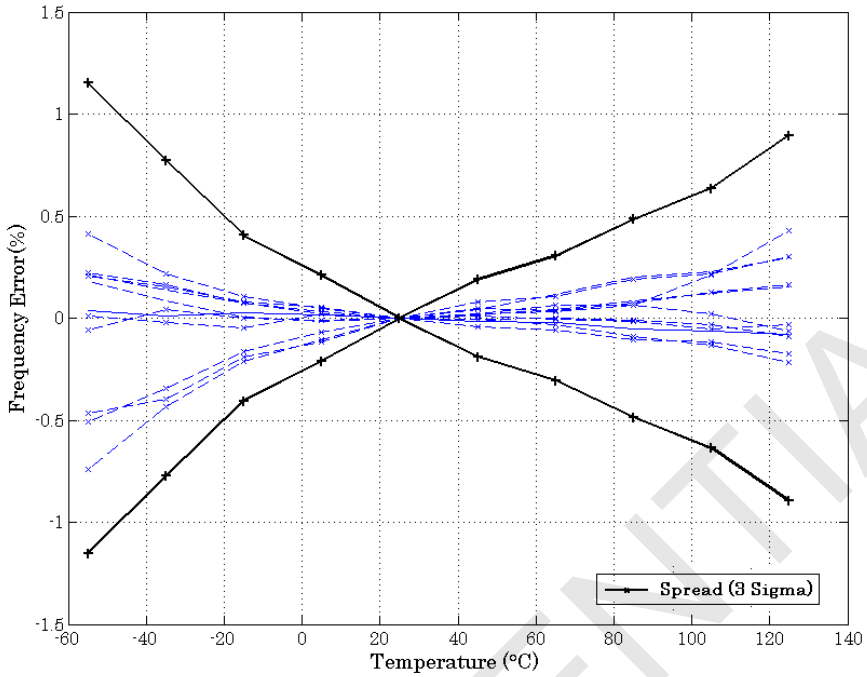

Figure 5.2.9: Frequency error with respect to average frequency vs. temperature after one-point trimming at room temperature for 12 samples

The temperature coefficients are shown in figure 5.2.10. The mean and standart deviation values of the histogram are 45.7 and 31.2 ppm/^{o}C, respectively.

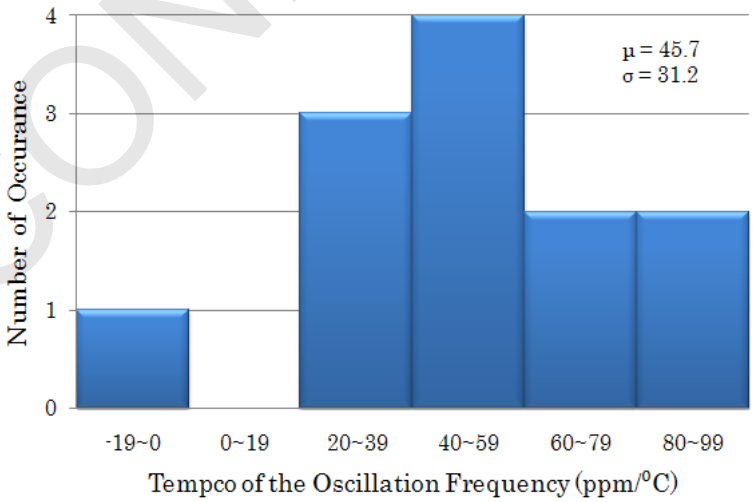

Figure 5.2.10: The frequency temperature coefficients of 12 samples

The measurement results shows a higher frequency deviation than the designed target over temperature. This difference can be attributed to the temperature coefficient of the offset voltages. To prove it, offset voltages should be measured at the extreme temperatures.

5.3 Chip Photomicrograph

The frequency reference was implemented in 0.16 μm CMOS process and a chip photo is shown in figure 5.3.1.

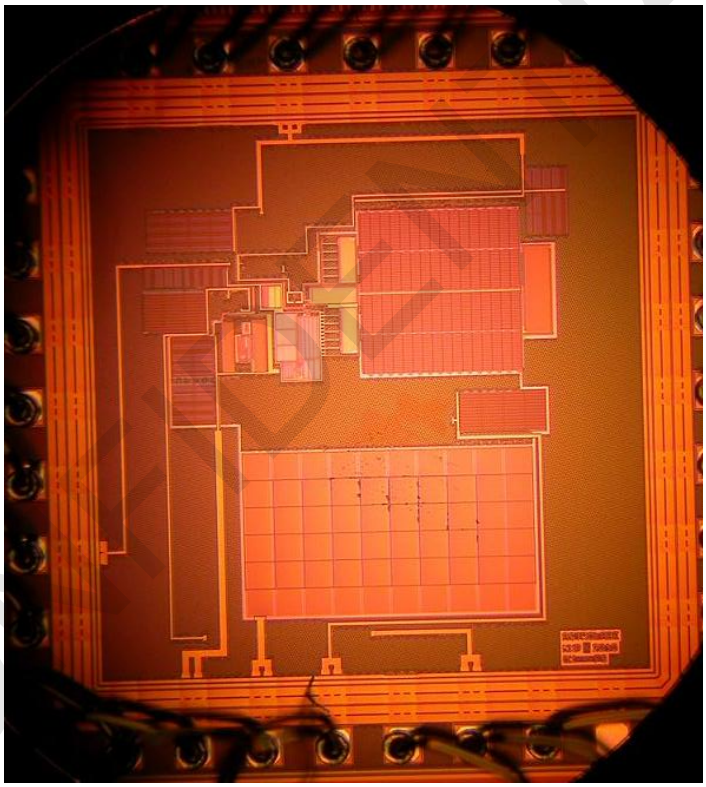

Figure 5.3.1: Chip photomicrograph of the frequency reference

5.4 Conclusion

The comparison of the initial targets and the measurement results is shown in table 5.2. The frequency accuracy is around 3 times worse than expected. The power dissipation of the chip is 25%, the average temperature coefficient is 40% lower than the targeted values. The output frequency of the

references is set to 210 kHz, which was initially targeted as 250 kHz. This frequency could easily be achieved if the capacitor trimming structure would work properly. However, this is not a critical design specification.

In table 5.3, the performance of this design is compared to other frequency references which appear to be suitable for WSNs. The power dissipation of this chip is the lowest one. It is around 4.8x, 2x and 10% lower than that of the designs in [9], [7, 8] and [16, 18], respectively.

The temperature coefficient performance of this chip is the second best one. In [8], [9] and [18] this performance is reported for only 1 sample. Therefore, to make a relatively fair comparison, the performance of the 12 measured samples is averaged out. The temperature coefficient is around 2x and 30% lower than that of the designs in [16, 7] (comparing the σ values) and [18, 9], respectively. However, it is 2x worse compared to the design in [18].

Since in different designs the frequency variation is measured in different temperature ranges, table 5.4 is prepared to be able to make a fair comparison. The performance is around 2x better than that of the designs in [16] and [7]. It is comparable to that of the designs in [8], [9] and [18]; however it should be considered that for this work 3σ values are reported.

Specification	Target Values	Measurement Results
Temperature Range	-55 ^{o}C to 125 ^{o}C	-55 ^{o}C to 125 ^{o}C
Power Dissipation [μW]	$<$ 50	37
Frequency Inaccuracy [%]	$\pm$0.27 (3σ)	$\pm$1.1/$\pm$0.9 (3σ)
Output Frequency [kHz]	250	210
Temp. Coefficient [ppm /^{o}C]	$<$ 80	46 (μ), 37 (σ)
Initial Accuracy (@27 ^{o}C) Trimmed Accuracy (@27 ^{o}C)	$\pm$20% $\pm$0.05%	$\pm$15.7% (3σ) - ($\pm$0.035%[1])
Process Node	0.16 μm CMOS	0.16 μm CMOS
Supply Voltage	1.2 V, 1.8 V	1.2 V, 1.8 V

Table 5.2: The summary of target specs vs measurement results

[1]This performance could be obtained if the decoder would work properly.

Literature	**This work**	[16]	[7]	[18]	[8]	[9]
Frequency [MHz]	0.21	0.1	6	2	10	30
Supply voltage [V]	1.2/1.8	1.2	1.2	1.8	1.2	1.8
Power [µW]	37	41	66	45	80	180
Area [mm^2]	0.57	0.11	0.03	0.04	0.22	0.08
Process [CMOS]	0.16 µm	65 nm	65 nm	0.18 µm	0.18 µm	0.18 µm
Variation [%] with Temperature [^oC]	± 1.15 / 0.9 (3σ) @ -55∼125	± 1.1 (3σ) @ -20∼80	± 0.88 (σ) @ 0∼100	± 0.75 ± 0.19* @ -40∼125	± 0.4 @ -20∼100	-0.7 / +0.5 @ -20∼100
Samples measured over temperature	12	11	6	1	1	1
Temp. coeff. [ppm /^oC]	46 (μ) 37 (σ)	73 (σ)	86 (σ)	91 23	67	90
Phase noise [dBc/Hz]	N.A.	N.A.	-96 (@100 kHz)	-90 (@100 kHz)	N.A.	-96 (@1 MHz)
Period jitter	22 ns (rms) (0.46%)	52 ns (rms) (0.52%)	N.A.	N.A.	N.A.	N.A.
Process sensitivity	16% (3σ) 20 samples	7% (3σ) 11 samples	0.8% (σ) 6 samples	N.A.	N.A.	2.7% (σ) 20 samples

Table 5.3: Comparison to the state-of-the-art frequency references suitable for WSNs

* This performance is obtained after temperature compensation.

Temp. Range [^{o}C]	**This work**	[16]	[7]	[18]	[8]	[9]
-40∼125	± 0.9(3σ)	-	-	± 0.75 ± 0.19*	-	-
-20∼100	±0.45/±0.60 (3σ)	-	-	-	± 0.4	-0.7/+0.5
0∼100	±0.25/±0.60 (3σ)	-	± 0.88(σ)	-	-	-
-20∼80	± 0.45(3σ)	± 1.1(3σ)	-	-	-	-
Samples measured over temperature	12	11	6	1	1	1

Table 5.4: Accuracy comparison to the state-of-the-art frequency references

* This performance is obtained after temperature compensation.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis, a new precision RC-locked oscillator topology for wireless sensor networks (WSNs) has been presented. The aim of this chip was to investigate the feasibility of the proposed concept and to obtain a competitive performance in terms of accuracy and power consumption compared to the state-of-the-art.

Despite some design errors, the new IC was sufficiently functional to be tested, and it achieved a frequency inaccuracy of $\pm 0.9\%$ (3σ based on 12 samples) from -40^oC to 125^oC, consuming 37 μW power. The achieved performance is comparable to the state-of-the-art, for a wider temperature range and for significantly more samples.

6.2 Future Work

The future work includes the corrections of the design errors to improve the accuracy. A chopper should be placed at the output of the offset trimming structure to make it fully functional. The same filter driver should be used to drive the mixer. The decoder that is used for capacitor trimming has to be synthesized properly.

An additional measurement to find the offset voltages at the extreme temperatures will clarify if the untrimmed offset is the main source of error.

It is also recommended to optimize the jitter performance of the frequency reference.

Appendix A

Calculations

In this section, the calculations are done to find out the oscillation frequency, the frequency error due to the offset voltage of the opamp and the number of bits required for the offset trimming are shown.

A.1 Calculation of the Oscillation Frequency

In figure A.1.1, the current waveform at the input of the integrator is shown. At the steady-state, the area under this curve is forced to be zero by the integrator opamp. This waveform is shaped by the filter which determines the oscillation frequency. Therefore, the oscillation frequency can be calculated by analyzing this waveform.

While the simulating the locked oscillator using the ideal building blocks i.e filter, integrator, mixer and VCO, an oscillation frequency which is equal to $0.926/2\pi RC$ is obtained while the initially expected value was $1/2\pi RC$. Therefore, the oscillation frequency is analyzed to verify the simulation results.

The area under one period of the waveform in figure A.1.1 can be written as follows:

$$f(t) = -\frac{V_{dd}}{2} + e^{-t/\tau}.\frac{V_{dd}}{2R}(1 + \frac{1 - e^{-T/2\tau}}{1 + e^{T/2\tau}}) \tag{A.1.1}$$

$$\int_{3T/8}^{T/2} -f(t)d(t) + \int_{0}^{3T/8} f(t) = 0 \tag{A.1.2}$$

where f(t) is the function that defines the signal in figure 3.4.2

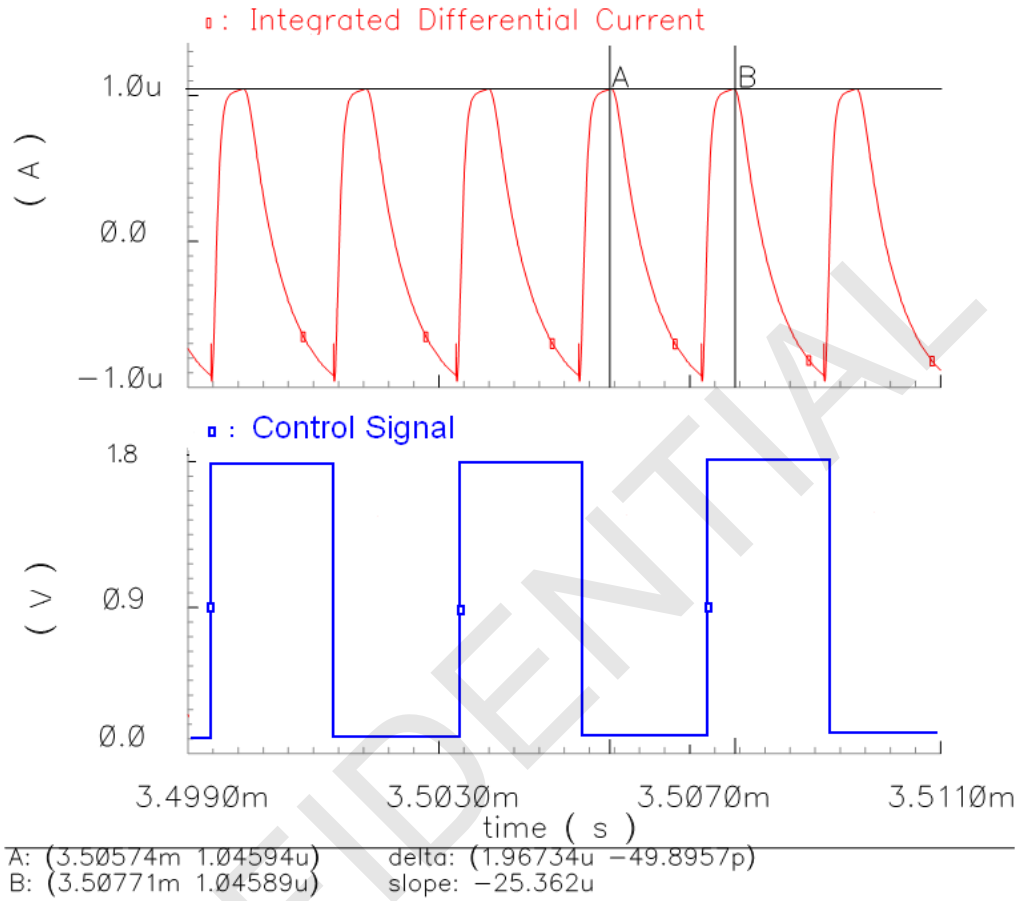

Figure A.1.1: The signal waveform at the integrator input

For the sake of simplicity only the solution of the equation is given as follows:

$$(\frac{1-\sqrt{x}}{1+\sqrt{x}}+1).(2.x^{3/8}-1-\sqrt{x})-\frac{lnx}{4}=0 \tag{A.1.3}$$

where,

$$x = e^{-T/\tau} \tag{A.1.4}$$

The solution of the equation is shown in figure A.1.2.

The roots of the equation (A.1.3) is found as $x_1 = 0.00113$ and $x_2 = 1$. x_2 is the solution at T=0. Therefore x_1 is the valid solution and leading to the following equation:

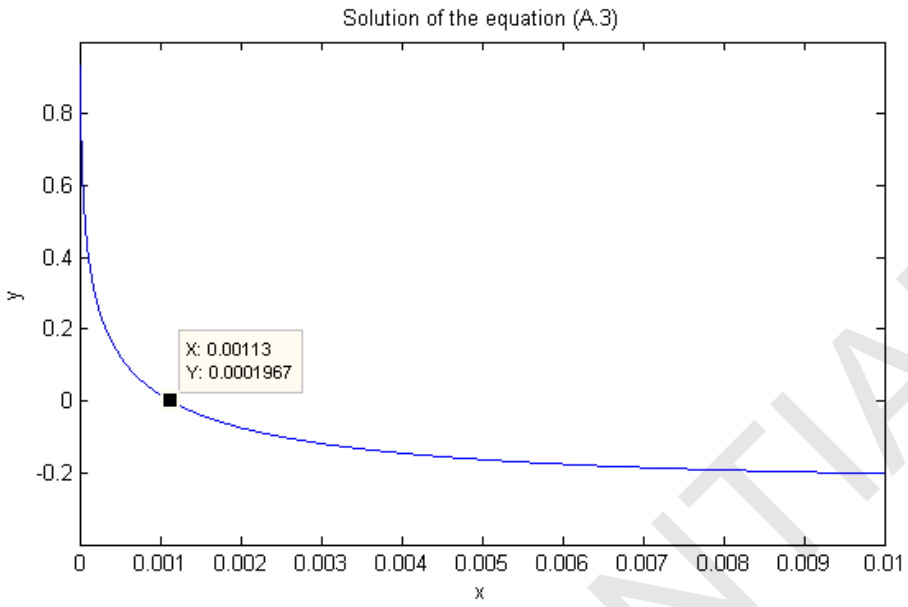

Figure A.1.2: The solution of the equation (A.1.3)

$$f = \frac{1}{T} = \frac{1}{-ln(x_2).\tau} \cong \frac{0.926}{2\pi RC} \tag{A.1.5}$$

A.2 Frequency Error Due to Offset Voltage

In section 3.5.3, the effect of the integrator opamp offset on the oscillation frequency is described. Here, this description is supported by the mathematical analysis.

The operation of the mixer can be separated into two phases ϕ_1 and ϕ_2. The operation in these two phases is shown in figure A.2.1 and A.2.2.

During ϕ_1,the following equations can be written as:

$$I_1 = (V_{dd} - V_{bias} - V_{os}/2)/Z \tag{A.2.1}$$

$$I_2 = (-V_{bias} + V_{os}/2)/Z \tag{A.2.2}$$

$$I_1 - I_2 = (V_{dd} - V_{os})/Z \tag{A.2.3}$$

$$I_1 - I_2 = (1 - \frac{V_{os}}{V_{dd}})/Z \tag{A.2.4}$$

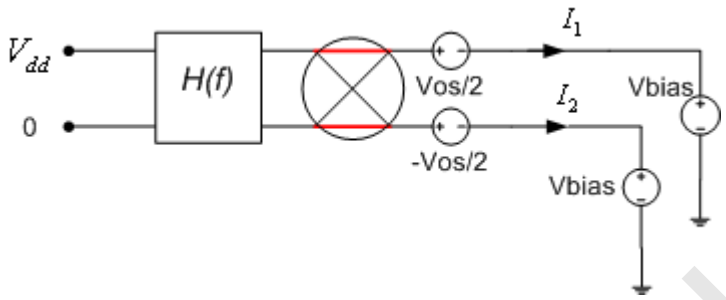

Figure A.2.1: The operation during phase ϕ_1

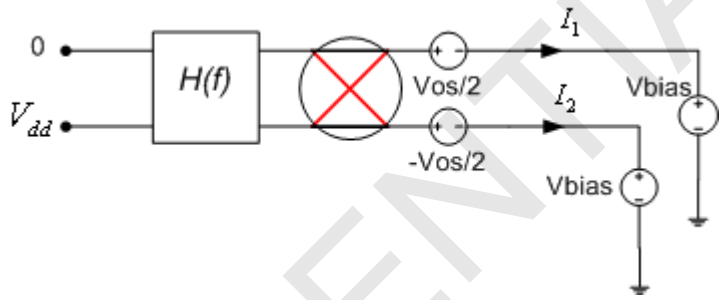

Figure A.2.2: The operation during phase ϕ_2

During ϕ_2,the following equations can be written as:

$$I_1 = (-V_{dd} + V_{bias} - V_{os}/2)/Z \tag{A.2.5}$$

$$I_2 = (V_{bias} + V_{os}/2)/Z \tag{A.2.6}$$

$$I_1 - I_2 = (-V_{dd} - V_{os})/Z \tag{A.2.7}$$

$$I_1 - I_2 = (-1 - \frac{V_{os}}{V_{dd}})/Z \tag{A.2.8}$$

Using the equations (A.2.4) and (A.2.8), the equation (A.1.2) can be modified as follows:

$$(1 + \frac{V_{os}}{V_{dd}}) \int_{3T/8}^{T/2} -f(t)d(t) + (1 - \frac{V_{os}}{V_{dd}}) \int_{0}^{3T/8} f(t) = 0 \tag{A.2.9}$$

This equation leads to the following solution, where $\alpha = V_{os}/V_{dd}$:

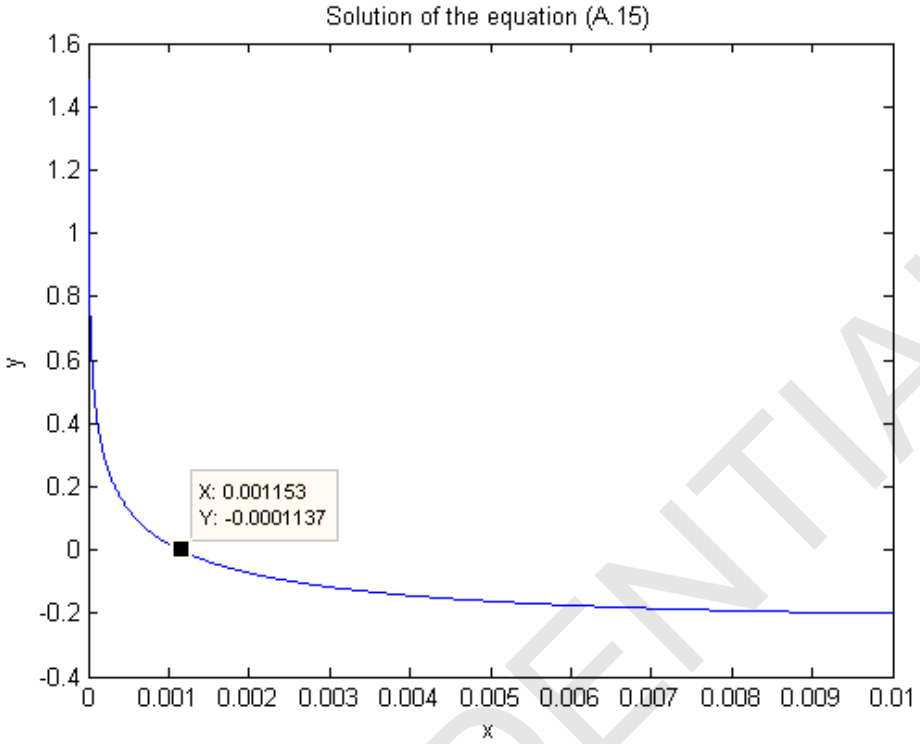

Figure A.2.3: Solution of the equation (A.2.10)

$$(\frac{1-\sqrt{x}}{1+\sqrt{x}}+1).[2.x^{3/8}-\sqrt{x}.(1-\alpha)-1-\alpha]-\frac{lnx}{4}(1+2\alpha)=0 \quad \text{(A.2.10)}$$

As an example, if the equation (A.2.10) is solved for V_{os} = 1 mV and V_{dd} = 1.2 V, the solution is obtained for x = 0.001153 as shown in figure A.2.3. This solution refers to a frequency deviation of approximately 0.3%, which is close to the simulated value.

A.3 Trimming Resolution of the RC Filter

When the trimming of an RC network is an issue, the trimming resolution and the trimming strategy have to be determined. Considering the target frequency accuracy, the trimming resolution is set to ±0.05%. To decide on the trimming strategy, first the number of bits that is required by the trimming has to be calculated. Only considering the process variations and

that the capacitors will be trimmed, the required number of bits to achieve the desired resolution is calculated as follows:

$$resolution = \frac{\frac{0.926}{2\pi R_{nom}(1+p_R)2C_{min}} - \frac{0.926}{2\pi R_{nom}(1+p_R)2(C_{min}+\triangle C)}}{f_{nom}} \quad \text{(A.3.1)}$$

where $\triangle f/f_{nom}$ is the trimming resolution, R_{nom} is the designed filter resistor, p_R is the process variation of a poly resistor, $\triangle$C is the capacitor step size, $C_{min}$is the minimum achievable capacitance after trimming using $\triangle$C.

Solving the equation (A.3.1) for f_{nom}=250 kHz , R_{nom} =30 kΩ, p_R=0.163, results with the following relation between $\triangle$C and C_{min}:

$$\triangle C = \frac{C_{min}^2 \times (1.2 \times 10^8)}{1 - (C_{min} \times 1.2 \times 10^8)} \quad \text{(A.3.2)}$$

The capacitor range should be wide enough to cover the process variations of both resistor and capacitor. This requirement is defined with the following equation:

$$fnom = \frac{K}{R_{nom}(1-p_R)C_{max}(1-p_C)} = \frac{K}{R_{nom}(1+p_R)C_{min}(1+p_C)} \quad \text{(A.3.3)}$$

where $K = 0.926/(4\pi)$, p_C is the process variation (p_C =0.158) of a fringe capacitor.

The equation (A.3.3) gives the desired the range of the filter capacitor, C_{max}=13.9 pF and C_{min}=7.3 pF. From equation (A.3.2), $\triangle$C is calculated as 6 fF.

The number of required bits is found from the following formula:

$$2^m = \frac{C_{max} - C_{min}}{\triangle C} \quad \text{(A.3.4)}$$

where m is the number of bits which is calculated as 10 bits.

From the calculations it is concluded that it is not easy to obtain the desired resolution by means of only trimming the capacitor.Because, the required unit capacitors are very sensitive to parasitics. Therefore, both the capacitor and the resistor are trimmed and totally 13 bits are used in the trimming structure. The need for the additional bits is to make sure that the coarse steps are overlapping as shown in figure 4.1.5. In addition, the mismatch of the small fringe capacitors is not considered in the calculation for simplicity.

Acknowledgement

The past two years I have spent at TU Delft have been a fabulous journey mostly because of the amazing people I have met, who have been a part of it. I have built a great knowledge and perspective both in my career and social life.

First and foremost, I would like to thank my supervisors Prof. Kofi Makinwa and Ir. Fabio Sebastiano whose support were always available when needed. I am grateful to Dr. Agnese Bargagli and Ir. Muhammed Bolatkale for their inestimable guidance and interest in the project. I would also like to thank Leo Warmerdam for giving me this opportunity and sponsoring the project.

Words cannot express my gratitude to my dear friends Aashini Gulati, Alper Kemal Koc, Cem Ozgur, Emre Can Kara, Gokturk Cinserin, Gokulraj Chandramohan, Halil Kukner, Oktay Cikili and Yunus Okmen for their constant support, understanding and welcoming me in their houses. I am truly lucky to have such great friends.

Finally, I would like to express my enormous thanks to my parents. No matter how far away they are physically, they are never far from my heart and mind. All my endeavors are to deserve their boundless love and support without which I would never have had the strength and courage to pursue my dreams, and for that I dedicate this thesis to them.

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