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Monolithic SPAD Arrays for High-Performance, Time-Resolved Single-Photon Imaging

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***Abstract*—SPAD (single-photon avalanche diode) arrays are single-photon sensors, which enable photon counting and unparalleled time-resolved imaging. In this paper, we will detail the architecture and characteristics of three representative SPAD arrays, implemented in standard CMOS technologies and targeted to a range of applications such as biophotonics, basic sciences, and engineering. Two sensors feature a high-performance pixel and enable time-gated and TCSPC operation, respectively. The third sensor is a line array whose pixels are coupled on a one-to-one basis with an FPGA for flexible data acquisition and processing.**

Keywords—single-photon, SPAD, CMOS, time-resolved, gating

I. Introduction

Individual single-photon avalanche diodes (SPADs), which are capable of detecting and time-stamping single optical photons with excellent timing resolution (10-100 ps), have been integrated in the recent past in arrays of increasing spatial resolution (10-100 kpixels). We will review three representative SPAD array implementations, aimed at basic science, biophotonics, and engineering applications; they illustrate the rich diversity of imager architectures with their respective strengths.

II. Image Sensor Architectures

SwissSPAD2 is a **512×512 pixel, widefield gated SPAD imager**, the largest array format reported to date [1]. It employs a p-i-n SPAD [2] with best-in-class combination of DCR, PDP and spectral width (Table I); the 10.5% native fill factor can be improved by up to 5× using microlenses. The imager can generate 1-bit images at a maximum frame rate of 98 kfps. An in-pixel time gate is distributed to the array using balanced signal trees to perform time-resolved imaging (Fig. 1); it can be shifted by 20 ps, in parallel over the whole array, using a reprogrammable phase shifter implemented in FPGA. SwissSPAD2 is thus suitable for time-resolved widefield applications such as fluorescence lifetime microscopy, thanks to the resulting deep sub-nanosecond timing resolution. While the corresponding data is currently being processed, Fig. 2 shows the fluorescence intensity image of a HeLa cell labeled with three different fluorophores, captured in a total exposure time of 12.5 ms with a camera module that drives one half of the array.

Piccolo is a **32×32 time-resolved SPAD imager**, capable of a maximum throughput of 220 million photons per second (Fig. 3, left). It also utilizes the p-i-n SPAD from [2]. Photon detection efficiency is increased with a dynamic time-to-digital converter (TDC) reallocation architecture [3], where any pixel in a column can access the first available TDC in a bank via a shared bus (in this case each column of 32 pixels shares four 50ps 12-bit TDCs). This mitigates the need for a TDC in every pixel, leading to a fill-factor of 28% in a 28.5μm pixel pitch. Each column has a dedicated 160 MHz output pad, resulting in a total bandwidth of 5.12 Gb/s. Piccolo is demonstrated in a light detection and ranging (LiDAR) application in Fig. 3, right. The sensor is here configured as a digital silicon photomultiplier, where data from all pixels is combined to form a single timing histogram. This histogram is constructed on an FPGA board (XEM7360 Opal Kelly), massively reducing the volume of data that must be communicated to the laptop via USB 3.0.

LinoSPAD is a **compact SPAD-based line camera** where **each pixel is connected directly to an FPGA** for maximum flexibility in the pixel circuitry and array interconnection (Fig. 4). It is based on a 256 SPAD sensor with a pixel pitch of 24μm and a fill factor of 41%. The FPGA implements an array of 64 TDCs capable of handling up to 133 million photons per second each (Fig. 5). TDC timestamps can be read out directly or be processed into time-of-arrival histograms enabling a wide range of applications [4]. The implementation of the sensor circuitry in reconfigurable logic enables efficient one-off applications and turns the camera in an interesting prototyping device for future sensors. The LinoSPAD camera system has been used in several applications, including transient imaging, which records the propagation of a light pulse through a scene [5]. This method enables to study light transport in and through objects to gather information about the object characteristics or to build better models for light transport for other applications.

III. Conclusions

The use of standard CMOS technologies and migration to advanced technology nodes has opened the route to high-performance SPAD implementations, two of which have been presented here (see DCR and PDP figures in Table I), with potential for low-cost volume fabrication. They have also enabled the investigation of a variety of sensor architectures, as exemplified by the gated, time-correlated and flexible imagers described in the paper, which can be matched to a variety of target applications.

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REFERENCES

[1] A. C. Ulku, C. Bruschini, X. Michalet, S. Weiss, and E. Charbon, “A 512×512 SPAD image sensor with built-in gating for phasor based real-time siFLIM,” in Int. Image Sensor Workshop, Hiroshima, 2017.

[2] C. Veerappan and E. Charbon, “A low dark count p-i-n diode based SPAD in CMOS technology,” IEEE Trans. Electron Devices, vol. 63, no. 1, pp. 65-71, 2016.

[3] S. Lindner, C. Zhang, I. M. Antolovic, J. M. Pavia, M. Wolf, and E. Charbon, “Column-parallel dynamic TDC reallocation in SPAD sensor module fabricated in 180nm CMOS for near infrared optical tomography,” in Int. Image Sensor Workshop, Hiroshima, 2017.

[4] S. Burri, C. Bruschini, and E. Charbon, “LinoSPAD: a compact linear SPAD camera system with 64 FPGA-based TDC modules for versatile 50 ps resolution time-resolved imaging,” Instruments 2017, 1(1), 6.

[5] M. O’Toole, F. Heide, D. B. Lindell, K. Zang, S. Diamond, and G. Wetzstein, “Transient imaging with SPADs,” in IEEE Int. Conference on Computer Vision and Pattern Recognition (CVPR), 2017.

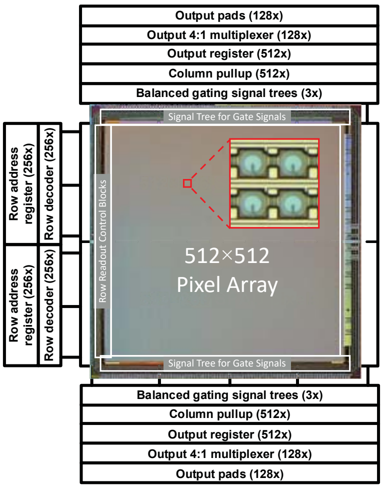

Fig. 1. SwissSPAD2 sensor architecture block diagram and die micrograph.

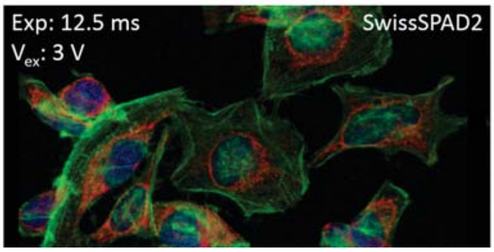

Fig. 2. Fluorescence intensity images of HeLa cells labeled with DAPI, Alexa 488, and Alexa 555, captured with SwissSPAD2. This RGB image is constructed from the intensity images of the three emission channels.

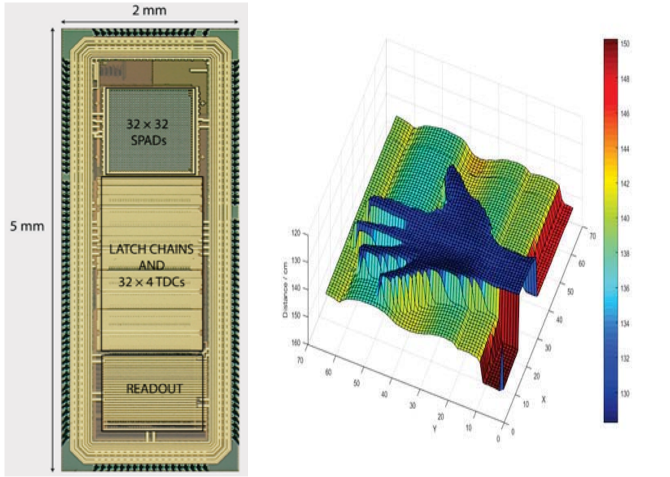

Fig. 3. Left: Piccolo 32×32 SPAD imager micrograph and main blocks. Right: 64×64 depth map of a hand obtained by raster scanning a laser point across the field of view of the camera, used here as a silicon photomultiplier. The data from each point in the field of view is acquired in 1 ms (limited by the speed of the scanner). The whole scene can be captured at 4 fps.

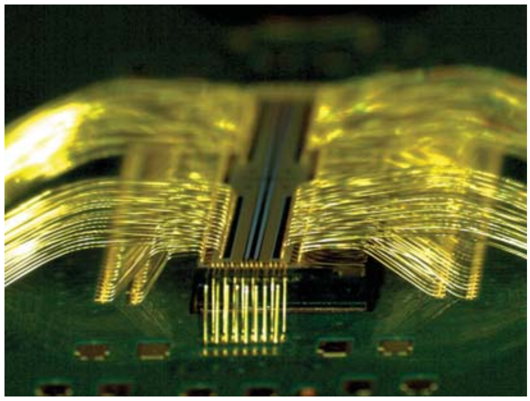

Fig. 4. LinoSPAD sensor bonded on PCB for connection with FPGA system board.

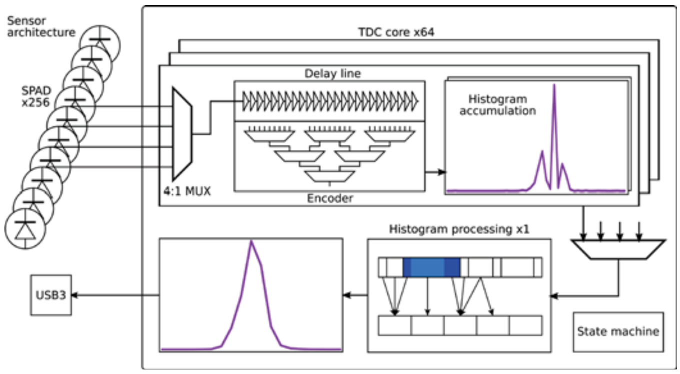

Fig. 5. LinoSPAD camera schematic with expanded FPGA firmware. The firmware contains 64 TDC modules with histogram engine shared among 4 pixels each and a common processing module for non-linearity correction.[4].

TABLE I MAIN PARAMETERS OF THE PRESENTED SPAD IMAGERS

Imager	Number of Pixels	Technology Node	DCR (median)	Pixel Pitch	Peak PDP (Wavelength)	Fill Factor (Native)	Operation Mode
SwissSPAD2	512×512	0.18 µm	8 cps/pixel	16.4 µm	> 45% @ 520 nm	10.5%	Gated
Piccolo	32×32	0.18 µm	95 cps/pixel	28.5 µm	> 45% @ 520 nm	28.5%	TCSPC[a]
LinoSPAD	256×1	0.35 µm	2000 cps/pixel	24.0 µm	> 30% @ 500 nm	41%	Flexible

[a] Time Correlated Single Photon Counting