PVT Tolerant Transconductor for Low-Voltage Highly-Selective High-Frequency Filter of MRI Front-end Receiver

by

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Abstract

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MRI machine has evolved tremendously over the years from its inception in order to render high-quality 3D images, best among its companion imaging systems. Of the whole system, RF receiver is the most crucial for its noise performance, which is expected to provide high SNR at all operating conditions. At Philips, MRI's RF receiver is based on direct-digitization architecture which has replaced the bulky data-acquisition system with an integrated on-coil receiver. It allows a lot of signal processing to be done digitally which was earlier done in analog-domain, thus improving the SNR and dynamic range to more than 100 dB. However, this has increased the design restrictions of the remaining analog front-end. The high frequency bandpass filter employed to select the signal band around the receiver's resonance frequency, has not only become highly selective (Q 400, 6^{th} order) to narrow down the signal bandwidth and reject the rest with a high stopband attenuation but also incorporates a high passband gain (60 dB), unlikely to see otherwise. Operating at a high frequency of 100's of MHz, with such a response, the filter can become drastically sensitive to the shift in its components with varying operating conditions. At Philips, the filter uses transconductor as one of its building blocks and filter frequency response is heavily dependent on the transconductance of unit cell as they are employed in large number in the circuit. The transconductor cell, at Philips, shows 15% deviation with process, supply and temperature variations. This leads to more than 10% variation in the passband gain of the filter. Operating at low supply voltage, such a deviation in MRI filter can deteriorate its output SNR and dynamic range by 10dB.

In this thesis, a new inverter based self-biased transconductance circuit has been proposed, which shows a deviation of ± 2.5% in transconductance under the process, temperature and supply variations. It limits the passband gain of the filter to 60 dB ± 2% and bandwidth shows a deviation of less than 0.1%. However, center frequency is matched precisely with the resonance frequency of receiver by the external components of the filter. Given, this matching is the basis for working principle of MRI receiver. With the proposed transconductance circuit, the filter shows an SNR of 112 dB, THD of -63 dB and consumes a power of 0.8 mW. The circuit has been implemented in 40 nm TSMC process and simulated for a temperature range of 0°C - 85°C at the power supply of 1.1 V ± 10%, post extraction.

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Contents

Contents i

List of Figures iii

List of Tables v

1 Introduction 1
- 1.1 Magnetic Resonance Imaging . . . 1
  - 1.1.1 Working Principle . . . 1
  - 1.1.2 RF Receiver . . . 3
- 1.2 Motivation . . . 5
- 1.3 State of the Art constant-g_m circuit . . . 8
- 1.4 Thesis Organisation . . . 9

2 System Design 10
- 2.1 Parallel RLC Resonator . . . 10
- 2.2 Filter Circuit . . . 13
  - 2.2.1 Filter Programmability . . . 15
  - 2.2.2 Architecture Overview . . . 16
  - 2.2.3 Previous Circuit . . . 19
  - 2.2.4 PVT Tolerance . . . 22

3 Circuit Implementation 27
- 3.1 Transconductor cell . . . 27
  - 3.1.1 Constant-g_m Biasing . . . 27
  - 3.1.2 Self-biased Transconductor . . . 33
  - 3.1.3 Complete "constant-transconductance" circuit . . . 36
- 3.2 Filter . . . 38
  - 3.2.1 Fully-Differential Filter . . . 38
  - 3.2.2 Parasitics in Filter . . . 40
  - 3.2.3 Programmability . . . 43
- 3.3 Layout . . . 45

4 Results **48**
4.1 Transconductor . . . 48
4.1.1 Transconductance Variation . . . 48
4.2 Filter . . . 52
4.2.1 Frequency Response . . . 54
4.2.2 Gain at Center Frequency . . . 56
4.2.3 Bandwidth . . . 58
4.3 Filter Performance . . . 60
4.3.1 Noise . . . 60
4.3.2 Distortion . . . 61
4.4 Achieved Results . . . 62

5 Discussion **63**
5.1 Transconductance circuit . . . 63
5.2 Filter circuit . . . 65

6 Conclusion **67**
6.1 Thesis contributions . . . 67
6.2 Future work . . . 68

Bibliography **69**

A Filter system modelling **72**

B More results **75**

List of Figures

1.1 Working principle of MRI [4, 5] . . . 2
1.2 Block diagram of MRI receiver's analog front-end . . . 3
1.3 Block diagram of MRI receiver's analog front-end with direct digitization . . . 4
1.4 Signal at the input of RF ADC [12] . . . 5

2.1 Circuit for illustrating the natural response of the parallel RLC circuit [27]. . . . 11
2.2 Natural response of parallel RLC circuit [27] . . . 12
2.3 LC filter . . . 13
2.4 Magnitude and Phase response of the desired filter . . . 14
2.5 Switchable transconductor for programmability . . . 16
2.6 Filter Architecture for MRI Receiver . . . 16
2.7 Ideal frequency response of the filter (excl. sixth zero) . . . 17
2.8 Fully-differential filter schematic using previous transconductor cell . . . 20
2.9 Previous transconductor implemented filter response - simulation results . . . 21
2.10 Concept of constant-g_m biasing . . . 24

3.1 Schematic of the proposed biasing circuit . . . 28
3.2 Operational Amplifier used for negative feedback loop in bias block . . . 31
3.3 Binary weighted 4-bit resistance bank. . . . 32
3.4 Proposed Transconductor . . . 33
3.5 Small-signal model of proposed transconductor . . . 35
3.6 Complete "constant-transconductance" circuit . . . 36
3.7 Fully-differential filter using proposed transconductor . . . 39
3.8 Equivalent model of the transconductor with parasitics . . . 40
3.9 Concept and implementation of negative resistance . . . 41
3.10 Negative resistance implementation with proposed transconductor . . . 42
3.11 Compensation for parasitic capacitance of transconductor . . . 43
3.12 Switches configurations in transconductor for filter programmability . . . 44
3.13 Transconductor cell Layout . . . 45
3.14 Floor plan of the g_m-cells tiling to construct Gm block . . . 46
3.15 Bias Block Layout. Transconductor cell shown for relative area . . . 47

4.1 g_m variation with temperature (curves with same colour show supply variation) 49

4.2 g_m variation with supply (curves with same colour show temperature variation) 49
4.3 Proposed transconductor g_m variation - Zoomed in 51
4.4 Transconductance variation with device mismatch using Monte Carlo simulation 52
4.5 Fully-differential filter using proposed transconductor 53
4.6 Filter frequency response. Comparison with ideal response (magenta) 55
4.7 Phase comparison between schematic and extraction with respect to the ideal . 56
4.8 Deviation in gain at f_0 (127.8MHz) of filter with supply and temperature 57
4.9 Monte Carlo simulation for deviation in gain at center frequency 127.8 MHz . . 57
4.10 Deviation in bandwidth (Δf) of filter with supply and temperature variation . . 58
4.11 Monte Carlo simulation for deviation in Δf 59
4.12 Filter magnitude response on absolute scale 60
4.13 Output noise power spectrum of filter 61
4.14 Distortion spectrum of the filter 62

A.1 Filter Architecture 72

B.1 Schematic simulation with normalized R_B. g_m variation with PVT 75
B.2 Schematic simulation with R_B as R_{bank}. g_m variation with PVT 76

List of Tables

1.1 Target Performance for the Proposed Transconductor 7

2.1 Poles and zeros of MRI filter 14
2.2 Component values (RLC) of three resonators corresponding to their poles 18
2.3 Transconductance per Gm block in ideal filter 18
2.4 Number of transconductor cells per Gm block in ideal filter 19
2.5 Number of transconductor cells per Gm block in previous circuit 20
2.6 Resonator components for previous transconductor implemented filter. L=50nH 22

3.1 Opamp in bias circuit. L= 0.5μm, except for M8 31
3.2 Programmable 4-bit binary weighted resistance bank 32
3.3 Transconductance per Gm block in ideal filter 38
3.4 Number of proposed transconductor cells per Gm block in filter 39
3.5 Resonator components for proposed transconductor implemented filter. L=50nH 41
3.6 Decoupling capacitance for Gm block in filter 43

4.1 4-bit digital code of resistance bank for process corner 50
4.2 Number of proposed transconductor cells per Gm block in filter 52
4.3 Resonator components of the filter after extraction of proposed g_m-cell. L=50 nH 54

5.1 Performance comparison of constant-g_m circuit 65

A.1 Poles and zeros of MRI filter 72
A.2 Component values (RLC) of three resonators (Z_{1-3}) corresponding to their complex-conjugate poles 73
A.3 Transconductance per Gm block in ideal filter 74
A.4 Scale factor of transconductor cells in ideal filter 74

Chapter 1

Introduction

1.1 Magnetic Resonance Imaging

Magnetic resonance imaging (MRI) is the most sophisticated clinical imaging system (CIS) compared to its counterparts like X-ray, CT and PET since it provides high-quality 3D images with relatively safe environment due to the absence of ionizing radiations, unlike others.

1.1.1 Working Principle

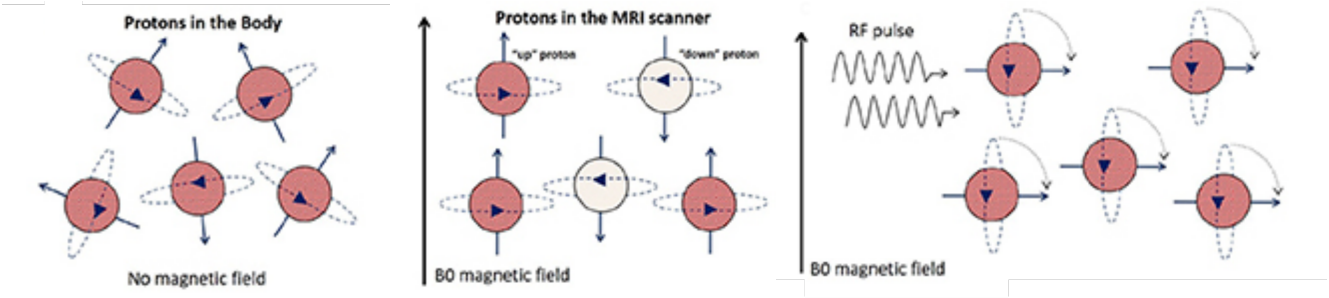
MRI is based on the principle of nuclear magnetic resonance (NMR). According to which, nuclei with an odd number of neutrons possess a nonzero nuclear spin, as a result they can be magnetized in an external field [1]. Our body carries multiple such nuclei like $\mathtt{H}^{+}$, $\mathtt{Ca}^{2+}$, $\mathtt{Mg}^{2+}$, $\mathtt{Na}^{+}$ etc which behave as dipole and can be scanned under MRI to determine the shape of the body tissues. MRI machine uses three fields - static magnetic field, radio frequency (RF) pulse and gradient field. The working principle is illustrated in Fig. 1.1. As soon as the static magnetic field (B_0) is turned ON, the target nuclei, say protons ($\mathtt{H}^{+}$) are magnetized and begin to precess about the axis of B_0 at Larmor frequency. Following which an RF pulse, transverse to the plane of B_0, is transmitted at Larmor frequency, this turns the nuclei transverse to B_0. Once the RF excitation is removed, the nuclei return back to their steady state, releasing the energy which is sensed by the RF receiver. The process of RF excitation and reception is repeated several times under the variation of gradient field to generate 3D images from 2D scans.

Here, precession is a motion of nucleus alike a "spinning top" and the Larmor frequency is defined as the rate of precession of the magnetic moment of the nucleus around the static magnetic field, B_0 [2] , which is given as

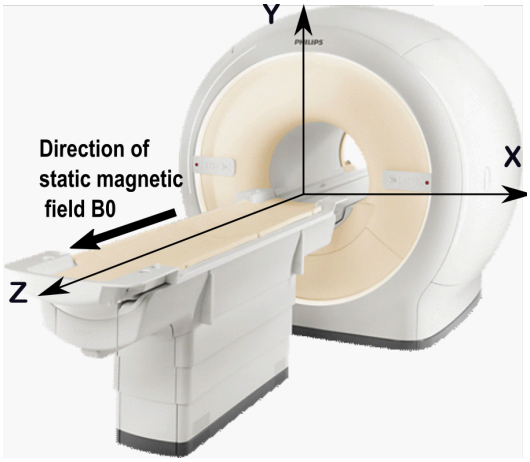
$$f_0 = \gamma B_0 \tag{1.1}$$

where, f_0 is the Larmor frequency in MHz, B_0 is the static magnetic field in tesla (T) and γ is gyromagnetic constant (42.6 MHz/T for $\mathtt{H}^{+}$) which depends on the target nucleus.

B_0 is the main field of MRI, so the machine is denoted with B_0 strength only say three tesla (3 T) MRI. Using the Larmor equation, the Larmor frequency of protons for 3 T machine is 127.8 MHz. A resonance is achieved between the protons and the RF receiver at Larmor frequency such that the released energy of protons is transferred onto the receiver, which senses the change in magnetic flux in the coil and induces current [3]. Following the Faraday's law, the amount of change in flux is proportional to the induced current. Hence, the quality of the received signal depends on how exact is the matching between the receiver electronics with that of the resonance frequency to minimize any possible loss of information.



(a) Protons without field (b) Protons in B_0 (c) Protons in B_0 and RF pulse



(d) MRI axis labeling

(e) Philips dstream Receiver

Figure 1.1: Working principle of MRI [4, 5]

1.1.2 RF Receiver

The precision of MRI system electronics is very high in order to render best quality 3D images incomparable to any other imaging system. In which the front-end of RF receiver is the most crucial, its goal is to achieve highest possible signal-to-noise ratio (SNR) for all operating conditions [1]. Being the first point of contact towards the receiving end, it is a deciding factor for SNR. Fig. 1.2 shows the classic RF receiver which aligns with the MRI RF receiver in general. It begins with antenna, here RF coil, to receive the signals reflected off the patient's body, followed by a low-noise amplifier (LNA) to suppress noise and amplify the signal, then a bandpass filter to select the desired band of interest, near Larmor frequency and then a signal processing chain from mixer till A-to-D driver to down-convert the RF signal into intermediate frequency (IF) so as to be digitized easily via analog-to-digital converter (ADC) in baseband. Following which, the signal is off for conversion into images in digital domain with the help of computer software and finally renders the output on the screen.

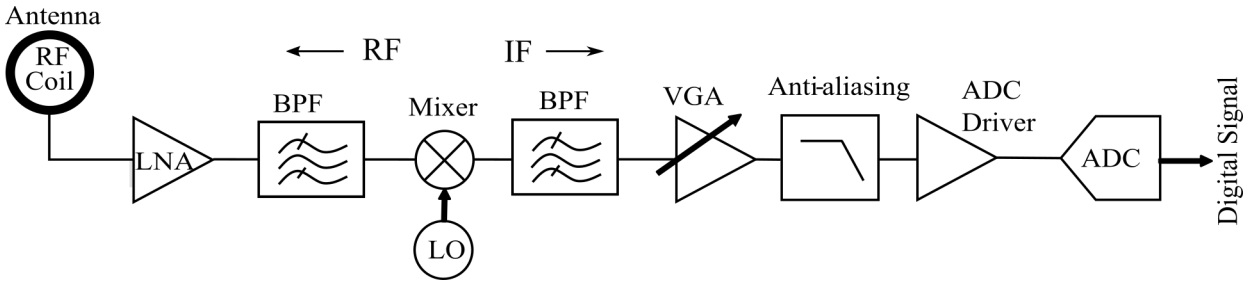


Figure 1.2: Block diagram of MRI receiver's analog front-end

The received signal is prone to noise from three sources. First, the stray radiations from the radio objects in the examination room. Second, the receiver electronics itself and third the thermal radiations from the patient's body. Of these the former two can be minimized by copper shielding the room and improving the receiver's electronic components respectively [6]. But the latter is inevitable and comparatively larger. Although patient's thermal noise can be modeled for a given configuration of receiver coil. It is generated from the random variation of charged particles in the patient's body tissue. Thus the signal which is of the order of few mV, available at the front-end is highly susceptible to noise. In traditional MRI receiver, the low-level RF input signal was transmitted over coaxial cable to MRI data acquisition system for signal processing, placed out of the examination room. In other words, from RF coil to LNA the signals were passed over long coax making it highly susceptible to interference[7]. Thus to ensure a high-quality image from a system view, the SNR of the receiver electronics should be higher than 90 dB [8]. The quest for higher SNR has been mostly realized with surrounding factors so far like increasing the static magnetic field B_0, increasing the number of channels, using parallel-imaging and averaging - taking multiple scans for the region under inspection and so on. But little had been done in the analog

front-end electronics until past decade. This has lead to bulky coaxial cables and connectors, increase in cost and scan time for MRI.

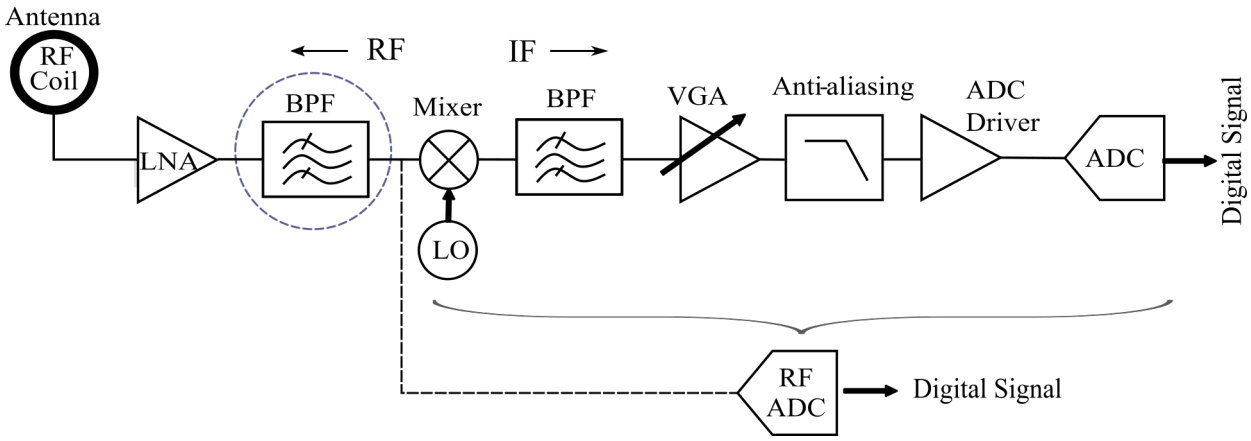


Figure 1.3: Block diagram of MRI receiver's analog front-end with direct digitization

Now with the advancement in CMOS technology, a lot more improvements can be done in analog front-end leading to the invent of on-coil receiver, i.e. using an integrated broadband receiver that digitizes the signal at the MRI machine itself. It is a paradigm shift in the MRI machine with lower interference, higher image quality, faster scan, lower power and thereby reducing the cost as well [7]. This has been made possible due to the direct digitization receiver architecture. It employs the high speed ADC known as RF sampling ADC to digitize the signal in RF band only. At Philips, MRI machine uses the direct digitization and its receiver architecture is referred to as dstream, shown in Fig. 1.1e [5]. The analog front-end of the RF receiver after employing the direct digitization is shown in Fig. 1.3. In this receiver architecture, single RF sampling ADC can replace the IF sampling subsystems including mixer, local-oscillator synthesizer (LO), amplifiers (VGA, ADC driver), filters and ADC [9]. It increases the digital integration and omits the need for down-conversion in analog-domain which is now moved to digital processing units such as ASIC/FPGA or can even be done inside RF ADC with custom integrated circuit (IC) design [10]. Digital signal processing has long been preferred causing analog electronics to shrink, for its immunity to noise and capability of reusing the same hardware for multiple configurations. It allows a lot more compact hardware, low power and low noise solution to the MRI receiver. However, at the same time, the specifications for remaining analog front-end now become stringent.

1.2 Motivation

As per the working principle of MRI, in order to receive the maximum signal strength, the RF excitation and reception takes place precisely at the Larmor frequency, say 127.8 MHz(for H^+ at 3 T). This implies that the signal of interest is only available around Larmor frequency. However, a wideband signal is fed into an RF sampling ADC, making it susceptible to noise. As a result, RF sampling ADC can limit the sensitivity of the receiver which refers to the minimum signal sensed efficiently. Whereas in IF receiver with the help of mixer, LO and ADC driver a sufficient gain has been added to the signal before ADC, raising the signal well above the noise-level also being at baseband the noise bandwidth was smaller [11] .

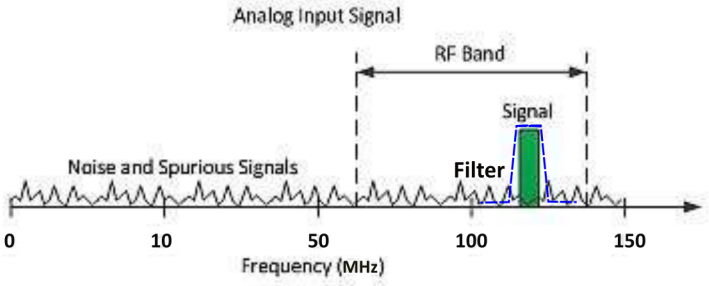


Figure 1.4: Signal at the input of RF ADC [12]

One of the efficient way of reducing the noise is to reject the undesired frequency band from the received signal with high stopband attenuation as shown in Fig. 1.4. That's the role of the front-end bandpass filter placed before the RF ADC in Fig. 1.3. The MRI front-end bandpass filter is employed to select the narrow band around the Larmor frequency and reject the rest of the input signal, i.e. suppressing noise in the stopband. The MRI front-end bandpass filter hereafter is termed as filter. Due to RF sampling ADC, the filter requires to be indispensably precise ahead of it. In such an SNR-critical application, a highly selective filter ($Q > 300$) is required with sharp roll-off and high stopband attenuation (70 dB-80 dB). In addition, it should prevent the desensitization of receiver with its high passband gain (50 dB-60 dB) compensating the gain of the signal-chain otherwise added by mixer, LO and ADC driver. In contrast, the filter for the classic receiver would have relaxed specifications with a sufficient stopband attenuation (60 dB) at nominal selectivity ($Q < 50$) with low or even no passband gain (0 dB).

Such strict requirements of the filter make it highly sensitive to the deviation in its components under variable operating conditions. At a high frequency of hundreds of MHz, one can expect even a small deviation in filter response will not only pass but also amplify the noise separated with few tens of kHz that should have been suppressed otherwise in stopband. This can deteriorate the SNR of receiver. Being a medical device of high precision it is required that the filter response should remain stable with the change in operating

conditions due to temperature of the environment, voltage supply fluctuation and process artifacts. Also, there is an associated concern of power dissipation in MRI electronics, due to which the operating supply voltages are lower which makes it even more complicated to achieve high dynamic range of the filter with such a response. Choosing an appropriate architecture of the filter can limit these variations.

The desired frequency response of the filter is defined by Philips based on their receiver architecture and so does the filter architecture as well. Philips adopted a sixth-order RLC bandpass filter for this purpose. Apart from passive components (LC tanks), the filter uses active components, i.e. transconductor. Transconductor acts as a gain element of the filter as well as a current source preventing the interference between the tanks. Transconductor blocks are implemented in the form of parallel-connected discrete cells for the feature of wideband programmability of the filter IC. The filter is further detailed in Chapter 2-*System Design*.

Transconductance (g_m) is of our interest here, which is the key parameter for passband gain and bandwidth of the adopted filter architecture. Transconductor's g_m is susceptible to variations as it is a function of process and temperature dependent variables. The currently employed transconductor is no exception and faces a deviation in g_m of more than 15% with process, temperature and supply variations. Consequently, deviation in g_m will lead to variation in the filter's gain (>10%) and bandwidth. Operating at low voltages, this will significantly deteriorate the SNR and dynamic range of the filter, hence that of the receiver. The total number of transconductor cells in the filter are more than 200. Having such a large quantity of transconductor cells makes the situation even more vulnerable, cascading the effect of deviation in a single cell on the filter response rendering it to become highly sensitive to g_m. The goal of the study is to achieve a constant g_m of the unit transconductor cell such that the filter response remains intact. The three variations that have been considered are defined as follows, also termed as PVT variations.

1. Power Supply : As it is a medical device, the power supply is well maintained during the MRI examination process. However, a variation of 10% about the operating voltage of 1.1 V is considered, i.e. voltage range is 0.99 V - 1.21 V. The origin of supply variation comes from two factors. First, the filter IC is the analog-mixed-signal chip, i.e. it has digital as well analog circuit implemented on the same chip so there is a high vulnerability of substrate noise from its digital counterparts. Moreover, 1.1 V is not an external supply, but generated on-chip with power converters this can lead to high frequency switching signals in the locally generated supply.

2. Temperature : Period of MRI scan can vary between 20 - 50 minutes [13]. The power dissipation in receiver electronics can result in thermal heating and prolonged exposure to the RF radiation can raise the temperature of the patient's body, also it may cause the electronics to heat up in RF field [8]. However, according to the safety standard IEC 60601-2-33[14], the increase in core body temperature shall be less than 1°C. This suggests that power dissipation in the receiver electronics remain the primary

source of increase in temperature. To ensure the performance of the medical device the temperature range of 0°C - 85°C is considered. Although, for safety and ambient experience of the patient 0°C and 85°C are extreme ends and less likely to occur.

3. Process corner: Process corners are the artifact of the IC fabrication. It occurs due to the non-uniformity of the doping level across the ICs on the same silicon wafer, depending on their location on the wafer. The transistors which receive lower doping are called slow(s) corner while the one with higher doping levels are called fast(f) corners. The variation in doping levels increase or decrease the threshold voltages of the respective corners. In our analysis, we have considered all five process corners – ss, ff, sf, fs and tt. The naming is conventional. The first letter denotes the type for N channel MOSFET (nMOS) and latter for the P channel MOSFET (pMOS). For example, sf implies slow nMOS and fast pMOS. While 't' refers to typical or nominal corner, that is when doping levels of the devices are same as expected.

The desired transconductor specifications are guided by the filter which is a sixth-order RLC bandpass filter with a high Q-factor of 400. It has a center frequency of 127.8 MHz (for 3 T, H^+), passband gain of 60 dB and bandwidth of merely 350 kHz. The tolerance of passband gain variation is about 2% and that of bandwidth is less than 0.5%, while the center frequency is finely tuned to the Larmor frequency (127.8 MHz) by the LC tank. For such a filter response, the unit transconductor cell has an acceptable g_m deviation of around 2% under the PVT variations, thus filter will have the subsequent performance as listed in Table 1.1 as compared to the one with previous transconductor.

	Previous Transconductor	Target Transconductor
Center frequency (Hz)	127.8M	
Order of Filter(biquad)	6^{th}, Bandpass	
g_m with voltage (0.99V-1.21V)	15%	∼2%
g_m with temperature (0°-85°C)	10%	∼2%
Passband Gain of filter	10%	∼2%
-3 dB BW of filter	0.5%	<0.5%
SNR of filter (dB)	110	110

Table 1.1: Target Performance for the Proposed Transconductor

The scope of this study is to investigate into the new transconductor cell and its respective biasing circuit to achieve the target performance as listed in Table 1.1 with respect to the previous transconductor (the one used at Philips). These specifications also implicate the

constraints such as low power supply (1.1 V), wide bandwidth (> 300 MHz) and low noise requirement on transconductor cell. The study includes three stages of design - architecture, transistor-level implementation and layout of the proposed transconductance circuit. It shall be noted that the passive components constructing the LC tank are placed off the chip and the filter IC being a mixed-signal chip is out of scope to layout. Although, the performance has been analyzed at the system level of filter using post-layout simulations of proposed transconductance circuit and modeling the off-chip components.

1.3 State of the Art constant-g_m circuit

In literature, several times the technique of constant-g_m biasing has been used to achieve a stable g_m with PVT variations [15, 16, 17, 18, 19, 20, 21, 22]. The implementation of the technique is conditioned to the application. So far, none of them has implemented it for a high frequency programmable filter with very high selectivity and passband gain.

Although [15] presents a programmable wide bandwidth filter for a range of 60 - 350 MHz but it is a low pass type with no gain (0 dB), relatively smoother response, i.e. Q $<$ 50 and acceptable cut-off frequency deviation of 2%. Whereas in this MRI specific filter, there exists a high passband gain of 60 dB which is a major function of g_m of the transconductors, while the center frequency is independent of the g_m, accurately held by LC tank to align with the Larmor frequency, so there is difference in the key parameters of the two systems. In [16, 20, 22], beta-multiplier is used based on square-law model which doesn't hold true for modern day short-channel process technology. In [15, 20, 22, 18], transconductance tracks the off-chip resistor, which is a costly solution and also suffers from parasitic pole-zero pair at lower frequency. Hence, it requires a large off-chip compensation capacitor[17]. In [17, 23], master-slave topology has been adopted to implement the on-chip resistor. [17] uses MOS operating in triode region as the resistor which is controlled by a switched capacitor network in a feedback loop. [23] uses an on-chip oscillator to tune the resistor precisely, but both are implemented for relatively lower frequency of few MHz only. In [19], author presents the transconductor biased in sub-threshold with on-chip switched-capacitor resistor but it is used for low frequency lower-order filter.

Moreover, looking at the constraints for our case, a lower power supply is available for the filter circuit. We know, the MRI front-end receiver has the requirement of high dynamic range. This implies there is a need for high input-output swing of the filter close to supply rails. In [24, 20, 23], inverter based transconductor is used for low-voltage application biased with constant-g_m methodology. Of which, [20] presents the application for high order bandpass filter. But all of them have a comparatively higher acceptable variation in center frequency/cut-off frequency deviation for their respective application. 10% for [24, 20] and 4% for [23]. [25, 26], presents a self-biased common-mode control for differential pair but not used in conjunction with constant-g_m bias methodology.

None of these align with all the criterion to be fulfilled for our design due to the difference in system-application, operating conditions and implementation level.

1.4 Thesis Organisation

The thesis is organized in four parts from chapter 2 to chapter 6 - system design, circuit implementation, results, discussion and conclusion.

- Chapter 2 provides study of the system design which includes choice of filter type, programmability feature, filter architecture and its implementation chosen by Philips. Further, it also describes the issues in the previous implementation of transconductor and looks into design challenges associated with PVT tolerance of the transconductor. Following which, constant-transconductance biasing technique is discussed as a potential solution.

- Chapter 3 presents circuit implementation of the proposed transconductor and its biasing circuit. It analyzes the chosen design with respect to the requirements. Further, this chapter presents the MRI filter using the proposed transconductor and tuning of the resonators after incorporating the parasitics. Also, switch configuration of the transconductor is presented here for the filter programmability. Lastly, the chapter presents the layout of the two blocks, the proposed transconductor and its bias.

- Chapter 4 presents the post-layout results and comparisons with the previous transconductor circuit. First, the standalone transconductor results are shown, then the impact of the proposed transconductor on the stability of the MRI filter's frequency response has been presented in terms of its passband gain and bandwidth. Lastly, it shows the performance of the filter in terms of noise and distortion.

- Chapter 5 presents the discussion on the design elements, highlighting the positives and trade-offs made. Also, a performance comparison of the proposed transconductor with respect to the state-of-the-art design has been done in this chapter.

- Chapter 6 provides an overall conclusion of the study and highlights the contributions made in this thesis. Lastly, it provides some insight into the possible improvements that can be taken up further in future.

There are two appendices provided at the end that can be referred for more details as it may require for further understanding of the reader.

Chapter 2

System Design

As we had discussed in the previous chapter, the front-end of MRI receiver requires a highly- selective bandpass filter to select the region around the Larmor frequency only, while drastically attenuate the noise in the rest. This becomes challenging due to direct-digitization. While operating at such a high frequency of hundreds of MHz one can expect noise separated between passband and stopband with few tens of kHz, which is quite small in logarithmic scale but significant for the application of MRI. In addition, given that MRI is an SNR-critical application, feeding the RF signal directly into the ADC, because of direct digitization, makes the receiver vulnerable to be desensitized, having to digitize the input signal without sufficiently separating it above the noise floor. Hence, there is a requirement of a bandpass filter with a very sharp roll-off to limit the noise bandwidth much closer to the passband as well as high gain to amplify the signal before sending it to RF ADC. On top of this, the stability of the filter's frequency response has to be maintained for the precision of MRI.

In this chapter, first, the theory of parallel RLC circuit is discussed, which is one of the building blocks of the filter architecture. Then, the filter architecture has been detailed, the one adopted and employed by Philips to meet the requirements of the MRI front-end receiver. Following which, the implementation of the filter circuit with the previous transconductor has been discussed and analyzed. Lastly, the challenges to achieve stable transconductance circuit have been discussed and the concept of constant-transconductance biasing methodology is presented, which is adopted to fulfill the requirements.

2.1 Parallel RLC Resonator

A highly selective bandpass filter can be realized very accurately using parallel RLC resonator. RLC resonators are widely used as tuning circuit for their ability to select narrow band from the radio signal. They can be tuned to exact pole frequency, also termed as resonance frequency, ω_0 as well as can achieve high Q-factor by choosing appropriate value of its components as defined in Eq. (2.1). At high frequencies of hundreds of MHz the inductor and capacitor lies in the order of tens of nanohenry and picofarad range respectively, which

can't be monolithic but placed off the chip. Q-factor for the system is defined as the ratio of peak energy stored in the circuit to the energy dissipated at resonance per radian. In terms of the filter it denotes the ability to pass the selected band of frequencies and reject the stop band.

$$\begin{aligned} \omega_0 &= \frac{1}{\sqrt{LC}} = 2\pi \cdot f_0 \\ Q &= R\sqrt{\frac{C}{L}} \end{aligned} \tag{2.1}$$

for band pass system,

$$Q = \frac{\omega_0}{\Delta\omega} \tag{2.2}$$

As per the requirements of Philips' MRI receiver, the filter needs a Q-factor of 400 at center frequency of 127.8 MHz for protons in 3 T MRI machine. In Eq. (2.2) $\Delta\omega$ represents the bandwidth that is defined as the difference between the -3 dB frequencies about the center frequency ω_0. For the center frequency(f_0) of 127.8 MHz and Q of 400 , the calculated bandwidth is 350 kHz, which is an extremely narrow band. To achieve high-selectivity, one can increase the Q-factor and the order of the filter. Higher order implies more number of storage elements. To realize such a filter, suitable components shall be selected. To determine the component selection, the understanding of the frequency response of the parallel RLC circuit is illustrated. Fig. 2.1 represents the the parallel RLC circuit for natural response analysis [27].

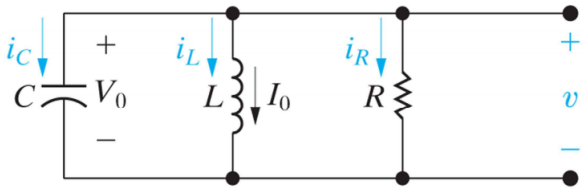


Figure 2.1: Circuit for illustrating the natural response of the parallel RLC circuit [27].

From Fig. 2.1, the equation for the differential voltage across the circuit can be given by

$$\begin{aligned} &\frac{v}{R} + \frac{1}{L}\int_0^t v d\tau + I_0 + C\frac{dv}{dt} = 0 \\ &\frac{1}{R}\frac{dv}{dt} + \frac{v}{L} + C\frac{d^2v}{dt^2} = 0 \end{aligned} \tag{2.3}$$

If we take the Laplace transform of the Eq. (2.3) we get the characteristic equation of the parallel RLC circuit.

$$s^2 + \frac{s}{RC} + \frac{1}{LC} = 0 \tag{2.4}$$

From this the roots of the quadratic equation can be calculated that is the poles of parallel RLC circuit's frequency response.

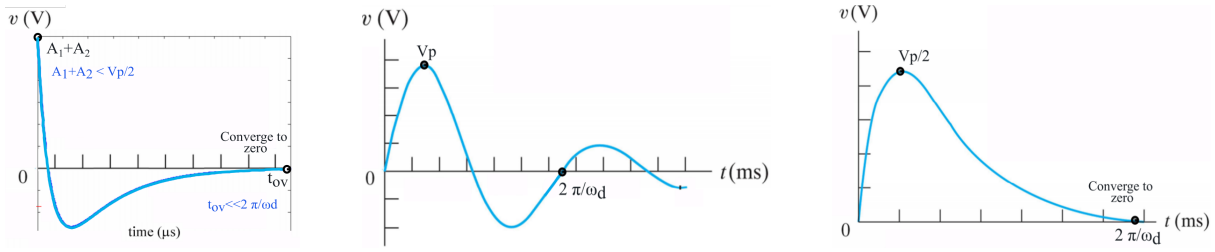
$$s_1, s_2 = \frac{-1}{2RC} \pm j\sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}} \tag{2.5}$$

$$\text{Neper frequency, } \alpha = \frac{1}{2RC}$$
$$\text{Resonant frequency, } \omega_0 = \frac{1}{\sqrt{LC}}$$

In time-domain, the solution of the characteristic equation Eq. 2.4 can be denoted as in Eq. 2.6, where A_1 and A_2 are the coefficients.

$$v = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{2.6}$$

There are three possible behaviours of the natural response guided by the ω_0 and α, independent of A_1 and A_2. If $\omega_0^2 < \alpha^2$, the response is overdamped, if $\omega_0^2 > \alpha^2$, the response is underdamped and if $\omega_0^2 = \alpha^2$, the response is critically damped. In time-domain, the damping represents the way the response reaches its final value, i.e. steady state value which is governed by the damping frequency, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ [27]. Hence, for a characteristic equation of a particular parallel RLC circuit, the three different natural response are possible depending on the value of the resistance as shown in Fig. 2.2.



(a) Overdamped (b) Underdamped (c) Critically damped

Figure 2.2: Natural response of parallel RLC circuit [27]

For the implementation of MRI front-end filter, there is a requirement of 60 dB gain (otherwise, 0 dB - 20 dB) in the passband with infinitesimally small loss of energy. One can visualize a response along the similar lines of underdamped case above but with increased peak-to-peak amplitude and very slow decay over time. Parallel RLC is a passive circuit, so to add gain there is a need of an active element to be included in the configuration that sources energy. The chosen active element is the transconductor which acts as a current source without disturbing the construct of LC tank, i.e. prevent any interference between the tanks [28]. For such a filter, it can be said that the component values are strongly guided by the desired poles and passband gain where R, L, C depend on poles and transconductance (g_m) depends on gain.

2.2 Filter Circuit

As per the requirements of the MRI receiver at Philips, the filter needs a Q-factor of 400 and three complex-conjugate pairs of pole, i.e. sixth order to achieve the desired high selectivity. To implement an analog filter, the four commonly used configurations are active-RC, g_m-C, switched capacitor (SC) and LC. SC filters are resilient to PVT variations. However, they are prone to noise due to the clock feedthru as well as preferable for relatively low-order low frequency operation. In active-RC and g_m-C, the pole/zero locations are defined by the R (or $1/g_m$) and C, so their stability depends on the matching achieved. Active-RC filters suffer from poor matching of R and C, thus time constants vary upto 30% with PVT variation [29]. However, g_m-C filters can achieve a good matching to provide stable filter response with high-order high frequency operation, but Q is limited to less than 100. This is because Q in g_m-C is based on the transconductance division. Also, active filters are prone to noise and non-linearity.

On the other hand, LC filters can implement Q as high as 1000 with high-order and high frequency of operation that too with low noise and good linearity [30]. In addition, the locations of time constants are accurately determined by the discrete components (L and C) providing stable response with PVT variations. Given the priority of noise, selectivity and accuracy of the filter in MRI front-end receiver, the LC implementation is best suited.

The filter IC is designed to be programmable for a range of 64 MHz -128 MHz, i.e. using same IC for a range of Larmor frequencies. In addition, there is a need of high gain (60 dB) in the passband. Hence effectively, the filter is a tunable amplifier [28]. For gain, an active element can be placed in parallel to the LC tank. An LC filter is as shown in Fig. 2.3. At resonance, the effective impedance, Z(s) of the RLC filter is only resistance, R so the voltage at the output, $Vout$ is directly proportional to current, $g_m V_{in}$, i.e. $Vout = -g_m V_{in} * R$. Thus, it can be said that the gain of the LC filter is $g_m R$, where R is constant decided by Q-factor of the filter.

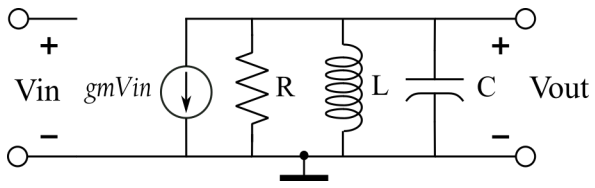


Figure 2.3: LC filter

The transfer function of the filter in Fig 2.3 can be written as

$$\frac{V_{out}}{V_{in}} = -g_m Z(s) = \frac{-g_m}{C}\left(\frac{s}{s^2 + \frac{s}{RC} + \frac{1}{LC}}\right) \tag{2.7}$$

Pole (MHz)	Zero (MHz)	Q_{pole}
-0.160 ± j 127.800	-5.578 ± j 129.656	400
-0.159 ± j 127.200	-3.003 ± j 125.816	400
-0.160 ± j 128.400	-150.900 & 0(origin)	400

Table 2.1: Poles and zeros of MRI filter

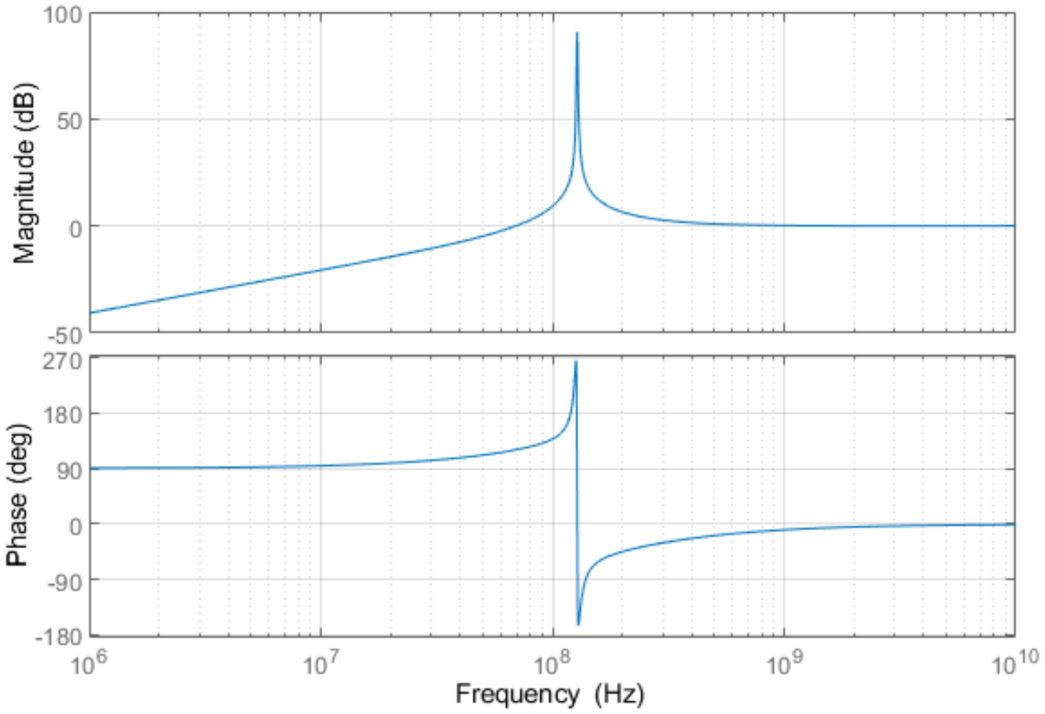


Figure 2.4: Magnitude and Phase response of the desired filter

The desired poles and zeros of the filter are defined in Table 2.1 and the corresponding frequency response is shown in Fig 2.4. From the frequency response of the filter, the poles and zeros can be identified as follows. There exists a zero at the origin, providing +90° phase shift. It is followed by two pairs of complex-conjugate zeros at 125.8 MHz and 129.7 MHz that surrounds the three pairs of complex-conjugate poles at 127.2 MHz, 127.8 MHz and 128.4 MHz. This marks the passband of the filter with Larmor frequency (127.8 MHz) at the center. This band brings a phase shift of -180°. Until here, we have our five zeros and six poles. Further, at 151 MHz there occurs the sixth zero shifting the phase by +90° bringing the resultant phase to 0°, for it is a biquad filter.

Three resonators can be placed in a cascaded fashion to implement the poles. Each resonator represents a second order section, adding up to sixth order of the filter. Resonator

frequencies are chosen close to each other, such that the Larmor frequency is in the middle of the three. Such a configuration prevents any major deviation in the filter response at the Larmor frequency, which can otherwise be impacted by the variation in field strength or MRI system electronics, thereby slightly shifting the resonance frequency of the receiver. To limit the phase shift across the filter to less than 180° as well as achieve flat passband six zeros are realized making it a biquad filter.

2.2.1 Filter Programmability

MRI filter IC incorporates the capability of tuning to a range of center frequencies from 64 MHz - 128 MHz. This means same filter IC can be employed in multiple scan machines as well as for varied nucleus targets. Center frequency of the filter is the resonance frequency of the receiver that is equal to the Larmor frequency, which depends upon the target nucleus and strength of MRI machine given by Eq. (2.8) (reiterating here for continuity), where f_0 is the Larmor frequency in MHz, γ is the gyromagnetic constant(for H^+, 42.6 MHz/T) and B_0 is the strength of static magnetic field in tesla (T).

$$f_0 = \gamma B_0 \tag{2.8}$$

In LC filter inductor and capacitor, being off-chip components, can be chosen as per the requirements of new resonance frequency of the receiver guided by the Larmor frequency. The off-chip capacitance is employed in conjunction with an on-chip variable capacitance, which is primarily used to incorporate parasitics in filter, will be discussed later. Given, high frequency operation, a change of few hundred's of fF can change the resonance frequency of filter in the order of MHz. Hence, new resonance frequency differed by few MHz can be realized without any variation in off-chip components but only using the integrated capacitance bank, upto a range of 2pF. However, in case of larger changes in resonance frequency, inductor and capacitor both should scale proportionally to keep the Q-factor constant.

For example, in case of scanning flouride ions (F^-) instead of proton (H^+, 128 MHz) in 3 T machine whose Larmor frequency is 120 MHz [31] which can be achieved by the on-chip capacitance bank without much deviation in Q-factor. Whereas, in case of protons under 1.5 T MRI machine, the Larmor frequency is reduced to half, 64 MHz. To achieve resonance at this frequency off-chip capacitance and inductance both are doubled maintaining the same Q-factor.

While programming the filter to a different resonance frequency, shape of the filter response should remain intact. This is achievable if we make the components on IC, i.e. transconductor, switchable. This will enable a complete freedom of varying the filter components as per the requirement of chosen filter configuration. Fig. 2.5 shows the transconductor Gm block as a group of parallel connected N transconductor cells whose switches are controlled by a digital selection signal "sel". Array of signal "sel" can be controlled by a binary decoder at the top level.

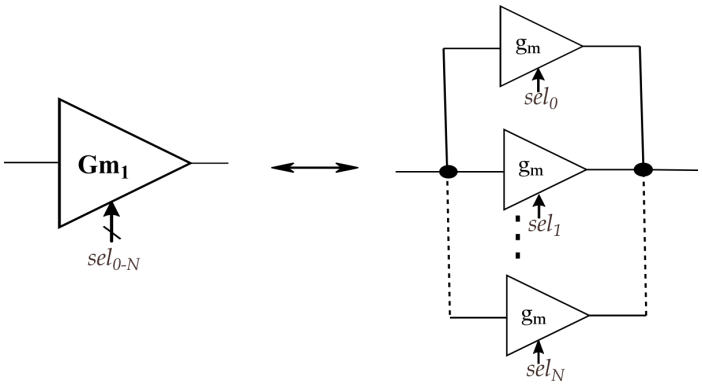
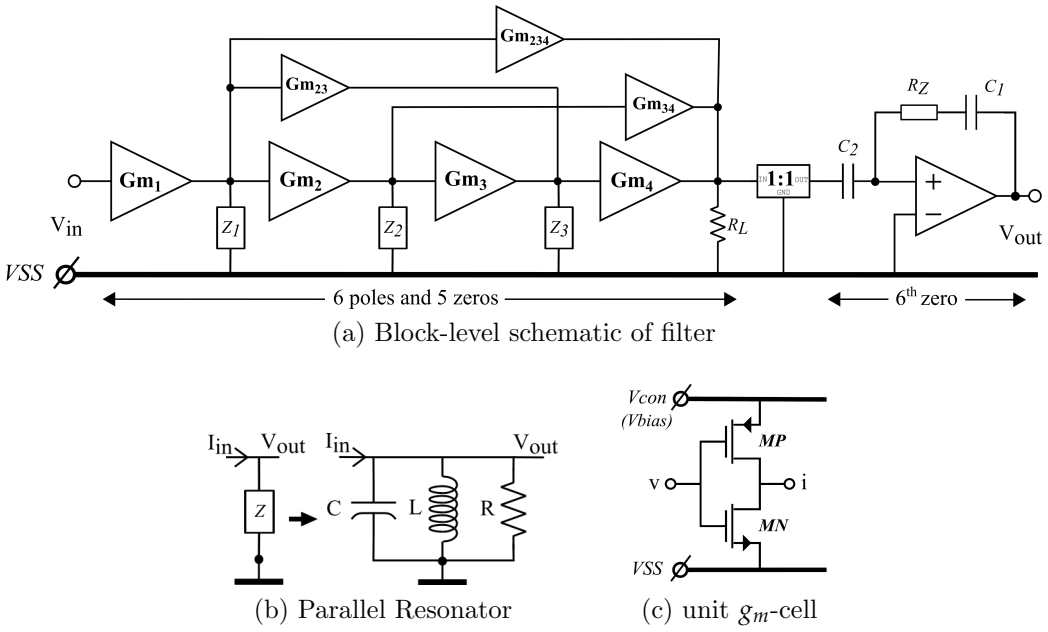


Figure 2.5: Switchable transconductor for programmability

2.2.2 Architecture Overview



(a) Block-level schematic of filter

(b) Parallel Resonator (c) unit g_m-cell

Figure 2.6: Filter Architecture for MRI Receiver

Filter architecture implements passive LC tanks tuned to the desired pole frequencies and corresponding active elements contributing gain in the passband, as shown in Fig. 2.6. It is a sixth order biquad filter with six poles and six zeros. Poles and zeros can be noticed in the filter as follows. Resonators, Z_{1-3} realize three pairs of complex-conjugate poles, making six poles in total. Feed-forward paths realize the two pairs of complex-conjugate zeros. Rest of the two zeros are real zeros, one is located at the origin as there exists a direct path from

input to output through Gm_{1-4} and second, the sixth zero has been implemented after buffer with an integrator. Here, Z denotes the parallel RLC resonator block while Gm denotes the transconductor block, i.e. transconductor cells connected in parallel.

Since, we are only concerned with improving the performance of filter by redesigning the transconductor, for that purpose only the filter stage from V_{in} until R_L is of our interest. The integrator doesn't play any role in the transconductor analysis, so it can be excluded. Fig. 2.6a shows the portion of the filter with six poles and five zeros, excluding the integrator. Fig. 2.7 shows its corresponding frequency response. Since, sixth zero (151 MHz) is well separated from the passband (125 MHz-130 MHz) of the filter, shape of the magnitude response in passband remains same, only the gain is reduced from 90 dB to 60 dB. While, the phase response shows an additional shift of -90° at 151 MHz as compared to the full filter circuit due to the exclusion of zero (at 151 MHz). For further references and reading, only the part from V_{in} until load resistance R_L is denoted as the filter. The total phase shift across the filter is 180° with the peak gain of 60 dB at 127.8 MHz.

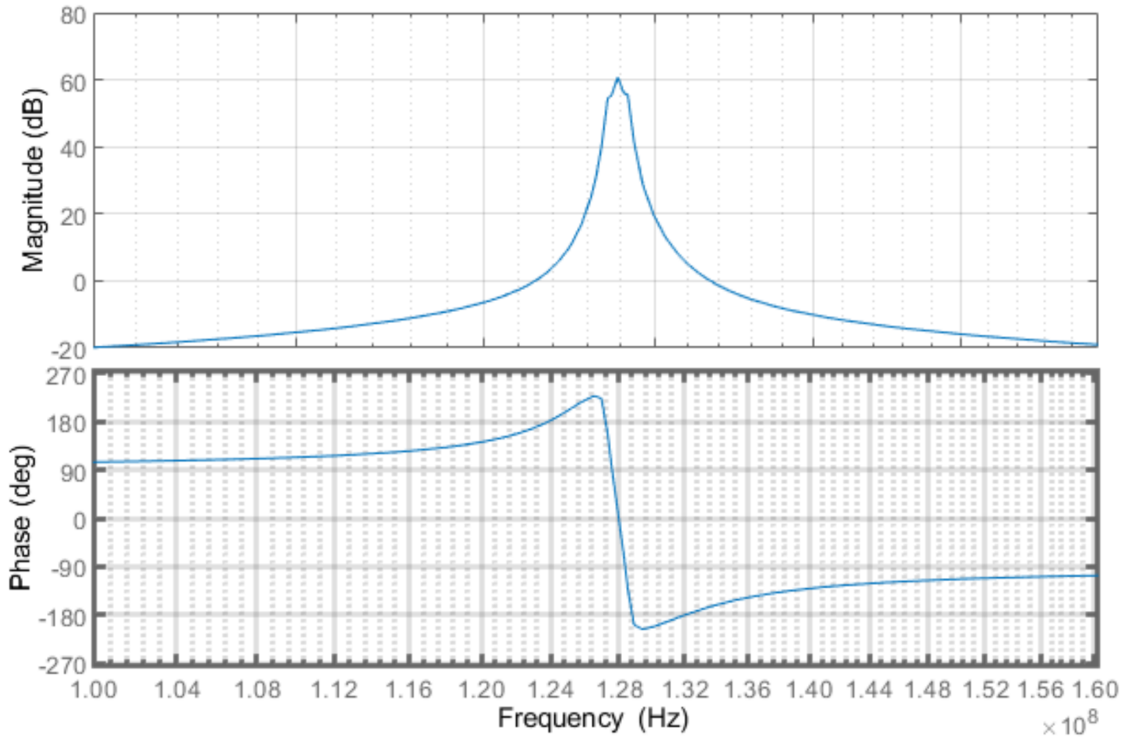


Figure 2.7: Ideal frequency response of the filter (excl. sixth zero)

Pole (MHz)	Resonator	Capacitance (pF)	Resistance (kΩ)	Inductor (nH)
-0.160 ± j 127.800	Z_1	31.02	16	50
-0.159 ± j 127.200	Z_2	31.31	16	50
-0.160 ± j 128.400	Z_3	30.73	16	50

Table 2.2: Component values (RLC) of three resonators corresponding to their poles

Once the architecture is decided, component selection can be done as follows. For a resonance frequency of the order of hundreds of MHz, the capacitor and inductor lies in the order of tens of pF and nH respectively. Since they are large to accommodate for monolithic implementation, they are placed off-chip. An inductor of 50 nH is chosen suited to the pole frequencies. Once the inductor is decided, the capacitor and resistance can be calculated for the respective poles frequencies with Q of 400 using the Eq. (2.1). The resistance comes out to be 16 kΩ while the capacitance is around 31 pF. The values are given in Table 2.2. Thus we know resonator components from desired pole frequencies, now we need to determine the transconductance of Gm block. This can be calculated by equating the transfer function derived from pole-zero information to that of the nodal analysis of filter architecture. The transconductances of the Gm blocks are decided by the passband gain of 60 dB, i.e. 1000x. With nodal analysis, transfer function of the filter architecture can be written in terms of transconductance Gm_{1-234} and resonator impedance $Z_{1-4}(s)$,

$$\begin{aligned}\frac{V_{out}}{V_{in}}(s) = R_L\{&(Gm_1Z_1(s)Gm_2Z_2(s)Gm_3Z_3(s)Gm_4 + Gm_1Z_1(s)Gm_4Z_3(s)Gm_{23} \\ &+ Gm_1Z_1(s)Gm_2Z_2(s)Gm_{34} + Gm_1Z_1(s)Gm_{234}\}\end{aligned} \tag{2.9}$$

$$Z(s) = \frac{1}{C}\left(\frac{s}{s^2 + \frac{s}{RC} + \frac{1}{LC}}\right) \tag{2.10}$$

Gm block	mA/V (mS)	Gm block	mA/V (mS)
Gm_1	2.5	Gm_{23}	-1.7
Gm_2	1.25	Gm_{34}	-0.02
Gm_3	1.25	Gm_{234}	0.34
Gm_4	0.625		

Table 2.3: Transconductance per Gm block in ideal filter

Table 2.3 shows the transconductances of the respective Gm blocks calculated after comparison of the two equivalent transfer functions. Note that the values in table only denote the result of mathematical calculation, which indicates there is a need of inversion

in transconductance Gm_{23} and Gm_{34}. Every Gm block is composed of a group of discrete transconductor cells connected in parallel, where unit transconductor cell is shown in Fig. 2.6c. If unit g_m-cell transconductance is g_m and the number of g_m-cells in a block is $N(Gm)$, then transconductance of that block, Gm equals to $N(Gm) * g_m$. The g_m of the unit transconductor cell can be chosen depending on the desired programming resolution. Lower the value, higher is the resolution. It has been found that the unit transconductance if aligns with the multiple of inverse of load resistance that is 62.5 μS (1/R), a good linearity of the filter is achieved. In the previous circuit, the unit transconductance (g_m) of 31.25 μS is realized. Thus, the number of transconductor cells per Gm block can be calculated by dividing the transconductance of the block, given in Table 2.3, by the unit cell g_m, 31.25 μS. Table 2.4 shows the number of unit transconductors in each block Gm_{1-234} denoted as $N(Gm_{1-234})$. For further understanding on calculating the scale factors of Gm block the reader is referred to Appendix A.

Gm block	No. of g_m-cell	Gm block	No. of g_m-cell
$N(Gm_1)$	80	$N(Gm_{23})$	54
$N(Gm_2)$	40	$N(Gm_{34})$	1
$N(Gm_3)$	40	$N(Gm_{234})$	11
$N(Gm_4)$	20		

Table 2.4: Number of transconductor cells per Gm block in ideal filter

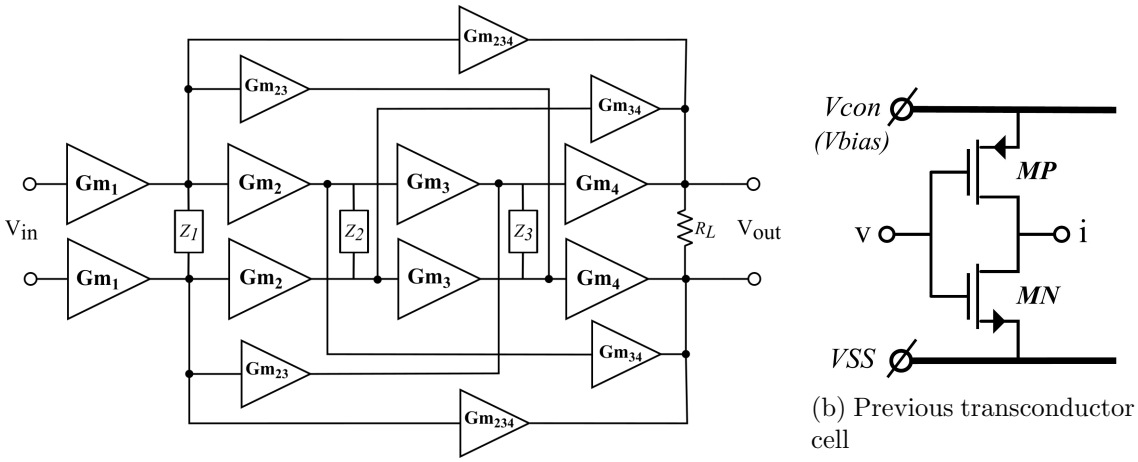
2.2.3 Previous Circuit

Previous circuit primarily, refers to the previous transconductor cell and the filter constructed after plugging those g_m-cells in the architecture mentioned above. It is the one which is employed at Philips, whose performance improvement is the goal of the thesis as mentioned earlier.

A. Previous Filter

As we noticed in Table 2.3, mathematically there is a requirement of negative transconductance for Gm_{23} and Gm_{34}, which means a polarity inversion in practice. It is because each of them provide an auxiliary feed forward path over two Gm blocks which reverses their polarity. Hence, a differential topology is adopted so as to make use of the opposite phase available on either side of the resonator.

Fig. 2.8 shows the filter circuit in differential form. Here Gm_{23} and Gm_{34} have their output and input cross connected respectively to other half of the schematic for the purpose mentioned above. To realize same transfer function with differential topology it can be understood that for each half circuit, resonator impedance will go half while current will go



(a) Fully-Differential Filter

(b) Previous transconductor cell

Figure 2.8: Fully-differential filter schematic using previous transconductor cell

Gm block	No. of g_m-cell	Gm block	No. of g_m-cell
$N(Gm_1)$	160	$N(Gm_{23})$	109
$N(Gm_2)$	80	$N(Gm_{34})$	1
$N(Gm_3)$	80	$N(Gm_{234})$	22
$N(Gm_4)$	40		

Table 2.5: Number of transconductor cells per Gm block in previous circuit

double. In simple words, for half circuit R$\rightarrow \frac{R}{2}$, L $\rightarrow \frac{L}{2}$, C $\rightarrow$ 2C, while the scale factor for transconductors goes 2x on each side of the differential filter configuration. The total resonator impedance of the full circuit remains same, hence component values of R, L and C in the fully-differential circuit are same as that of the single-ended, previously shown in Table 2.2. Whereas, transconductor cells per Gm block as well as the number of Gm blocks become double in fully-differential filter. This employs 4x the total number of unit transconductor cells as compared to the single ended filter, shown in Table 2.5. The circuit in Fig. 2.8 has been employed in the Philips MRI machine. This is our reference for benchmarking. The transconductor cell used here is referred to as the previous transconductor.

B. Previous Transconductor

The previous transconductor is a single-ended CMOS transconductor as shown in Fig. 2.8b. It provides high input-output swing with its complementary MOS input-output pair, suitable for high dynamic range (>90 dB) at low voltage supply (1.1 V) operation. It is biased with a fixed voltage bias $Vcon$, which is set at 860 mV providing a fixed transconductance

of 31.25 μS to the transconductor cell. Frequency response of the filter using the previous transconductor is shown in Fig. 2.9. With real implementation of the filter circuit, frequency response matches fairly well to the desired response (ideal). This confirms that this adopted architecture meets the requirements of the filter, given that circuit elements are stable and not subject to variations.

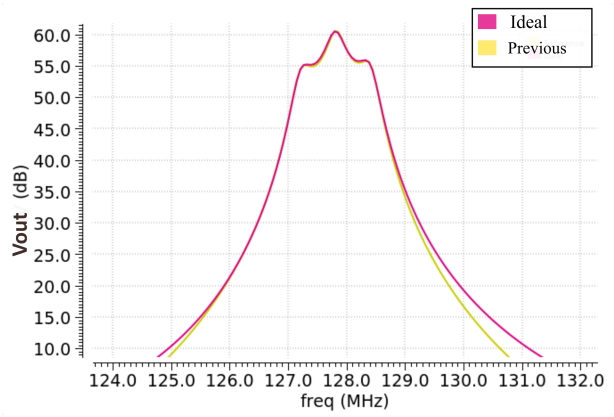


Figure 2.9: Previous transconductor implemented filter response - simulation results

Although, Table 2.2 depicts the component values of resonators in ideal case, in practical the transconductor cell's output capacitance and resistance will act as parasitic to the filter, which shall be incorporated to keep the frequency response intact. As mentioned before, for three resonators, the inductor is fixed at 50 nH due to the standard off-chip component, resistance is monolithic integrated component while capacitance has been divided into two parts, one being integrated capacitance bank and other, an off-chip standard capacitance. This implies that during the IC implementation, it is possible to incorporate the shift in filter poles arising due to the parasitics of the g_m-cells, with the help of resonator capacitance and resistance as required. It is further detailed with respect to the proposed transconductor in *Parasitics in Filter* (Section 3.2.2). Resonator capacitance and resistance after including the parasitics from the transconductors is given in Table 2.6. However, it shall be noted that the net resistance and capacitance at resonator remains same as that of the ideal which is the requirement of the system, the values "with Gm" only indicates the residual component values required to achieve the ideal value after parasitics are considered. The table shows that there is a requirement of negative resistance in resonators. This can be implemented using the transconductor itself. Principally, a transconductor is a voltage-to-current converter and if the polarity of voltage across a device is in reverse with the polarity of the flow of current through it, it can be treated as a negative resistance. This is also detailed with respect to the proposed transconductor in *Parasitics in Filter* (Section 3.2.2).

Pole (MHz)	Capacitance (pF)		Resistance (kΩ)		Q-factor
	Ideal	with Gm	Ideal	with Gm	(with Gm)
-0.160 ± j 127.8	31.02	30.97	16	-20	398
-0.159 ± j 127.2	31.31	31.27	16	144	387
-0.160 ± j 128.4	30.73	30.7	16	-87	410

Table 2.6: Resonator components for previous transconductor implemented filter. L=50nH

2.2.4 PVT Tolerance

There are four circuit elements in the filter - inductor, capacitor, resistor and transconductor. The inductor and capacitor being off-chip can be chosen to have high precision, while integrated resistor is a negative resistance implemented with transconductor and lastly transconductor itself. This implies, predominantly it is transconductor which is responsible for the performance of the filter IC. For filter to accurately select the channel with the desired passband gain under the process, voltage and temperature variations, the g_m of the transconductor shall be constant.

A. Challenges

Transconductance is subjected to variation due to its dependency on temperature and process variable parameters such as threshold voltage V_{th}, mobility μ. Previous transconductor also suffers from g_m deviation due to several factors. First, it uses a fixed-voltage bias ($Vcon$). Although, $Vcon$ is a stable biasing voltage, but there are more than 200 x 4 transconductor cells on the chip which are biased with same voltage supply, $Vcon$. Any coupling with other signals on chip or voltage drop across $Vcon$ path can disturb the biasing point of transconductor cell. Second, it lacks any self-stabilizing capability being a single-ended structure. It has no power supply or common-mode rejection ability, thereby highly sensitive to any variation in its operating conditions say temperature or voltage. This makes the stability of the transconductor be solely dependent on its bias, which in itself is vulnerable to variations as mentioned formerly.

In post-layout simulations, it is observed that previous transconductor cell suffers from more than 15% g_m deviation under the impact of PVT variations. This leads to up to 10% degradation in filter passband gain, which is highly undesirable for it degrades the noise performance and dynamic range, having placed at the forefront of MRI receiver. Since, transconductor cells are present in large quantity, filter frequency response depends heavily on its performance and it is very sensitive to the change in its unit cell.

To address the issue of transconductor having no common-mode rejection which degrades its performance due to coupling of control signal, fully-differential topology has been adopted in literature. Further to add stability, cascoding technique can be an option which increases the effective impedance, thus reduce the impact of variations. However, while designing for

high dynamic range at low voltage supply, which is a necessity in the application of MRI and has to be atleast 90 dB, transistor stacking should be avoided. This is because cascoding topology can make it difficult for the devices to avail a sufficient overdrive voltage to stay in saturation region, thus lowering the possible signal swing.

On the other hand, one can look into improving the biasing technique to add stability to the g_m of transconductor. Previous transconductor uses constant-voltage biasing, but it is highly susceptible to variation due to coupling and also it is difficult to maintain exact biasing point with fixed-voltage bias due to the voltage drop along the bias path, which is why it is not a recommended technique. Among traditional biasing methods - constant-current biasing has been used very often because of the ease of generating a fixed current bias and distributing it by creating multiple copies of the current-mirror. This is convenient from layout perspective as well, being resilient to parasitic coupling. With constant-current bias, it was observed that the variation in transconductance across process corner is 9% while across temperature is upto 30% at typical process corner. We know, for a constant-current biasing, the output current is expressed by the square-law

$$I_{ds} = \mu Cox \frac{W}{L}(V_{gs} - V_{th})^2 \tag{2.11}$$

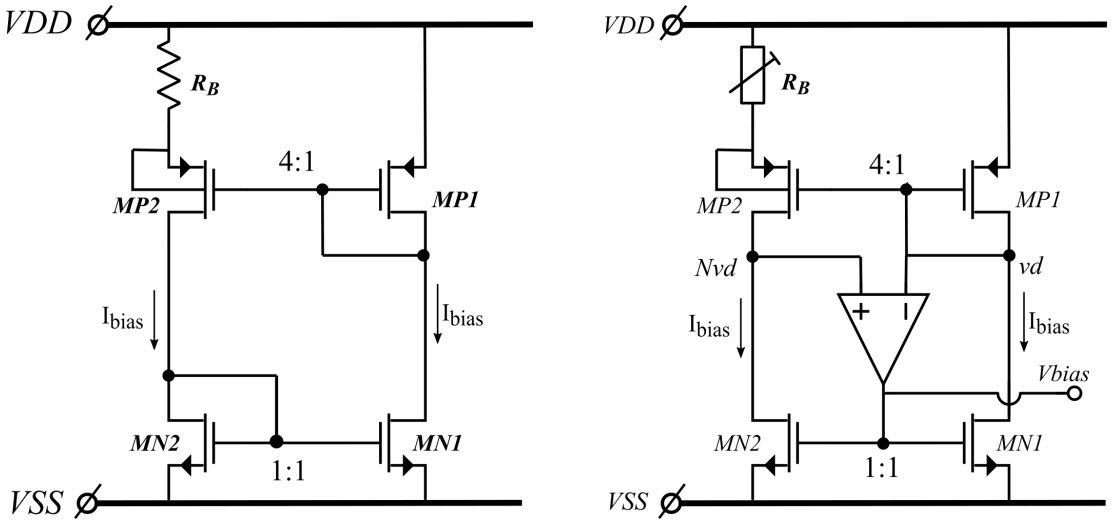
This shows that the current has direct dependency on temperature dependent parameters that is mobility and square of threshold voltage, which is steered directly to the transconductance as well. Hence, such a huge variation is seen because the current copy is imbalanced due to the mobility degradation with temperature and also temperature dependency of threshold voltage. Thus, constant-current biasing is not suitable for our requirements. We know that g_m is defined as change in output current per unit change in input voltage, so if we need a constant g_m with temperature, there needs to be a biasing scheme which cancels out the effect of temperature variation on g_m with that on current.

B. Potential Solution - Constant-g_m Bias

The methodology of constant-g_m biasing has been adopted in literature to avail stable transconductance circuit with PVT variations.

Constant-g_m biasing is based on the principle of PTAT current generator used in BJT. It uses two current-mirror pairs, one each of nMOS and pMOS connected back to back as shown in Fig. 2.10a. The transistors are sized such that one of the pair is at equal size while the other is skewed in the ratio of 4:1. This ensures a constant current in both the branches and the difference in the overdrive voltages of the skewed pair appears across the resistor, where resistor shall be ideally independent of the temperature variation. This way the transconductance (g_m) becomes proportional to the inverse of resistance and independent of process and temperature variations. It can be said that constant-g_m biasing ensures the transconductance tracks the precise resistance.

Here, a current has been generated which adjusts itself with temperature variations such that the transconductance remains constant. This is further illustrated with the help of the



(a) Basic concept of constant-g_m biasing with Temperature

(b) Using negative feedback loop for stability against supply variations

Figure 2.10: Concept of constant-g_m biasing

Eq. (2.12)-(2.17). where, V_{thP} is threshold voltage of pMOS, V_{gs} is the gate-source voltage, I_{ds} is the drain-source current, V_{gt} is the overdrive voltage ($V_{gs} - V_{th}$) and K is the process variable ($0.5\mu C_{ox}$).

$$\begin{aligned} V_{gsMN1} &= V_{gsMN2} \\ \text{hence, } I_{dsMN1} &= I_{dsMN2} = I_{bias} \end{aligned} \tag{2.12}$$

$$\begin{aligned} I_{dsMP1} &= I_{dsMP2} = I_{bias} \\ \text{where, } I_{dsMP1} &= K\frac{W}{L}(V_{gsMP1} - V_{thP})^2 \\ I_{dsMP2} &= K\frac{4W}{L}(V_{gsMP2} - V_{thP})^2 \end{aligned} \tag{2.13}$$

from (2.13),

$$(V_{gsMP1} - V_{thP}) = 2(V_{gsMP2} - V_{thP}) \tag{2.14}$$

because of same current in each branch, I_{bias},

$$V_{gsMP1} - V_{gsMP2} = I_{bias}R_B \tag{2.15}$$

from (2.14) and (2.15),

$$\frac{2I_{bias}}{V_{gsMP1} - V_{thP}} = \frac{1}{R_B} \tag{2.16}$$

we know $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$, $g_m = \frac{2Ids}{V_{gs}-V_{th}}$

$$g_{mMP1} = \frac{1}{R_B} \tag{2.17}$$

Using the pMOS pair over nMOS, to skew in the ratio of 4:1 prevents the body effect due to the feasibility of connecting the bulk with the source of pMOS in the CMOS technology. Under body effect, the threshold voltage of MOS varies with change in source-bulk voltage, V_{SB}. Whereas with the adopted technique, while generating difference in gate-source voltage V_{gs} of pMOS pair available across resistor, voltage V_{SB} is maintained at zero for both $MP1$ and $MP2$ and so matching of all four transistors is retained. The circuit in Fig. 2.10a produces current I_{bias} such that the transconductance tracks the resistance R_B with temperature variation.

However, any variation in supply voltage from V_{DD} at the source of $MP1$ will translate to its drain, subsequently creating a difference in the drain voltage of $MN1$ and $MN2$ in the current-mirror pair. This disrupts the current-mirroring action, i.e. the current in each of the two arms will no longer stay equal. To add stability against supply variation, one can choose to go for cascoding the current mirror pair or add negative-feedback loop as shown in Fig. 2.10b. Cascoding is not suitable for low voltage operations, limiting the signal swing. The operational amplifier (opamp) is added such that the negative-feedback loop, comprised of $MN2$ and opamp, is stronger than positive-feedback loop, comprised of $MN1$ and opamp. This is so, because the output impedance looking into the negative-feedback loop dominates, whereas the output impedance in positive-feedback loop is merely a diode connected transistor impedance $1/g_{mMP1}$[32]. The opamp need not to be a very complex one here, as its purpose is only to keep the drain-source voltage, V_{ds} across the nMOS current-mirror pair constant. This ensures the current(I_{bias}) in each of the arms of the current mirror pair to match by virtue of its sufficient loop gain. In principle, under a negative-feedback an opamp tries to keep both of its inputs at same potential called as virtual ground. Since it is a dc-bias there is not a very hard limitation on its speed which governs the settling time.

In practicality, the resistor has some dependencies on temperature. A precise resistor can be implemented off-chip ([20],[15]) to ensure it retains its value throughout the PVT variations, but this comes with the penalty of parasitic capacitance, generating a parasitic pole-zero pair at low frequencies which interferes with the stability of the system and so needs a large compensation off-chip capacitance [17]. Although, with the advancement in process technology very low temperature coefficient (TC) is achievable for on-chip resistor like poly resistance with TC as low as 47ppm/°C. However, using a poly resistor is a trade-off, due to the additional dependency of resistance with process corner variation in lieu of minimizing temperature variability. One possible solution is to add programmability to the resistor, which can be tuned externally for process variations. This has been adopted in the previous circuit as well for one-time calibration of filter IC to correct bias voltage by trimming the resistance with an external input of digital binary code.

One of the challenge is to achieve the stable g_m along with the high dynamic range at low voltage operation. For which biasing the devices in strong inversion saturation region may require higher overdrive voltages, thus limiting the output swing. In the next chapter, we present a design that encounters all the challenges and provides constant-g_m to the filter.

Chapter 3

Circuit Implementation

In previous chapter, the system requirements of the filter and its architecture were discussed. Also, the challenges associated with previous transconductor implemented filter were analyzed and the biasing methodology suitable for the purpose of constant-g_m transconductor was introduced.

In this chapter, transistor-level implementation of the proposed transconductor and its biasing circuit has been presented including the analysis of design choices with respect to the requirements, discussed in *Introduction* chapter. Further, the implementation of the filter using the proposed transconductor has been shown as well as the tuning of the resonators required after including transconductor parasitics is discussed. Also, switch configuration of the transconductor is provided to support programmability of the filter. The chapter ends with the layout of the unit transconductor and its bias circuit in the last section.

3.1 Transconductor cell

The proposed transconductance circuit uses the constant-g_m biasing methodology and an inverter based self-biased fully-differential transconductor. The section starts with the biasing circuit followed by transconductor circuit and lastly shows the complete constant-transconductance circuit, representing how the transconductor is connected with its bias.

3.1.1 Constant-g_m Biasing

As discussed in *System Design* (Section 2.2.4), here we are employing constant-g_m biasing circuit, which comprises of two current-mirror pairs one each of nMOS and pMOS connected back-to-back as shown in Fig. 3.1. To avail an n-bias required for the transconductor, the geometry of pMOS pair ($MP2 : MP1$) is skewed, generating the difference in gate-source voltages while nMOS pair is kept at equal size, mirroring the current in two arms of the bias circuit. The type of bias required for g_m-cell will be evident in subsequent section. Choosing such a configuration also prevents the mismatch arising due to the variation in

threshold voltages of the skewed pair under the impact of body effect due to the provision of connecting source-bulk of pMOS in n-well process.

For the requirement of high dynamic range of MRI front-end receiver, i.e. large output swing at low-voltage operation, biasing in weak inversion saturation region has been adopted which reduces the overdrive voltage. Unlike, conventional constant-g_m bias, here transistors are biased in the subthreshold region to generate current, I_{bias} which follows the exponential relation with gate-source voltage as the dominant current is diffusion current instead of drift current. The drain-source current in subthreshold region can be expressed as

$$I_{DS} = I_{DS0}\frac{W}{L}exp(\frac{V_{gs} - V_{th}}{nV_T}) \tag{3.1}$$

where, I_{DS0} is the subthreshold saturation current given as $(n-1)\mu C_{ox}V_T^2$, hereafter denoted as I_0, V_T is the thermal voltage kT/q, V_{th} is threshold voltage and n is the subthreshold slope factor [32]. Hereafter, overdrive voltage $(V_{gs} - V_{th})$ is denoted as V_{gt}.

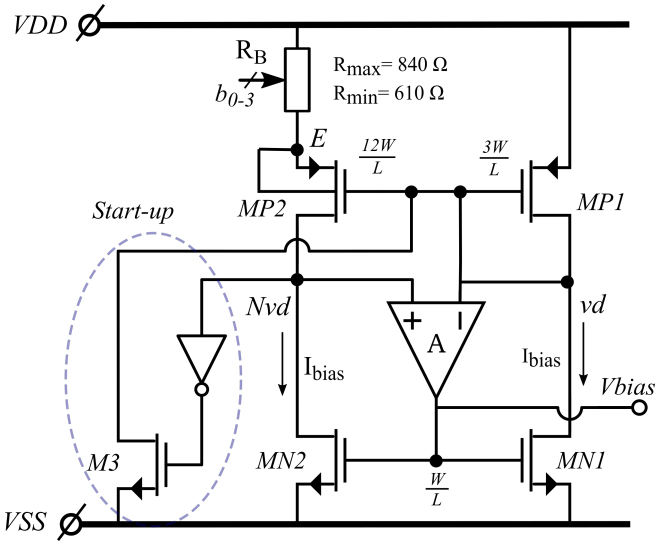


Figure 3.1: Schematic of the proposed biasing circuit

The constant-g_m bias generates the difference of the skewed current-mirror pair's gate-source voltage, thereby difference of overdrive voltage (ΔV_{gt}), across the resistance R_B. This is valid for subthreshold operation of the devices as well. Fig. 3.1 shows the proposed biasing circuit. The transconductance (g_{mbias}) of the biasing circuit can be calculated as follows.

$$\begin{aligned} I_{MP1} &= I_0\frac{W}{L}exp\left(\frac{V_{gt1}}{nV_T}\right) \\ I_{MP2} &= I_0\frac{4W}{L}exp\left(\frac{V_{gt2}}{nV_T}\right) \end{aligned} \tag{3.2}$$

From Eq. (3.2)

$$V_{gt1} = nV_T ln\left(\frac{I_{MP1}}{I_0 \frac{3W}{L}}\right)$$
$$V_{gt2} = nV_T ln\left(\frac{I_{MP2}}{I_0 \frac{12W}{L}}\right) \tag{3.3}$$

Reiterating from Section 2.2.4,

$$I_{MP1} = I_{MP2} = I_{bias}$$
$$I_{bias} = \frac{V_{gt1} - V_{gt2}}{R_B} \tag{3.4}$$

From Eq. (3.3) and (3.4),

$$I_{bias} = nV_T \frac{ln(4)}{R_B} \tag{3.5}$$

Given that ($V_{DS} > 5V_T$), the transistor is under the weak inversion saturation region. The transconductance of the transistor biased with I_{DS} in subthreshold region is given by [32]

$$g_m = \frac{I_{DS}}{nV_T} \tag{3.6}$$

Substituting Eq. (3.5) in (3.6)

$$g_{mbias} = \frac{ln(4)}{R_B} \tag{3.7}$$

Hence, this circuit generates a current proportional to temperature such that the transconductance of all the transistors biased with it, is independent of temperature. Infact, transconductance is now given by only a fixed proportion of resistance, R_B, depending on the geometric ratios. In biasing circuit, the nMOS and pMOS are sized such that $g_{mMP1} = g_{mMN1} = g_{mbias}$, for better matching and linearity [24].

The proposed biasing circuit includes four elements namely, two current-mirror pairs, negative feedback loop, programmable resistance bank and start-up circuit. Each arm of the current-mirror generates a biasing current of 4.5 μA (I_{bias}), which is assisted by an opamp to reject the supply variations, a start-up circuit to put the self-biased circuit into the desired stable state as soon as the supply is switched ON and a digitally programmable resistance bank to compensate for the process corner variations. The details of these four circuit elements are as follows.

A. Start-Up

This biasing circuit is a self-biased circuit, hence there exists another metastable state due to the presence of high impedance nodes, where both the current-mirror pairs are OFF when the circuit is switched ON, as a result no current flows in the circuit. To protect this undesirable situation, a start-up circuit is used as displayed in Fig. 3.1. The worst-case is

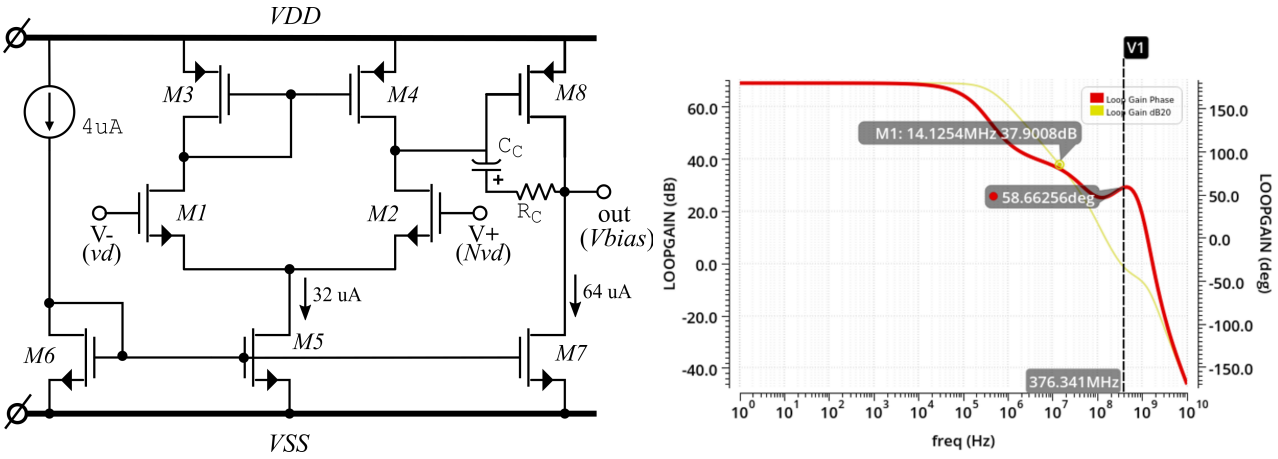
when node Nvd is at V_{SS} while node vd is at V_{DD}. The inverter in the start-up circuit senses Nvd and turns $M3$ ON, thus pulling down the node vd. Further, with self-biasing action of the two current-mirror pairs, bias circuit attains the desired stable state. The start-up circuit uses weak devices, i.e. the W/L ratio is very small as compared to the current-mirror pairs, hence it does not interfere with the main circuit. In normal operation, node Nvd rises well above V_{SS}, turning the start-up circuit OFF.

B. Opamp

The negative feedback loop is employed using an operational amplifier (opamp), A. The opamp has both negative as well as positive feedback loop. Placing the opamp in the configuration as shown in Fig. 3.1 ensures the negative feedback is dominating due to the higher output impedance of the $MP2$ with respect to $MP1$ which is merely a diode connected transistor. Ideally, the opamp is employed to operate at DC, since it is only a biasing circuit. Which means the only necessity is to have a moderate loop gain (around 40-50 dB) to reduce the error with a nominal settling speed (say 0.1ms) good enough for the system to stabilize, no tough restrictions. This implies it is a very simple opamp only meant to equate the currents in the two arms of the biasing circuit by the virtue of its error-correcting nature to reduce the difference in its virtual ground nodes when placed in a negative feedback loop and the quality of error-correction is defined by its loop gain.

So, it could have been implemented with a single stage opamp, as also done in [18]. However, the power supply, V_{DD} of 1.1 V is not an external supply, but generated on-chip using the switched capacitor power converter. This introduces high frequency transients to the supply, so the supply is not clean. Hence, a substantial loop gain at 15 MHz, which is the switching frequency of the power converter, is sought after rather than DC gain. To achieve this, a two stage miller compensated opamp has been chosen. It provides a sufficient loop gain along with the high bandwidth. This helps in achieving higher power supply rejection.

Fig. 3.2a shows the implemented opamp. The DC loop gain of 70 dB is implemented which provides a loop gain of 40 dB at 15 MHz to increase the PSRR (>20 dB). The high loop gain is also a result of the load impedance seen by the opamp at its output ($Vbias$) which comprises of the gate impedance of nMOS current-mirror and output impedance of $MP2$. A phase margin of $60°$ is ensured to keep the stability of the loop as shown in Fig 3.2b. The opamp uses an on-chip available current source of 4 μA. The total current consumption of the opamp is 90 μA. A low valued compensation capacitor, C_C of 350 fF is used to retain the wider bandwidth, implemented with the metal-oxide-metal (MOM) capacitor. A resistor, R_C of 4 kΩ is used to compensate for the right hand pole (RHP) induced by C_C, implemented with the poly resistor having very low temperature coefficient. The transistor device sizes are given in Table. 3.1. $M8$ is sized such that the W/L ratio is large for high gain but its size is small so as to reduce its gate-oxide capacitance, thereby requiring a lower compensation capacitance, C_C which in turn allows to achieve wider bandwidth.



(a) Two-stage Miller compensated opamp

(b) Stability analysis of loop

Figure 3.2: Operational Amplifier used for negative feedback loop in bias block

Device	W(μm), m-factor	Device	W(μm), m-factor
M1-M2	4, 8	M6	2, 2
M3-M4	8, 8	M5	2, 16
M8	8/0.08 (W/L), 8	M7	4, 16

Table 3.1: Opamp in bias circuit. L= 0.5μm, except for M8

C. Resistance Bank

Resistance, R_B chosen is the n+ polysilicon resistance in isolated n-well with temperature coefficient of 47ppm/°C. This renders transconductance nearly independent of temperature. Although being a poly resistance, there is an additional dependency with process variations. To compensate for the process corner variation, a digitally programmable binary weighted resistance bank has been employed, shown in Fig. 3.3.

At slow corner the effective resistance per unit area of the poly increases while for the fast corners it decreases. Hence, a fixed length of poly resistance is used as a base resistance which aligns with worst case corner ss, i.e. 610 Ω . Further, the resistance is increased by sensing a digital input of four bits i.e, b_{0-3}. As the bit is high, the switch is turned off and its corresponding parallel resistance is added on top of the fixed resistance in series. Similarly, when the bit is low, switch is turned on and it short-circuits the resistance of the corresponding arm. The resistances are laid out in binary fashion with step size of 15Ω and range of 0 Ω to 225 Ω. The minimum possible unit resistance is limited by the sheet resistance which is 175 Ω/□. Hence, the poly resistances have been sized accordingly as per the convenience of geometrical size vs equivalent resistance as shown in Table 3.2. Say

if the unit resistance is equivalent to about 240 Ω, so 8 parallel units are placed to employ 30 Ω. Each of the resistance in Fig. 3.3 shows two parallel units from R_{2-15} except R_1. The switch resistance is small ($R_{SW} \ll R_{1-15}$) such that it does not interfere with the equivalent R_B.

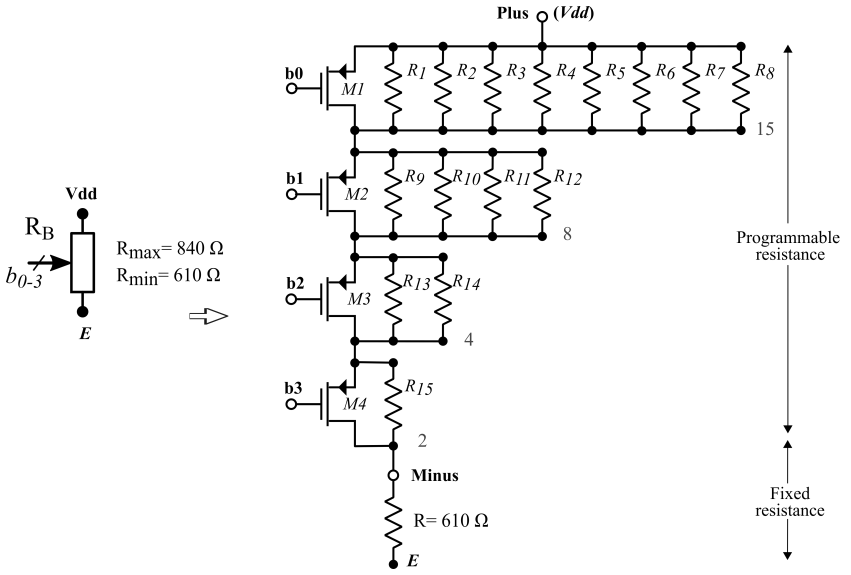


Figure 3.3: Binary weighted 4-bit resistance bank.

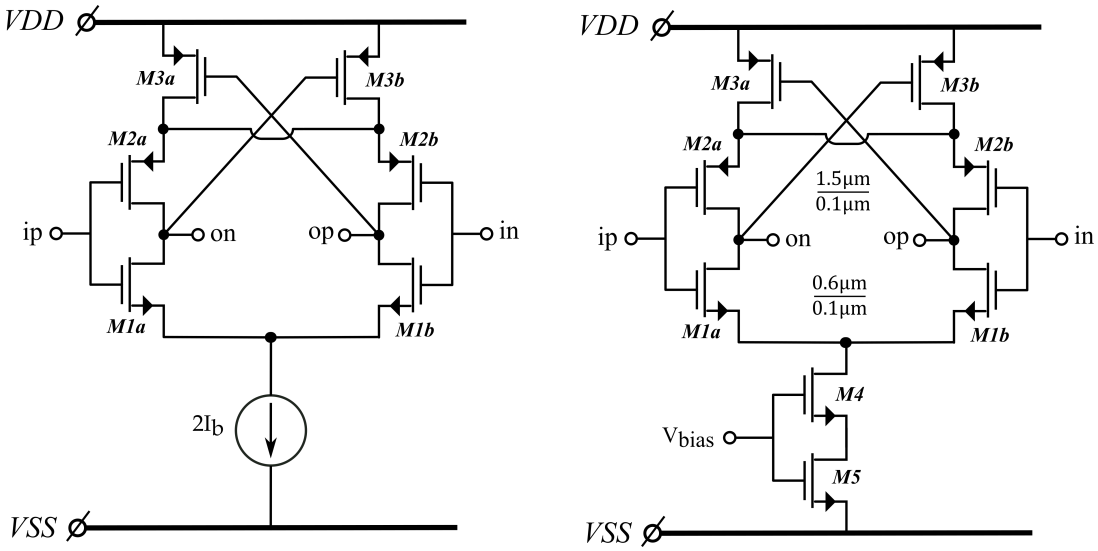
Binary 4 Bits	Range 0-225Ω	Step size =15 Ω	
bit	no. of res	equiv. res (Ω)	unit res (Ω(WXL)μ)
b0	15	15	227(1.2x1.2)
b1	8	30	241(1x1.04)
b2	4	60	241(1x1.04)
b3	2	120	241(1x1.04)

Table 3.2: Programmable 4-bit binary weighted resistance bank

This on-chip implementation of the resistance bank provides one-time calibration to the filter IC by trimming the resistance based on an external digital code, to make it precisely hold its desired value combating the process variations.

3.1.2 Self-biased Transconductor

An inverter based self-biased fully-differential transconductor has been proposed considering the requirements presented in *Introduction* (Section 1.2), which are further detailed in the theory of operation.



(a) Transconductor Architecture (b) Transconductor Schematic

Figure 3.4: Proposed Transconductor

A. Theory of Operation

For a combination of wide bandwidth, linearity and high dynamic range, the architecture shown in Fig. 3.4a has been proposed for the transconductor. It has four circuit elements namely − fully differential structure, complementary input-output pair, self-biased output common-mode control and cascode current-source. These can be noticed in the schematic, shown in Fig. 3.4b, as follows. $M1 - M2$ forms the fully-differential complementary input-output pair, parallel transistors $M3_{a-b}$ forms the self-biased common-mode control and $M4 - M5$ forms the self-cascode current source.

First, fully-differential structure increases linearity, thereby reduces distortion due to the cancellation of even order harmonics. In addition, it increases the circuit's ability to reject noise or interference from other signals, rendering a high noise performance. This is because fully-differential circuits are symmetric at its axis as a result, the effect of external sources is equally seen on both half-circuits, thus canceling out their net-impact. In other words, fully-differential circuit has a high common-mode rejection which adds to its stability.

Second, complementary input-output pair encounters the requirement of the filter to have high dynamic range at low voltage supply (V_{DD}). Given, that dynamic range is a critical

specification for MRI front-end receiver and could be challenging to achieve at the low voltage of $1.1V$ where threshold voltages are in the order of 0.4V. This is achievable with the help of inverter based circuit, also adopted previously in [20, 23] and biasing in weak inversion saturation region. For a typical inverter, the output swing is one overdrive off the supply rails at both ends. Here, the biasing transistors $M3$ and $M4$-$M5$ also take some headroom but that's small, of the order of 0.25 V in all, as $M3$ and $M5$ are biased in triode while $M4$ in deep weak inversion saturation. Apart from this, inverter based transconductor has higher g_m-efficiency and so it's very well suited for low power application, MRI receiver.

Third, self-biased common-mode control assists the strong requirement of constant-g_m of the transconductor, for it is a fully-differential topology [25] [26]. It acts as a common mode control of output. The self-biased pair senses the output and adjusts bias current in each of the half circuit, maintaining the total bias current constant. For example, if op goes high $M3_a$ becomes weak, sourcing less current. On the other hand, $M3_b$ becomes stronger sensing relatively lower potential at on, thus compensating the reduction by sourcing more current. Since, the two have common-source and common-drain they are acting in parallel, thus the net-current sourced from supply remains constant. Moreover, in the filter circuit common-mode level of the transconductor is taken care of by the self-biased transconductor connected in cross-coupled fashion to realize a negative resistance at the LC tank load. This will become evident in *Parasitics in filter* (Section 3.2.2) on negative resistance implementation of the proposed transconductor.

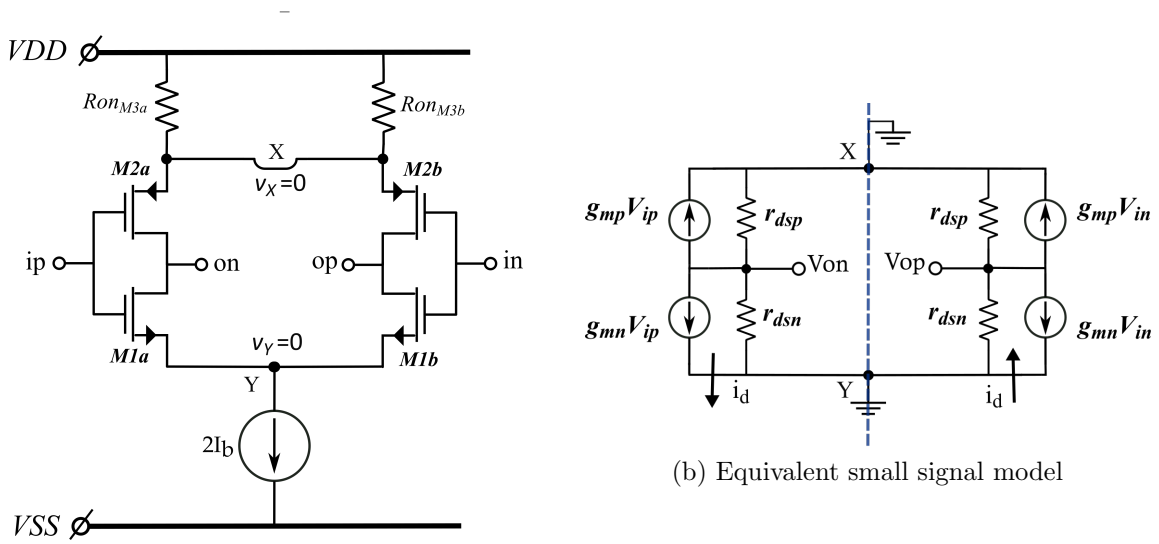
Fourth, for current-source of a regular transconductor, a simple matched current-mirror pair using a single transistor could have been an option. But as discussed before, there is a need of high tolerance to the supply variation, so a single-transistor doesn't serve the purpose. A single transistor current-mirror pair is not stable as it follows square-law model which doesn't suit the modern-day lower technology nodes due to second-order effects becoming predominant such as channel-length modulation. Instead, here a self-cascode current-source has been chosen as shown in Fig 3.4b. It consists of two transistor $M4$ and $M5$ sharing common gate. The lower transistor $M5$ operates in triode region while upper transistor is the main current-source acting in weak inversion saturation region. $M4$ increases the impedance looking into the current-source thereby increasing its stability with supply variation [32] [33]. With the help of $M3$ acting as common-mode feedback and $M4 - M5$ as current source, the inverter pair, $M1 - M2$ has been isolated from the power supply. Thus, they altogether improve the power supply rejection ability of the transconductor [34].

This transconductor is very suitable for high frequency operation as it lacks internal nodes, hence it doesn't induce any parasitic pole or zero. Moreover, it allows to merge its output capacitance and resistance (parasitic to filter) with that of the RLC resonator, leveraging an ease of interfacing. This could have been challenging with a multistage or cascoded transconductor for the programmability of the filter, where the parasitics would vary with the number of unit cells switched ON for a particular filter configuration. As a result of which, Q of the filter will vary with the configuration of the IC. This will become more evident in *Parasitics in Filter* and *Programmability* (Section 3.2.2 & 3.2.3).

The nMOS ($M1$) and pMOS ($M2$) transistors of the inverter are matched with each

other as well such that the K_p equals K_n, which renders matched g_m, i.e. g_{mp} equals g_{mn} reducing the sensitivity to process, temperature and mismatch variation significantly [23]. Additionally, matched nMOS and pMOS provides the inherent benefit of non-linearity cancellation between the two transistors in the inverter [20, 24]. K is the process variable denoting the term $\mu C_{ox} W/L$.

B. Small-signal Analysis



(a) Differential mode operation

(b) Equivalent small signal model

Figure 3.5: Small-signal model of proposed transconductor

Fig. 3.5a shows an equivalent model of the proposed transconductor to represent its differential mode operation. $M3_{a-b}$ acts as a p-bias, unlike the usual case it is not a current source, but operating in deep triode region with a very small on-resistance. The two transistors are connected in parallel, so the drain-source voltage drop across $M3_{a-b}$ is very small transferring almost entire V_{DD} to the input pair while acting as the self-biasing transistors. There is no signal current through $M3$, i.e. the signal voltage at the common source of $M2_{a-b}$, node X is zero. Additionally, this helps in providing large overdrive voltage to the input-output pair. On the other end, the self-cascode current source is acting as n-bias supplying the bias current $2I_b$. Again, the signal current is zero across $M4$ and $M5$, so the signal voltage at the common source of $M1_{a-b}$, node Y is also zero. Thus, equivalent small-signal model of the proposed transconductor reduces to the one in Fig. 3.5b.

The equivalent model of g_m-cell is symmetrical at its axis, looking at which, it can be said that the proposed transconductor is identical to a differential inverter. If $V_{ip} - V_{in}$ is the differential input voltage ΔV and signal current is i_d then transconductance of the g_m-cell, g_{meff} is given by the sum of the transconductances of pMOS and nMOS input transistors.

$$
\begin{aligned}
i_d &= g_{mp}\Delta V + g_{mn}\Delta V \\
g_{meff} &= \frac{i_d}{\Delta V} \\
g_{meff} &= g_{mp} + g_{mn}
\end{aligned}
\tag{3.8}
$$

3.1.3 Complete "constant-transconductance" circuit

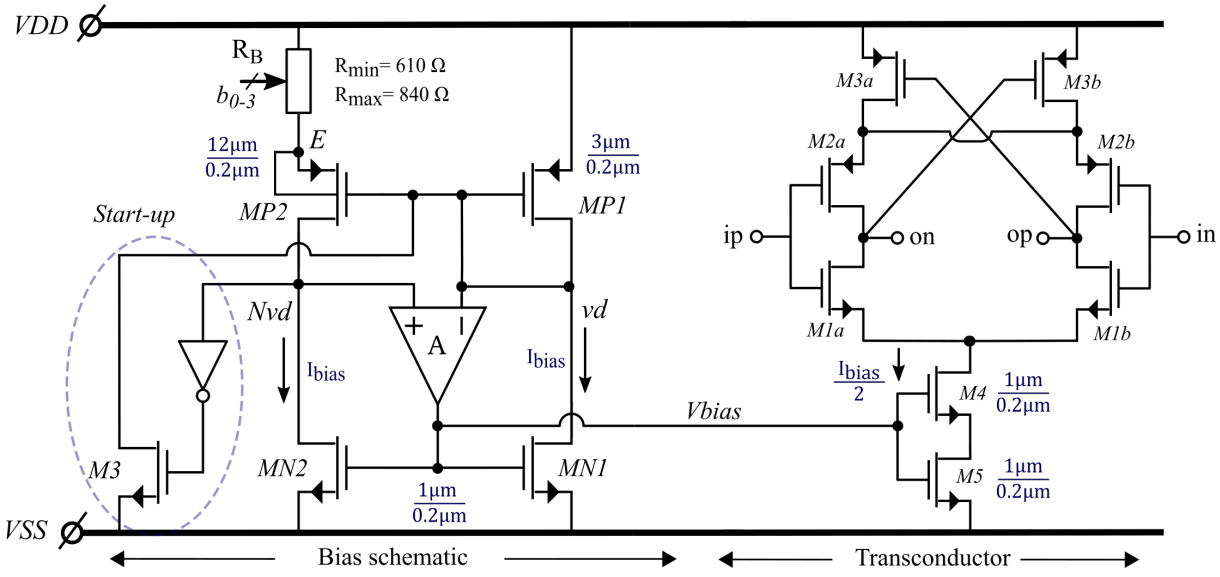


Figure 3.6: Complete "constant-transconductance" circuit

The biasing circuit provides a linear-bias current that cancels out the impact of mobility degradation with the rise in temperature, to keep the transconductance(g_m) constant. The current from the bias circuit is copied to the transconductor cell using the self-cascode current-mirror as shown in Fig. 3.6. The self-cascode current-source is matched with nMOS pair ($MN1 : MN2$) in the bias circuit making series-parallel current-mirror pair [35]. Moreover, as the voltage $Vbias$ is controlled under the negative-feedback loop and responsible for generating the bias current, I_{bias}, taking the same node to bias the transconductor as well acts as a replica-biasing, given that the device sizes are well matched.

As we have deduced before, the transconductance in biasing circuit, g_{mMP1} is equal to $ln(4)/R_B$ and given that the transconductor cell is biased with the same current (proportion of current) I_{bias}, then g_m of the transconductor cell is given by Eq. 3.10.

Reiterating Eq. (3.6) and (3.5)

$$\begin{aligned} g_m &= \frac{I_d}{nV_T} \\ I_{bias} &= nV_T \frac{ln(4)}{R_B} \end{aligned} \tag{3.9}$$

Given that, bias current in half-circuit of the transconductor is $I_{bias}/4$ and $g_{mp} = g_{mn}$, then total g_m of the transconductor ($g_{m\text{eff}}$) can be calculated as follows

$$\begin{aligned} g_{mn}, g_{mp} &= \frac{ln(4)}{4R_B} \\ g_{m\text{eff}} &= \frac{ln(4)}{2R_B} \end{aligned} \tag{3.10}$$

It can be said that g_m of all the transconductor circuits on chip is constant being a function of resistance, R_B and geometry only. The geometric ratios include that of the biasing transistors as well as the current-source in transconductor cell.

The impact of having matched nMOS and pMOS transistor in inverter which is two fold in terms of reducing the sensitivity to variation and cancelling non-linearity, can be illustrated as follows. With $K_p = K_n$, transconductance of the g_m-cell is independent of process and temperature variables.

$$g_{m\text{eff}} = \frac{ln(4)}{4R_B}\left(1 + \frac{K_n}{K_p}\right) \tag{3.11}$$

The output current in g_m-cell is the sum of nMOS and pMOS drain current which comes out to be linear with input voltage, V_i. Assuming, $V_{thn} = V_{thp}$. Using Taylor series expansion

$$\begin{aligned} &i_d = i_{dn} + i_{dp} \\ &i_d = I_{0n.p}\left\{exp\left(\frac{V_{gsn} - V_{th}}{n_n V_T}\right) - exp\left(\frac{V_{gsp} - V_{th}}{n_p V_T}\right)\right\} \\ &i_d = b_0 + b_1 V_i \\ &where, b_0 = \frac{-I_0 V_{DD}}{nV_T}\left(1 + \frac{V_{DD}}{nV_T} + \frac{2V_{th}}{nV_T}\right), b_1 = \frac{2I_0}{nV_T}\left(1 + \frac{V_{th} + V_{DD}}{nV_T}\right) \end{aligned} \tag{3.12}$$

To increase matching in the bias circuit, multiplier for devices constituting the current-mirror pairs have been increased by a factor of 20. This increases current in bias block, I_{bias} 20 times which becomes 90 μA. While the transconductor cells have no impact in current and remains half of 4.5 μA. The transconductance of bias circuit is $ln(4)/R_B$, 1.5 mS and that of the proposed transconductor cell is 37 μS, which is 1/40 times that of the bias as per the geometric ratios. This value arises by taking the starting point of similar g_m efficiency as that of the previous transconductor cell and then incorporating the design choices as discussed. Having similar g_m-efficiency transforms into similar programmability resolution of the filter as that of the previous circuit.

3.2 Filter

From our discussion in *System Design* (Section 2.2), we know that the high frequency front-end filter in MRI receiver is a 6^{th} order bandpass filter with Q-factor of 400 to provide a sharp-roll off in its frequency response. Also, it provides a gain of 60 dB at the center frequency which is the Larmor frequency (127.8 MHz) of MRI receiver. For an application of MRI where the demand for accuracy is high, it is important that the filter should retain its desired time constants at all operating condition. A limitation imposed by its working principle, achieving a resonance between the MRI receiver and magnetized protons in body (if, target nucleus is H^+). So, it is implemented with RLC resonators and transconductors connected in parallel, together achieving high stop band attenuation and high passband gain accurately as demanded.

The LC tanks implement the three pair of complex-conjugate poles which holds their position very precisely, being the off-chip components. This eliminates the need for a supplementary tuning circuitry, otherwise required in the case of active-RC and g_m-C filters, whose time constants are prone to large fluctuations (upto 30%) with process, supply and temperature variations [32]. With the help of tuning circuit, the time constants are realized in terms of the ratio of components rather than the absolute value by making the use of an accurate clock. Given, that such a tuning can be extremely challenging at the high frequency of 100's of MHz and Q $>$ 20, the adopted filter architecture despite being a high frequency and highly selective filter, leverages the benefit of accuracy required for MRI without any need for tuning circuit.

3.2.1 Fully-Differential Filter

Gm block	mA/V (mS)	Gm block	mA/V (mS)
Gm_1	2.5	Gm_{23}	-1.7
Gm_2	1.25	Gm_{34}	-0.02
Gm_3	1.25	Gm_{234}	0.34
Gm_4	0.625		

Table 3.3: Transconductance per Gm block in ideal filter

Recalling the filter architecture and the schematic, it is a fully-differential circuit. With proposed transconductor, which is also a fully-differential circuit, the filter schematic is presented in Fig. 3.7. As it was discussed in *System Design* (Section 2.2), transconductance per block (Gm) is decided by the filter specifications and comes out to be as shown in Table. 3.3 (reiterating for continuity). Also, g_m of the unit transconductor cell can be any value depending on the desired resolution of the filter programmability. Taking the same resolution, the realized g_m of the proposed transconductor is 37 μS, while the previous transconductor

had a value of 31.25 μS. The g_m of 37 μS arises with the starting point of keeping similar g_m efficiency as well as balancing the design choices as discussed in the earlier section. No doubt, a different g_m value could have been achieved by varying R_B and biasing point of transistors. But at this value, the common-mode level of transconductor is maintained nearly in the middle of the voltage supply, V_{DD}. With the proposed transconductor, the number of unit cells, $N(Gm)$ in the filter can be calculated by dividing transconductance of the block from table above with that of the unit g_m-cell (37 μS). Table 3.4 shows the number of unit g_m-cells in each Gm block for fully-differential filter employing proposed transconductor.

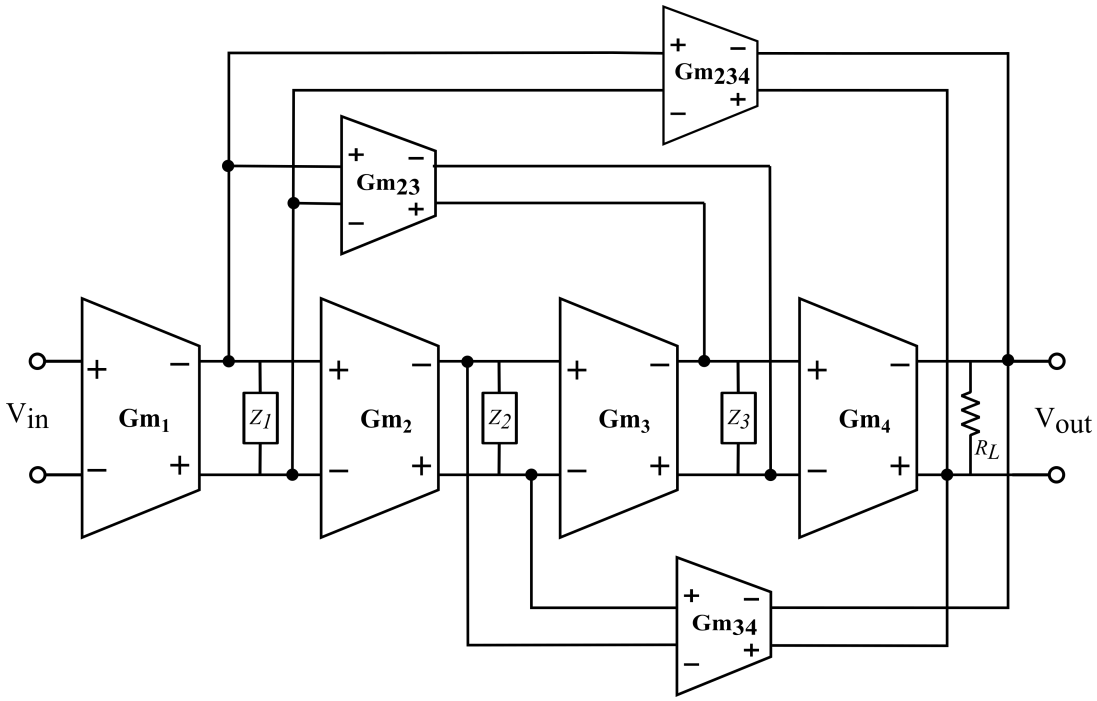


Figure 3.7: Fully-differential filter using proposed transconductor

Gm block	No. of g_m-cell	Gm block	No. of g_m-cell
$N(Gm_1)$	67	$N(Gm_{23})$	46
$N(Gm_2)$	34	$N(Gm_{34})$	1
$N(Gm_3)$	34	$N(Gm_{234})$	9
$N(Gm_4)$	17		

Table 3.4: Number of proposed transconductor cells per Gm block in filter

3.2.2 Parasitics in Filter

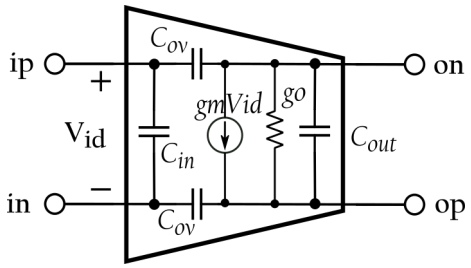


Figure 3.8: Equivalent model of the transconductor with parasitics

An equivalent model of the transconductor with an input V_{id} and transconductance g_m is shown in Fig. 3.8. Apart from the desired parameter of g_m, transconductor has some output conductance(g_o), input and output capacitance(C_{in} and C_{out}) as well as coupling capacitance(C_{ov}). These are undesirable parameters of transconductor for ideal implementation of filter and thereby seen as parasitics to the filter. However, due to adopted architecture the parasitics can be well accommodated into the respective resonator.

A. Resonator Tuning

Effectively, resonator elements of the filter namely inductance, capacitance and resistance always remain same as that of the ideal filter since they are in accordance with the three pole frequencies. After plugging the proposed transconductor cell, the filter has to tune back to match its desired resonance frequency and Q-factor at all three LC tanks which are otherwise impacted by the parasitics from transconductor. The output resistance or parasitic resistance(R_{par}) from transconductor cell can be analytically calculated as

$$R_{par} = \frac{1}{g_o} = 2(r_{outp}||r_{outn}) \tag{3.13}$$

If R_{par} is parasitic at the output of unit transconductor cell, then parasitic resistance at the output of one Gm block equals to $R_{par}/N(Gm)$, where $N(Gm)$ denotes the number of transconductor cells sharing the common output. Parasitic resistance is seen in parallel with the LC tank, now the resonator resistance can be calculated such that the net load at LC tank is 16 kΩ, same as the ideal. .

Similarly, input and output capacitance of the transconductor cell also contribute in tank-capacitance for the three resonators. Table 3.5 provides the residual resistance and capacitance required for resonator once the parasitics from proposed transconductor cells are included. It can be noticed that the tank capacitances needs a precision of less than 100 fF, owing to high Q and high frequency operation. To meet this requirement the tank capacitor has been realized in two parts. One, an integrated capacitance bank with its

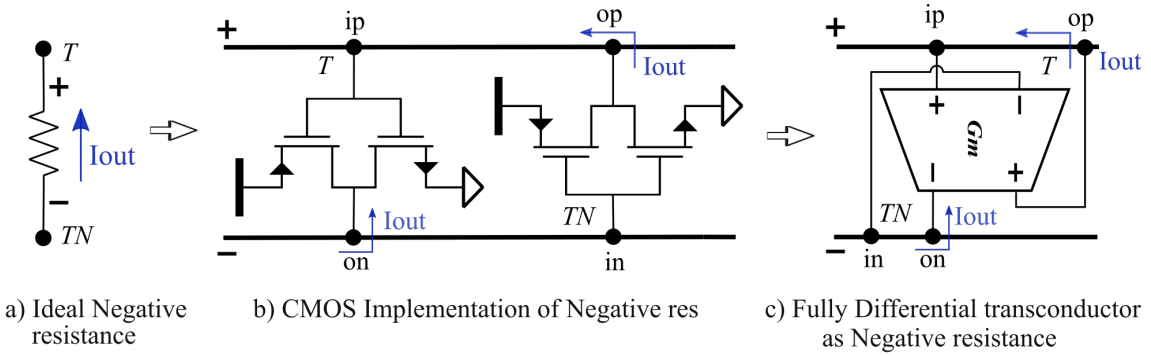
Pole (MHz)	Capacitance (pF)		Resistance (kΩ)		Q-factor
	Ideal	with Gm	Ideal	with Gm	(with Gm)
-0.160 ± j 127.8	31.02	30.32	16	-16.5	394
-0.159 ± j 127.2	31.31	31.02	16	310	387
-0.160 ± j 128.4	30.73	30.26	16	-13.1	384

Table 3.5: Resonator components for proposed transconductor implemented filter. L=50nH

precision of less than 10 fF and a range of 2 pF. It is a digitally programmable capacitance bank and shall be calibrated one-off. While the other part is standard off-chip capacitance.

B. Negative Resistance

Table 3.5 shows negative resistance and also the discussion of negative resistance came up earlier in relation with the previous transconductor implemented filter in *System Design*. The concept of negative resistance is fundamentally opposite to that of the normal course of resistance. Normally, if there is a voltage applied across a resistor, the current flows from positive terminal to negative terminal, following the Ohm's law the ratio of V/I is positive. Whereas for negative resistance, a voltage applied across its terminals results in the current flow from negative terminal towards positive. Such a circuit has to produce power instead of dissipating, so needs to be an active device. This can be realized with a transconductor as it's a voltage to current converter analogous to resistance. Fig. 3.9 depicts the concept and implementation of negative resistance with the help of inverter as the proposed transconductor is inverter based.



a) Ideal Negative resistance

b) CMOS Implementation of Negative res

c) Fully Differential transconductor as Negative resistance

Figure 3.9: Concept and implementation of negative resistance

For node T, the inverter gives rise to an inward current (I_{out}), a negative current, at on in response to a positive voltage applied at ip. Similarly for node TN, another inverter gives rise to an outward current (I_{out}), a positive current, at op in response to negative voltage

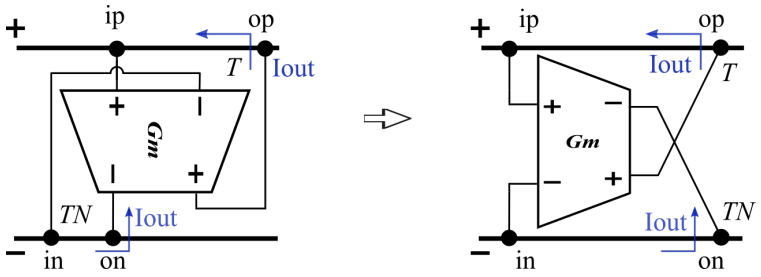


Figure 3.10: Negative resistance implementation with proposed transconductor

applied at *in*. This way the two inverters behave as negative resistance for the respective node looking into their input. As discussed in the previous section, the small-signal model of the proposed transconductor is equivalent to that of two inverters connected differentially, it can be used to implement the negative resistance as shown in Fig 3.9.c.

The proposed transconductor implemented negative resistance can be redrawn as shown in Fig 3.10. It can be noticed here that the transconductor is connected in a cross-coupled fashion from input to its own output providing a self-bias structure. It senses its output common-mode level and makes the correction thereby maintaining the desired common-mode level of all the transconductors throughout the filter and omitting the need to implement any common-mode feedback (CMFB) circuit separately. Note to be taken, all the three resonator resistances are negative in order to incorporate the parasitic resistance of the off-chip components. This can be seen in the Table 4.3 under Section 4.2.

C. Resonator Decoupling

In addition to the tuning of tank elements as explained above, parasitics from transconductor also lead to the coupling of tanks which is highly undesirable. Three resonators are meant to function independent of each other so as to show the peak response only at their respective resonance frequency. However, coupling would disrupt desired behaviour of the filter due to interference of the signal between resonators. Being an inverter based transconductor, same transistor pair is employed to function as input as well as output. So, there exists a capacitance between input and output node of the inverter coming from gate-drain capacitance C_{gd} of MOS denoted as C_{ov} in the parasitic model of the transconductor in Fig. 3.8. In the fully-differential filter, coupling would arise across three Gm blocks which are connected between any two resonators, i.e. Gm_2, Gm_3 and Gm_{23} as can be seen in the filter schematic, Fig. 3.7.

This parasitic capacitance can be compensated for proposed transconductor as shown in Fig. 3.11. For a single inverter there exists two C_{gd} capacitances between its input and output one each from nMOS and pMOS. The proposed transconductor is a fully-differential pair of inverter so the capacitance is doubled, incurring $2C_{gd}$ per inverter. To compensate this parasitic capacitance an equivalent capacitance of $2C_{gd}$ can be placed in a cross-connected

fashion, thereby decoupling the Gm block as shown in Fig. 3.11c. Table 3.6 shows decoupling capacitance, $C(Gm)$ required for the three Gm blocks.

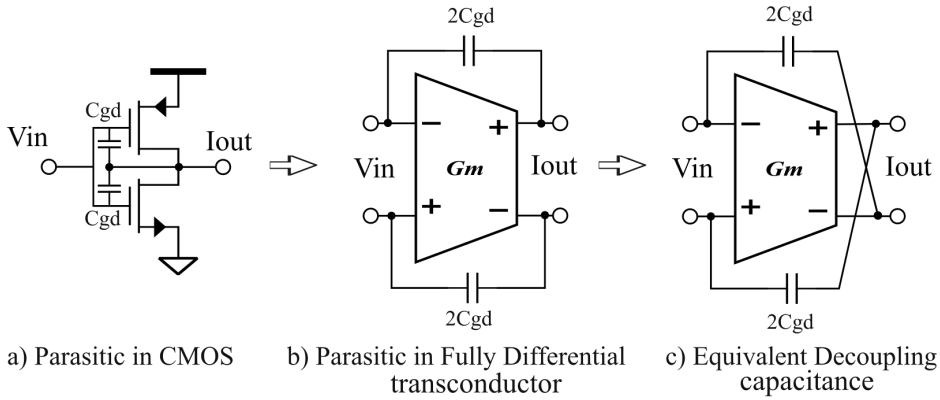


Figure 3.11: Compensation for parasitic capacitance of transconductor

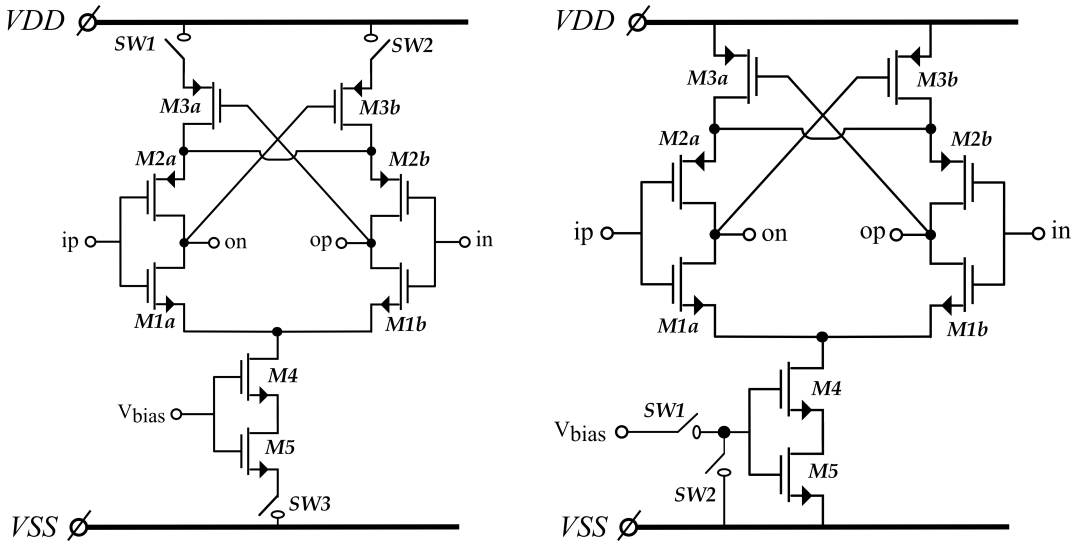
Gm block	Decoup Cap (fF)
$C(Gm_2)$	29
$C(Gm_3)$	29
$C(Gm_{23})$	40

Table 3.6: Decoupling capacitance for Gm block in filter

3.2.3 Programmability

Implementing Gm block in the filter by using parallel-connected identical unit transconductor cells, provides the freedom of programmability to the IC. Leveraging the absence of internal nodes in the proposed transconductor cell, there are no parasitic high order poles introduced in the filter which could have led to the phase error and disturb its Q-factor. However, parasitic capacitance and resistance in the filter will vary depending upon the number of unit cells turned-on or off, which can affect the frequency-tuning and Q-factor while achieving wide programmability of the filter using switchable g_m-cells. But in our design since the transconductor parasitics are directly available at the output, this is taken care of with the help of integrated capacitance bank and knowing that the tank load is also implemented with g_m-cell, they can be switched on or off, varying the resistance as per the need. Thus, this filter implementation exploits the benefit of parasitic-immunity which obviates the need for extra circuitry for Q-tuning or frequency-tuning with the change in center frequency, necessary in the case of cascoding or cascaded transconductor topology.

While tuning the receiver to a new resonance frequency with the help of inductor and capacitor only poles get shifted, but there is a need of shifting the zeros as well proportionally with the poles, such that the three complex-conjugate pair of poles are always surrounded by the two complex-conjugate pair of zeros. Given that, zeros are implemented by transconductors in the feed-forward paths. In addition, while programming the filter to new frequency, although the resonator load will remain same depending on Q, but the current will scale. It is because, with the reduction in center frequency the noise bandwidth will reduce, so the passband gain requirements may vary. This altogether implies that the transconductance cells should be scaled as well depending on the requirements. It implies that there is a need of programmability feature in the transconductor cell, such that the number of ON transconductors can be scaled up or down depending on the required configuration of the filter IC with the help of switches.



(a) Switch Configuration - A

(b) Switch Configuration - B

Figure 3.12: Switches configurations in transconductor for filter programmability

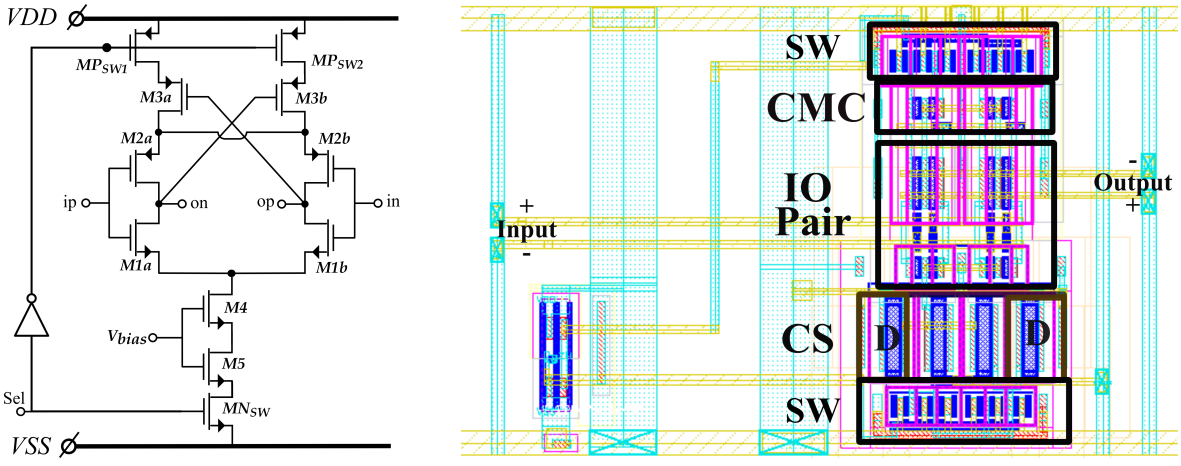
Two of the switching configurations for the proposed transconductor are discussed here, shown in Fig. 3.12. Configuration-A uses three switches, SW1 and SW2 in series with $M3_{a-b}$ pair, connecting them to V_{DD} supply and SW3 in series with $M5$, connecting it to V_{SS} supply. Configuration-B uses two switches in the current-source. One switch, SW1 is in series with $Vbias$ whose one node is connected to common-gate of $M4 - M5$ and other to the $Vbias$, thus responsible for a connection to the biasing circuit, while the second switch SW2, is pulling the bias node to ground when the transconductor is turned-off. Although, latter of the two configurations provides a power efficient low-leakage solution, but it adds a series transistor biased in triode region to the bias node whose resistance can vary with process, temperature and voltage variations and so it will compromise the matched structure of

constant-g_m technique and defeats the purpose. Hence, for variation immunity and matching reasons the switch configuration-A has been adopted. Here, the two set of switches are regulated with an inverter and controlled by a digital input signal Sel. If Sel is high, the transconductor is switched ON and vice-versa shown in Fig. 3.13a. This raises the need for implementing switches in the bias circuit as well to keep the matching consistent although they are always ON. In bias circuit, it's the nMOS current-mirror pair which is matched to the current-source of transconductor under replica biasing. Hence, switches in bias block are implemented only at the connection of V_{SS} power supply.

3.3 Layout

For high frequency operation low-threshold voltage (LVT) transistor-models have been used. Since, the filter integrated circuit is a mixed-signal chip which means analog circuit is sharing chip with that of digital, to prevent the analog design from substrate noise due to its digital counterparts deep n-well transistors have been used. The circuit implementation is dependent on matching of the transistors, the common-centroid layout methodology has been ensured locally in the cell structure including the placement of devices and routing of signals.

A. Transconductor cell



(a) Schematic (b) Layout

Figure 3.13: Transconductor cell Layout

Fig. 3.13 shows the layout of the proposed transconductor unit cell. The overlays in the figure show the three elements of the transconductor paired with top and bottom switches (SW) for programmability- common-mode control (CMC), input-output inverter

pair (IO pair) and self-cascode current source (CS). The block at the right end of the layout, Fig. 3.13b, shows the standard inverter cell used for regulating switches with the digital input signal "Sel". The area of unit proposed transconductor cell is $10\mu m$*$7\mu m$.

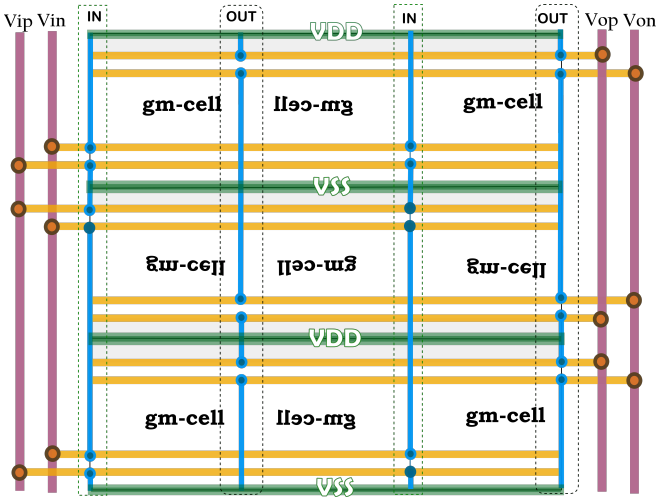


Figure 3.14: Floor plan of the g_m-cells tiling to construct Gm block

The g_m-cell is laid out such that it can be mirrored horizontally as well as vertically for tiling the complete Gm block with common-centroid symmetry, sharing the common input-output rails as well as power supply rails between the adjacent cells, shown in Fig. 3.14. Horizontal yellow lines display IO paths in metal 2, blue interconnects display vertical connection between IO ports for the adjacent cells, routed in metal layer 1. The input-output of unit cells connect with Vip-in and Vop-on at the higher level in upper metal layer. Whereas, green lines display the local power supply rails of the g_m-cell shared with adjacent cells which are also routed in metal 2. The complete Gm block shall be surrounded with an array of dummy cells at the edges. This way the matching between the transconductor cells is ensured.

B. Fixed-transconductance Bias

Fig 3.15 shows the layout of biasing circuit. Overlays in figure display the three elements of biasing circuit - nMOS and pMOS current-mirror pair (CM pair), negative feedback loop (opamp) and resistance bank (R_{bank}). The transconductor (g_m-cell) is shown along the bias circuit to reflect on their relative sizes. The overlay named "CM pair" in figure consists of the nMOS and pMOS current-mirror pairs as well as nMOS switches in the bottom rows. "CM pair" strictly follows the common-centroid structure, as matching is a necessity of the constant-g_m bias technique.

Opamp is locally following the common-centroid layout in its components - differential input, active-load, current source and second stage transistors. Overlay named R_{bank} includes

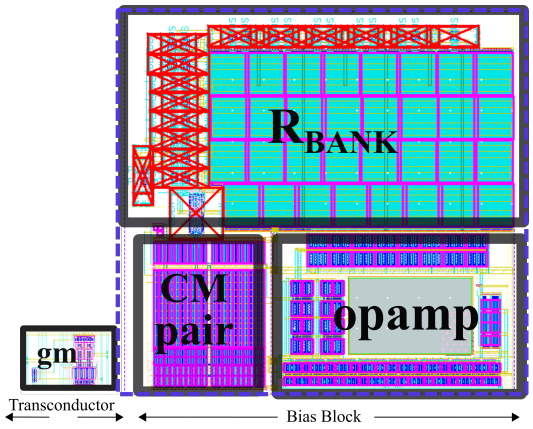


Figure 3.15: Bias Block Layout. Transconductor cell shown for relative area

fixed resistance and programmable 4-bit binary weighted resistance bank. Rows in blue display the four switches $b_0 - b_3$, while the red marking display the poly resistor, it's an isolated n-well resistor which provides much better stability to variations as mentioned before. There also exists start-up circuit in this layout, not marked here due to its small display size owing to its small geometry (W, L) since it uses weak devices (small W/L). The area of the complete biasing circuit is 60 μm * 60 μm. All g_m-cells on the chip will be biased with a single block, shown in Fig. 3.15. Hence, only one biasing unit is required for the entire chip.

Chapter 4

Results

In previous chapter, design implementation for the proposed transconductor and its biasing circuit have been detailed. Following which the filter was presented incorporating parasitics and programmability of the transconductor.

In this chapter, post-layout simulation results have been presented to show the performance of proposed constant-transconductance circuit. For benchmarking, results have been compared with post-layout simulation of the previous transconductor. The impact of transconductor on filter is depicted using frequency response and shift in bandwidth as well as passband gain. The variations considered are process, voltage, temperature and mismatch. Lastly, the filter performance is evaluated corresponding to output noise in terms of SNR and linearity in terms of THD.

4.1 Transconductor

In this section, performance of the proposed transconductor cell is evaluated in terms of its transconductance, g_m with the help of post-layout simulations. A testbench has been constructed in ADE/ADEXL environment of Cadence Virtuoso as described in the section below.

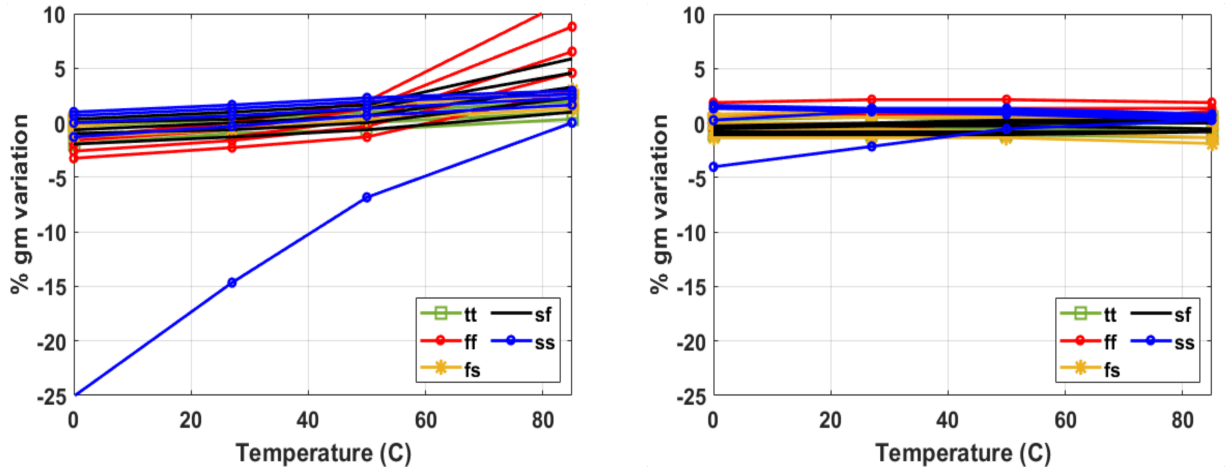
4.1.1 Transconductance Variation

A. Process, Voltage supply and Temperature variation

To evaluate deviation in g_m of the proposed transconductor, RC extraction of the bias and g_m-cell have been simulated for a temperature range of $0°C - 85°C$ at a voltage supply of 1.1 V, varying within $\pm 10\%$ for all five process corners. In simple words, for every process corner (tt, ss, ff, sf, fs), there are four temperature (0, 27, 50 and 85)°C and five supply variation (-10, -5, 0, 5 and 10)% data points evaluated.

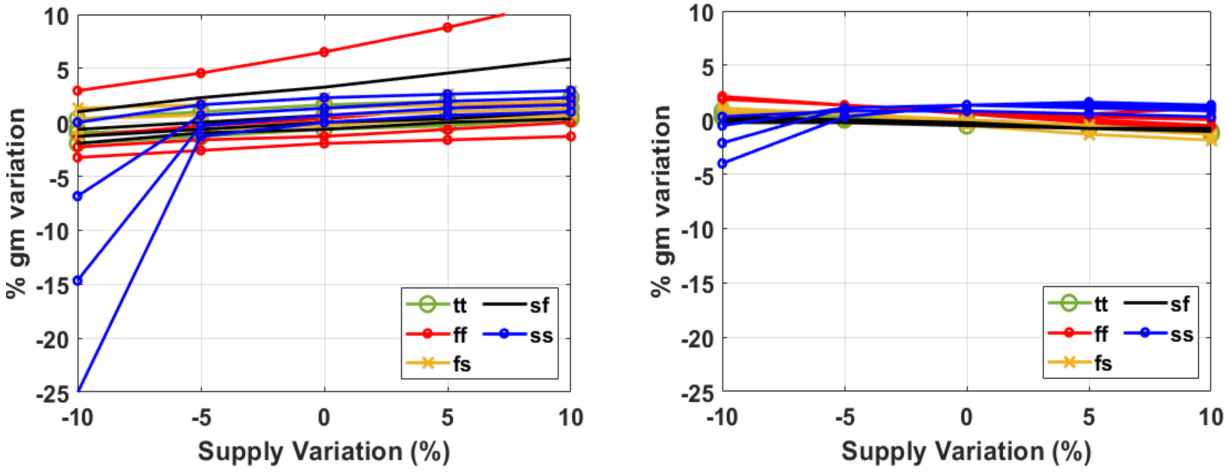
As discussed in previous chapter, to incorporate process variations in the bias resistance, R_B, a digitally programmable resistance bank has been employed. It trims R_B corresponding

to the process corner so as to keep its effective resistance same all throughout the process variations. The 4-bit digital code corresponding to five corners used for simulations is given in Table. 4.1. However at the chip level with sufficient flexibility provided by the range and resolution of bank, the bias resistance will be trimmed in accordance with desired response of the filter only.



(a) Previous Transconductor (b) Proposed Transconductor

Figure 4.1: g_m variation with temperature (curves with same colour show supply variation)



(a) Previous Transconductor (b) Proposed Transconductor

Figure 4.2: g_m variation with supply (curves with same colour show temperature variation)

Process corner	4-bit binary code
tt/sf/fs	0110
ss	0000
ff	1111

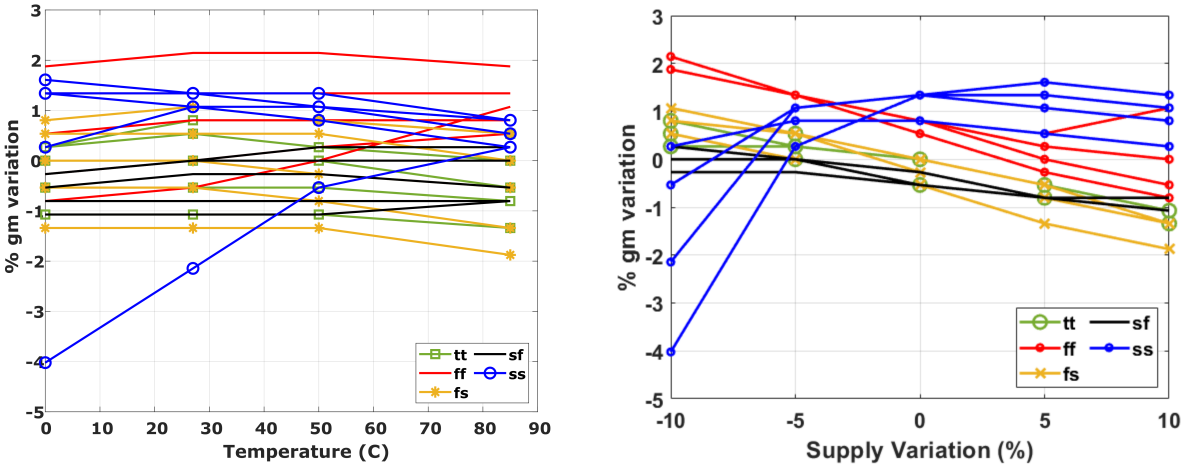
Table 4.1: 4-bit digital code of resistance bank for process corner

Fig. 4.1 and 4.2 shows the comparison of g_m deviation in proposed transconductor circuit with that of the previous circuit. Fig. 4.1 shows the results with temperature on x-axis and multiple curves with same colour denote the voltage variations for one process corner. Likewise, Fig. 4.2 shows the voltage variation on x-axis and vice versa. The two figures represent the same data but with different x-axis.

As it is clearly visible from the two comparisons, the proposed transconductor circuit provides constant-g_m over PVT variations, rendering plots almost parallel to x-axis parameter variation. It can be noticed that ff corner shows the maximum positive deviation while ss corner gives the maximum negative deviation. This is expected as the effective resistance of R_B decreases at ff corner, following which the g_m increases and vice versa for ss corner.

At typical corner, the proposed transconductor shows a deviation of merely 1%, whereas including process variations the deviation in g_m remains mostly under $\pm$ 2.5%. It is an improvement of more than 10% as compared to the previous transconductor across all corners whereas an improvement of 4% at typical corner. Along with the major factor of constant-g_m bias technique, replica biasing and matching, other factors such as making K_n equal to K_p has also assisted in obtaining such a good stability as they balance out the variations.

Zooming in to see the performance of the proposed transconductance circuit in Fig. 4.3b, which is a magnified version of Fig. 4.2b. As mentioned earlier the two plots show the same results only difference is that of the representation. The worst case condition of extremely low voltage supply (-10%) and cold temperature of 0°C at slow (ss) corner, shows a deviation of -4% in g_m. Given that in subthreshold region, the devices are biased such that ($V_{DS} \geq 5V_T$) to remain in weak inversion saturation and independent of drain-source voltage. At slow corner, low temperature and low voltage supply threshold voltages increases and headroom decreases, due to which the operating point of tail current-source transistor, M4 in Fig. 3.4b shifts from deep saturation to the edge of saturation, thus its biasing current reduces. The situation could have been improved by sizing the input/output pair further wider but that means it will shift the common-mode level away from mid of the supply. Another possibility is skewing the inverter such that nMOS is wider than pMOS to keep the common-mode level at mid as well as providing the headroom to current-source but then we have K_n much greater than K_p and they will not be balancing the variations anymore. The input/output pair have been sized such that K_n equals to K_p, balancing the variations as well as canceling the non-linearity which has reaped significant benefit, visible in the results. Although, it can be said that being a medical device which is examining the patient's body for a duration of



(a) With Temperature (b) With Supply

Figure 4.3: Proposed transconductor g_m variation - Zoomed in

20-50 minutes, it is highly unlikely that the temperature of the examination room or more precisely the temperature of the receiver while taking the scan is 0°C, under the practical operation of MRI [36].

B. Process and Mismatch variations

To verify that g_m deviation of the proposed transconductor stays within limitations under the impact of mismatch, Monte Carlo simulations have been done for all five process corners at a total of 1000 points. Unlike, usual "process and mismatch" simulations, here the process corner variations are taken care of with the help of digital code, as mentioned before in Table 4.1, that trims the bias resistance, R_B to the desired value for each of the five process corners denoted as tt_MC, ss_MC, ff_MC, sf_MC and fs_MC. Fig. 4.4 shows a combined histogram for the proposed transconductor representing g_m deviation due to mismatch for all process corners on same scale.

It can be noticed that deviation in g_m due to mismatch across all five process corners is majorly within -1.5% to 2.5%. It is ff corner that shows the maximum positive deviation with mismatch which is expected as well. Since, at ff corner the effective resistance of R_B per unit length of poly will be minimum, it requires maximum length or in other words, maximum resistance realized on bank. For higher accuracy, one can increase the range and resolution, i.e. reduce the least significant bit of resistance bank but this means more number of bits and higher area. For every bit added, the number of resistors become double and switches need to be even larger, so as to have a negligible ON resistance compared to the smallest resistance realized. So, it's a trade-off between accuracy and area. Since, there are very few such cases, 2 in 1000, i.e. less than 0.2% probability, for which the variations reach

3% maximum across all process corners. It can be accepted here taking the trade-off into consideration.

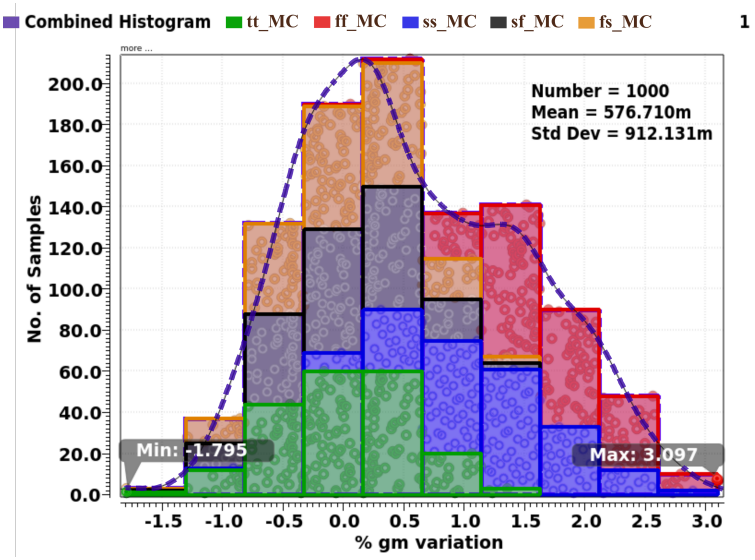


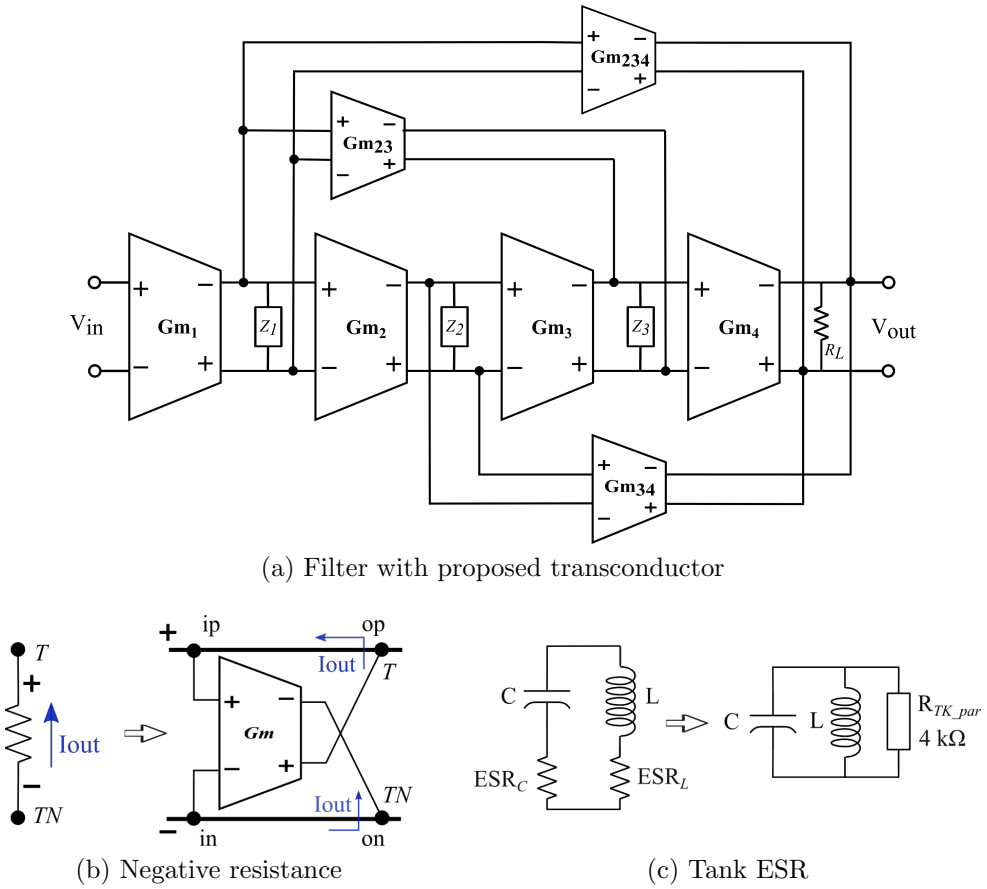
Figure 4.4: Transconductance variation with device mismatch using Monte Carlo simulation

4.2 Filter

As mentioned before, the filter IC is out of scope to layout, for it is a mixed-signal IC, sharing area with digital counterparts. However to replicate the scenario which concerns with evaluation of the proposed transconductor in filter circuit, a testbench has been created in Cadence Virtuoso ADE/XL environment. Testbench takes care of parasitics associated with the transconductor as well as off-chip components, i.e. LC tank has an equivalent series resistance (ESR). The testbench can be summarized as follows, refer to Table 4.2 and Fig. 4.5.

Gm block	No. of g_m-cells	Gm block	No. of g_m-cells
$N(Gm_1)$	67	$N(Gm_{23})$	46
$N(Gm_2)$	34	$N(Gm_{34})$	1
$N(Gm_3)$	34	$N(Gm_{234})$	9
$N(Gm_4)$	17		

Table 4.2: Number of proposed transconductor cells per Gm block in filter



(a) Filter with proposed transconductor

(b) Negative resistance

(c) Tank ESR

Figure 4.5: Fully-differential filter using proposed transconductor

- RC extracted transconductor cells are called n times for a Gm block, say Gm_1 has 67 unit cells, so here n = 67. This connects 67 g_m-cells in parallel at Gm_1 block, in the netlist.
- All transconductor cells are biased with a single unit of RC extracted biasing circuit.
- ESR of inductor and capacitor constructing LC tank is modeled with its equivalent parasitic tank resistance of 4 kΩ in parallel. This resistance has to be accounted in load resistance at each of the three tanks.
- Parasitics from the transconductor cells have been incorporated in the resonators' resistor and capacitor.
- Resistance required after incorporating parasitics in the filter to achieve the net load resistance of 16 kΩ at each of the three resonators, is negative. Negative resistance is implemented with cross-coupled transconductor as explained before in *Parasitics in*

Filter (Section 3.2.2). Table 4.3 shows resonator components after incorporating the parasitics in filter.

- Process variation has been taken care of with the help of digital code as mentioned earlier, provided in Table 4.1.

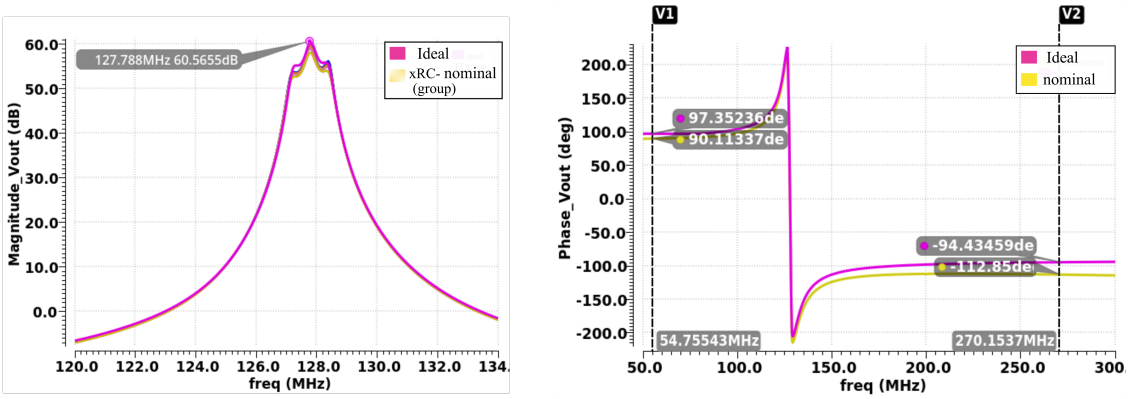
Pole (MHz)	Capacitance (pF)		Resistance (kΩ)	
	Ideal	with Gm	Ideal	with Gm
-0.160 ± j 127.8	31.02	30.32	16	-3.25
-0.159 ± j 127.2	31.31	31.02	16	-4.05
-0.160 ± j 128.4	30.73	30.26	16	-3.04

Table 4.3: Resonator components of the filter after extraction of proposed g_m-cell. L=50 nH

Impact of transconductance variation on the filter is depicted in its frequency response. Magnitude and phase response are analyzed separately. Since it is a very high Q filter with narrow passband, frequency response as a whole doesn't provide clear evaluation of stability of the transconductor. Henceforth, two major parameters of the filter, i.e. passband gain and bandwidth which are dependent on transconductance (g_m), have been analyzed individually with temperature, supply, process and mismatch variations. Rather than passband gain, gain only at the center frequency of the filter is analyzed here, as it is important to ensure gain at the Larmor frequency for MRI receiver. In the adopted architecture, rather than having a flat passband, it is slightly skewed with a peak at the center frequency due to the presence of closely lying poles on its either side.

4.2.1 Frequency Response

Frequency response gives a reflection of an overall behaviour of the filter showing its stopband, passband and related attenuation/gain respectively. Fig. 4.6 shows the magnitude response on the left and phase response on the right. Both are compared with the ideal response (magenta). The magnitude plot shows the response of the filter at typical process corner including supply and temperature variations, denoted as the "xRC - nominal (group)". While the phase response only shows the nominal corner without supply and temperature variations, for the purpose of clarity of the plot. From magnitude response away from the pass band, one can see the filter response aligns quite well with each other. Therefore, it can be said that phase response matches for all other PVT variations and will be same as depicted for one plot. It can be asserted from the transconductance variation analysis with process corners in Section 4.1.1, that for other corners the frequency response of the filter will follow the same suit. Moreover, the process variations are taken care of in the Monte Carlo simulations in the subsequent section.



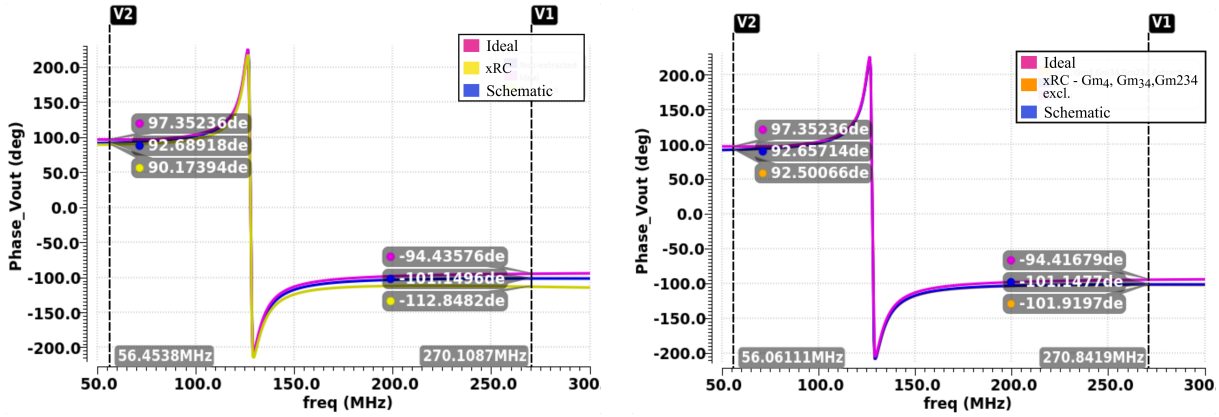
(a) Magnitude Response (b) Phase Response

Figure 4.6: Filter frequency response. Comparison with ideal response (magenta)

Magnitude response is shown in log domain and it can be inferred that it matches quite well with the ideal. However, phase response shows some deviation at higher frequencies. Limitation of phase response is that the phase-shift at 270 MHz should be under -30° from ideal response. This is driven from the receiver architecture specific to Philips. Remember, the filter so far analyzed has been excluding sixth-zero, implemented with an integrator after the buffer. There is a phase-shift of -180° across the filter (the one, excluding sixth zero) coming from resonator block. After adding sixth-zero, a phase-shift of +90° is added such that the total phase-shift across full filter would be -90° from -180°. By ensuring the phase difference limited to -30° from ideal response, phase error has been controlled as per the receiver requirements. 270 MHz is the half of on-chip clock-frequency of 540 MHz for 3 T MRI machine. This is set by sampling frequency requirements of ADC stage succeeding the filter in the MRI front-end receiver.

With proposed g_m-cell, the phase difference between the extracted and ideal response of the filter at 270 MHz is -18° (-112°+94°), which lies within the limitation of -30°, as shown in Fig. 4.6b. However, it is further investigated to understand the cause of this difference. In Fig. 4.7a, it can be observed that the phase response of the schematic simulations of the filter in blue, show a deviation of only -7° from ideal. Which means there is a difference in extracted and schematic simulation results by -11°. To understand the origin of the phase difference, the transconductor blocks which are connected at the output of the filter, i.e. R_L have been replaced with their schematic version and after simulation it has been observed that two simulations are now aligned (orange and blue) as shown in Fig. 4.7b. This implies that the additional phase difference of -11° is coming from the parasitic output capacitance of the transconductor which has been increased after extraction and induces a high order pole, out of the band of interest.

For such a highly selective and high frequency filter, having a very narrow passband, looking at frequency response only doesn't give any good understanding of the performance



(a) Extracted vs Non-extracted

(b) Extracted excl. output Gm vs Non-extracted

Figure 4.7: Phase comparison between schematic and extraction with respect to the ideal

of transconductor cell. Therefore, parameters of the filter response such as center frequency (f_0), gain at the center frequency and bandwidth (Δf) can be analyzed separately under the impact of process, temperature and supply variations to understand the resilience of the proposed transconductor at the system level more closely. Given that, the pole frequencies are well-regulated by three LC tanks, the center frequency is fixed at 127.8 MHz achieved by tuning the filter incorporating parasitics as mentioned previously, wherein the integrated capacitance bank uses digital input code to align filter to the desired resonance frequency.

4.2.2 Gain at Center Frequency

Impact of transconductance variation leads to change in passband gain of the filter. Transconductors are the only gain element of the filter and being available in such a large quantity makes the passband gain sensitive to g_m of unit cell. Gain at the center frequency reflects amplification of the signal at the Larmor frequency and it is a crucial parameter for SNR and dynamic range of the filter.

A. Voltage and Temperature variations

Ideally, gain at the center frequency (f_0), 127.8 MHz is 60 dB. Under temperature and supply variations at nominal corner, deviation in gain at f_0 is shown in Fig. 4.8. The five curves show variation in supply voltage, i.e. from 0.99 V to 1.21 V (-10% to +10%). The results show an overall deviation of +1.8% to -2% in gain, which is decreasing with temperature rise. This is because g_m of the unit cell also shows a very small decline with temperature rise nominally, as in Fig. 4.3a. Thus, deviation in gain of the filter is under 2%, which is the sought-after performance from the proposed circuit. It can be noticed that the variation

with supply is negligible, thanks to the self-cascode current source in transconductor and negative feedback loop in bias circuit.

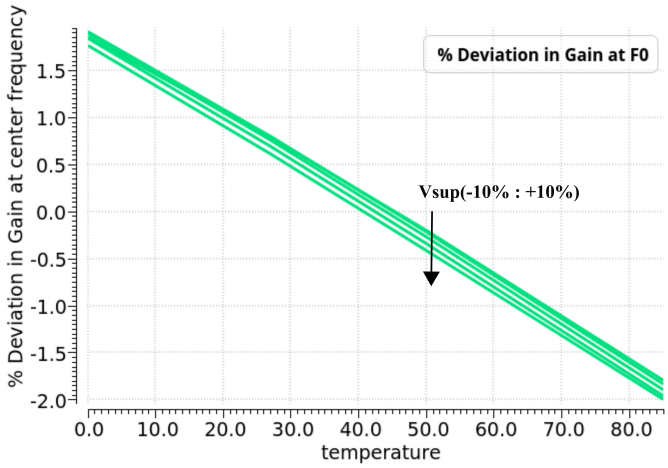


Figure 4.8: Deviation in gain at f_0 (127.8MHz) of filter with supply and temperature

B. Process and Mismatch variations

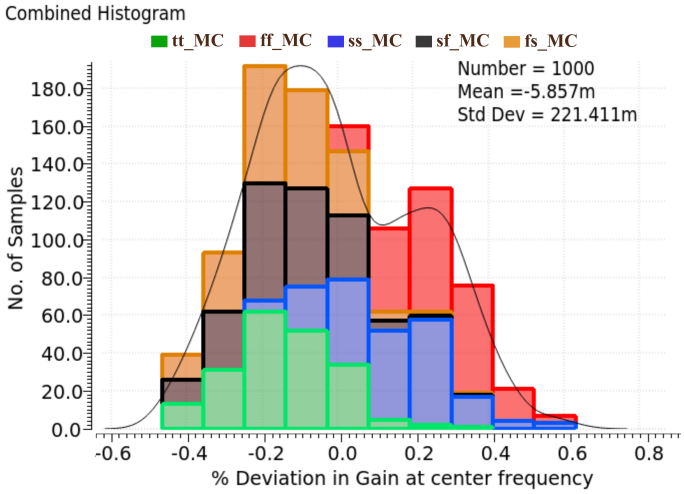


Figure 4.9: Monte Carlo simulation for deviation in gain at center frequency 127.8 MHz

The process and mismatch variations have been evaluated likewise as done for the transconductance variation before. Five process corners (tt_MC, ss_MC, ff_MC, sf_MC and fs_MC) take the input of the digital code to trim the bias resistance. A total of 1000 Monte Carlo

simulations give a combined histogram, shown in Fig. 4.9. It depicts deviation in gain of the filter at 127.8 MHz (f_0) with process and mismatch variations, which lies between -0.5% to +0.6%. The results are very well under the performance target of ± 2% about 60 dB. It can be said that mismatch and process variations affecting the gain of filter are taken care of quite well, thanks to the common-centroid matching in the layout.

4.2.3 Bandwidth

Bandwidth (Δf) for a bandpass filter is defined as the difference between -3 dB frequency points of rising and falling edge about the center frequency. We know that pole frequencies are taken care of by resonator components providing an almost fixed resonance frequency (center frequency) and two complex-conjugate pair of zeros define beginning and end of passband. However, passband is not flat but skewed in the center. Bandwidth of the filter can vary depending on g_m of the transconductor which is responsible for the shape of passband. Variation in transconductance of g_m-cell can alter the rate of change of filter response with frequency. Which then effectively disturbs the selectivity of the filter and bandwidth can spread more than desired.

A. Voltage and Temperature variations

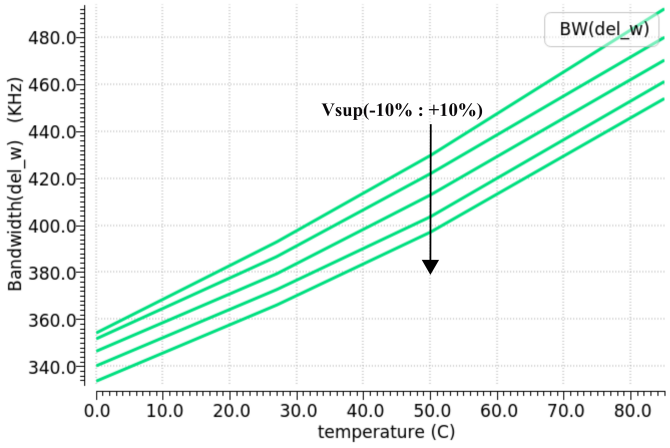


Figure 4.10: Deviation in bandwidth (Δf) of filter with supply and temperature variation

Ideally, -3 dB bandwidth of the filter is 350 kHz. Under temperature and supply variations at nominal corner, deviation in bandwidth of the filter (Δf) is shown in Fig. 4.10. Likewise, as in the case of gain variation, multiple curves in the plot show supply variations. The results show that -3dB bandwidth spreads with the rise in temperature due to the reduction in gain, the steepness of curve reduces.

It varies from 330 kHz to 490 kHz, i.e. the maximum deviation in bandwidth is 120 kHz which is merely 0.07% with respect to its center frequency 127.8 MHz, quite a negligible change. Due to the high selectivity of the filter it has a very narrow band and the change is extremely small. It is predominantly due to the fact that pole frequencies are fixed by the LC tank, thanks to the topology chosen for filter implementation. Also, with the stability of the transconductor the fact continues to remain intact.

B. Process and Mismatch variations

The impact of process and mismatch variations on bandwidth have been evaluated with the same setup as that of the gain deviation above. The combined histogram of 1000 Monte Carlo simulations is shown in Fig. 4.11. It depicts deviation in bandwidth (Δf) of the filter with process and mismatch variations that varies from 370 kHz to 428 kHz, i.e. a variation of 70 kHz maximum. This is equivalent to merely 0.05% with respect to center frequency 127.8 MHz, again a negligible change.

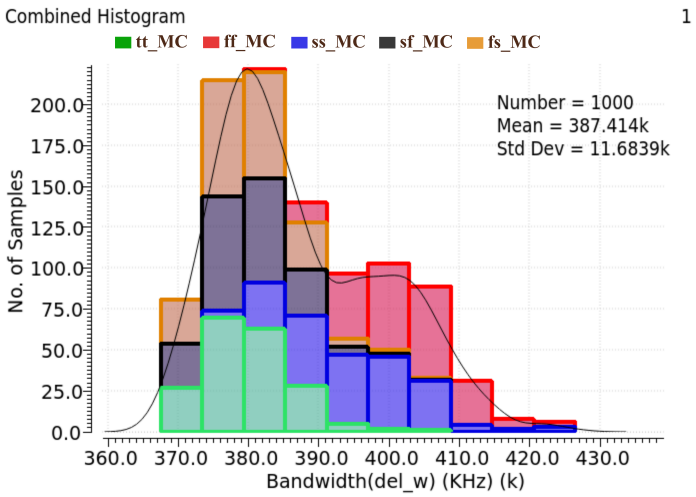


Figure 4.11: Monte Carlo simulation for deviation in Δf

From the results above we see that deviation in gain at f_0 is under 2% and deviation in bandwidth is under 0.1%. This indicates that the proposed transconductance circuit provides desirable filter frequency response.

4.3 Filter Performance

The filter is evaluated in terms of noise performance, dynamic range and linearity. The desired SNR from the MRI filter should be atleast greater than 90 dB as mentioned earlier.

4.3.1 Noise

This filter performs noise shaping operation on the incoming band defined by its transfer function. It suppresses noise in stop band with a desired attenuation and limits noise bandwidth with narrow passband as shown in Fig. 4.12. This is a major reduction in noise for such a wide band operation of 100's MHz by eliminating the noise floor out of band and limiting it to merely few MHz (125 MHz-130 MHz). Output noise power is 2.96 μV^2. The SNR calculation is done normalized to 1 V. For a sinusoidal input of $1V_{pk}$ AC, the peak output signal voltage at 127.8 MHz is 1 kV as shown in Fig. 4.12. Thus, SNR of the filter can be calculated as

$$\begin{aligned} SNR_{out} &= \frac{P_{sig}}{P_{noise}} = \frac{(1kV)^2/2}{2.96\mu V^2} \\ SNR_{dB} &= 10log_{10}(SNR_{out}) \end{aligned} \tag{4.1}$$

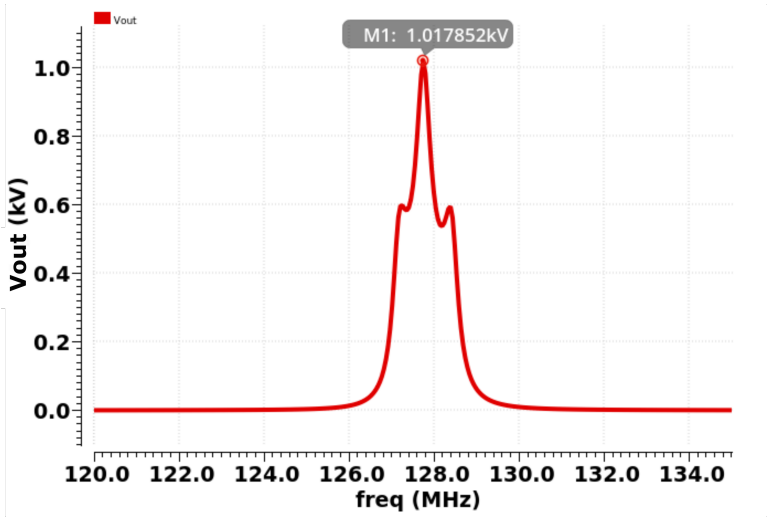


Figure 4.12: Filter magnitude response on absolute scale

SNR of the filter using proposed transconductance circuit is 112 dB, which is similar to the previous circuit. As long as the transconductor has a stable g_m, the noise performance is predominantly dependent on the adopted filter architecture due to its very narrow bandwidth with substantial passband gain. If it were a moderate Q filter with 0 dB passband gain, the noise would have been guided by the transconductors. However the noise performance of the filter indicates that the noise of the proposed transconductor is small as it is same as that of

the noise induced by a simple single ended inverter transconductor in the previous circuit. The noise spectrum of the filter with proposed transconductor is shown in Fig. 4.13.

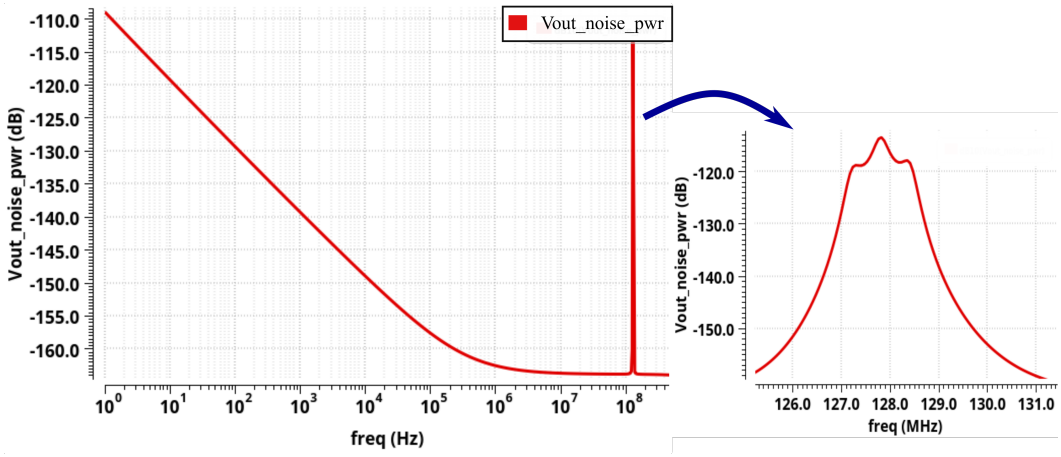


Figure 4.13: Output noise power spectrum of filter

Gain in passband of the filter amplifies the noise as well. This seems to be undesirable for noise blocking feature of filter although it is highly necessary requirement from the dynamic range point of view. The filter adds 1000x gain, so it separates the signal sufficiently above the noise level increasing its ability to sense weak signals efficiently. The dynamic range is defined as the ratio of maximum signal to the minimum signal sensed by the filter undistorted. The maximum is limited by voltage supply and minimum is set by the noise floor. However, in this case a normalized value can be considered because of the high frequency operation the signals show transient nature, rapidly changing over time and never clips which otherwise could have, under a steady-state operation. The normalized dynamic range of the filter is 112 dB.

4.3.2 Distortion

The distortion of the filter with proposed g_m-cell is analyzed at 127.8 MHz input frequency in terms of total harmonic distortion (THD). Fig. 4.14 shows the distortion spectrum of filter with THD of -63 dB, while that of the previous circuit is -42 dB. Since it is a very high frequency signal, the distortion under consideration is limited to third harmonic, higher order falls out of band of interest. The proposed transconductor has a differential topology, so it cancels out the even order harmonic non-linearity adding 6 dB more. Also, by making K_n equals to K_p for the input-output CMOS pair, the linearity has been enhanced significantly which was not implemented in the previous circuit.

In addition, power consumed by the filter using proposed circuit is 0.8 mW as compared to the previous circuit which consumes 1.75 mW. This is because with fully differential gm-cell total number of cells on chip are 1/4 that of the single ended cells, used in previous circuit,

whereas differential structure doubles the power consumption. This altogether reduces the total power to half.

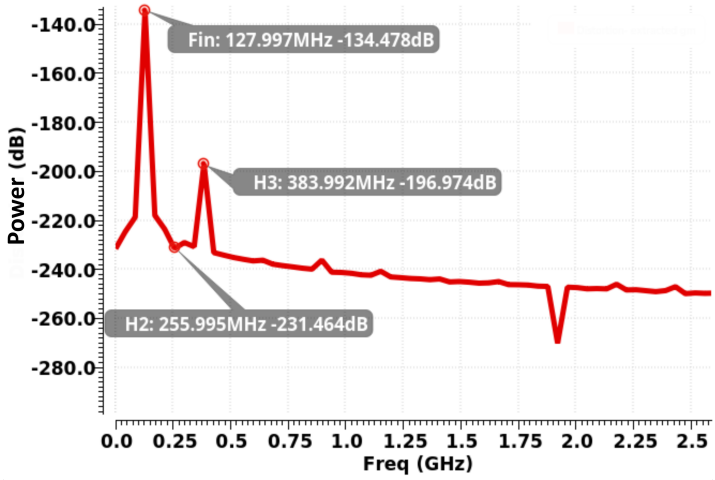


Figure 4.14: Distortion spectrum of the filter

4.4 Achieved Results

It can be summarized that the proposed transconductor in standalone as well as in the filter circuit for a range of 0°-85°C at 1.1 V with ± 10% supply variations for all process corners including mismatch after post-layout simulations, shows

- deviation in g_m of ± 2.5%
- phase deviation of 18° at 270 MHz for the filter
- gain at center frequency (127.8 MHz) of 60 dB with ± 2% deviation for the filter
- bandwidth of 350 kHz with 0.07% deviation for the filter
- SNR of 112 dB and THD of -63 dB for the filter

Chapter 5

Discussion

In previous chapter, post-layout simulation results for the proposed transconductor and its corresponding filter were presented, analyzed and compared with the previous circuit.

In this chapter, we delve into the significance of design choices in the light of relevance of results. It begins with discussing design elements of the proposed constant-transconductance circuit. Then, improvements seen in the proposed transconductor implemented filter have been discussed. It also includes a performance comparison of the filter with that of the prior art to show how this work stands out.

5.1 Transconductance circuit

A circuit for constant transconductance has been realized which shows a deviation of 2.5% under the pvt variations. With the help of constant-g_m biasing methodology, a temperature dependent bias current has been generated such that the transconductor cell biased with it tracks the on-chip resistance, canceling out the temperature dependency. Apart from the basic current-mirror pair setup, the proposed bias circuit makes use of an opamp, placed in a negative feedback loop. This ensures the stability of the bias current against voltage supply variations, by the error correction at virtual ground nodes of the opamp. Moreover, opamp increases the output impedance at the skewed current-mirror pair in the bias circuit eliminating the need for cascode and facilitating large overdrive voltage for the devices. In addition to the stability against temperature and voltage supply variations, the bias circuit also compensates for process variations with the help of digitally programmable binary weighted resistance bank. It is an on-chip resistance trimming, which uses one-time calibration of the filter IC to tune to its desired value.

The proposed g_m-cell assists biasing circuit to ensure there is a constant value of g_m in the complete circuit. The inverter based fully differential architecture of the transconductor cell helps in rejecting the common-mode signals, noise, supply variations as well as canceling non-linearity, balancing g_m deviation with mismatch by sizing IO pair pMOS and nMOS to have same g_m. The architecture uses self-biased pMOS load and self-cascode current

bias, both of which prevents the circuit from supply variations. Former senses the output and provides parallel path to the bias current in each half circuits. thereby balances the difference in two. While, latter uses cascode to increase the output impedance and thereby prevents the impact of supply variations. In addition, the self-biasing pMOS load also acts as common-mode control for the circuit thereby eliminating the need for a separate CMFB circuit. This reduces the complexity of constant-g_m circuit, lesser the circuitry lower the requirement of transistor matching. In addition, it lowers the power consumption of the filter as compared to a generic fully-differential circuit because of reduced number of transistors required.

The proposed transconductance circuit is resilient to coupling issues as well as harbors zero voltage drop, while routing the bias voltage to more than 200 cells on chip. Thus, all transconductor cells throughout the chip will attain constant g_m, biased with the same current.

For perfect replica-biasing in constant-transconductance circuit, it may seem that cascode structure might have been adopted in biasing circuit likewise as that of the transconductor current source. But replica-biasing is still attained in the proposed circuit by using the same node under negative feedback loop in biasing circuit to also bias the current-source in transconductor cell. The self-cascode current source and the nMOS pair of bias are perfectly matched having same size and connected in series-parallel current-mirror arrangement [35]. Moreover, cascode in transconductor is used to achieve stability against voltage supply variation by making use of its increased impedance, whereas in bias circuit it is achieved with the opamp of sufficient loop gain that rejects supply variation with its error correction in negative feedback loop, so it eliminates the requirement of cascoding in bias circuit. However, removing the cascode in biasing circuit provides sufficiently larger overdrive voltage across the skewed pMOS current-mirror pair alongside maintaining all the transistors in saturation region across all variations. On the other hand, since this is a low voltage operation, cascoding in the bias will force the nMOS cascode out of saturation into triode or worst case cut-off for negative supply variation at slow corner. Also there will be body effect coming into consideration rising the threshold voltages with temperature making the cold temperature the worst case, plus disrupting the matching between pMOS and nMOS of bias circuit, increasing the non-linearity.

Resistance bank is employed to incorporate process variations but it is limited by mismatch in the layout. As we can see from Fig. 4.4, the process corner show mismatch variation upto 3% , one of the reason for such a deviation is also due to lack of common-centroid layout of the resistance bank. Although, a common-centroid approach for the unit resistances of the bank could have been adopted but that would have increased the metal routing of the connections made to the switches. Since the bank connects the resistance is series alignment, the metal routing could have been increased to a point it interferes with the total effective resistance employed at any stage and being a metal parasitic resistance, it will be highly dependent on temperature. The worst case routing is between the bit b_0 and b_1 as it is connected to maximum number of resistances and so is the longest. At the same time, since the spread in mismatch is small, the deviation is also coming from the accuracy limited by

available step size and range as we have discussed the trade-off earlier.

5.2 Filter circuit

Filter after using the proposed transconductance circuit shows a well matched frequency response with that of the ideal as shown in Fig. 4.6. However, in phase response, there is a deviation of 18°, which is due to the output capacitance of the transconductor. Although it is within the limitation of the acceptable phase at the output of the filter which is less than 30° from ideal response at frequency 270 MHz. Given, this limitation is specific to the receiver architecture at Philips. An improvement in the layout can be made to reduce the output capacitance.

The performance measurement is done with respect to two parameters primarily , the passband gain and bandwidth of the filter. We know that passband gain of the filter depends heavily on g_m of the transconductor cell. Being the gain element of the filter and available in large number (more than 200), makes the passband gain sensitive to the unit transconductance. The filter needs to ensure a steady high passband gain for its high noise performance and high dynamic range. In this LC based filter architecture, the center frequency of the filter is ensured by the LC tank, so it is very accurately fixed at 127.8 MHz (for protons, 3 T). Moreover the other two, closely lying poles are also tuned by LC tanks in the narrow passband, preventing the response from spreading too much under the influence of variations in field, chip operating conditions etc, thereby the bandwidth variation is always less than 1% atleast. Further, to ensure that bandwidth matches more closely with the ideal, the transconductance stability comes into play.

Parameter	[15]	[18]	[19]	[23]	**Prev.**	**this work**
Implementation level	Chip	Simulation	Simulation	Chip	Post Layout	
CMOS technology	$0.25\mu m$	$0.5\mu m$	130nm	180nm	40nm	
Order of Filter	4^{th} Lowpass	1^{st} Lowpass	2^{nd} Low-pass	3^{rd} Bandpass	6^{th} Bandpass	
Center/Cut-off freq (Hz)	60-350 M	12	22 k	2 M	127.8 M	
g_m dev. with voltage (0.99 V-1.21 V)	N/A (3-3.6V)	N/A (1.1-1.7V)	1.5% (1.2-1.5V)	N/A	15%	2.5%
g_m dev. with temperature (0°C - 85°C)	2% (0°-75°C)	3% (-30°-120°C)	N/A (0°-120°C)	4%	10%	2%
Bandwidth variation	2%	1%	1%	2%	0.5%	0.1%
Pass band gain variation	N/A	N/A	1.27%	N/A	10%	2%

Table 5.1: Performance comparison of constant-g_m circuit

Table 5.1 shows the performance comparison of the proposed transconductor built filter with that of the prior art constant-transconductance circuits. Note that none of these authors have depicted the variations with process corner explicitly in their results, but only stated how the process variations have been compensated in their design. So given that, their results are provided for typical corner only. Also, these filters are g_m-C filters and have $Q < 20$.

[19, 18] show better stability in g_m at 1.2 V supply for a range of 0°-120° C temperature, but they implement low-order lowpass filter of second order and cut-off frequency of few kHz, despite that also, they show a higher variation in bandwidth. Whereas, in our design, the filter shows a variation of merely 0.1% in bandwidth after using the proposed transconductor, which is the least among all. The high frequency operation is undertaken in [15, 23], both of which are chip level measurement results and thus presents the measurement only for their filter and while transconductor performance is provided from simulation results at typical corner with temperature variations only. Among all these circuits, the utility of [15] matches most closely with our case of MRI filter being a high frequency programmable filter but [15] is a low pass filter with a very moderate Q and no passband gain (0 dB), hence it also doesn't provide a fair comparison as well.

None of the cases show pass-band gain variation as they are only employed for nominal filtering with less than 20 dB passband gain. Whereas the passband gain in our case is the most relevant factor to show the stability of the transconductor as this filter has 60 dB passband gain which is a direct function of the transconductance and order of the filter. Due to variability in application-specific critical parameters, filter architectures and design implementation level, it is not a legitimate comparison. The most appropriate performance comparison is with respect to the previous circuit (Prev.) in the table, which shows there is a significant improvement achieved with the proposed design.

Chapter 6

Conclusion

This chapter highlights the conclusion drawn from the study and summarizes the contributions made in this thesis work. Lastly, some future work predictions have been provided.

6.1 Thesis contributions

A stable filter response has been achieved using the proposed transconductor over the variation of process, supply and temperature in the given range. This has been made possible due to the constant-g_m biasing technique complemented by replica biasing, self-biasing and balanced differential inverter in transconductor. The circuit stability depends heavily on matching and ensuring the common-centroid layout has assisted the design in keeping the mismatch variations minimum and a non-dominant factor. The differential circuit in transconductor has provided a capability of rejecting common-mode signals which was absent in the previous design. Along with its self-biasing nature, the transconductance variations has been further controlled, at the same time common-mode level is ensured itself to the mid supply. Taking benefit of the cross-coupled self biased transconductor to realize the negative resistance which also acts as CMFB circuit, eliminates the need to implement it separately. Thus, proposed transconductance circuit has better biasing scheme as well as self-stabilising transconductor cell compared to the previous transconductance circuit. Also, the proposed biasing scheme safeguards all cells against layout artifacts as compared to the previous, which was using fixed-voltage bias, thereby heavily prone to coupling and voltage drop.

With the proposed transconductor, we have been able to meet the performance target set at the beginning, i.e. limiting the transconductance variation to around 2% such that filter response is limited to 2% over a temperature range of 0°-85°C at the voltage supply of 0.99 V-1.21 V across all process corners. Given, that the filter IC is programmable over a range of 64 MHz-128 MHz and results have been analyzed at 127.8 MHz center frequency, 350 kHz bandwidth for a 3T MRI machine. In summary, the overall contributions made in

this study can be listed as below -

1. The proposed transconductance circuit provides a constant-g_m with 2.5% deviation as compared to the previous transconductor which shows a deviation of 15%. It is an improvement of 12% in the g_m stability.

2. The filter implemented with proposed transconductor provides a passband gain of 60 dB $\pm$ 2% as compared to the previous filter circuit which has the deviation of more than 10%. It is an improvement of more than 8%.

3. The filter bandwidth also becomes more stable with the proposed transconductor and shows a deviation of 0.07% as compared to 0.5% deviation in previous filter circuit.

4. The SNR and dynamic range of the filter with proposed transconductor are 112 dB, which is equivalent to that of the previous filter circuit, but distortion has reduced to -63 dB from -42 dB in the previous filter circuit.

5. The power consumption of the filter IC has reduced to 0.8 mW from 1.75 mW in the previous circuit.

6.2 Future work

The proposed constant-transconductance circuit shows very high stability with supply and temperature variation of about 1% as shown in Fig. 4.1. It is the variation with process corners that there is total deviation of 2.5% and this is also after the implementation of on-chip resistance bank. The accuracy of this circuit heavily depends on the precision of the resistance whereas by using the poly resistance, the resistance has become process dependent and thereby compensating the process variation by resistance bank. It has already been observed that using a bank is an area-consuming trade-off to accuracy and prone to mismatch which degrades the stability of the circuit achieved through the design otherwise. Another possible implementation of the on-chip resistor is using switched capacitor resistor (SCR). This has been implemented in [17, 19, 23]. It uses an on-chip precise clock frequency (f_{clk}) to switch a small-flying cap (C_s) between the source of the skewed transistor and supply voltage, which establishes an equivalent resistor of $(f_{clk}C_s)^{-1}$. Although, bias circuits operate at low-frequency relatively but, here supply of 1.1V is generated using on-chip power converter, switching at 15 MHz. This requires the SCR to switch at a frequency of the order of 100's of MHz which is challenging and prone to noise. Also, the frequency of the SCR has to take into consideration that ripple falls outside the passband of the filter which pushes it further to more than 150 MHz. As in case of [19], SCR has a switching frequency of 90 kHz for cut-off frequency of the filter at 22 kHz.

Bibliography

[1] J. Anders and G. Boero. "A low-noise CMOS receiver frontend for MRI". In: *2008 IEEE Biomedical Circuits and Systems Conference*. 2008, pp. 165–168.

[2] Andrew Murphy and Dr Jeremy Jones. "Larmor frequency". In: *Radiopaedia* (). URL: https://radiopaedia.org/articles/larmor-frequency#:~:text=The%20Larmor%20frequency%20and%20equation,Larmor%20(1857-1942).&text=The%20Larmor%20or%20precessional%20frequency,around%20the%20external%20magnetic%20field..

[3] Bernhard Gruber et al. "RF coils: A practical guide for nonphysicists". In: *Journal of Magnetic Resonance Imaging* 48.3 (2018), pp. 590–604. DOI: 10.1002/jmri.26187.

[4] Kathryn Mary Broadhouse. "The Physics of MRI and How We Use It to Reveal the Mysteries of the Mind". In: *Frontiers for Young Minds* 7 (2019). DOI: 10.3389/frym.2019.00023.

[5] Ham K et al. Possanzini C Harvey PR. URL: https://www.usa.philips.com/healthcare/education-resources/technologies/mri/dstream.

[6] Scott W. Atlas. *Magnetic Resonance Imaging of the Brain and Spine*. Vol. 1. Lippincott Williams & Wilkins, 2009.

[7] 2013. URL: https://www.analog.com/media/cn/technical-documentation/apm-pdf/adi-mri-solution_en.pdf.

[8] Olaf Dietrich et al. "Measurement of signal-to-noise ratios in MR images: Influence of multichannel coils, parallel imaging, and reconstruction filters". In: *Journal of Magnetic Resonance Imaging* 26.2 (2007), pp. 375–385. DOI: 10.1002/jmri.20969.

[9] Texas Instruments(TI). 2012.

[10] Umesh Jayamohan. *Not Your Grandfather's ADC: RF Sampling ADCs Offer Advantages in Systems Design*. 2015. URL: https://www.analog.com/en/technical-articles/rf-sampling-adc-offer-advantages-in-systems-design.html.

[11] Bob Dobkin and Jim Williams. *Analog Circuit Design: Volume 2: Immersion in the Black Art of Analog Design*. Newnes, 2013.

[12] Robert Keller. In: *Planet Analog* (Jan. 2015). URL: https://www.planetanalog.com/signal-chain-basics-part-97-faster-is-better-gsps-adcs-enable-wide-bandwidth-rf-digitizers/#.

[13] URL: https://www.nhs.uk/conditions/mri-scan/what-happens/#:~:text=A%20magnetic%20resonance%20imaging%20(MRI,number%20of%20images%20being%20taken..

[14] IEC 60601-2-33. *Particular Requirements for The Basic Safety and Essential Performance of Magnetic Resonance Equipment for Medical Diagnosis*. Tech. rep. Edition 3, Amendment 2. Geneva, Switzerland: International Electrotechnical Commission(IEC), 2015.

[15] S. Pavan, Y. P. Tsividis, and K. Nagaraj. "Widely programmable high-frequency continuous-time filters in digital CMOS technology". In: *IEEE Journal of Solid-State Circuits* 35.4 (2000), pp. 503–511.

[16] A. McLaren and K. Martin. "Generation of accurate on-chip time constants and stable transconductances". In: *IEEE Journal of Solid-State Circuits* 36.4 (2001), pp. 691–695.

[17] N. Talebbeydokhti et al. "Constant transconductance bias circuit with an on-chip resistor". In: *2006 IEEE International Symposium on Circuits and Systems*. 2006, 4 pp.–2860.

[18] V. Agarwal and S. Sonkusale. "A PVT independent subthreshold constant-Gm stage for very low frequency applications". In: *2008 IEEE International Symposium on Circuits and Systems*. 2008, pp. 2909–2912.

[19] N. Mirchandani and A. Shrivastava. "High Stability Gain Structure and Filter Realization with less than 50 ppm/° C Temperature Variation with Ultra-low Power Consumption using Switched-capacitor and Sub-threshold Biasing". In: *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2018, pp. 1–5.

[20] P. Andreani and S. Mattisson. "On the use of Nauta's transconductor in low-frequency CMOS g/sub m/-C bandpass filters". In: *IEEE Journal of Solid-State Circuits*. Vol. 37. 2. 2002, pp. 114–124.

[21] C. Chu and Y. Wang. "A PVT-Independent Constant- G_m Bias Technique Based on Analog Computation". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 61.10 (2014), pp. 768–772.

[22] Jiwei Chen and Bingxue Shi. "Novel constant transconductance references and the comparisons with the traditional approach". In: *Southwest Symposium on Mixed-Signal Design, 2003.* 2003, pp. 104–107.

[23] R. J. E. Jansen, J. Haanstra, and D. Sillars. "Complementary Constant- g_m Biasing of Nauta-Transconductors in Low-Power g_m –C Filters to ±2% Accuracy Over Temperature". In: *IEEE Journal of Solid-State Circuits* 48.7 (2013), pp. 1585–1594.

[24] R. Harjani and R. K. Palani. "Design of PVT tolerant inverter based circuits for low supply voltages". In: *2015 IEEE Custom Integrated Circuits Conference (CICC)*. 2015, pp. 1–8.

[25] Johan Huijsing. "Operational Amplifiers". In: second. Springer, 2011. Chap. 4.

[26] M. Bazes. "Two novel fully complementary self-biased CMOS differential amplifiers". In: *IEEE Journal of Solid-State Circuits* 26.2 (1991), pp. 165–168.

[27] James W. Nilsson and Susan Riedel. "Electric Circuits". In: ninth. One Lake Street, Upper Saddle River, New Jersey, 07458: Pearson Education, Inc., publishing as Prentice Hall, 2011. Chap. 8.

[28] Adel S.Sedra and Kennel C. Smith. "Microelectronic Circuits". In: fifth. Oxford University Press, 2004. Chap. 12.

[29] Massoud Tohidian, I. Madadi, and Robert Staszewski. "Analysis and Design of a High-Order Discrete-Time Passive IIR Low-Pass Filter". In: *IEEE Journal of Solid-State Circuits* 49 (Nov. 2014), pp. 2575–2587. DOI: 10.1109/JSSC.2014.2359656.

[30] Unai Alvarado. *Low power rf circuit design in standard cmos technology*. Springer, 2013.

[31] *Gyromagnetic ratio (γ)*. URL: http://mriquestions.com/gyromagnetic-ratio-gamma.html.

[32] Tony Chan Carusone, David A. Johns, and Kenneth W. Martin. "Analog Integrated Circuit Design". In: second. John Wiley & Sons, Inc., 2012. Chap. 1,7.

[33] S. S. Rajput and S. S. Jamuar. "Low voltage analog circuit design techniques". In: *IEEE Circuits and Systems Magazine* 2.1 (2002), pp. 24–42.

[34] Willy Sansen. "Opamps, Gm-Blocks or Inverters?" In: *Efficient Sensor Interfaces, Advanced Amplifiers and Low Power RF Systems: Advances in Analog Circuit Design 2015*. Ed. by Kofi A.A. Makinwa, Andrea Baschirotto, and Pieter Harpe. Cham: Springer International Publishing, 2016, pp. 125–138. DOI: 10.1007/978-3-319-21185-5_7. URL: https://doi.org/10.1007/978-3-319-21185-5_7.

[35] R. Fiorelli, A. Arnaud, and C. Galup-Montoro. "Series-parallel association of transistors for the reduction of random offset in non-unity gain current mirrors". In: *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*. Vol. 1. 2004, pp. I–881.

[36] Mr D Grainger. *Safety Guidelines for Magnetic Resonance Imaging Equipment in Clinical Use*. Tech. rep. Medicines and Healthcare Products Regulatory Agency(MHRA), 2014.

Appendix A

Filter system modelling

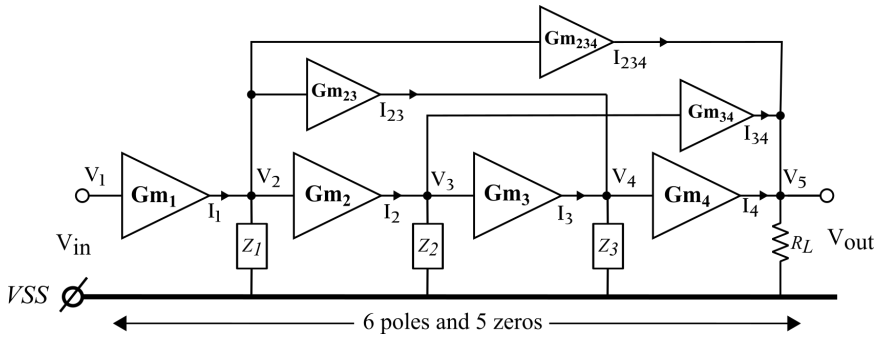


Figure A.1: Filter Architecture

Transfer function from PZ- MATLAB The poles and zeros information is dependent on the RF receiver architecture and the Larmor frequency, which is 127.8 MHz for 3T machine, and are given in Table .A.1.

Pole (MHz)	Zero (MHz)	Q_{pole}
-0.160 ± j 127.800	-5.578 ± j 129.656	400
-0.159 ± j 127.200	-3.003 ± j 125.816	400
-0.160 ± j 128.400	-150.900 & 0(origin)	400

Table A.1: Poles and zeros of MRI filter

Transfer function corresponding to the poles and zeros can be written as

$$H(s) = \frac{(s-z_1)(s-z_2)(s-z_3)(s-z_4)(s-z_5)(s-z_6)}{(s-p_1)(s-p_2)(s-p_3)(s-p_4)(s-p_5)(s-p_6)} \tag{A.1}$$

Nodal Analysis

In the filter architecture, Gm represents the transconductance block, while Z represents the resonator block and denotes its respective impedance. The nodal equations can be written as follows.

$$\begin{aligned} I_1 &= V_1 G_1 & V_2 &= I_1 Z_1 \\ I_2 &= V_2 G_2 & V_3 &= I_2 Z_2 \\ I_3 &= V_3 G_3 & V_4 &= (I_{23} + I_3) Z_3 \\ I_4 &= V_4 G_4 & V_5 &= (I_4 + I_{34} + I_{234}) R \end{aligned} \tag{A.2}$$

The transfer function constructed from nodal equations, $H(s) = V_{out}/V_{in} = V5/V1$ can be given as follows.

$$\begin{aligned} H(s) =& R_L\{(Gm_1 Z_1(s) Gm_2 Z_2(s) Gm_3 Z_3(s) Gm_4 + Gm_1 Z_1(s) Gm_4 Z_3(s) Gm_{23} \\ &+ Gm_1 Z_1(s) Gm_2 Z_2(s) Gm_{34} + Gm_1 Z_1(s) Gm_{234}\} \end{aligned} \tag{A.3}$$

Given, that Z is the impedance which is given by

$$Z(s) = \frac{1}{RC}\left(\frac{s}{s^2 + \frac{s}{RC} + \frac{1}{LC}}\right) \tag{A.4}$$

where components R, L, C can be calculated from pole values. Given, Q (400) $= R\sqrt{C/L}$ and $\omega_0 = \sqrt{1/LC}$.

The denominator of the transfer function is given by the product of the poles which can be written in the form of denominator of the impedance of three resonator blocks

$$Dr(s) = \prod_1^3 \left(s^2 + \frac{s}{RC_i} + \frac{1}{L_i C_i}\right) \tag{A.5}$$

where R_i, L_i and C_i are given in Table A.2.

Pole (MHz)	Resonator	Capacitance (pF)	Resistance (kΩ)	Inductor (nH)
-0.160 ± j 127.800	Z_1	31.02	16	50
-0.159 ± j 127.200	Z_2	31.31	16	50
-0.160 ± j 128.400	Z_3	30.73	16	50

Table A.2: Component values (RLC) of three resonators (Z_{1-3}) corresponding to their complex- conjugate poles

Solving the two Eq. A.1 and A.3 gives the value of transconductance per block, Gm given in Table A.3.

$$H(s) = Gain\frac{Nr(s)}{Dr(s)} = \frac{V_{out}}{V_{in}} \tag{A.6}$$

Gm block	mA/V (mS)	Gm block	mA/V (mS)
Gm_1	2.5	Gm_{23}	-1.7
Gm_2	1.25	Gm_{34}	-0.02
Gm_3	1.25	Gm_{234}	0.34
Gm_4	0.625		

Table A.3: Transconductance per Gm block in ideal filter

For a unit transconductance of 31.25 μS. The scale factor of filter, Fig. A.1 can be calculated as in Table A.4.

Gm block	No. of g_m-cell	Gm block	No. of g_m-cell
$N(Gm_1)$	80	$N(Gm_{23})$	54
$N(Gm_2)$	40	$N(Gm_{34})$	1
$N(Gm_3)$	40	$N(Gm_{234})$	11
$N(Gm_4)$	20		

Table A.4: Scale factor of transconductor cells in ideal filter

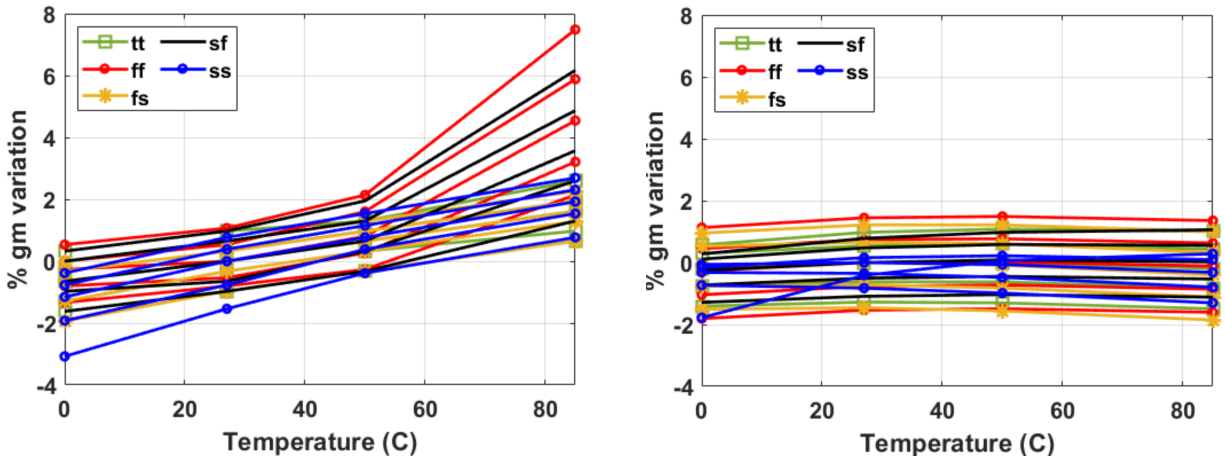
Appendix B

More results

Schematic PVT results

1. *R_B Normalized :* R_B is the poly resistance of fixed length and the simulation results have been normalized to the typical corner for all five process corners as given in Fig. B.1. The plot shows results with temperature variation on x-axis and voltage variation is depicted with multiple curves in same colour.

The plot shows the previous transconductor has larger g_m deviation upto 8% at high temperatures while the proposed transconductor has relatively small g_m deviation, within $\pm$ 2% for all PVT variations.



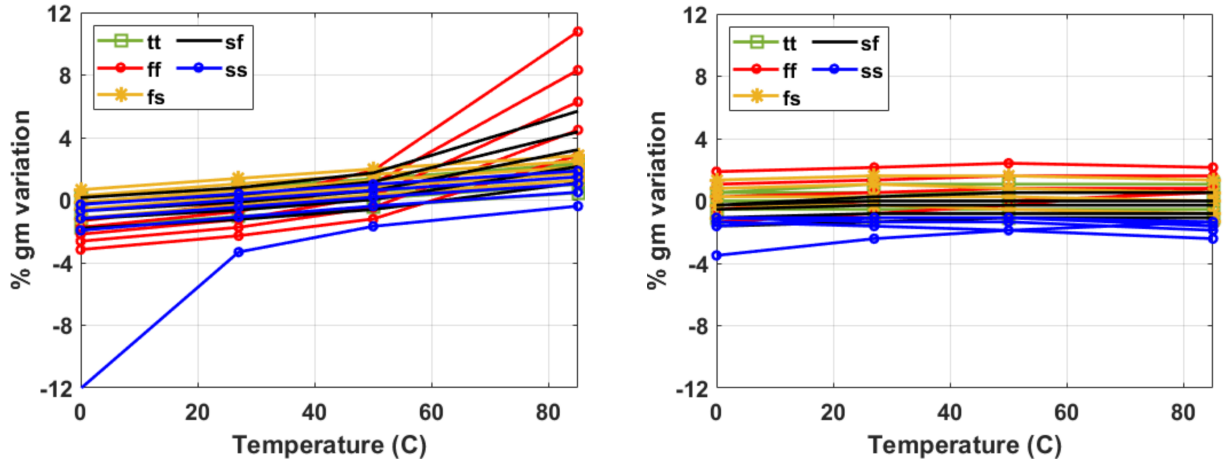
(a) Previous transconductor

(b) Proposed transconductor

Figure B.1: Schematic simulation with normalized R_B. g_m variation with PVT

2. *R_B as R_{bank} :* The simulation results of schematic view with R_B as R_{bank}, the schematic version of the final design, are shown in Fig. B.2. The results are represented same as above.

The plot shows the deviation in g_m for the previous transconductor is about $\pm$ 12% while for the proposed transconductor, it is within $\pm$2% except the worst case of 0°C and slow corner (ss) which shows a deviation of -3.6%. The plots are quite close to the post-layout simulation results. Although, a difference can be seen between ideal resistance and digitally calibrated resistance bank. It is because of the reason that ideally the polysilicon resistance doesn't follow a linear trend with process variations, whereas with binary-weighted resistance bank we have formulated a linear approximation. Either we can go for thermometer code rather than binary code but that will cost a lot of area. We understand that using a bank is not a very accurate solution to combat the process dependency of the resistance bank.



(a) Previous transconductor

(b) Proposed transconductor

Figure B.2: Schematic simulation with R_B as R_{bank}. g_m variation with PVT