EXCIMER LASER ANNEALING FOR ULTRASHALLOW JUNCTIONS AND CONTACTS

VIKTOR GONDA

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PROEFSCHRIFT

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Dit proefschrift is goedgekeurd door de promotor:

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Contents

Chapter 1

Introduction

Miniaturization has driven electronic devices from micro to nano scale in order to increase speed and functionality of the circuits. In planar technologies, lateral downscaling is required to be able to place more electronic components on the silicon surface. This leads, on one hand, to a reduction of the size of contacts to the silicon and, if no special measures are taken, the contact resistances will increase accordingly. One option for decreasing the contact resistivity is to increase the doping of the contact surface. On the other hand, due to the increased proximity of doped regions, such as for the source and drain of a metal-oxide-semiconductor field-effect transistor (MOSFET) where short channel effects become detrimental, there is also a drive towards vertical downscaling. For this, aggressively scaled highly-doped, ultrashallow junctions are needed. According to the international technology roadmap for semiconductors (ITRS) [itr, 2007], beyond 2009, ultrashallow source-drain extensions should scale below 10 nm, with lateral abruptness below 2 nm/decade. Full-melt laser annealing in combination with low energy implants, which is the topic of this thesis, is one of the few techniques that can fulfil these requirements.

The straightforward route that the industry took to downscale junctions was to decrease the implantation energies and the thermal budget for the annealing. This route was eventually complicated by fast diffusion effects related to non-equilibrium diffusion phenomena, and this has led to the development of high-temperature short-time annealing in combination with innovative defect engineering techniques.

Laser annealing for the doping of silicon was first studied in the 1970's [Lojek, 1999]. However, due to issues such as junction leakage, reproducibility and IC-processing compatibility, that were related to the high implantation energies and laser equipment limitations of that time, this technique was all but forgotten by the mid 1980's. A

revival of the research was launched in 1999 when the technique appeared on the ITRS roadmap and was recognized as being naturally capable of fabricating the ultrashallow junctions necessary for future CMOS generations. Nevertheless, integration proved to be difficult and unlike most other processing techniques, the optical properties of the wafer became a vital parameter. There were two other techniques that at that time had just reached some degree of maturity and also needed to take the optical properties of the wafers into consideration: rapid thermal annealing (RTA) methods such as flash lamp annealing [Lerch et al., 2007] and UV lasering for (re-)crystallisation had found its ways into the fabrication of thin-film displays [Kagan and Andry, 2003]. This latter application demonstrated another useful property of laser annealing: it is a surface annealing technique, i.e., only the surface layer is affected by the heat, due to the low thermal budget, the small absorption depth and the short timescales, the temperature quickly drops towards the bulk of the wafer. This makes the technique attractive for applications where thermal limitations apply such as for the thin-film panels where silicon is deposited and recrystallized on glass that must be processed at temperatures below about 500 °C.

The recent work in the literature on the laser-annealing of implanted junctions has to a great extent been devoted to engineering the junction depth and sheet resistance values that make the method attractive for source/drain fabrication in future CMOS generations [Surdeanu et al., 2002, Whelan et al., 2003]. Yet other studies have focused on the actual integration in CMOS [Yu et al., 1999, Wong et al., 2005], which still remains very challenging. In any case, the integration of the laser annealing is complicated by the optical nature of the method, which results in a strong pattern sensitivity, by the localized nature of the anneal, which gives high thermal gradients, and by the low thermal budget available for annealing the implanted dopants. The latter means that not all defects are annealed and non-annealed defects must either be eliminated by additional processing or be tolerated in the specific device structure being fabricated, which may entail customized device optimization.

Rather than having a flat panel or CMOS focus, the work in this thesis has been performed in the context of the non-MOS high-frequency silicon device integration research being performed at DIMES. In general, in high-frequency devices the demand for thin, abrupt and accurately tailored doping profiles has also put focus on low-temperature processing techniques. Moreover, the demand for low parasitic resistance and capacitance in both devices and circuits has lead to the development of aggressive isolation schemes. At DIMES the search for solutions answering to these demands has crystallized in the development of an in-house silicon-on-glass technology in which special bipolar junction transistors, heterojunction SiGe bipolar transistors and high-linearity varactor circuits have been successfully realized. In all these implementations, the use of laser annealing to integrate ultrashallow junctions or low-

Table 1.1: Typical annealing times, temperatures, and heating rates for different types of thermal annealing techniques.

Anneal type	Furnace	Soak	Spike	Flash	Laser
Timescale	$\times$10 min	$\times$1 min	$\times$1 sec	$\times$1 msec	$\times$1 μsec
Temperature (°C)	900	1000	1100	1200	$>$1300
Heating rate (°C/sec)	$<$0.1	1	10	100	10^6

ohmic contacts has played a crucial role. In particular, the thermal restrictions after silicon substrate transfer by gluing to glass are severe: no thermal treatments above 300 °C can be tolerated. In the SiGe devices for the preservation of the doping profiles, it is attractive to keep temperatures below 700 °C after SiGe epitaxy and below 500 °C after implanting dopants.

In this thesis, the integration of high-power excimer laser annealing to activate low-energy implanted regions is investigated with the goal of fabricating ideal junctions and low-ohmic contacts in high-frequency silicon-on-glass devices. The results of the investigation include several generally applicable rules for optimizing the fabrication and integration sequence to accommodate the laser anneal step. In particular, the integration of a suitable reflective laser masking layer to protect regions that should not be annealed is challenging since the desire for minimum device dimensions dictates the use of self-aligned techniques. Moreover, obtaining an ideal annealing of the perimeter of a junction that is self-aligned to the contact window becomes the most critical issue.

1.1 Overview of annealing methods

For the different types of thermal annealing techniques, the processing times can range from hours to microseconds as is shown in Table 1.1. A high-temperature thermal step will induce diffusion and activation of the dopants as well as movement and repair of defects. With respect to shallow junctions, where the requirements are shallowness and abruptness, high activation, and low leakage, the preference is to have low diffusion, high levels of activation and a high amount of defect repair.

1.1.1 Evolution of annealing for implanted dopants

Early laser annealing

In the late 1960's laser–semiconductor interaction was first studied in Russian groups. They demonstrated a laser-annealed diode and the re-crystallization of a deposited amorphous silicon layer [Kutolin and Kompanec, 1969]. In the mid 1970's the use of laser annealing of implanted damage was researched [Pilipovic, 1975]. In the early 1980's the high research interest resulted in extensive understanding and modelling of the fundamental mechanisms governing the laser annealing process: the melt and solidification processes including the associated impurity diffusion and segregation [Poate and Mayer, 1982, Thompson et al., 1984]. Excimer lasers were applied for the first time for device fabrication, and laser doping in the gas phase was also investigated [Lojek, 1999]. Despite a quite significant and valuable research effort, device integration proved to be too complicated: in the laser–Si interaction the optical properties of Si become important and the process is very different from the commonly applied furnace annealing. Therefore, focus was shifted to extending the well-known thermal annealing techniques that used tens-of-minute anneal times into the time-frame of what was then called rapid thermal annealing (RTA) and aimed at minute long anneals.

Rapid thermal annealing and TED

If only thermal equilibrium diffusion effects are assumed, deep diffusion of dopants can be avoided for shallow-junction formation either by using high temperatures with short anneal times or by using low temperatures with longer anneal times to nevertheless eliminate the influence of defects. However, in the latter, much deeper diffusion than expected was observed especially in the case of implanted boron [Eaglesham et al., 1994]. This was found to be due to the long defect dissolution times at low temperatures and a non-equilibrium diffusion induced by dopant interaction with mobile defects. This effect, which is called transient enhanced diffusion (TED) [Stolk et al., 1997] has driven research towards RTA with short times at high temperatures. In the development of the annealing equipment the major effort was also put into tools for realizing shorter annealing times.

Millisecond anneal and co-implants

At present the state of the art in manufacturing is millisecond annealing [Timans et al., 2006]. In order to slow down the demands for decreasing the thermal budget, defect engineering methods have also been developed. These include methods where in addition to the dopant an additional non-active species such as F or C is co-implanted

to retard diffusion, and methods using vacancy engineering to retard enhanced diffusion [Claverie et al., 2008]. As the thermal budget decreases and anneal times are shortened, flash lamps are often used as the heating elements. This has meant that the optical properties of the substrates to be annealed have also started to play a role in this case and pattern sensitivity is also an issue. To decrease the junction depth beyond what has been possible with thermal methods and shallow implants, alternative methods for doping are being researched.

1.1.2 Laser doping

In ultrashallow junction technology, techniques to substitute low-energy ion-implantation with something less damaging have received an increasing amount of interest. All in all, low-energy implantations together with low thermal budget anneals suffer from reduced activation efficiency, channelling, transient enhanced diffusion and tradeoffs between residual damage and thermal budget.

Since a thermal step is unavoidable in the doping process, a laser thermal processing step is attractive due to the fact that the very high temperatures can be achieved with an extremely low thermal budget while only affecting the surface of the wafers. In laser doping, dopants can be introduced by a spin-on technique [Lo et al., 1996b], or, with a much better dose control, by gas-immersion laser doping [Carey et al., 1985].

Dose control is also excellent in the atomic-layer-doping technique, where an adsorbed dopant monolayer can be deposited by using CVD. These layers can then be capped by oxides so that dose loss during a subsequent thermal drive-in thermal step can be avoided. [Song et al., 1999] demonstrated arsenic and phosphorous drive-in, while [Kim et al., 2000a] demonstrated it for boron. Such junctions have been integrated in MOS transistors on SOI [Koh et al., 2002], and in devices with SiGe source/drain regions [Jung et al., 2002]. [Popadic et al., 2007] analyzed diffusion from a monolayer for arsenic and phosphorous as a function of the annealing temperature.

Nevertheless, these alternative doping techniques do not have the versatility with respect to integration that implantation has. This is the main reason that most of the work in this thesis is focused on the laser annealing of implantations. While the device structures fabricated in the silicon-on-glass technology have allowed the use of full-melt annealing, considerable research has been reported by others on non-melt and partial-melt techniques that aim to enhance the compatibility of the laser anneal step with CMOS process flows.

1.2 Ultrashallow junctions by laser-anneal-only

In most of the work reported in the literature on the formation of ultrashallow junctions with laser annealing, thermal processing steps after the laser anneal have been included in the total process flow [Chong et al., 2002]. This has mainly been because the laser anneal alone did not remove enough implantation damage at the junction to be able to achieve low-leakage diode characteristics. It has been attempted to remove this damage by thermal processing at temperatures as low as 600 °C. Moreover, the post-laser process flow often demands that the laser-annealed doping profile should tolerate some degree of thermal processing. The results of the laser-annealing are in the most of these cases far from optimal in part due to TED effects.

In contrast to this work, at DIMES the research focus has been on the laser-anneal-only approach. At the time when this thesis work started, it had just been demonstrated that near-ideal diodes with excellent ideality factors of $n \approx 1.1$ could be fabricated by activating implanted dopants purely by excimer laser annealing [Nanver et al., 2003, Gonda et al., 2005a]. To completely avoid post-laser thermal processing steps, a straightforward process flow was implemented where dopants were implanted directly in a contact window that was etched through a reflective layer stack of aluminium on a thermal oxide surface isolation. The laser annealing is then performed just before the contact metallization. This basic scheme proved very attractive for the silicon-on-glass applications that were under development at DIMES and these are described in the next section.

The laser-anneal-only approach is not easily made compatible with conventional CMOS. However, it may be very attractive for advanced CMOS that aims at high-k-dielectric metal-gate stacks. A first demonstration of this was given by [Baek et al., 2004] who integrated laser-annealed source/drain regions in metal-gate transistors. In this case the gate metal functions as the reflective mask. A similar device is now under development at DIMES in the framework of the FP6 project *High-frequency disposable SiGe dot FET*. The device has an SiO_2-Al_2O_3-Al gate stack that masks the laser annealing of arsenic implanted source/drain regions.

1.3 Laser annealing in silicon-on-glass technology

Since 1999 high-frequency silicon-on-glass IC-processes have been under development at DIMES. In the original SOG substrate-transfer technology that was pioneered by Philips [Dekker et al., 1997] the processing after transfer to glass was limited to non-critical large-area patterning and contacting of the back-wafer (backside of the wafer). The DIMES version of SOG processing is specifically referred to as back-

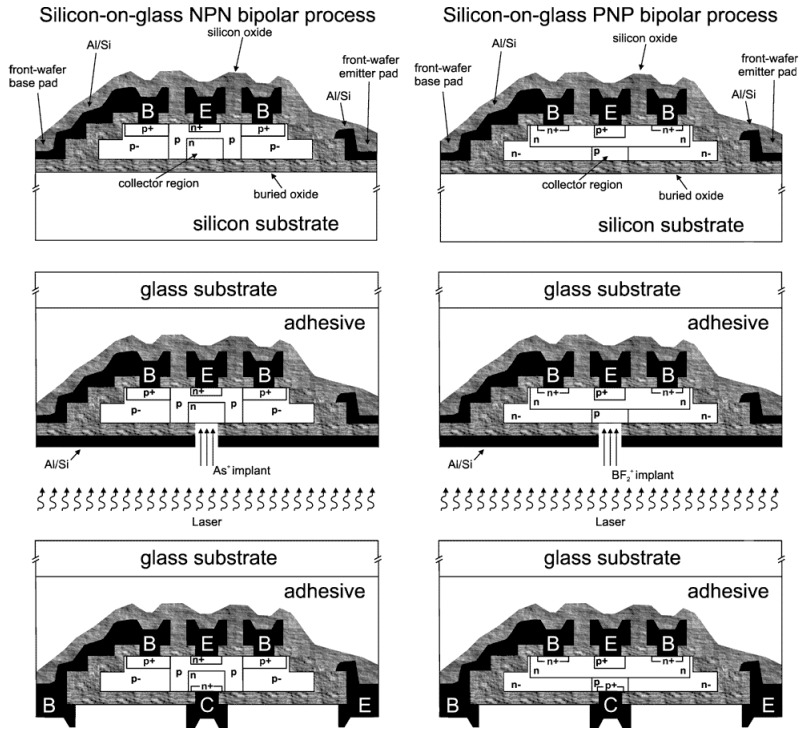

Figure 1.1: Schematic process flow of the DIMES silicon-on-glass implanted and laser annealed back-wafer-contacted complementary bipolar technology [Lorito et al., 2006].

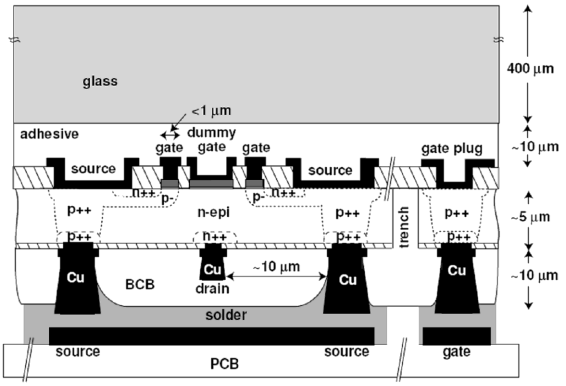

Figure 1.2: Schematic cross section of the surface mounted silicon-on-glass VDMOS-FET with p^{++} and n^{++} implanted and laser annealed regions [Nenadovic et al., 2004].

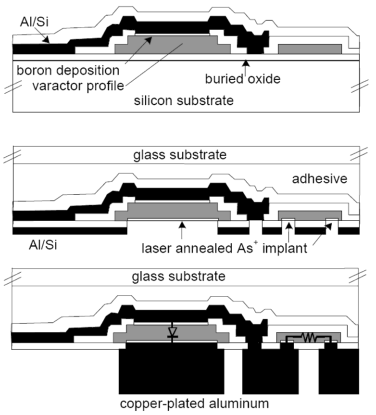

Figure 1.3: Schematic process flow for the integration of SOG varactor diodes and high-ohmic resistors with a laser annealed As^{+} implant [Buisman et al., 2005].

wafer-contacted SOG technology [Nanver et al., 2008c] because it distinguishes itself from earlier versions by the implementation of minimum dimension waferstepper patterning on both the front-wafer (front side of the wafer) and back-wafer and the use of laser annealing to produce junctions and low-ohmic contacts on the back-wafer. The transfer to glass is performed by gluing with an acrylic adhesive that does not tolerate temperatures above 300 °C. Therefore laser annealing is one of the techniques that can be used to activate implanted dopants on the back-wafer. A successful implementation of this technique was already demonstrated in 1999 for collector-contacting of SOG NPNs [Nanver et al., 1999] and later a complementary bipolar process with similar vertical PNPs was also demonstrated [Lorito et al., 2006]. A schematic of the basic process flow is shown in Fig. 1.1. In the course of the work it became clear that under certain circumstances the implants in the back-wafer could have a detrimental effect on the parts of the device regions already processed during the front-wafer processing. An investigation of these effects and their dependence on the implant and laser-anneal conditions has been performed in the context of this thesis [Gonda et al., 2006b, Gonda et al., 2006a] and are treated in Chapters 4 and 5. For the bipolar SOG devices a new type of collector contacting was developed that avoids the use of implantations in the back-wafer: the ohmic collector contact was replaced by a Schottky contact [Lorito et al., 2006] and this has proven to have advantages for the performance of the transistors for many analog applications.

In another SOG device, the vertically diffused MOS (VDMOS), low-ohmic contacts on the back-wafer to the p-type source and n-type drain are made with laser annealed implants. This solution could be implemented without any compromises because the other device regions containing junctions are more than 3 μm away [Nenadovic et al., 2004]. This can be seen in Fig. 1.2.

However, in yet another application, the high-linearity SOG varactor [Buisman et al., 2005], back-wafer contacting with very low series resistance is vital for the device performance. This is easily achieved with implantation and laser annealing as shown in Fig. 1.3. However, in this application the residual implantation damage is positioned so that it can reduce the varactor diode breakdown voltage, which is a crucial parameter for the overall performance. Therefore it becomes important to find ways of minimizing the amount of the defects created around the contact.

The ultimate goal of the bipolar SOG work has been to integrate a SiGe HBT with no TED effects after formation of the epitaxially-grown boron-doped strained-SiGe base. To achieve this, the emitter and base contact should be fabricated without combining implantations with thermal anneals. Although this would appear to be quite doable by replacing the thermal anneal by laser annealing in a process as in [Nanver et al., 2003], a straightforward implementation, even for micron size contacts, is complicated by the fact that the limited thermal budget after SiGe epitaxy also does

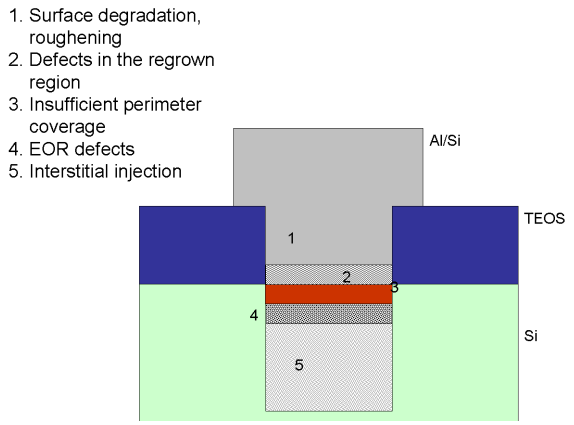

Figure 1.4: Main issues related to laser annealing of implanted junctions.

not allow the growth of thick thermal oxides like those used in that publication. On the contrary, the isolation layer is effectively composed of less ideal materials deposited by chemical-vapor-deposition (CVD) methods. With respect to these materials the thermal oxide has the advantage of a very uniform composition that guarantees a uniform etching and in addition the etch rate in HF that is used to remove native oxide is low. The latter has consequences for the dip etching of the contact window before metallization. Excessive etching of the contact perimeter during this step can lead to diode perimeter leakage because the laser annealed diodes are very critically aligned to the original contact window.

Despite the isolation issues, experimental bulk devices with laser-anneal-only emitter and base contact fabrication that give a first proof-of-concept were realized [Lorito et al., 2008]. These devices have an aggressively downscaled emitter-base doping profile with an emitter depth of about 10 nm but the current gain and high-frequency performance are shown to be good. In Chapter 5 these devices are analyzed with respect to the influence of residual damage in the base region as a result of implantation and laser annealing.

1.4 Outline of the thesis

To summarize, as shown in Fig. 1.4, the main issues related to laser annealing of implanted junctions are residual implantation induced damage, non-ideality of diodes related to bulk and perimeter imperfections, pattern dependence and non-uniformities. All of these issues are treated in this thesis, with the main focus placed on establishing process flows that enable high-frequency device fabrication in the back-wafer-contacted SOG technology.

The following chapter introduces the tools with which the work in the thesis has been performed. In first instance the high-power excimer laser annealing systems are described followed by the methods used to model the basic thermal behavior during laser annealing. A short overview of the applied material analysis techniques is given, while the electrical characterizations techniques, which have been the most important means of evaluating the quality of the laser anneal junctions and contacts, are treated in detail. These include the measurement of test structures for determining contact resistance and the I–V and C–V characteristics of diodes, bipolar junction transistors and junction field-effect transistors.

In Chapter 3, the basic process flow is described for integrating the laser annealing of an implanted region with the goal of obtaining a near-ideal ultrashallow junction. The results of a series of systematic experiments where the influence of individual process steps is evaluated make it possible to optimize the process flow in different device integration situations.

Both the implantation and the subsequent laser anneal can have an effect on the doping in regions in the vicinity of the implant. Chapter 4 concentrates on the effects of residual defects injected into the substrate and not annealed by the laser, which can result in increased junction leakage and deactivation of dopants. It is shown that the severity of these effects can be reduced by modifying the implantation parameters. In the region just below the implant, the heat pulse sent into the substrate from the laser melt region can be instrumental in reactivating dopants that were deactivated by the implantation. This is experimentally demonstrated in Chapter 5 where the laser annealed junction functions as emitter in SiGe HBT transistors. In these devices the SiGe base is as close as 50 nm to the emitter.

In Chapter 6 some initial experiments are described for replacing arsenic implants with CVD deposited monolayer of arsenic. The high deposition temperature complicates the fabrication of the laser reflective masking layer but nevertheless encouraging results were achieved.

In the last year of this thesis work, double laser annealing with short pulse offsets became available [Gonda et al., 2007a, Gonda et al., 2007b]. This new technique offers a novel method of extending the effective laser heating time and it is shown in Chapter

7 to be a useful extra parameter for optimizing the thermal budget of the overall anneal. In Chapter 8 the conclusions of this thesis work are given along with recommendations for future work.

Chapter 2

Laser annealing methods and evaluation techniques

In this chapter the infrastructure for the laser annealing experiments is described. First the laser systems are introduced, followed by the description of the laser annealing mechanism and the thermal modelling for laser annealing. Finally, the test structures for material analysis and the electrical device structures are described together with the electrical characterization methods.

2.1 Excimer laser annealing

2.1.1 Excimer laser systems

There were two laser systems used in this work: a single laser system by XMR was used at DIMES until the end of 2005, and a custom built double excimer laser setup by Exitech that replaced the XMR in early 2006.

Single laser system

A schematic of the XMR laser setup is shown in Fig. 2.1. The XMR 5100 laser source uses Xe and Cl_2 active gases and emits at a wavelength of 308 nm, with a pulse duration of 60 ns full width at half maximum (FWHM). The output energy is measured by a removable energy meter. The fluence is set roughly by reducing the transmittance with beam splitters in the attenuator box, after which the fine tuning is achieved by

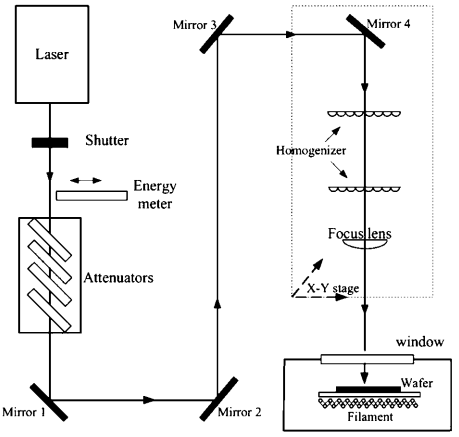

Figure 2.1: Schematic of the XMR7100 system.

adjusting the position of the upper cylindrical lens array of the homogenizer, therefore varying the actual spot size. Typical spot sizes are 0.3–1 $\times$ 1 cm^2. The homogenizer also provides a uniform spatial profile of the pulse. Scanning is performed by moving the optical components shown enclosed with the dotted line in Fig. 2.1, while the wafer is fixed in a vacuum chamber. The sample can be preheated up to 450 °C by a tungsten filament.

Double laser system

A schematic of the Exitech double laser crystallization setup is shown in Fig. 2.2. It consists of two Lambda Physik LPX 210 XeCl excimer laser sources with a wavelength of 308 nm, and a pulse duration of 25 ns FWHM, which are triggered by the pulse generator. Different pulse offsets can be realized by the pulse generator settings, and the jitter between the laser pulses at 1σ is 4 ns. Examples of the temporal profiles are shown in Fig. 2.3. The energy densities are set with the attenuators after which the laser beams are combined. There is an optional path for the pulse extender, which was not used in this work. A homogenizer was used to produce a flat-top intensity profile with a 7% energy variation across a 10 mm^2 area. Spot sizes of either 3 $\times$ 5 mm^2 or 1.5 $\times$ 2.5 mm^2 are determined by the magnification of the projection lens in use, which therefore determines the energy density range too. If both lasers are used simultaneously, then respectively 1200 and 4800 mJ/cm^2 can be achieved. The wafer

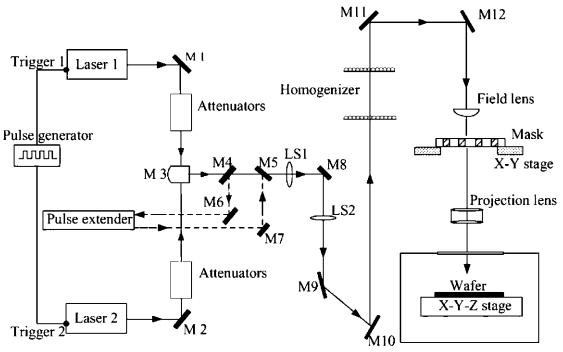

Figure 2.2: Schematic of the Exitech M8000V double laser system. The M1–M12 are mirrors.

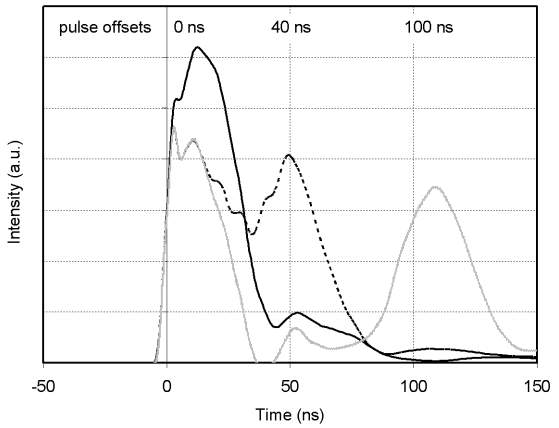

Figure 2.3: Pulse shapes as a result of combining two equal laser pulses with offsets of 0, 40 and 100 ns.

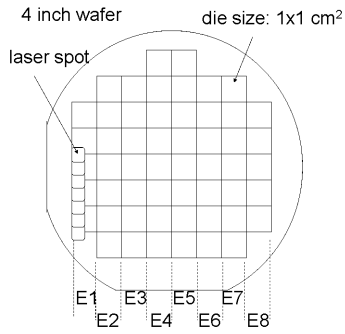

Figure 2.4: Laser annealing makes it possible to vary the annealing parameters over the wafer. A columnar layout for applying the annealing parameters E1–E8 is shown as an example.

is held in the vacuum chamber on a moving stage, which can be positioned with μm accuracy. The chuck can be heated up to 450 °C.

Laser annealing parameters (e.g. energy density, pulse offset or number of shots) can be varied over the wafer. Throughout this work variations were frequently made in a columnar fashion, an example of which shown in Fig. 2.4. Due to the localized manner of the laser annealing, the resulting anneal is subjected to spot-to-spot non-uniformities [Vandervorst et al., 2008].

2.1.2 Laser annealing mechanism

The laser annealing mechanism is described here by considering the variations of the sheet resistance of a laser annealed arsenic implant. P-type bulk or SOI wafers were used, with an SOI thicknesses of 110, 220, 450, 750 or 1500 nm and a buried oxide thickness of 1000 nm. After a 4 min 0.55% HF dip, As^+ was implanted with 15 keV to a dose of 5×10^{14} cm^{-2}. The laser annealing was carried out with the Exitech setup in vacuum, using laser energy densities from 200–1200 mJ/cm^2 with 66% pulse overlap at room temperature or chuck heating of 250, 300 or 350°C. Sheet resistances were measured by a CDE Resmap 4 point probe system.

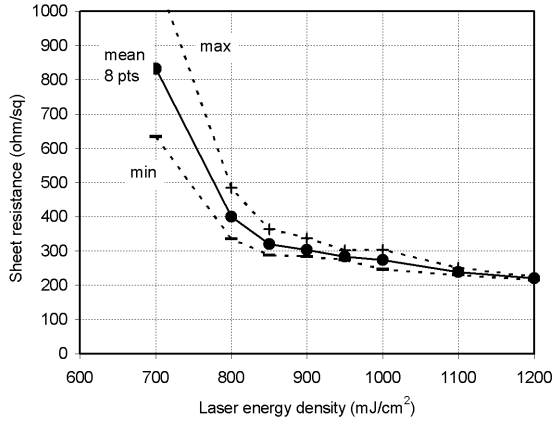

Figure 2.5: Sheet resistance of a laser annealed As^+ 15 keV, 5×10^{14} cm^{-2} implant versus the laser energy density. From 6 to 8 measurement points taken across the wafer are averaged and shown with the solid line. Minimum and maximum values are shown with dotted lines.

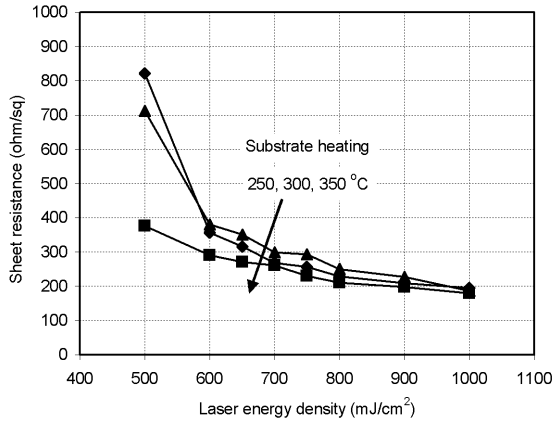

Figure 2.6: Sheet resistance of a laser annealed As^+ 15 keV, 5×10^{14} cm^{-2} implant while the substrate is heated to 250, 300 or 350 °C.

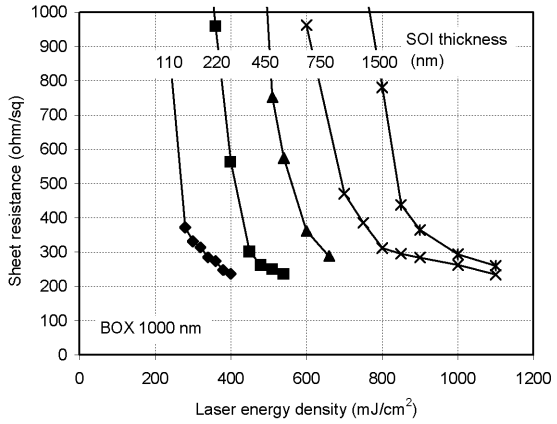

Figure 2.7: Sheet resistance of a laser annealed As^+ 15 keV, 5×10^{14} cm^{-2} implant in SOI with silicon thicknesses of 110–1500 nm. The buried oxide was 1000 nm thick.

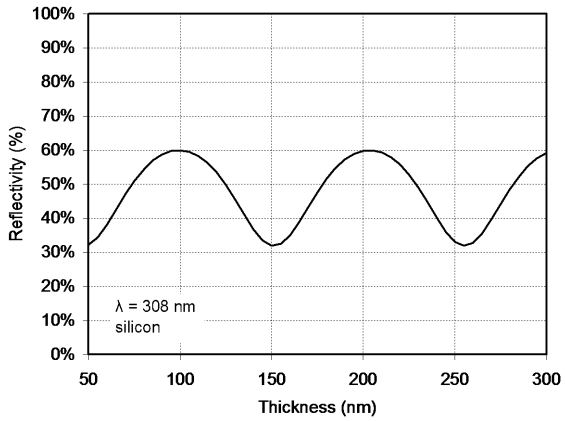

Figure 2.8: Calculated reflectivity of the oxide–silicon stack at a wavelength of 308 nm as a function of the thickness of the oxide capping layer.

Implanted dopant activation

The UV lasing wavelength of 308 nm is absorbed within 6 nm of the amorphous or crystalline silicon surface. While the total thermal budget is very low, it is concentrated in a very small volume at the surface for a very short time. Increasing laser energies result in increasing surface temperatures. The temporal thermal balance is determined by the thermal properties of the substrate, towards which the temperature rapidly decays. Above certain laser energies, surface temperatures exceed the melting temperature of Si. The melt depth extends deeper with the increasing laser energies. In c-Si, ablation will limit the achievable melt depth. In a thin a-Si surface layer above c-Si, such as in implanted Si, melting occurs earlier than in c-Si, because of the lower thermal conductivity and melting temperature of a-Si. As melting temperature is 200–300 °C lower than that of c-Si, the molten part is severely supercooled and explosive crystallization occurs before the full melt [Thompson et al., 1984]. If the melt depth reaches the crystalline interface, it can only propagate further if the melt temperature of c-Si is reached. If this interface is reached, then the c-Si layer will act as a seed layer for resolidification, and therefore an epitaxial layer will solidify. If this interface is not reached, then polycrystalline Si will regrow, and the crystalline quality can be correlated to the laser energy density.

Any dopants residing in the melt, diffuse orders of magnitude faster than in the solid, and will distribute uniformly. During the quick solidification, they are trapped at substitutional sites in the lattice. Due to trapping, concentrations can extend the solid solubility limits.

The sheet resistance, R_{sh} of the layer is strongly dependent on the melt depth, which determines the junction depth, x_j

$$R_{sh} = \frac{1}{q\mu(x_j)N(x_j)x_j} \tag{2.1}$$

where q is the electron charge, μ is the charge carrier mobility, and N is the active doping density. The mobility slightly changes with the doping at high concentrations, further it is also dependent on the number of inactive dopants [Rousseau et al., 1996] and on the crystalline quality of the regrown layer. A typical plot of the measured sheet resistance versus the laser energy is shown in Fig. 2.5. The scatter decreases as the sheet resistance decreases, presumably due to the improvement in the crystalline quality and defect anneal.

Thermal balance

The thermal balance is strongly dependent on the substrate conditions and boundary conditions. Substrate heating increases the total thermal budget and for the same R_{sh} the laser energy range shifts to lower energies as shown in Fig. 2.6. At elevated wafer temperatures, the resulting temperature profile has low thermal gradients and therefore solidification velocities are smaller. As an extra advantage, this effect can be beneficial for defect annealing [Venturini, 2005]. A strong thermal confinement occurs in the case where SOI wafers are used since oxide has a heat conduction coefficient two orders of magnitude lower than Si. The shift to the lower laser energies is dependent on the thickness of the top silicon layer (Fig. 2.7). A trench will also have some effect due to the lateral confinement. An oxide capping layer, as used in Chapter 6, creates a complex situation because the laser light reflectivity of the oxide changes periodically with its thickness as shown in Fig. 2.8. Moreover, as it will draw some heat, it can act as a heat storage or a heat sink, dependent on the thickness [He et al., 2006].

2.2 Process and device modelling

2.2.1 Thermal simulations

To estimate temperature profiles heat conduction is considered and the transient heat transfer equation in 1-D is formulated as

$$\rho c_p(T)\frac{\partial T}{\partial t} + Q_f = \frac{\partial}{\partial x}\left(k(T)\frac{\partial T}{\partial x}\right) + Q(x,t) \tag{2.2}$$

where ρ is the mass density, c_p the specific heat capacity, Q_f the heat of fusion, k the heat conductivity, T the absolute temperature, and t the time.

The heat, Q, generated in the silicon by the laser irradiation is given by

$$Q(x,t) = \alpha(1-R)I(t)\exp(-\alpha x) \tag{2.3}$$

where α is the absorption coefficient, R is the reflectivity of the surface, and I the intensity of the laser pulse. The boundary conditions that are applied in the numerical simulations are given by assuming that the surface is insulated so that

$$\frac{\partial T}{\partial x}|_{x=0} = 0 \tag{2.4}$$

and in the substrate beyond the zone affected by the laser heating the temperature, $T_{x_{max}}$, is set at a constant temperature

$$T_{x_{max}} = T_0 \tag{2.5}$$

The phase transition during melting or solidification causes a moving boundary at the solid–liquid interface, and its velocity depends on the heat rate difference at the interface, which is formulated in a Stefan problem. Different implicit solutions exist such as the enthalpy based method, the moving grid, the level set, and the phase field method. An excellent comparison of the numerical models for the Stefan problems can be found in [Javierre et al., 2006]. In this work, the enthalpy based method and the phase field method were used.

Enthalpy based method

Melting is most conveniently formalized by using the enthalpy [Taler and Duda, 2006]. The enthalpy, h, has a jump discontinuity at the liquid-solid interface determined by the latent heat, L_H given by

$$h(T) = \int c_p(T)dt + L_H \cdot H(T - T_m) \tag{2.6}$$

where H is the Heaviside step function, T_m is the melt temperature. By differentiating this relationship it follows that

$$c'(T) = \frac{dh}{dT} = c_p(T) + L_H \cdot \delta(T - T_m). \tag{2.7}$$

The latter form can be very easily implemented in the simulators. As in Eq. 2.2, Q_f is embedded in a modified specific heat capacity function.

Phase field method

A physically more valid formalization of the moving interface problem is possible with the phase field method as the driving forces acting on the interface are related to the phase field parameters. The sharp liquid-solid interface is replaced with a smooth, diffused interface. A phase function, Φ, that is changing continuously between 0 (liquid) and 1 (solid) can be introduced. The implementation of the phase field method for laser annealing is used hereafter [La Magna et al., 2004]. In Eq. 2.2, Q_f is written as

$$Q_f = 6\Phi(1 - \Phi)\rho L_H \frac{\partial \Phi}{\partial t}. \tag{2.8}$$

The kinetic equation is written as

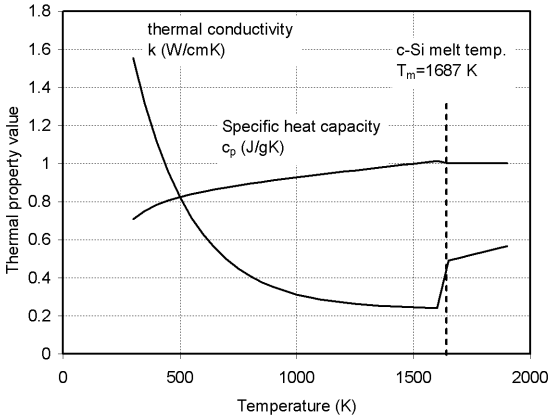

Figure 2.9: Temperature dependent thermal conductivity and specific heat capacity for c-Si and l-Si used in the numerical simulations [Fogarassy et al., 1989, Unamuno and Fogarassy, 1989].

$$\frac{\partial \Phi}{\partial t} = M \frac{\delta F}{\delta \Phi} \tag{2.9}$$

where M is related to the interface mobility, and F is the thermodynamic driving force. The Helmholtz free energy of the system is

$$F = \int_V \left(f(\Phi, T) + \frac{\epsilon}{2} |\nabla \Phi|^2 \right) dV \tag{2.10}$$

where V is the system volume, $f(\Phi, T)$ is the Caginalp-type potential function, ϵ is the interface width. Parameters of this model and a more detailed description can be found in [La Magna et al., 2004].

Equations 2.2 and 2.9 form a system of two coupled partial differential equations describing the system and should be solved simultaneously.

Simulation parameters

In all the simulations performed in this thesis, a 1-D portion of silicon to a depth of 10 μm was simulated with a dense mesh being used close to the surface. The laser pulse shape was approximated as a smooth trapezoidal-like shape with a 10 ns rise time, 10

ns hold time and 30 ns fall time, where the pulse full width at half maximum was 25 ns. Double pulses can be applied with defined offsets.

The absorption coefficient was $\alpha = 10^6$ cm^{-1}, the reflectivity was $R_c = 0.65$ and $R_l = 0.7$ in the solid and in the liquid state, respectively. The melting temperature was $T_m = 1687$ K, the latent heat was $L_H = 1780$ J/g. The material density was ρ = 2.33 g/cm^3. Temperature dependent thermal properties, as shown in Fig. 2.9, were obtained from literature [Fogarassy et al., 1989, Unamuno and Fogarassy, 1989]. For the solid phase the relationship becomes

$$k(T) = 0.235 + 4.45\exp(-T/247) \tag{2.11}$$

$$c_p(T) = 0.81 + 1.3 \cdot 10^{-4}T - 1.26 \cdot 10^4 T^{-2} \tag{2.12}$$

while in the liquid state

$$k(T) = 0.502 + 2.99 \times 10^{-4}(T - T_m) \tag{2.13}$$

and $c_p = 1$ J/gK.

2.2.2 Process and device simulation

Modelling of implantations and furnace anneals was performed with *TSUPREME4*. Low energy implants were modelled by *TRIM/SRIM*. Simple carrier concentrations were calculated with *MEDICI*.

2.3 Test structures and characterization methods

2.3.1 Material analysis

Laser annealed layers were analyzed by measuring the sheet resistance with a four point probe. Chemical and electrical dopant profiling were made with SIMS and SRP, respectively. TEM was used for the analysis of the crystallinity, and AFM was used to analyze the surface morphology.

Four-point resistance measurements

The CDE Resmap sheet resistance meter was used to measure the sheet resistance of laser annealed implants with energies down to 5 keV. The arsenic implants were performed in p-type wafers with a resistivity of 2-5 ohm-cm.

A critical issue with respect to shallow junction measurement is the probe penetration and its influence on the measured results. An excellent treatment of this subject can be found in [Clarisse et al., 2006]. Measurement heads with 100 and 500 μm probe radii were used. The latter provides lower contact forces so it was used to measure shallow layers.

Normally the CDE meter is used to measure uniformly implanted and annealed wafers. If the surface is patterned the value measured within one uniform region will depend on the distance to the neighbouring regions and the doping profile depth of the individual junctions. These parameters will determine the current spreading into the neighbouring regions. Since the laser annealed regions are very shallow, it was possible to pattern the surface in regions of 1×1 cm^2 by trench isolation and still measure sheet resistance values to an accuracy within 1%.

Probes were placed at least $2\times$ the probe spacing distance from the perimeter of these areas so that edge effects were negligible. Accuracy can be an issue where partially annealed areas are measured since these can contain grains that give a non-uniform current distribution. In the formulas homogenous sheets are assumed.

SIMS

Chemical doping profiles have been determined with secondary ion mass spectroscopy (SIMS). It requires a relatively large square area of about 300 $\times$ 300 μm^2, and the detection limit is about 10^{16} cm^{-3}, depending on the element. The resolution is about 0.5-1 nm/decade, which limits the accuracy of the measurement in conjunction with very abrupt and ultrashallow profiles.

SRP

Electrically active dopant profiles can be determined by spreading resistance profiling (SRP). In this method, the surface is bevelled under a low angle, and the probes measure the spreading resistance along the bevelled path. This is then translated to a depth profile. The spreading resistance is calibrated with doped etalons so that the carrier concentration can be measured. A Poisson-solver can be used to accurately determine the active doping concentrations [Dickey, 1992]. Steep profiles are difficult to measure due to carrier spilling and space-charge effects [Clarisse et al., 1996].

TEM

Imaging with transmission electron microscopy (TEM) is used to inspect cross sections and it is capable of atomic resolution. The TEM images shown in the following section

in Fig. 3.2 and Fig. 3.12 were prepared from of a fully processed and electrically characterized transistor test structure with a laser annealed emitter. The emitter size was 40 $\times$ 40 μm^2, and the cutting plane was approximately across the midplane of the active region at an edge of a contact window. The sample dimensions were 5 $\times$ 3 μm^2 for the cross sectional area, and the thickness was about 100 nm. Magnifications up to 100.000$\times$ were used.

AFM

The surface roughness for etched, implanted or laser annealed surfaces was measured by atomic force microscopy (AFM). The scanned base area was 5 $\times$ 5 μm^2 for all the measurements. The pre-processing of the data consists of compensating for waviness or any background envelope or skewness. Then the surface roughness was determined over the whole field, and extreme peaks were excluded in this case.

The root mean square is a common statistical parameter describing the scatter, and it is formulated for the surface roughness measurements by

$$R_q = \sqrt{\frac{1}{A}\int_A (x - \overline{x})^2 dA}. \tag{2.14}$$

where A is the surface area, x is the height parameter, the overscore denotes the mean value.

2.3.2 Electrical device characterization

A set of rectangular and ring-shaped circular bipolar transistor structures are available with different emitter sizes [Liu et al., 2006]. The basic cross-section is shown for an NPN transistor in Fig. 2.10. The buried n$^+$-layer forms the collector contact on which an undoped epitaxy layer is grown. A 30 nm thermal oxide is grown through which the p$^+$ contacts, the n$^+$-plug to the buried layer and the lightly-doped p-type base are implanted and annealed.

The circular bipolar transistors with double base contacts were designed with different emitter lengths, which allows to extract transistor parameters in the intrinsic transistor region by subtracting the peripherial regions as shown in Fig. 2.11. The central radius of the emitter is constant (emitter width, $W = 431$ μm) for all the devices, while the emitter length, L, varies from 1, 2, 4, 6, and 10 μm. Therefore emitter area, A, varies (A = 431, 862, 1724, 2586 or 4310 μm^2) while the perimeter lengths are practically the same ($P = 2W = 862$ μm).

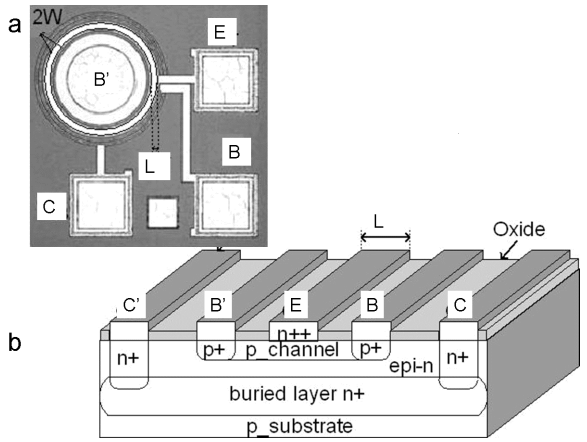

Figure 2.10: (a) Photo of a ring-shaped NPN test structure. (b) Cross section through the ring from inner to outer edge. [Liu et al., 2006]

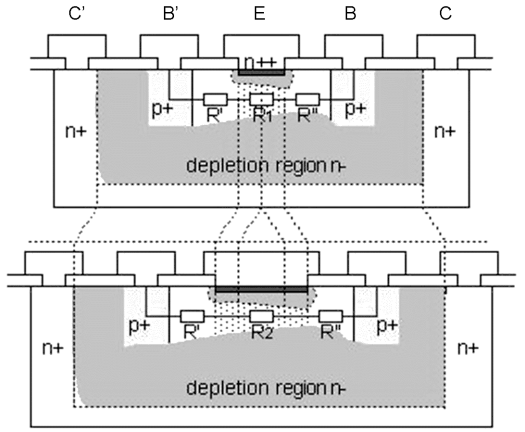

Figure 2.11: Cross section showing that the B–B' contact regions are the same for both small and large L. The emitter and collector depletion regions for $V_{B-B'} < 0$ and $V_B = V_E = V_C$ are indicated. [Liu et al., 2006]

Sheet and contact resistance structures are also available on patterned wafers. Sheet resistances can be determined by using van der Pauw crosses through a four point measurement. The measurement limit is about 40 kohm/sq. Contact resistance can be measured by specially designed Kelvin structures with contact sizes from 10×10 down to 2×2 μm^2 [Nanver et al., 1996].

The electrical characteristics were measured using an Agilent 4156C parameter analyzer, a HP 4278A capacitance meter, and a Cascade Microtech probe station equipped with DCM200 probes that have negligible probing series resistance.

The following electrical measurements were carried out on the ring shaped structures: junction characterization, Gummel plots, determination of pinch-off and base sheet resistance, capacitance-voltage characteristics, and mobility in the base.

Diode characteristics

The emitter masks designed for transistors have also been used to fabricate diodes to the substrate, which then is contacted either on the front or by metallizing the back of the wafer. The junctions have been characterized by diode I–V measurements, an example of which is shown in Fig. 6.2, where the emitter contact has been biased from -1 to 1V and the substrate is the grounded. The forward diode current in the small to medium current range follows the relationship

$$I = I_0 \exp\left(\frac{V}{n(V)V_T}\right) \tag{2.15}$$

where I is the measured current, I_0 is the saturation current, V is the applied bias, $n(V)$ is the ideality factor, $V_T = kT/q$ is the thermal voltage, in which k is Boltzmann's constant, T the absolute temperature.

Gummel plots

Both the B–E and the B–C diode quality can be evaluated in the forward and reverse Gummel plots. In the forward Gummel plots, the base current is determined by the emitter Gummel number, G_E, the base–emitter junction area, A_{BE}. The collector current is determined by the base Gummel number, G_B. The magnitude of the currents in the small to medium current range can be written in the form of eq. 2.15 where the parameters for I_0 and V can be chosen for the particular setup and measured current I from Table 2.1. These formulas are only valid for the laterally uniform case, i.e. when perimeter components are excluded. The intrinsic carrier concentration is n_i. The Gummel number is the total majority carrier charge in the concerning transistor region. D_n and D_p are the electron and hole diffusion coefficients, respectively.

Table 2.1: Parameters for Eq. 2.15 for the determination of the transistor currents of forward or reverse Gummel plots in low to medium current range.

Gummel plot	I	I_0	V
forward	I_B	$qn_i^2 A_{BE} \frac{D_p}{G_E}$	V_{BE}
	I_C	$qn_i^2 A_{BE} \frac{D_n}{G_B}$	
reverse	I_B	$qn_i^2 A_{BC} \frac{D_p}{G_C}$	V_{BC}
	I_E	$qn_i^2 A_{BC} \frac{D_n}{G_B}$	

By measuring the reverse Gummel plot, The base current is determined by the collector Gummel number, G_C, for the base-collector junction area, A_{BC}. The emitter current is determined by the base Gummel number, G_B.

For any of the measured currents, I, the current per unit area, J, in the laterally uniform region under the emitter can be isolated by plotting I as a function of L. The perimeter component I_P, which includes all currents that do not scale linearly with L may be extracted by identifying the emitter lengths that are large enough to give a linear relationship. From the extracted forward Gummel plots the J characteristic corresponding to the base current can be isolated as well as the ideality of this current. If the gain of the transistor is much higher than 1, the base current will be lower than the corresponding total diode current and is therefore a much more sensitive monitor of any non-ideal leakage currents. From the measurements, the ideality factor n of the diode region localized under the emitter can also be extracted by Eq. 2.15. In general a large emitter length is advantageous for accurate determination of parameters that scale linearly with L, while the access to several small gate lengths gives a better means of evaluating of perimeter components.

Pinch-off

In a junction FET (JFET) like operation, the two base contacts act as source and drain and the base becomes the channel. In such a setup the pinch-off can be measured by measuring the channel current while narrowing the channel by reverse biasing the top or bottom gate. The pinch-off is corresponding to the closing of the channel.

Sheet resistance

The sheet resistance in the intrinsic base can be extracted by measuring the base resistance by I–V measurements across the $B - B'$ contacts of the ring structures for $V_{B-B'} = 0$ while keeping the emitter and the collector reverse biased. The sheet resistance, R_{sh} can be extracted by plotting the measured resistance as a function of the emitter length, L, and identifying the linear region

$$R_B = \frac{dV_{B-B'}}{dI_B}\Big|_{V_{B-B'}=0} = R_p + R_{sh}\frac{L}{W} \tag{2.16}$$

where R_B is the base resistance between the two base contacts, $V_{B-B'}$ is the voltage applied between the two base contacts, I_B is the measured base current, R_p is the perimeter component, L and W are the emitter length and width, respectively. The sheet resistance or the sheet conductance, G_{sh} at a certain emitter or collector reverse bias, is dependent on the base active dopant concentration, N_A, the base width, w_B, and the hole mobility in the base, μ_p

$$R_{sh}(V_C, V_E) = \frac{1}{G_{sh}(V_C, V_E)} = \frac{1}{q\int_{w_B(V_C,V_E)} \mu_p(x) N_A(x) dx} \tag{2.17}$$

Capacitance-voltage characteristics

The laterally uniform capacitance in the intrinsic region can be isolated by means of differential measurements similar manner as in eq. 2.16. This way the parasitic effects are also excluded. As the laser annealed emitter-base junction is abrupt and high-doped, capacitances measured here can be used for extracting the active doping profile in the base

$$N_A(x = x_j + w(V_E)) = \frac{-2}{q\varepsilon_s \left(\frac{d(1/C^2(V_E))}{dV_E}\right)} \tag{2.18}$$

where ε_s is the permittivity of silicon, C is the specific capacitance, V_E is the applied reverse bias, x_j is the emitter's junction depth, and the depletion depth, w, is

$$w(V_E) = \frac{\varepsilon_s}{C(V_E)} \tag{2.19}$$

Mobility in the base

The mobility in the base is determined in a differential manner by combining the sheet conductance and the active doping profile data. The mobility in a p-doped base as a function of the depth can be extracted by rearranging eq. 2.17 as

$$\mu_p(x) = \frac{dG_{sh}}{-qN_A(x)dx}. \tag{2.20}$$

Chapter 3

Process optimization for laser annealing of implanted junctions

In this chapter, the integration of laser annealing with the use of LPCVD TEOS as surface isolation and an Al reflective masking layer is examined and generally valid conclusions on the procedures needed to achieve good ideality of the laser annealed diodes are extracted.

3.1 Experimental considerations

The basic process flow for the fabrication of laser annealed diodes is shown in Fig. 3.1 for n^+p diodes. Both p^+n and n^+p diodes are fabricated on (100) p-type silicon wafers that are patterned with both n- and p-type regions with a surface doping of 10^{17} cm^{-3}. In all the results presented in this chapter, the p^+ and n^+ regions to be laser annealed are formed by a 5 keV, 1–3 $\times$ 10^{15} cm^{-2} BF_2^+ and As^+ implantations, respectively with tilt angles of 7 and 30 degrees. Buried layers and deep implants are employed in some structures to allow contacting via the surface rather than from the back of the wafer and to achieve low diode series resistance. Rectangular diodes are measured in a size range from 2 $\times$ 1 to 40 $\times$ 40 μm^2. Moreover, on some wafers Kelvin contact resistance test structures and van der Pauw sheet resistance structures are fabricated with the extra implants.

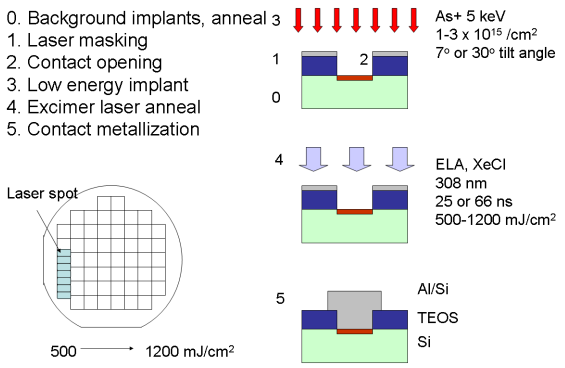

Figure 3.1: Schematic of basic process flow for fabrication of n^+p laser annealed diodes.

The ELA implants are performed directly in the contact windows, which has the advantage that no high temperature thermal processing is necessary after the laser anneal to complete the devices and the characteristics achieved by pure laser activation can be studied. The individual processing steps have been varied in several respects:

- The 330 nm thick surface isolation layer is either thermal oxide, LPCVD TEOS oxide deposited at 700 °C or a stack of 30 nm thermal oxide covered with LPCVD TEOS.

- The ELA reflecting masking layer is either a Al/Si(1%) or a pure Al layer deposited with different thickness by PVD at either 50 °C or 350 °C,

- the contact windows are defined by different combinations of plasma and wet etching through the Al and oxide to the silicon. The bulk of the plasma etch is performed by high rate, high power plasma etching where the Al is etched with a chlorine plasma until the underlying oxide layer that then is etched in a fluorine plasma. The actual landing on the silicon is performed with either a hard landing, where the oxide is etched with the high power plasma down to the silicon surface, or a soft landing where the power is reduced by 66%. Moreover a wet landing using different HF solutions is investigated,

- just before implanting the contacts, a short dip etch step is performed to remove the native oxide. A 3 min 0.55% HF dip is compared to dipping in 1:7 diluted buffered hydrofluoric (BHF) acid,
- the implantation was performed with either a standard 7° tilt with 22° twist or high tilt angles of 30° or 45° with 8 equal rotations to minimize shadowing with doses from 1–3 $\times$ 10^{15} cm^{-2}.
- The laser annealing after the implantation was performed in a vacuum, using a XeCl excimer laser system with a wavelength of 308 nm, pulse duration of 66 ns (full width at half maximum), unless otherwise specified. On each wafer the laser energy densities are varied in the range of 500 to 1200 mJ/cm^2. A single shot anneal is used because the masking layer deteriorates after each shot [Nanver et al., 2003].
- Before the standard metallization process, a HF dip etch step is performed to remove the native oxide before the metallization. The dip etch times are varied from 0–4 min.
- A new layer of 600 nm Al/Si(1%) is sputtered, patterned and the created contacts are measured before and after alloying at 400 °C for 30 min in forming gas.

3.2 Results

Processing steps shown in Fig. 3.1 from 1–5 are evaluated.

3.2.1 Laser masking

Isolation layer

The ideal isolation layer is also a good Si interface passivation layer. Moreover, it has low deposition temperature, good dielectric properties, good interface properties, is reflective to laser light and has low etch rates in HF. CVD nitrides that has extremely low etch-rates in HF are not directly an option because these materials have a high absorption of laser light and readily ablate for the energies applied here. For this reason only oxides are considered. Process parameters for the available oxides are summarized in Table 3.1. PECVD oxides are deposited at low temperatures (∼400 °C) but they are not directly applicable to Si due to the interface properties and the low material density. High etch rates during the pre-metallization dip etch step result in enlargement of the contact windows, therefore insufficient oxide overlap at the diode edges, which leads to

Table 3.1: Process parameters for the isolation layers.

layer	dep. temp. (°C)	etch rate in 0.55% HF (nm/min)
thermal oxide	>1000	2.5
LPCVD TEOS	700	10
PECVD TEOS	400	15

perimeter leakage of the diodes. The available LPCVD TEOS deposited at 700 °C has better properties, but is still not suitable as sole isolation layer because of its interface properties, and the relatively high etch rate. Thermal oxides give the best isolation properties, and low etch rates but at high temperature processes. For this reason a combination of 30 nm thermal oxide and 300 nm LPCVD TEOS is needed. The thin thermal oxide layer is sufficiently dip etch resistant to preserve the isolation of the diode edges due to the low etch rate of 2.5 nm/min in 0.55% HF. All oxide layers are partially transparent at the laser wavelength. Therefore, an additional reflective masking layer is needed.

The ideality of diodes fabricated using the different combinations of isolation layer is summarized in Table 3.2. Very low ideality factors of 1.1 are achieved with pure thermal oxide isolation when hard landing and HF dip is used (Fig. 3.3). The same etch conditions give very high values, about 1.66–2.3, when replacing the bulk of the thermal oxide with TEOS. A combination of 30 nm thermal oxide and 300 nm LPCVD TEOS with soft landing and BHF dip gives a very significant improvement with values from 1.1–1.3 being reached (Fig. 3.13). This is comparable to the pure thermal oxide

Table 3.2: Comparison of n^+p diodes with different isolations. Al/Si layer thickness: 100 nm, implant tilt: 30°, pre-metallization dip etch in 0.55% HF: 4 min.

isolation	ideality
330 nm thermal oxide	1.1
330 nm TEOS	1.66–2.3
30 nm thermal oxide + 300 nm TEOS	1.1–1.3

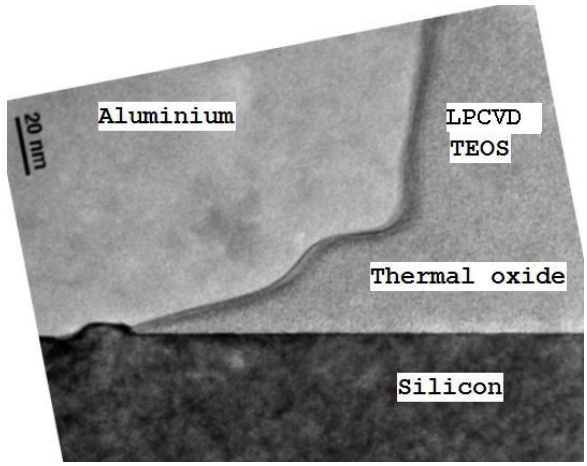

Figure 3.2: TEM image of the contact window edge. Laser masking: 30 nm thermal oxide, 300 nm TEOS, 100 nm Al/Si. Pre-implantation dip etch: 15 sec in 1:7 BHF, pre-metallization dip etch: 4 min in 0.55% HF.

situation. Figure 3.2 shows a TEM image of a diode edge in a fully processed device. Due to the lower etch rate of thermal oxide compared to PECVD TEOS, a smaller enlargement of the contact window at the interface is apparent, and therefore the diode edges are protected. The thermal oxide ensures sufficient isolation and prevents leakage. Pre-metallization etching time was 4 min in 0.55% HF for all cases.

Reflective mask

Laser annealing can be masked by a reflective layer. The reflectivity of the oxides for the lasing wavelength is periodically changing with its thickness between 30-60% (Fig. 2.8). A more controllable situation can be created by adding a high reflectivity layer. In our case sputtered Al layers are used as reflective coating. The more than 300 nm thick Al/Si(1%) layers normally used for metallization were found to have several drawbacks. Normally a sputtering temperature of 350 °C is used to achieve good step coverage but this also entails large grain formation. The laser annealing of these large grain layers results in a non-uniform composition of the Al/Si that is difficult to plasma etch uniformly during subsequent contact window etching. Using 100 nm thin layers deposited at 50 °C results in a fine grain structure. An improvement in the diode

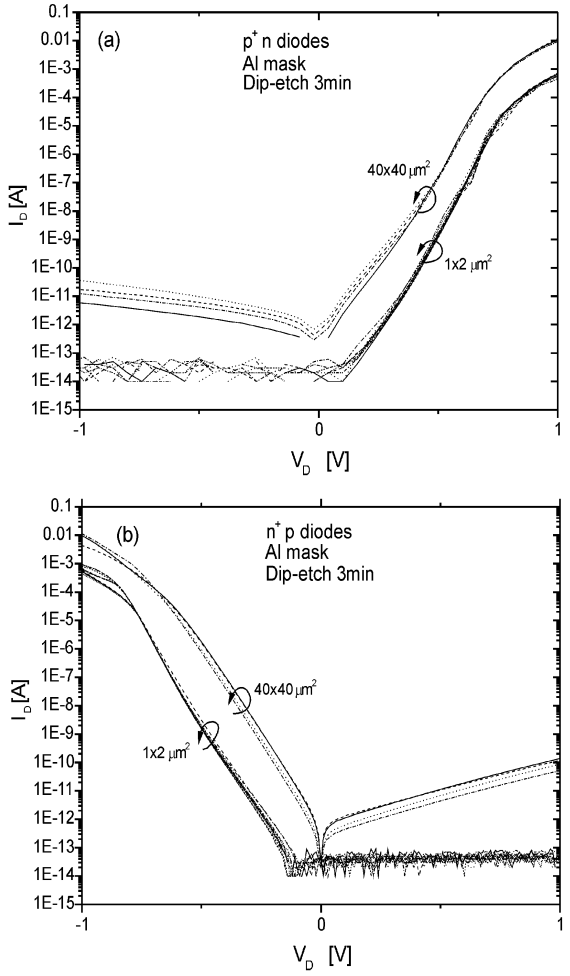

Figure 3.3: Over the wafer measurements of I–V diode characteristics for (a) p^+n and (b) n^+p diodes, with diode areas of $1 \times 2\ \mu m^2$ and $40 \times 40\ \mu m^2$. Laser masking: 300 nm thermal oxide, 600 nm Al/Si [Nanver et al., 2003].

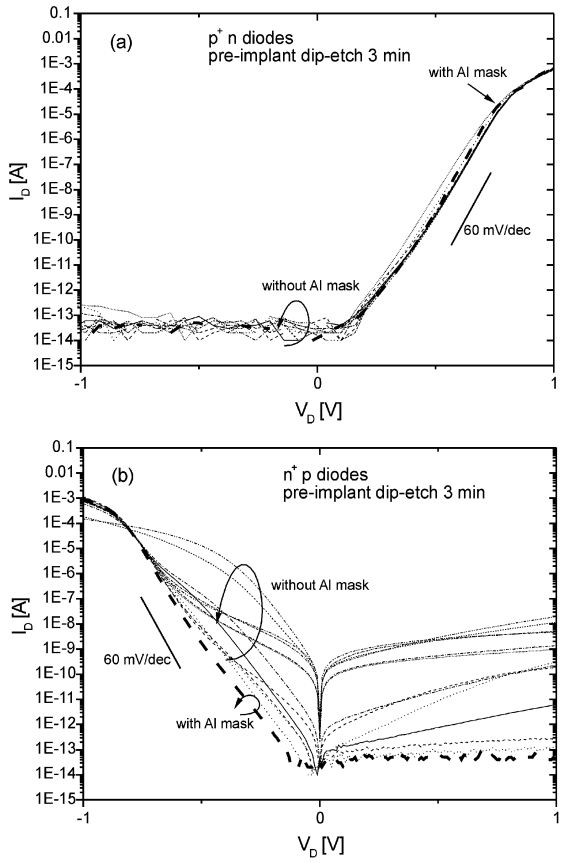

Figure 3.4: Over the wafer measurements of I-V diode characteristics for (a) p^+n and (b) n^+p diodes with a diode area of $1 \times 2\ \mu m^2$, with and without an Al masking layer. Laser masking: 300 nm thermal oxide, 600 nm Al/Si [Nanver et al., 2003].

Table 3.3: Pre-implant RMS surface roughness (angstrom) as a function of the type of Al masking layer and the etch process used for landing on the silicon. Laser masking: 300 nm thermal oxide, 100 nm Al(/Si).

landing	Al	Al/Si
hard	17	27
soft	12	12
wet	11	35

characteristics is shown in Fig. 3.4 with an Al/Si reflective layers for As^+ and BF_2^+ ELA implants.

3.2.2 Contact window etching

The laser annealed junctions are self-aligned to the contact windows, in which they are implanted. Opening the contact window requires etching through the Al(Si)/ TEOS/ (thermal oxide) layer stack, which is performed by plasma etching with chlorine chemistry for the metal and fluorine chemistry for the oxide layers. The landing on the silicon has to be tuned in order to prevent large overetching and consequent surface degradation.

The effect of the landing is studied by determining the surface roughness of the silicon surface after etching by AFM [Gonda et al., 2004]. The measurement procedure is described in Section 2.3.1. Results are shown in Table 3.3. The soft landing procedure, where plasma power was decreased when reaching the Si surface, in general resulted in the smoothest surface in the close to 10 angstrom RMS roughness. However, excessive soft etching (overetching) can damage the silicon surface so in practice it can become a critical step. The wet landing in combination with pure Al results in an equally smooth surface. For both hard and wet landing the results indicate an increased surface roughness when Al/Si is used as reflective layer. For wet landing, this can be attributed to Si precipitates from the Al/Si and to avoid this issue it can be more attractive to use a pure Al reflective coating.

However, when most of the thermal oxide is replaced by TEOS, the resulting diode characteristics also become sensitive to the total contact window etch procedure, especially to the pre-implantation dip etching.

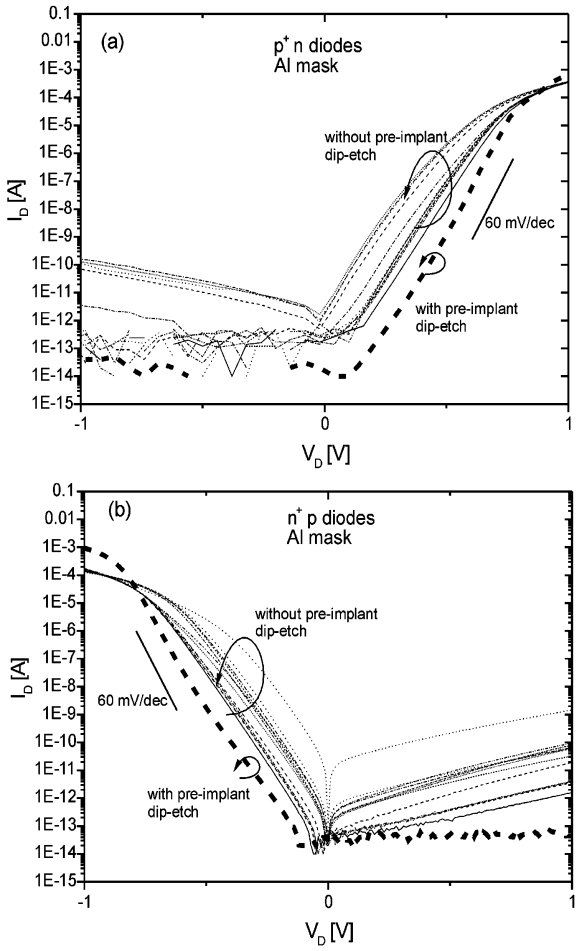

Figure 3.5: Over the wafer measurements of I–V diode characteristics for (a) p^+n and (b) n^+p diodes with a diode area of $1 \times 2\ \mu m^2$, with and without a 3 min dip etch in 0.55% HF prior to the implantation. Note that in case of p-diodes at uncovered edges a Schottky diode forms. Laser masking: 300 nm thermal oxide, 600 nm Al/Si [Nanver et al., 2003].

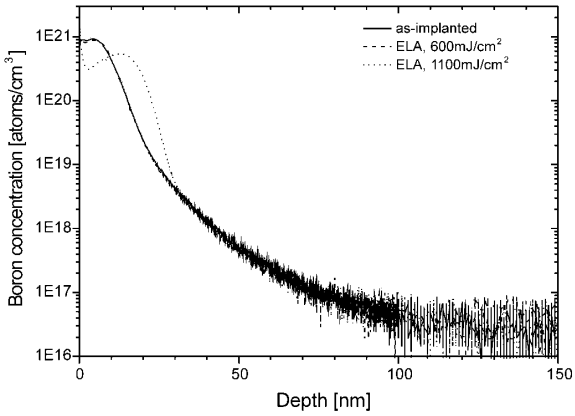

Figure 3.6: SIMS profiles of the boron chemical concentration after a 5 keV 10^{15} cm^{-2} BF_2^+ 7° implant and laser annealing at 600 or 1100 mJ/cm^2 [Burtsev et al., 2004].

3.2.3 Low-energy implantation

Pre-implant dip etch

The results in Fig. 3.5 show that the surface of the contact window should be dip etched in HF to remove native oxide before the low-energy implant in order to guarantee good diode characteristics. This is correlated to the fact that due to the very short range of the ions, a large number are captured in the non-uniform native oxide layer.

However, with the conventionally applied 0.55% HF acid the etch rate of Al is high (75 nm/min) and this prohibits its use in combination with thin reflective coatings. An alternative, short time etching in BHF, was found to give attractive results for an etch time of 15 s. In this process about 50 nm Al/Si and 60 nm of TEOS oxide are etched. In BHF the etching of the Al is a self-terminating process with a maximum of 50 nm being etched so that a reliably thin masking layer remains.

Implantation parameters

A shallow implantation can be achieved by using low implantation energies. The lowest achievable energy depends on the implanter machinery. A SIMS profile of the 5 keV BF_2^+ implant with a tilt angle of 7° is shown in Fig. 3.6, the as-implanted B^+ projected range is about 7 nm. The advantage of the compound is that 49/11 times higher energies

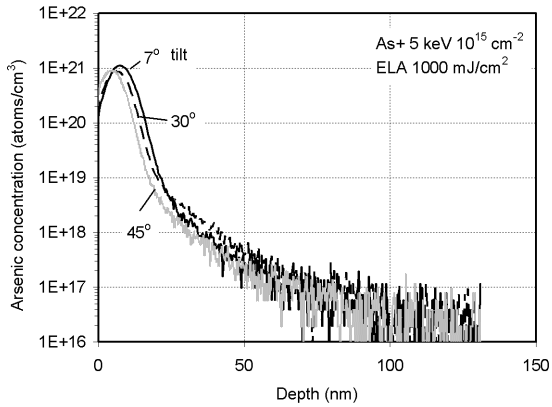

Figure 3.7: SIMS profiles of the arsenic chemical concentration after a 5 keV 10^{15} cm^{-2} As^{+} implant with tilt angles of 7, 30, and 45 degrees and laser annealing at 1000 mJ/cm^2 with a 25 ns pulse.

can be used to achieve the same implant depth compared to B^{+} ion implantation due to the large total mass.

All the doses used for the shallow implants are well above the amorphizing limit. Increase of the dose from 1 to 3 $\times$ 10^{15} cm^{-2} will not give a significant increase in the implantation depth, but the amorphous zone will be deeper. This is valid for the implant energies in the low energy range [Jones et al., 1998]. The generated amount of implantation damage scales with the implant dose as well [Hobler and Otto, 2003].

Tilted implants are beneficial to increase the overlap with the window or gate edges, and these implants also result in shallower profiles. Trim simulations results for 5 kev As^{+} implantation into silicon show that increasing tilt angles of 7°, 30° and 60° results in projected ranges of 85, 74 and 46 angstroms with straggle of 30, 29 and 25 angstroms, respectively. Sputtering of silicon also increases with the increasing tilt angles as 1, 1.58 and 6 atoms/ion, respectively. SIMS results for a 10^{15} cm^{-2} As^{+} implant with tilt angles of 7, 30, and 45 degrees, laser annealing at 1000 mJ/cm^2 are compared in Fig. 3.7. Increasing tilt angles result in shallower profiles. The dose loss is apparent in the measured doses: 1.05 $\times$ 10^{15} cm^{-2}, 7.98 $\times$ 10^{14} cm^{-2}, and 7.43 $\times$ 10^{14} cm^{-2} with the increasing tilt angles. Slightly more channelling is seen at 30° tilt. The abruptness of the tail of the profiles are about 5 nm/decade.

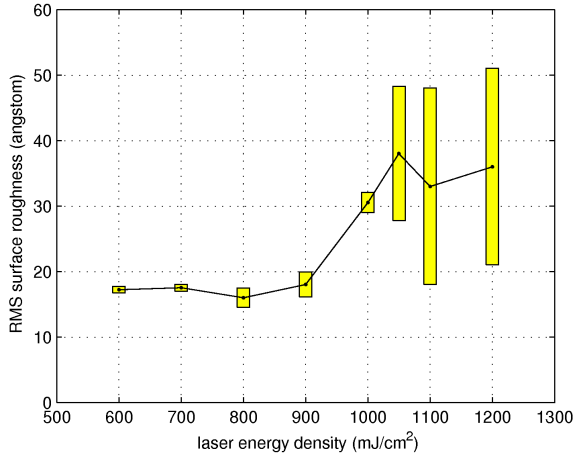

Figure 3.8: AFM measured surface roughness of an As^+ 10^{15} cm^{-2} 5 keV implanted and laser annealed surface as a function of laser anneal energy [Burtsev et al., 2004].

Electrical diode characteristics show a dependence on the tilt for the n^+p but it is less obvious for the p^+n diodes. Typical measurements of the I-V characteristics of p-type diodes that were fabricated with 30° tilt during the implant are shown in Fig. 3.14. The spread in ideality factor increases as the laser energy density increases, which can be attributed to laser induced surface roughening. Leakage currents are reduced in the case of As^+ implants, when the implantation tilt is changed from 7° to 30° as can be seen from the improvement in I–V characteristics of n^+p diodes in Fig. 3.13.

3.2.4 Laser anneal

During the laser illumination the surface layer is melted to a depth that depends on the laser energy. The redistribution of dopants seen in Fig. 3.6 indicates that for an ELA of 600 mJ/cm^2 is necessary for the melt onset while 1100 mJ/cm^2 causes full melt with a depth 20 nm. The junction depth at a doping of 10^{18} cm^{-3} has also been measured by a special CV-profiling technique [Nanver et al., 2003] to be in this range. The activation is very high in the melted region and for an optimal recrystallization of this region the melt zone should extend past the original amorphous/ crystalline interface. Beneath the recrystallized region the implantation induced end-of-range defects are not necessarily annealed. The defect distribution has been studied by positron annihilation

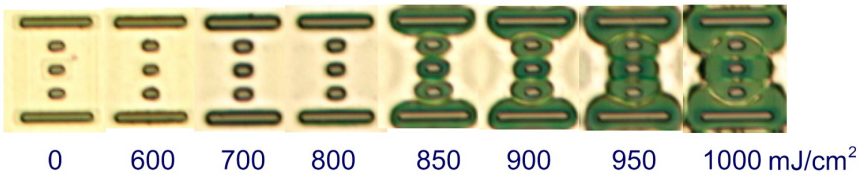

Figure 3.9: Enlargement of the aluminium mask windows due to the high temperatures experienced around the laser annealed silicon. The size of the small opening is 2 × 1 μm^2. Laser masking layer: 30 nm thermal oxide, 300 nm LPCVD TEOS, 100 nm Al/Si.

doppler broadening technique [Burtsev et al., 2004], and it was shown that defects also accumulate at a depth of 150-200 nm.

At energies as large as 1200 mJ/cm^2 a pattern generally referred to as laser induced periodic surface structure (LIPSS) develops [Burtsev et al., 2004]. Surface roughness values are somewhat lower for B^+ implanted surfaces but the trend is the same. With the 30° tilt the amorphous region is shallower than with the 7° tilt. Since the amorphous region melts at a lower temperature than the crystalline silicon (about 1150 °C as compared to 1414 °C) the depth of the a-Si is decisive for the depth of the melt zone. Therefore, for the higher energies the 30° tilt diodes will be shallower than the 7° tilt ones. It is plausible that the increased surface roughness at the high energies will have a detrimental effect on the diode characteristics if the junction depth reaches a critically low value.

The observed surface degradation can be correlated to the measured surface roughness after the laser energy, an example of which is shown in Fig. 3.8 for an As^+ implanted Si surface. At lower laser energies the root mean square (RMS) surface roughness of 17 angstrom is equivalent to the as-implanted situation. For energies above 1000 mJ/cm^2 this increased to values above 30 angstrom.

Heating effects

The silicon temperature achieved by laser annealing exceeds melt in the windows and decays toward the bulk of the wafer as well as laterally. In the latter direction temperatures may exceed ablation limits of the aluminium mask, which then show enlargements after the laser annealing as shown in Fig. 3.9. At energies of 850 mJ/cm^2 the characteristic length is about 1.5 μm causing the enlarged areas to join since the dis-

tance between the openings is 3 μm. The mutual heating can cause different temperature distributions in openings with different pitch and/or shape, resulting in different annealing, i.e. a pattern effect. As openings are much larger than the laser wavelength, this pattern effect does not involve diffraction.

3.2.5 Metallization

Dip etching

To ensure a low resistance contacting, a dip etch in 0.55% HF is carried out before the deposition of the metal contacts to remove the native oxide. Long etching times may be detrimental as the laser annealed implantations are very closely aligned to the contact windows, which are also etched and enlarged by the dip. The effect of the dip etch is shown in Fig. 3.10 for the contact resistance to a laser annealed As^+ or BF_2^+ implant. The dip etch cannot be avoided but in this experiment its duration could be reduced from the standard 4 min to 1 minute, while still achieving low contact resistance. However, the overall conditions leading to native oxide formation are not well-controlled and shorter than 4 min dip etches have proven to be unreliable.

Alloying

The reduction of diode leakage due to the H-passivation of the oxide–Si interface is shown in Fig. 3.11 on the diode characteristics for p^+n diodes before and after the alloying step. The alloying is carried out at 400 °C for 30 min in forming gas.

3.3 Optimal process results

Devices are fabricated with the following process parameters:

- The surface passivation consists of a 30 nm thermal oxide layer, on which 300 nm LPCVD TEOS is deposited.
- The ELA reflecting masking layer is 100 nm Al/Si(1%) deposited by PVD at 50 °C.
- Contact windows are opened by high power plasma etching in chlorine chemistry through the Al and fluorine chemistry through the bulk of the oxide. The actual landing on the silicon is performed with soft landing with a low power plasma.

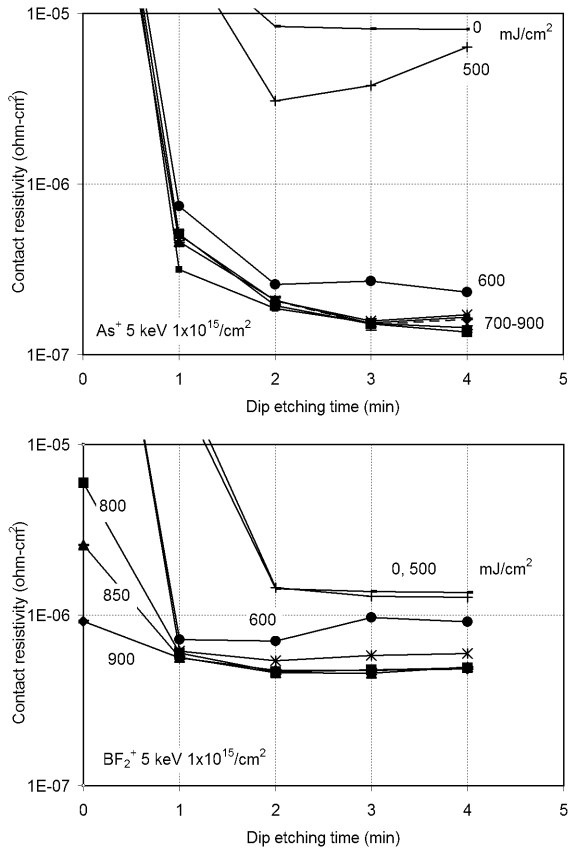

Figure 3.10: The effect of the dip etching times and laser annealing on Kelvin contact resistivities for As^+ (top) or BF_2^+ (bottom) implanted contacts, annealed with a 25 ns pulse. Laser masking: 30 nm thermal oxide, 300 nm LPCVD TEOS, 100 nm Al/Si.

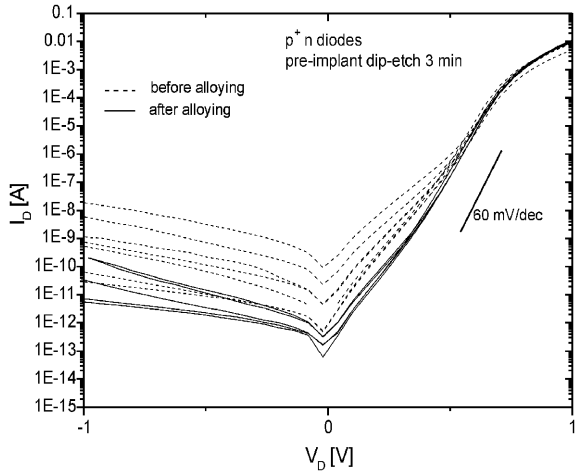

Figure 3.11: Over the wafer measurements of I–V diode characteristics for p^+n diodes before and after the alloying step. Diode areas of 40×40 μm^2. Laser masking: 300 nm thermal oxide, 600 nm Al/Si [Nanver et al., 2003].

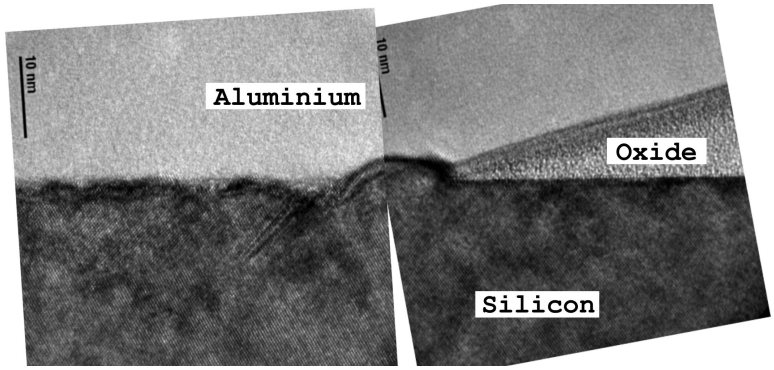

Figure 3.12: HRTEM of crystallinity in the laser annealed region. As^+ 5 keV $3\times10^{15}cm^{-2}$, tilt 30°, annealed at 900 mJ/cm^2.

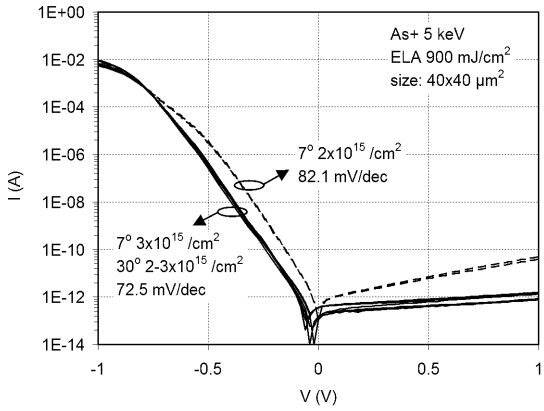

Figure 3.13: I–V characteristics of diodes implanted with As^+ at a tilt angles of 7° or 30° and laser annealed at 900 mJ/cm^2. The forward slopes are indicated. The optimized fabrication process was used.

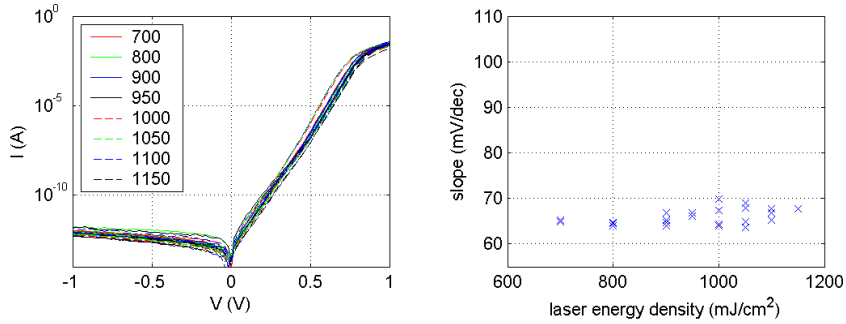

Figure 3.14: Over the wafer measurement of 40×40 μm^2 p^+n diodes implanted with BF_2^+ at an angle of 30°, 2×10^{15} cm^{-2}, 5 keV (left), slope @0.4 V versus laser energy density (right). The optimized fabrication process was used.

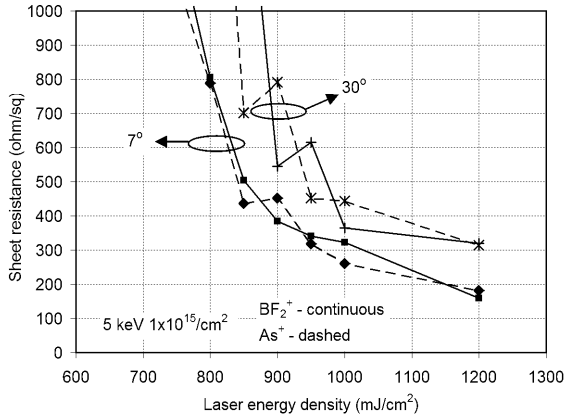

Figure 3.15: Sheet resistance of laser annealed As^+ and BF_2^+ implanted layers. Implantation dose 10^{15} cm^{-2} under 7° or 30° tilt angles.

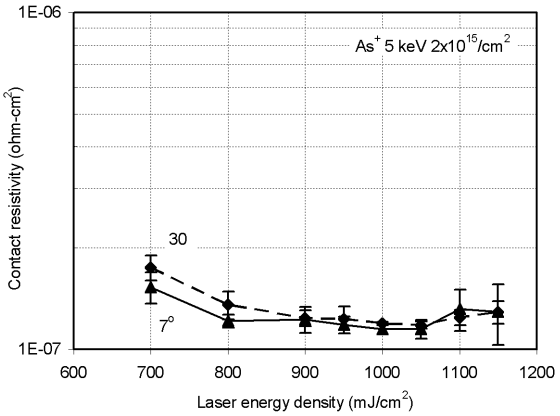

Figure 3.16: Contact resistivity versus laser energy density of the 5 keV 2×10^{15} cm^{-2} As^+ implants under 7° or 30° tilt angles.

- Just before the low energy implantation, a 15 sec dip etch step is performed in 1:7 BHF to remove the native oxide.

- Implantations are compared with either a 7° or 30° tilt with doses from 1–3 $\times$ 10^{15} cm^{-2}.

- The excimer laser annealing was performed in a vacuum, pulse duration of 66 ns, single pulsed, the optimal energy range is 900-1000 mJ/cm^2.

- Before the standard metallization process, a 4 min 0.55% HF dip etch step is performed to remove the native oxide before the metallization.

- Contacts are alloyed at 400 °C for 30 min in forming gas.

Figure 3.12 shows a TEM image of a laser annealed As^+ implantation close to the window edge. Crystallinity is very high quality in the regrown region. Increased surface roughness is visible due to the laser annealing. Close to the window edge a small dislocation arose probably due to stress effects during the regrowth.

Higher leakage caused by low implantation tilt angles is only visible at the As^+ implants shown in Fig. 3.13. P-type diodes have in general more ideal slopes in the medium current forward regions, diode edges are not as vulnerable and non-ideality here only arises due to the residual implantation defects. While the laser energy densities above the melt limit have a small effect on the diode characteristics, shown in Fig. 3.14, they apparently affect the resistance of the laser annealed sheet. The sheet resistance increases with the laser energy density as the melt depth and therefore the highly active sheet thickness increases (Fig. 3.15). As the high dose implants have a sharp a/c interface, the laser energy window gets apparent when the melt depth reaches this interface, although is step in laser energy density is large ($>$10%). The higher sheet resistance of the 30° tilted implants is a consequence of the shallower amorphous depth, therefore results in a shallower junctions. BF_2^+ implants are slightly deeper than As^+ implants annealed at the same energy density, as sheet resistances are somewhat lower.

The contact resistivity measurement results are shown in Fig. 3.16. A minimum contact resistivity of about 1.2×10^{-7} ohm-cm^2 is reached for laser energies from about 800 to 1050 mJ/cm^2. For both 7° and 30° tilts an increase of contact resistivity is seen at the lowest energy where the melting is limited and at high energies where the surface roughness is large. Contact resistivity also increases at the highest energies as the surface roughness increases.

3.4 Conclusions

Ultra-shallow n^+p and p^+n diodes by direct implantation in contact windows and using only ELA for dopant activation are fabricated with near-ideal diode characteristics, and sheet resistances below 1 kohm/sq. The diode quality is shown to be very dependent on the surface/edge isolation. The ELA diodes are very closely aligned to the contact window, and the surface morphology and diode edge isolation have a decisive influence on the diode quality. The most ideal diodes are fabricated with thermal oxides at the interface. Diodes with reproducible ideality factors in the range 1.1 – 1.3 are demonstrated for an isolation stack of 300 nm TEOS on 30 nm thermal oxide in combination with a 100 nm Al reflective layer. Here the residual implantation damage causes non-idealities in the diode characteristics. The alignment of the implantation to the contact window edges can be a major issue but becomes less critical if a large-angle tilted implant is performed. This is apparent for the very shallow As^+ implants, for which going from a 7° to a 30° tilt results in improved ideality factors and lower perimeter leakage of the n^+p diodes. At laser energies high enough to modify the surface topology, the diode characteristics deteriorate and the contact resistance increases. However, the applicable laser energy processing window is quite large and found to be about 900 to 1000 mJ/cm^2. Surface morphology has also an influence shown by slightly increasing contact resistance at high energies. Otherwise a wide laser energy range results in good quality diodes: the optimal energy range is only defined by the lowest scatter of the idealities.

Chapter 4

Deactivation and junction leakage in the vicinity of laser annealed implantations

4.1 Introduction

The laser annealing thermal cycle occurs within a microsecond, making solid state dopant diffusion negligible. Therefore, implantation damage located deeper than the amorphous/crystalline interface will not be annealed and this can have a detrimental effect on the electrical behavior of devices fabricated with laser annealed junctions.

Studies of the modification of electrical characteristics due to residual implantation defects are reported as early as devices were first fabricated with implantations [Bull et al., 1979] and residual damage is connected with excess generation-recombination centers, reduced lifetime, and early breakdown voltages [Holt and Yacobi, 2007]. Increased non-ideal currents in high frequency silicon-on-glass (SOG) transistors [Lorito et al., 2006] have been observed, and reduced varactor breakdown voltage and increased series resistance in SOG varactors [Buisman et al., 2005]. In both devices back-wafer contacts were made after the wafer transfer. Therefore, the contact implants could only be activated by laser annealing due to the thermal limitations of the adhesive and glass wafer. Although the fabrication of laser annealed implants was optimized with diodes for ideal electrical behavior, as discussed in the previous chapter, due to its very low thermal budget and short timescale ELA is not able to anneal out all

implantation induced defects. This also applies to excess point defects which penetrate far below the amorphized implanted region [Larsen et al., 1996] and the melt depth.

Implantation-induced damage has been extensively studied by analytical techniques, such as deep level transient spectroscopy [Leveque et al., 2003] or positron annihilation spectroscopy [Burtsev et al., 2004]. In these techniques elevated temperature treatments are not applied. Another approach is to detect non-equilibrium dopant redistributions caused by defect ripening/dissolution by secondary ion mass spectroscopy on transient enhanced diffusion (TED) of buried boron markers after high temperature annealing [Jain et al., 2002]. The latter technique has been also used to show that laser annealing may introduce defects in the crystal lattice [Mannino et al., 2005]. TED has been also observed after post annealing of laser annealed implantations [Jones et al., 1999]. Though this truly useful technique gives valuable information about the dopant locations, and indirectly the defect locations, it gives no information about the electrical activation. Also, these techniques give information after high temperature annealing, which alters the defect concentration in silicon and mixes implantation and diffusion effects.

Dopant segregation in implantation background layers was investigated by SIMS [Kim et al., 2000b] and computer modelling of SIMS data [Lo et al., 1996a], showing that redistribution is induced by dissolution of implantation defects during annealing.

It is effectively only shown by spreading resistance profiling to determine the deactivated dopants in background layers, that self-interstitial defects are injected much deeper than the implantation range [Giannazzo et al., 2004, Larsen et al., 1996]. However, non-doping implantations were used in very low concentration doped background layers.

In this chapter, we investigate the degradation in the electrical characteristics of bipolar test structures where the emitters have received an implantation that is only annealed by the laser. Consequently, all the implantation and doping parameters are of a practically useful range. The effects of the residual ion-implantation defects on the junction properties and in the base region are investigated, and the amount and location of the damage is correlated with the implantation and laser annealing parameters.

4.2 Experimental procedures

The fabrication of an n^+p type ultrashallow junction is shown in Figure 3.1. Such laser-annealed junctions were integrated as emitters of bipolar test transistors described in Section 2.3.2.

The starting material is 4 inch (100) 2-5 ohm-cm p-type silicon wafers. Buried collector regions are implanted, annealed and a 1 μm epitaxial layer is grown.

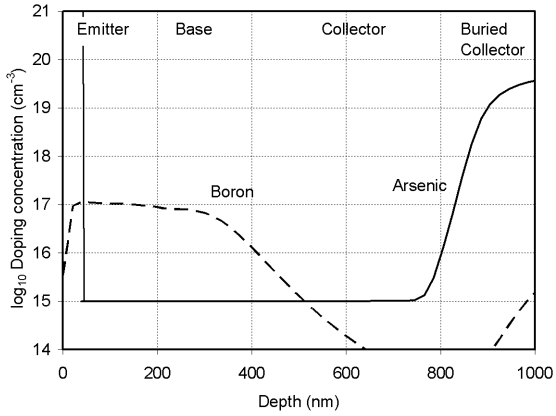

Figure 4.1: Schematic of the doping profiles in the intrinsic transistor region.

A p-type background layer was implanted with a combination of B^+ implants using different energies with a total dose of 3.4×10^{12} cm^{-2} to reach a uniform concentration of 10^{17} cm^{-3} to a depth of 300 nm. Furthermore, junction isolations and contacts to the buried layers are implanted. All the background implantations were performed through a 30 nm thermal oxide layer and activated by 1 min annealing at 1050 °C.

The subsequent processing is as in Section 3.4. Forming the shallow junction, As^+ ions were implanted with 5 keV. Four different diodes were created with implantation doses of either 2 or 3×10^{15} cm^{-2} with tilt angles 7° or 30°, the latter with 8 equal rotations.

The doping profile of the created NPN transistor is shown in Fig. 4.1.

4.3 Results

4.3.1 Ideality of the junctions

Forward and reverse Gummel plots are measured to characterize the B–E junction, the base region and the B–C junction in the devices having different emitter implantations annealed at 900 mJ/cm^2. Results are shown for the emitter size dependence of the ideal and non-ideal currents, and the temperature dependence of the non-ideal currents.

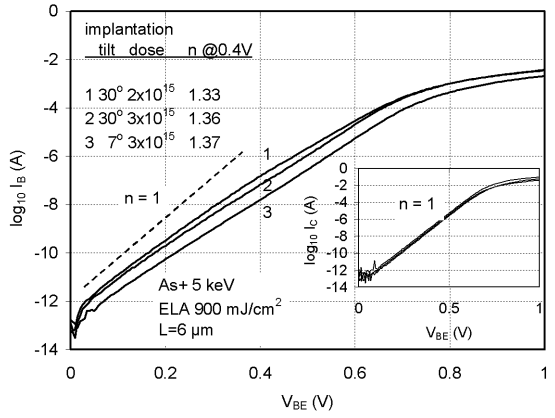

Figure 4.2: Base current of the forward Gummel plots for different emitter implantations laser annealed at 900 mJ/cm^2. $V_{BC} = 0$ V. The collector current is shown on the inset. The base leakage is represented by the minimum n measured at 0.4 V for each implant condition. The emitter length was 6 μm.

E–B junction

Forward Gummel plots are shown for various emitter implants laser annealed at 900 mJ/cm^2 in Fig. 4.2. The base current, I_B is the hole current flowing through the forward biased E–B junction, and shows large leakage. The ideality factors are tabulated for all the curves measured in the low-medium current regime at 0.4 V. The emitter junction leakage can be explained by non-annealed implantation defects remains after the laser annealing in the proximity of the junction, and these defects provide extra sources of generation-recombination currents. During the implantation large amounts of lattice defects are generated, as the foreign atoms collide with the lattice atoms causing recoil. As the laser only anneals the surface, damage caused by interstitials that have diffused deeper than the heat affected zone will not be annealed out. Indeed, the ideality factor increases with the implantation dose as more defects are injected during the implantation. Non-idealities are slightly decreased with the increased implantation tilt angles as less defects are directed towards the bulk.

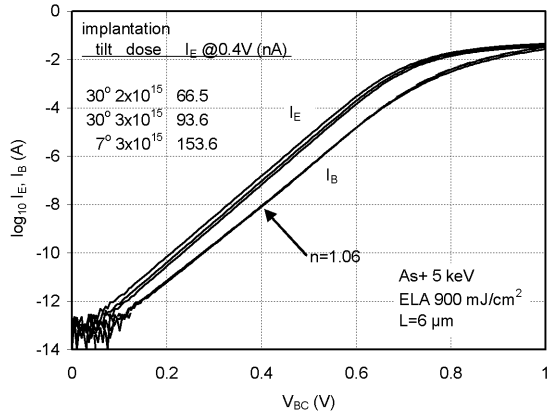

Figure 4.3: Reverse Gummel plots of devices made with different emitter implants laser annealed at 900 mJ/cm^2. $V_{BE} = 0$ V. The emitter length was 6 μm.

B–C junction

The B–C junction is located more than 300 nm away from the silicon surface, so it is expected to be less influenced by the emitter fabrication. From the reverse Gummel plot as seen in Figure 4.3, the behavior of the forward biased base-collector junction can be evaluated. The base current shows near-ideal behavior, and is apparently not affected by the emitter fabrication. The collected current I_E increases, as will be discussed in 4.3.2.

Emitter size dependence

The size dependence of the currents at 0.4 V on the forward and reverse Gummel plots are shown on Figure 4.4. The currents are bulk currents: they show linear dependence on the emitter length, which is linearly proportional to the junction area. The perimeter component is very low, about 10 nA. The I_B of the forward Gummel plot, which depends on the properties of the laser annealed junction, shows somewhat larger scatter than the other currents due to the laser treatment and the residual ion-implantation defects.

However, the I_B of the reverse Gummel plots shows no dependence on the base-collector junction area. This suggests that the most of the current is collected along the

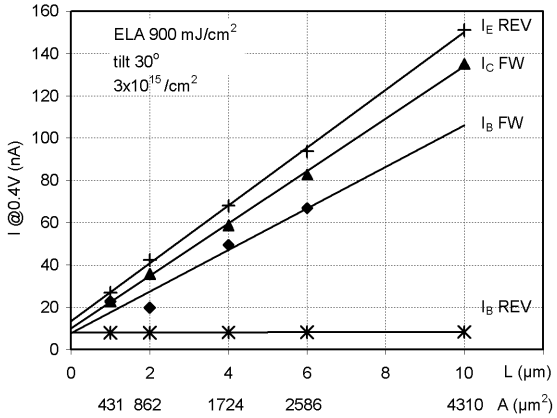

Figure 4.4: Currents of the forward and reverse Gummel plots measured at 0.4 V as a function of the emitter size. The emitter was As^+ implanted with a dose of 3×10^{15} cm^{-2} under 30°, and laser annealed at 900 mJ/cm^2.

the perimeter of the junction that extend beyond of the emitter implantation window.

Temperature dependence

The temperature dependence of the base currents at the laser annealed junction is shown in Fig. 4.5. The forward Gummel plots are measured as a function of temperature, and only the base current is plotted. Ideality factors the currents at 0.4 V are shown in Fig. 4.5. As the temperature increases the diffusion current contribution increases over the generation-recombination current, therefore the ideality factor decreases.

4.3.2 Base properties

As the emitter fabrication is the last implantation step in the processing and it is introduced into a defect-free thermally annealed implanted silicon, and no high temperature steps are performed after the laser annealing, residual defects can be found in the base region and beyond. That the emitter fabrication has an effect on the base can be seen in the Gummel plots: the collector current of the forward Gummel plot and the emitter current of the reverse Gummel plot depend on the base's Gummel number. Comparing the emitter currents in Fig. 4.3. for the different emitter implantations, it seems

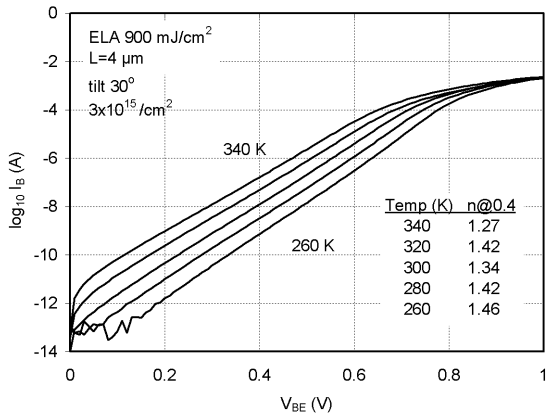

Figure 4.5: The base current measured of the forward Gummel plots as a function of V_{BE}, measured at temperatures from 260 to 340 K in steps of 20 K.

that the Gummel number of the base, which is inversely proportional to I_E, is effected by the emitter fabrication. Further measurements are carried out to determine the effects on the base: the resistance/conductance in the intrinsic base is measured, which is dependent on the electrically active dopant (boron) concentration and the hole mobility; and capacitance-voltage measurements of the E–B and B–C junctions are carried out from which the electrically active boron concentration is calculated. In the latter measurement, results are not dependent on the hole mobility.

Conductance and pinch-off

The sheet conductance of the intrinsic base is calculated from Eq. 2.17 and plotted while narrowing the base by increasing the emitter reverse biasing in Figure 4.6. The decrease of the pinch-off shows that the integral base doping decreases with increasing the emitter implant dose. Note that the emitter junction depth can be slightly larger due to the increasing dose, therefore the depletion region into the base can be slightly larger, also causing an increase in the measured sheet resistance. However this effect is estimated to have an impact of less than 10%.

The punch-through breakdown is very sensitive the emitter fabrication process variations. Therefore the effect of the laser annealing might be observed. However, the effect of the laser annealing can only be seen clearly for the 7° 3×10^{15} cm^{-2} implan-

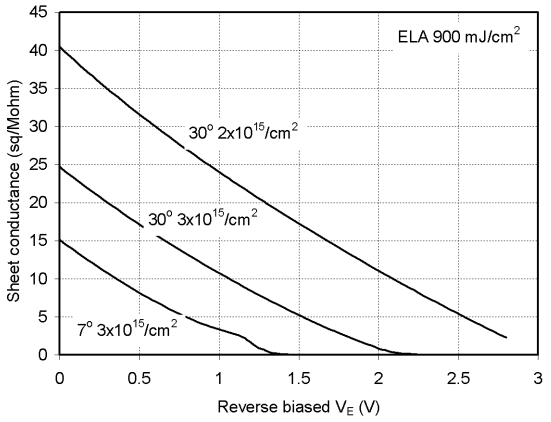

Figure 4.6: Sheet conductance in the intrinsic base while depleted from the emitter compared for different emitter implantations laser annealed at 900 mJ/cm^2.

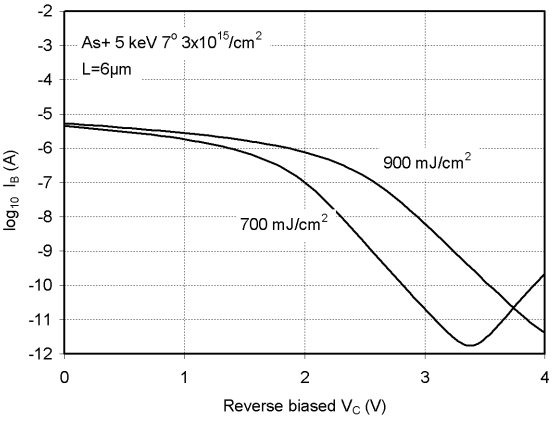

Figure 4.7: Pinch-off vs laser energy density measured by depleting the base from the collector. $V_{B-B'} = 5$ mV. The emitter was As$^+$ implanted with a dose of 3×10^{15} cm^{-2} under 30°, and laser annealed at 700 or 900 mJ/cm^2.

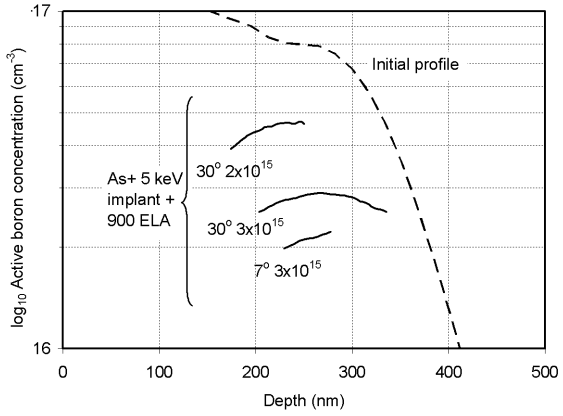

Figure 4.8: Active boron concentration profiles extracted from C–V measurements at different laser annealed emitter implants annealed at 900 mJ/cm^2. The initial profile was calculated by *TSUPREME4*.

tation, where the most defects are generated due to the high dose implantation, and the pinch-off voltage is the lowest. In figure 4.7, the curves are shown for the low (700 mJ/cm^2) and optimal laser energies (900 mJ/cm^2), suggesting that some defect repair occurs with increasing laser energies. Note, that pinch-off voltages are larger than in Fig. 4.6, since the base narrowing was driven from the collector.

Base doping deactivation

The active doping concentrations have been determined by capacitance-voltage doping profiling and are shown in Fig. 4.8 for laser annealing at 900 mJ/cm^2. The active dose in the base without the emitter implants is 3.4×10^{12} cm^{-2}, which is reduced by 78% in the case of a high dose emitter implant. High doses and low tilt angles caused larger levels of deactivation. This deactivation in the base is the result of silicon interstitials that diffuse beyond the end-of-range zone displacing boron atoms from substitutional sites and forming boron-interstitial pairs [Larsen et al., 1996].

Deactivations are shown for increased background doping levels in Fig. 4.9. Boron implanted to a concentration of 10^{18} and 10^{19} cm^{-3} was annealed at 1050 °C for 1 min. A shallow arsenic implantation was then made with 5 keV, 3×10^{15} cm^{-2}, 30° tilt, and laser annealed at 900 mJ/cm^2.

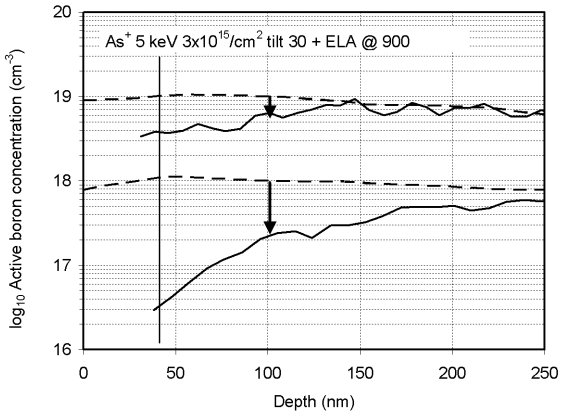

Figure 4.9: Active boron concentration profiles measured by SRP (solid lines) after an implant of 5 keV As^+ 3×10^{15} cm^{-2}, 30° tilt, laser annealed at 900 mJ/cm^2 with a 25 ns pulse. Initial active concentrations calculated by *TSUPREME4* are also shown (dashed lines).

Table 4.1: Boron background deactivation under As^+ 5 keV emitter implants laser annealed at 900 mJ/cm^2.

Measurement technique	Background conc. (cm^{-3})	Background dose (cm^{-2})	Emitter implant tilt (°)	Emitter implant dose (cm^{-2})	Deactivated B^+ dose (cm^{-2})	Deactivated B^+ (%)
C–V	10^{17}	3.4×10^{12}	30°	2×10^{15}	1.41×10^{12}	42
C–V	10^{17}	3.4×10^{12}	30°	3×10^{15}	2.19×10^{12}	64
C–V	10^{17}	3.4×10^{12}	7°	3×10^{15}	2.66×10^{12}	78
SRP	10^{18}	3.4×10^{13}	30°	3×10^{15}	1.9×10^{13}	56
SRP	10^{19}	3.4×10^{14}	30°	3×10^{15}	9.0×10^{13}	26

Active boron concentration profiles were measured by spreading resistance profiling (SRP), therefore depletion effects are not disturbing the measurement below the shallow junction (50 nm) due to the material removal of the surface region with bevelling.

Measured values are summarized in Table 4.1 and they show strong dose dependency. As the emitter implantation dose increased by a factor 1.5 from 2 to 3×10^{15} cm^{-2}, the deactivated dose increased by the same factor. In the case where the background doping is increased tenfold up to 10^{18} cm^{-3}, the deactivated dose increased approximately the same factor. Further increasing the background doping $10\times$ to 10^{19} cm^{-3} will lead to a relatively lower relative increase ($5\times$) in the deactivations. In this case, all interstitials are "used", showing that the boron deactivation efficiency (number of boron deactivated by an interstitial) of a 3×10^{15} cm^{-2} dose of As^{+} implanted at 30° is about 0.03. Interstitials are more readily captured and not penetrate as far, therefore the deactivation decays in a shorter distance as it is seen in Fig. 4.9.

Increasing the tilt angle from 7° to 30° reduces the vertical energy component by 13%, resulting in slightly less and shallower damage.

Mobility

The mobility of the base was calculated as a function of the depth for different emitter implantations laser annealed at 900 mJ/cm^2 (Fig. 4.10). For the calculations the data for the sheet conductivity in Fig. 4.6 and the active doping in Fig. 4.8 were combined by eq. 2.20. At low emitter implantation dose the mobility in the base remains about at its original value for the 10^{17} cm^{-3} boron doped base. At higher emitter implantation dose the mobility increases with the lower amount of active dose in the base, but slightly lower then than expected as the electrically deactivated boron retards the increase in the mobility. This suggests that defects introduce deep levels in the band, therefore compensating active dopants, as well as at large emitter implant doses actual deactivations occur causing increase in the mobility.

4.4 Discussion

4.4.1 Diffusion and activation effects

Repair of the damage introduced by ion-implantation can be achieved by thermal annealing, whereby diffusion and activation of the dopants, and defect dissolution can be induced. To minimize diffusion for shallow junction formation, low thermal budget annealing strategies are used, where high temperature, short time anneals are favored

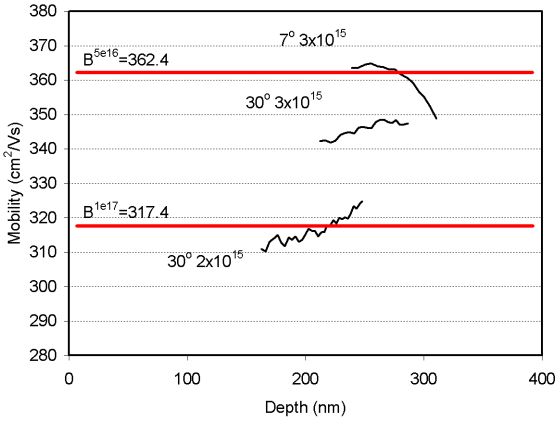

Figure 4.10: Measured hole mobility of the base as a function of depth for different As^+ emitter implantations laser annealed at 900 mJ/cm^2. Reference values for the hole mobility are given for the doping level of 10^{17} cm^{-3} and 5×10^{16} cm^{-3} and shown by the thick lines.

in order to avoid transient enhanced diffusion. Melting laser annealing is considered at the ultimate end of this scale, but as thermal budgets decrease, ion-implantation damage cannot be fully repaired. Table 4.2 summarizes the chemical mechanisms that play a role, and focuses on favored case of ELA implants in boron background doping.

Ion-implantation creates a large amount of damage in the crystalline lattice through collision cascades initiated by the dopant and sustained by recoiled atoms. As only a very small amount of implanted arsenic dopants might stop at substitutional positions, the activation is very low. The created Frenkel-pairs annihilate at the initial stage of annealing or even after the implantation, after which a net excess of interstitials remains, which causes supersaturation at the tail of the doping. Nevertheless, a smaller amount of interstitials penetrate farther than the end-of-range (EOR) deeper into the bulk of silicon, which in the case treated here is boron doped with full activation. These interstitials react with B atoms in the background layers. The reaction between a silicon interstitial I and a substitutional boron atom BS can be described as pairing or kick-out mechanisms: $I + BS \rightarrow BI$ or $I + BS \rightarrow B_I$, respectively, where BI is a boron-interstitial pair and B_I is boron at an interstitial position. The reaction is dose dependent, and it can be described by

Table 4.2: Summary of the mechanisms.

Stage	As^+ implant	B background	Defects
1. Implantation	Most As^+ ions are inactive, some stop at active position.	Deactivation occurs, which shows dose dependency.	Frenkel pairs develop, with net I super-saturation towards the dopant tail. Small number of I escapes deeper depends on the background doping.
2. Laser anneal	Uniform box-shaped profile due to high diffusivity in the melt. Activation above the solid solubility due to solute trapping during quenching.	No dopant diffusion occurs. Deactivation level is still high, some reactivation occurs in the heat affected zone.	Considerable amount of defects remain beyond the melt. No time for defect clustering.
3. Additional anneal	Enhanced diffusion in the tail, clustering at high concentrations and deactivation occurs. Remaining activation depends on annealing conditions.	Redistribution due to diffusion towards the EOR. In EOR immobile zone develops due to clustering, if concentration is high.	Dopants and/or defect clustering occurs first, then dissolution.

$$C_{BI} = KC_I C_{BS} \tag{4.1}$$

where C_{BI}, C_I, and C_{BS} are the number of boron-interstitial pairs, self-interstitials and substitutional boron atoms, respectively, and K is a constant, KC_I is much smaller than 1. [Larsen et al., 1996] shows by spreading resistance profiling that the deactivation is dependent on dose, atomic weight and interstitial trapping, and considers that deactivation is a result of pairing. [Giannazzo et al., 2004] concludes through scanning capacitance microscopy experiments, that the deactivation is due to an electrical compensation effect, arising from deep levels in the band gap. Both authors use low implant doses and background concentrations, and the compensation effect results in apparent dopant type inversion. In the measurement results shown in Fig. 4.10, the mobility increase is a result of a discrepancy in the sheet resistance and capacitance measurements suggesting that both effects play a role. [Cristiano et al., 2006] shows that in the case of boron-interstitial cluster (BIC) generation the mobility is inversely proportional to the active dopant concentrations as in eq. 2.20, and not affected by the interstitial concentration.

The laser energy density used for the annealing has two effects: 1) the primary effect is that the shallow As^+ implantations are annealed, 2) a secondary effect is the reactivation of the deactivated dopants in the background within the heat affected zone. The optimal energy range for the annealing can be found, starting where the energy is large enough to fully melt the amorphized region. The sheet resistance of the recrystallized region decreases as the melt depth increases. The difference in the melting point of the amorphous Si and c-Si gives the self limitation to this process and determines the processing window, which is around 10% laser energy variation. As the energy further increases, the crystalline Si melts too. A slight overmelt ensures a good seed for the regrowth and beneficial for defect repair. However, surface flatness deteriorates as the surface roughness increases with the increasing laser energies [Burtsev et al., 2004]. At large energies the increase of the roughness can deteriorate the electrical performance.

The laser annealing activates fully the implanted As^+ ions but only has a minor effect on defects in the background layer as they are located below the a/c interface. Only a small amount is dissolved close to the heat affected zone, since the heat pulse decays towards the bulk. In case the laser annealing is repeated, i.e. multiple shots are used, more defects are repaired [Sharp et al., 2006].

Laser annealing is fast enough to avoid transient enhanced diffusion of the dopants. However, as not all the defects are annealed out, arsenic deactivation at the high concentration regime and TED of the arsenic tail would be present in a furnace post annealing, and [Jones et al., 1999]. Post-annealing has not been studied in this work because of thermal limitations in the targeted processes. Nevertheless, it is still rele-

vant to mention post-annealing as most knowledge about the presence of defects and defect evolution has been gathered indirectly through their influence on diffusion during thermal annealing. The presence of very high interstitial concentrations generated by ion-implantation is well known to cause transient enhanced diffusion at the early stages of annealing [Jain et al., 2002]. This is due to an interstitial flux caused by the interstitial defect dissolutions.

If the huge interstitial supersaturation overlaps a boron doped region, a band of boron-interstitial clusters can nucleate, some already during implantation or at the very early stages of annealing [Mannino et al., 2000]. They can form well below the solid solubility of boron, at about 1/10 of the solid solubility at the given temperature [Cowern et al., 1990]. Redistribution of the background doping is driven towards the EOR due to the interstitial flux [Lo et al., 1996a] and the electric field might also play a role [Kim et al., 2000b]. Within the EOR region, dopant or dopant–interstitial clustering can occur, and this causes deactivation. The amount of deactivation depends on both the number of generated excess interstitials and the amount of boron in the background layer. [Mannino et al., 2001] shows that deactivation due to BIC formation increases linearly with the implantation generated interstitials until it saturates at around 75% at high interstitial densities. The linear dependence would suggest that the number of deactivated boron is an absolute amount, that is, it would not depend on the number of boron dopants in the background layer. If deviation occurs, it can be explained as the pairs can have different sizes ($B_n I_m$) [Pelaz et al., 1997].

4.4.2 Effect of the ELA implant on an ideal BJT

Laser annealed implants are often used to create a contact region. In such cases a thermally annealed, defectless junction is in the vicinity of the laser annealed implantations. In the wafer transfer process developed in DIMES [Nanver et al., 2004], the distance of the junctions from the contact implant are located more than 400 nm. Within NPN structures, such as described in Fig. 4.1, the B–C junction is located at such a distance from the emitter, and at depths where no deterioration is observed from the emitter fabrication. Two scenarios have been studied: introduction of and ELA implant into a a) high concentration shallow region, or b) low concentration region. The scenario is depicted in Fig. 4.11.

An NPN transistor is shown in Fig. 4.11a with a thermally annealed emitter implant (As^+ 7.5×10^{15} cm^{-2} 40 keV), annealed at 950 °C in 20 minutes resulting in junction depth of about 200 nm. The ELA implant (As^+, 5 keV, 2×10^{15} with tilt angels 7 or 30 degrees). The results are summarized in Fig. 4.12. The junction (bulk) leakage scales with the size of the emitter width. This can be explained by the fact that the real junction area consists the perimeter (vertical section) of the thermally annealed junction, about

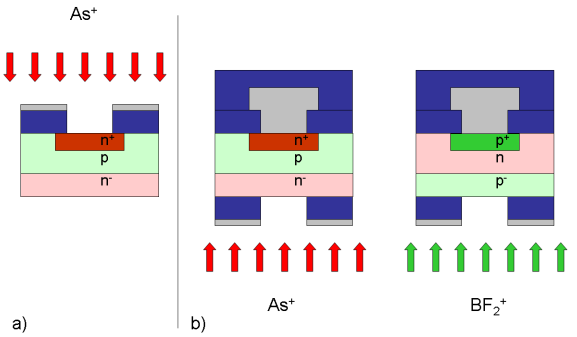

Figure 4.11: Experimental configurations for ELA implant effect on the defectless intrinsic transistor: ELA implant into a close vicinity of a junction a) into a highly doped shallow emitter region, b) into a low doped collector region as in [Lorito et al., 2006].

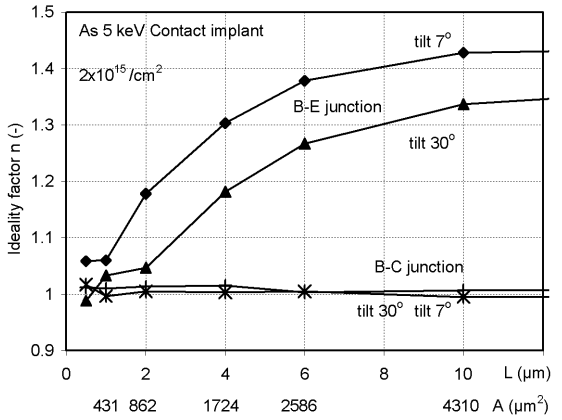

Figure 4.12: Junction ideality of a contact implant as a function of the emitter size for case a) in 4.11. Ideality factors of the base current are extracted from the forward and reverse Gummel plots, with 0.4 V on the forward biased junction.

200 nm deep, and it remains unaffected, contributing to the ideal current component.

This perimeter component is dominant at small emitter sizes, and gradually overtaken by the non-ideal component as the emitter size increases. The effect of the tilt angles is more prominent even at this implantation dose. The 7° tilted implants are injecting interstitials straight into the intrinsic region of the transistor distributing them rather uniformly laterally over the junction, leaving the vertical sides intact. At increased tilt angles of 30 degrees, a similar number of interstitials determined by the total dose are distributed over a much wider region, hitting larger portions of the sidewalls at much lower dose (1/8 to 1/4 due to the rotations), while the full dose region does not cover all the intrinsic region, moreover the vertical component of the implantation energy is reduced, therefore better overall ideality is obtained.

The moderate amount of damage detected in NPNs can be caused by the fact that deactivation and leakage are correlate not only the amount of injected interstitials but the amount of reacting species (trapping), which in these structures are implanted boron in relatively low dose. The typical interstitial to boron doses are about 1000:1.

The laser annealed contact implants through wafer transferred SOI NPN and PNP transistors were studied by [Lorito et al., 2006]. The effect of contact fabrication was shown in the non-ideal behavior of the emitter-base junction, which is located at a distance of 740 nm from the collector contact. The thermally annealed boron dose in a PNP transistor before contact formation at the collector was 1.5×10^{13} cm^{-2}, while at the emitter it was 5×10^{15} (BF_2, 10 keV). The collector contact was implanted by BF_2^+ at 5 keV 10^{15} cm^{-2} after the wafer transfer. This combination results in interstitial to boron doses to and below 1:1 at the collector side, therefore the characteristic decay length is much deeper. Interstitials can be trapped at the emitter. This resulted in ideality factors increasing to over 1.4 at a junction depth 740 nm below the contact implant.

4.4.3 Methods of suppressing defects

The quest for shallow junction formation introduces a trade-off in between activation, diffusion, and defect repair. Low energy implantations in combination with low thermal budget annealing will result in high activation, small or negligible diffusion and high leakage. Mostly, the bulk leakage is a result of interstitial defects. Most research is directed towards defect engineering, e.g. pre-amorphization with Ge is used to shift EOR damage as well as to reduce channelling [Jones and Ishida, 1998]. Co-implantations, where interstitial-trapping non-charging dopants such as C and/or F are also implanted, can retard diffusion, so somewhat higher thermal budgets are allowed [Timans et al., 2006]. Deactivation of the background doping also shows that the dopant atom can be an interstitial trap, therefore the background profile can be tailored to use up intersti-

tials. Vacancy engineering is an alternative, where by using non-doping implants and tuning the implantation parameters, a vacancy rich zone is created in a way that it will overlap the EOR damage created by the subsequent shallow implant, therefore defect annihilation occurs [Smith et al., 2006, Bruno et al., 2008].

In conjunction with laser annealing, a multipulse approach can be beneficial for defect dissolution [Sharp et al., 2006], however other effects introduced by the laser should be considered, such as surface degradation.

Many research groups are trying to substitute ion-implantation with laser doping either from gas precursor [Kerrien et al., 2002] or from a spin-on [Lo et al., 1996b] or CVD deposited [Popadic et al., 2007] dopant source.

4.5 Conclusions

In order to evaluate residual implantation damage after laser annealing in devices, ring shaped NPN test structures were fabricated with As^+ implanted and laser annealed emitters. The degradation of the transistor regions under different emitter implantation parameters and optimal laser annealing were measured and analyzed. Bulk damage stemmed from non-annealed excess interstitials reaching depths larger than 300 nm under the emitter. They cause junction leakage and electrical deactivation in the active transistor region. The residual damage can be reduced by decreasing the implantation dose or using tilted implants which would effectively decrease implantation of the bulk.

The low energy, high dose shallow implantation is performed in defect-free background layers: the implant damage thus overlaps doped layers. As laser annealing is a surface annealing method, a considerable amount of residual implantation damage remains in the background layers below the recrystallized region, deeper than the EOR damage. This region does endure high temperatures as the heat pulse decays towards the bulk, but the short times in the microsecond range only allow activation and no diffusion.

The amount of residual damage scales with the implantation dose. The residual damage appears in the electrical behavior of the transistors as junction leakage at the B–E junction where defects act as recombination centers in the depletion region and cause deactivation in the background layers due to the reaction of the injected interstitials with the substitutional boron through kick-out and pairing reactions. Electrically, the pair introduces a compensational level in the band gap at lower I/B ratios, while as the I/B ratio increases, the actual deactivation appears also as an increase in the mobility.

The laser annealing activates the implanted As^+, and reactivates small amounts of boron close to the heat affected zone.

Chapter 5

Laser annealing and Si/Ge/C strained layers

In this chapter, the integration of a laser annealed implantation together with strained layers is evaluated. NPN HBTs were fabricated with arsenic implanted laser annealed ultrashallow emitters on top of a Si/SiGe/SiGe:C thin epitaxially grown base highly doped with boron. The sheet resistance in the base is measured for various emitter implantation dose and tilt angles and laser annealing conditions.

Essentially the thin base acts as a boron marker, such as is often used in TED experiments in combination with SIMS measurements to determine its chemical doping concentration. In this work, the measured electrical properties are related to the electrically active dopant or carrier concentrations. The boron peak is narrow and located very close to the top surface. Therefore, it is very sensitive to deactivation due to the emitter implantation. The active concentration in the base is also dependent on the heat pulse generated by the laser annealing, and is therefore a measure of any reactivation due to laser annealing.

5.1 Experimental procedures

A schematic of the device structure is shown in Fig. 5.1. A buried collector layer was implanted and annealed on p-type wafers, above which a pedestal collector was formed in an intrinsic epitaxially grown layer. The boron in-situ doped base structure shown in Fig. 5.2 was formed by a subsequent epitaxial step carried out at 700 °C to

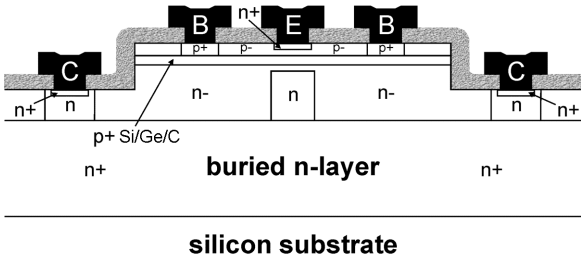

Figure 5.1: Schematic of the Si/Ge/C HBT device structure.

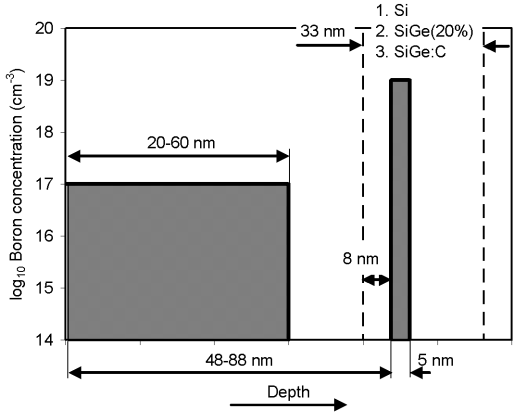

Figure 5.2: Schematic of the boron profile grown epitaxially at 700 °C. The highly doped peak is confined in either (1) Si or (2) SiGe or (3) SiGe:C.

avoid outdiffusion of the boron dopants. Three sets of wafers were fabricated with the following variations in the base region:

1. Silicon control structure with doping in the boron peak of 2×10^{19} cm^{-3}. The distance of the peak from the surface was varied from 48, 58, 68, 78, 88 nm by increasing the thickness of the boron doped top layer.

2. The highly doped peak, which was doped at about 5×10^{19} cm^{-3} was grown in a silicon-germanium (20% Ge) layer. The distance of the peak from the surface was varied from 48, 58, 68, 78, 88 nm by increasing the thickness of the boron doped top layer.

3. The highly doped peak was grown in a silicon-germanium (20% Ge) layer with or without carbon ($>10^{19}$ cm^{-3}) peak. The distance of the peak from the surface was kept at 68 nm. The doping in the peak was varied by applying different diborane gas flow of 60, 120, or 180 sccm during the epitaxy resulting in concentrations $\geq5\times10^{19}$ cm^{-3}.

The peak contains from 5×10^{12} to 5×10^{13} cm^{-2} boron.

The devices were separated with shallow trench isolation, and collector contacts were implanted. Laser masking was created as described in Section 3.3 with one exception: as thermal processes are limited to 700 °C to avoid outdiffusion of boron and relaxation in the germanium alloy, the 30 nm thermally grown dry oxide used for surface passivation was replaced with a wet oxide grown at 700 °C with a thickness of about 5 nm. To form the shallow junction, As^+ ions were implanted at 5 keV.

Implantation doses were varied from 0.5–1.5$\times10^{15}$ cm^{-2} with tilt angles 7°, 30°, 45° or 60°. Combinations of these implantations were also used. Laser annealing was performed with energy densities in the range of 600–1000 mJ/cm^2, with 25 ns pulse width. A reduced pre-metallization dip-etch time of 1 min was used before metallization. Wafers were alloyed at 400 °C in forming gas.

Sheet resistances of the base were measured either directly on Van Der Pauw structures or on a set of ring shaped transistors with two base contacts as described in Section 2.3.2. In the latter case the sheet resistance was calculated by Eq. 2.16.

5.2 Results

5.2.1 Transistor operation

An example of transistor characteristics is shown in Fig. 5.3 and Fig. 5.4 for a SiGe base doped to 5×10^{19} cm^{-3}, with an emitter implanted at 30° with a dose of 10^{15}

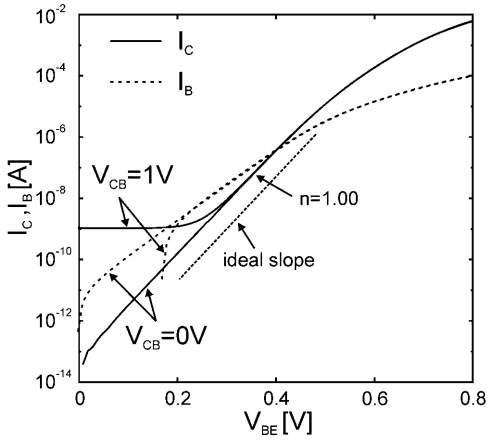

Figure 5.3: Measured forward Gummel plot of a SiGe HBT for $V_{CB} = 0,1$ V. The emitter contact area is 20 $\times$ 40 μm^2. Base doping: 5×10^{19} cm^{-3}, boron peak depth: 68 nm. The emitter was As$^+$ implanted at 30° 10^{15} cm^{-2} and laser annealed at 700 mJ/cm^2 [Lorito et al., 2008].

cm^{-2}, and laser annealed at 700 mJ/cm^2. Similar characteristics were measured for transistors made with the emitter implanted at tilt angles of 30° or 45°, low implantation doses of 0.5–1$\times10^{15}$ cm^{-2}, and laser annealing at energies from 600–800 mJ/cm^2, and the base located at least 68 nm from the surface.

5.2.2 Simulated hole profiles

The hole concentration profiles extracted from 1-D Medici simulations are shown in Fig. 5.5 for Si and in Fig. 5.6 for SiGe. The boron peak is doped to 2×10^{19} cm^{-3}. Initially, in the as-grown case, the holes fill up the intrinsic gap between the boron doped regions. When an arsenic doped emitter is added, to mimic the laser annealed junction, which is doped to 10^{20} cm^{-3}, 20 nm deep from the surface, the surface region is depleted of holes. The depletion width will extend to the germanium alloyed base, and it will be very insensitive to low voltage biasing unlike in the case of silicon base, where holes are not much confined in the as-grown base peak. This is true, when the base is highly doped, but if the doping is lowered to 2×10^{18} cm^{-3}, implementing a 10$\times$ deactivation, then charge balance depletes holes from the base, amplifying deactivation effects.

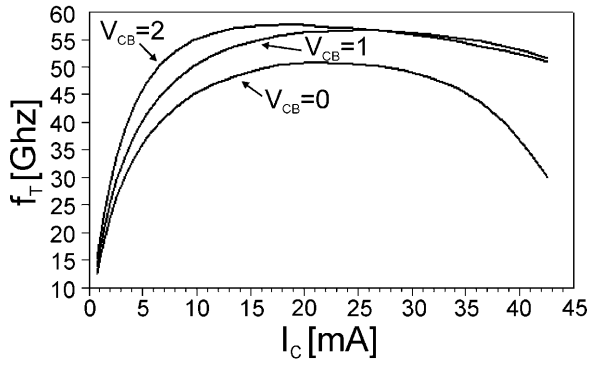

Figure 5.4: Measured $f_T - I_C$ characteristics of a SiGe HBT for different values of V_{CB}. The emitter contact area is 1×20 μm^2. Base doping: $5{\times}10^{19}$ cm^{-3}, depth: 68 nm. The emitter was As$^+$ implanted at 30° 10^{15} cm^{-2} and laser annealed at 700 mJ/cm^2 [Lorito et al., 2008].

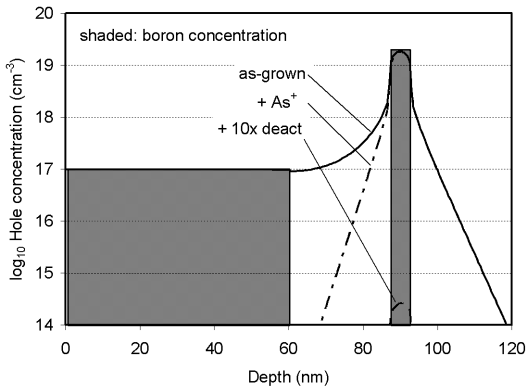

Figure 5.5: Simulated hole concentration in the pure Si base in cases: 1. as-grown; 2. after the emitter is fabricated w/o deactivation in the base; 3. after the emitter fabrication assuming $10\times$ boron deactivation in the base.

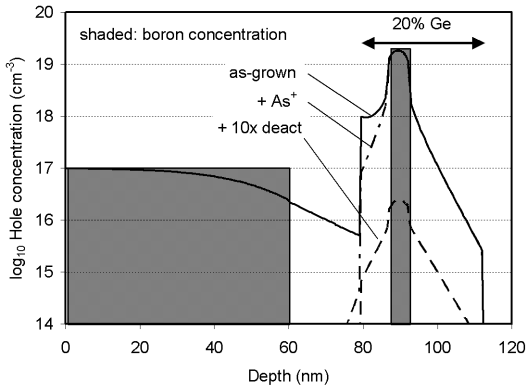

Figure 5.6: Simulated hole concentration in the SiGe base in cases: 1. as-grown; 2. after the emitter is fabricated w/o deactivation in the base; 3. after the emitter fabrication assuming $10\times$ boron deactivation in the base.

5.2.3 Sheet resistance in the intrinsic base

Initially, the dopants in the base are fully active because they are incorporated during epitaxy. The sheet resistance is primarily determined by the narrow peak due to its high doping level. Increase in the base sheet resistance can occur due to the emitter fabrication. In particular, the interesting effect is the creation of arsenic implantation induced defects in the base, which are not annealed out by the laser as described in Chapter 4. Silicon interstitials generated during the implantation react with boron in the base layer, and can cause deactivation. The deactivation causes increase in the sheet resistance, and this has been evaluated for devices with the base formed in Si, SiGe, and SiGe:C regions.

Pure Si base region

The base sheet resistance as a function of the laser energy density is shown in Fig. 5.7 in the pure silicon structure. The boron peak located at 88 nm is doped to 2×10^{19} cm^{-3}, the solid solubility level at 700 °C. This gives an initial sheet resistance of about 7 kohm/sq. Increasing the arsenic implantation dose results in increasing sheet resistance to more than one order of magnitude. The as-implanted case corresponds

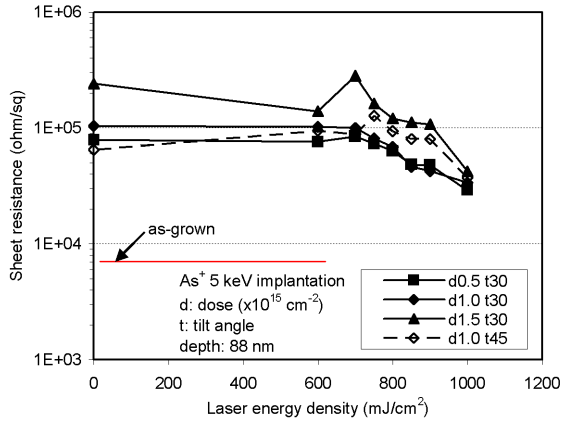

Figure 5.7: Sheet resistance in the pure Si base as a function of the laser energy density, and emitter implantation parameters. The base peak is located at a depth of 88 nm.

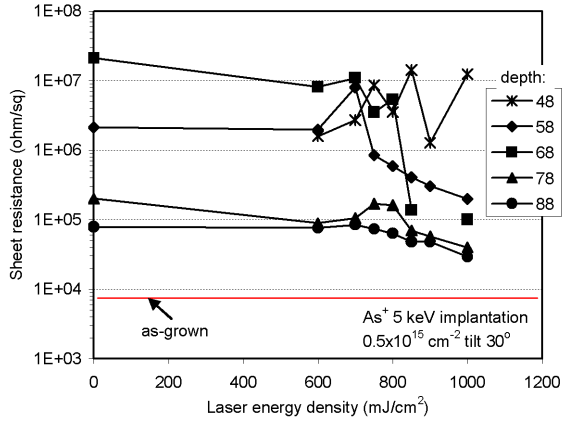

Figure 5.8: Sheet resistance of the pure Si base peak as a function of the laser energy density for peaks located at different depths from the surface, for the implant As^+ 5 keV at 30° tilt angle.

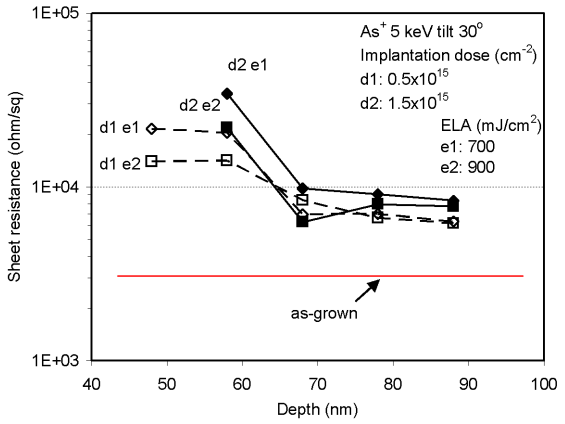

Figure 5.9: The emitter implantation dose influence on the base sheet resistance for low and high laser energy densities as a function of the distance of the boron peak from the surface in SiGe.

to 0 mJ/cm^2. With the increasing laser energy density, the sheet resistance decreases, to 1000 mJ/cm^2 by a factor of 2. Tilt angles of 30° or 45° do not show significant difference. Low implantation doses are beneficial, as long as they still are above the amorphization limit as required for well-controlled laser annealing. Moreover a certain dose is needed to achieve an emitter that is deep enough to sufficiently suppress hole injection.

A comparison of results for different depths of the boron peak are shown in Fig. 5.8. Increasing emitter implantation dose causes more deactivation of dopants, therefore the sheet resistance increases. Increasing laser energies reactivate dopants, and the effect of the heat pulse is more evident closer to the surface. Sheet resistance in the intrinsic base as well as scatter of the data increases as the boron peak gets closer to the arsenic implant.

SiGe base region

The as-grown sheet resistance dropped to about 3 kohm/sq for the SiGe samples. This is due to the higher boron incorporation in SiGe and there is possibly some mobility enhancement. Overall, a lower leakage made it possible to evaluate sheet resistance, and therefore also deactivation, as a function of the boron peak depth. The effect

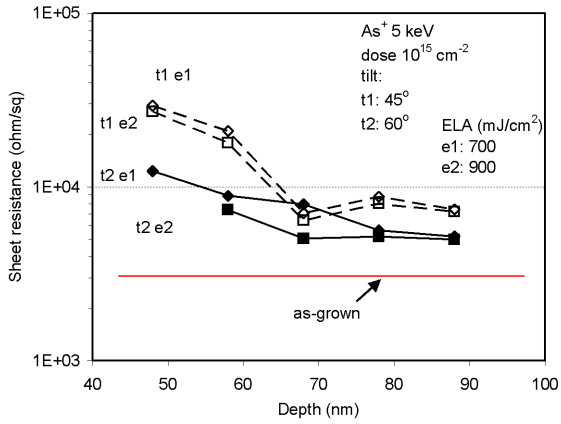

Figure 5.10: The emitter implantation tilt angle influence on the base sheet resistance for low and high laser energy densities as a function of the distance of the boron peak from the surface in SiGe.

of the emitter implantation dose on the base sheet resistance is shown in Fig. 5.9. The lower laser energy of 700 mJ/cm^2 is just above the melt onset, and it does not induce any significant reactivation in the base, while 900 mJ/cm^2 causes full melt and higher temperatures. For shallower boron peak locations, the larger deactivation with the increasing implantation dose as well as the higher levels of reactivation due to the increasing laser energy are obvious. At 48 nm, the high sheet resistance readings are less reliable: the peak is too close the end-of-range damage of the arsenic implant. Just 10 nm deeper, reliable data is obtained. With increasing depth, the sheet resistance decreases as the levels of deactivation decrease. At 68 nm or deeper, the boron peak is away from the end-of-range and only detects interstitials which are escaped from the highly damaged zone, and deactivation only slightly decreases with the depth. As the depth increases, the effect of the laser energy vanishes, therefore the reactivation decreases, because the temperature exponentially decreases with the depth, the boron peak is out of the heat affected zone.

The effect of the implantation tilt angle to the sheet resistance is shown in Fig. 5.10. The residual damage decreases with the increasing tilts.

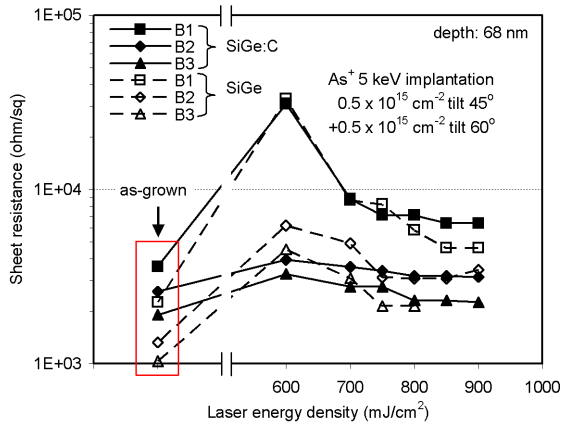

Figure 5.11: Evaluation of the base sheet resistance with varying boron dose and carbon incorporation in SiGe at combined arsenic emitter implantation as a function of the laser energy density. B1, B2, and B3 corresponds to 60, 120, and 180 sccm diborane flow.

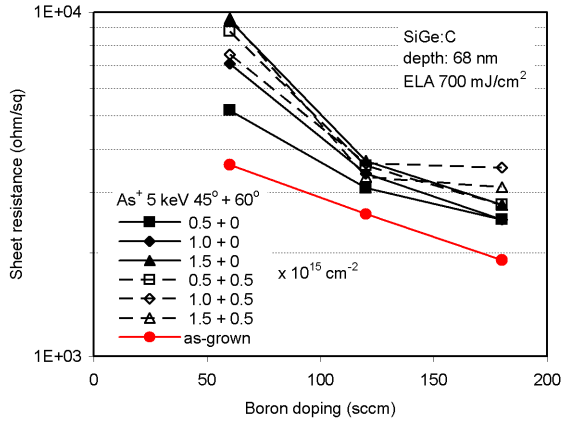

Figure 5.12: Comparison of the effect of the emitter implantations in the SiGe:C base sheet resistance as a function of the doping in the boron peak.

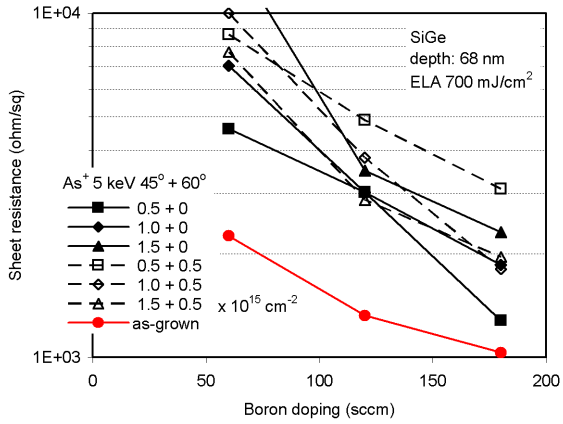

Figure 5.13: Comparison of the effect of the emitter implantations in SiGe base sheet resistance as a function of the doping in the boron peak.

SiGe:C base region

The boron peak was kept just out of the highly damaged region at 68 nm, and the boron peak doping and carbon incorporation is evaluated in Fig. 5.11. Carbon can act as an interstitial trap, therefore it can be used in suppressing defects. It will increase of the sheet resistance of the as-grown layers to 2–3 kohm/sq versus 1–2.5 kohm/sq for the same range of boron doping without carbon. The boron doping is controlled by the diborane gas flow during the epitaxy, and it is a linear function of the gas flow. The emitter is implanted with a combination of 45° and 60° tilted implants carried out with two mask steps, therefore double dip etch. It did not cause increased leakage, as high tilt angles were used, moreover deactivation in the base was relatively low due to the low implantation doses. Lower deactivation at increasing boron doping shows dose dependency, the interstitial–boron ratio is approximated by the arsenic–boron dose ratio, which is about 200:1 to 20:1 with the increasing boron doping. If carbon is incorporated, the sheet resistance curves cover a smaller range than the corresponding curve without carbon: although initial sheet resistances are higher with carbon, deactivations are relatively lower. All in all, carbon incorporation makes the base region less sensitive to the emitter fabrication.

The comparison of the resulting base sheet resistance for all the emitter implantations is shown as a function of the base doping with carbon incorporation in Fig. 5.12

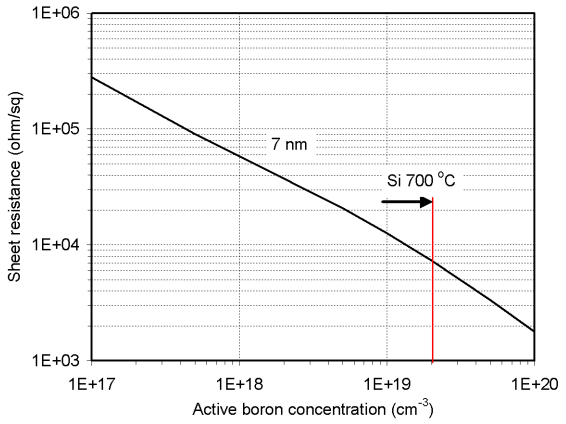

Figure 5.14: Calculated sheet resistance of the deep boron peak versus the active doping of the peak. An equivalent peak width of 7 nm is used. Activation is limited at the temperature of the epitaxy (700 °C) by the solid solubility of boron in Si.

and without carbon in Fig. 5.13.

5.3 Discussion

5.3.1 Active doping in the base

The Irvin-relation between the resistivity and the doping in silicon can be used to to estimate the sheet resistance of the box-shaped boron doped peak as shown in Fig. 5.14. The solid solubility at 700 °C is marked, and due to carrier spilling an equivalent thickness of 7 nm is used to fit the sheet resistance in the 1st case. The highly doped part from 5×10^{18} to 5×10^{19} cm^{-3} can be approximated by

$$N = 1.2850 \times 10^{24} R_{sh}^{-1.2495} \tag{5.1}$$

where N is the active boron doping concentration, and R_{sh} is the sheet resistance. In principle, this formula should be valid for extracting deactivation in the case of a pure silicon base. The shape and slope of the curve determined by the relationship is assumed to be the same in the case using a germanium with or without carbon, but its vertical position might be shifted. In order to overcome the unknown vertical shift,

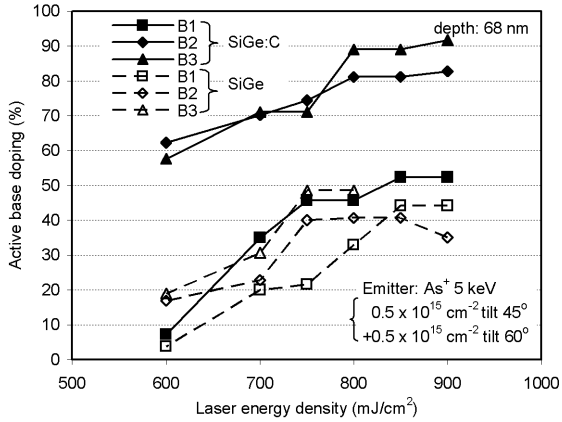

Figure 5.15: Calculated active base doping in SiGe and SiGe:C as a function of the laser energy density for a combined emitter implant. B1, B2, and B3 corresponds to 60, 120, and 180 sccm diborane flow.

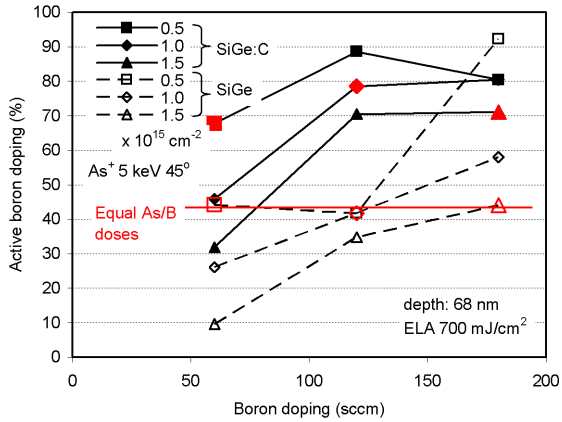

Figure 5.16: Calculated active base doping in SiGe and SiGe:C as a function of the base doping at different emitter implantation doses implanted at 45° tilt. Equal As/B does ratios are marked.

moreover the initial boron peak doping is not accurately know in all cases, the active doping concentration measured after the emitter fabrication can be related to the initial doping concentration (subscript i) of the highly doped base region in the as-grown structure as

$$\frac{N}{N_i} = \left(\frac{R_{sh}}{R_{shi}}\right)^{-1.2495} . \tag{5.2}$$

The active fraction of the base doping was calculated for the combined emitter implant of Fig. 5.11 and shown in Fig. 5.15. The maximum deactivation is about $10\times$, and about the half of the deactivated dopants are reactivated at the highest laser energy. Boron doses at B2 and B3 doping give very similar results, while B1 is clearly lower doped and therefore more affected at the same emitter implantation dose. Carbon retard greatly the deactivations, by using up approximately half of the injected interstitials.

The active base doping after the 45° tilted emitter implantations is plotted as a function of the initial base doping in Fig. 5.16. The boron dose in the base peak is linearly proportional to the gas flow. The implantation dose dependence of the deactivation is obvious in SiGe: deactivation scales with the increasing arsenic dose as well as the decreasing boron dose. Large amount of boron is deactivated as it is the only trap for the generated interstitials. Because doses are chosen that the smallest is doubled and tripled both for arsenic and boron, equal dose ratios marked with enlarged symbols in Fig. 5.16 result in equal deactivations at about 60% as long as carbon excluded. In case of carbon included, it will trap a constant amount of interstitials, therefore the ratios are shifted and the close constellation of the data points for SiGe:C is a coincidence. While the resistance to deactivations increase with the boron doping at the lower boron doses, at 180 sccm level the amount of deactivation saturates or even increases. This is because resistance to deactivation is so high, that most of the injected interstitials are used up in the boron peak with the help of carbon, therefore the sensitivity of the marker is lost.

5.4 Conclusions

The shallow epitaxially grown Si/Ge/C transistors have a narrow highly doped base which essentially act as a boron marker that is very sensitive to deactivations caused by the emitter formation process. Moreover, the close vicinity of the boron marker to the heat affected zone of the laser annealing makes it clear that the increasing laser energy reactivates dopants. The heat pulse has an effect of reactivation as the sheet resistance of the base decreases with the increasing laser energy densities. The deactivation is caused by interstitials escaping from the end-of-range region and reacting with the

boron doped background layers. The amount of deactivation is maximum 10 $\times$, and about the half of that dose is reactivated by the decaying heatpulse of the laser.

The ultrashallow arsenic implanted laser-annealed junctions are suitable as emitters in SiGe transistors even though the junction depth is only about 10 nm. The laser annealing can be performed without inducing relaxation of the strained SiGe layer. The deactivation of boron in the base appears to be reduced by the incorporation of C in the SiGe layer.

The very straightforward processing scheme used here results in high B–E leakage. The situation could perhaps be improved by using a thin spacer technology or densified TEOS oxide to improve the contact window perimeter processing, or by introducing another contact metallization scheme to suppress leakage currents.

Chapter 6

Laser doping from CVD deposited As source

In this chapter, a laser doping technique is evaluated, where the doping of the Si surface is achieved by first depositing an arsenic monolayer by reduced pressure chemical vapor deposition (RPCVD) which was subsequently driven-in by one or more excimer laser pulses. The laser annealing was performed either through an oxide capping layer or directly irradiating the As covered Si surface. The evolution of the surface doping versus the laser energy density used is shown in the diode characteristics and contact resistances.

6.1 Experimental procedures

The schematic process flow for the diode fabrication is shown in Fig. 6.1. The Si substrate was implanted with boron to a surface concentration of 10^{17} cm^{-3} through a 30 nm thick thermal oxide layer. This layer was used as a hard mask. The deposition windows were wet etched in BHF 1:7. Before the dopant deposition, a 4 min 0.55% HF dip was performed to remove any native oxide from the deposition windows, this step reduces the hard mask thickness to about 20 nm. Subsequently, an arsenic monolayer was deposited in the Epsilon One epitaxial reactor from an AsH_3 precursor at 700 °C. The adsorbed arsenic monolayer self limits the deposition and reaches a surface dose of 6.8×10^{14} cm^{-2} [Song et al., 1999]. Subsequently, the processing of a laser capping layer was varied as follows:

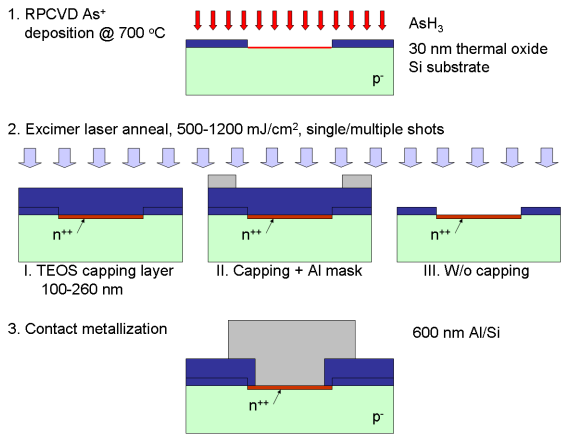

Figure 6.1: Schematic of the n^+p diode fabrication by laser doping from an RPCVD deposited arsenic monolayer.

Table 6.1: Summary of the parameters for the PECVD deposited laser capping layer, laser masking, and the laser irradiation.

Wafer	Capping layer			Al mask	No. of
	source gas	dep. temp. (°C)	thickness (nm)	thickness (nm)	pulses
a	TEOS	350	260	–	1
b	TEOS	350	260	100	1
c	TEOS	350	200	–	1
d	TEOS	350	200	100	1
e	Silane	400	150	–	4
f	Silane	400	100	–	4
g	–	–	–	–	1
h	–	–	–	–	2

I. an oxide capping layer is deposited by PECVD at temperatures $\leq$400 °C. The thickness was chosen at calculated reflectivity extremities of 100, 150, 200 or 250 nm (Fig. 2.8),

II. an oxide capping is deposited as in I. and an additional 100 nm thick Al/Si laser masking layer was sputtered at 50 °C, which was patterned afterwards in a wet Al etchant solution which does not etch oxide.

III. The arsenic depositions were left uncovered.

The wafers were laser annealed in vacuum at 500–1200 mJ/cm^2 by using single, double or 4 shots at a location. Subsequently an extra PECVD TEOS layer was deposited to increase the isolation layer thickness. Contact windows were plasma etched through this layer to the silicon surface. Soft landing with a low power plasma was used. The contact window was about a micron smaller than the deposition window, so that an oxide spacer is formed in this step to ensure the edge passivation of the diodes. Immediately before the Al/Si metallization a 4 min 0.55% dip etch was performed to remove any native oxide. Wafers were completed with a 400 °C alloying in forming gas. The fabrication parameters are summarized in Table 6.1. The diode characteristics were measured by contacting the back of the wafer on square shaped diodes with size of 40 $\times$ 40 μm^2.

Kelvin contact resistance structures were fabricated in p- and n-type diffusion taps. The p-type taps were implanted with boron at 5×10^{15} cm^{-2} 180 keV with an additional shallow implant of 9×10^{14} cm^{-2} 20 keV. The n-type taps were implanted with phosphorous 5×10^{15} cm^{-2} 180 keV. Implants were furnace annealed at 950 °C for 20 min. Subsequently the laser doping was utilized as described above, with 150 nm silane oxide capping layers were used and the dopants were driven-in by double laser pulses. The measured contact size was 4 $\times$ 4 μm^2.

6.2 Results

6.2.1 Diodes

A typical example for the resulting diode characteristics as a function of the laser energy density is shown in Fig. 6.2. With the increasing laser energies, the Schottky barrier height towards the aluminium contact is modulated in the range from p-Schottky ($<$800 mJ/cm^2) to a n$^+$p diode ($>$ 900 mJ/cm^2) with a transient region in between. The junction depth scales with the increasing laser energy density when laser energies exceed the melt limit of c-Si. Melt depths are expected to be smaller here than in the

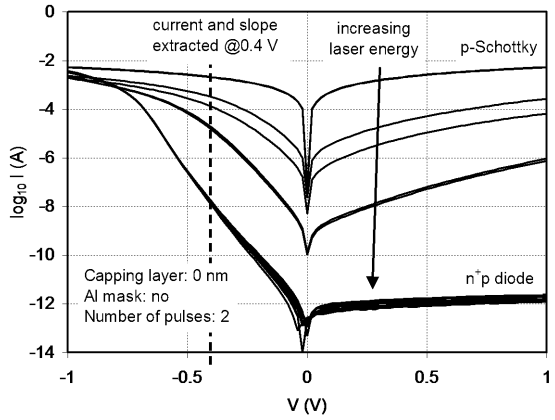

Figure 6.2: Example of the evolution of the diode characteristics for increasing laser energy density for the double shot drive-in. No capping layer was used (wafer h). Diode size: 40×40 μm^2.

implanted case such as shown in Fig. 3.7, therefore junction depths are expected to be smaller than 20 nm.

The current at 0.4 V forward bias and the corresponding slope of the I–V curve is extracted for each wafer type and shown in Fig. 6.3 and Fig. 6.4. In case of a Schottky contact the current is above 10^{-4} A, and in a n$^+$p it drops below 10^{-6} A as marked in Fig. 6.3a. Between these currents a transient region is enclosed. In terms of laser energy densities, a drive-in onset is defined at the laser energy density where the current starts to drop, and a full drive-in is defined at the energy level where stable low currents are reached for all the four measured diodes across the wafer at one laser energy density.

In Fig. 6.3a–d the application of the Al masking is evaluated for two capping layer thicknesses. The drive-in onset is at above 1000 and 900 mJ/cm^2 for 260 nm and 200 nm capping layer thicknesses, respectively which is inconsistent with the calculated reflectivity values here when TEOS oxides cappings were used. The use of the Al masking gives no clear improvement of the diode characteristics. Best uniformities are reached for the case in Fig. 6.3c, and the lowest ideality factor is around 1.16 (70 mV/decade) at 1100 mJ/cm^2. Higher energy densities caused some degradation at the capping layer interface, therefore the ideality factor increases to 1.5 (90 mV/decade).

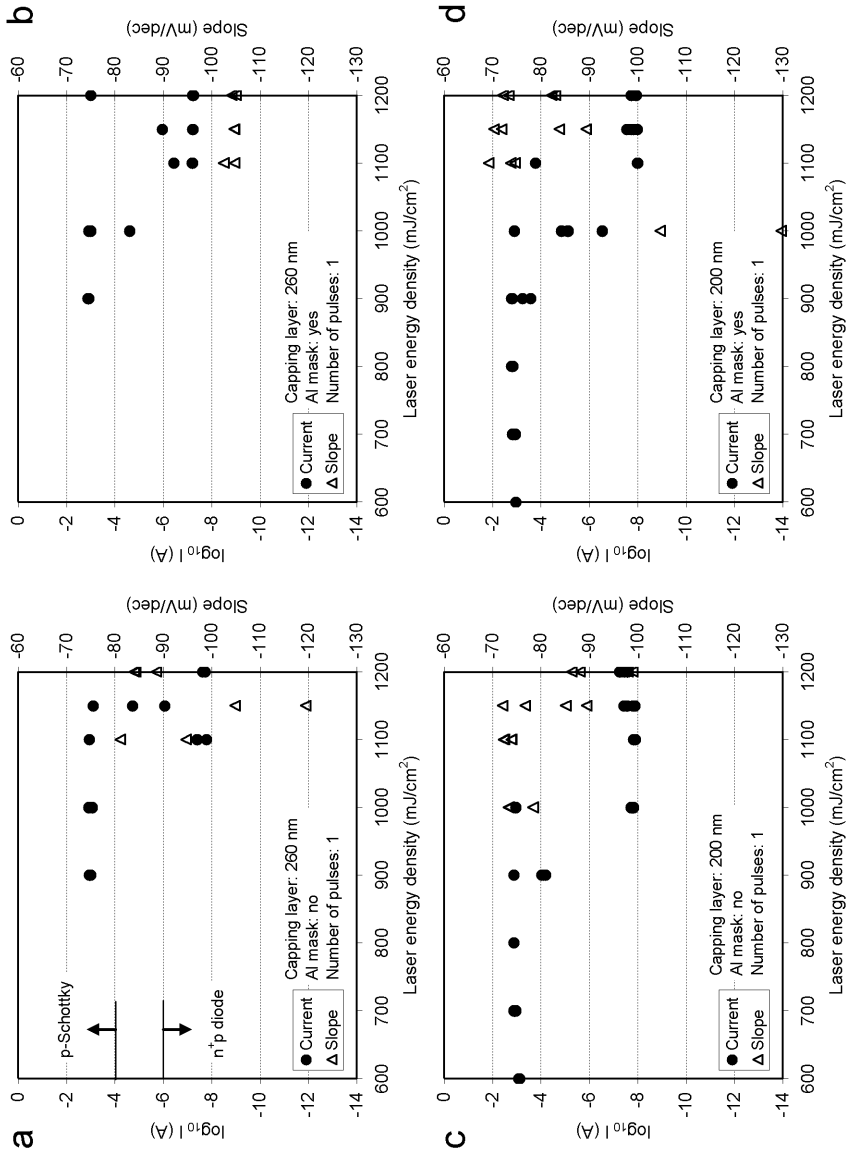

Figure 6.3: Diode current and slope at 0.4 V forward bias on wafers a–d.

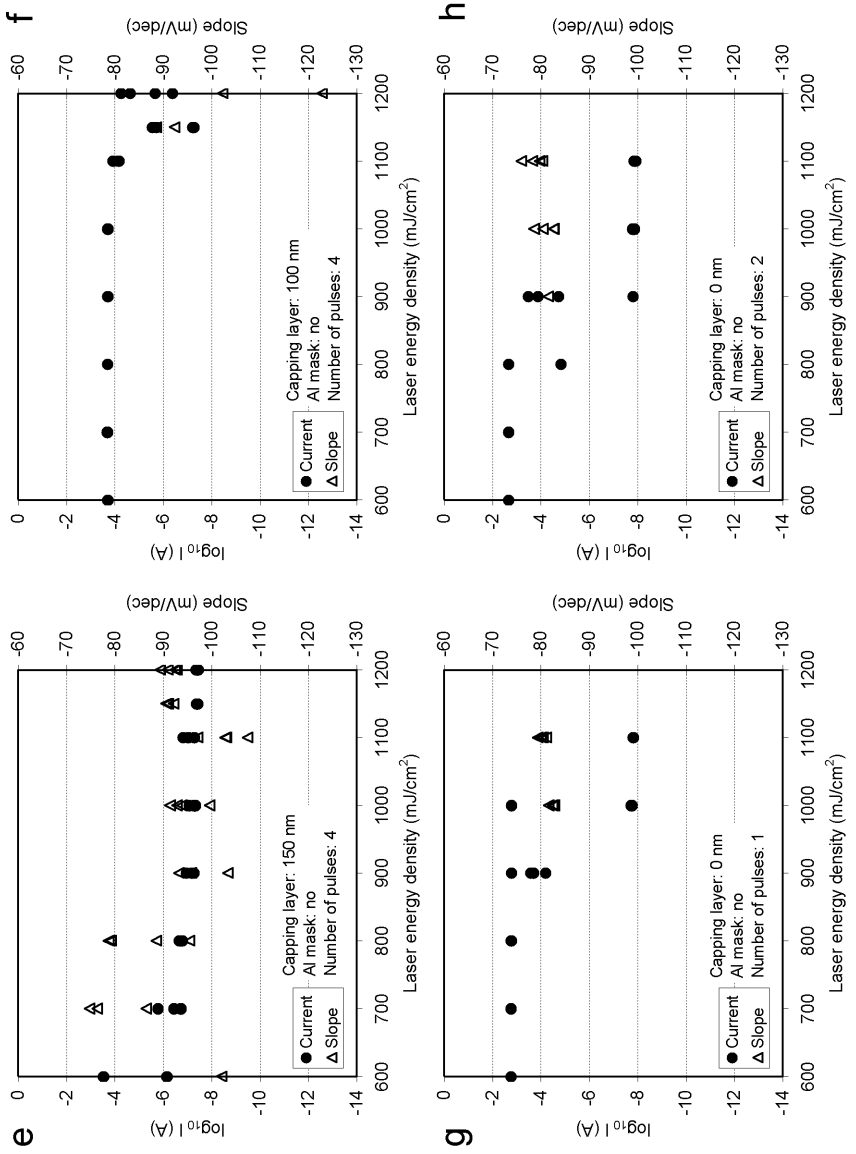

Figure 6.4: Diode current and slope at 0.4 V forward bias on wafers e–h.

The drive-in onset dropped significantly to 700 mJ/cm^2 in wafer e with the increased number of laser pulses, and changes of the onset were correlated with the reflectivity for the 150 and 100 nm silane oxide cappings. An increase in the ideality factor is more obvious due to the larger range: the values are from 1.16–1.5.

The wafers with uncovered arsenic monolayers stayed in a carrier in air ambient for about one week from the deposition to the laser drive-in step. A single and double pulse drive-in step was applied and results are shown in Fig. 6.4g and h. The drive-in onset is 900 mJ/cm^2 for single pulse and it drops to 800 mJ/cm^2 for a double pulse drive-in. Excellent uniformity was achieved over the wafer, and ideality factors were around 1.33, the lowest was 1.25. Interface leakage might contribute to these high values due to the high roughness at the passivation. During the laser annealing the thermal oxide hard mask used for the monolayer deposition covers the non-active areas. After the laser annealing a very high roughness is occurred under these areas with a characteristic pattern as will be described in Section 6.2.3.

The energy limits are not only a function of the reflectivity of the capping layer stack but they are influenced by the modified thermal balance too. The capping layer in principle acts as a heat sink, although its thermal properties eg. its heat conduction coefficient qualifies it as a heat insulator, it still can draw and store heat better than the uncapped case where the heat cannot be lost by conduction outwards from the silicon surface due to the vacuum. [He et al., 2006] studied such a phenomena for recrystallization of a-Si deposited on oxide, which limits the thermal diffusion towards the bulk as well, and concludes by using 1-D simulations that the capping layer can act as a heat capacitor as well as a heat sink. [Fortunato et al., 2002] studied a 2-D case by experiments and simulations for bulk oxide capped silicon wafers and shows that the diode edges are very sensitive to the oxide layer thickness. Such pattern effects, that give a different cooling condition at the diode edges, is studied by [Sadra and Ji, 1998] in combination with gas immersion laser doping (GILD), and showed that less activation can occur due to the higher heat diffusion than at the center of the diodes.

6.2.2 Contacts

Contact resistances are compared with and without As depositions as a function of laser energy density. In Fig. 6.5 and in Fig. 6.6 the measured Kelvin contact resistance is shown for p- and n-type structures, respectively. In both cases double laser shots were used through a 150 nm silane oxide capping.

In the case of p-type Kelvin structures, the deposition of As result in resistances are slightly increased by the arsenic depositions, but still the contact resistance is low. With increasing laser energy densities, more dopants are driven-in. The surface is counter-doped and if only a small amount of As is driven-in, the surface layer gets depleted,

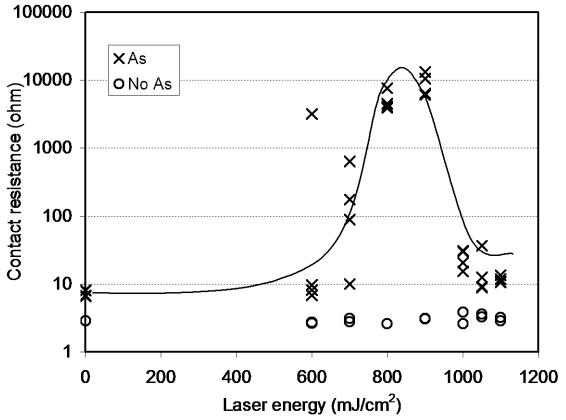

Figure 6.5: Contact resistance with and without As depositions on p-doped Kelvin structures as a function of laser energy density. Double laser shots were used with 150 nm silane oxide capping. The solid line indicates the trend for the As case.

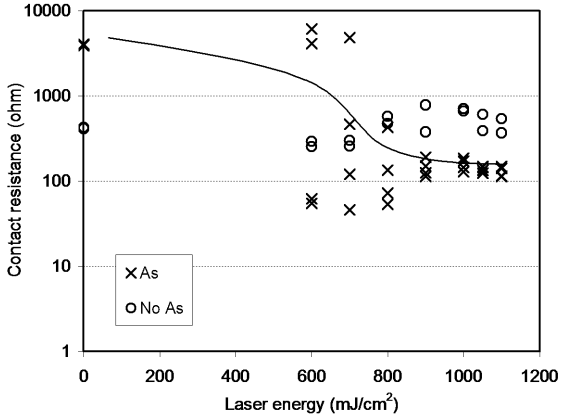

Figure 6.6: Contact resistance with and without As depositions on n-doped Kelvin structures as a function of laser energy density. Double laser shots were used with 150 nm silane oxide capping. The solid line indicates the trend for the As case.

therefore the resistance increases. At high laser energy densities, due to the sufficiently high As surface dose, the surface layer cannot be depleted and therefore a low ohmic contact is formed.

In case of n-type Kelvin structures, contact resistance improves monotonically with the increasing laser energy densities, and improvement is seen over the reference values as a sufficiently high dose is driven-in.

The reference values were measured on a control wafer without As deposition which was subjected to the same processing including laser irradiation. Increasing laser energy densities result in slight surface degradation as scatter in the contact resistance increases. Overall larger contact resistances were measured for the n-type Kelvin structures due to the lower surface doping. In this case the improvement from the ultrashallow As surface doping was at maximum about a factor of 8. However in case of very low contact resistances, the measurement is limited by the Kelvin structures and measured values are influenced by the sheet resistance of the diffusion layer [Ren, 2002].

6.2.3 Laser induced surface patterns

High roughness surface patterns known as laser induced periodic surface structures (LIPSS) were observed in the case of no capping layer was used. It is seen in areas covered by the thermal oxide masking layer as shown in Fig. 6.7.

The thickness of the oxide masking is about 20 nm. It is compressively stressed after the growth at room temperature due to the thermal expansion mismatch between the oxide and the Si substrate. During the laser irradiation the underlying silicon layer absorbs the light and at high enough energies it melts. As the thin oxide capping looses constraint, it relaxes by buckling [Serrano and Cahill, 2002], therefore a wrinkled pattern develops. With the further cooling this shape freezes. The roughness of the surface increases with the increasing laser energy densities, i.e. increasing melt depth.

In large covered areas random shapes develop. If continuity of the layer is broken, then specific patterns are seen. The pattern is perpendicular to the cooling directions close the the window opening. In the windows the laser light is absorbed without loss, therefore higher temperatures develop. If the shape of the window is concave or it encloses an oxide covered island, then no roughening occurs, and the oxide surface remains smooth within the thermal length. At these free edges the stresses in the oxide can relax without buckling. LIPSS structures do not appear if a thicker oxide layer ($>$100 nm) is used, as those layers are stiffer.

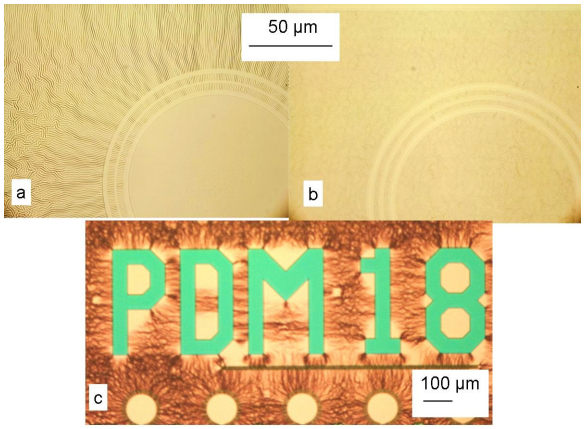

Figure 6.7: Laser induced periodic surface structures (LIPSS) under the 20 nm oxide hard mask used for the deposition (a) for 1100 mJ/cm^2, and (b) lower roughness at 700 mJ/cm^2. The circular rings without the LIPSS pattern are windows to the arsenic covered silicon surface. (c) Low roughening is seen in areas of oxides enclosed by contact windows (1100 mJ/cm^2).

6.3 Conclusions

To avoid residual implantation damage, dopants can be deposited by a CVD technique and driven-in by the excimer laser. Drive-in under a capping layer as well as without capping is feasible. Multi-pulses drive in with better efficiency, but leads to degradation in diode idealities. The relatively high energies needed are detrimental for the Si-SiO_2 interface, if Al masking is not used in combination with the CVD process.

Near-ideal diodes are fabricated with the lowest ideality factors measured at 0.4 V forward bias reach 1.16 under the capping layer and 1.25 at double shots without capping layers. At the highest tested energies degradation occurs at the capping layer interface, therefore ideality factor increases. The benefit of the utilization of multiple shots is that spot-to-spot non-uniformities are reduced, moreover an increasing number of dopants are driven-in with multiple shots, therefore lower energies can be used. While annealing without any capping or masking layers, laser induced periodic surface structures (LIPSS) occurred at the oxide interface. These patterns are only visible at high laser energy densities and were not found while capping layers were used.

Chapter 7

Double laser annealing

7.1 Introduction

Tailoring the annealing thermal cycle is less evident in laser annealing than in furnace annealing. While the pulse shape is not directly adjustable, with additional pulse extender optics longer pulses can be achieved. In this way, the thermal gradients can be reduced [Venturini, 2005] and thermal budget can be increased by 2-3 times which can be beneficial for defect annealing [Matsuno et al., 2002].

While most laser setups consist of one laser, some groups have investigated double laser processing with excimer and Ar^+ laser [Lee et al., 2001] or two solid state lasers [Kudo, 2006]. [Ishihara and Matsumura, 1995] studied silicon recrystallization with a double excimer laser annealing setup.

The two excimer laser operation gives the opportunity to introduce a pulse offset between the two laser pulses in equal energy density mode. By using short offsets the pulse shape is modulated. Long offsets on the other hand are equivalent to annealing with repetitive pulses with a single laser as complete cooling is reached in the delay. However, in a medium offset range, where laser pulses are separated, heat pulses may not, which is not possible to achieve with a single excimer laser due to the slow repetitions of such lasers. Short pulse offsets may result in non-uniformities due to the time jitter between the firing of the lasers. However, the timing between ignitions of the lasers becomes critical at zero offset as jitter can cause spot-to-spot power non-uniformities.

In this chapter, double laser annealing with variable pulse offsets is demonstrated by comparing sheet resistances of the laser annealed implantations. At zero offset, the

pulses are completely overlapping, and therefore providing the largest power. As the pulses separate and peak power drops, the total energy density remains unchanged and therefore the surface temperature drops. In this regime, the effective pulse duration is longer. When the pulses are separated further, the effective energy density reduces and is ultimately halved. The temperature drop can be compensated by increasing the laser energy density and/or the substrate temperature. Spot-to-spot uniformity improves with increasing pulse separation. In practice, the longer pulses have a beneficial effect on reducing defect concentrations below the amorphous/crystalline interface. By using dissimilar pulse amplitudes, pre- and post-heating can be realized. The optimal pulse separation and amplitude ratio can be found for a given thermal limitation at a spot-to-spot uniformity tolerance.

7.2 Experimental procedures

The n^+ implanted regions to be laser annealed are formed by a 15 keV, 5×10^{14} cm^{-2} As^+ implantation on p-type wafers. This implantation gives an amorphous depth around 50 nm, and when the implant is fully activated by the laser anneal, the sheet resistance drops below 300 ohm/sq. The laser annealing after the implantation was performed at room temperature in vacuum, with a laser pulse overlap of 66%. The pulse offsets are set for different wafers at 0, 40, 60, 100, 200 and 400 ns. An example of the resulting pulse shapes are shown for 0, 40 and 100 ns in Fig. 2.3. The energy ratio of the pulses was varied as 1:1, 1:2 and 2:1 to realize equal energies, pre-heating and post-heating, respectively.

The sheet resistance of each wafer was measured by 4 point sheet resistance mapping over the wafer with the CDE Resmap sheet resistance meter as described in Section 2.3.1.

7.3 Results

7.3.1 Equal energy ratio

Simulation results

The temperature history is shown for the irradiated silicon surface by double laser annealing with various pulse offsets (Fig. 7.1). The melting was calculated with the enthalpy based method as described in Section 2.2.1. For the simple simulated case of irradiating c-Si, the heat generated from a single laser pulse can be superimposed, to approximate the heating effect. Therefore, as the temperature decays from the first

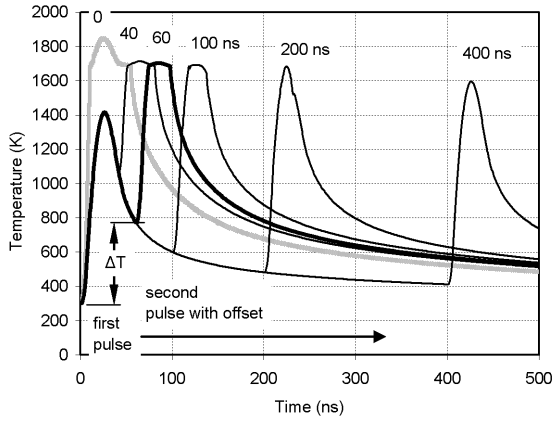

Figure 7.1: Surface temperature evolution calculated by the enthalpy based method in double pulse laser annealing with pulse energies of 500 mJ/cm^2 and pulse offsets from 0–400 ns.

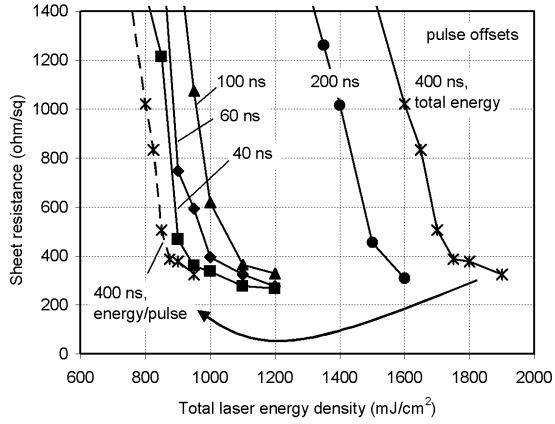

Figure 7.2: Sheet resistance of a laser annealed As$^+$ 15 keV, 5×10^{14} cm^{-2} implant with ELA at different pulse offsets with pulse energy ratio 1:1.

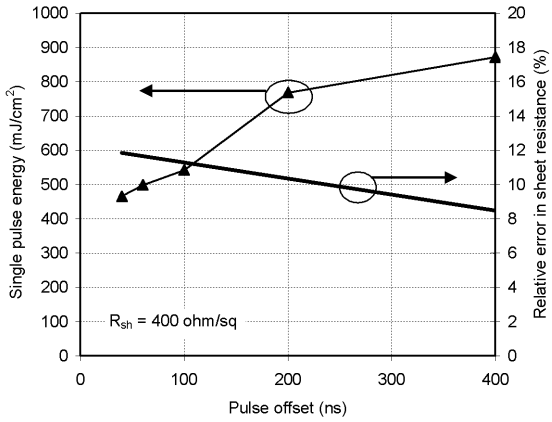

Figure 7.3: Required energy density per pulse in double laser annealing with increasing pulse offsets to reach a melt depth giving a sheet resistance of 400 ohm/sq extracted from Fig. 7.2. Relative error in the sheet resistance with the increasing pulse offset.

pulse, it gives lower and lower initial temperature for the second pulse, hence a lower overall temperature can result. The absolute temperature profile would be slightly different if the thin amorphous implanted layer would have been considered: a-Si has a much lower thermal conductivity, somewhat higher heat capacity, and a lower melting temperature. All in all, this would result in a faster heating. Considering phase transformation at melting, latent heat can act as a buffer for the heat. As melting reaches the amorphous/crystalline interface, the difference in melting temperature limits the process, and the melting only progresses further if the temperature reaches the melting point of c-Si. The regrown Si properties are very much dependent on the process of cooling by which the heat injected into the silicon surface is conducted away by the bulk substrate. Although a basic thermal model was used in the simulation, it still gives a good estimate of the total heating, in view of the fact that the cooling properties are very important and the thermal budget is otherwise correct. However, thermal losses due to radiation and ablative processes can cause deviations in the total heating or cooling times.

Wafer samples

The measured sheet resistance values are shown in Fig. 7.2 for samples laser annealed with different pulse offsets. In general, increasing laser energy density is needed with increasing pulse offsets in order to achieve a certain melt depth/ sheet resistance. As a function of the offset time, three regions can be distinguished.

1. Short offsets ($<$ 100 ns). Early pulse separation can be considered to result in one elongated pulse as can be seen in Fig. 7.2 for the 40 ns offset, as long as the second pulse is ignited in the close neighborhood of the peak of the first pulse. As the laser pulses overlap, offsets result in a drop in the peak power of the resulting pulse. However, after the laser pulses are separated ($>$ 40 ns), extended heating can happen up to 100 ns, where the gap between the laser pulses is $3\times$ the native pulse width. As the thermal pulses are still not separated, the peak temperature difference (ΔT) is very high. In this regime, the melting and activation is driven by the second laser pulse.

2. Medium offsets (100–400 ns). After a pulse offset of 100 ns, as ΔT drops, the pulse energy needed for annealing becomes suddenly very high so melting temperatures are already reached with the first pulse. However, ΔT is so large that the second pulse will contribute in further melting and activation even though it hits the surface after the solidification has started. Therefore, both laser pulses result in partial melting. It should be noted, that in principle with long pulses it is possible to reach the non-melt laser annealing regime, but this is not the case with pulse separation of such narrow single pulses.

3. Large offsets ($>$ 400 ns). At offsets of 400 ns or larger, the first pulse is entirely responsible for the activation process, as thermal pulses are truly separated, ΔT is so small that the second pulse cannot melt the regrown layer, it has only a minor effect on the redistribution of the dopants [Fogarassy et al., 1989]. This situation is equivalent to a single laser annealing with half the energy and double shots. What energy density is needed per pulse to melt a certain depth with double pulse annealing? This can be seen in Fig. 7.3. In laser annealing with a melting energy, the annealed profile will be uniform as the dopants can diffuse much faster in the melt than in the solid. In this way the sheet resistance correlates to the melt depth before (and after) reaching the a/c interface. In Fig. 7.3 the required laser energy per laser is shown for activating the test implant to a sheet resistance of 400 ohm/sq slightly before the melt reached the a/c interface. The scatter in the sheet resistance values results from the following effects: when the melt has not yet reached the a/c interface, the process is not self-limited, and the melt depth will be dependent on the fluctuations of the laser fluence. Moreover, the jitter in the pulse timing can result in variations in the heating. The scattering effect shown for the jitter here decreases as the pulse offset increases.

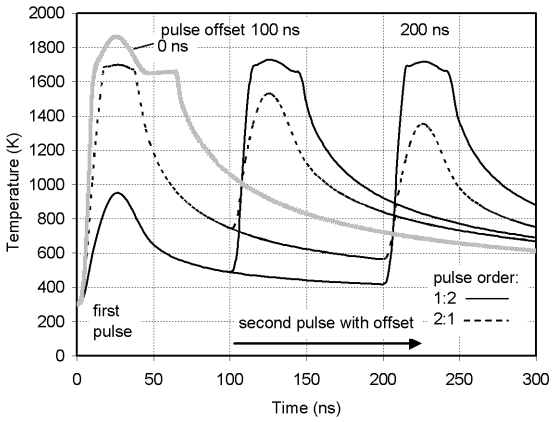

Figure 7.4: Surface temperature history in double pulse laser annealing with a total energy of 1000 mJ/cm^2 (large pulse: 667 mJ/cm^2, small pulse 333 mJ/cm^2, and pulse offsets from 0, 100, and 200 ns.

7.3.2 Non-equal pulse ratios: pre- and post-heating

Simulation results

Surface temperatures were calculated by using the phase field method as described in Section 2.2.1. Temperature history is shown for the irradiated silicon surface by double laser annealing with various pulse offsets in Fig. 7.4. In the case of the pre-heating pulse arrangement, the small pulse is first (pulse order 1:2), and then the maximum temperature is always reached by the second (large) pulse. In case of a post-heating arrangement (pulse order 2:1), the peak temperature is reached by the first (large) pulse at large pulse offsets.

Wafer samples

The measured sheet resistance values are shown in Fig. 7.5 for samples laser annealed with pulse offsets of 0 and 200 ns in a pre-heating pulse arrangement (small pulse followed by a large pulse, with an energy ratio of 1:2). In general, increasing the total laser energy density is needed with increasing pulse offsets in order to achieve a certain melt depth/ sheet resistance. The effective laser energy is in between the total and the largest pulse energy:

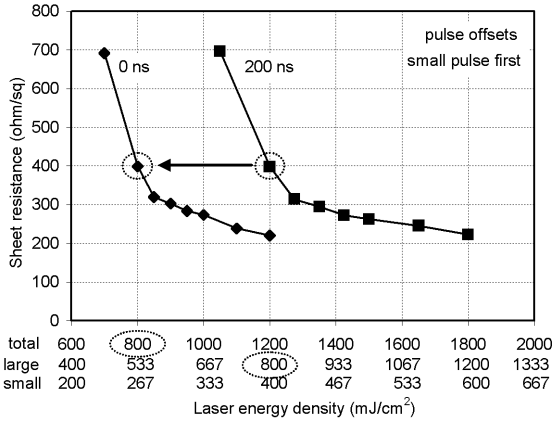

Figure 7.5: Sheet resistance of a double laser annealed As^+ 15 keV, 5×10^{14} cm^{-2} implant with ELA at different pulse offsets in a pre-heating pulse arrangement. Laser energy densities are shown for the small and the large pulse as well as their sum (total) on the horizontal axis.

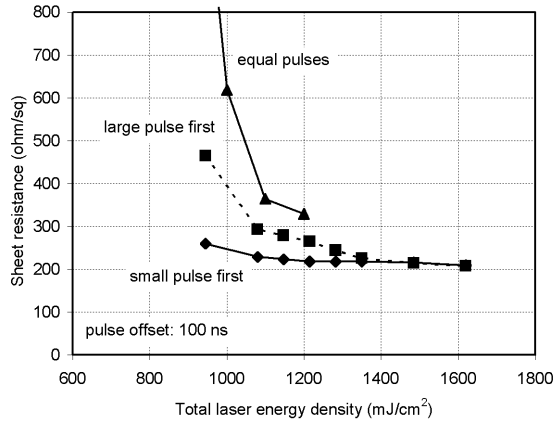

Figure 7.6: Sheet resistance of a double laser annealed As^+ 15 keV, 5×10^{14} cm^{-2} implant with 100 ns offset at different pulse energy orders of 1:1, 2:1, 1:2.

$$E_{total} = E_{small} + E_{large} \geq E_{eff} \geq E_{large} \tag{7.1}$$

The curves in Fig. 7.5 show the extremities: at 0 ns offset the two laser pulses are completely overlapped, resulting in one pulse with the largest possible peak power and the effective laser energy equals the total energy density. At 200 ns offset, however, not only the laser pulses are separated, but also the generated heat pulses are separated. This happens at smaller offsets at non-equal pulse energies than at equal pulse energies, where complete separation occurred at 400 ns for the same implantation. In the present case, the second (large) pulse is responsible for the activation process as opposed to the equal-pulse or post-heating arrangement. The first (small) pulse has so low energy (Fig 7.4), that it cannot initiate phase changes in the amorphous layer, and its heating effect vanishes at already 200 ns offsets. Melting of a thin layer of the a-Si can start at energies of 500 mJ/cm^2, but then the second pulse is so high that the initial effect is negligible. As the small pulse has negligible effect, the effective laser energy density equals to the energy density of the large laser pulse, e.g. to reach 400 ohm/sq activation, at 0 offset both pulses contribute a total of 800 mJ/cm^2, while at 200 ns pulse offset this sheet resistance is reached at 1200 mJ/cm^2 total energy density, of which only the large pulse is effective, with exactly 800 mJ/cm^2.

A comparison of the different pulse arrangements (equal pulses: 1:1, large pulse first: 2:1, small pulse first: 1:2) at 100 ns pulse offsets is shown in Fig. 7.6. Apparently, this offset falls into the small offset range, where the heat pulses generated from the laser pulses are not yet separated, therefore both laser pulses contribute to the effective laser energy. In other words, the resulting sheet resistances cannot be reached with a single pulse set to the largest contributing energy. For the 1:1 and 2:1 cases the first pulse reaches melting and then the second pulse contributes with more heat. The effect of the first pulse is important, in 2:1 the first pulse is larger than in 1:1, therefore the resulting sheet resistance is smaller. Melting starts at about 500 mJ/cm^2. Solidification has not started after 100 ns. In the simulation results, this regime is not captured. In the case of the 1:2 pulse order the first pulse is so small, that it cannot melt. However, a-Si keeps heat longer, and the second pulse starts at elevated temperature and causes melt. This situation is similar to laser annealing with substrate heating. The sheet resistance stabilizes at high enough laser energies (total energy $>$ 1300 mJ/cm^2) for 1:2 and 2:1, because for the former case, the small first pulse energies become large enough for melting.

7.4 Conclusions

It has been demonstrated that in the use of double-pulse laser annealing of implanted silicon regions, the pulse offset is an important parameter for the total amount and reproducibility of the heat transfer to the Si. As a general result, it is shown that with increasing the pulse separation, higher laser energy is needed to fully activate implantations. This is a result of the fact that the temperature rise due to the second pulse superposes on the heat profile generated by the first pulse, thus a higher energy of the individual pulses is needed to achieve the desired heat transfer as the pulse offset is increased. Increasing the pulse offset has also the advantage that non-uniformities in the annealing caused by the time jitter between the two laser operation are decreased.

The high energy densities needed for full dopant activation with single pulse laser annealing can be reduced by increasing the substrate temperature. In this way, the thermal budget can be fine tuned for the trade-off shallow junction depth versus implantation induced defect annealing.

The use of non-equal energies makes the complete separation offset smaller. The use of pre- or post heating arrangements has different effects on the sheet resistances in the small offset regime: the pre-heating results in lower sheet resistances as the small first pulse does not induce melting, therefore the second pulse does not hit liquid Si.

Fine tuning the thermal budget is possible with the double laser system by introducing a small offset between the laser pulses. This offset is much smaller than the delay from the repetition time of the laser, therefore it is possible to superpose the heating cycles introduced by the individual pulses. Pre- or post heating configurations can be distinguished, and the efficiency can be shown by the resulting sheet resistances. Preheating is the most efficient, while post heating has the largest thermal budget at equal total energy densities.

Chapter 8

Conclusions and recommendations

Excimer laser annealing has been investigated for implementation of ultrashallow junctions and low-ohmic contacts in back-wafer-contacted silicon-on-glass technology. Ultrashallow, abrupt and highly-doped regions were fabricated with sub-50 nm depths, as well as low sheet and contact resistance. Devices have been demonstrated with near-ideal diode behavior corresponding to low residual leakage. It is shown that it is feasible to fabricate these diodes in close proximity to SiGe strained layers and functional SiGe HBTs with laser-annealed emitters were realized in this manner. Laser drive-in from deposited dopant source is promising for ultrashallow junctions below 20 nm. Modulating the thermal profile and fine tuning of the thermal budget was made possible by using a double laser setup.

The main conclusions of this thesis are:

- The laser annealed diodes are self-aligned to the contact window into which the dopants are implanted. The quality of the material in which the window is defined is critical for the quality of the fabricated diode since it determines the quality of the diode perimeter passivation as well as the actual alignment of the junction to the final contact window. The most ideal diodes with a ideality factors $n \approx 1.05$ have been fabricated with thermally grown oxides because these are not excessively removed during the contact metallization processing and they provide the best interface passivation.

- The surface morphology of the contact window before implantation influences

the bulk diode quality. The smoother the surface the more ideal the diode characteristics. The isolation oxide/ reflective Al mask layer stack and the etching sequence was optimized to have an surface roughness below 30 angstrom.

- The surface is also roughened by very high energy anneals. This can increase in the contact resistance to the implanted region and give a more non-ideal diodes behavior. Below these energies a wide laser energy range results in good quality diodes with a low spread in the ideality factors.

- The laser annealed implantations have an effect on the doped regions surrounding the implanted region. This is particularly shown for NPN bipolar transistors where the residual implantation damage deactivates the base dopants. Especially boron dopants are susceptible to deactivation. The presence of non-annealed defects also cause leakage currents in the transistor I-V characteristics. The detrimental effects are strongly dependent on the implantation dose and tilt angle, with a reduction being achieved with lowering of the dose and increase of the tilt angle.

- The heat pulse sent into the substrate by the laser annealing process can have the effect of reactivating the dopants deactivated by the implantation. However, this has only been clearly observed in the case of thin boron doped layers placed within a few tens on nanometers from the implantation. This is the situation created in SiGe HBTs where an epitaxially grown strained SiGe boron-doped base is positioned about 50 nm under a laser-annealed implanted arsenic-doped emitter.

  Recommendation: To heal defects at a greater distance from the implantation, an increase of the thermal budget might be beneficial. This could be achieved by long pulse annealing using pulse extender optics.

- The ultrashallow arsenic implanted laser-annealed junctions are suitable as emitters in SiGe transistors even though the junction depth is only about 10 nm. The laser annealing can be performed without inducing relaxation of the strained SiGe layer. The deactivation of boron in the base appears to be reduced by the incorporation of C in the SiGe layer.

  Recommendation: The very straightforward processing scheme used here results in high B–E leakage. The situation could perhaps be improved by using a thin spacer technology or densified TEOS oxide to improve the contact window perimeter processing, or by introducing another contact metallization scheme to suppress leakage currents.

- To avoid implantation damage, implants can be deposited by CVD techniques and can be driven-in by the excimer laser melting. Drive-in while still preserving good diode characteristics seems feasible both with and without a capping layer. Multi-pulses drive-in could perhaps be used to achieve deeper junctions but might also lead to surface deterioration. The relatively high energies needed are detrimental for the Si–SiO_2 interface. Laser induced surface structures (LIPSS) and high roughening can be avoided by using a thick surface oxide.

- When a thin surface oxide is used in combination with laser annealing, the visible oxide roughening can provide a means of studying the thermal gradients and thus the pattern sensitivity of the annealing.
  Recommendation: This technique could be especially useful for understanding the annealing behavior in FETs where the source/ drain regions are created by laser annealing and the annealing efficiency is a function of the gate length due to mutual heating of the annealed regions.

- Fine tuning of the thermal budget is possible with the double laser system by introducing a small offset between the laser pulses. This offset is much smaller than the delay associated with the repetition time of the laser. Therefore it is possible to superpose the heating cycles introduced by the individual pulses. Pre- or post-heating configurations are effectively different, as has been demonstrated by measuring the resulting sheet resistance that can be assumed to be proportional to the corresponding junction depth. Pre-heating is more efficient than post-heating, which requires the largest effective thermal budget at equal total energy densities.
  Recommendation: A time resolved reflectivity study could be used to reveal the true melting characteristics.

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Summary

Excimer laser annealing for ultrashallow junctions and contacts
by Viktor Gonda

The work in this thesis has been performed in the context of the non-MOS high-frequency silicon device integration research being performed at DIMES. In general, in high-frequency devices the demand for thin, abrupt and accurately tailored doping profiles has also put focus on low-temperature processing techniques. Full-melt laser annealing in combination with low energy implants, is one of the few techniques that can fulfil these requirements.

In this thesis, the integration of high-power excimer laser annealing to activate low-energy implanted regions is investigated with the goal of fabricating ideal junctions and low-ohmic contacts in high-frequency silicon-on-glass devices. The results of the investigation include several generally applicable rules for optimizing the fabrication and integration sequence to accommodate the laser anneal step.

Chapter 2 introduces the tools with which the work in the thesis has been performed. In first instance the high-power excimer laser annealing systems are described followed by the methods used to model the basic thermal behavior during laser annealing. A short overview of the applied material analysis techniques is given, while the electrical characterizations techniques, which have been the most important means of evaluating the quality of the laser anneal junctions and contacts, are treated in detail. These include the measurement of test structures for determining contact resistance and the I–V and C–V characteristics of diodes, bipolar junction transistors and junction field-effect transistors.

In Chapter 3, the basic process flow is described for integrating the laser annealing of an implanted region with the goal of obtaining a near-ideal ultrashallow junction. Sub-50 nm junction depth p^+n and n^+p diodes are formed by excimer laser annealing (ELA) of BF_2^+ and As^+ implants, respectively, performed directly in the contact win-

dows. The latter are etched through a stack composed of a reflective Al masking layer deposited on a silicon oxide isolation layer. The isolation stack, the etching process, the laser anneal energy and the implantation parameters are optimized for good edge coverage of the diodes and lowest possible residual damage. In this manner near-ideal diode characteristics with ideality factors of 1.1–1.3 and low contact resistances are achieved in the laser energy processing window of 900–1000 mJ/cm^2. The results of a series of systematic experiments where the influence of individual process steps is evaluated make it possible to optimize the process flow in different device integration situations.

Both the implantation and the subsequent laser anneal can have an effect on the doping in regions in the vicinity of the implant. Chapter 4 concentrates on the effects of residual defects injected into the substrate and not annealed by the laser, which can result in increased junction leakage and deactivation of dopants. It is shown that the severity of these effects can be reduced by modifying the implantation parameters. Bipolar transistor test structures are fabricated with implanted and laser annealed emitters. The transistor characteristic are compared for devices with the laser annealed implantation parameters varied. Results show that junction leakage is present due to non-annealed implantation defects by the laser act as generation-recombination centers. Moreover, the emitter implantation has an effect much deeper in the background base implantation, which appears in deactivations in the base and the amount is related to the emitter implantation dose and tilt angle, thus the amount and location of the damage generated. Less bulk residual implantation damage is present at low implantation doses or high tilt angles.

The integration of a laser annealed implantation together with strained layers is evaluated in Chapter 5. NPN HBTs were fabricated with arsenic implanted laser annealed ultrashallow emitters on top of a Si/SiGe/SiGe:C thin epitaxially grown base highly doped with boron. The sheet resistance in the base is measured for various emitter implantation dose and tilt angles and laser annealing conditions.

Essentially the thin base acts as a boron marker, such as is often used in TED experiments in combination with SIMS measurements to determine its chemical doping concentration. In this work, the measured electrical properties are related to the electrically active dopant or carrier concentrations. The boron peak is narrow and located very close to the top surface. Therefore, it is very sensitive to deactivation due to the emitter implantation. The active concentration in the base is also dependent on the heat pulse generated by the laser annealing, and is therefore a measure of any reactivation due to laser annealing.

In Chapter 6 a laser doping technique is evaluated for replacing arsenic implants with CVD deposited monolayer of arsenic. The doping of the Si surface is achieved by first depositing an arsenic monolayer by reduced pressure chemical vapor deposition

(RPCVD) which was subsequently driven-in by one or more excimer laser pulses. The laser annealing was performed either through an oxide capping layer or directly irradiating the As covered Si surface. The evolution of the surface doping versus the laser energy density used is shown in the diode characteristics and contact resistances.

In Chapter 7 Double-pulsed high-power excimer laser annealing is investigated for use as a means of implanted dopant activation. The laser setup incorporates two lasers that allow double pulse laser annealing with pulse offsets much smaller than the repetition of the individual XeCl excimer lasers. In this configuration, the pulse offset can be fine tuned. Sheet resistances are measured and thermal simulations are conducted to study temperature profiles. Results show, that the total laser energy needed for a complete activation increases with the pulse separation. The increase can be compensated by substrate heating. By using non-equal pulse energies, complete separation occurs earlier and pre-heating arrangement is favorable to post-heating. In this way the thermal budget can be tuned with more freedom.

Samenvatting

Excimer laser annealing voor ultraondiepe juncties en contacten
Door Viktor Gonda

Het in dit proefschrift beschreven werk werd uitgevoerd in de context van het DIMES-onderzoek naar de integratie van hoogfrequente siliciumdevices die niet MOS gebaseerd zijn. Over het algemeen heeft voor hoogfrequente devices de vraag naar dunne, abrupte en exact op maat gemaakte doteringsprofielen ook lage-temperatuur-procestechnieken op de voorgrond geplaatst. *Laser annealing* (uitgloeiing door middel van een laser), waarbij een laag silicium volledig wordt gesmolten, is in combinatie met lage-energie implantaties in veel situaties een van de weinige technieken die aan deze voorwaarden kan voldoen.

Onderwerp van dit proefschrift is de geïntegreerde toepassing van excimer laser annealing met hoog vermogen om geïmplanteerde gebieden met lage energie te activeren. Het doel is om ideale juncties en laag ohmische contacten in hoogfrequente silicium-op-glas devices te vervaardigen. Het onderzoek heeft onder andere geresulteerd in een aantal algemeen toepasbare regels voor de optimalisatie van het fabricageproces en het integratie-verloop, zodat de laser anneal processtap kan worden ingepast.

Hoofdstuk 2 is een inleiding op de gereedschappen waarmee het werk in dit promotieonderzoek werd uitgevoerd. Allereerst worden de excimer laser annealing systemen met hoog vermogen beschreven, gevolgd door de methoden die werden gebruikt om het fundamentele thermische gedrag gedurende laser annealing te modelleren. Er wordt een beknopt overzicht gegeven van de toegepaste materiaal-analysetechnieken. De elektrische karakterisatietechnieken – de voornaamste middelen om de kwaliteit van de laser anneal juncties en contacten te beoordelen – worden gedetailleerd behandeld. Hiertoe behoren de metingen van teststructuren om de contactweerstand en de I–V en C–V karakteristieken van diodes, bipolaire junctie transistors en junctie veldeffect-transistors.

In hoofdstuk 3 wordt de basisproces flow beschreven voor de integratie van de laser annealing van een geïmplanteerd gebied, met als doel een bijna ideale ultra-ondiepe junctie te verkrijgen. Sub-50 nm junctiedieptes van p^+n en n^+p diodes worden gevormd door excimer laser annealing (ELA) van respectievelijk BF_2^+ en As^+ implantaties, die direct in de contactgaten wordt uitgevoerd. Deze contactgaten worden geëtst door een lagenpakket, bestaande uit een reflectieve Al maskeringslaag die op een siliciumoxide isolatielaag is gedeponeerd. Het isolerende lagenpakket, het etsproces, de laser anneal-energie en de implantatieparameters worden geoptimaliseerd voor goede randbedekking van de diodes en de laagst mogelijke restschade. Op deze wijze worden bijna-ideale diode-karakteristieken met idealiteitsfactoren van 1.1–1.3 en lage contactweerstanden bereikt voor laserenergieën van 900–1000 mJ/cm^2. De resultaten van een serie systematische experimenten waarin de invloed van individuele processtappen wordt beoordeeld maken het mogelijk de proces flow te optimaliseren voor device-integratie onder verschillende omstandigheden.

Zowel de implantatie als de laser annealing die daarop volgt, kunnen van invloed zijn op de dotering in gebieden in de buurt van de implantatie. Hoofdstuk 4 is gewijd aan de effecten van restdefecten die in het substraat worden gebracht en niet door de laser worden uitgegloeid. Deze kunnen leiden tot een toename van junctielekstroom en tot deactivering van de dotering. Er wordt aangetoond dat de ernst van deze effecten kan worden verminderd door de implantatieparameters te veranderen. Bipolaire transistor-teststructuren worden vervaardigd met emitters die door laser annealed geïmplanteerd arseen zijn gevormd. De transistorkarakteristieken worden vergeleken voor verschillende devices waarbij de laser anneal- en implantatieparameters zijn gevarieerd. De resultaten laten zien dat de junctielekstroom optreedt ten gevolge van niet uitgegloeide implantatiedefecten die zich gedragen als generatie-recombinatie-centra. In het bijzonder heeft de emitterimplantatie tot effect dat het boor in de onderliggende p-gedoteerde basis wordt gedeactiveerd. De mate van deactivatie staat in verband met de emitterimplantatie dosis en de hoek waaronder wordt geïmplanteerd. Over het algemeen is er minder restschade door implantatie in het substraat bij lage implantatiedoses of grote implantatiehoeken.

In hoofdstuk 5 wordt de integratie beoordeeld van een laser annealde implantatie van lagen die onder mechanische spanning staan. Er werd een serie NPN heterojunctie bipolaire transistors (HBT's) vervaardigd met arseen-geïmplanteerde laser annealde ultraondiepe emitters, samen met een dunne epitaxiaal gegroeide basis van hetzij Si, SiGe, of SiGe:C dat hooggedoteerd is met boor. De sheetweerstand in de basis wordt gemeten voor verschillende emitterimplantie doses, implantatiehoeken en laser annealing condities. In essentie gedraagt de dunne basis zich als een boormarker. Deze techniek wordt vaak gebruikt in experimenten die worden opgezet om transient enhanced diffusion (TED) te detecteren door metingen van de chemische doteringsconcentratie

met behulp van secondary-ion-mass spectroscopy (SIMS). In dit onderzoek zijn de gemeten elektrische eigenschappen gerelateerd aan de elektrisch actieve doterings- of ladingsdrager-concentraties. De boorpiek is smal en bevindt zich zeer dicht bij het bovenste oppervlak. Daardoor is deze piek zeer gevoelig voor deactivatie die wordt veroorzaakt door de schade als gevolg van de emitterimplantatie. Bovendien kan de hittepuls die door de laser annealing wordt gegenereerd en het siliciumsubstraat in wordt gestuurd het annealen van de implantatieschade tot effect hebben. Dit effect blijkt overduidelijk uit de experimentele resultaten met SiGe HBTs.

In hoofdstuk 6 wordt een laser doteringstechniek bestudeerd om arseenimplantaties te vervangen door een monolaag van arseen. De dotering van het Si oppervlak wordt tot stand gebracht door eerst een arseen monolaag te deponeren met behulp van chemical-vapor deposition onder lage druk (RPCVD). Het arseen wordt vervolgens in het silicium gedreven door één of meer pulsen van de excimer laser. De laser annealing wordt uitgevoerd hetzij door een oxide deklaag, hetzij door de directe bestraling van het met As bedekte siliciumoppervlak. De relatie tussen de oppervlaktedotering en de dichtheid van de laserenergie wordt bekeken door de diodekarakteristieken en de contactweerstanden te meten.

In hoofdstuk 7 wordt hoog vermogen excimer laser annealing met twee pulsen onderzocht als middel om geïmplanteerde doopstof te activeren. De laseropstelling bestaat uit twee lasers die laser annealing met twee pulsen mogelijk maken. Hierbij blijkt dat de twee pulsen veel sneller aankomen dan de herhaalde pulsen van een enkele XeCl excimer laser. In deze configuratie kan de tijd tussen de twee pulsen nauwkeurig worden afgesteld. Sheetweerstanden worden gemeten en thermische simulaties worden uitgevoerd om temperatuurprofielen te bestuderen. De resultaten laten zien dat de totale laserenergie die voor een complete activering nodig is toeneemt met de tijd tussen de twee pulsen. De toename kan worden gecompenseerd door verwarming van het substraat. Door ongelijke pulsenergieën te gebruiken vindt eerder volledige scheiding plaats; om het smelten te maximaliseren is voorverwarmen effectiever dan verwarmen achteraf. De toegang tot laseropstellingen met twee pulsen geeft meer vrijheid bij het afstemmen van de thermische belasting.

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About the author

Viktor Gonda was born in Budapest, Hungary, on April 8, 1973. He received the Bachelor's degree in mechanical engineering from the College of Dunaujvaros and the Master's degree from the Technical University of Budapest, Hungary in 1997 and 2001, respectively. He completed his Master thesiswork at the Laboratory of Engineering Mechanics at the Delft University of Technology, the Netherlands, supported by a Huygens scholarschip. In 2002-2003 he worked as a research fellow in Delft and partly at Philips CFT in Eindhoven in the topics of mechanics of microelectronic materials. He started his PhD in prof. Lis Nanver's group at the Laboratory of Electronic Components, Technology and Materials at the Delft University of Technology in 2003.