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RESEARCH ARTICLE

Energy-Based Voltage Stabilization in DC Shipboard Power Systems With Dual Loop Control

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ABSTRACT The electrification of shipboard power systems carries an increasing variety in power sources, energy storage systems, and power converters. DC distribution is gaining relevance due to efficiency increase, space savings, and high controllability. The dominant primary control method voltage droop control, which offers easily implementable and scalable power sharing and voltage stabilization. However, compared to terrestrial microgrids, shipboard power systems have low line impedances and highly fluctuating loads. Most primary loads are power-controlled, introducing a non-linearity that leads to a weak damping and unstable operation points. To handle this non-linearity, this study proposes an energy-based control approach as an alternative to the voltage-based scheme. The controller is further extended by integral feedback loop to achieve fast voltage restoration. A low-bandwidth communication is leveraged for an adaptive power sharing control that facilitates an efficient allocation of the load among parallel units under varying conditions. The proposed control structure is deployed on an I/O board embedded in a hardware-in-the-loop testbed. It is shown that the energy-based controller operates stably and achieves a reduced voltage deviation from the nominal voltage in various load conditions compared to the conventional voltage-based method.

INDEX TERMS DC grid, dual loop control, HiL simulation, primary control, shipboard power system, voltage stabilization.

I. INTRODUCTION

Modern shipboard power systems (SPSs) are subject to a multitude of developments in the context of decarbonizing the maritime sector. Key changes encompass ship electrification, DC distribution technology [1], as well as the introduction of energy storage systems (ESSs) and zero-emission power supplies [2], [3]. Such systems can be regarded as islanded DC microgrids [4]. Several aspects set SPSs apart from terrestrial power systems. The number and variety of components are considerably lower, and the network's impedances are often negligibly small. The main loads are subject to high fluctuations and are typically power-controlled, e.g.,

propulsion machinery and service equipment. In addition, SPSs must follow special requirements for power availability, influencing the power system architecture and its control. In an integrated DC power system, it is key to maintain the bus voltage around its nominal value, and to prevent a loss of load or even a blackout. Hence, fast and accurate voltage stabilization and restoration are crucial objectives, which are further aggravated in systems with constant power loads (CPLs), low inertia and negligibly low line impedances. This study focuses on the primary and secondary control layers, as described in [5], [6], covering the voltage stabilization and restoration with parallel power sources.

The conventional primary control strategy is voltage droop, a decentralized method that does not require any communication [7]. Droop-based strategies are generally

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avored since they allow a system extension and require no high-bandwidth communication, thereby offering modular characteristics [8]. In the context of voltage stability with CPLs, a comparative analysis of standard droop schemes in DC microgrids is conducted in [9]. The effect of the negative incremental impedance of CPLs and the consequent weak damping of the power system is analyzed in [10]. Several studies delve into non-linear control approaches for the stabilization with CPLs [11]. However, these approaches typically investigate a single converter supplying one CPL [12], [13], [14], [15], [16]. Several works attempt to increase the stability of droop-controlled systems with CPLs by extending the standard droop scheme with virtual impedances and filters [10], [17], [18], [19]. Although these studies address stability with a CPL in droop-controlled systems, a decentralized method for parallel control of power converters that directly addresses the non-linearity between the voltage-based controller and the power load is lacking. Passivity-based approaches for DC link stabilization regard the power system control from an energy-based perspective [13], [14], [15], [16]. Following this concept, this study proposes the adaptation of an energy-based scheme for stabilizing low-inertia, low-impedance DC power systems. The energy-based approach offers the scalability and modularity of conventional droop control, due to its decentralized architecture, while improving the system stability and voltage restoration speed by explicitly accounting for the non-linearity of CPL.

As a drawback, standard droop control yields a steady-state voltage deviation, which requires the implementation of a secondary control layer for voltage restoration. Conventionally, this function is centralized and reference changes are broadcast via communication links [6], [7], [20]. The centralized voltage restoration is accurate [8], but slow, especially without a high-bandwidth communication [6], [21]. To increase the control speed, this study considers a local implementation of the voltage restoration, yielding a dual loop controller. Several studies attempt a local implementation of PI loops, increasing the speed of voltage restoration [22], [23], albeit at a loss of power sharing accuracy. However, inaccuracies in the power sharing can be compensated by additional methods utilizing low-bandwidth information sharing, e.g., via average current sharing [8], droop coefficient adaptation [24], [25], or voltage reference shifting [26], [27]. In this work, an adaptive power sharing control loop supported by a low-bandwidth communication network is proposed. This facilitates a compensation of power sharing imbalances arising from the decentralized control architecture and ensures that the power ratio of parallel components is accurately tracked while maintaining a fast voltage stabilization and restoration.

To summarize, the main contributions of this work are as follows. 1) An energy-based dual loop control scheme to increase stability and damping of the bus voltage with fluctuating loads in DC SPSs with CPLs; 2) An adaptive power sharing loop utilizing low-bandwidth communication

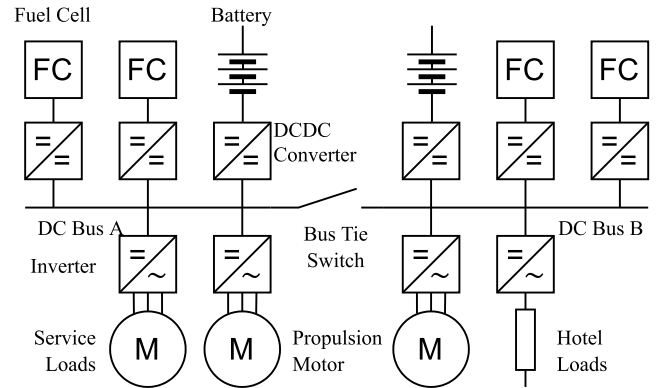


FIGURE 1. Exemplary shipboard power system topology with FC-battery hybrid energy system with DC distribution and power electronics-interfaced subsystems.

to ensure accurate power sharing among parallel power supplies.

This paper first introduces the considered SPS topology and the modeling approach for the system and its components in Section II. In Sections III and IV, the conventional and the proposed energy-based droop scheme are analyzed, and the controllers are tuned via pole placement. Furthermore, the adaptive power sharing control is described here. A HiL testbed for the validation is presented in Section VI, where the performance and applicability of the proposed control strategies are demonstrated. For this purpose, two test setups, for control of a single converter and for parallel control, are deployed on the testbed. Finally, the results and conclusions of these contributions are summarized in Section VII.

II. SYSTEM DESCRIPTION AND MODELING

This study considers the primary systems of a fully electrified SPS with DC distribution and power converter-interfaced components. The load-side converters follow a power demand, while the generation-side converters stabilize the bus voltage. Here, batteries are implemented as ESSs and fuel cells (FCs) are incorporated as zero-emission power supplies. Accordingly, no inertia from conventional engines remains. An exemplary topology is shown in Fig. 1. This section describes the modeling approach for the power sources, DC-DC converters, DC distribution system, and power loads.

A. POWER SOURCES

For the power sources, i.e., the ESSs and FCs, dynamic simulation models are implemented using static current-voltage curves and first-order transfer functions. The models are parameterized based on manufacturer data. The ESSs are represented by Li-ion batteries using standard parameters following the approach in [28]. Hydrogen proton-exchange membrane FCs are represented using a similar model from [29].

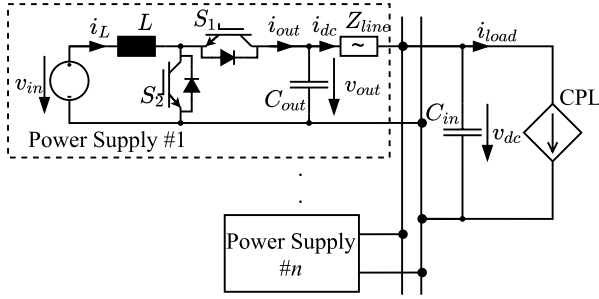


FIGURE 2. Equivalent circuit of the modeled DC system with constant power load and multiple idealized power supplies connected via half-bridge DC-DC converters.

B. DC-DC CONVERTERS

The DC-DC converters are modeled as half-bridges, as implemented in [30]. This topology allows bi-directional power flows, although the operation of the FCs is limited to positive power flows into the DC bus. Since this work focuses on the coordinated control of multiple sources, the high-frequency switching actions of the transistors are neglected. Hence, the converters are implemented as averaged models, as in [31] and [32].

Fig. 2 shows the equivalent circuit of a synchronous boost converter connected to the DC bus. The dynamics of the averaged inductor current i_L in this topology can be computed as

$$\frac{di_L}{dt} = \frac{1}{L}(v_{in} - (1-d)v_{out}) \quad (1)$$

where v_{in} and v_{out} signify the source and output voltages where $v_{in} < v_{out}$, and L the converter's inductance. d is the duty cycle of switch S_2 , serving as the control input in boost mode. In buck mode, switch S_1 is operated with duty cycle $\tilde{d} = 1 - d$. Each converter is additionally equipped with an output capacitance C_{out} such that the output voltage is given as

$$\frac{dv_{out}}{dt} = \frac{1}{C_{out}}(i_{out} - i_{dc}) = \frac{1}{C_{out}}((1-d)i_L - i_{dc}) \quad (2)$$

where i_{out} is the current flowing from the power supply to the DC bus. The local current controller is implemented as a PI feedback controller, tracking a reference for i_{out} obtained from the primary control level. Multiple half-bridges in parallel can be used to connect a power supply as an interleaved converter. In this case, each phase leg is controlled individually following the method above.

C. DC DISTRIBUTION SYSTEM AND POWER LOADS

The most significant system loads are constituted by the propulsion motors and service equipment. These loads are typically interfaced with inverters are regulated such that they draw a constant power. Hence, on the system level, these loads can be seen as CPLs, which are characterized by their negative incremental resistance, i.e., a voltage drop yields an increasing current draw at constant power. All loads are modeled as an aggregated CPL given as an exogenous input

p_{load} . Using the DC bus voltage v_{dc} over the load's input capacitance C_{in} , the power demand can be translated to a load current $i_{load} = p_{load}/v_{dc}$. The interconnection of power supplies, loads, and the DC bus is depicted in Fig. 2. Each power supply is connected to the DC bus via a line impedance Z_{line} , modeled as a series RL-element. The output current of each i -th converter connected to the bus can be denoted as $I_{dc,i}$, and the time derivative of the DC-link voltage $\frac{d}{dt}v_{dc}$ can then be computed as

$$\frac{d}{dt}v_{dc} = \frac{1}{C_{in}}\left(\sum_{i=1}^N I_{dc,i} - i_{load}\right) \quad (3)$$

III. CONVENTIONAL DROOP CONTROL

This section introduces voltage-based droop as the conventional primary control method, including an extension by an integral action for bus voltage restoration. Assumptions for the local control and a simplification of the plant model for the controller synthesis are presented. Subsequently, transfer functions for the conventional control are derived and control parameters are determined via pole placement.

A. LOCAL CONTROL

Each power converter has a local controller regulating its output current. Local PI current controllers are implemented, which are tuned such that they meet the designed bandwidth of the current control loop (see [22]). In the context of a modular system design, we assume the utilization of off-the-shelf power converters with a fixed switching frequency and limited current control speed which, for SPSs, is typically in the range of 1000 Hz [33]. For the controller synthesis, the current control transfer function H_{cc} is simplified as a first-order low-pass filter with unitary gain and current control bandwidth ω_{cc} .

B. VOLTAGE DROOP

In SPS, line impedances are typically very low. In the considered power system, the time constants comprised of each module's output filter and line impedance are significantly faster than the current control speed of the power electronics converters. This means that the voltage balances faster among the distributed capacitances than the decentralized controllers act. This allows the simplified representation of the entire DC bus as a lumped capacitance C_{dc} , which is approximated as the sum of all power supplies' output capacities and the load's input capacitance. This assumption requires that the electrical distance between components is sufficiently small such that the balancing of voltages between the distributed capacitances occurs faster than the current control dynamics. This approach is in line with the model description for DC SPSs proposed in [4]. Hence, for the control, the DC bus is modeled with transfer function

$$\frac{v_{act}}{i_{act} - i_{load}} = \frac{1}{sC_{dc}} \quad (4)$$

where v_{act} is the DC bus voltage, i_{act} the total current from all power supplies, and i_{load} the current drawn by the load.

The conventional droop scheme operates in voltage-mode, where each device computes a target output voltage as

$$v_{ref} = V_{nom} - R_d i_{out} \quad (5)$$

where V_{nom} is the nominal bus voltage, R_d is a virtual resistance and i_{out} is the measured output current. Power sharing among parallel devices is realized by tuning the virtual resistances inversely proportional to the source's rating.

The same scheme can be transformed such that a current reference is obtained based on the output voltage measurement, which is more appropriate for the considered SPS with negligibly small line impedances. This scheme's block diagram for a single power supply is shown in Fig. 3. The current reference i_{ref} is determined as

$$i_{ref} = (v_{ref} - v_{msr})H_{vc} \quad (6)$$

where H_{vc} is the transfer function of the droop controller. Furthermore, the real measured feedback signal v_{msr} of the bus voltage includes measurement noise d_m , and the power load p_{load} acts as an input disturbance on the plant. Conventionally, a proportional gain is used, such that $H_{vc} = \frac{1}{R_v}$. Both the voltage- and current-mode droop schemes yield an equivalent steady-state behavior and similar dynamic responses. A more detailed comparison, including stability analysis, is presented in [9]. In this work, the current-mode droop control is considered the baseline approach.

C. VOLTAGE RESTORATION

In steady state, conventional droop schemes yield a non-zero voltage error $\Delta v = v_{ref} - v_{msr}$. This can be mitigated by implementing an integral gain on the voltage error, yielding a dual loop approach with PI feedback control. The integral action is often realized in a central, secondary control layer [6]. To achieve a fast voltage restoration, however, a local implementation is more desirable, as in [23]. Accordingly, instead of a virtual resistor, as in the standard voltage droop in (6), a PI controller with proportional gain k_p and integral gain k_i is implemented. The current reference is then generated according to

$$i_{ref} = k_p \Delta v + \frac{k_i}{s} \Delta v \quad (7)$$

D. DUAL LOOP CONTROL DESIGN

To analyze the dynamic behavior and tune the control parameters, we first simplify the system shown in Fig. 3. The voltage control bandwidth ω_{vc} should be sufficiently slower than the current control ($\omega_{vc} \ll \omega_{cc}$). Hence, in the controller synthesis, we disregard the transfer function of the current controller and assume $H_{cc} \approx 1$, yielding $i_{act} = i_{ref}$. We further disregard measurement noise in this study, such that $v_{msr} = v_{act}$. For the performance of the voltage stabilization, the controller's ability to compensate for input

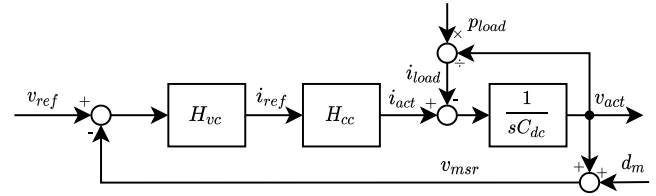


FIGURE 3. Block diagram of conventional voltage-based scheme in current-mode including input and measurement disturbances.

disturbances is decisive for minimizing the set point error, while the reference voltage typically does not change. Hence, we consider the transfer function G_{do} from disturbance, i.e., the unknown CPL, to the actual bus voltage. Due to the negative incremental resistance of power-controlled loads, the CPL introduces a non-linear feedback loop from the DC bus voltage to the load current. Hence, we linearize the load current around the nominal voltage V_{nom} as $\tilde{i}_{load} = p_{load}/V_{nom}$. The voltage dynamics can then be described as

$$v_{act} = (v_{ref} - v_{act})H_{vc} \frac{1}{sC_{dc}} \quad (8)$$

The transfer function of the voltage-based dual loop control is then obtained as

$$G_{do} = \frac{v_{act}}{i_{load}} = -\frac{1}{sC_{dc} + H_{vc}} = -\frac{s}{s^2 C_{dc} + s k_p + k_i} \quad (9)$$

By analyzing the denominator of (9), it can be derived that the poles of G_{do} , lie at

$$s_{1,2} = -\frac{k_p}{2C_{dc}} \pm \sqrt{\left(\frac{k_p}{2C_{dc}}\right)^2 - \frac{k_i}{C_{dc}}} \quad (10)$$

We select the PI gains to place the poles of G_{do} at the desired voltage control bandwidth ω_{vc} . Eliminating the term under the square root in (10) ensures a fast voltage restoration while ensuring the poles do not contain imaginary parts. This yields

$$k_p = \omega_{vc} \hat{C}_{dc} \quad \text{and} \quad k_i = \frac{k_p^2}{4\hat{C}_{dc}} \quad (11)$$

Although popular due to its simplicity, ease of implementation, and decentralized architecture, the voltage-based approach has a series of limitations. One key challenge is posed by the operation of loads in SPSs at constant power. Fig. 3 outlines the dependence of the load current on the actual DC bus voltage. The conventional scheme attempts to reject disturbances originating from a power load via the current as an input variable. However, the real system contains a non-linearity due to the feedback of the power load on the bus voltage. For this reason, we introduce an energy-based droop scheme, generating a power reference to stabilize the disturbance, in the following section.

IV. ENERGY-BASED VOLTAGE CONTROL

This section describes the proposed energy-based droop. The concept of energy-based control is introduced in the context of droop control, and subsequently, a dual loop

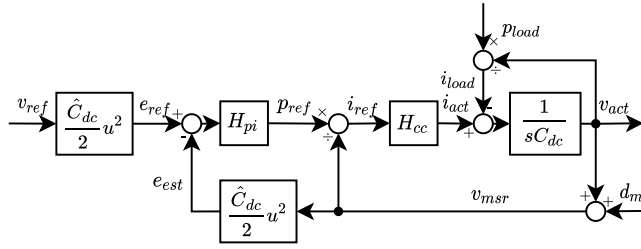


FIGURE 4. Block diagram of proposed energy-based control including input and measurement disturbances.

controller is designed via pole placement, analogously as in Section III. The stability of the proposed schemes are assessed, and finally the sensitivity of the proposed schemes to an inaccurate DC bus capacitance estimate and the underlying current control speed are analyzed.

A. ENERGY-BASED DROOP

The key step for setting up an energy-based droop scheme is transforming the voltage- and current-based control into a system where the energy in the DC bus is controlled via the input power. Using the voltage-energy relationship of capacitances and regarding the DC bus as a single capacitance C_{dc} , we can define a reference energy e_{ref} , as well as an estimate energy in the DC bus e_{est}

$$e_{ref} = \frac{\hat{C}_{dc}}{2} v_{ref}^2 \quad \text{and} \quad e_{est} = \frac{\hat{C}_{dc}}{2} v_{msr}^2 \quad (12)$$

$\hat{C}_{DC}$ is an estimate of the system's DC bus capacitance. In the energy-based scheme, the local controller computes a power reference, as opposed to a current reference in the conventional scheme. Since the lower level current control loop requires a current reference, the power reference is then transformed back. Using a proportional controller yields the energy droop scheme

$$p_{ref} = k_p(e_{ref} - e_{est}) \quad \text{and} \quad i_{ref} = p_{ref}/v_{msr} \quad (13)$$

This scheme is visualized in Fig. 4. Here, the linear relationship between controller output and input disturbance, which are power quantities, can be seen, setting the energy-based droop apart from the conventional strategy.

B. DUAL LOOP CONTROL DESIGN

As the conventional droop, the energy-based droop yields a steady-state voltage deviation without an integral action. As before, this is mitigated by feeding the energy error $\Delta e = e_{ref} - e_{est}$ through a PI loop.

$$p_{ref} = (k_p + \frac{k_i}{s}) \Delta e \quad (14)$$

For the derivation of the transfer functions, no linearization of the CPL is required in the energy-based scheme since now the disturbance and controller output are both power quantities. In the relationship between disturbance and output G_{do} , the

squared bus voltage is regarded:

$$v_{act}^2 = \frac{2}{C_{dc}} e_{act} = \frac{2 p_{ref} - p_{load}}{s C_{dc}} \quad (15)$$

$$p_{ref} = -H_{pi} \frac{\hat{C}_{dc}}{2} v_{act}^2 \quad (16)$$

$$G_{do} = \frac{v_{act}^2}{p_{load}} = -\frac{s}{s^2 \frac{C_{dc}}{2} + s \frac{\hat{C}_{dc}}{2} k_p + \frac{\hat{C}_{dc}}{2} k_i} \quad (17)$$

Hence, we see that the disturbance has a linear effect on the stored energy, or alternatively, on the squared DC bus voltage. Again, the voltage controller shall be tuned to reject disturbances according to the desired voltage control bandwidth ω_{vc} . The poles of the transfer function G_{do} in (17) are located at

$$s_{1,2} = -\frac{\hat{C}_{dc}}{2C_{dc}} k_p \pm \sqrt{(\frac{\hat{C}_{dc}}{2C_{dc}} k_p)^2 - \frac{\hat{C}_{dc}}{C_{dc}} k_i} \quad (18)$$

With an accurate DC bus capacitance estimate, i.e., $\hat{C}_{dc} = C_{dc}$, the poles can be placed as desired by setting

$$k_p = \omega_{vc} \quad \text{and} \quad k_i = \frac{k_p^2}{4} \quad (19)$$

Inserting (19) into (17) and (18) yields the closed-loop transfer function of the designed controller and the location of its poles:

$$G_{do} = -\frac{s}{s^2 \frac{C_{dc}}{2} + s \frac{\hat{C}_{dc}}{2} \omega_{vc} + \frac{\hat{C}_{dc}}{8} \omega_{vc}^2} \quad (20)$$

$$s_{1,2} = -\frac{\omega_{vc} \hat{C}_{dc}}{2C_{dc}} \pm \frac{\omega_{vc}}{2} \sqrt{(\frac{\hat{C}_{dc}}{C_{dc}})^2 - \frac{\hat{C}_{dc}}{C_{dc}}} \quad (21)$$

C. DISTURBANCE REJECTION

To analyze the stability of the proposed controller, we regard the disturbance transfer function G_{do} of voltage- and energy-based schemes, with and without voltage restoration, to assess the deviation of the bus voltage as a function of the load. Fig. 5 shows the corresponding gain for the different control schemes, over varying load frequencies. The data in this figure is generated via numerical simulations, injecting a load power with varying frequency and magnitude to the modeled system, and logging the bus voltage.

All controllers reject load disturbances with frequencies significantly smaller than the voltage control bandwidth very well, whereas the DC bus capacitance filters out high-frequency loads. The gain of energy-based scheme is only affected by the load frequency but remains unaffected by the load magnitude. The transfer function of voltage-based control shows an additional dependency on the load amplitude. At low magnitudes, its gain matches those of the energy-based schemes. However, at higher load magnitudes, the gain increases, due to the non-linear relationship to the constant power load. Beyond a certain magnitude, the voltage-based control becomes unstable and tends towards infinity, as indicated in Fig. 5. Purely proportional voltage

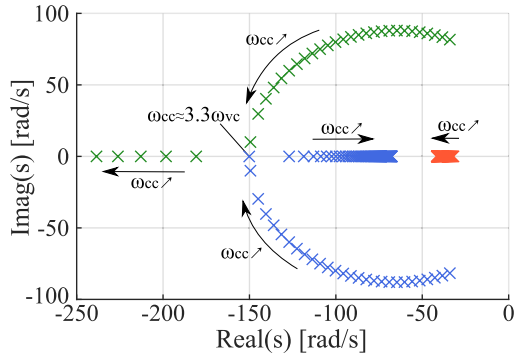


FIGURE 8. Root locations of disturbance-output transfer functions for variation of the current control bandwidth for energy-based control with PI loop.

reduced current control speed shifts the pole locii, lowering the frequency of the slowest pole and possibly introducing imaginary pole pairs. This highlights the importance of ensuring that the inner control loop is sufficiently fast enough. In practice, the achievable or available speed of the the inner loop limits the realizable voltage control speed.

V. PARALLEL CONTROL

In the previous sections, the bus stabilization with a single controlled power supply has been investigated. The decentralized design requires applying the proposed strategy to the parallel control of multiple power sources. This section discusses the design of a coordinated control between multiple parallel ESS, and coordination with main power supplies for bus stabilization and efficient dispatch of resources.

A. POWER SHARING AMONG PARALLEL ESS

We assume that multiple ESS systems are connected to the DC SPS and are responsible for the stabilization of the bus voltage. Every system has an individual available power $P_{av,i}$. The total available power in the system follows from the sum of all N units as

$$P_{av,tot} = \sum_{j \in N} P_{av,j} \quad (23)$$

The actual supplied power of each unit can be computed locally as

$$P_{act,i} = v_{out,i} i_{out,i} \quad (24)$$

and the sum of all power outputs yields the total supplied power

$$P_{act,tot} = \sum_{j \in N} P_{act,j} \quad (25)$$

We define the goal of the power sharing among parallel power supplies to ensure that the ratio of power output to available power is equal for all units. For this we define the

actual power sharing gain as

$$\gamma_{act,i} = \frac{P_{act,i}}{P_{act,tot}} \quad (26)$$

whereas the desired reference for the power sharing gain is

$$\gamma_{ref,i} = \frac{P_{av,i}}{P_{av,tot}} = \frac{P_{av,i}}{\sum_{j \in N} P_{av,j}} \quad (27)$$

Since the local controllers cannot measure the power output of other units, we introduce a central control unit connected via a low-bandwidth communication network. This controller collects the individual power outputs $P_{act,i}$ and available power levels $P_{av,i}$ from all units and broadcasts $P_{act,tot}$ and $P_{av,tot}$. Thus, the required information is made available for all local controllers to compute $\gamma_{ref,i}$ and $\gamma_{act,i}$. The control architecture and signal exchange is visualized in Fig. 9 To realize the power sharing according to the available power, each local energy control loop is modified by multiplying the PI-controller output with $\gamma_{ref,i}$, as can be seen in Fig. 9.

In a real system, multiple factors influence the accuracy of the desired power sharing. These encompass sensor noise and bias, parallel processing on different controller hardware, unequal line impedances, and further effects. To compensate for a mismatch between $\gamma_{ref,i}$ and $\gamma_{act,i}$, we introduce an adaptive droop gain $r_{d,i}$ which shifts the individual reference energy $e_{ref,i}$. Adaptive techniques with droop gain variation have been shown to be effective in compensating imbalances [6]. Here, we initially set the droop gain to zero and only use small values to compensate for power sharing imbalances. The gain is then controlled using a PI loop as

$$r_{d,i} = (\gamma_{act,i} - \gamma_{ref,i}) \left(k_{p\gamma,i} + \frac{k_{i\gamma,i}}{s} \right) \quad (28)$$

with control gains $k_{p\gamma,i}$ and $k_{i\gamma,i}$. Following the nominal voltage V_{nom} , the adjusted energy reference is obtained as

$$e_{ref,i} = \frac{\hat{C}_{dc}}{2} V_{nom}^2 - r_{d,i} P_{out,i} \quad (29)$$

B. COMMUNICATION FAILURE

A key challenge of a centralized controller, as proposed here for the power sharing control loop, is its vulnerability towards faults in the high-level control or communication. To mitigate this, the system can safely transition to a purely decentralized fallback mode after a communication fault. In fallback mode, the power sharing control switches to a droop-based approach that affects the reference voltage $e_{ref,i}$ with a fixed droop gain $R_{fb,i}$:

$$e_{ref,i} = \frac{\hat{C}_{dc}}{2} V_{nom}^2 - R_{fb,i} P_{out,i} \quad (30)$$

That droop gain is set inversely proportional to the unit's power rating. This approach resembles a conventional droop approach in voltage mode, albeit transformed to an energy-based framework. The approach is known to provide accurate power sharing at high droop resistances, with the drawback of a steady-state voltage deviation from the nominal value [34].

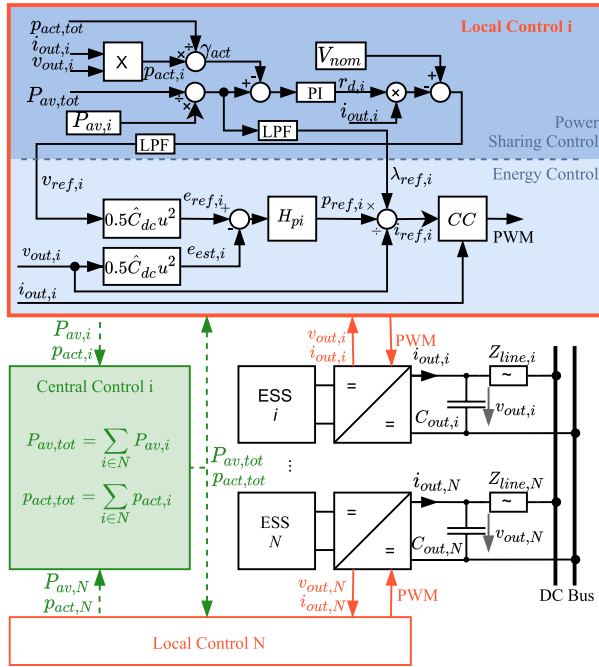


FIGURE 9. Control and communication architecture for parallel control of multiple power sources.

C. POWER SPLIT BETWEEN ESS AND MAIN POWER SUPPLIES

This study focuses on the stabilization of the DC bus using fast-responding power system components, e.g., batteries, to compensate for imbalances between load and generation dispatch. Considering an all-electric SPS with ESSs and FCs, as shown in Fig. 1 this is required due to low transient capabilities of the FCs. The generation dispatch is an output from the energy management layer, giving set-points to the main power supplies to meet the estimated load, and to ESSs for state-of-charge (SoC) management additional support. The energy management and SoC management are out of scope for this study, since their time-frame is considerably slower than the voltage stabilization and restoration, and in a hierarchical control architecture, each layer may be addressed individually. However, important for the method presented in Section V-A, is that the available power values $P_{av,i}$, $P_{av,tot}$, $P_{act,i}$, and $P_{act,tot}$ only account for available and supplied power to compensate for power imbalances. Otherwise, the energy management set-points would interfere with the voltage stabilization and vice-versa.

VI. RESULTS

For validation of the proposed control methods, a hardware-in-the-loop (HiL) simulation environment is used. This section introduces the HiL test setup, describes the deployment of controllers and plant model and discusses the results of various test-cases for a single-converter and parallel control setups.

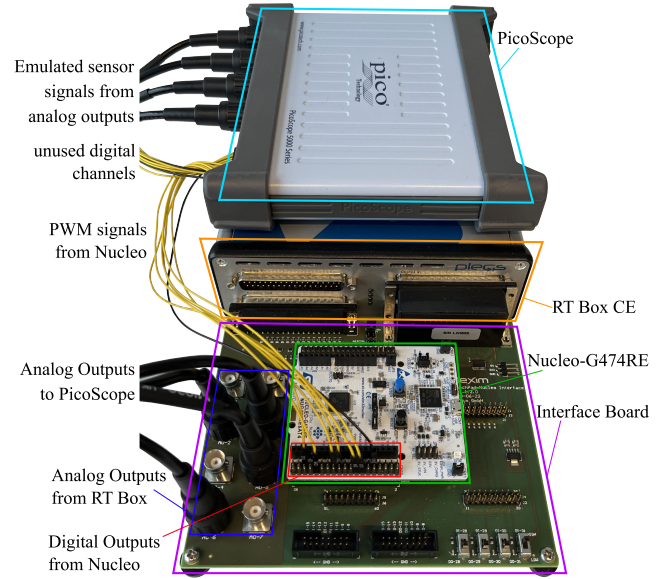


FIGURE 10. HiL simulation test setup consisting of Plexim RT Box CE real-time target machine, STM32 Nucleo-G474RE I/O Board, a dedicated interface board, and PicoScope oscilloscope for measurement logging.

A. HiL TESTBED

The HiL testbed used for the investigations is shown in Fig. 10. The plant model, comprised of energy source(s), power converter(s), DC distribution system, and loads, is implemented in a Plexim RT Box CE ([35]), a dedicated real-time simulation platform for power electronics systems. The digital control is deployed on the STM32 Nucleo-G474RE I/O Board ([36]), which is able to capture the emulated sensor signals from the RT Box and generate pulse-width modulation (PWM) signals for the actuation of the virtual power switches in the plant model. Both the plant model as well as the digital control are implemented in PLECS, using available block-sets for the RT Box and STM32 Nucleo board to handle inputs and outputs. The analog and PWM signals are measured directly on the I/O board pins via a PicoScope oscilloscope ([37]).

B. SINGLE CONVERTER

In a first step, the performance of the proposed controllers is tested in a single converter topology, as shown in Fig. 11. For this purpose, a power source is connected to the DC system via a three-phase interleaved DC-DC converter, whose output current i_{out} is to be controlled to stabilize the DC bus voltage v_{dc} . The power converter is connected to the DC grid via a line impedance Z_{line} . The capacitances of the remaining grid components, which in this case are not participating in the voltage stabilization, are modeled as an aggregated capacitance C_{grid} series-connected with an equivalent impedance Z_{grid} . The system loads are modeled as an aggregation of resistive loads R_{load} and power controlled loads CPL . These are connected to a capacitance C_{dc} which is the reference point for the DC bus voltage v_{dc} .

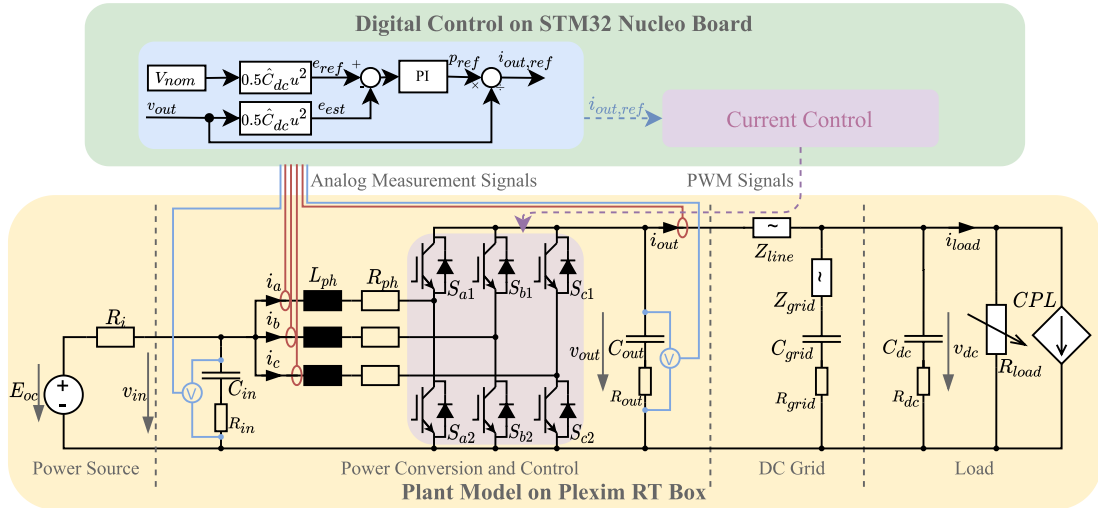


FIGURE 11. Plant model and digital control implementation for HiL simulation of single power source connected to DC grid via three-phase interleaved converter feeding resistive and constant power loads.

An output filter capacitance C_{out} is attached to the converter output to reduce its voltage ripple and, similarly, an input capacitance is connected on the source-side. The voltages v_{out} and v_{in} over the respective output and input terminals, are measured and captured by the digital control. In addition, the total output current i_{out} , as well as the three phase currents are measured. The parameters for this test setup are listed in Table 1.

The digital control is comprised of a voltage or energy control loop and a current control loop, which receives a current reference $i_{out,ref}$ from the former. The current control translates this into references for the inductor currents, which are realized as three individual PI-controllers with anti-windup via back propagation. The PWM generation of the three phase legs is shifted symmetrically such that the current ripple at the output is minimized.

1) STEP RESPONSE

For the operation of the power system, it is crucial to ensure that the DC bus voltage stays within its required limits. A critical case is the possibility of an undervoltage due to a sudden load step or a loss of generation. Due to its limited size, compared to terrestrial power systems, the loss of a power generation system can account for a significant share of the total installed power. In the reference design shown in Fig. 1, 50 % of the FC systems can be disconnected instantaneously due to a single fault. To test the voltage stabilization and restoration via the proposed control scheme, we test the system response to an application of a load step as a fraction of the total installed FC power, mimicking the disturbance occurring due to a severe loss of generation while operating at full power. Fig. 12 shows the voltage stabilization after load steps of 650 kW and 1300 kW, amounting to half and full load power, for voltage and energy based droop control schemes without voltage restoration. The controllers

TABLE 1. Plant model and control parameters for HiL simulation.

Parameter	Description	Value
V_{nom}	Nominal DC-link voltage	700 V
E_{oc}	Voltage source	400 V
L_{ph}	Phase inductance	500 μ H
C_{in}	Input capacitance	10 mF
C_{out}	Output capacitance	20 mF
C_{dc}	DC link capacitance	20 mF
C_{grid}	Remaining grid capacitance	40 mF
Z_{line}	Line impedance single unit	63.9 $\mu\Omega$, 3.2 μ H
$Z_{line,A}$	Line impedance to unit A	63.9 $\mu\Omega$, 3.2 μ H
$Z_{line,B}$	Line impedance to unit B	319.5 $\mu\Omega$, 16 μ H
Z_{grid}	Line impedance to remaining grid	31.9 $\mu\Omega$, 1.6 μ H
R_{ph}	Phase resistance	0.5 $\mu\Omega$
R_i	Power source resistance	10 m Ω
R_{in}	ESR of C_{in}	15 m Ω
R_{out}	ESR of C_{out}	15 m Ω
R_{dc}	ESR of C_{dc}	15 m Ω
R_{grid}	ESR of C_{grid}	7.5 m Ω
$P_{load,max}$	Maximum CPL load	1300 kW
$R_{load,full}$	Resistive load at full power	376.9 m Ω
$P_{av,A}$	Available power unit A	650 kW
$P_{av,B}$	Available power unit B	325 kW
f_{sim}	Sampling rate of RT Box	250 kHz
f_{sw}	Switching frequency	10 kHz
ω_{cc}	Current control bandwidth	1000 rad/s
ω_{vc}	Voltage control bandwidth	100 rad/s
$k_{p\gamma,i}$	γ -control proportional gain	— 2500
$k_{i\gamma,i}$	γ -control integral gain	— $\frac{P_{av,i}}{25000}$
$R_{fb,i}$	Droop gain in fallback mode	— $\frac{P_{av,i}}{1500}$

are tuned such that the voltage droop controller yields a 10 % voltage deviation at half load, and the energy droop is tuned to match the control bandwidth. Results show that the energy-based droop, when tuned for the same control bandwidth, achieves a lower voltage drop due to its non-linear characteristics. The relative difference between the two control schemes, increases progressively with the magnitude of the load.

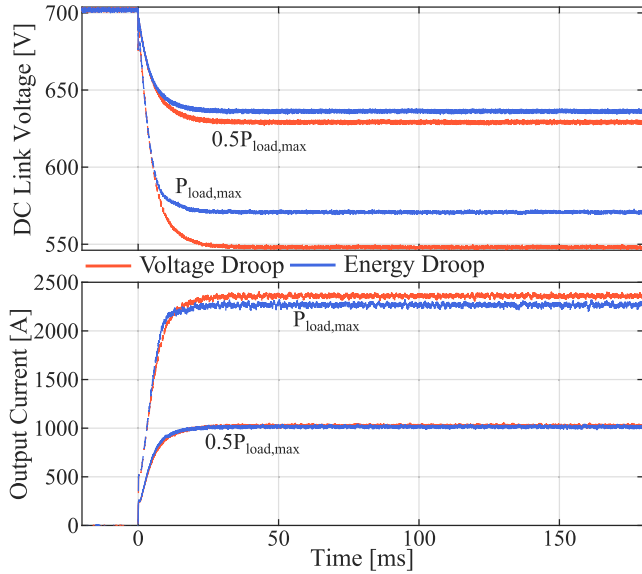


FIGURE 12. Voltage and energy droop with power load.

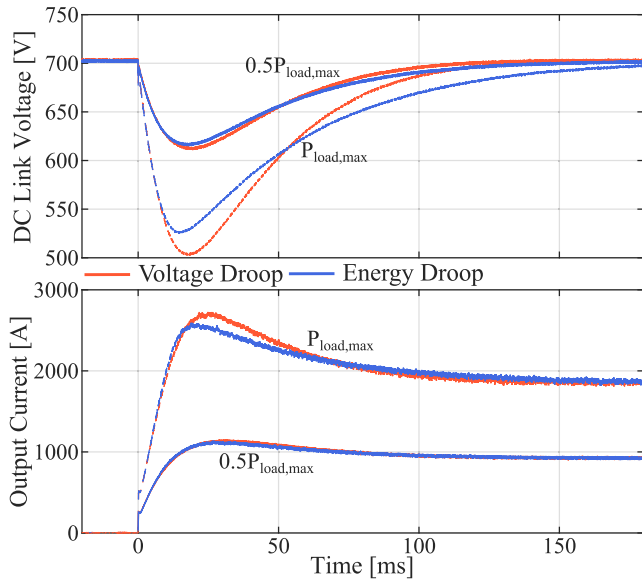


FIGURE 13. Voltage and energy dual loop control with power load.

Fig. 13 shows the results for the same test case with dual loop controllers to restore the voltage. As before, a difference of the voltage stabilization speed and voltage sag becomes clear when we consider power loads. With an increase in load step magnitude, the voltage sag of the conventional controller becomes progressively larger while the energy-based scheme keeps the voltage drop roughly proportional to the load magnitude.

2) FREQUENCY RESPONSE

Apart from ensuring the maintenance of the bus voltage within critical limits, it is key to evaluate the controller's stability and its overall disturbance rejection capabilities.

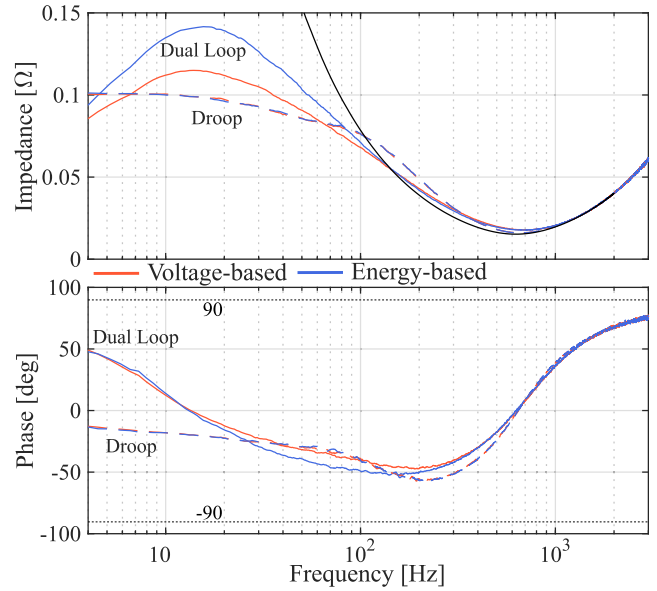


FIGURE 14. Observed controller output impedance at DC bus in HiL simulation via injection of voltage error (v_{dc}/i_{out}).

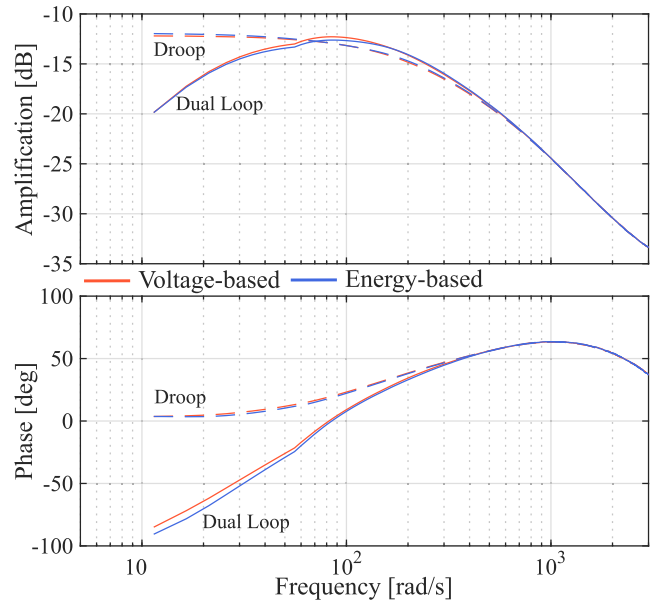


FIGURE 15. Observed controller disturbance rejection in HiL simulation via injection of oscillating load power (amplification in $[V^2/W]$).

To this end, we analyze the open-loop output impedance of the controller by applying a sinusoidal voltage disturbance to the DC bus voltage v_{dc} and measuring the output current as a reaction to the voltage variation. Fig. 14 show the impedance of the four control schemes, computed as $-\frac{\Delta v_{dc}}{i_{out}}$. The region below the target control bandwidth shows an increased impedance of the energy-based controller, compared to the conventional voltage-droop, meaning that a lower output current is supplied by the power converter. The real part of the impedance is positive over the tested frequency interval and voltage magnitude, meaning that the converter is passive

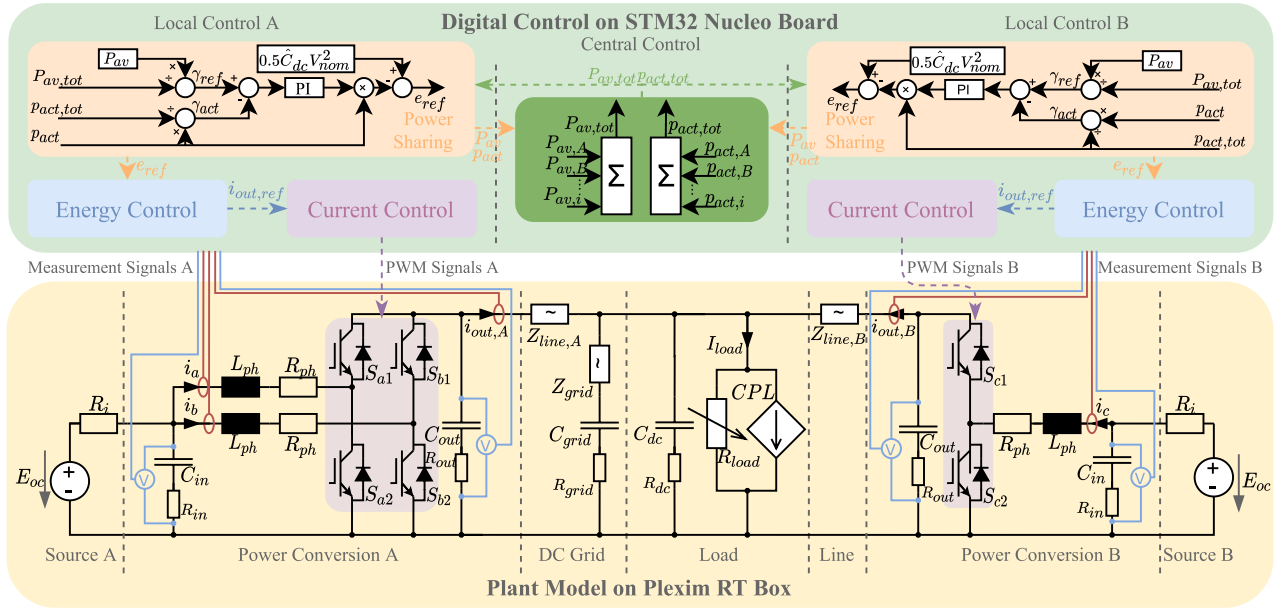


FIGURE 16. Plant model and digital control for HiL simulation of parallel power sources connected to DC grid with differently rated converters feeding resistive and constant power loads.

in this test case and no shortage of stability has been observed for either control approach.

In addition, we test the closed-loop frequency response of the bus voltage when applying a sinusoidal power controlled load to the system. The resulting bode plot of the disturbance rejection is displayed in Fig. 15. We see that the amplification is limited for all controllers and the dual loop schemes peak around the implemented control bandwidth. As expected, the voltage-based controller has a slightly elevated gain in the high-amplification region, which explains the increased voltage sag observed after a load step.

C. PARALLEL CONTROL

The parallel control of multiple DC-DC converters is tested via a different plant model. Fig. 16 shows the HiL simulation test setup with two differently rated sources and power converters feeding the DC system. Power source A is interfaced via a two-phase interleaved converter, while power source B, rated at half the power of source A, is connected via a single-phase synchronous converter. As for the previous case, the parameters for this test setup are listed in Table 1. The goal is to ensure that the overall voltage stabilization is achieved with the same quality as with a single converter while keeping the power sharing between the sources at the desired ratio.

Each converter has a local controller deployed on the STM32 Nucleo board, which have only access to the measurements belonging to their respective emulated hardware. In addition, a central control unit is implemented in the digital control, which receives information signals from the local controllers and periodically broadcasts information accessible to all local units.

1) LOAD STEP

The total system response the load is intended to be independent of the number of stabilizing power supplies, achieved by introducing the power sharing gain into the control loop, as shown in Fig. 9. To test this, the power system is subjected to a load step of 975 kW, equaling total power rating of power supplies A and B. The resulting output currents and DC bus voltage in this scenario are shown in Fig. 17. It can be seen that the voltage is restored within the same time frame as in the single-converter scenario. This shows that multiple parallel converters are able to stabilize and restore the voltage in the same manner as a single converter could.

2) POWER SHARING

Each local controller has only its local output voltage $v_{out,i}$ available. Furthermore, $Z_{line,B}$ is set to five times $Z_{line,A}$. Hence, even in steady-state operation, minor differences in measurements and voltage drops over the line will result in imbalances in power-sharing. The accuracy of the power sharing control described in Section V-A is tested by holding the load from the previous test case at a constant level for 30 s, and observing the ratio of output currents from power supplies A and B. The resulting measurements of currents for the parallel control without power sharing control and with power sharing control are shown in Fig. 18. The results show that, without intervention, the output currents of parallel converters diverge from the desired setpoint and already after less than a minute, the power sharing ratio has changed significantly (here: ca. 1.2:1 instead of the desired 2:1 after 30 s). However, including the central controller for power sharing control, the currents of both controllers are quickly

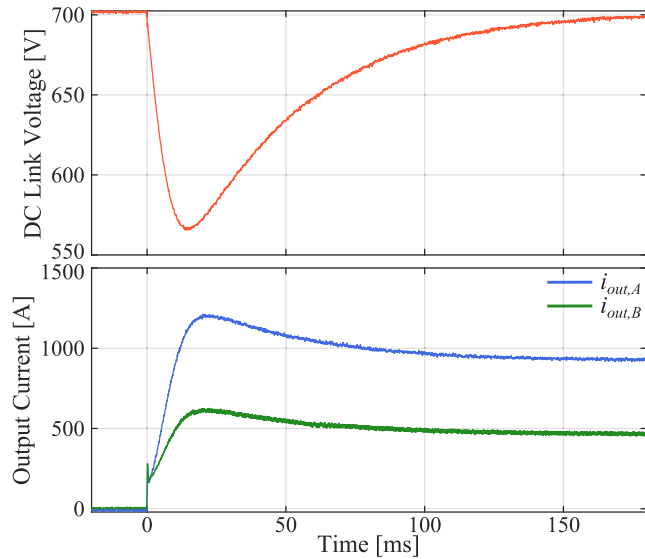


FIGURE 17. Voltage stabilization after load step with two parallel converters.

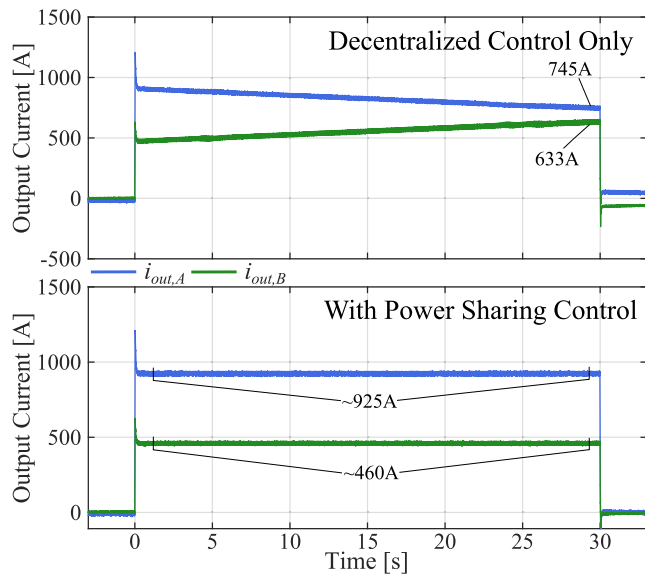


FIGURE 18. Power sharing between two parallel converters without and with adaptive power sharing loop.

stabilized at the desired setpoint. Here, this means a current ratio of two-to-one between units A and B.

3) FAULT CONSIDERATIONS

During the operation of the SPS, a fault can occur at any given time, affecting the ideal power sharing among parallel power supplies. The power sharing control is intended to adapt to such changes by modifying the local power sharing gains. To demonstrate this, we consider a fault in power supply A that leads to a reduction of its available power by 50 %. The currents of the parallel power supplies before and after the degradation of unit A are shown in Fig. 19. As intended,

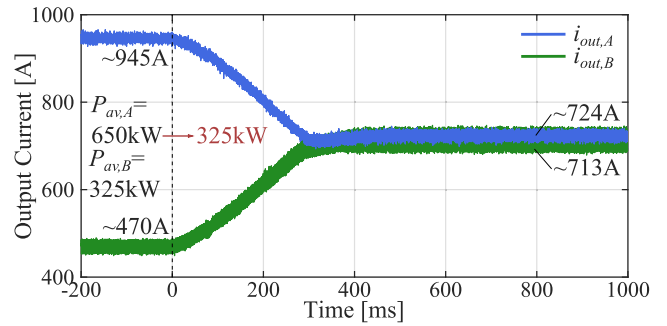


FIGURE 19. Adaptive power sharing between parallel converters during change of available power.

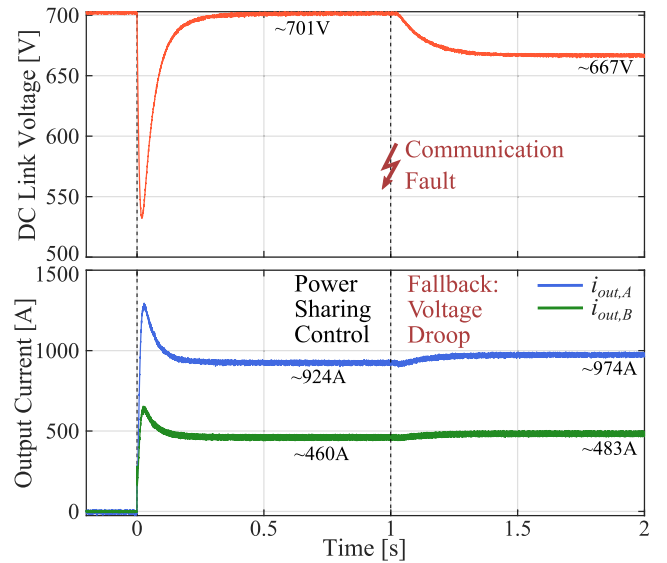


FIGURE 20. Current outputs of parallel converters before and after fallback mode due to communication failure.

before the fault ($t < 0$ s), unit A is carrying twice the current of unit B, matching the ratio of their available power. After the fault ($t > 0$ s), the power availability of both units is equal. Hence, the currents converge to the new, desired power sharing ratio, equally divided among both units. Following the same concept, the power sharing control can also adapt to deliberate variations of the available power of each units, e.g., arising from an optimized allocation of power reserve from a high-level controller.

The transition to fallback mode, as described in Section V-B, is displayed in Fig. 20. At time $t = 0$ s, a load step occurs with the original power sharing control still intact. At $t = 1$ s, the communication fails and both units switch to fallback mode, employing a fixed droop constant. As a result, the bus voltage is reduced, requiring both units to increase their currents to deliver the power demand. However, due to the comparably low droop gains, as opposed to the adaptive control regime, the power sharing ratio is still close to the desired value of two-to-one between units A and B.

VII. CONCLUSION

The decentralized voltage control for DC systems is a specific challenge for shipboard applications due to minimal line impedances and highly fluctuating CPLs, setting it apart from terrestrial DC microgrids, as well as DC links in automotive applications. Voltage-based droop as the state-of-the-art solution for decentralized power sharing is challenged due to the negative incremental resistance of CPLs, resulting in low damping and possibly voltage instability at high load steps. This study proposes a transformation of the voltage droop to an energy-based control scheme, eliminating the non-linear relationship between the power load and the controlled variable, where a power reference replaces the current reference of the state-of-the-art approach. HiL test results highlight the energy-based controller's improved performance in stabilizing the bus voltage even at high load steps, and its accurate voltage restoration according to the specified bandwidth, while conventional voltage-based control leads to increased voltage sags due to the low damping with CPLs. Assuming a fixed current controller of an off-the-shelf power converter, this enables fast restoration of the DC bus voltage with minimal deviations during transients. Hence, the proposed energy-based scheme serves as a crucial element for securing the power availability in decentralized systems with critical loads and a network with low capacitances and low line impedances. An adaptive power sharing loop lets parallel power supplies accurately track their desired power sharing ratio without compromising the control speed. This yields a stable and flexible voltage control, suitable for the implementation in modular power systems where number and rating of power supply units are variable.

Future work will see the proposed method embedded into complete hierarchical control schemes to investigate its interaction with energy and power management strategies. The flexibility of the proposed method is very suitable to interact with optimal power and reserve power allocations from a higher-level controller. Additionally, the proposed control design can further be fine-tuned and optimized with attention to application-specific performance criteria. Whereas this study focuses on voltage stabilization and regulation using an energy-based control scheme, the next step should expand the focus to include optimized power sharing, and battery SoC management, leveraging the low-bandwidth communication links in the system.

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