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A 0.8-V BJT-Based Temperature Sensor With an Inaccuracy of ±0.4 °C (3σ) From −40 °C to 125 °C in 22-nm CMOS

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***Abstract*— This article presents a compact sub-1-V bipolar junction transistor (BJT)-based temperature sensor for thermal management applications. To operate from a sub-1-V supply, two capacitors are first pre-charged to a supply-independent initial voltage (>1 V) by regulated charge pumps (RCPs) and then discharged through two diode-connected BJTs. By using different discharge times, proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) voltages can be generated. These are then read out by an area- and energy-efficient charge-balancing ΔΣ modulator to generate a digital representation of temperature. To reduce its noise, the modulator's first inverter-based integrator employs both chopping and auto-zeroing. Fabricated in a standard 22-nm bulk CMOS process, the sensor occupies 0.01 mm^2 and consumes 2.9 μW from a 0.8-V supply. It achieves a 1-point trimmed inaccuracy of ±0.4 °C (3σ) from −40 °C to 125 °C, which is the best reported in sub-65-nm CMOS. It also achieves high energy efficiency, resulting in a resolution figure of merit (FoM) of 0.41 pJ · K^2.**

***Index Terms*— ΔΣ modulator, capacitively biased (CB) bipolar junction transistor (BJT), charge pump, inverter-based amplifier, temperature sensor, temperature to digital converter.**

I. Introduction

MODERN system-on-chips (SoCs) require several low-cost temperature sensors for on-chip thermal management [1], [2], [3], [4]. These sensors are placed close to dense digital circuitry to detect cold and hot spots. To reduce fabrication costs, they should be as compact as possible [3], [4]. Such sensors should also achieve good accuracy (<2 °C error) over a wide temperature range (>100 °C) with minimal trimming to reduce calibration costs [1]. Moreover, to minimize routing complexity, they should be able to operate with the local digital supply, which is typically less than 1 V in sub-65-nm processes [1], [2], [5].

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Although conventional bipolar junction transistor (BJT)-based sensors can achieve good accuracy, they typically do not meet the sub-1-V requirement [6], [7], [8]. Compact MOSFET [4], [9], [10], [11] and resistor-based [2], [3], [5], [12] sensors have been reported to operate with a sub-1-V supply voltage, but they usually have lower accuracy or require a costly 2-point trim.

To achieve good accuracy at a low supply, temperature sensors based on the capacitively biased (CB) "diode" technique have been proposed [1], [9], [13], [14]. This involves pre-charging a sampling capacitor to an initial voltage, for example, the supply voltage, and then discharging it through a diode for a fixed period. The resulting sampled voltage will be complementary to absolute temperature (CTAT) [15]. A proportional to absolute temperature (PTAT) voltage can then be generated by subtracting the outputs of two CB diodes with a fixed discharge time ratio [16]. The diodes can be realized by bulk diodes [1], DTMOSTs [9], and diode-connected BJTs [13], [14]. Compared to the static current source biasing used in conventional temperature sensors, this capacitive biasing technique requires little headroom and enables sub-1-V operation over a wide temperature range.

In this article, which is an extended version of [17], the design of a compact 0.8-V CB PNP-based temperature sensor with both high accuracy and energy efficiency is presented. It uses the proposed regulated charge pumps (RCPs) to pre-charge two sampling capacitors to a supply-independent over-1-V voltage. These capacitors are then discharged across two diode-connected PNPs with fixed periods, thus generating PTAT and CTAT voltages from a 0.8-V supply. The ratio of these voltages is further digitized by an area and energy-efficient charge-balancing ΔΣ analog to digital converter (ADC). For both area and energy efficiency, the modulator's first inverter-based integrator employs both chopping and auto-zeroing. Fabricated in a standard 22-nm bulk CMOS process, the sensor occupies 0.01 mm^2 and consumes 2.9 μW from a 0.8-V supply. It achieves an inaccuracy of ±0.4 °C (3σ) from −40 °C to 125 °C after a 1-point trim, which is the best reported in sub-65-nm CMOS. It also achieves high energy efficiency, resulting in a resolution figure of merit (FoM) of 0.41 pJ · K^2.

The rest of this article is organized as follows. Section II describes the proposed sub-1-V sensor front-end, which employs CB PNPs with local RCPs. Next, the proposed charge-balancing ΔΣ-modulator-based readout scheme is pre-

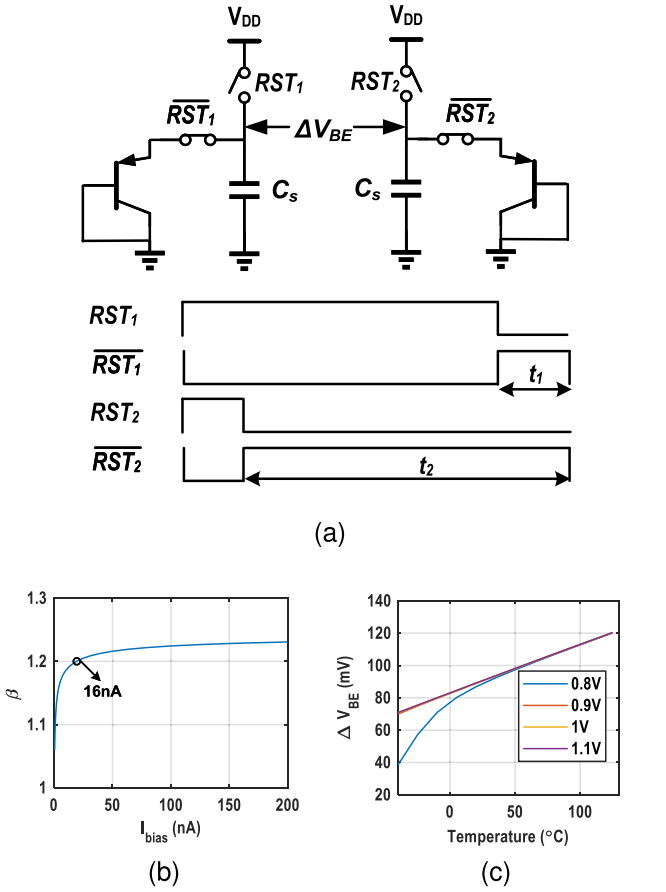

Fig. 1. (a) Block and timing diagrams of the CB PNP pair. (b) Simulated current gain of the PNP transistor ($1.6 \times 1.6\ \mu m^2$) at different emitter bias currents I_{bias}. (c) Simulated ΔV_{BE} at different supply voltages and temperatures ($t_1 = 50$ ns, $t_2 = 1.6\ \mu$s, and $C_S = 1$ pF).

sented in Section III. A detailed circuit implementation of the sensor is then described in Section IV. Its measured performance is presented in Section V and compared to the state-of-the-art. Finally, conclusions are drawn.

II. Sensor Front End

In the target 22-nm CMOS, the supply voltage is typically 0.9 V. So, to accommodate a ±10% supply tolerance, the temperature sensor should be able to operate from a 0.8-V supply. This section will describe a CB PNP-based sensor front end that meets this requirement.

A. CB PNP

To determine the minimum required supply headroom for the CB front end, the parasitic PNPs available in the target 22-nm were evaluated. In a test bench, two 1-pF sampling capacitors are first pre-charged to the supply voltage and then discharged through two diode-connected PNPs. A PTAT voltage ΔV_{BE} is generated by subtracting the outputs of two CB PNPs with a fixed discharge time ratio of 32 [$t_1 = 50$ ns and $t_2 = 1.6\ \mu$s; Fig. 1(a)]. As shown in Fig. 1(b), t_2 is chosen to ensure that the BJT is biased at the edge of its flat current gain β region ($I_{bias} = 16$ nA), while t_1 is chosen to minimize the supply dependency of the generated ΔV_{BE} [16]. Fig. 1(c) shows the simulated ΔV_{BE} over supply voltage and temperature. Done to supply voltages of 900 mV, ΔV_{BE} is a

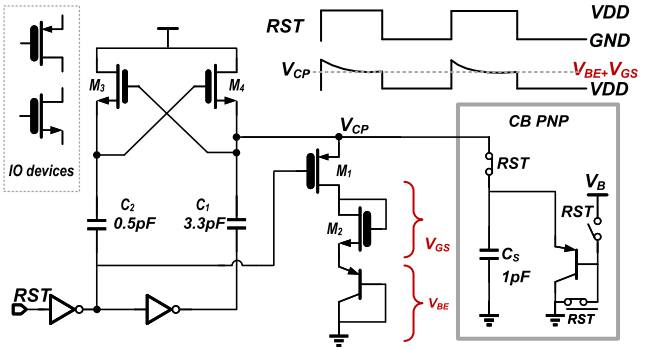

Fig. 2. Block diagram of the CB PNP with an RCP.

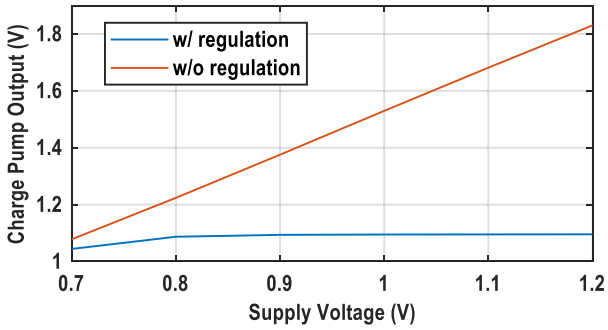

Fig. 3. Simulated charge pump output V_{CP} at room temperature with and without regulation.

linear function of temperature. Below this, it becomes nonlinear, especially at low temperatures. This is because V_{BE} is about 850 mV at −40 °C, and so there is not enough headroom to charge the PNPs.

B. Regulated Charge Pump

To enable operation at low supply voltages, a local charge pump can be used to boost the initial voltage of the sampling capacitor, as shown in Fig. 2. Compared to the charge pumps used in conventional temperature sensors, which have to bias BJTs at constant currents [18], the charge pump used in this work only needs to pre-charge a single capacitor C_S during the RST phase, which simplifies its design. As shown in Fig. 2, the output of the charge pump V_{CP} is boosted above V_{DD} when the input RST signal transitions from low to high. Due to the charge sharing between the boosting capacitor (C_1) and sampling capacitor (C_S), the initial boosted voltage V_{CP} is given by

$$V_{CP} = \frac{2C_1}{C_S + C_1} \cdot V_{DD}. \tag{1}$$

With $C_1 = 3.3$ pF and $C_S = 1$ pF, V_{CP} is about $1.5 \times V_{DD}$, which is always >1 V for $V_{DD} > 0.7$ V. This ensures that there is enough voltage headroom to robustly bias the PNPs. To reduce its supply sensitivity, V_{CP} is regulated by loading it with the series connection of a diode-connected BJT Q_0 and a thick-oxide nMOS transistor M_2. During the RST phase, C_1 and C_S will then discharge through Q_0 and M_2 when the pMOS switch M_1 is closed, resulting in a regulated output voltage of $V_{BE} + V_{GS}$. This technique makes the headroom (V_{GS} and >290 mV over temperature) of the CB PNP relatively supply-independent, thus reducing the sensor's power supply sensitivity (PSS). Fig. 3 shows the simulated V_{CP}

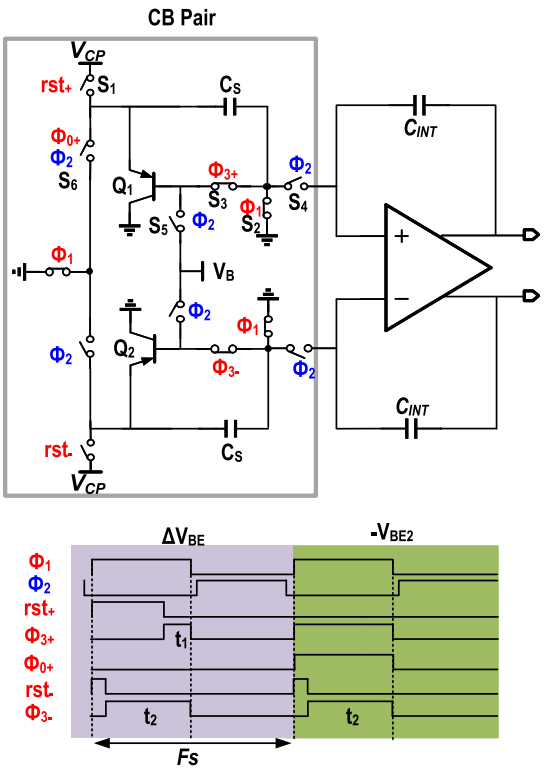

Fig. 4. Block and timing diagrams of the CB PNP in an SC integrator.

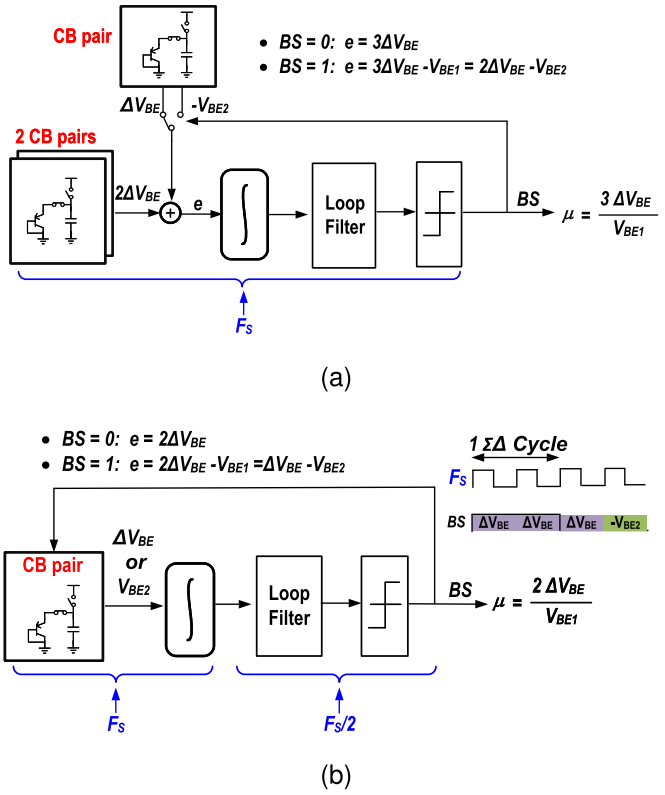

Fig. 5. (a) Simplified diagram of the readout scheme in [14]. (b) Simplified diagram of the proposed readout scheme.

at room temperature, with and without regulation. Adding the regulator reduces the V_{CP} variation to less than 9 mV as V_{DD} changes from 0.8 to 1.2 V. Moreover, it only increases the power consumption of the front end from 0.52 to 0.7 μW with a 0.8-V supply. For reliability and low leakage current, transistors M_1–M_4 are I/O devices, as well as all the switches.

III. Readout Scheme

A. CB PNP in an SC Integrator

As in [14], the output of the CB PNPs can be readily read out by a charge-balancing $\Delta\Sigma$ ADC to generate a digital representation of temperature. Fig. 4 shows the block and timing diagrams of the CB PNP combined with the switched capacitor (SC) integrator, which is the first stage of the 1-bit $\Delta\Sigma$ modulator. At the beginning of the sampling phase Φ_1, the sampling capacitors C_S are first pre-charged to the initial voltage V_{CP} by closing switches S_1 and S_2, where V_{CP} is the output voltage of the RCP. They are then discharged through the BJTs with different discharge times (t_1 and t_2) by opening switch S_1 and closing switch S_3. Opening switch S_3 will turn off the PNPs, stop the discharge phase, and sample the PTAT voltage ΔV_{BE} on C_S. Controlled by the Φ_{0+} signal, a CTAT voltage V_{BE} can also be generated by simply shorting one of the sampling capacitors C_S to ground. During the integration phase Φ_2, the voltages on the two differential sampling capacitors are then transferred to the integration capacitor C_{INT} of the SC integrator by opening switch S_2 and closing switches S_4 and S_6. The PNPs can be completely turned off by connecting their bases to a bias voltage V_B ($\simeq V_{BE}$). As in [14], this is generated by a dummy CB PNP with relaxed accuracy.

B. Conventional Readout Scheme

To generate a digital representation of temperature, the ratio of the PTAT and CTAT voltages $\mu = \Delta V_{BE}/V_{BE}$ can be read out by a charge-balancing $\Delta\Sigma$ ADC. Although μ is a nonlinear function of temperature, it can be readily linearized in the digital domain and converted to temperature as in [14] and [19]

$$T = A \cdot \frac{\alpha \cdot \mu}{\alpha \cdot \mu + 1} - B \tag{2}$$

where α, A, and B are fitting parameters.

Fig. 5(a) shows the simplified diagram of the CB PNP-based temperature sensor described in [14]. To make good use of the ADC's dynamic range, a gain of 3 is applied to ΔV_{BE}, which is realized by using three identical CB pairs. When the bitstream output BS is 0, all of them sample $\Delta V_{BE} = V_{BE1} - V_{BE2}$. When the BS is 1, however, one of them is configured to generate $-V_{BE2}$, thus transferring a charge proportional to $2\Delta V_{BE} - V_{BE2}$. As a result, the BS average $\mu = 3\Delta V_{BE}/V_{BE1}$. Since multiple CB pairs are required, this readout scheme requires a large area [14]. Moreover, to ensure high gain accuracy, a complex dynamic element matching (DEM) scheme is also required.

C. Proposed Readout Scheme

In this work, to reduce area and complexity, a charge-balancing scheme based on a single CB pair is proposed. Instead of using multiple CB pairs to amplify ΔV_{BE} [14], the output of a single pair can be sampled and integrated multiple times [20]. In this work, the output of a single CB pair is integrated twice per $\Delta\Sigma$ cycle to achieve a gain of 2. As a

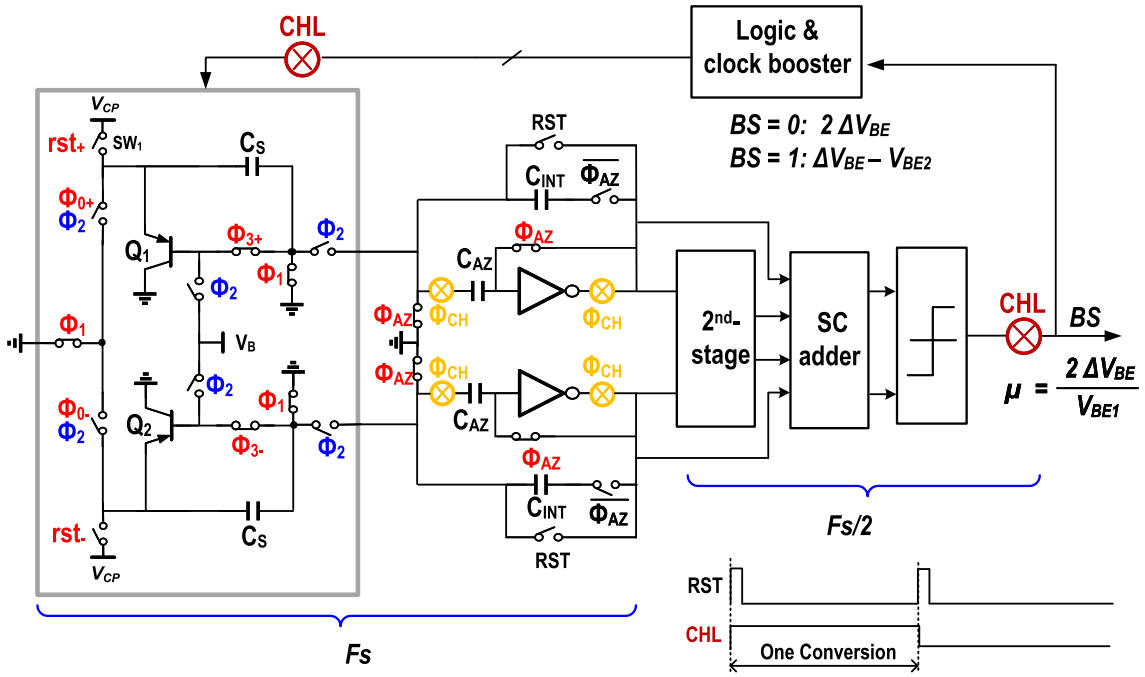

Fig. 6. Block diagram of the proposed temperature sensor.

result, the first integrator and the CB pair run at F_S, while the rest of the loop filter runs at half of the sampling frequency $F_S/2$. To generate a BS average of $\mu = 2\Delta V_{\rm BE}/V_{\rm BE1}$, $2\Delta V_{\rm BE}$ is integrated when BS is 0, and $\Delta V_{\rm BE} - V_{\rm BE2}$ is integrated when BS is 1. Since only one CB pair is used, DEM is not required, so a smaller area can be achieved. Although the ADC's dynamic range (26%) is used less efficiently than that in [14], resulting in greater quantization error, this can be compensated for by increasing the modulator's over-sampling ratio (OSR).

IV. Circuit Implementation

A. 1-Bit Second-Order ΔΣ Modulator

Fig. 6 shows the block diagram of the proposed temperature sensor. It employs a 1-bit second-order SC ΔΣ modulator. To reduce the output swing of the first integrator, thus facilitating sub-1-V operation, a feed-forward topology is employed as in [21]. All timing control signals are generated from a 20-MHz system clock $F_{\rm IN}$, which defines the discharge times ($t_1 = 50$ ns and $t_2 = 1.6$ μs) using an on-chip clock divider. The first integrator and the CB pair then run at F_S ($=F_{\rm IN}/64 =$ 312.5 kHz).

B. Auto-Zeroed Chopper Inverter Amplifier

To facilitate sub-1-V operation, the modulator's integrators are built around auto-zeroed inverter-based pseudo-differential OTAs. Fig. 7 (left) shows one-half of the amplifier used in the first integrator. To reduce the gate leakage current and improve the gain, the input transistors (M_{P1} and M_{N1}) are implemented by I/O devices. Cascode transistors M_{P2} and M_{N2} are further applied to ensure a dc gain of >50 dB in the target 22-nm CMOS process. As in [14], the auto-zeroed inverter-based OTA biases its pMOS and nMOS input pairs separately, resulting in a minimum supply voltage of $V_{\rm GS} + 2V_{\rm DS}$, which is lower than 1 V. Here, $V_{\rm GS}$ is the gate–source voltage of the input pMOS transistor (M_{P1}), and $V_{\rm DS}$ is the drain–source voltage of the cascode nMOS (M_{N2}) and input nMOS (M_{N1}) transistors. However, the OTA in [14] requires large auto-zero capacitors $C_{{\rm AZN},P}$ (17 pF) to reduce kT/C noise, thus ensuring that the integrator's input-referred noise is dominated by the kT/C noise of the CB pair.

In this work, to reduce the capacitor size without a noise penalty, the OTA is auto-zeroed and chopped. Instead of auto-zeroing at F_S [14], the OTA of the first integrator is auto-zeroed at $F_S/2$ in this work. Fig. 7 (right) shows its operation phases. At the beginning of each ΔΣ cycle, the OTA is auto-zeroed. Its bias current (500 nA) is set via an nMOS current mirror, and the gate voltages of M_{N1} and M_{P1} are stored on capacitors $C_{{\rm AZN},P}$, respectively. Thanks to the auto-zero operation, the offset and $1/f$ noise of the OTA are mitigated. However, some kT/C noise $V_{\rm ns}(n)$ will be sampled and held on the capacitors $C_{{\rm AZN},P}$. Together with the input signal, this will be transferred to the integration capacitor $C_{\rm INT}$ during the next integration phase. To reduce this noise, the OTA is then chopped during the next sampling phase. As a result, the same sampled voltage noise will be integrated with the opposite polarity ($-V_{\rm ns}(n)$) during the next integration phase. The kT/C noise generated during each auto-zero phase will therefore be exactly averaged out during the two integration phases of each ΔΣ cycle. This allows the use of much smaller auto-zero capacitors (0.7 pF) without a noise penalty. Fig. 8 shows the simulated input-referred noise density of the SC integrator using the proposed inverter-based amplifier. With a 0.7-pF $C_{{\rm AZN},P}$, the addition of chopping reduces the in-band noise density from 521 to 352 nV/$\sqrt{\rm Hz}$. To achieve a similar noise level with auto-zeroing only, it requires a 10× larger $C_{{\rm AZN},P}$ (7 pF) as shown in Fig. 8. Since the noise of the

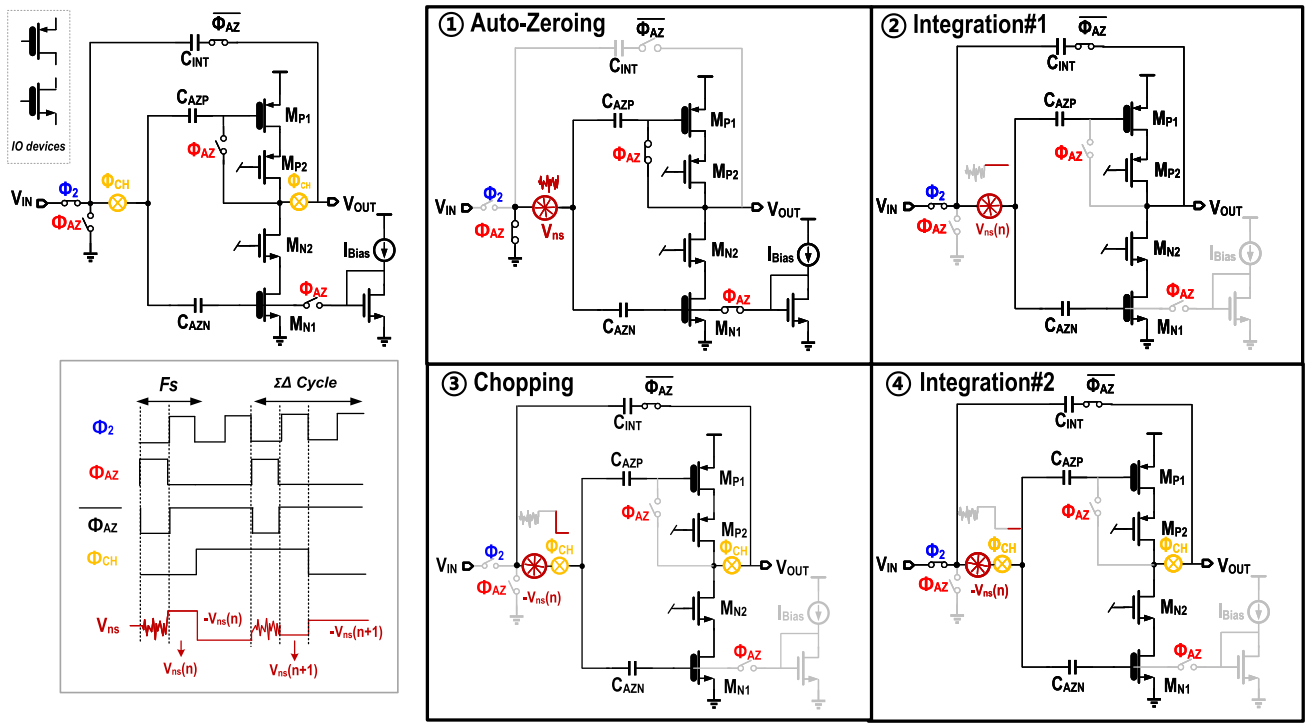

Fig. 7. Block and timing diagrams of the auto-zeroed chopper inverter amplifier.

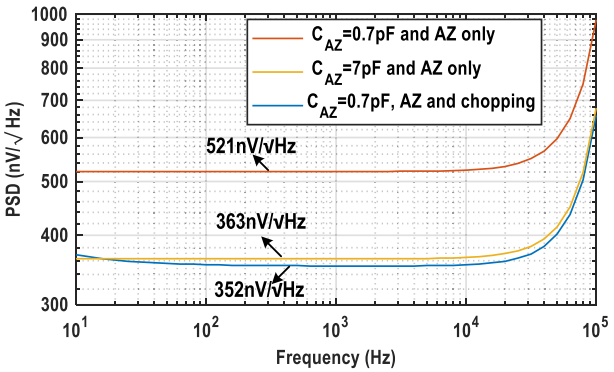

Fig. 8. Simulated input-referred noise density of the auto-zeroed SC integrator with and without chopping.

second integrator will be suppressed by the gain of the first stage, a scaled auto-zeroed OTA without chopping is used for simplicity.

C. Design Considerations

Although the current ratio of the PNPs (Q_1 and Q_2) is defined accurately by the different discharge times, PNP and C_S mismatch inside the CB pair still affects the accuracy when generating the ΔV_{BE}. In this work, this error is mitigated by using system-level chopping at a low frequency (CHL). As in [13] and [14], this is done in the digital domain by swapping the appropriate timing signals of the CB pair, avoiding the need for extra analog switches. CHL also suppresses any residual offset and $1/f$ noise of the $\Delta\Sigma$ modulator, thus improving accuracy. To reduce the leakage current of the switches, all the switches in the CB pair are implemented by I/O devices, which are driven by clock boosters as in [13] and [14].

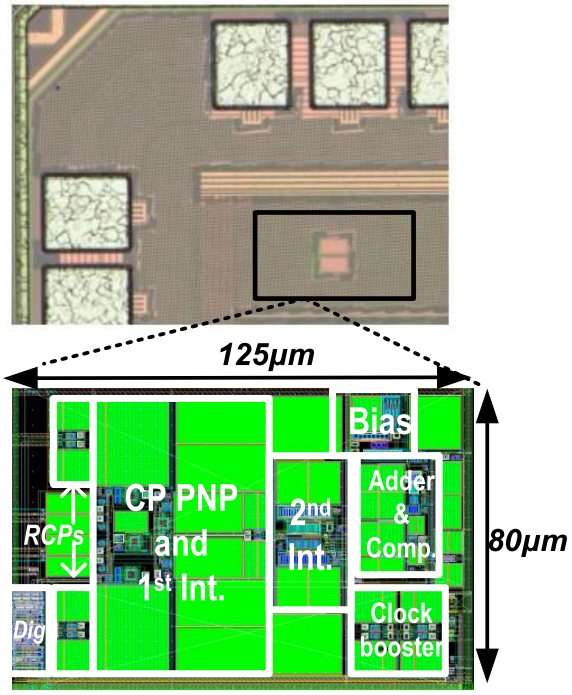

Fig. 9. Die photograph and layout of the proposed temperature sensor.

V. Measurement Results

Fig. 9 shows the die photograph and layout of the proposed temperature sensor. It was fabricated in a standard 22-nm bulk CMOS process with a core area of 0.01 mm^2. All the required timing signals were generated on-chip from a 20-MHz system clock. The sinc^2 decimation filter was implemented off-chip for flexibility. Simulations show that integrating it on a chip only occupies 300 μm^2 and consumes 1 μW.

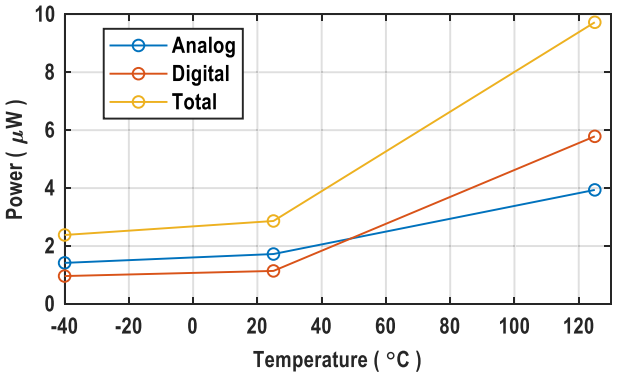

Fig. 10. Measured power consumption of the sensor with a 0.8-V supply over temperature.

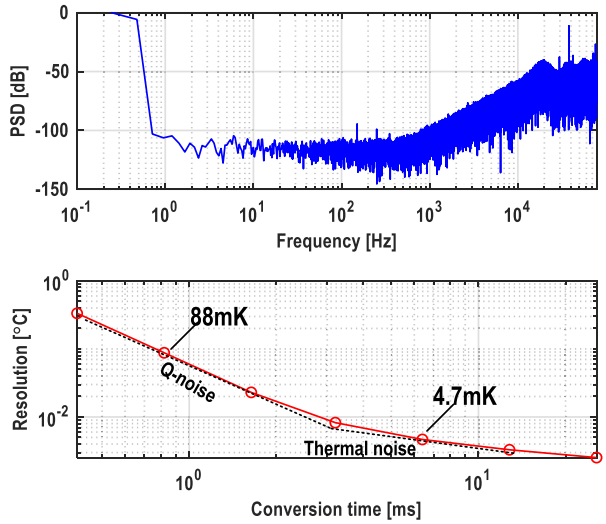

Fig. 11. FFT of the sensor's bitstream and resolution at different conversion times.

Fig. 10 shows the measured power consumption of the sensor over temperature. At a sampling frequency F_S = 312.5 kHz, the sensor dissipates 2.9 μW at room temperature with 40% consumed by the digital control signal generation circuits. The power consumption increases to 9.7 μW due to the leakage current at high temperatures.

A. FFT and Resolution

Fig. 11 (top) shows the measured FFT of the sensor's bitstream with the modulator operating in the free-running mode. It has a flat in-band noise floor, thanks to the auto-zeroing and chopping techniques, which migrate $1/f$ noise. Fig. 11 (bottom) shows the measured resolution for different conversion times. With an OSR of 1000, it achieves a thermal-noise-limited resolution of 4.7 mK in 6.4 ms, corresponding to a resolution FoM of 0.41 pJ · K^2. Sub-1 ms conversions are also possible, but at the expense of quantization-noise-limited resolution, for example, 88 mK in 0.82 ms (OSR = 128).

B. Accuracy Measurement

Twenty-three samples from one batch were measured from −40 °C to 125 °C with a standard 0.9-V supply. As shown

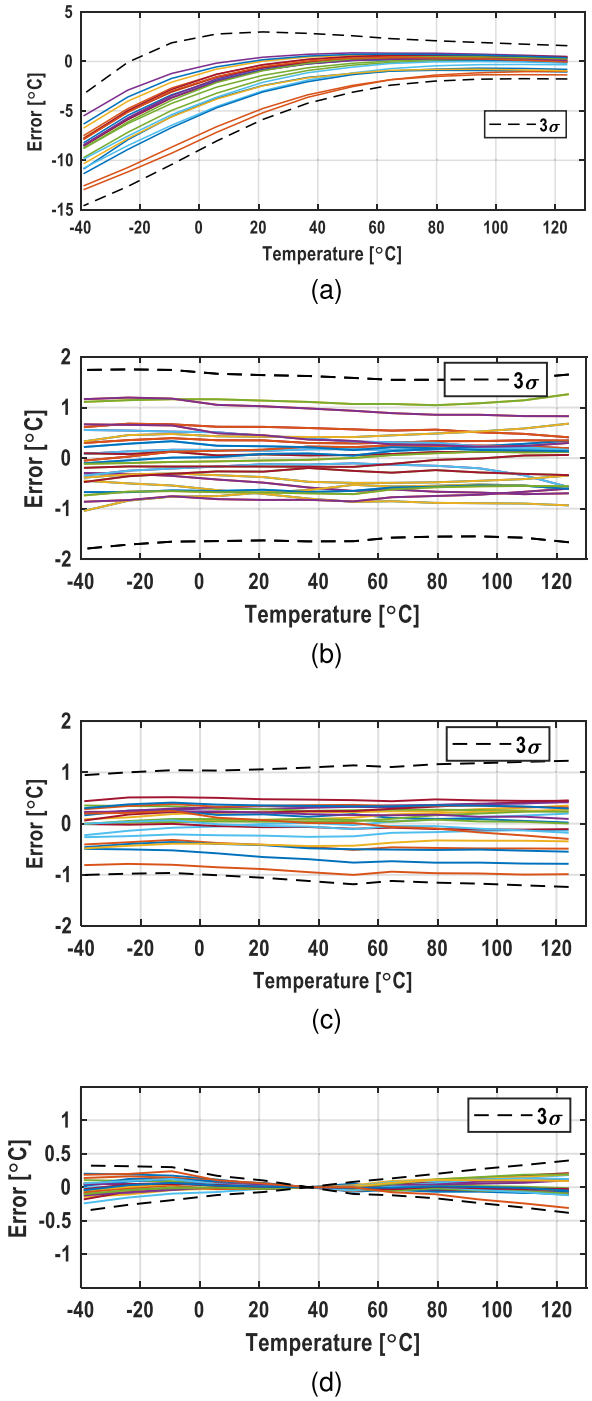

Fig. 12. (a) Untrimmed error w/o RCP. (b) Untrimmed error w/ RCP and w/o CHL. (c) Untrimmed error w/ RCP and CHL. (d) Measured one-point trimmed error. The same fitting coefficient α = 6.151 is applied for all the plots.

in Fig. 12(a), without the RCP, large errors (>10 °C) at low temperatures occur due to the lack of supply headroom. With the RCP, the untrimmed inaccuracy improves to ±1.8 °C [Fig. 12(b)] and drops to ±1.25 °C (3σ) with CHL [Fig. 12(c)]. After a 1-point offset trim, the sensor achieves a 3σ inaccuracy of ±0.4 °C from −40 °C to 125 °C [Fig. 12(d)]. The residual error is mainly due to the spread of the BJTs. The spread of their saturation current causes PTAT errors in V_{BE}, while the spread of their current gain causes non-PTAT errors in ΔV_{BE}.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

	This work		JSSC'23 [14]	SSCL'19 [1]	ISSCC'18 [22]	ISSCC'17 [8]	CICC'20 [9]	ISSCC'22 [2]	ISSCC'24 [5]
Technology	**22nm CMOS**		180nm CMOS	16nm FinFET	22nm FinFET	28nm CMOS	28nm CMOS	5nm FinFET	3nm FinFET
Type	**PNP**		PNP	Bulk Diode	PNP/MOS	PNP	DTMOST	Metal	Metal
Area [mm^2]	**0.01**		0.25	0.0025	0.0043	0.00946	0.017	0.00635	0.0009
Supply [V]	**0.8-1.1**		0.95-1.4	0.85-1	0.97-1.3	1.8	0.85-1.15	0.65-0.9	0.65-0.85
T. Range [°C]	**-40 to 125**		-55 to 125	-15 to 105	-30 to 120	-25 to 125	-10 to 90	-40 to 150	-25 to 125
3σ error (Trim point*)	**±1.25 (0) ±0.4 (1)**		±0.45 (0) ±0.15 (1)	+1.5/-2.0 (0)	±2.81 (0) ±1.07 (1)	0.6/-1.85 (0)	±0.9 (1)	±1.8 (2)	±1.5 (1)
RIA [%] (Trim point)	**1.5 (0) 0.48 (1)**		0.5 (0) 0.17 (1)	2.9 (0)	3.75 (0) 1.4 (1)	1.64 (0)	1.8 (1)	1.89 (2)	2 (1)
Power [μW]**	**2.9**		0.81	18	50	18.75	33.75	15	20
PSS [°C/V]	**1.3**		0.2	1.5	/	/	0.27	0.41	0.6
Tconv [ms]	**0.82**	**6.4**	128	0.013	0.032	8.192	0.1	0.012	1
Res. [mK]	**88**	**4.7**	1.8	300	580	150	10.2	114.1	22.1
Res. FoM* [pJ· K^2]**	**18.3**	**0.41**	0.34	21	540	3460	0.36	2.3	9.8

* 0: no individual trim; 1: 1-point individual temperature trim.
** at room temperature
*** Res. FoM=(Energy/conversion)·(Resolution)^2.

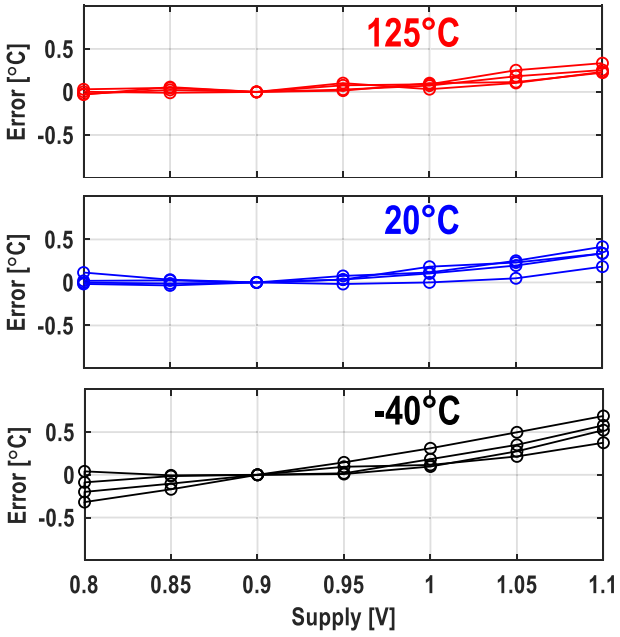

Fig. 13. Power supply sensitivity measurement at different temperatures.

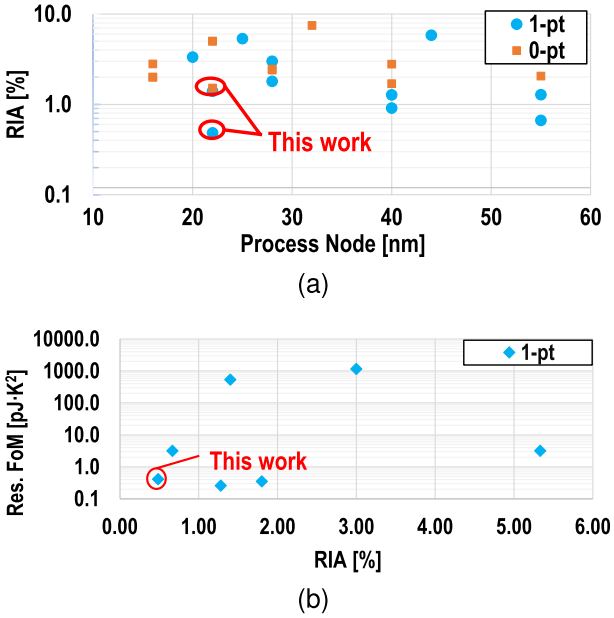

Fig. 14. Comparison with state-of-the art temperature sensors implemented in sub-65-nm CMOS [23]. (a) RIA versus process nodes. (b) RIA versus resolution FoM.

C. Power Supply Sensitivity

As shown in Fig. 13, four sensors were measured with different supply voltages over temperature. Thanks to the proposed RCP, it can operate down to 0.8 V from −40 °C to 125 °C. When operated from 0.8 to 1.1 V, the PSS of the sensor ranges from 0.58 °C/V to 1.3 °C/V at room temperature. The residual PSS is limited by the charge injection and clock feedthrough error of switches at high supply voltages. Since the OTA requires a higher voltage headroom at low temperatures, this limits the minimum supply and increases the PSS variation at low temperatures.

D. Comparison With the State-of-the-Art

Table I summarizes the performance of this work and compares it to state-of-the-art temperature sensors. The proposed sensor can operate with a 0.8-V supply and has a compact area of 0.01 mm^2. It achieves the best accuracy among sub-65-nm CMOS temperature sensors as well as high energy

efficiency. Compared to [14], the degraded accuracy is mainly due to the degraded quality of the BJTs in the 22-nm CMOS process. Fig. 14 shows the graphical comparison of its relative inaccuracy (RIA) and energy efficiency with other reported temperature sensors in sub-65-nm CMOS processes according to [23]. This is the only temperature sensor that achieves an RIA $< 0.5\%$ after a 1-point trim, together with sub-$\text{pJ} \cdot \text{K}^2$ energy efficiency.

VI. Conclusion

A 0.8-V compact BJT-based temperature sensor with both high accuracy and high energy efficiency is proposed in this work. It uses RCPs to pre-charge the sampling capacitors of the CB PNP pair, thus achieving a 0.8-V operation from −40 °C to 125 °C. For both high accuracy and compact area, a charge-balancing $\Delta\Sigma$-modulator-based readout scheme is proposed, and a chopped auto-zeroed inverter-based amplifier is employed. Fabricated in a standard 22-nm bulk CMOS process, the sensor occupies 0.01 mm^2 and consumes 2.9 μW from a 0.8-V supply. It achieves an inaccuracy of ±0.4 °C (3σ) from −40 °C to 125 °C after a 1-point trim, which is the best reported in sub-65-nm CMOS. It also achieves high energy efficiency and shows a resolution FoM of 0.41 $\text{pJ} \cdot \text{K}^2$.

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