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A BJT-Based Temperature-to-Digital Converter With a ±0.25 °C 3σ-Inaccuracy From −40 °C to +180 °C Using Heater-Assisted Voltage Calibration

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***Abstract*— This article presents a BJT-based temperature-to-digital-converter (TDC) that achieves ±0.25 °C 3σ-inaccuracy from −40 °C to +180 °C after a heater-assisted voltage calibration (HA-VCAL). Its switched-capacitor (SC) ADC employs two sampling capacitors and, thus, the minimum number of critical sampling switches, which minimizes the effects of switch leakage at high temperatures and improves accuracy. The TDC is also equipped with an on-chip heater, with which the sensing BJTs can be rapidly (<0.5 s) heated to about 110 °C. This, in turn, enables VCAL at two different temperatures without the need for a temperature-controlled environment. Realized in a 0.16-μm standard CMOS, the TDC, including the on-chip heater, occupies 0.15 mm^2 and operates from 1.8 V.**

***Index Terms*— BJT, calibration, heater-assisted, low leakage, on-chip heater, temperature sensor, voltage calibration (VCAL).**

I. Introduction

ACCURATE temperature sensing at high temperatures (>150 °C) is often required in automotive applications, for instance, in engine or transmission control or the measurement and control of air, gases, and fluids [1], [2]. In such applications, BJT-based sensors are the preferred choice due to their well-known behavior, long-term stability, and high accuracy after a one-point calibration [3]–[7].

At high temperatures, however, exponentially increasing leakage currents can significantly alter the bias currents of the sensing BJTs, leading to temperature-sensing errors. To mitigate such errors, BJT-based sensors have either employed relatively large biasing currents [3], been realized in low-leakage SOI processes [4], [5], or employed leakage compensation schemes [6], [7]. Good accuracy at high temperatures is, thus, achieved at the expense of higher power consumption, complexity, or cost.

Thermal diffusivity (TD) sensors [8] and resistor-based sensors [9] have also demonstrated good accuracy at high temperatures. Compared to BJT-based sensors, however, the milliwatt-level power dissipation of TD sensors and the two-point calibration required by precision resistor-based temperature-to-digital-converters (TDCs) make them less suitable for automotive applications.

Another drawback of BJT-based temperature sensors is their stress dependence, which increases their inaccuracy after plastic packaging [10], [11]. This then necessitates one- or two-point postpackaging calibration, which is significantly more expensive than wafer-level calibration.

In this article, a precision BJT-based TDC is proposed that can operate up to 180 °C without the aforementioned drawbacks. It employs a switched-capacitor (SC) ADC to sample and digitize the base–emitter voltages of two sensing BJTs. The ADC employs two sampling capacitors and, thus, the minimum number of sampling switches, which mitigates the effect of switch leakage at high temperatures. As a result, the sensing BJTs can be biased at low-current levels, while still obtaining state-of-the-art inaccuracy and power consumption.

The proposed TDC is also equipped with an on-chip heater, with which the sensing BJTs can be rapidly heated. This facilitates a rapid two-point calibration without the need for a temperature-controlled environment. This low-cost heater-assisted voltage calibration (HA-VCAL) can be carried out after plastic packaging to correct for stress-related shifts [10].

This article is organized as follows. Section II describes the TDC's front end and provides some background about both conventional temperature and VCAL methods. Section III then elaborates on the proposed HA-VCAL scheme, the realization of the on-chip heater, and potential error sources. Section IV provides a leakage analysis and presents a detailed description of the operation of the SC-ADC. Section V includes the experimental results, and finally, section VI concludes this article.

II. Background

A. Sensing Front End

Fig. 1 shows the front end of the TDC, which consists of a bipolar core and a bias circuit. As in [10], the bipolar core generates temperature-dependent voltages V_{BE} ($= V_{\mathrm{BE2}}$) and ΔV_{BE} ($= V_{\mathrm{BE2}} - V_{\mathrm{BE1}}$) from two PNPs ($Q_L$ and Q_R), which are biased at a current density ratio of 1 : 5. The required bias currents are generated by the bias circuit with the help of another pair of PNPs (Q_{Lb} and Q_{Rb}), which are also

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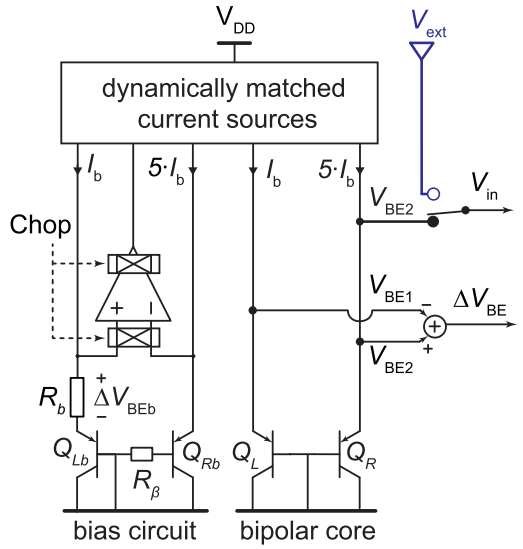

Fig. 1. Sensor front end, which generates V_{BE1}, V_{BE2}, and ΔV_{BE}. During VCAL, V_{BE2} is replaced by an external reference V_{ext}.

biased at a 1 : 5 current density ratio. An opamp forces the resulting ΔV_{BEb} across a poly resistor R_b, thus generating a proportional-to-absolute-temperature (PTAT) bias current I_b ($= \Delta V_{\mathrm{BEb}}/R_b$). A second poly resistor, R_β ($= R_b/5$) cancels the effect of β on V_{BE} by making I_b slightly β-dependent [12], [13].

The opamp employs a folded-cascode topology, which achieves more than 90-dB dc-gain over process and temperature variations. Its offset is mitigated by chopping, while dynamic element matching (DEM) ensures accurate 1 : 5 ratios in both the bias circuit and the bipolar core [14].

B. Temperature Calibration

The front end is followed by an ADC that digitizes the temperature-dependent ratio $X_T = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$, where X_T is a nonlinear function of temperature. A linear function of temperature can then be obtained in the digital domain by computing $\mu_T = \alpha/(\alpha + X_T)$, where α ($\sim$16) is a calibration parameter [13], [14]. This can then be mapped to degrees Celsius by evaluating $D_{\mathrm{out}} = A \cdot \mu_T + B$, where A ($\sim$610) and B (~ -283) are also the calibration parameters.

The coefficients A, B, and α can be found by batch calibration, which involves calibrating several TDC samples over the desired temperature range. Due to the PTAT spread of V_{BE}, however, the resulting inaccuracy of individual samples will still be in the order of several degrees. To obtain higher accuracy, V_{BE} must be individually trimmed.

Conventionally, the information required to trim V_{BE} is determined by temperature calibration. This involves placing the TDC in good thermal contact with a reference temperature sensor. After thermal equilibrium is reached, the die temperature T_{die} is known (assuming negligible self-heating), and the output of each sample can then be corrected by applying a PTAT trim to V_{BE} [15]. Reaching thermal equilibrium, however, is a slow (minute-long) process, which significantly increases the TDC's production costs.

Although high accuracy (less than 0.1 °C over the military temperature range) can be achieved after the one-point calibration of ceramic-packaged samples, two-point calibration is required to correct for the non-PTAT errors caused by the packaging stress present in plastic-packaged samples [10], [11]. In other words, the calibration parameters A and B must be adjusted to preserve accuracy [10], [11]. However, the costs associated with two-point calibration are quite high, especially for packaged devices.

C. Voltage calibration

VCAL does not require an accurate temperature reference and is, thus, a faster alternative to temperature calibration [16], [17]. Instead, T_{die} is determined by comparing ΔV_{BE} to an external voltage reference V_{ext}. Experiments show that ΔV_{BE} is quite robust to process variations [14] and to the mechanical stress caused by the plastic packaging [10].

VCAL involves two steps. First, the TDC digitizes the ratio $X_V = V_{\mathrm{ext}}/\Delta V_{\mathrm{BE}}$, from which T_{die} can be estimated with the help of a master curve obtained by a one-time batch calibration. Second, the TDC digitizes the ratio $X_T = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$, which corresponds to an untrimmed temperature output. Since both steps are completed in quick succession (within a few hundred milliseconds), T_{die} can be assumed to be constant. The output of the TDC can then be corrected by trimming V_{BE}.

The accuracy of VCAL relies on the accuracy of V_{ext} and ΔV_{BE}. While V_{ext} is an external voltage, which can be quite accurately defined, ensuring the accuracy of ΔV_{BE} is more challenging. For two PNPs biased via their emitters

$$\Delta V_{\mathrm{BE}} \approx \eta \cdot kT/q \cdot \log(p) + \eta \cdot kT/q \cdot \Delta\beta/\beta^2 + r_S \cdot (p-1) \cdot I_b \tag{1}$$

where η is the nonideality factor of the PNPs, r_s is their equivalent series resistance, β is their nominal current gain, $\Delta\beta$ is the difference in β at the two emitter currents, p is the emitter current ratio, and I_b is the bias current. In this design, the use of low bias current ($I_b \approx 160$ nA at 25°C) and DEM to establish the 1:5 ratio is enough to ensure that the equivalent spread in ΔV_{BE} is less than ± 0.15 °C over different batches [14] and packages [10].

III. Heater-Assisted Voltage Calibration

A. Principle of Operation

Since ΔV_{BE} can be used to accurately estimate T_{die}, VCAL can be carried out at any temperature. The only requirement is that T_{die} is stable during its two steps. HA-VCAL exploits these features, by using an on-chip heater to rapidly warm up the die to an elevated, but not very well-defined, temperature (see Fig. 2). VCAL can then be carried out at two temperatures: at room temperature (T_1) and at this elevated temperature (T_2).

Initially, the heater is OFF, and $T_{\mathrm{die}} = T_1$. The TDC then outputs T_{1V} and T_{1T}, where T_{1V} is the estimated die temperature obtained from $X_V = V_{\mathrm{ext}}/\Delta V_{\mathrm{BE}}$, and T_{1T} is the untrimmed output temperature derived from $X_T = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$. This set of values ($T_{1T}$, T_{1V}) is similar to that obtained during conventional VCAL. The heater is then turned on, thus elevating T_{die} to T_2, after which the TDC outputs T_{2V} and

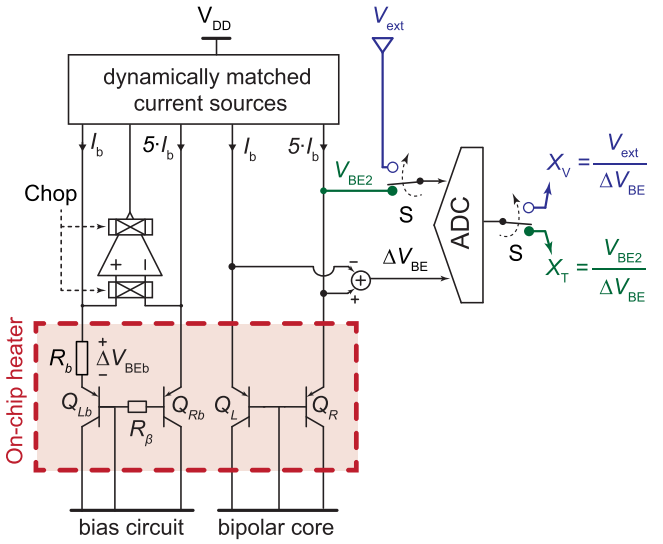

Fig. 2. HA-VCAL. The on-chip heater heats up the temperature-sensitive elements, and VCAL is repeated at two temperatures: room temperature and elevated temperature.

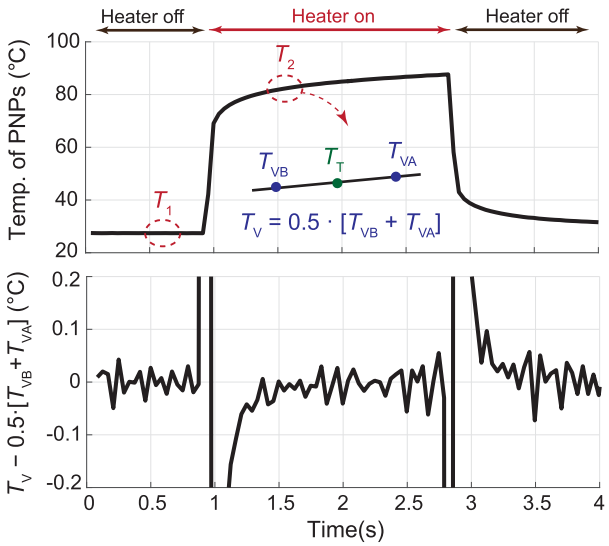

Fig. 3. Measured die temperature taken from [10]. Top: temperature of PNPs when the on-chip heater is pulsed. Bottom: measured interpolation error.

T_{2T}. The two sets of values (T_{1V}, T_{1T}) and (T_{2V}, T_{2T}) can then be used to perform a two-point calibration.

Due to the thermal time constants of the die and package, the transient in T_{die} caused by turning on the heater takes several minutes to fully settle [see Fig. 3 (top)]. Rather than waiting for this, a first-order interpolation scheme is used to ensure that T_{die} is effectively the same during both steps of VCAL. This involves averaging the value of T_V before (T_{VB}) and, after (T_{VA}), the T_T conversion [see Fig. 3 (top)]. For consistency, this is done during both phases of HA-VCAL.

Fig. 3 (bottom) shows the difference between the measured T_V and its interpolated value $0.5 \cdot (T_{VA} + T_{VB})$ during a heating transient. It can be seen that the error after interpolation reaches the noise level in less than 0.5 s, even as the die-temperature changes from ~25 °C to ~90 °C. HA-VCAL, therefore, can be reliably carried out in less than a second.

B. On-Chip Heater

In order to perform the HA-VCAL, it is sufficient to heat just the temperature-sensitive elements of the TDC: the four PNPs (Q_R, Q_L, Q_{Rb}, and Q_{Lb}) and the two poly resistors (R_b and R_β). As a result, the required heater can be quite small, saving both power and area. To be as close as possible to the PNPs and the poly resistors, the heater is realized in Metal-2 [see Fig. 4 (top)], with Metal-1 being reserved for local routing.

In [18], four on-chip heaters were used to calibrate a frequency reference. To minimize on-chip temperature gradients, the heaters were placed far away from the circuits being calibrated, and a heat-spreading metal layer was applied to the bottom of the die during a postfabrication step. In this article, instead of attempting to heat the die uniformly, a single heater is used to create a hotspot directly above the circuit to be calibrated. As a result, only a small volume of silicon needs to be heated, resulting in much faster calibration and obviating the need for an additional heat-spreading metal layer.

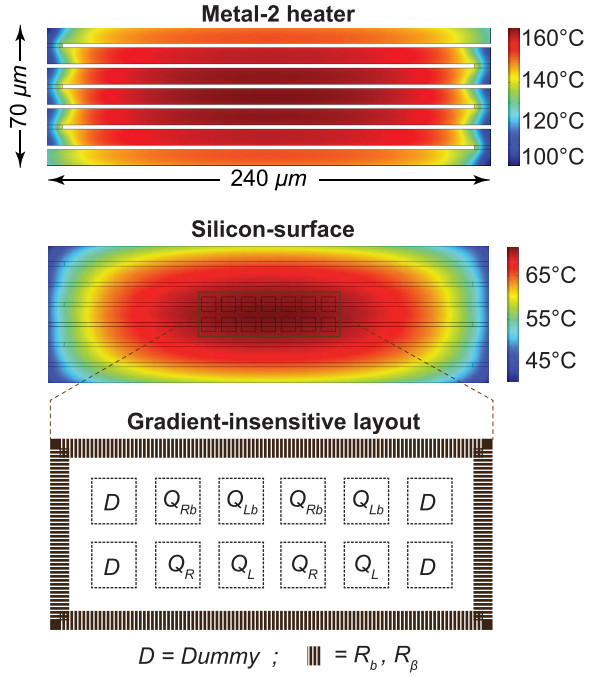

Fig. 4. Top: serpentine-shaped Metal-2 heater and the simulated temperature gradient using COMSOL. Middle: temperature gradient on the silicon surface under the heater. Bottom: gradient-insensitive layout.

However, without any special measures, large temperature gradients will be created under the heater. These could cause significant temperature differences between Q_L and Q_R, causing errors in ΔV_{BE} and, thus, errors in both T_{2V} and T_{2T}. Similarly, the temperature difference between the poly resistors and the PNPs or between Q_{Lb} and Q_{Rb} could cause errors in the bias current and, thus, errors in V_{BE} and, finally, errors in T_{2T}. Temperature differences between the PNPs of the bias circuit and the bipolar core could also cause errors in the β-compensation, again causing errors in V_{BE} and, hence, in T_{2T}.

Fig. 4 shows the results of a COMSOL simulation of a serpentine heater in Metal-2 that dissipates 0.5 W. Large temperature gradients can be seen in the heater and on the silicon substrate under the heater. There is also a significant vertical gradient between the heater and the silicon substrate.

To mitigate the effect of such gradients, the sensitive elements of the TDC are placed in a small (0.002 mm^2) area under the much larger heater (0.017 mm^2). In addition, a gradient-insensitive layout is used [see Fig. 4 (bottom)]. Each PNP is split into two halves and placed in a common-centroid manner around the heater's symmetry axes [see Fig. 4 (bottom)]. Similarly, all top-level metal routings above the heater were done symmetrically with respect to its axes of symmetry.

The resistors R_b and R_β are located around the PNPs and are, thus, further away from the heaters centroid. Being implemented in Poly, however, they are actually closer to the Metal-2 heater than the PNPs. These two effects partially counteract each other and help reduce the temperature difference between the PNPs and the resistors. Simulations show that their average temperature difference is ~7 °C. Given the low-temperature coefficient of the resistors, this results in a 0.2% error in their resistance, which corresponds to a negligible error of 45 m°C in T_{2T}.

C. Local Heating Versus Uniform Heating

In normal operation, the TDC is uniformly heated by changes in ambient temperature. During HA-VCAL, however, it is heated locally. In this case, the area directly under the heater will be significantly hotter than the rest of the TDC, i.e., the front end and the ADC. To prevent calibration errors, the performance of this circuitry should be the same during both modes of operation.

Temperature-dependent errors in the front end, such as opamp offset and current ratio mismatch, are mitigated by the use of chopping and DEM. Similarly, ADC errors, such as offset and gain error, are mitigated by the use of correlated-double sampling, system-level chopping, and DEM. These techniques make the front end and the ADC insensitive to temperature gradients. As a result, their performance is essentially the same during both local and uniform heating.

However, the leakage current of the ADC's sampling switches increases exponentially with temperature. Compared to normal operation, the temperature gradients created with HA-VCAL will then cause different levels of leakage current, which could be a potential source of calibration errors.

One way to avoid such errors is to also place the sampling switches under the heater. However, this would require a significant increase in the area of the uniformly heated zone under the heater and, thus, to a significantly larger heater. A better solution is to use circuit techniques to make switch leakage negligible compared to the bias currents of the critical PNPs.

IV. Low-Leakage Read-Out Circuit

A. Switch Leakage

Fig. 5 (left) shows a simplified diagram of the sampling network of the SC-ADC used in the TDC. Switch leakage

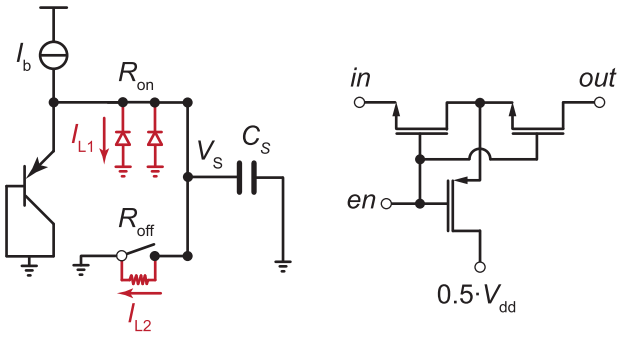

Fig. 5. Left: switch leakage causes V_S to be different from V_{BE}. I_{L1} flows through the reverse diodes of the switches. I_{L2} flows through the OFF-resistance of the switches. Right: low-leakage switch adapted from [19].

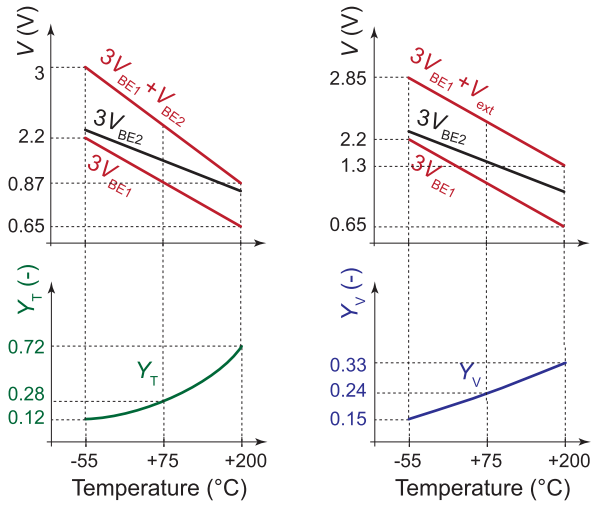

Fig. 6. Charge-balancing scheme in the modulator. The modulator outputs Y_T in the normal mode and Y_V in the VCAL mode.

will alter the PNP's bias current and, thus, cause errors in V_{BE}. Furthermore, errors in the sampled voltage V_S will be caused by leakage current flowing through the ON-resistance R_{ON} of the switch. There are two components of leakage current: I_{L1} and I_{L2}. The former is associated with the reverse-biased junctions between the substrate and the source and drain of the sampling switch, while the latter is the current that flows through the OFF-resistance R_{OFF} of any other switches connected to C_S. The sampling error in V_S due to I_{L1} is directly proportional to the total number of switches connected to the BJTs, while the sampling errors due to I_{L2} are a function of $R_{ON}/(N \cdot R_{OFF})$, where N is the number of "OFF" switches involved.

In previous work [10], HA-VCAL was applied to a TDC based on a zoom ADC [11]. Its sampling network consisted of a capacitor array with 64 unit elements, each of which could be connected to V_{BE1}, V_{BE2}, or V_{ext} via three sampling switches. The switches enabled the application of DEM to the capacitor array, thus significantly mitigating the effect of capacitor mismatch, but resulting in a total of 192 sampling switches. Their leakage led to a small systematic error after HA-VCAL.

As shown in Fig. 7, the proposed ADC uses only two sampling capacitors, which then requires ten switches to

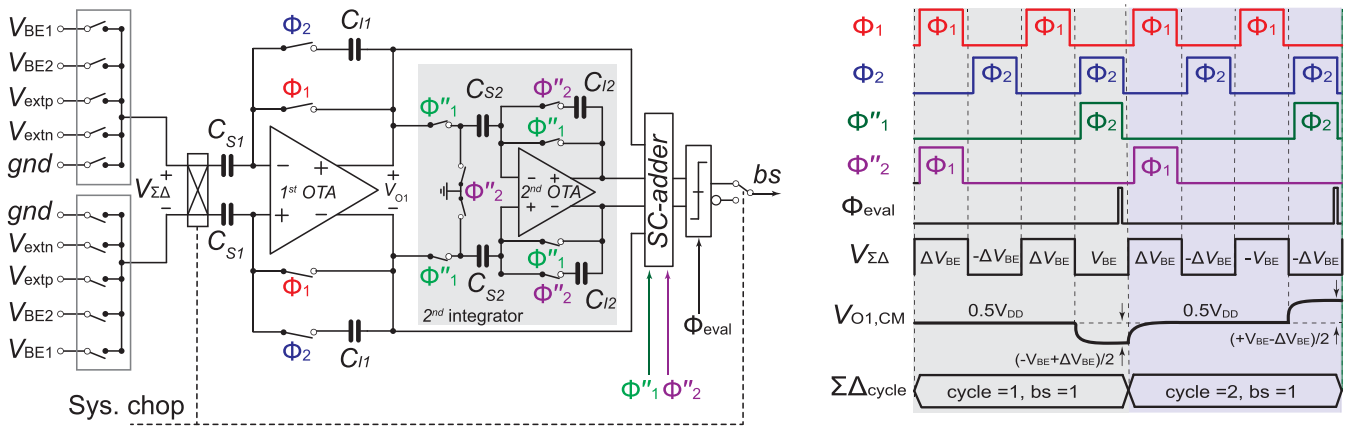

Fig. 7. Left: low-leakage ADC. Right: timing diagram.

sample V_{BE1}, V_{BE2}, and gnd, as well as to differentially sample V_{ext} via V_{extn} and V_{extp}. Compared to the 192 switches used in [10], the substantial reduction in the number of switches proportionally reduces the effect of switch leakage. Furthermore, as shown in Fig. 5 (right), the effective OFF-resistance of each switch was increased by adopting a T-configuration [19]. This consists of two NMOSFETs in series with a PMOSFET that biases the central node to $V_{DD}/2$ when the switch is OFF. As a result, one of the two NMOSFETs is always in the deep cutoff region. As will be shown in the following, the proposed low-leakage ADC enables a higher accuracy at high temperatures, as well as a more robust HA-VCAL.

B. Charge-Balancing Scheme in the Low-Leakage ADC

Using two sampling capacitors in the proposed ADC requires a different charge-balancing scheme than that of the zoom ADC. Similar to [20], the ADC digitizes the ratio $Y_T = 3 \cdot \Delta V_{BE}/V_{BE2}$, which varies from 0.15 to 0.72 as T_{die} varies from −40 °C to +180 °C. The factor of 3 was chosen to maximize the ADC's dynamic range in this temperature range.

In each cycle of the modulator, the first stage integrates a charge proportional to $3 \cdot \Delta V_{BE}$ when bs $= 0$ or a charge proportional to $3 \cdot (\Delta V_{BE} - V_{BE2})$ when bs $= 1$. This results in the desired decimated value: $Y_T = 3 \cdot \Delta V_{BE}/V_{BE2}$. As shown in Fig. 6, this charge-balancing scheme is equivalent to setting the ADC's input to $3 \cdot V_{BE2}$ and then straddling it with two temperature-dependent references $3 \cdot V_{BE1}$ and $3 \cdot V_{BE1} + V_{BE2}$.

During VCAL, V_{BE2} is replaced by V_{ext}. The ADC then outputs $Y_V = 3 \cdot \Delta V_{BE}/V_{ext}$, which varies from 0.15 to 0.33 (for $V_{ext} \sim 0.65$ V) over the operating temperature range. The factor 3 is maintained for simplicity even though it does not optimize the ADC's dynamic range.

Compared to the previous zoom ADC [10], the proposed low-leakage ADC requires much simpler control logic, as the modulator is not preceded by an SAR conversion. Also, since the same capacitors sample ΔV_{BE} and V_{BE}, there is no need for DEM and the associated logic. However, the maximum loop-filter input is now $3 \cdot (\Delta V_{BE} - V_{BE2})$, which is much larger than $2 \cdot \Delta V_{BE}$ of the zoom ADC [11]. In order to handle this extra swing with the same current-reuse OTAs used in [14], the first integrator's capacitor was simply increased, to 710 fF, i.e., by about 4×.

C. Sampling Scheme in the Low-Leakage ADC

In order to implement the gain factor (3) required by the charge-balancing scheme, the low-leakage ADC samples ΔV_{BE}, V_{BE}, or V_{ext} multiple times. As shown in Fig. 7 (right), the first integrator uses four nonoverlapping clock phases ϕ_1 and ϕ_2 to sample and transfer the required charge to the integration capacitor C_{I1}. During the fourth phase, the output voltage of the first stage is sampled by the second-stage integrator during ϕ_1'' and then accumulated during ϕ_2'' to realize a one-cycle integration delay. The output voltages of the two stages are then summed by an SC-adder and evaluated by the comparator (triggered by ϕ_{eval}) to generate the output bitstream (bs). The sampling capacitor C_{S1} is 125 fF, and each sampling phase takes 1.25 μs, resulting in a 5 μs ΣΔ cycle.

The differential input voltage $V_{\Sigma\Delta}$ of the modulator is shown in Fig. 7 (right) for the case when bs $= 1$. The input switches then realize the charge-balancing scheme by applying the following sequence of voltages to $V_{\Sigma\Delta}$: $+\Delta V_{BE}$, $-\Delta V_{BE}$, $+\Delta V_{BE}$, and $+V_{BE}$. This sequence, however, also has a CM component equal to $(-V_{BE} + \Delta V_{BE})/2$, which will also be integrated. Although this component will initially be suppressed by the integrators CMFB circuit, it is cumulative and may eventually cause the first OTA to clip.

To prevent this, as in [21], the CM component is inverted each time the bs $= 1$ state occurs. This involves applying toggling between the $V_{\Sigma\Delta}$ sequence described above and the following sequence: $+\Delta V_{BE}$, $-\Delta V_{BE}$, $-V_{BE2}$, and $+\Delta V_{BE}$. This results in the same differential voltage but inverts its CM component, thus driving the integrated CM shift back to zero. Similarly, when bs $= 0$, the $V_{\Sigma\Delta}$ sequence is toggled between $+\Delta V_{BE}$, $-\Delta V_{BE}$, $+\Delta V_{BE}$, and 0 and $+\Delta V_{BE}$, $-\Delta V_{BE}$, 0, and $-\Delta V_{BE}$, respectively.

To suppress the residual offset of the first integrator, as well as the mismatch of the two sampling capacitors, the ADC also employs system-level chopping. This is implemented by

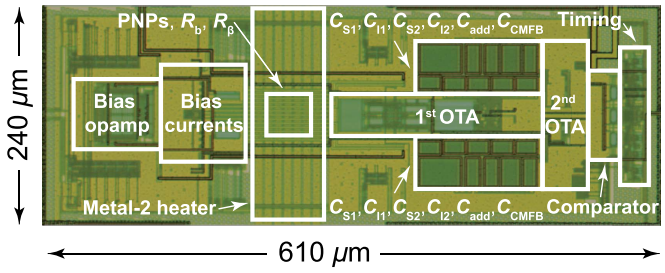

Fig. 8. Chip micrograph.

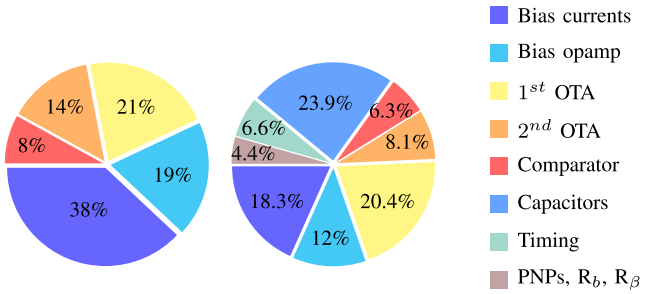

Fig. 9. TDC's (left) power and (right) area breakdown.

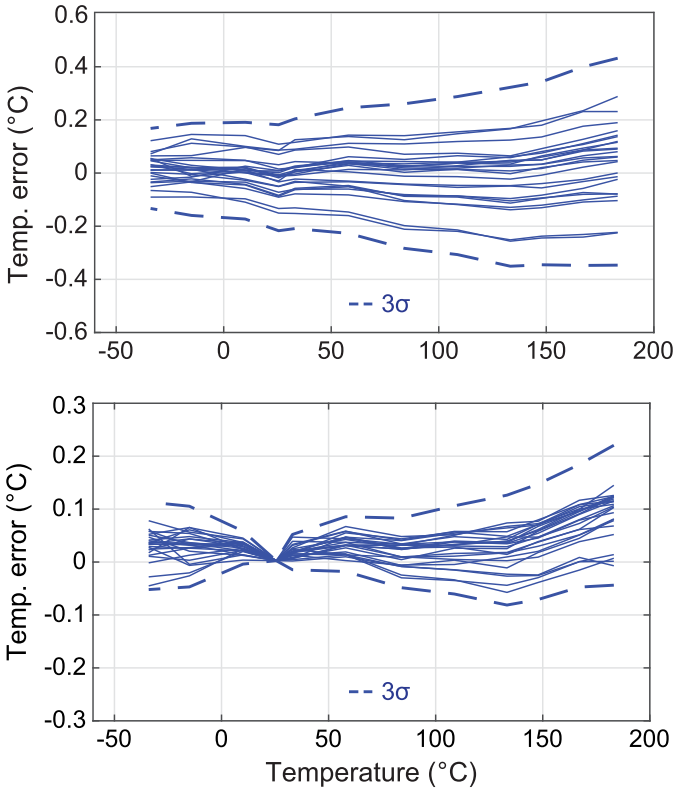

Fig. 10. Measured inaccuracy of 24 TDC samples. Top: untrimmed. Bottom: after temperature calibration and trimming at room temperature.

chopping $V_{\Sigma\Delta}$ and digitally inverting the bitstream polarity. The ADC's final output is then the average of two subconversions, each made with a different polarity of the system-level choppers.

In the proposed ADC, the time allocated to $\Delta V_{\rm BE}$ sampling is the same as that allocated to $V_{\rm BE}$ sampling. Since $\Delta V_{\rm BE}$ is significantly smaller than $V_{\rm BE}$ (about 16× smaller at 25 °C), this means that too much time is allocated for $\Delta V_{\rm BE}$ sampling. This, in turn, results in a significant loss of energy efficiency. As in [22], a better approach would be to use different settling times for $\Delta V_{\rm BE}$ and $V_{\rm BE}$, at the expense of a more complex clock generator.

V. Experimental Results

The TDC is realized in a 0.16-μm standard CMOS process and occupies 0.15 mm^2 (see Fig. 8). The TDC circuitry occupies 0.05 mm^2; a breakdown is provided in Fig. 9. The on-chip heater occupies 0.017 mm^2, which corresponds to 11% of the total occupied area. When supplied from a nominal 1.8 V, the TDC draws 5.41 μA; the bias currents make up 38%, the bias opamp consumes 19%, and the first- and second-stage integrators and the comparator consume 21%, 14%, and 8%, respectively. For flexibility, the calibration logic and decimation filter are realized off-chip. The TDC achieves a thermal-noise limited resolution of 23 mk (rms), in a 20-ms conversion time. This corresponds to a resolution FoM of 103 pJK^2.

To evaluate the TDC's accuracy, 24 samples from one wafer were packaged in ceramic (DIL-28) and then characterized from −40 °C to +180 °C in a climate chamber. As shown in Fig. 10 (top), the TDC achieves ±0.45 °C (3σ) inaccuracy after batch calibration. This improves to ±0.2 °C [see Fig. 10 (bottom)] after temperature calibration at room temperature followed by a PTAT trim. Note that no systematic nonlinearity correction is applied.

Table I summarizes the TDC's main characteristics and compares it with [3] and [10], which are both based on zoom ADCs and other high-temperature CMOS TDCs. Although not as energy efficient as the zoom ADC-based designs, its relative inaccuracy is comparable to [10] and 2× better than [3]. With the exception of [10], it also consumes significantly less power than the other designs.

A. Heater Operation

Since the resistance of the heater has a significant TC (∼0.3%/°C), the temperature of the heater can be accurately determined by measuring its resistance. This was calibrated in a climate chamber and found to vary from about 18 Ω at 25 °C to about 27 Ω at 180 °C. The on-chip Kelvin contacts were used to exclude the series resistances introduced by the bonding wires, PCB traces, and external switches. Similarly, $\Delta V_{\rm BE}$ was voltage calibrated to determine the exact temperature of the PNPs.

Fig. 11 shows the measured response of the PNPs and the heater when a 5.3-V pulse is applied to the heater. Both the heater and the TDC are clocked by an FPGA, allowing their operation to be accurately synchronized. Initially, the temperature of the heater rapidly rises from ∼25 °C to ∼170 °C. The temperature of the PNPs also changes rapidly but only reaches a maximum of ∼90 °C since they are separated

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER HIGH-TEMPERATURE CMOS TDCS

Item	This work		[10]	[3]	[5]	[8]	[9]
Sensor type	BJT		BJT	BJT	BJT	TD [a]	Resistor
Technology (μm)	CMOS (0.16)		CMOS (0.16)	CMOS (0.16)	CMOS SOI (1)	BiCMOS SOI (0.5)	CMOS (0.18)
Temperature range (°C)	−40 to 180		−55 to 125	−55 to 200	25 to 225	−70 to 200	−40 to 180
Inaccuracy (°C)	±0.2 (3σ)	±0.25 (3σ)	±0.1 (3σ)	±0.4 (3σ)	±1.6 [b]	±0.4 (3σ)	±0.11 (3σ)
Relative inaccuracy (%)	0.18	0.23	0.11	0.31	1.6	0.30	0.10
Calibration (points)	Temp (1)	HA-VCAL (2)	Temp (1)	Temp (1)	Temp (1)	Temp (1)	Temp (2)
Power (μW)	9.75		6.9	35	90	2600	52
Area (mm^2)	0.15		0.17	0.1	0.41	1	0.12
Resolution (mK)	23		7.5	20	200 [c]	75	0.46
Conversion time (ms)	20		20	4.2	100	1430	10
FoM (pJK^2) [d]	103		7.8	59	40×10^3	21×10^6	0.11
Samples	24		20	16	7	12	20

[a] Thermal diffusivity. [b] Worst case. [c] Calculated based on the reported 10-bit counter.
[d] (Energy per conversion)×(resolution^2).

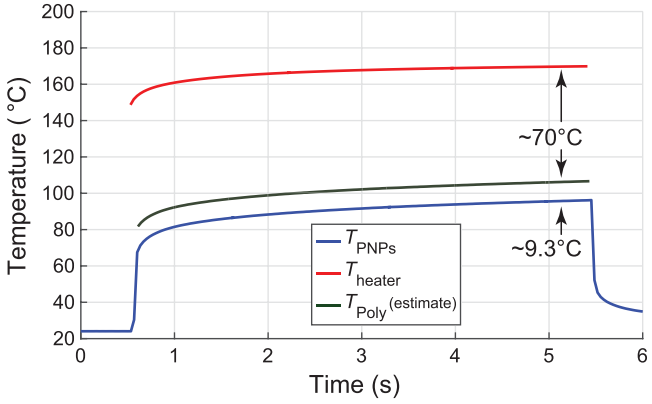

Fig. 11. Measured temperature of the PNPs, and the on-chip heater, in a thermal transient.

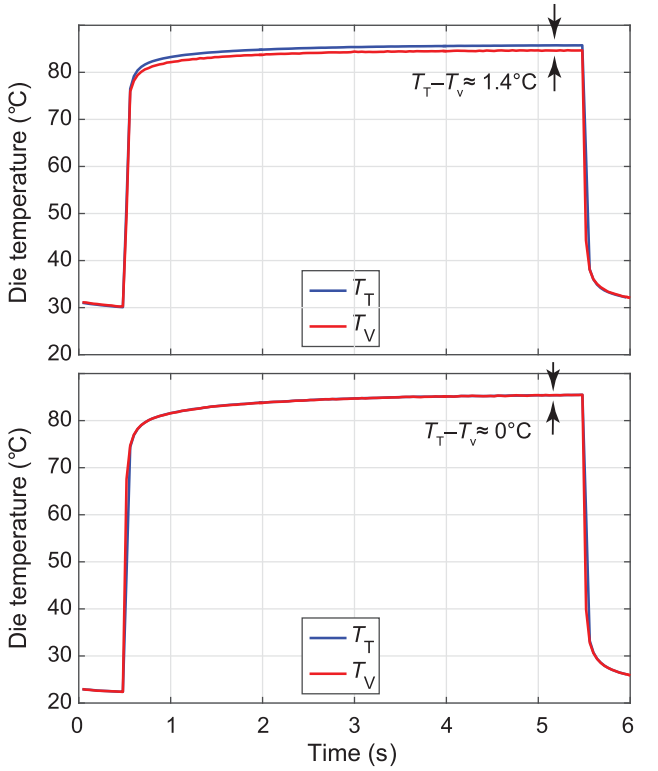

Fig. 12. Voltage calibrated T_V and temperature calibrated T_T outputs of TDCs during a transient heating. Top: based on a zoom ADC. Bottom: based on the proposed low-leakage ADC.

from the heater by insulating layers of oxide. The initial rapid rise in temperature is followed by a slow settling phase, which is mainly due to the large thermal time constant of the package.

The temperature difference between the poly resistors and the PNPs can be estimated by assuming that the temperature difference (∼80 °C) between the PNPs and the heater is uniformly distributed over the oxide layers between them. Using the layer thicknesses given in the technology datasheet, the estimated poly-PNP temperature difference is ∼9.3 °C, in reasonable agreement with the COMSOL simulations.

B. Local Heating Versus Uniform Heating

An experiment was carried out to verify that the output of the TDC during local heating is well correlated with its output during uniform heating. In other words, to verify that local heating no longer causes the systematic calibration error observed in [10]. First, both temperature calibration and VCAL were performed on a TDC, while it was uniformly heated in a climate chamber. The resulting outputs, T_T and T_V, respectively, were then used to obtain master curves. These curves were then used to determine the temperature of the TDC during HA-VCAL. As shown in Fig. 12 (bottom), there is an excellent agreement between the two curves (mainly limited by the TDCs own noise). In contrast, a systematic error of about 1.4 °C can be seen in the results obtained with the TDC of [10]. This demonstrates the effectiveness of the proposed ADC in mitigating front-end errors due to switch leakage.

C. Conventional VCAL Versus HA-VCAL

The ultimate accuracy of HA-VCAL is limited by the spread in T_V above room temperature. Fig. 13 (top) shows the spread in T_V from 10 °C to 130 °C.

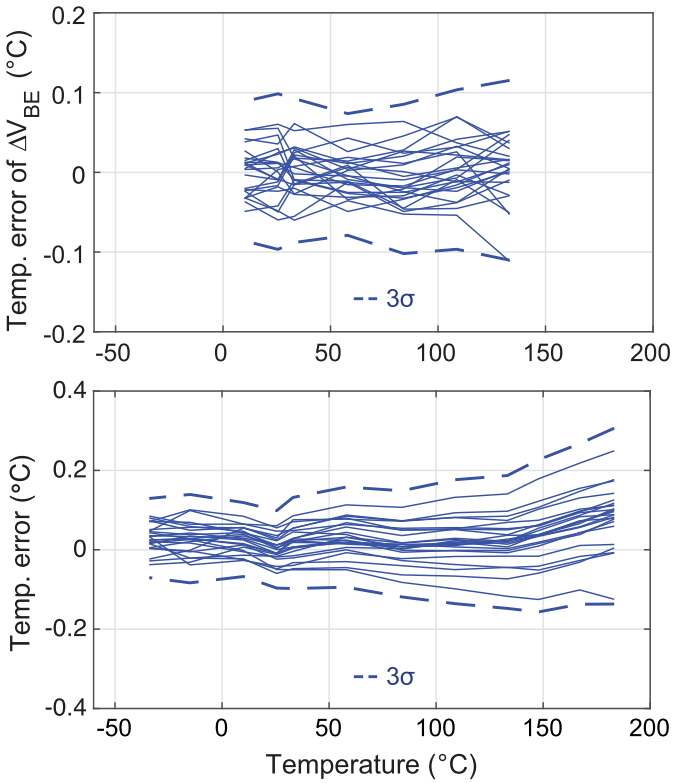

Fig. 13. TDC inaccuracy using conventional VCAL. Top: inaccuracy of T_V obtained from ΔV_{BE} measurement. Bottom: VCAL at room temperature.

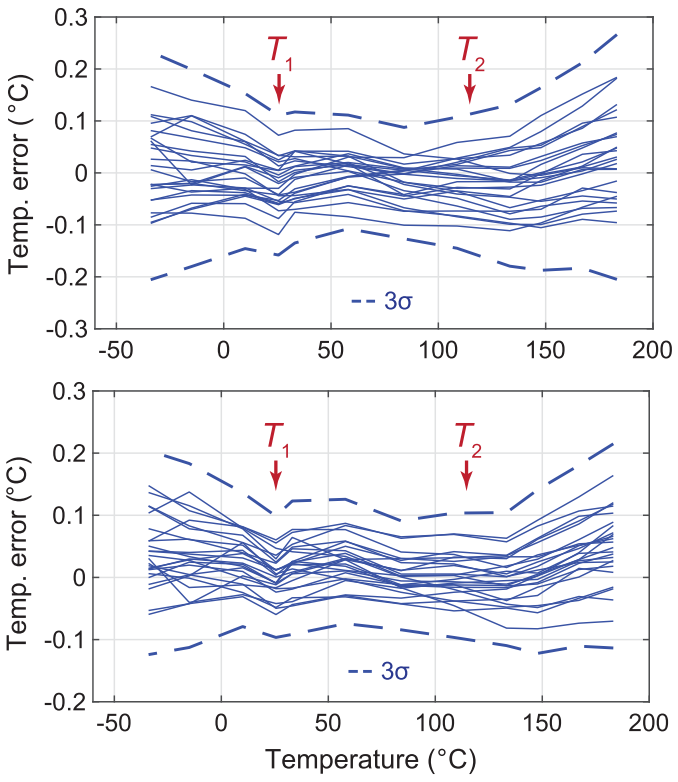

Fig. 14. TDCs inaccuracy after using heater-assisted two-point VCAL. Top: using the on-chip heater. Bottom: using a climate chamber.

As shown in Fig. 13 (bottom), after VCAL at ∼25 °C, the TDC achieves ±0.3 °C (3σ) inaccuracy from −40 °C to +180 °C. This improves to ±0.25 °C after HA-VCAL at T_1 ∼25 °C and T_2 ∼110 °C, as shown in Fig. 14 (top). Further increases in T_2, which would be expected to result in even higher accuracy, were limited by the heater's maximum current-handling capability.

To further verify the robustness of HA-VCAL, two-point VCAL was performed by uniformly heating the same TDC samples in a climate chamber. Fig. 14 (bottom) shows the results, where T_1 and T_2 are the same as in Fig. 14 (top). This results in an inaccuracy of ±0.2 °C (3σ), which is slightly better than those obtained with HA-VCAL. However, this comes at the expense of significantly more calibration time: tens of minutes versus 0.5 s for HA-VACL.

D. Post Package HA-VCAL

HA-VCAL can also be used to correct for the non-PTAT shift in V_{BE} caused by packaging stress [23]–[25]. This shift depends on the location of the sensing PNPs on the die, as well as on the package type and size. For a given package, this can be mitigated with the help of package-specific calibration parameters, obtained by batch calibration. Higher accuracy can be achieved with two-point temperature calibration at the expense of increased cost. HA-VCAL is a low-cost alternative since it can be applied to any package and does not require a temperature-controlled environment. This has been demonstrated in [10], where HA-VCAL was used to obtain similar accuracy in both plastic (SO-20) and ceramic packaged (DIL-20) TDCs.

VI. Conclusion

A TDC that operates up to +180 °C, while achieving state-of-the-art inaccuracy (±0.2 °C (3σ), 24 samples) and power consumption (9.75 μW), has been presented. It employs an SC-ADC based on two sampling capacitors, substantially reducing the number of switches, and, hence, the associated high-temperature leakage currents in its analog front end. The TDC is also equipped with an on-chip heater, which is used to implement HA-VCAL. This enables rapid two-point calibration with purely electrical measurements. Although somewhat less accurate than temperature calibration [±0.25 °C (3σ)], it is much faster and cost efficient since it can be carried out within 0.5 s without the need for a temperature-stabilized environment.

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