An Algorithmic Readout Approach for Thermal Conductivity Based CO_2 Sensors

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Dedicated to my beloved parents

Abstract

This thesis presents a new approach to reading out thermal-conductivity-based gas sensors. This method is intended for the readout of a CMOS-compatible resistive thermal-conductivity transducer for indoor CO_2 sensing applications, without requiring precision off-chip components. Instead of accurately regulating the power dissipated in the transducer and measuring its temperature, the temperature and power dissipation are both measured using an algorithmic approach. A high-resolution ADC digitizes the voltage drop across the transducer and the current through it, measured using an on-chip reference resistor. Moreover, by digitizing several base-emitter voltages of an on-chip bipolar transistor, a precision bandgap voltage reference is constructed in the digital domain, and accurate information about the ambient temperature is obtained, which is used to temperature compensate the voltage reference and the reference resistor. Thus, all necessary ingredients are obtained to calculate the power dissipation and temperature of the transducer, from which the thermal conductivity of the surrounding air, and hence CO2 concentration, can be obtained.

A prototype integrated circuit implementing this readout approach has been realized in 0.16μm CMOS. It has been tested in a climate chamber in combination with a platinum resistor mimicking the transducer. The digitally-constructed voltage reference has a temperature coefficient of 9ppm/$^\circ$C, while ambient temperature is sensed with accuracy of $\pm$0.2°C, with a resolution of 0.15°C. The resistance readings have an inaccuracy ranging between -1mΩ to 4mΩ on a nominal resistance of about 100Ω (-10ppm - 40ppm) with a resolution of around 2mΩ in the temperature range from 10°C to 40°C; for the power measurements, the circuit achieved an accuracy between -0.03% and 0.06%, with an 800nW of resolution (in the same temperature range) which is one

order of magnitude better than results presented in previous work.

Although no CO_2 measurements have been performed, an estimated thermal-resistance accuracy of around 2862ppm with a resolution of 155.64[K/W] should be possible, which would enable detection of the CO_2 levels in the air with an accuracy of around 0.72% and a resolution of 7705ppm.

Acknowledgements

This work would have not been possible without the help ad support of many people. First of all, I would like to thank Michiel, my supervisor, for the opportunity of being part of his research group, and his great guidance during the past year and 2 months; I learned a lot from him and his experience. Also, I would like to thank Zeyu, my co-supervisor, who always was there for any trouble I encountered. And Robert, my supervisor from NXP, thank you for all your time and help, you beleive in this project from the very begining.

But, none of this would have been possible without the love and support of my family. My two brothers that have been always giving me their hand when I needed, and my parents: dad, mom...*tienen un hijo master*!!!

Thanks to all my friends, without you around to go out for a beer, to a party, or just to hang out and talk about anything, these two years would have not been the same. You guys are amazing!!!!

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Chapter 1

Introduction

THE Indoor Air Quality (IAQ) of a building is a very important indicator of human comfort. One of the many ways used by HVAC (Heating, Ventilating and Air Conditioning) systems to determing IAQ is by measuring the CO_2 concentrations in the air; one could think of a room that gets full of people, where the air inside can get stale, which is mostly due to exhaled carbon dioxide (CO_2), causing a reduction of the well-being, lack of concentration and deterioration in performance.

An adult person, on average, exhales 35000 to 50000 CO_2 molecules per million molecules of air [1], or parts per million (ppm), which is around 100 times higher than what is found typically in the outside air (OSA). According to the American Society of Heating Refrigerating, and Air Conditioning Engineers (ASHRAE), the recommended maximum level of CO_2 at indoor environments should not exceed the OSA concentration by more than about 650ppm, which would give a maximum value of 1030ppm of CO_2 concentration in the air.

High CO_2 levels could be mitigated by implementing a constant ventilation rate, where OSA is let into the building. This approach is not very energy efficient, since it doesn't take into account the occupancy rates (how many people are inside); by using a Demand Controlled Ventilation (DCV) system, monitoring constantly the CO_2 concentration with an accurate sensor, it is possible to save from 5 to 27% of the HVAC energy usage in a common office

environment, and even more, in places with high occupancy rates [1].

Infrared spectroscopic analyzers are commonly used for this purpose, but their large size and high cost are great disadvantages of these types of CO_2 sensors [2]. Silicon-based CO_2 sensors can overcome such problems, and at the same time obtain more reliable systems with lower power consumption.

This chapter presents the CO_2 sensor used in this project, as well as its physical parameters. With the target resolution of the CO_2 sensor (100ppm) the relative variations of the transducer's power consumption and temperature are found. Also, the study of the state of the art of circuits that can provide a constant power to a load independent of its value is reviewed, as well as the state of the art of CO_2 sensors, mainly, based on the thermal conductivity approach. Finally, the proposal of a "Constant Power" circuit in which the CO_2 sensor will be based is presented, which will be further explained in the next chapter.

1.1 The CO_2 Sensor

In this work, a micro Thermal Conductivity (μTC) pellistor is used as the transducer to sense the CO_2 concentration in the air (see Figure 1.1). These transducers have a calorimeter component (for this transducer a tungsten wire is used) and a cavity underneath it (created by etching the surrounding oxide), which causes the wire to be suspended in ambient air [3]. The tungsten wire is then heated in order to detect the gas' thermal conductivity; normally, it is heated to a specific temperature, or at a well defined power level. In this work, the latter approach will be of most interest to develop the CO_2 sensor.

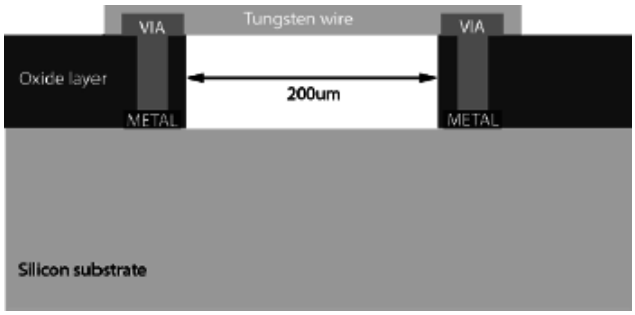


Figure 1.1: Cross-section of the μTC transducer.

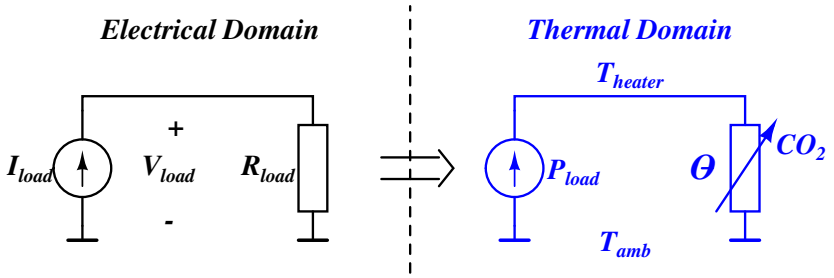


Figure 1.2: Electrical and Thermal Equivalent.

1.1.1 The Thermal Conductivity Approach

A μTC-based gas sensor relies on the sensing of the gas' thermal conductivity. The changes in the thermal conductivity can be detected as changes in the way a heated wire loses its heat to the ambient, since this heat loss is partially determined by the conductive losses through the air. Due to the difference in the thermal conductivity of the CO_2 (0.0168 $^{W}/_{m\cdot K}$ at 300K and 1bar) and the air (0.0262 $^{W}/_{m\cdot K}$ at 300K and 1bar), when the transducer is in an environment with levels of CO_2 in the air, its thermal heat transfer characteristic changes, making possible the detection of CO_2 concentration in the air.

In reality, what is measured is the thermal conductance (or its reverse, the thermal resistance) of the transducer, which is then translated to CO_2 concentration in the air. The thermal resistance Θ can be expressed in terms of the CO_2 concentration in the air (Q_{CO_2} in parts-per-million, ppm) as:

$$\Theta = \Theta_o + S_\Theta \cdot Q_{CO_2} \tag{1.1}$$

where Θ_o is the thermal resistance of the transducer at 0ppm CO_2 concentration and S_Θ is the sensitivity of the transducer to the CO_2 levels in the air, in $[^{K}/_{W\cdot ppm}]$.

In this kind of devices, an interaction between the thermal and the electrical domain is present which makes it possible to measure the thermal resistance (see Figure 1.2). In the thermal domain, the heat flux caused by the power P_{load} dissipated in the device acts as the equivalent of an electrical current, while the resulting temperature difference acts as the equivalent of a voltage. The thermal resistance (Θ) acts as the equivalent of the electrical resistance, which depends on the CO_2 levels in the air, as shown before.

One of the main approaches in thermal-conductivity-based CO_2 sensing schemes is the measurement of the temperature difference between the load and the environment (ΔT), while keeping constant the power dissipated in the load to a known value.[1] Normally, either of two different ways are used to measure ΔT: via a separate temperature sensor (commonly a thermocouple [4]), or by using the heater itself.[2] The latter is decided to be used in this work, since it is easier to manufacture.

Stabilizing the power dissipated in the load is not a trivial task, as it requires a stable power reference. An additional complication is the temperature dependency of the heater, which derives in the self-heating effect; due to the power dissipated in the device, it will heat up and change its nominal resistance, hence changing the power dissipated in the resistance.

Mathematically speaking, the thermal and electrical resistances can be expressed as follows (Equations 1.2 and 1.3, respectively):

$$\Theta = \frac{\Delta T}{P_{Load}} \tag{1.2}$$

$$R_{load} = R_o \cdot \left[1 + \alpha_R \cdot (T_{amb} + \Delta T - T_o)\right] \tag{1.3}$$

where, T_o and T_{amb} are the reference and ambient temperature respectively, α_R is the temperature coefficient of the resistance, and R_o is the nominal resistance value at T_o.

It can be seen that the electrical resistance has a temperature dependent term[3] which is positive for the transducer used in this work, so when the device temperature is increased the electrical resistance increases. This property is used to sense ΔT, but it may also cause the power dissipated in the transducer to change, affecting the measurement of the CO_2 levels. Hence, an accurate power stabilization or measurement is needed.

[1] Actually, it is more important to maintain the power stable regardless if the value is known or not, since callibration techniques will be applied.

[2] Often used in microhotplates.

[3] It may also have higher-order temperature coefficients.

1.1.2 Target Specifications

It must be studied up to which levels of stability the power P_{load} dissipated in the load should be stabilized, and how accurate the measurementof of the temperature difference ΔT should be to ensure a proper reading of the CO_2 concentration. To do this, both ΔT and P_{Load} will be expressed in terms of R_{Load}, as:

$$\Delta T = \frac{1}{\alpha_R} \cdot \left[\left(\frac{R_{Load}}{R_o} - 1 \right) - \alpha_R \cdot (T_{amb} - T_o) \right] \tag{1.4}$$

$$P_{Load} = I_{Load}^2 \cdot R_{Load} = \frac{V_{Load}^2}{R_{Load}} \tag{1.5}$$

By substituting Equations 1.4 and 1.5[4] in Equation 1.2, R_{Load} can be found as a function of Θ by solving the following quadratic equation:

$$R_{Load}^2 - R_o \cdot [1 + \alpha_R \cdot (T_{amb} - T_o)] \cdot R_{Load} - (\alpha_R \cdot R_o \cdot V_{Load}^2) \cdot \Theta = 0 \tag{1.6}$$

In order to find numerical values for the changes in the power and temperature levels due to changes in the CO_2 concentration, in Table 1.1 the parameters of the transducer to be used in this project are presented.

The CO_2 sensor that is intended to be designed must be capable of sensing changes in the CO_2 concentration in the air of around 100ppm. From this information, the specification for the power stability needed can be derived. Furthermore, the raise in the temperature of the device as well as the variations of the temperature to changes in the CO_2 concentration can also be studied.

The procedure to find the relative variations[5] of the device's temperature and power to changes of 100ppm CO_2 concentration in the air ($\Delta Q_{CO_2} = 100$ppm) for different power levels is as follows:

1. With the target Power Level ($P_{load_o} = P_{load}(\Theta_o)$), R_{load} (Eq. 1.6), the V_{load}

[4]The term related with the load voltage will be used since the final expression is easier to manage.

[5]The relative variations are calculated with respect to the values at $Q_{CO_2} = 0$ppm.

Parameter	Description	Value
R_o [Ω]	Nominal electrical resistance @ T_o	100
α_R [K^{-1}]	Electrical resistance 1st-order temperature coefficient	2.6m
T_o [°C]	Reference Temperature	27
Θ_o [K/W]	Thermal resistance @ $CO_2 = 0$ppm	51k
S_Θ [K/(W· ppm)]	Thermal resistance sensitivity to the CO_2 concentration (ppm)	20.2m

Table 1.1: Transducer's parameters.

(Eq. 1.5) and ΔT at $Q_{CO_2} = 0$ppm can be found. The load voltage will be maintained constant for the following calculations.

2. The thermal resistance (Θ_1) is calculated from Equation (1.1) for $Q_{CO_2} =$ 100ppm. With the latter, the new value of R_{load}, and hence, P_{load} and ΔT can be obtained.

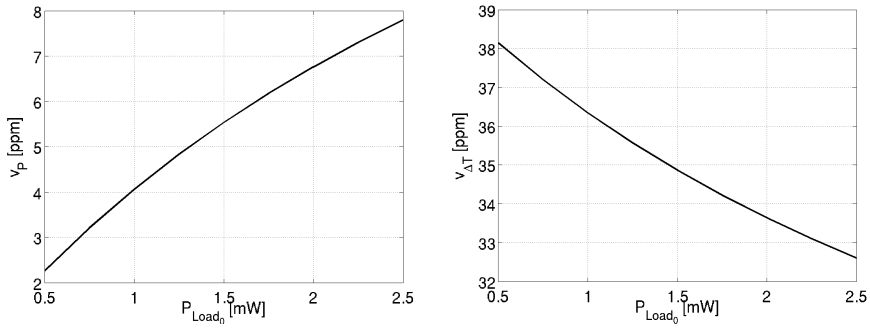
3. The relative variations are then calculated as:

$$v_P = \frac{P_{load}(\Theta_1) - P_{load}(\Theta_o)}{P_{load}(\Theta_o)} \tag{1.7}$$

$$v_{\Delta T} = \frac{\Delta T(\Theta_1) - \Delta T(\Theta_o)}{\Delta T(\Theta_o)} \tag{1.8}$$

where v_P and $v_{\Delta T}$ are the load Power and ΔT relative variations to 100ppm changes in the CO_2 concentration in the air. The plots of these variations as a function of the target power dissipation in the load (P_{load_o}) are shown in Figure 1.3.

It can be seen that when increasing the power dissipation in the transducer, the relative variation of the device's temperature decreases, while the relative variation of the load power increases. This means that the circuit should be able to stabilized the power dissipated in the transducer at the ppm levels presented in Figure 1.3a. Since power consumption is not an issue in this project, one could say that the best would be to dissipate more power in the device, in order to have more relaxed specifications. The latter finds a limitation when looking



(a) Relative variation of P_{Load} vs P_{load_o}. (b) Relative variation of ΔT vs P_{load_o}.

Figure 1.3: Relative variations due to 100ppm CO_2 concentration in the air, for different load power levels.

the temperature of the device for different power levels; Figure 1.4 shows this effect.

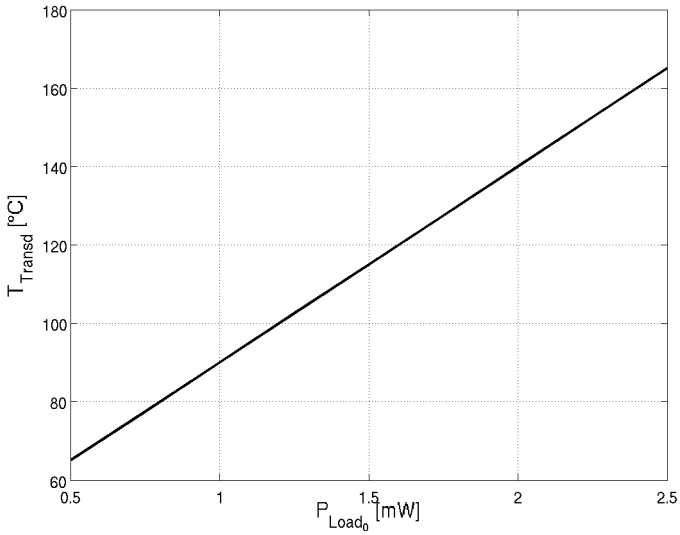


Figure 1.4: Transducer's temperature vs target load power dissipation (P_{load_o}) @ $T_{amb} = 40°C$.

A value for the power dissipation stability in the transducer must be selected as relaxed as possible, while at the same time limiting the temperature of the device. From the previous figures, one could agree that 1mW of power dissipated in the load could give a good trade-off between the mentioned conditions, with relative variations in the power levels and in the ΔT of 4ppm

and 36.2ppm, respectively, for 100ppm change in the CO_2 concentration and a device's temperature of 60-90°C in the ambient temperature range.[6] Table 1.2 shows the target specification of the CO_2 sensor, and the corresponding specification for the control of the power levels in the device, as well as the temperature of the heater and the temperature relative variation due to 100ppm changes in the CO_2 concentration.

Specification	**Value**
ΔQ_{CO_2} [ppm]	100
P_{Load} [mW]	1.0
ΔP_{Load} [nW]*	4.0
T_{amb} [°C] (range)	10-40
T_{Transd} [°C] (range)*	60-90
ΔT_{Transd} [mK]*	1.8
v_{Θ} [ppm]*	40
v_P [ppm]*	4.0
$v_{\Delta T}$ [ppm]*	36.2

* *For* $\Delta Q_{CO_2} = 100ppm$ *and* $P_{load} = 1mW$.

Table 1.2: Target Specifications.

From this table it can be concluded that the levels of stability needed for the power dissipated in the transducer are a great challenge for the design of a "Constant Power" circuit. In order to see if there is any circuit capable of achieving this kind of result, a study of the state of the art will be reviewed in Section 1.3.

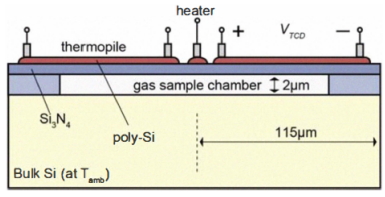
[6] The values for the temperature and power dissipation were obtained with the help of the transducer empirical model given by NXP.

1.2 State of the Art in Readout Circuits for Thermal-Based Gas Sensors

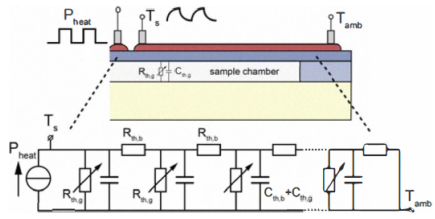
As described previously, the architecture for the CO_2 readout circuit will be based on the control of the power dissipated in the transducer, which is why the main focus of the literature review was the study of "Constant Power" circuits (Section 1.3). Nevertheless, in the literature are few readout mechanisms for themral-based gas sensors have been reported, and they will be shown in this section for benchmarking purposes.

1.2.1 Phase Readout of a Thermal Conductivity-Based Gas Sensor

The work presented in [5] focuses on H_2 sensing, and uses a different device structure than the one in Figure 1.1. Here an alternative to amplitude measurements is shown; basically, the shift between the heater driving signal and the thermopile output voltage is used as a measure of H_2 conccentration. The readout circuit is integrated with the micro-thermal conductivity detector (μTCD), which is presented in Figure 1.5.



(a) Schematic cross section of the μTCD gas sensor.



(b) Thermal filtering model of the μTCD.

Figure 1.5: Thermal Conductivity Gas Sensor based on a phase readout method [5].

Figure 1.5a shows the schematic cross section of the μTCD, and Figure 1.5b persents its thermal filtering model; since the components in this model (resistances and capacitances) are a function of the geometry of the μTCD, which are defined at manufacture, and will not vary significantly under the gas presence, having certain advantages over amplitude readings, which depends more on the gain accuracy of the electronic components used [5].

The system works by driving the μTCD with an AC heat signal and digitizing its gas concentration-dependent phase shift with a phase-domain sigma-delta

modulator (PDΣΔM). Simulations[7] of the system found that its SNR corresponds to a resolution of $0.07\%_{rms}$ H_2 concentration in the air (equivalent to 700ppm), in a 2Hz bandwidth at a power dissipation of only $50\mu W$.

Other gas sensors readout circuits are based on this approach [6, 7], although the readout circuits are not integrated with the sensor; also, the data acquisition is not done with a PDΣΔM. As a difference with [5], mechanisms to control the power dissipated on the heater are implemented, since the power levels are much higher (on the order of mW), increasing the error due to the self-heating effect [5].

The problem with this approach, is that the μTCD requires a more complex manufacture process, since it needs a thermocouple device. For this reason, this method will not be used in this work.

1.2.2 A μC-based Interface Circuit as Readout for a Thermal Flow Sensor

Although the main purpose of this work is to measure gas concentration, the work presented in [8] sensor is also included in the literature review, since the methodology implemented is very similar to the one that will be introduced later in this thesis.

A microcontroller-based interface circuit for data acqusition and control of a micromechanical thermal flow sensor is presented in [8]. The block diagram of the circuit interface is shown in Figure 1.6.

In this work, a polysilicon heating resistor and two thermopiles situated symmetrically on each side of the heater are used as a thermal flow sensor (similar as in [5]). The circuit contains an analog and digital part, which are developed in the same board. The data acquisition circuit can determine both the thermopile voltage and the heater resistance by the use of a multiplexer, employing the SPI port to transfer the corresponding values. In both cases a 16-bit ADC is used.

To determine the heater resistance, the voltage drop of a shunt resistor (R_s in the figure) connected in series with the heater is measured, and hence, the current through the heater is determined. The thermopile is used to measure the temperature of the heater.

[7] This paper doesn't present measurement results.

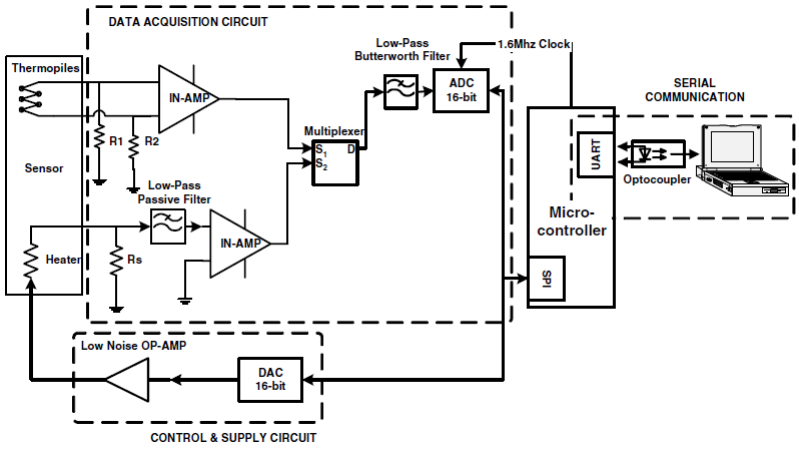


Figure 1.6: Block diagram of the circuit interface [8].

Three different modes can be used in this circuit interface: Constant Voltage (CV), Constant Power (CP, and Constant Temperature (CT) mode. The first one consists of applying a constant voltage, and sense back the thermopile voltage and heater current, from where the heater power and resistance can be obtained.[8] In the CP mode, a voltage is applied, and the same readings as in the previous case are obtained, but with the help of the control loop formed by the 16-bit DAC, a correction voltage can be applied, so to stabiliz the power on the heater. Finally, the CT mode is very similar to the CP mode, but instead of stabilizing the power, the algorithm focus on stabilize the temperature of the device.

The results show that this configuration is capable of stabilizing (measuring) the heater resistance and power consumption to the levels of $\pm 200\text{m}\Omega$ and $\pm 25\mu\text{W}$, respectively.

The main issue with this implementation, is that the applied voltage is considered constant, which could introduce significant errors in the power and resistance readings; even more, no analysis on the referencing accuracy and drift of the ADC and DAC, as well as for the shunt resistance (used as reference to sense the heater current) is addressed. As it will be shown later, the architecture that will be presented in this project, which is very similar to the one in Figure 1.6, tackles these problems, and propose a solution to them.

[8] This values will vary according to the thermal flow of the gas.

1.3 State of the Art in “Constant Power" Circuits

Although few circuits have been reported that are capable of maintaining a constant power dissipation in a load, independent of external factors (self-heating, ambient temperature, etc.), some of the architectures found will be studied in this section, and their advantages and disadvantages will be analyzed. A comparison will be made and conclusions on the different topologies will be drawn.

1.3.1 The Translinear Loop Circuit

In [9], the translinear principle is used in order to produce a constant output power independent of external factors. The translinear principle dictates that in a closed loop containing an even number of forward biased pn junctions arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction [10], or:

$$\prod_{\text{n} \in \text{CW}} J_n = \prod_{\text{n} \in \text{CCW}} J_n \tag{1.9}$$

Figure 1.7a) shows the core of the circuit that provides a constant output power. The translinear loop is formed by the bipolar transistors Q_1, Q_2, Q_3 and Q_4.

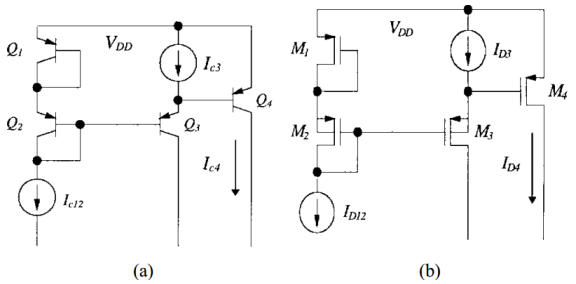


Figure 1.7: (a) Bipolar Translinear Loop. (b) Simple CMOS TL Loop [9].

In order to see how this circuit can maintain the power dissipation of a load constant, one can solve Equation 1.9 associated with the static translinear loop, obtaining the following relation:

$$I_{c12}^2 = I_{c3} \cdot I_{c4} \tag{1.10}$$

Now, if $I_{c3} = V_{load}/R_{ref}$, $I_{c4} = I_{load}$ and $I_{c12} = I_{ref}$, then:

$$P_{Load} = V_{Load} \cdot I_{Load} = I_{ref}^2 \cdot R_{ref} \tag{1.11}$$

Suppossing that the reference resistance and current are ideal and constant, it can be concluded that the load power is maintained constant, independent of any other factors. Of course, in practice, since there are no ideal resistances nor ideal current sources, there will be always some remaining errors.

The interesting thing about the circuit presented in [9], is that no bipolar transistor was implemented; instead, a bipolar-like CMOS equivalent is implemented, where the transistors are in saturation (Figure 1.7b). The bahavior of this circuit will deviate even more from the ideal case, and although for the work presented in the paper it was enough, for this project it may not be adequate due to the tight specifications already described.

A stability of $\pm 1\%$ was reported for variations in the load resistance of $\pm 50\%$ ($1k\Omega$) at 5.8mW of power dissipation. A lower stability was achieved ($\pm 3\%$) when dissipating 11mW of power. A dual-supply voltage is used of $\pm 5V$. It must be mentioned, that nothing is reported about the current reference construction, and no temperature behavior is presented.

A list of the limiting factors that can cause this circuit to not behave as in the ideal case can be drawn:

- Stability of the current reference and resistance reference (power reference).
- Precision of the current mirrors.
- OpAmp's offset & gain (also their temperature drift).
- Matching of the transistors.
- Thermal noise.

This list will be analyzed later in this chapter, since almost all the topologies found in the literature have the same kind of restrictions.

1.3.2 The Power Regulator

In [11], a circuit capable of regulating the power delivered to a load is presented (see Figure 1.8). The key to this circuit is the high-side power and current monitor IC1 (MAX4210), which includes the circuitry necessary to generate a feedback voltage proportional to the instantaneous load power. It contains a current monitor that measures load current, a voltage divider to measure load voltage, and an analog multiplier that multiplies the two together, producing an output voltage proportional to the load power.

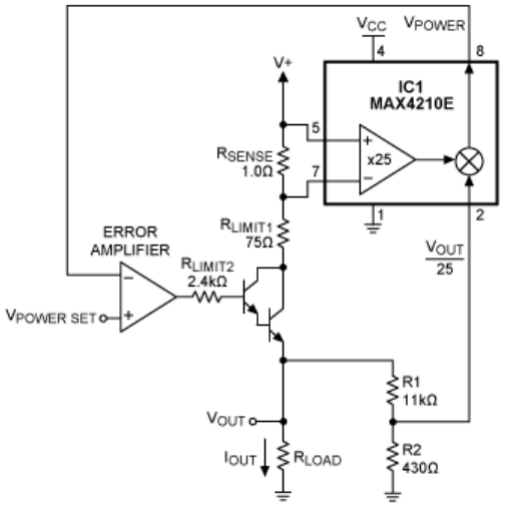


Figure 1.8: Power Regulator using a load-monitoring IC (MAX4210) [11].

Other components can be seen in this circuit, such as the sense resistor R_{sense}, used in the first input of the monitor IC1, as well as the resistive divider formed by R_1 and R_2 used to sense the load voltage which is applied to the second input of IC1. Also, an error amplifier is implemented; it drives a high-gain Darlington pair, which is used to minimize base current, which flows in the load but not through the sense resistor. This error amplifier forces the output of IC1 (proportional to load power) to equal the VPOWER SET signal, provided by a reference voltage circuit. This circuit is used to control the power dissipated in the heater material in [7], mentioned in Section 1.2.1.

Although no stability values were reported, the circuit supports variations in the load resistance from 10Ω-500Ω, and different power levels up to 100mW. A supply voltage of $\pm$18V was used.

As before with the translinear circuit, a list with the main limitations for this

architecture is presented:

- Stability of the current reference and resistance reference (power reference).
- Stability of the voltage divider and amplifier's gain.
- Stability of the multiplier.
- OpAmp's offset & gain (also their temperature drift).
- Matching of the transistors.
- Thermal noise.

1.3.3 The Resistive Mirror Constant Power Circuit

In [12], a constant power circuit based in a resistive mirror architecture is presented. The basic principle of the circuit is shown in Figure 1.9.

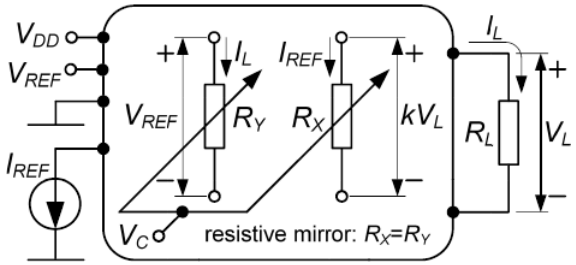


Figure 1.9: Basic principle of the constant power circuit using resistive mirror [12].

In the figure, V_L and I_L are the voltage and current of the resistive load R_L, respecitvely, V_{REF} is a reference voltage, I_{REF} is the reference current, R_X and R_Y are Voltage Controlled Resistances (VCRs) forming the resistive mirror controlled by the control voltage V_C, k is a constant lower than 1, and V_{DD} is the supply voltage.

The topology proposed in [12] (Figure 1.10), is such that the following is fullfilled:

- The current flowing through R_X (transistor M_2 in the figure) is I_{REF}.
- The voltage across R_X is proportional to V_L by a proportional factor k.

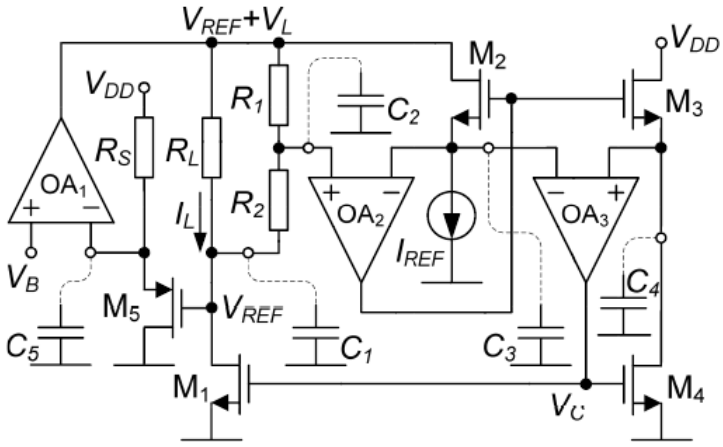


Figure 1.10: Schematic of the constant power circuit using resistive mirror [12].

- The current flowing through R_Y (transistor M_1) is nearly I_L.
- The voltage across R_X is proportional to V_{REF}.

The resistance R_X and R_Y can be then calculated as follows:

$$R_X = \frac{kV_L}{I_{REF}} \tag{1.12}$$

$$R_Y = \frac{V_{REF}}{I_L} \tag{1.13}$$

since these resistances form a “resistive mirror", they are equal; hence, the power dissipated in the load can be expressed as:

$$P_L = V_L I_L = \frac{1}{k} V_{REF} I_{REF} \tag{1.14}$$

which is independent of the load value R_L.

A stability of around $\pm 0.4\%$ was reported for variations in the load resistance of $\pm 50\%$ (1kΩ) at 0.48mW of power dissipation. Other stabilities were achieved at different power levels ($\pm 2\%$ at 1.2mW) with the same load variation. A supply voltage of ± 7V was used.

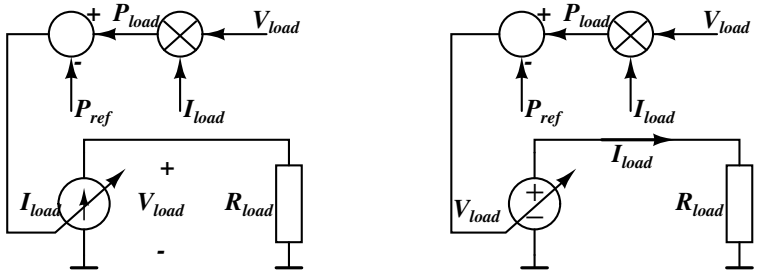
A list of limitations can be derived (as for the topologies already discussed) for this architecture:

- Stability of the current reference and voltage reference (power reference).
- Stability of the voltage divider (R_1-R_2).
- OpAmps' offset & gain (also their temperature drift).
- Matching of the transistors.
- Thermal noise.

From the previous list, some similarities can be found with respect to the previous architectures and other topologies in the literature [13–15]. Due to the latter, a general analysis of the approaches to have a "Constant Power" circuit and their limiting factors will be done in the next section.

1.4 Power Control

From the topologies found in the literature, a general mechanism to create a "Constant Power" circuit can be derived. Figure 1.11 shows the block diagram explaining the general approach behind the control of the power dissipation.



(a) Current Approach. (b) Voltage Approach.

Figure 1.11: Power Control.

As it can be seen, the approach that all the circuits implement to control the power dissipated in a load uses a feedback network where they:

- Sense the load voltage (V_{load}) and load current (I_{load}).

- Multiply them (analog multiplier: Gilbert cell, TL circuit, etc) to obtain P_{load}.
- Compare the result with a “Power Reference" (P_{ref}).
- Correct for errors.

The last item on the list, the error correction, can be performed in two different ways: by correcting the current (Current Approach), or by correcting the voltage (Voltage Approach).

1.4.1 The Current Approach

In this approach, the error signal controls the current which is applied to the load of the circuit. Figure 1.11a shows the block diagram of this mechanism.

In this approach when no feedback is applied to corrrect for any variations in the load power with respect to the reference, a positive feedback loop is formed between the thermal and electrical domain (Self-Heating Effect).[9]

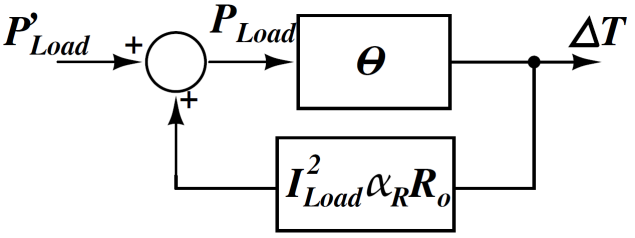


Figure 1.12: Electric-Thermal Feedback Loop (Self-Heating Effect).

Figure 1.12 illustrates the mentioned loop, where I_{Load} is the applied current (which is constant because no correction is applied), Θ is the thermal resistance, α_R is the electrical resistance's first order temperature coefficient, R_o is the nominal electrical resistance at the reference temperature, and P'_{load} is the power dissipated in the load if the self-heating effect is not taken into account:

$$P'_{load} = I^2_{Load} \cdot R_o \cdot [1 + \alpha_R \cdot (T_{amb} - T_o)] \tag{1.15}$$

[9]The current approach leads to a positive feedback loop if the resistance temperature coefficient is positive, which normally is the case.

In other words, when applying a current through the transducer, this would dissipate some power, which will increase the temperature of the device; due to the self-heating effect, the electrical resistance will also increase, further increasing the power dissipation.

When analyzing the transfer function, one can come to the conclusion that in order to obtained a stable system, the loop gain must be lower than one; the condition for complete stability can be drawn as:

$$\Theta \cdot I_{Load}^2 \cdot \alpha_R \cdot R_o < 1 \tag{1.16}$$

Since the electrical and thermal resistances, and the temperature coefficient are parameters given for an specific transducer, the current applied to the device will be the dominant factor for the stability condition. In any case, there could be an issue if the transducer's parameters suffer from process variability. This can be solved if a voltage approach is implemented.

1.4.2 The Voltage Approach

In the voltage approach, the correction is done by changing the load voltage (see Figure 1.11b). In contrast to the current approach, when operating the voltage approach in an open loop configuration, the Self-Heating Effect forms a negative feedback loop.

Qualitatively speaking, when a voltage is applied to the load, some power will be dissipated, elevating the temperature of the device and increasing its electrical resistance; this will reduce the load power, which at the same time will decrease the heater temperature and its electrical resistance, further increasing the power dissipation, and so on. This process will continue until the system stabilizes, which will depend on the loop gain of the control network.

1.4.3 Limitations

All the topologies in the state of the art share some limitating factors, which can be divided into two groups:

- Circuit-related Limitations:

  - OpAmp's gain & offset.
  - Stability and precision of analog multipliers, voltage dividers, current mirrors, etc.
  - Matching.
  - Thermal noise.

- Fundamental or External Limitations:
  - Power reference (voltage, current and resistance references).

In the first group, all the errors that can be corrected by circuit techniques, better design and layout are listed. On the other hand, in the second group the power reference is shown as the fundamental or external limiting factor; as it was seen, in all of the architectures a reference is needed in order to construct a control loop to maintain stable the power dissipation.

1.5 Proposal

After analyzing the general methodology to create a "Constant Power" circuit and discussing the main limitations of these types of circuits, a new approach to this issue is presented in this work.

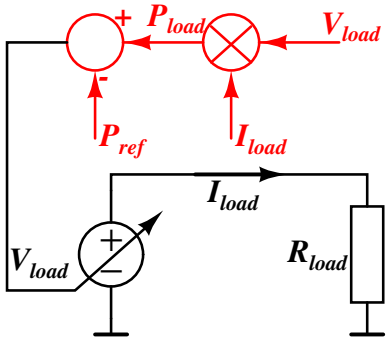


Figure 1.13: Proposal Block Diagram.

The main objective will be to reduce the circuit-related errors that were stated before, by implementing an approach where the circuit does the least harm to the sensing scheme. To achieve the latter it is proposed that instead of implementing the signal processing and feedback loop (see the red part in

Figure 1.13) in the analog domain, as is commonly done, these tasks will be performed in the digital domain by digitizing the necessary signals with a high resolution ADC.

Furthermore, the fundamental problem due to the reference voltage will be engaged by implementing a new technique where the construction and compensation of such a reference is done in the digital domain. At the same time, with the same components used to construct the reference, a a digital temperature sensor can be obtained. The temperature sensor enables compensation for cross-sensitivity to ambient temperature of the voltage and resistance references, which will be fully explained in the next chapter.

1.6 Summary

In this Chapter, the CO_2 transducer that has been used in the project is described, as well as the thermal-conductivity approach to measure the CO_2 levels in the air. After showing the target CO_2 resolution and the transducer's parameters, the relative variation of its temperature and power consumption have been investigated, to see the stability needed in the Constant Power circuit, and the resolution of the temperature sensor, elements needed for the construction of the CO_2 sensor. A study of the state of the art for Constant Power circuits, as well as for the CO_2 sensor, has been shown, reviewing some of the most popular approaches for both cases. Finally, the proposal to be implemented in this project has been introducedi. This will be explained in more detail the next chapter.

Chapter 2

Architectural Design

As described in the previous chapter, the proposal in this work is to control the power dissipated in the transducer in order to sense changes in the CO_2 concentration in the air from changes in the resulting temperature of the transducer. This chapter describes in detail the proposed architecture, and how the limitations listed before are tackled with this architecture.

It is organized as follows: first, the power measurement and control scheme is presented, and then, the development of the architecture is shown, where the construction of a digital reference is described, followed by an explanation on how from this approach, the readout circuit for the CO_2 sensor can be obtained. Finally, an accuracy analysis is presented, were the most important error sources of the circuit are included.

2.1 Power Measurement and Control

Based on the approach of sensing the load voltage and current to control the power dissipated in a load, a new approach to measure and control the load power is presented in this work. Figure 2.1 presents the block diagram of the basic idea behind this new approach.

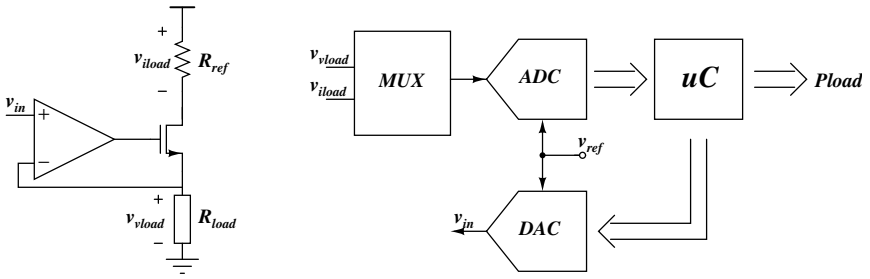


Figure 2.1: Block diagram for the measure and control of the load power.

From the block diagram it can be seen that through a voltage-to-current converter a voltage is applied to the load (transducer), while driving the current with a MOS transistor and sensing the current with a reference resistor. The measurement of the load current and load voltage is carried out with a high-resolution ADC in order to perform the signal processing in the digital domain (with a microcontroller or FPGA), which has the potential to introduce fewer errors than analog processing.

Since all the signals to be processed are DC signals, time multiplexing can be applied so that only one ADC is needed, reducing the complexity of the circuitry and matching problems that appear when using multiple ADCs. The two main signal conversions will be:

$$\mu_1 = \frac{V_{load}}{V_{ref}} \tag{2.1}$$

$$\mu_2 = \frac{I_{load} \cdot R_{ref}}{V_{ref}} \tag{2.2}$$

where V_{ref} and R_{ref} are the ADC's reference voltage and the reference resistance, respectively. After converting these two signals to the digital domain, the load power can be obtained as:

$$P_{load} = \mu_1 \cdot \mu_2 \cdot \left(\frac{V_{ref}^2}{R_{ref}} \right) \tag{2.3}$$

which shows that P_{load} is digitized relative to an implicit power reference

defined by V_{ref} and R_{ref}. In the configuration presented in Figure 2.1, the input of the voltage-to-current converter can be controlled via a high-resolution DAC,[1] to correct for the errors present in the power readings.

One of the main advantages of the approach proposed in this work, is that the power dissipated in the load is actually measured, and since the voltage approach (see previous chapter) is used, the temperature and load power will be stable. When measuring the thermal conductivity to sense the CO_2 concentration in the air, one of the main approaches is to keep the power constant up to certain levels of stability which depends on the resolution needed for the CO_2 sensor; by measuring the power, there is no need of maintaining the power stable on the load,[2] which means that the scheme presented before can operate in an “open loop" configuration without controlling the load power (see Figure 2.2).

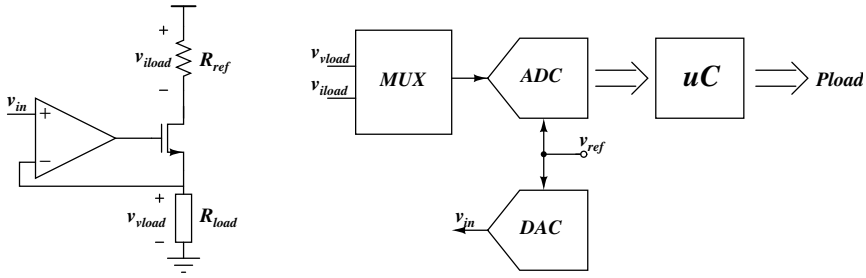


Figure 2.2: Block diagram to measure the load power (open loop configuration).

This scheme eliminates the need for a high-resolution DAC in the feedback loop, which was needed in order to maintain the load power stable; still, the fundamental limitations analyzed in the first chapter, such as the voltage and resistance reference, are still present.

2.2 Inclusion of BJTs: “The Digital construction of a Voltage Reference"

In order to find out the effect of the reference resistance and the reference voltage on the measurement readings of the CO_2 concentration, it is necessary to refer to Table 1.2 in Chapter 1 and Equation 2.3. From the equation, one can

[1] A DAC with the same order of resolution of the ADC is needed, to be able to control the power consumption at those levels of precision.

[2] The load power should be stable at least during the reading of the CO_2 concentration.

calculate the sensitivity of the load power measurement with respect to V_{ref} and R_{ref} as:

$$\Delta P_{Load} = \left|\frac{\partial P_{Load}}{\partial V_{ref}}\right| \cdot \Delta V_{ref} + \left|\frac{\partial P_{Load}}{\partial R_{ref}}\right| \cdot \Delta R_{ref} + \left|\frac{\partial P_{Load}}{\partial \mu_1}\right| \cdot \Delta \mu_1 + \left|\frac{\partial P_{Load}}{\partial \mu_2}\right| \cdot \Delta \mu_2 \tag{2.4}$$

Assuming that the conversion errors are negligible compared to the errors introduced by the reference resistance and voltage, it can be found that:

$$v_P = \frac{\Delta P_{Load}}{P_{Load}} \approx 2 \cdot \frac{\Delta V_{ref}}{V_{ref}} + \frac{\Delta R_{ref}}{R_{ref}} < 4\text{ppm} \tag{2.5}$$

If the same error budget is given for the two terms in the previous equation, then the reference resistance must have variations lower than 2ppm, while the variations for the reference voltage should be lower than 1ppm.

The previous analysis has different implications for both elements regarding their characteristics. In one hand, the resistance should have a temperature drift (or temperature coefficient) lower than 0.067ppm/°C,[3] while for the voltage reference, the noise level should be lower than 1ppm and its drift lower than 0.033ppm/°C.

Commercially, resistors with such a low temperature coefficient can be found [16], although they are quite expensive. When looking for integrated voltage references, it is hard to find one that is close to the mentioned characteristics; the best voltage references in the prior art have temperature coefficients ranging between 3-10ppm/°C [17],[4] while commercially, some circuits with lower temperature drift can be found [18], but still an order of magnitude above the needed specifications. Because of this, a new technique to construct and compensate a voltage reference will be introduced.

This precision voltage reference will be based on the bandgap principle. In order to create a bandgap voltage reference, p-n junction devices are needed. Commonly, two BJT transistors are used with different collector currents and/or emitter areas; by combining the resulting base-emitter voltages in the analog

[3] Taking into account the operational temperature range of the CO_2 sensor (10°C - 40°C).

[4] It must be noted that the operational temperatures of these voltage references are in the automotive, industrial and military ranges, which are much wider than the specifications of t his project.

domain, a temperature compensated voltage reference can be obtained [19].

In our implementation, by taking advantage of the fact that the voltages to be measured are time multiplexed, a single BJT is used and biased with two different collector currents[5] (one at a time) to produce the needed base-emitter voltages (see Figure 2.3). These voltages are individually digitized as:

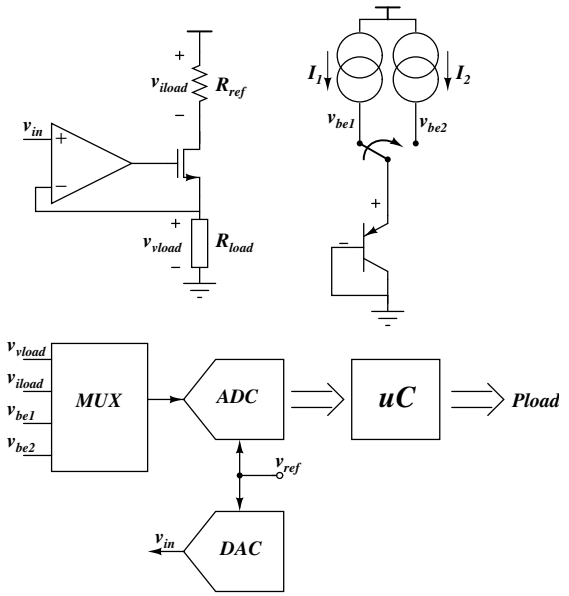


Figure 2.3: Block diagram.

$$\mu_3 = \frac{V_{be1}}{V_{ref}} \tag{2.6}$$

$$\mu_4 = \frac{V_{be2}}{V_{ref}} \tag{2.7}$$

where V_{be1} and V_{be2} are the base-emitter voltages when applying the collector currents I_1 and I_2, respectively. It should be mentioned that V_{ref} (the analog reference voltage) is not accurate, and it doesn't have to be accurate (just have a low-noise behaviour). After digitizing the base-emitter voltages, they are combined in the digital domain so as to obtain:

[5] In fact, the BJT is biased with emitter currents. The effect of this on the V_{be} will be analyzed later on this work.

$$V_{ref_{dig}} = (\alpha \cdot \mu_3 + \beta \cdot \mu_4) \cdot V_{ref} \tag{2.8}$$

This new voltage reference, can now be used to replace the analog voltage reference V_{ref} in (2.3):

$$P_{load} = \frac{\mu_1 \cdot \mu_2}{(\alpha \cdot \mu_3 + \beta \cdot \mu_4)^2} \cdot \frac{V^2_{ref_{dig}}}{R_{ref}} \tag{2.9}$$

thus, the measurement becomes independent of the ADC's analog reference voltage V_{ref}.

This approach has certain advantages over the conventional bandgap references, where the combination of the base-emitter voltages and the curvature compensation schemes are done in the analog domain, limiting their performance to the precision of the analog circuitry used. By digitizing the two main ingredients of a bandgap reference voltage, and combining the results in the digital domain, various sources of error, such as OpAmps, resistors and other analog components, are avoided. Furthermore, in the digital domain, the signals can be processed to compensate for the BJT non-idealities, either the ones that are product of the biasing (tollerance of collector currents, ratio between them, etc.), or the ones inherent to the transistor nature (saturation current, base emitter resistance, finite forward current gain, etc.).

A similar technique is implemented in [20], where a digital curvature compensation technique is used, based on a predefined lookup table. Still, two BJTs instead of one are used (introducing mismatch errors), and the digitized voltages correspond to PTAT (Proportional To Absolute Temperature, ΔV_{be}) and CTAT (Complementary To Absolute Temperature, V_{be}) voltages, which will require further analog circuitry to produce the former, increasing the error sources in the implementation. In any case, the results obtained in that work are up to the levels of 1.7ppm/°C temperature drift in the entire industrial temperature range, which gives an extra incentive when implementing the proposed technique in a more relaxed temperature range (10°C-40°C).

2.3 From the Constant Power Circuit to the CO_2 Sensor

2.3.1 Calculating the Thermal Conductivity

Up to now, the architecture has just focused on the measurement of the power dissipated in the load, but in order to obtain a complete CO_2 sensor based on the thermal conductivity approach, the temperature difference between the transducer and the ambient is also needed.

From equations 1.2, 1.4 and 1.5, the thermal conductivity can be expressed as:

$$\Theta = \left[\left(\frac{R_{load}}{R_o} - 1\right) - \alpha_R \cdot (T_{amb} - T_o)\right] \cdot \left(\frac{1}{\alpha_R \cdot P_{load}}\right) \tag{2.10}$$

With the topology presented, it is possible to obtain the remaining ingredients to measure the thermal conductivity. As mentioned, with the readings of the load voltage and current, the power dissipated in the transducer can be found, but also its impedance R_{load} can be determined as:

$$R_{Load} = \frac{\mu_1}{\mu_2} \cdot R_{ref} \tag{2.11}$$

Furthermore, with the inclusion of the base-emitter voltages, this architecture is capable of measuring the ambient temperature (the last component of Equation 2.10) as it will be described in the next section.

2.3.2 Temperature Measurement

A BJT-based temperature sensor can be constructed in the digital domain with the combination of the digitized base-emitter voltages. The difference of two V_{be}'s generates a PTAT voltage, which can be used to sense the ambient temperature. This difference can be expressed as:

$$\Delta V_{be} = V_{be1} - V_{be2} = \frac{kT}{q} \cdot \ln\left(\frac{I_1}{I_2}\right) = (\mu_3 - \mu_4) \cdot V_{ref} \tag{2.12}$$

if the previous equation is referred to the digital reference in Equation 2.8, the ambient temeprature can be obtained as:

$$T = \left[\frac{\mu_3 - \mu_4}{(\alpha \cdot \mu_3 + \beta \cdot \mu_4)}\right] \cdot \left[\frac{q}{k \cdot \ln(r_I) \cdot V_{ref_{dig}}}\right] \tag{2.13}$$

where k is the Boltzmann's constant, q is the electron charge and r_I is the ratio between the two collector currents (I_1 / I_2). It can be seen that this temperature measurement is still dependent on the accuracy of the ratio of the two collector currents, besides other non-idealities that will be studied in the next section. Nevertheless, in Chapter 3, analog and digital techniques will be studied in order to suppress some of these errors, so to obtain the desired accuracy in the temperature measurement, and hence, achieve the target accuracy for the CO_2 sensor.

Finally, it should be mentioned that the construction of both, the digital reference (Equation 2.8) and the digital temperature sensor (Equation 2.13), will be more complex than what was presented in this section, where a first order approximation was studied, giving an idea on how the system should work.

2.4 Accuracy Analysis

In this section, the top-level specifications will be estimated in order to design each of the required circuits, but first, the main error contributors must be recognized.

2.4.1 Dominant Error Sources

The following are the dominant error sources in the Analog Front-End of the CO_2 sensor architecture presented in Figure 2.3. Information on how these non-idealities have been modeled can be found in Appendix A.

ADC Non-Idealities:

- Quantization Noise (Resolution).
- Integral Non-Linearity (INL).

As will be explained later, when describing the output-referred thermal noise, the ADC's quantization noise should be such that is not dominant when comparing it to the circuit core's noise.

The INL is an important parameter because non-linearity (as opposed to offset and gain errors) introduces errors that depend on the levels of the voltage to be measured, and since different voltages will be measured with this configuration, the errors introduced in the readings due to this effect are of major concern.

Although these are the two main ADC non-idealities, other sources of error must also be taken into account. These include the Common-Mode Rejection Ratio (CMRR) which for this case plays an important role due to the different common-mode voltage levels that must be measured (mainly V_{vload} and V_{iload}, which are closer to ground and the supply voltage, respectively). The CMRR can be modeled as a change of the gain and offset of the ADC, which in principle can be modeled in the same way as the INL; this is the reason why is not included in the main list of errors.

The Power Supply Rejection Ratio (PSRR), the input capacitance and the sampling frequency must also be considered. The first one, should be in the same order as the CMRR; the second and third ones should have special considerations.

In the case of the sampling frequency, care must be taken to ensure sufficient settling in the analog front-end. The voltages to be measured should be able to settle during the sampling phase to have errors in the order of magnitude of the ADC resolution (even lower); the input capacitance is of course important, since it normally limits the bandwidth of the system.

Also, when sampling, the switched capacitor will load the output nodes of the analog front-end, and errors in the conversions can appear. The case in which this is more critical is when sensing the voltage and current of the load. When considering the ideal case without any resistance parasitics, if the switched capacitor is in parallel with the transducer, it wouldn't have any effect on the voltage measurement since the same voltage is applied to the device, dissipating the same power as without any additional load. Since this is not the case, and there always be some parasitics, the power dissipated in the tranducer when connecting the input impedance of the ADC to its terminals will change, introducing an error in the voltage measurement. A similar effect happens when sensing the voltage across the reference resistor (current measurement); in this case, the actual resitance will slightly change, affecting the reading.

Even though the previous errors are important for the selection of the high resolution ADC, they will not be including in the ADC's model, for simplicity,

when deriving an error budget for the circuit design. These error sources will be revised when selecting an appropiate ADC (see Chapter 4).

Reference Resistance (R_{ref}):

- Spread of R_{ref} at the reference temperature (R_{refo}).
- Temperature dependency of R_{ref} modeled by its 1st- and 2nd-order temperature coefficient (TCR1 and TCR2).

Although the analysis of the maximum permissible change in the value of the reference resistance was already presented, it must be remembered that the signal post processing will be performed in the digital domain, which means that, if one knowis with certain precision the temperature behavior of the reference resistance, a correction could be applied with the help of the temperature sensor, in order to compensate for the variations.

The latter implies that the errors that can be introduced in the measurements due to the reference resistance will come from the fabrication process variability[6] and long-term stability; this is why the nominal values of the resistance (R_{refo}) and its temperature coefficients (TCR1 and TCR2) will be evaluated, in order to find the maximum variations that the system can tolerate.

BJT Non-Idealities (Reference Voltage, Temperature sensor):

- Spread of the Forward Current Gain (β_f).
- Spread of Saturation Current (I_s).
- Non-Idealities of BJT Biasing (tolerance of collector currents, the ratio between them, etc).

In a similar way as for the reference resitance, based on the nominal values of the BJTs parameters, an analysis will be performed to find the maximum variations due to the fabrication process that can be tolerated.

The main parameters of the BJTs that will be evaluated in this section are the forward current gain, the saturation current, the collector currents, and the ratio between them. Other sources of error, such as the base resistance (r_b) and errors in the BJT biasing circuit (mismatch, OpAmp gain and offset, etc) should

[6] Actually, if individual calibration is performed, even process spread should not matter. Then, the main performace limiting factor will be the instability of the resistor's parameters.

be considered as well. A series of analog and algorithmic techniques will be implemented in order to mitigate these errors, so they will be assume negligible in this accuracy analysis. The mentioned techniques will be presented in Chapter 3.

Thermal Noise:

The final parameter to be considered is the thermal noise for each of the voltages to be digitized. To ensure that the ADC's noise contribution (consisting of quantization and thermal noise) is not dominant compared to these noise levels, a sufficiently high Effective Number of Bits (ENOB) should be chosen.

2.4.2 Top-Level Specifications

Now that the different sources of error have been listed, the set of specifications for the top-level design will be derived. In order to do this, a testbench was implemented and simulated in the *Cadence Design System*, a block diagram of which is shown in Figure 2.4.

Several things can be highlighted in Figure 2.4. First of all, instead of using a multiplexing technique with one ADC, for simplicity, four ADCs with the same characteristics. Also, an ideal OpAmp (voltage source controlled by voltage, with high gain) and transistor (voltage-controlled current source) were used; although the characteristics of these two elements have a great impact in the circuit design, the considerations to implement them have not been taken into account in this preliminary phase, but they will be considered in the next Chapter. It must be noted that the rest of the elements in the circuit were modeled with Verilog-A in order to control their parameters in an easier way (see Appendix A).

After defining the testbench, a parametric analysis was performed varying the already mentioned error sources and two environmental parameters: the CO_2 concentration and the temperature. In order to have an idea of the sensitivity of the CO_2 concentration reading to the different errors, as a first approach, only one error source was varied at a time, while the others were kept constants. The final result (the CO_2 concentration after digital post processing) is then sent to Matlab, where a calibration scheme is simulated to correct for the remaining errors.

The calibration procedure in Matlab is as follows (see Figure 2.5 as reference):

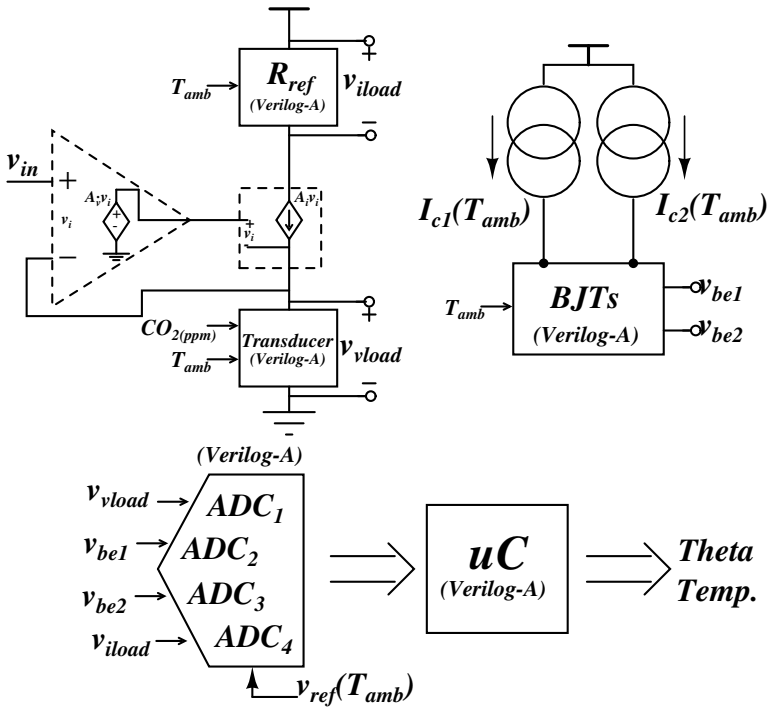


Figure 2.4: Top-Level Testbench.

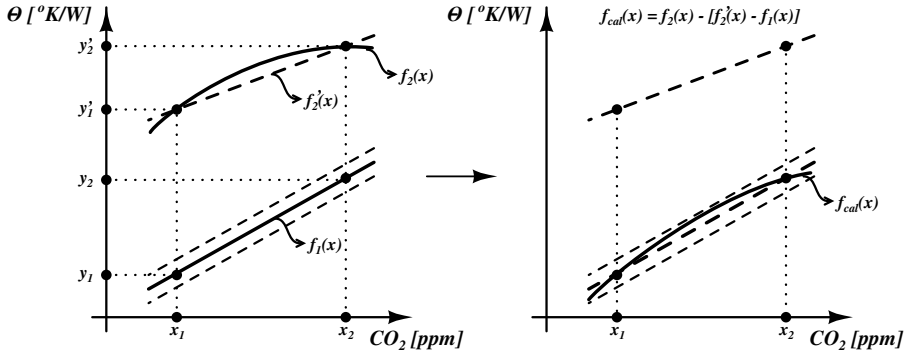


Figure 2.5: Calibration procedure (left: before, right: after calibration).

1. The output result from Cadence ($f_2(x)$ in the figure) is sent to Matlab where a linear polyfit in the CO_2 domain ($f_2'(x)$) is done:[7]

[7]For the polyfit, only two CO_2 levels are used (x_1 and x_2).

$$f_2'(x) = m_2 \cdot x + b_2 \tag{2.14}$$

2. Then, the ideal output of the CO_2 sensor ($f_1(x)$) is substracted from the obtained polyfit, to obtain a correction factor.

3. Finally, this correction factor is substracted from the actual output of the CO_2 sensor, obtaining the calibrated result:

$$f_{cal}(x) = f_2(x) - [f_2'(x) - f_1(x)] \tag{2.15}$$

It must be noted that at the two CO_2 levels taken for the polynomial fit, the error between the calibrated and the actual output is zero; also, it must be ensured that for the rest of the points, the deviation from the ideal case is within the maximum allowable error (see the dashed lines above and below $f_1(x)$) which determine the sensor's target accuracy ($\pm$50ppm).

This calibration model corresponds to a production calibration procedure in which every sensor is calibrated at two known CO_2 levels. Even though this procedure is performed, the latter is not enough to assure a correct reading from the sensor. A lot of other environmental factors, such as humidity and temperature, play an important role on the behavior of the device; then, if it is possible to correct for those cross-sensitivities, the final output would be almost independent on external parameters different from the CO_2 concentration in the air.

By exploting the fact that the proposed architecture provides temperature information, one could also calibrate for the temperature dependency of the CO_2 measurement as Figure 2.6 suggests, where the different colored lines indicate CO_2 readings at three different temperatures.

The calibration procedure when taking into account the temperature cross-sensitivity is as follows:

1. In Cadence, the simulations were carried on with three different temperatures. As with the calibration in the CO_2 domain, the results were sent to Matlab, where three different linear polyfit for each one of the temperatures are obtained:

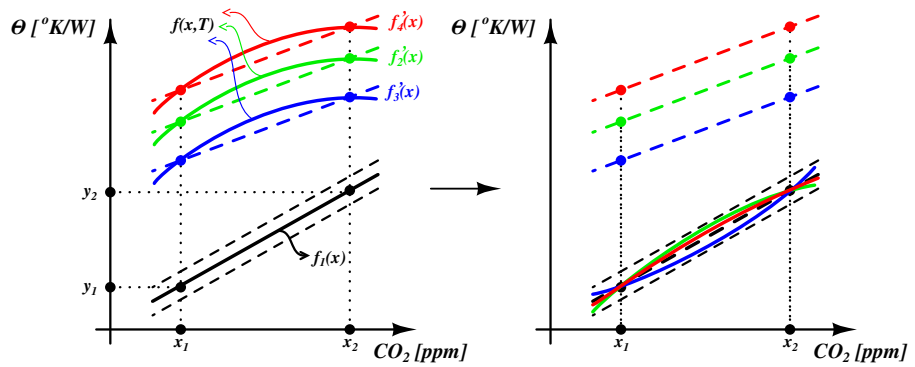


Figure 2.6: Calibration procedure including temperature cross-sensitivity (left: before, right: after calibration).

$$f_2'(x) = m_2 \cdot x + b_2 \tag{2.16}$$
$$f_3'(x) = m_3 \cdot x + b_3 \tag{2.17}$$
$$f_4'(x) = m_4 \cdot x + b_4 \tag{2.18}$$

2. From Figure 2.5 it can be seen that the slopes and the offset values for the linear functions $f_2'(x)$, $f_3'(x)$ and $f_4'(x)$ are temperature dependent. Then, one could also do a polyfit (quadratic polynomial) with these values in order to calibrate the temperature dependency of the offset and slope:

$$m(T) = a_2 \cdot T^2 + a_1 \cdot T + a_o \tag{2.19}$$
$$b(T) = c_2 \cdot T^2 + c_1 \cdot T + c_o \tag{2.20}$$

   Then, a linear function dependent on the temperature can be obtained as:

$$f_T(x) = m(T) \cdot x + b(T) \tag{2.21}$$

3. The ideal output of the CO_2 sensor ($f_1(x)$) is substracted from the obtained temperature dependent linear function,[8] to obtain the correction factor.

4. Finally, this correction factor is substracted from the actual output of the CO_2 sensor, obtaining the calibrated result:

[8] It is possible to interpolate the correction factor for any temperature due to the presence of the embedded temperature sensor.

$$f_{cal}(x) = f(x,T) - [f_T(x) - f_1(x)] \tag{2.22}$$

where $f(x,T)$ is the output of the sensor.

After applying this calibration procedure, the maximum value of each of the error sources is determined, that would be allowed if the entire error budget (100ppm CO_2 concentration) is allocated to that error source. This will give an idea on the relative importance each of the non-idealities present in the circuit, but it will not determine the final set of specifications, which will be more strict since the different error sources will add up.

Once the maximum error values are known, the documentation for the technology to be implemented in this work is consulted in order to see which are the maximum deviations of some of the design parameters (nominal resistance and tempco's, BJT saturation current, BJT forward current gain, etc);[9] other parameters such as the possible ADC resolution and INL, and the ratio accuracy between the collector currents were obtained from [21] and [22], respectively.

With this set of specifications, another parametric analysis is done by simulating a combination of all non-idealities to check if the selected error values can be calibrated with the mentioned procedure. This corresponds to a trial and error methodology to find a proper error budget.

A total of 512 possible error combinations have been tested; the calibration was performed as explained before. Table 2.1 summarizes the maximum error values (1st column) and the set of specifications for the top-level design (2nd column), while Figure 2.7 shows the sensor's output after the calibration in Matlab. In this figure the calibration effect can be observed at the two CO_2 level values where the error is zero (a butterfly shape appears). Also, almost all of the curves are within the $\pm$50ppm limits (black bold lines); just at the end of the CO_2 level range, segments of some curves are outside the boundaries.

Figure 2.8 illustrates a histogram with the number of samples within the error limits (90% of them passed, while the remaining 10% are close to the target). It should be mentioned that, for simplicity, the parametric analysis was performed by allocating the maximum error possible for each error source, and no statistical analysis was done. Therefore, the results are likely to be even better than what was obtained, leaving certain error margin for the circuit design.

It must be mentioned that the sensor's output is more sensitive to variations

[9] NXP provided all the relevant documentation for this analysis.

Specification	**V**alue	
P_{load} [mW]	1.0	
ADC Res. [bits]	21	
V_{ref} [V]	1.0	
	Max. Error	**Set of Specs**
INL (ppm)	950	**23**
R_{refo} (%)	$\pm$40	$\pm$**5**
TCR1 (%)	$\pm$50	$\pm$**20**
TCR2 (%)	$\pm$50	$\pm$**20**
BJTs I_c (%)	$\pm$50	$\pm$**5**
BJTs I_s (%)	$\pm$50	$\pm$**40**
β_f (%)	$\pm$50	$\pm$**40**
Ratio I_{c1}/I_{c2} (%)	$\pm$50	$\pm$**0.1**
Thermal Noise	1LSB	0.5LSB

Table 2.1: Set of Specifications for the Proposed architecture (100ppm change in CO2).

in the nominal reference resistor's parameters, and the selected values are considerably lower (mainly for the nominal resistance) than the ones given by the technology documents; some techniques will be discussed later in this work to compensate for this.

2.5 Summary

In this chapter the architecture implemented in this project was presented. It was explained in a detailed way, how from a power control topology, a CO_2 sensor readout circuit can be developed, even more, how is not necesary to fully control the power dissipated in the load. Furthermore, the problem of the reference voltage and reference resistance was explained and a possible solution to this issue, where a digital reference is constructed, was presented. Finally, an accuracy analysis was done, where some of the most important error

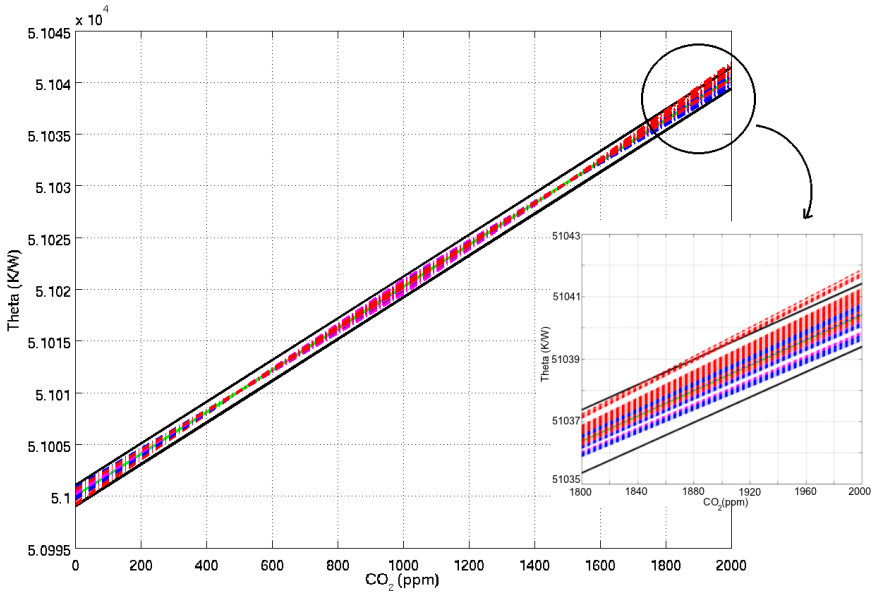


Figure 2.7: Parameteric analysis result (for the set of specifications) after calibration in Matlab. **Note:** The different colors in the figure respresent different temperatures (blue is 10°C, pink is 27°C and red is 40°C); the green curve represents the ideal case.

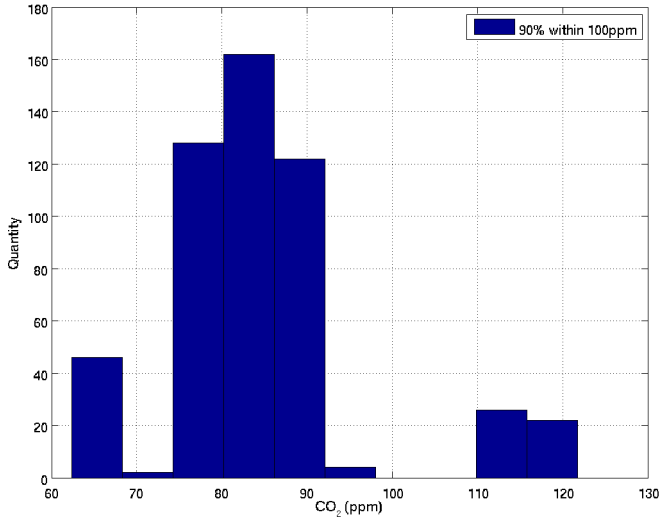


Figure 2.8: Histogram of the maximum error in terms of CO_2 concentration.

sources are included; for this analysis, verilog models were used, preliminary simulations were performed, and a calibration procedure were implemented, so to obtain a set of specifications for the final circuit design, which will be presented in the next chapter.

Chapter 3

Transistor-Level Design

This Chapter contains the considerations made for the transistor-level design of the CO_2 sensor architecture presented in Chapter 2. The set of specifications obtained in the accuracy analysis for the sensor's top-level, in section 2.4, will be translated to transistor level specifications in order to design the different building blocks present in the circuit. Also, circuit techniques (i.e, chopping, DEM, BJT biasing with β_f-compensation, etc) to mitigate some of the errors will be presented.

The chapter is divided according to the two main building blocks of the sensor. First, the different features needed for the correct functionality of the "Transducer Front-End", in charge of driving the CO_2 transducer, are described. The second section of this chapter explains the design of the "BJT Front-End", which provides the base-emitter voltages needed for the digital construction of a voltage reference and a temperature sensor; in this section, the biasing of the main BJT device is shown as well as the different techniques to correct for some of the errors present due to process variations, mismatch, etc. Finally, a summary of this chapter is presented.

3.1 Transducer Front-End

The first building block to be discussed is the "Transducer Front-End", the circuit that will drive the CO_2 transducer. As described in Chapter 2, the Transducer Front-End consists of a voltage-to-current converter and a reference resistor as illustrated in Figure 3.1.

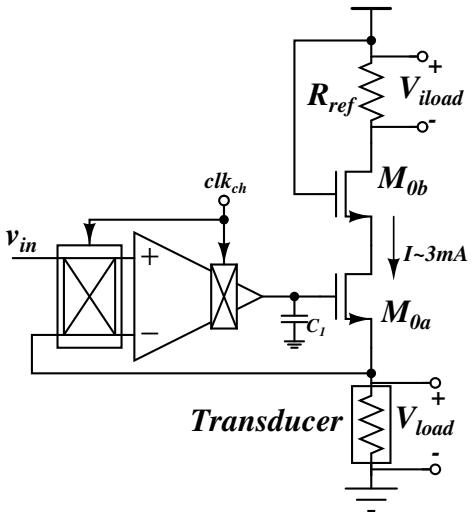


Figure 3.1: Transducer Front-End.

From the specifications shown in Table 2.1, this circuit must fulfil the following requirements:

- The circuit should be capable of driving sufficient current through the transducer: since the electrical resistance of the transducer is around 100Ω and the power dissipated is around 1mW, the current level that the transistors M_{0a} and M_{0b} should be able to handle is above 3mA.
- The total output integrated noise at the measurement points (transducer and reference resistance voltage drop) should be lower than half of the ADC's LSB.
- The variations of the reference resistance parameters should be the minimized: an extensive characterization of the different resistors can be found in the NXP documentation, where the parameters variation due to process can be seen; at the end, the resistor with the lowest temperature coefficients was chosen (N-Poly Resistor) since the variability in all the

resistor types was higher than what is needed for the design (see Table 2.1).

From Figure 3.1 one could think that only one driving transistor is enough, and the cascode configuration is not needed. In fact, when a worst-case simulation is performed with only M_{0a} and with the supply voltage above the nominal value (10% higher), current leakage can be seen due to Hot Carrier Injection (HCI) to the bulk of the transistor. The maximum allowable leakage current can be calculated as the current equivalent to half LSB error in the voltage measurement, or (taking into account the set of specification shown in Table 2.1):

$$I_{leak} \leq \frac{0.5 \cdot V_{LSB}}{R_{ref}} = 2.1\text{nA} \tag{3.1}$$

where V_{LSB} is the Least Significant Bit Voltage, and R_{ref} is the reference resistance (around 114Ω). To diminish the HCI effect, it was decided to implement another transistor as a cascode device (M_{0b}) which decreases the drain-source voltage of the main transistor, reducing effectively the leakage current.

For this design, a chopped OpAmp is preferred to reduce its noise contribution. The amplifier's precision requirements for this application are relaxed. Since it only serves as a tool to set the transducer's voltage, and since this is measured by a high resolution ADC, the accuracy is not an issue. This means that this OpAmp doesn't need high gain, gain stability or low voltage offset, but these specifications must be considered when designing the biasing for the BJT, where the same amplifier will be implemented;[1] this discussion will be reexamined in section 3.2.

Figure 3.2 shows the OpAmp's architecture, a PMOS folded-cascode; the PMOS input is necessary since the transducer's voltage is quite low (around 330mV), making impossible to use NMOS transistors. This topology was selected with the two applications in mind in which the OpAmp is going to be applied, since it gives high gain and high input common-mode voltage range (the input common-mode voltage in the BJT biasing circuit is higher than the one in the Transducer Front-End).

The pair of transistors M_1-M_2, M_9-M_{10} and M_3-M_4 are the devices that contribute the most to the noise of the OpAmp (mainly thermal noise, in that specific order); although the input pair noise is inevitable, the thermal noise

[1] Due to time constraints, it was decided to use the same OpAmp for both circuits.

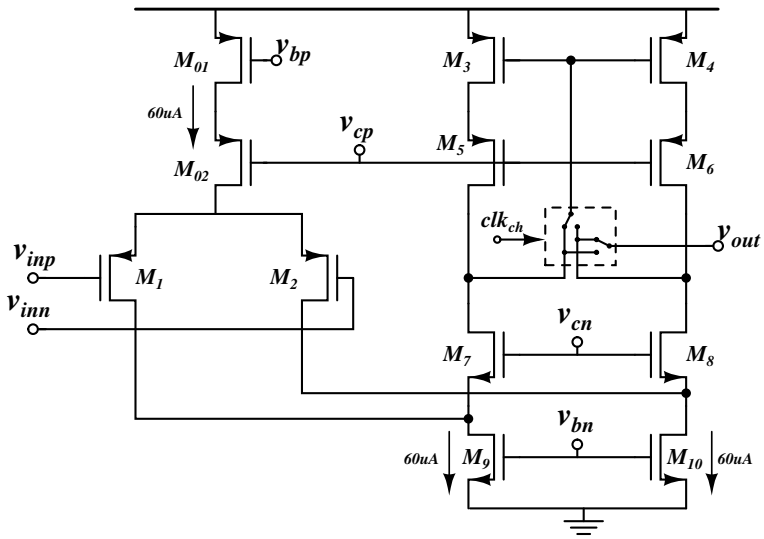


Figure 3.2: OpAmp Architecture.

coming from the other transistor pairs can be made less significant (compared to the input pair noise) by making their transconductances ($g_{m_{3,4}}$ and $g_{m_{9,10}}$) much lower than the input pair ones ($g_{m_{1,2}}$). Also, to reduce even more the flicker noise of the transistors, long channel and wider devices are preferred.

The capacitance C_1 (see Figure 3.1) is also used to reduce the output integrated noise. It must be remembered that the voltage and current of the transducer will be measured with an ADC, so sampling is needed; this sampling will have a folding effect on the noise (the noise bandwidth will fold into $f_s/2$, where f_s is the sampling frequency), which will result in "kT/C" noise [23]. Normally, the "kT/C" noise is dominated by the sampling capacitor, since it would contribute to the dominant pole of the system; in this architecture, the dominant pole is situated at the output of the OpAmp, so the total integrated noise depends on the value of C_1.[2]

The noise levels obtained for V_{load} and V_{iload} are around $37\mu V_{rms}$, which means that extra filtering is needed to achieve the desired resolution. The ADC can serve for this purpose (e.g., if a sigma-delta ADC is used) by averaging; the number of cycles calculated to reduce the noise levels to less than half an LSB is around 24300.

[2] If the closed-loop approach is implemented to control the power dissipated on the transducer, C_1 shouldn't be too high since it will determine the settling behavior of the system.

Table 3.1 shows the size of the devices presented in Figure 3.1 (including the OpAmp, Figure 3.2).

Device	Type	Width [μm]	Length [μm]	Multipliers	Value
M_{0a}/M_{0b}	NMOS	5.0	1.0	156	–
R_{ref}	resNpoly	20.0	0.304	77	114.3[Ω]
C_1	capNwellNpoly	74	74	1	50.5[pF]
OpAmp					
M_{01}	PMOS	5.0	5.0	12	–
M_{02}	PMOS	5.0	1.0	18	–
M_1/M_2	PMOS	5.0	1.0	160	–
M_3/M_4	PMOS	5.0	5.0	6	–
M_5/M_6	PMOS	5.0	1.0	40	–
M_7/M_8	NMOS	5.0	8.0	28	–
M_9/M_{10}	NMOS	3.12	1.0	12	–

Table 3.1: Devices' size of the Transducer Front-End.

To overcome the variation in the reference resistor's parameters, it is calibrated against an external device. As was mentioned in Chapter 2, commercial resistors with very low temperature coefficients (0.05ppm/°C) can be found; such a resistor will be used to calibrate the nominal resistance of the internal reference device at room temperature, and to correct for the variations in the temperature coefficients when testing the chip at different temperatures. The same approach can be implemented in the transducer case, where an external device is used to correct for process errors; the latter also gives the freedom to use the circuit with other transducer devices, for testing purposes.

Figure 3.3 shows the final Transducer Front-End architecture. In this illustration the main topology can be appreciated, as well as the addition of the external devices and an additional pair of transistors for calibration and testing purposes. The transistors are used as analog switches to alternate between the different devices,[3] so four different circuit configurations can be obtained from this scheme; the switches are controlled with two digital signals coming from an FPGA or microcontroller. It should be mentioned that the voltages in all of the resistors and transducers are sensed with Kelvin connections, although they are not shown in the figure (even for the external devices, the kelvin connections are wired to the chip, where they are multiplexed to be measured by the ADC).

[3]When a transistor is not selected, its gate is connected to ground.

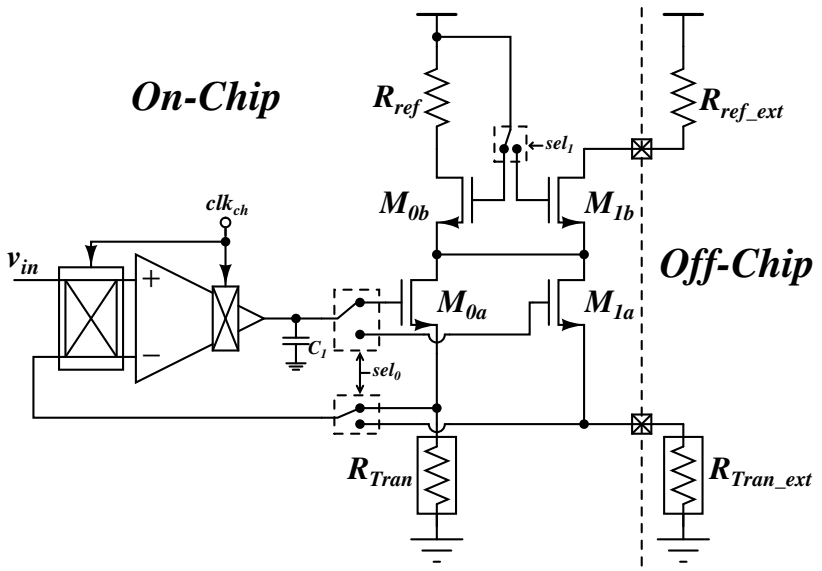


Figure 3.3: Final Transducer Front-End Architecture.

3.2 BJT Front-End

The "BJT Front-End" provides the base-emitter voltages which are used to construct the voltage reference and the temperature sensor in the digital domain, after they have been converted on the ADC. This circuit also provides bias currents with a proper temperature dependency to the main BJT device. Several circuit techniques to decrease error sources have been implemented.

According to the results obtained in section 2.4, the "BJT Front-End" should be able to:

- Deliver two base-emitter voltages with noise levels equals to one LSB of the ADC: for the base-emitter voltages, the error due to noise in the measurement can be as high as 1LSB, according to different top-level simulations.

- Provide the proper current levels to the main BJT device.

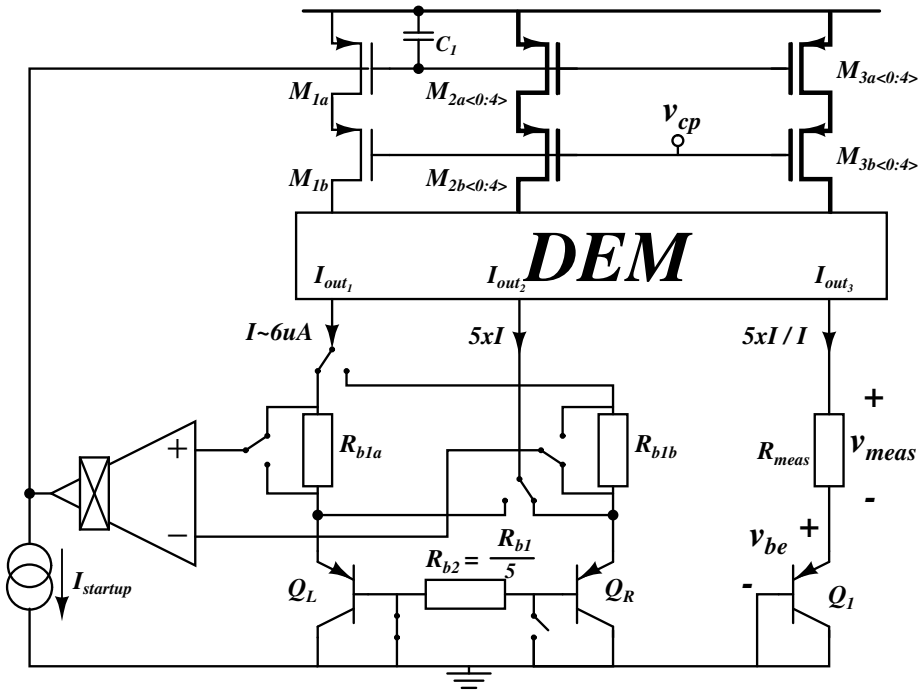


Figure 3.4: BJT Front-End.

3.2.1 Analog Domain

Figure 3.4 shows the BJT Front-End architecture. According to [24], a biasing current with a well known temperature dependency is needed to be able to predict, up to some extent, the behavior of the base-emitter voltage to be measured; it also helps to correct the inherent curvature that appears in the V_{be} voltages due to the temperature dependency of the saturation current I_s.[4] A biasing circuit architecture, which generates bias currents that are Proportional To Absolute Temperature (PTAT) [25], is then implemented.

The bias current generated by the circuit in Figure 3.4 can be found as:

$$I = \frac{V_{be_R} - V_{be_L}}{R_{b1}} \cdot \left(\frac{\beta_f + 1}{\beta_f}\right) = \frac{kT}{q} \cdot \ln(r_I) \cdot \left(\frac{\beta_f + 1}{\beta_f}\right) \tag{3.2}$$

[4] Applying a bias current proportional to T^m, with m close to η (a constant dependent on the BJT process), will reduce the curvature of V_{be} to negligible levels.

where $r_I = 5$ is the ratio between the collector currents.

In this equation, there is a term related to the forward current gain "β_f" of the bipolar transistor, which appears due to the presence of resistor R_{b2}, and is used to compensate for the β_f of the transistor Q_1[5] [25]. The principal reason to use this technique, is that the main BJT (Q_1) is biased by setting its emitter current, while the base-emitter voltage is dependent on the collector current, which is related to the former by the forward current gain as shown in Equation (3.3):

$$V_{be} = \frac{kT}{q} \cdot \ln\left(\frac{I_c}{I_s}\right) = \frac{kT}{q} \cdot \ln\left(\frac{I_e}{I_s} \cdot \frac{\beta_f}{\beta_f + 1}\right) \tag{3.3}$$

By substituting the current obtained in Equation (3.2) in this equation (as the emitter current), one obtains a V_{be} independent of β_f, and linearly dependent on the ambient temperature. The latter will not remove completely the β_f dependency, since its value is greatly related to the current applied to the BJT device (Figure 3.5).

In order to have the minimum variations in the value of β_f, currents in the flattest part of the curve are chosen. In contrast with [22], where a relatively low bias current density ($J = 3.6\text{nA}/\mu\text{m}^2$, which is equivalent to $I = 90\text{nA}$ per unit transistor) is used to save power, in this design, it was decided to implement a higher emitter density current ($J = 46.8\text{nA}/\mu\text{m}^2$, equivalent to $I = 1.2\mu\text{A}$ per unit transistor), in the flattest part of the curve. Moreover, this relatively high current is needed to ensure accurate settling when the sampling capacitor is connected to the output of the circuit.

A disadvantage of using this relatively high current density is the effect of the base and emitter resistances on the V_{be} voltage; with lower density currents, the errors due to these resistances are almost negligible. Later on this chapter, a method to diminish the base resistance effect on V_{be} will be discussed, which will give an extra incentive for the previous design choices.

Another feature of the architecture in Figure 3.4 is its capability of measuring the different bias currents through the BJT. In order to do that, an N-Poly resistor (R_{meas}) is placed in series with the emitter of Q_1; with the inclusion of this resistor, only two more voltages should be measured by the ADC in order to know the currents used to bias Q_1. This feature will allow to measure not only the currents, but also their ratio, two of the main error sources analyzed in Chapter 2, improving the results and giving the possibility of allocate more

[5] Q_1 is the device that provides the the base-emitter voltages to the input of the ADC.

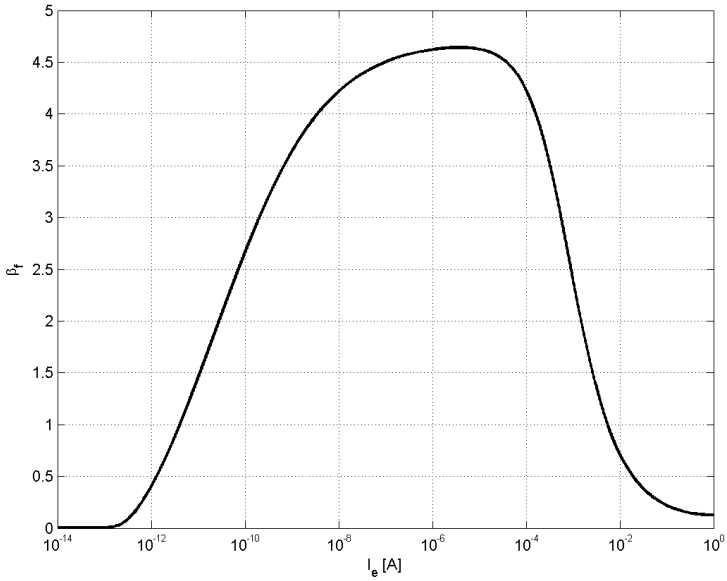


Figure 3.5: The forward current gain (at 25°C) of a substrate PNP transistor (5μm x 5μm) as a function of collector current in the 0.16μm CMOS process used.

of the error budget to other error sources.

As mentioned in section 3.1, the OpAmp shown in Figure 3.2, is reused in this bias architecture. This OpAmp should have low-offset voltage,[6] and high open-loop gain[7] to mitigate errors in the bias current [25]. To implement a low-offset amplifier, chopping is used; special care should be taken with the gain of this OpAmp when it is chopped, since the use of big cascode devices, generate a big capacitance at the output of the amplifier; the combination of chopping and the parasitic capacitance will create a load effect on the OpAmp, which could reduce the effective output impedance, hence, reducing the overall gain of the system. In this design, the open-loop gain is above 60dB in all corners.

Besides the chopped amplifier, this topology uses DEM (Dynamic Element Matching) techniques to reduce errors due to mismatch. In the core of the bias circuit, the two main branches are swapped, averaging any error due

[6]For the current ratio used in this designed, and a maximum inacuracy of 0.01K for the temperature sensor, the maximum offset voltage should be around 48μV [25].

[7]The open-loop gain of the circuit is not only dependent on the OpAmp's gain, but also on the common source PMOS transistor and the R_{bias} resistor.

to mismatch between the transistors Q_L and Q_R; at the same time this DEM serves to chop the input of the OpAmp. Furthermore, DEM is applied to all the PMOS current sources, in contrast with the scheme presented in [22], where DEM is only used in the current sources aimed to bias the devices that generate ΔV_{be} and V_{be} (here Q_1). Thus, higher accuracy in the current ratio can be achieved. Moreover, the switchable current sources needed for DEM will also be a useful tool to compensate for different non-idealities in the digital domain, as will be explained in the next subsection.

Device	Type	Width [μm]	Length [μm]	Multipliers	Value
$M_{1a}/M_{2a}/M_{3a}$	PMOS	6.0	5.0	1	–
$M_{1b}/M_{2b}/M_{3b}$	PMOS	6.0	1.0	4	–
R_{b1a}/R_{b1b}	resNpoly	20.0	0.304	1	8800[Ω]
R_{b2}	resNpoly	20.0	0.304	5	1760[Ω]
R_{meas}	resNpoly	20.0	0.304	2	4399[Ω]
C_1	capNwellNpoly	60	60	1	33[pF]

Table 3.2: Devices' size of the BJT Front-End.

The size of the devices presented in Figure 3.4 are shown in Table 3.2. The noise levels obtained in V_{be} is around $34\mu V_{rms}$ (worst case), while for V_{meas} the noise levels are around $36\mu V_{rm}$ (when the bias current is I) and $70\mu V_{rms}$ (when the bias current is $5I$). The number of cycles needed for the V_{be} to average out the noise to a level of one ADC's LSB is 5058; for V_{meas}, if a current ratio accuracy of 0.01% is wanted, 1082 cycles (single current source) and 162 cycles (five current sources) are needed.

3.2.2 DEM Scheme

Before going into detail in the digital compensation approach, the DEM scheme will be introduced. The block diagram of the DEM scheme is shown in Figure 3.6. The circuit consists of eleven 1-to-4 analog demultiplexers for each of the unit current sources, to allow the redirection of the current to any of four different paths: I_{out_1} and I_{out_2} correspond to the currents applied to the BJT bias circuit, I_{out_3} biases the main BJT, and I_{out_4} goes to a dummy BJT.[8] The

[8]When some of the current sources are not used in the BJT Front-End (for example, when Q_1 is biased with a single current source) they will be floating. When the swapping starts to take action, the transient from being floating to active can take some time; by using a dummy device, the effect of this transient becomes less significant.

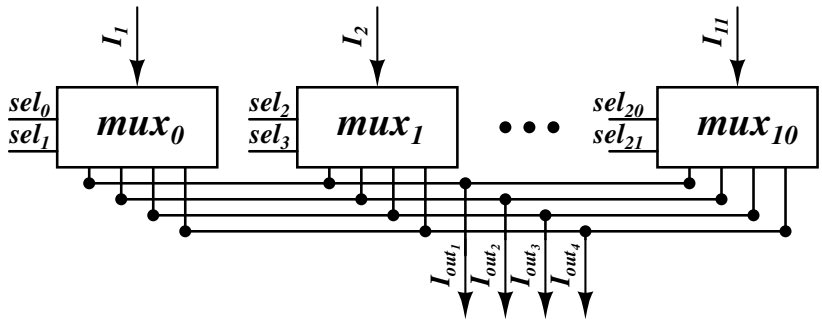


Figure 3.6: DEM circuit.

DEM will be carried out by applying control signals that will be updated at a rate equal to the chopping frequency or divisors of it.

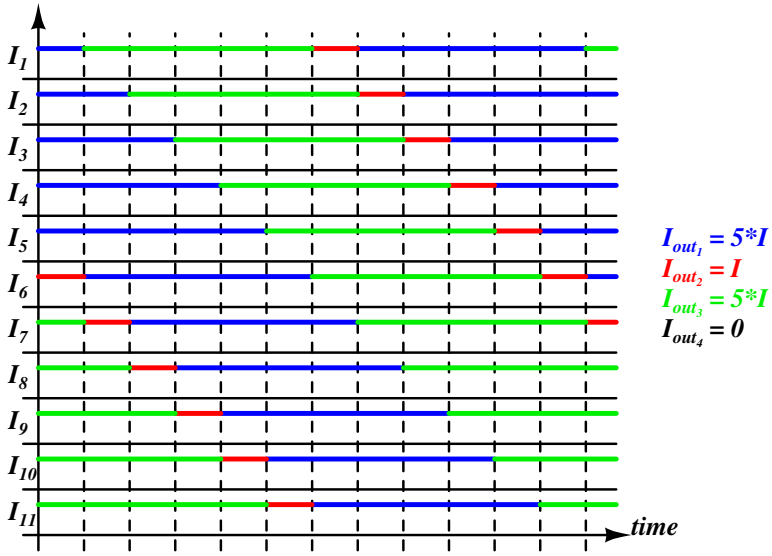


Figure 3.7: Current direction diagram, for the case where the main BJT is biased at $5 \cdot I$.

Figure 3.7, the diagram of the current sources direction over time is presented. Each dashed line indicates an update event of the demultiplexers' control signals. I_{out_1} should always be equal to $5{\cdot}I$, and $I_{out_2} = I$, while I_{out_3} can be varied from I to $5{\cdot}I$ (in Figure 3.7, $I_{out_3} = 5{\cdot}I$); the latter will provide the tools necessary to compensate for non-idealities (curvature correction due to the

temperature dependency of I_s, base resistance, current accuracy, accuracy of the current ratio, etc.) in the digital domain.

3.2.3 Non-Idealities of V_{be}

As mentioned before, the topology presented in this work will compensate for several non-idealities of the base-emitter voltage in the digital domain. This will allow the construction of a digital reference voltage, as well as a digital temperature sensor (which will be used for for temperature compensation) to the levels of accuracy described in Chapters 1 and 2.

Still, two main non-idealities haven't been adressed by the analog circuitry: the ones caused by the temperature dependency of the saturation current, and by the series resistance and base-width modulation. First, the temperature dependency of the saturation current will be reviewed to understand its effect in the base-emitter voltage. The saturation and collector currents can be written as [25], respectively:

$$I_s(T) = CT^{\eta}\exp\left(-\frac{qV_{g0}}{kT}\right) \tag{3.4}$$

$$I_c(T) = CT^{\eta}\exp\left(\frac{q(V_{be}(T) - V_{g0})}{kT}\right) \tag{3.5}$$

where V_{g0} is the extrapolated bandgap voltage at 0K, T is the ambient temperature, and C and η are constants. Then, the base-emitter voltage $V_{be}(T)$ can be expressed as:

$$V_{be}(T) = V_{g0}\left(1 - \frac{T}{T_o}\right) + \frac{T}{T_o}V_{be}(T_o) - \eta\frac{kT}{q}\ln\left(\frac{T}{T_o}\right) + \frac{kT}{q}\ln\left(\frac{I_c(T)}{I_c(T_o)}\right) \tag{3.6}$$

where $V_{be}(T_o)$ and $I_c(T_o)$ are the base-emitter voltage and collector current at a specified reference temperature T_o. Equation (3.6) can be rewritten as a taylor series taking as a reference point T_o:

$$V_{be}(T) = V_{be_o} + \lambda_1 \cdot T + \lambda_2 \cdot T^2 + \lambda_3 \cdot T^3 + \ldots \tag{3.7}$$

If $I_c(T)$ is assumed to be proportional to a power of T (for this design $m = 1$),

$$I_c(T) = I_c(T_o) \cdot \left(\frac{T}{T_o}\right)^m \tag{3.8}$$

then, the components of the taylor series (third order) presented in Equation (3.7) for $V_{be}(T)$ (Equation 3.6) are:

$$\begin{array}{rcl} V_{be_o} & = & V_{g0} + \frac{kT_o}{3q} \cdot (\eta - m) \\ \lambda_1 & = & \frac{V_{be}(T_o) - V_{g0}}{T_o} + \frac{k}{2q} \cdot (\eta - m) \\ \lambda_2 & = & -\frac{k}{qT_o} \cdot (\eta - m) \\ \lambda_3 & = & \frac{k}{6qT_o^2} \cdot (\eta - m) \end{array} \tag{3.9}$$

One can actually quantify the error (in Volts) of the V_{be}'s taylor series depending on the polynomial order. This is illustrated in Figure 3.8, where the error for the first four taylor polynomial orders against temperature is presented.

It must be remembered that this circuit gives the possibility of measuring the emitter current of the BJT, hence, there is no need to assume the collector current as a power of T in equation (3.6); the new components of the taylor series (third order) with the measured $I_c(T)$ are:

$$\begin{array}{rcl} V_{be_o} & = & V_{g0} + \frac{kT_o}{3q} \cdot \eta \\ \lambda_1 & = & \frac{V_{be}(T_o) - V_{g0}}{T_o} + \frac{k}{q} \cdot \left[\frac{\eta}{2} + \ln\left(\frac{I_c(T)}{I_c(T_o)}\right)\right] \\ \lambda_2 & = & -\frac{k}{qT_o} \cdot \eta \\ \lambda_3 & = & \frac{k}{6qT_o^2} \cdot \eta \end{array} \tag{3.10}$$

The main issue with this approach, is that the current measured by the circuit is not the collector current, but the emitter current; then, the current gain of the BJT must be included into the equation, and even more, the empirical model for its temperature dependency [25]:

$$\beta_f(T) = \beta_{fo} \cdot \left(\frac{T}{T_o}\right)^{X_{TB}} \tag{3.11}$$

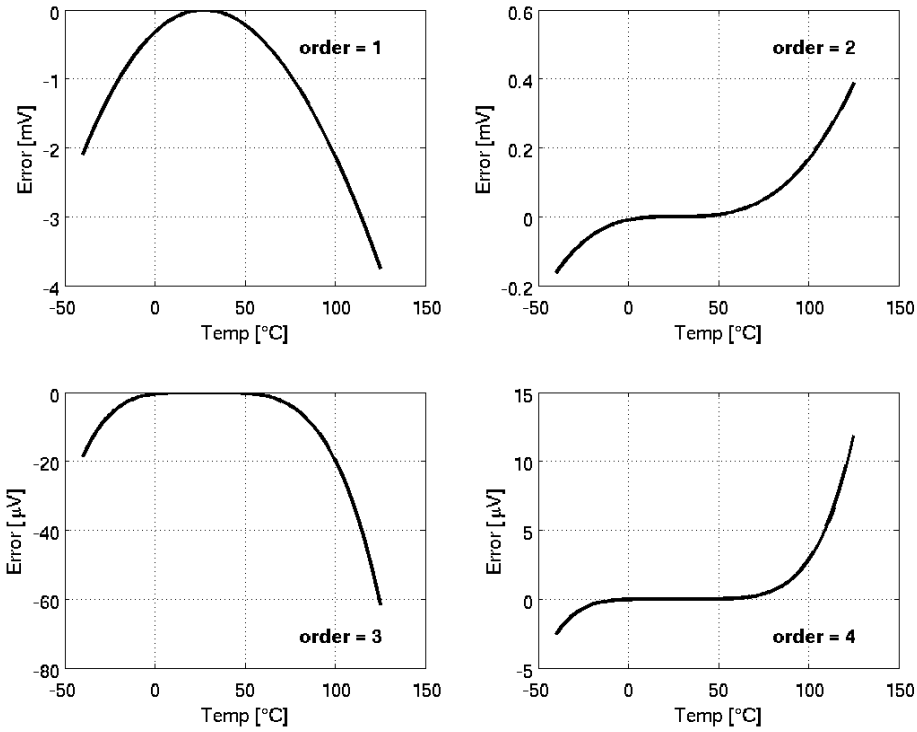


Figure 3.8: Error of the V_{be}'s taylor series vs Temperature ($T_o = 27°C$).

where β_{fo} and X_{TB} are found by fitting the equation to measured data, and can be obtained from the BJT spice model.

Now that the temperature dependency of the saturation current has been described, the effect of the series resistance and the base width modulation will be presented. The total base emitter voltage can be expressed as [25]:

$$V_{be} = \frac{kT}{q} \ln\left(\frac{I_c}{I_s}\right) + I_e \cdot R_s \tag{3.12}$$

where R_s is a resistance in series with the emitter. Here, the emitter resistance (R_e), the base resistances (R_b), as well as the base width modulation (forward Early effect) can be included (respectively) [25]:

$$R_s = R_e + \frac{R_b}{\beta_f + 1} + \frac{kT}{qV_{AF}}\left(\frac{\beta_f R_c}{\beta_f + 1} - \frac{R_b}{\beta_f + 1}\right) \tag{3.13}$$

where V_{AF} is the forward Early voltage.[9] It must be mentioned that the multiplicative error that appears with the reverse Early effect will not be taken into account for the temperature measurement, since it would be performed by a ratiometric operation, but for the construction of the digital reference, this effect should be included.

3.2.4 Digital Compensation of Non-Idealities of V_{be}

Now that the series resistance effect and the temperature dependency of the saturation current have been described, the base-emitter voltages of the main BJT can be written as the sum of three terms:

$$V_{be_n}(T) = V_{be_o} + [\lambda_{1n} + f(T)] \cdot T + I_{e_n} \cdot R_s \tag{3.14}$$

where V_{be_o} and λ_{1n} are the constant term and first order coefficient of the base-emitter voltage taylor series (respectively), $I_{e_n} \cdot R_s$ is the effect of the series resistance, and $f(T)$ is the higher-order temperature dependency term. The subscript 'n' identifies the corresponding V_{be} for a given bias current (e.g., V_{be_2} when it is applied $I_{e_2} = 2 \cdot I$).

From Equation (3.14), it can be seen that if three different base-emitter voltages are used in a System of Linear Equations (three linearly independent equations), it would be possible to create a temperature-dependent voltage, or a temperature-independent (reference) voltage. One could think that it would be better to have more base-emitter voltages to compensate for the higher-order termperature effect (since there is the possibility to have up to five different V_{be}'s), but these terms (represented by $f(T)$ in Equation 3.14) are the same for any base-emitter voltage, which would create more equations linearly dependent to the main three.

With the latter in mind, a linear combination of three different base-emitter voltages will be used to digitally construct the voltage reference needed for the conversions (suppossing that V_{be_1}, V_{be_3} and V_{be_5} are used):

[9] For the technology, $V_{AF} = 85$.

$$V_{ref_{dig}} = \alpha_1 \cdot V_{be_1} + \alpha_2 \cdot V_{be_3} + \alpha_3 \cdot V_{be_5} \tag{3.15}$$

and the corresponding System of Linear Equations is:

$$\begin{bmatrix} V_{be_o} & V_{be_o} & V_{be_o} \\ \lambda_{1_1} + f(T) & \lambda_{1_3} + f(T) & \lambda_{1_5} + f(T) \\ I_{e_1} & I_{e_3} & I_{e_5} \end{bmatrix} \cdot \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix} = \begin{bmatrix} V_{ref_{dig}} \\ 0 \\ 0 \end{bmatrix} \tag{3.16}$$

In the same way, the temperature can be obtained with a linear combination of three base-emitter voltages:

$$T_{dig} = \gamma_1 \cdot V_{be_1} + \gamma_2 \cdot V_{be_3} + \gamma_3 \cdot V_{be_5} \tag{3.17}$$

and the corresponding System of Linear Equations is:

$$\begin{bmatrix} V_{be_o} & V_{be_o} & V_{be_o} \\ \lambda_{1_1} + f(T) & \lambda_{1_3} + f(T) & \lambda_{1_5} + f(T) \\ I_{e_1} & I_{e_3} & I_{e_5} \end{bmatrix} \cdot \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \tag{3.18}$$

For the case of the digital temperature sensor construction, it might be more convenient to talk in terms of ΔV_{be}'s, as is commonly done (the results will be exactly the same). The $\Delta V_{be_{n_1-n_2}}$ voltage can be expressed as:

$$\Delta V_{be_{n_1-n_2}} = V_{be_{n_1}} - V_{be_{n_2}} = \frac{kT}{q} \ln\left(r_{I_{n_1-n_2}}\right) + \left(I_{e_{n_1}} - I_{e_{n_2}}\right) \cdot R_s \tag{3.19}$$

where $r_{I_{n_1-n_2}} = I_{e_{n1}} / I_{e_{n_2}}$. It can be seen then, that in order to obtain a temperature reading without the effect of the series resistance, a linear combinarion of two ΔV_{be} voltages are needed (or three V_{be} voltages, as in Equation 3.17):

$$T_{dig} = \rho_1 \cdot \Delta V_{be_{3-1}} + \rho_2 \cdot \Delta V_{be_{5-1}} = \rho_1 \cdot (V_{be_3} - V_{be_1}) + \rho_2 \cdot (V_{be_5} - V_{be_1}) \quad (3.20)$$

By comparing Equations (3.20) and (3.17), it can be found that $\gamma_2 = \rho_1$, $\gamma_3 = \rho_2$ and $\gamma_1 = -(\rho_1 + \rho_2)$. The System of Linear Equations for this case is simpler than in the previous case (Equation 3.18):

$$\begin{bmatrix} \frac{k}{q}\ln(r_{I_{3-1}}) & \frac{k}{q}\ln(r_{I_{5-1}}) \\ I_{e_3} - I_{e_1} & I_{e_5} - I_{e_1} \end{bmatrix} \cdot \begin{bmatrix} \rho_1 \\ \rho_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad (3.21)$$

To solve the proposed equations, four different approaches will be used. The difference between the approaches lies in the way the collector current ($I_c(T)$) and $f(T)$ are obtained:

Approach 1: The collector current is assumed to be:

$$I_c(T) = I_c(T_o) \cdot \left(\frac{T}{T_o}\right) \quad (3.22)$$

and $f(T) \cdot T$ is approximated to a truncated taylor series.

Approach 2: $I_c(T)$ is assumed as in Equation (3.22), but $f(T) \cdot T$ is not approximated.

Approach 3: $I_c(T)$ is obtained from measurements,[10] and $f(T) \cdot T$ is approximated with a taylor series.

Approach 4: $I_c(T)$ is obtained from measurements, and $f(T) \cdot T$ is not approximated.

From the latter, the different expressions for the terms in Equation (3.14), for each one of the four approaches, can be determined; these terms are presented in Table 3.3. In Chapter 4, the four approaches will be implemented to see which one of them gives the best performance.

Finally, and to complete the digital algorithm, an iteration process must be carried out. This is due to the presence of temperature dependent terms ($f(T)$)

[10] It must be remembered that the actual measurement is performed over the emitter current.

Term	Approach 1	Approach 3	Approach 2	Approach 4
V_{be_o}	$V_{g0} + \frac{k \cdot l_1}{q} \cdot T_o$			
λ_{1n}	$\frac{k \cdot l_2}{q} + \frac{V_{be_n}(T_o) - V_{g0}}{T_o}$			
$f(T)$	$\frac{k \cdot l_3}{q} \cdot \left[\frac{1}{6}\left(\frac{T}{T_o}\right) - 1\right] \cdot \left(\frac{T}{T_o}\right)$		$\frac{k \cdot l_3}{q} \cdot \left[1 - \ln\left(\frac{T}{T_o}\right) - \frac{T_o}{T}\right]$	
$l_1{}^*$	$\frac{\eta - 1}{3}$	$\frac{\eta}{3}$	$\eta - 1$	η
$l_2{}^*$	$\frac{\eta - 1}{2}$	$\frac{\eta}{2} + \ln\left(\frac{I_c(T)}{I_c(T_o)}\right)$	$-(\eta - 1)$	$-\eta + \ln\left(\frac{I_c(T)}{I_c(T_o)}\right)$
$l_3{}^*$	$\eta - 1$	η	$\eta - 1$	η

* *Multiplicity factors; they are different for each approach (l_1, l_2 and l_3 can be found in the expressions for V_{be_o}, λ_{1n} and $f(T)$, respectively).*

Table 3.3: Terms for Equation (3.14) according to each of the four Approaches.

in the Systems of Linear Equations presented before; since it is desired to obtain a reference voltage, the temperature is needed in order to correct the effects generated by $f(T)$, but the temperature reading depends on the digitally constructed reference voltage, so the problem must be solved by an iterative set of steps:

1. As a first step, the temperature is calculated using the analog reference instead of the digitally contructed one; for that, the System of Linear Equations presented in Equation (3.21) is used.

2. The next step is to use this temperature value to calculate the digital reference with Equation (3.16).

3. This new reference is then used to calculate the value of the temperature; a change of reference is performed, or what is equivalent, Equation (3.20) is divided by Equation (3.15).

4. Finally, steps 2 and 3 are repeated until the value of the digital reference is settled to a value with a sufficiently low error.

3.3 Summary

In this chapter the considerations made for the transistor-level design of the two main blocks needed for the CO_2 and temperature sensors have been described. The Transducer Front-End circuit was explained in detail, showing the different design choices, such as:

- Inclusion of a cascode transistor to mitigate the current leakage due to hot carrier injection effect.
- Selection of an OpAmp architecture with high-gain and enough input common-mode voltage range to be used in both Transducer and BJT Front-End.
- Selection of optimum ratios between the transconductances in the OpAmp's transistors to make their contribution to the output referred noise less significant.
- Use of chopping to further reduce the effect of flicker noise.
- Inclusion of an external reference resistance with low temperature drift for calibration purposes. For the latter an improved architecture of the Transducer Front-End has been shown.

In the case of the BJT Front-End, two main topics have been presented: the analog techniques implemented in the circuit, and all the things related to the digital domain.

Analog Domain:

- The architecture for the biasing of the BJT device have been shown. It was decided to implement a PTAT/R biasing circuit with β_f compensation.
- Selection of the BJT current density to mitigate the effect of the biasing on the forward current gain.
- Inclusion of a resistance in the emitter of the main BJT device, in order to measure the biasing current, which is used in the digital domain to compensate for non-idealities of the base-emitter voltage.
- Explanation on how the previously designed OpAmp is fully compatible with the biasing circuit.

Digital Domain:

- The DEM scheme is presented and explained. It shows how this circuit is capable of using five different currents to bias the main BJT device, with the inclusion of demultiplexers.
- The main non-idealities of the base-emitter voltage have been explained to fully understand how they can be reduced in the digital domain.
- Finally, the digital algorithm is described in detail, explaining the different methods implemented to reduce the non-idealities of the V_{be}s, so to be able to construct a digital reference as well as a digital temperature sensor.

Chapter 4

Measurement Results

IN order to see if the circuit proposed in this project is suited to sense the concentration of CO_2 in the air, a chip has been fabricated in a 0.16μm CMOS technology, and different measurements have been carried out to understand its different functionalities.

This chapter is divided as follows: first, the block diagram of the test is shown, in which all the components and test modes of the chip are described; then, the experimental setup used to measure the chip is explained, followed by the measurement results obtained and a comparison with prior work in constant power circuits. Finally, a summary of the chapter is presented.

4.1 Test Chip

The block diagram of the test chip is presented in Figure 4.1 (Figure 4.2 shows the chip layout where all the components are highlighted). The components inside the chip can be seen from this diagram: the two main analog blocks (the Transducer Front-End and the BJT Front-Ent), the circuitry from which the bias current of the analog blocks is obtained, the on-chip and off-chip transducers, as well as the off-chip reference resistor, two multiplexors, and two digital registers, one of 22-bits and the other of 6-bits.

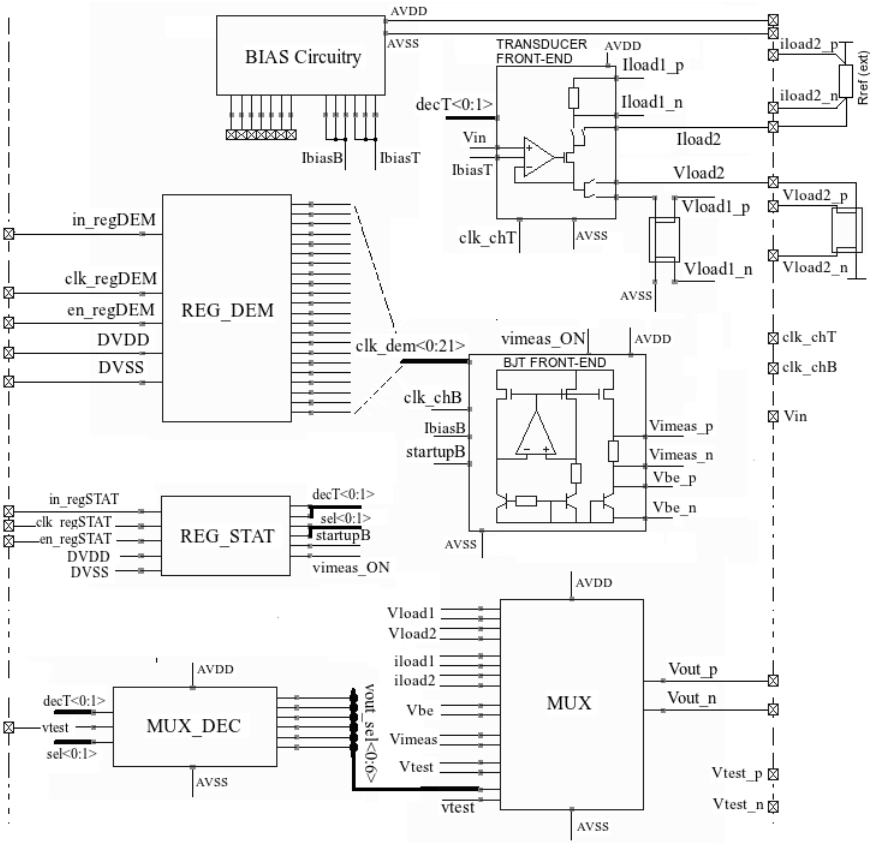


Figure 4.1: Block diagram of the test chip.

The Bias circuitry was taken from a previous design in the Electronic Instrumentation group [26], and it is aimed to deliver, in each branch, around 6uA.

The Transducer Front-End, as described in Chapter 3, has several test modes; in the block diagram of the test chip, the input and output pins of this circuit block are shown:

- *decT<0:1>:* a two bits control signal, that determines whether the circuit uses the on-chip transducer or resistor, or the off-chip ones.
- V_{in}*:* the input voltage to drive the transducer.
- *IbiasT:* the bias current for the OpAmp's bias circuitry.
- *clk_chT:* the chopper clock signal.

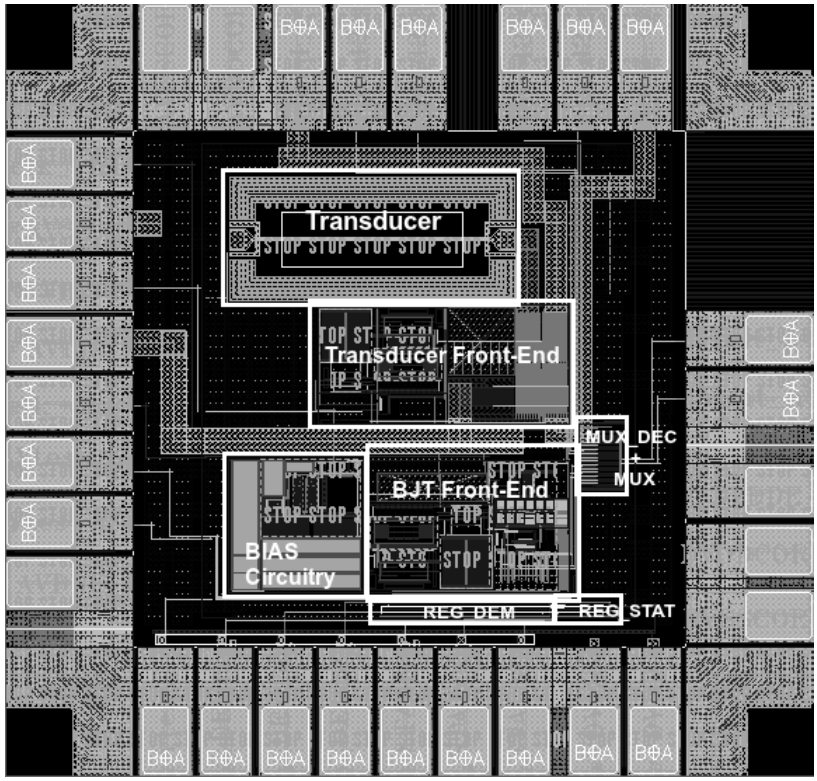


Figure 4.2: Layout of the test chip.

- I_{Load1_p},I_{Load1_n}*:* the two sense signals from the kelvin connections to the on-chip reference resistance. They go directly to the output mux.
- I_{Load_2}: the connection to the off-chip reference resistor.
- V_{Load_1}: the connection to the on-chip transducer.
- V_{Load_2}: the connection to the off-chip transducer.

As well, the input and output pins of the BJT Front-End are described as follows:

- *clk_dem<0:21>:* a 22-bit signal control for the eleven demux in charge of the DEM of the BJT biasing circuit.
- *clk_chT:* the chopper clock signal.

- *IbiasB:* the bias current for the OpAmp's bias circuitry, which is also used for the startup current.
- *startupB:* control bit to enable/disable the startup current for the BJT bias circuit.
- *vimeas_ON:* control bit to enable/disable the measurement of the emitter current through the main BJT.
- V_{imeas_p},V_{imeas_n}: sense signals for the current measurement.
- V_{be_p},V_{be_n}: sense signals for the base-emitter voltage measurement.

The digital registers are serial to parallel registers (consisting of flip-flops), each with its own clock and enable signal. The difference between them is the number of bits and the purpose they serve; the 22-bit register, or the "*REG_DEM*" in the block diagram is the register used to set the proper control values for the BJT Front-End DEM signals, and changes dynamically over time (during one measurement); the 6-bit register, or the "*STAT_REG*", is used to set those control signals that are static over time, like the *decT<0:1>*, *startupB*, *vimeas_ON* and *sel<0:1>* which are the two control bits to select the output voltage in the main MUX.

A differential test input (V_{test_p} and V_{test_n}) is included as well as a control bit *vtest*, that will override any other control signals, so when active, the output of the main MUX will always be the test input voltage. This voltage will be used to auto-calibrate for system-level offset errors, in an auto-zeroing configuration.

Finally, a micrograph of the test chip is shown in Figure 4.3. It has been fabricated in a 0.16μm CMOS technology, and has an area of 0.906mm^2, and is pacakged in a ceramic DIL package.

4.2 Experimental setup and PCBs

In orther to test the chip, a very complex experimental setup has been developed, for which two PCBs have been designed, and an FPGA test board is used to control, in an automatic way, every test mode on the chip and PCBs. The experimental setup is shown in Figure 4.4.

The main PCB (PCB_1 in the figure) is put inside a temperature chamber (Oven) in order to measure the different functionalities of the DUT (Device Under

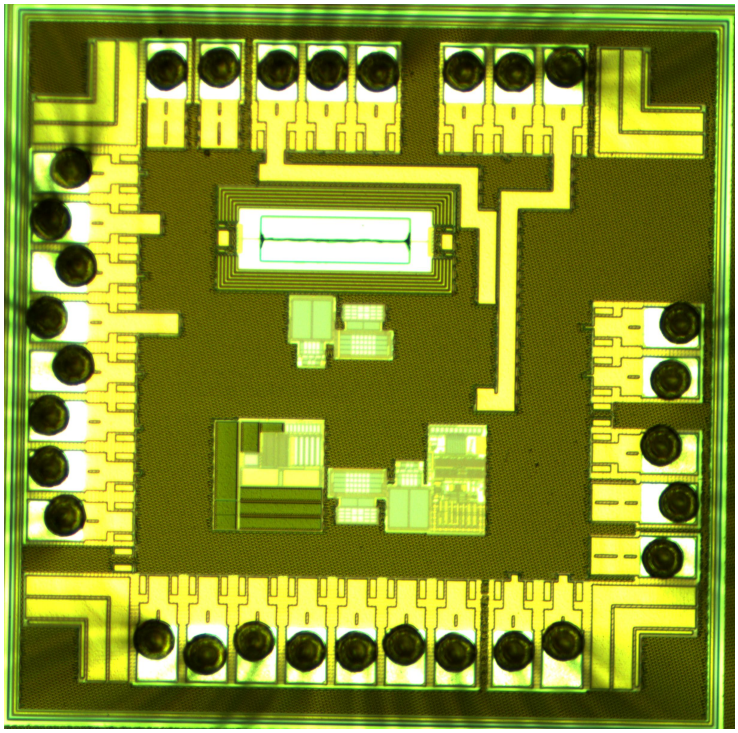


Figure 4.3: Micrograph of the test chip.

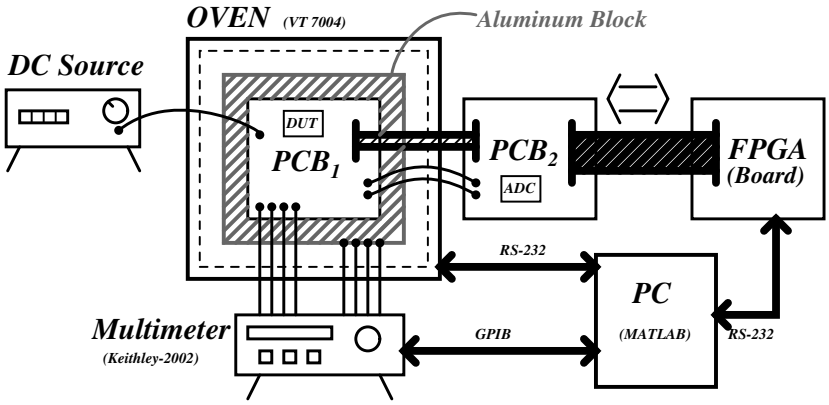


Figure 4.4: Experimental Setup.

Test, test chip) under different temperatures (from -40°C to 125°C). Since the spatial temperature variation of the oven is around ±2.0K, an aluminum

block is used to have a better temperature control; to measure the aluminum block's temperature, two PT100 RTDs are used and measured with a Keithley multimeter, which is also used to measure with a 4-wire connection different resistances included on the main PCB (external transducer). Also, an external DC source (with low noise) is used in order to set the input voltage for the Transducer Front-End inside the chip.

The main PCB receives the control signals generated in the FPGA through the ADC PCB, on which level shifters are includedto translate the logic levels of the FPGA to those of the DUT; the main PCB sends back through two coaxial cables (in a differential connection), the analog voltages obtained from the chip, so to digitized them with the ADC. The FPGA also controls all the functions of the ADC, including its master clock signal.

In order to control everything, and to post-process the measured signals, *MATLAB* has been used; RS-232 connections were used to control the oven and the FPGA[1], while a GPIB (General Purpose Interface Bus) was used to control the multimeter and receive the measured data. When all the data is retrieved in *MATLAB*, a script is used in which the methodology described in Chapter 3 is implemented to obtain the desired information from the measurements (temperature, transducer's power consumption and resistance, etc.).

4.2.1 Main PCB

The block diagram of the main PCB is shown in Figure 4.5; this PCB is where the test chip is included. It is connected to the ADC PCB via a 17x2 adapter, from which all the control signals for the test chip are sent, as well as other control signals for the other components on the PCB (i.e., three 1-bit signals to control off-chip multiplexers, as well as two signals to control an 8-bit DAC with an I2C protocol). On the PCB can be found:

- *Supply Voltage inputs (2):* Two inputs for the supply voltages, one positive and one negative ($\pm$6V).
- *Voltage Regulators (10):* to set the proper supply voltages, the two voltage inputs are regulated and distributed to the DUT and to different ICs included in the PCB. It should be mentioned that digital and analog grounds are derived from this voltage distribution.

[1]The FPGA program has different modes: temperature mode - where the BJT Front-End is measured, CO_2 mode - where the Transducer Front-End is measured, multimeter mode - where the external transducer is measured with the multimeter, etc. In order to set the proper mode, a master program is needed.

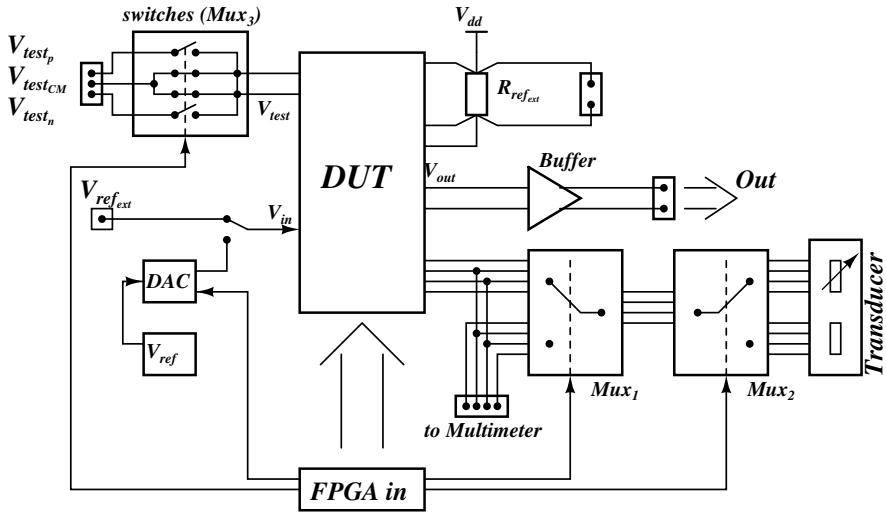


Figure 4.5: Block Diagram of the main PCB.

- *SMB connectors (12):* three are for the Common-Mode (1 connector) and Differential-Mode (2 connectors); one is to sense/set the input voltage that goes directly to the input pin of the Transducer Front-End; two are used to sense the voltage drop over the off-chip reference resistor; two are to sense the output voltage of the DUT (which is buffered); the last four connectors are used to measure the resistance of the off-chip transducer with a multimeter in a 4-Ω configuration.

- *A precision Reference + 8-bit DAC:* This configuration is used as an alternative to set the input voltage to the Transducer Front-End, by having a high precision reference [18] as the input of a DAC [27], to set different voltage values automatically. This concept can be also used in the closed-loop configuration explained in Chapter 2.

- *Reference Resistor:* This reference resistor has a precision of 0.05% and a temperature drift of 0.5ppm/°C over the military temperature range [16].

- *2-1 DEMUX (3) [28]:* The first one is used to multiplex between a CM voltage or differential one to the test input voltage that goes to the DUT, so it can be used as a system-level auto-zero configuration; the second demux is used to alternate between which device will measure the resistance of the off-chip transducer, either the DUT or the multimeter that will be connected to the PCB; the last one is used to multiplex between the two different off-chip transducer: the reference and the sense tranducer, in which the latter has higher sensitivity to CO_2 levels in the

air.

- *Buffer:* Zero-drift Opamps with high-gain and low-offset are used to buffer the differential output of the DUT [29]. It was decided to use buffers at the output of the test chip, in order to be able to connect different measurement devices (commercial ADC and multimeter) and not overload the circuits inside the DUT.
- *40-DIP sockets:* This 40-DIP socket is used to plug the set of off-chip transducers.
- *Jumpers:* Several jumpers are used for test-point purposes (i.e., to check that the regulators are delivering the proper current to the DUT), while others are used to manually set different test-modes of the PCB.

4.2.2 ADC PCB

It should be mentioned at this point, that the entire design of the CO_2 and temperature sensors was made thinking that the ADC to be used was the "Zoom-ADC" [21] which was developed in the Electronic Instrumentation group of TU Delft. Due to time constraints, it was not possible to use this ADC, since by itself it would need an entire characterization process. Instead, an external ADC with a very high-resolution (24-bit out of 5V reference voltage) is used [30], but of course, several issues are presented: the system is much slower than what was expected with the Zoom-ADC in order to achieve similar noise performance; the loading effect of the input impedance of the commercial ADC is quite different from the one of the Zoom-ADC, so a buffer is needed to mitigate this effect, which will add some gain and offset errors; due to the speed of the conversions, the temperature will vary considerably during a single measurement, reducing the accuracy and resolution that can be obtained from the configuration.

It was decided then, to use a second PCB completely dedicated to the external ADC. This PCB is located outside the oven, since the range of temperatures in which this IC could work properly was between -40°C-105°C, while the measurements were carried out up to 125°C. The PCB block diagram is shown in Figure 4.6. It serves also as a bridge between the control signals coming from the FPGA to the main PCB (where the signals are level-shifted from 3.3V to 1.8V), as well as for the postive and negative supply voltages. Also, on this PCB can be found:

- *Supply Voltage inputs (2):* Two inputs for the supply voltages, one positive

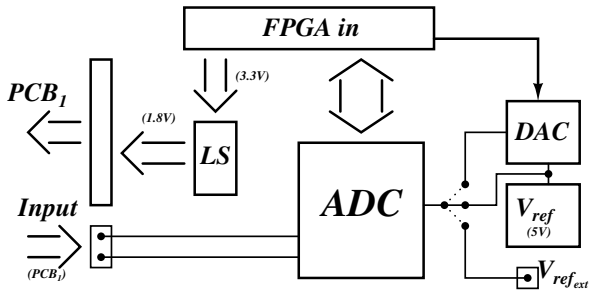


Figure 4.6: Block Diagram of the ADC PCB.

and one negative (±6V); the negative one, goes directly to the main PCB, since it doesn't play a role in this PCB.

- *Voltage Regulators (4):* to set the proper supply voltages, the positive voltage input is regulated and distributed to the different ICs included in the PCB. As well as with the main PCB, a digital and analog ground are derived from this distribution.

- *High-Precision Voltage Reference [18]:* This 5V precision bandgap voltage reference will set the reference for the ADC. Although the most important characteristic of the analog reference is very low-noise behavior, it was decided to include a reference that also is very precise and has low temperature drift, to be able to have more testability freedom. An 8-bit DAC is also added, to change automatically the reference, and see that the digital constructed reference is insensitive to these changes. The possibility of use an external reference voltage is also provided in the PCB, via a SMB connector (the different reference configurations can be seen in Figure 4.6).

- *16-bit Level-Shifter [31]:* This IC is used to voltage translate the control signals from the FPGA to the DUT, from 3V to 1.8V, which is the tolerable by the test chip.

- *24-bit ADC [30]:* a high-precision 24-bit analog-to-digital converter (ADCs) with an onboard, low-noise programmable gain amplifier (PGA), precision delta-sigma ADC and internal oscillator.

- *SMB connectors (4):* two of the connectors are for the voltage to be measured which comes from the main PCB; one is to set/measure the ADC reference voltage externally; the last one was put to accomodate the Zoom-ADC, so the FPGA can provide a sampling clock for this ADC.

4.2.3 Oven

In order to investigate the accuracy of the temperature sensor, and to test the Transducer Front-End over temperature variations, the main PCB is put inside the VT7004 Vötsch temperature test chamber, to be able to control the ambient temperature around the chip, with a spatial temperature variation of $\pm$2.0K inside the chamber. To have even better control over the temperature variation (around $\pm$0.01K), the chip is put in contact with an aluminum block, that filters the variations of the temperature, and stabilizes it to more accurate levels. To sense the temperature of the aluminum block, two PT100 RTDs are put inside the block; one of them is calibrated to detect changes in temeprature of around 0.005°K. The oven is finally controlled with MATLAB via an RS-232 connection, by sending the proper commands described in the user manual.

4.2.4 Multimeter

The multimeter used in the measurements was a Keithley-2002 multimeter. This multimeter was controlled with MATLAB via a GPIB interface, and it was used for several purposes:

- Measure the PT100's resistances with a 4-wire configuration (one at a time, by time multiplexing).
- Measure the external transducer's resistance with a 4-wire configuration.
- Measure the voltage drop across the external transducer.

In order to obtain measurements with the proper noise levels, the multimeter was set with the highest resolution possible (8.5 digits), as well with a Number of Power Cycles (NPLC) equal to 10; the NPLC indicates how long an input signal is integrated to obtain a single measurement. Noise introduced from the power line tends to be periodic. If the A/D converter integrates for an amount of time equal to one cycle of the power line noise, then the signal components from the periodic noise can be canceled. Generally speaking, the longer a signal is integrated by the A/D converter, the more accurate the reading result, but the counterpart is that the reading will be slow; for example, For 50Hz power and 10 NPLC, a new value can be reported no faster than at 200 msec intervals.

Since the NPLC mainly reduces the noise coming from the power line, still the noise coming from the circuit itself must be reduced. For that, a digital

filter is applied within the multimeter's functions; the digital filter consists off averaging a specific number of contiguous measurements, which is set by the user. While this will increase the time that a single measurement takes, it would increase the resolution of the readings.[2]

4.2.5 Emulation of the Off-Chip Transducer

In order to characterize the chip in combination with a thermal-conductivity-based CO_2 sensor, a climate chamber in which the CO_2 levels in the air can be controlled is needed. Since all the measurements were carried out in a temperature test chamber, where the only parameter that can be controlled is temperature, another method to investigate the performance of the circuit was implemented.

It was decided to develop another PCB that could be plugged in the DIP-40 socket, with only two components in it: a high-precision, low temperature drift reference resistance (as the one included on the main PCB), and a PT100 RTD, both with 4-wire connections; the PT100 is actually one of the PT100 used to measured the temperature, so it is embedded in the aluminum block.

The idea with this configuration is to measure the voltage and the current through a device with a well known temperature behavior (PT100), and to see how well the read-out circuit behaves over temperature. The reference resistance is used in this case for calibration purposes. The measurements will be carried by the DUT, and from them, the resistance and the power dissipated on the devices can be obtained. Since the resistance and the voltage of the devices will be also measured with the multimeter, the measurements performed by the chip can be compared in an accurate way, and the actual performance of the Transducer Front-End can be determined (it should be remembered that the performance of the read-out circuit of the CO_2 transducer, depends on the accuracy of the voltage and current measurements).

With the latter in mind, the measurement results of the transducer's resistance and power dissipation will be presented by comparing the values obtained from the chip with the values obtained with the multimeter; furthermore, a transducer-like behavior will be emulated with a PT100, to see how good the read-out circuit is over temperature variations.

[2]Since the measurements take so long, the temperature varies more than expected, which introduces errors in the measurements; in order to see how much are these errors, the temperature is measured before and after every measurement.

4.3 Measurement Results

In this section, all the measurements performed with the chip are presented. Due to time constraints, only one sample of the chip has been measured. The measurements were carried out in the military temperature range, and at each temperature point, ten repetitions of the set of readings was performed.

The measurements at a temperature point start when the PT100 temperature reading stabilizes to errors in temperature lower than 0.005°C. The set of readings includes (from the first to the last):

1. Temperature reading ($PT100_1$).
2. BJT Front-End voltages (an offset measurement with the system-level auto-zeroing,[3] and all five V_{be}s and I_es).
3. Temperature reading ($PT100_2$).
4. Transducer's Front-End voltages (offset measurement, load voltages and currents).
5. Temperature reading ($PT100_3$).
6. Multimeter readings (Voltage and resistance measurements of the PT100 used as load).
7. Temperature reading ($PT100_4$).
6. Multimeter readings (Voltage and resistance measurements of the high-precision resistor used as load).
9. Temperature reading ($PT100_5$).

4.3.1 Temperature Sensor and Voltage Reference Measurements

The temperature readings obtained from the digital algorithm explained in Section 3.2.4, as well as the values of the digitally-constructed reference voltage are presented in this section.

[3]Since this offset measurement is performed with the use of off-chip devices, the actual path of the readings is not the same when using this approach, and it is possible that extra errors could be added; this is why this measurement readings were not used in the final measurements.

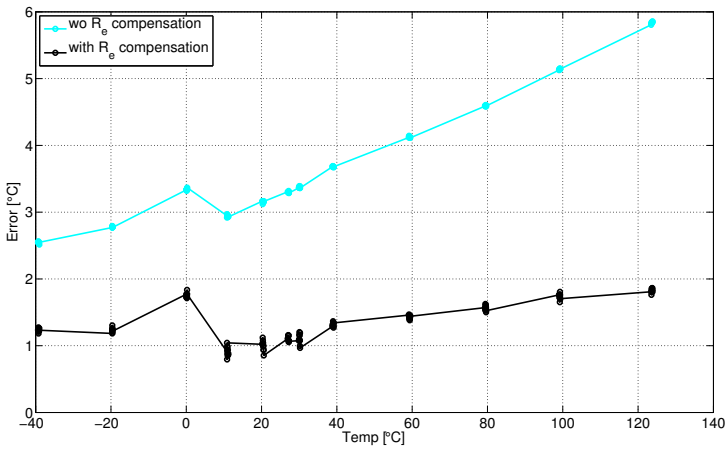


Figure 4.7: Temperature readings obtained with the external analog reference (blue: without emitter resistance correction, black: with emitter resistance correction).

Figure 4.7 shows the temperature readings obtained by digitizing the different ΔV_{be}s relative to the external voltage reference of the ADC; in other words, the digitally-constructed reference voltage was not used here to obtain these results. Two curves can be seen in this figure: the blue line corresponds to the case in which the effect of the series resistance has not been compensated, while the black line shows the result when implementing the method to mitigate this error described in Section 3.2.4. It is interesting to see how big this effect can be at these levels of current density, in contrast with [22]. The error corresponds to a series resistance of about 13Ω, which is in line with expectations.

Now, the construction of the digital reference is done in order to obtain self-referenced temperature readings. Four different digital references were constructed after applying the four approaches explained in Section 3.2.4. The results are shown in Figure 4.8.

It can be noticed that the digitally-constructed references are very temperature dependent. This is due to the difference between the simulated base-emitter voltages and emitter currents values, and the actual ones. As with any bandgap reference, calibration and correction are needed, as will be explained below.

Another interesting effect occurs with approaches number three and four; it must be remembered that for these cases, the collector current is not assume, but is obtained from measurements.This is due to an odd behavior of the current measurements at higher temperatures, which can be appreciated in the

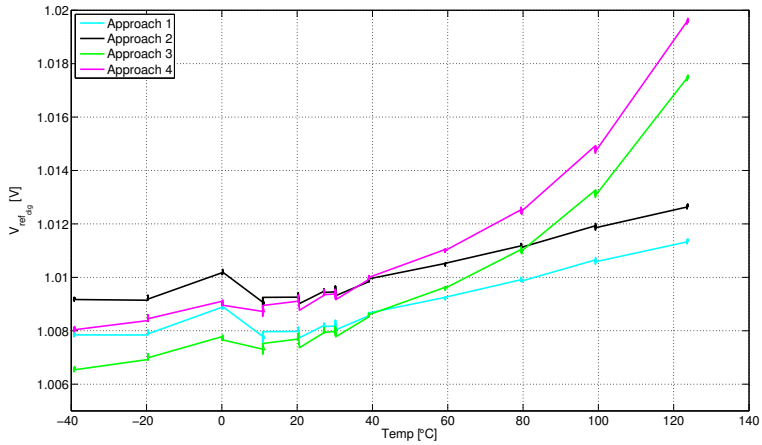


Figure 4.8: Digitally-constructed reference (with four approaches; see Section 3.2.4).

current ratio measurements in Figure 4.9.

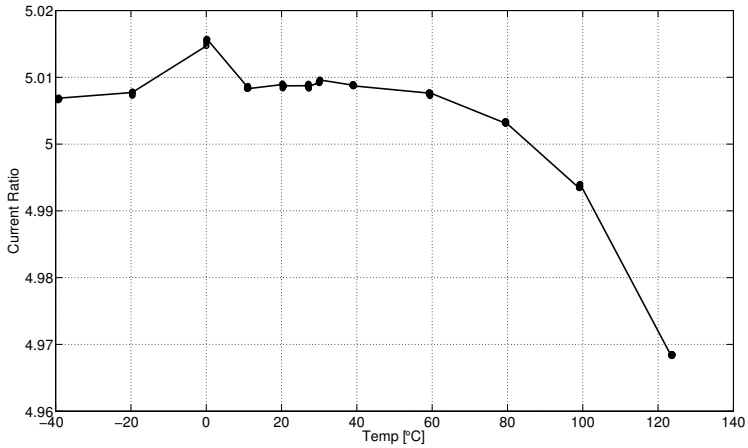


Figure 4.9: Current ratio measurements (ratio = 5).

A very accurate current ratio was expected since DEM was used, but at high temperature, the errors are close to 1% of the designed current ratio. Due to time constraints, this effect could not be further investigated, so it was decided to use the first two approaches as references for the following measurements.

Also, it should be noticed that at 0°C, a strange “jump" occurs in all the measurements performed. This may be ascribed to moisture in the oven around this temperature, which would lead to erronous readings.

In order to mitigate the temperature behavior of the reference voltages, a 1-point calibration is performed at 27°C and a correction is made in the $V_{be}s$ and I_es, where the measured values are used to construct the references.[4] Figure 4.10 shows the values of the references (approaches 1 and 2), thus obtained, after the correction is applied.

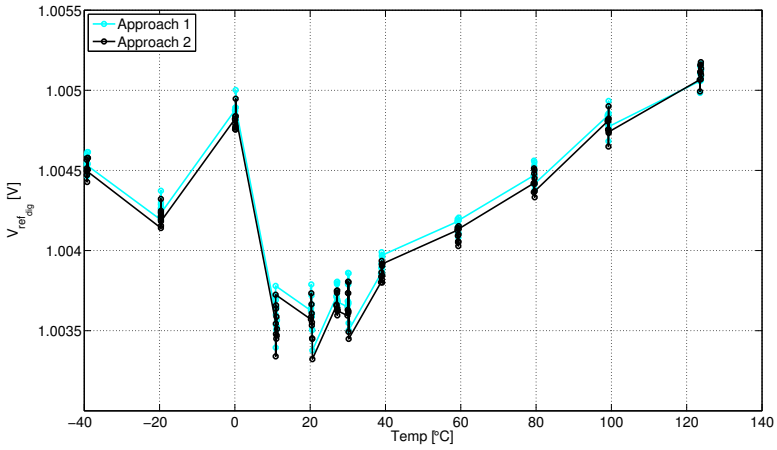


Figure 4.10: Digitally-constructed reference (after correction at 27°C).

Still, some higher-order temperature effects can be seen in the curves, which may be explained due to the deviation between the model and real values of the extrapolated bandgap voltage at 0K (V_{g0}), and the η constant. More than one point calibration can be made in order to obtained the necessary data and correct for these errors in the algorithm, but this has not been done in this work.

Still, a very good voltage reference is obtained, with a temperature coefficient of around 9ppm/°C in the military temperature range, which is in accordance with what it can be found in the state of the art as discussed in Chapter 2. Furthermore, the voltage reference is more stable around the CO_2 sensor target temperature (10°C-40°C), but it is also where the repeatability of the measurement is worse. This may be due to the fact that the region of temperatures close to 27°C, is where the oven has more difficulties to stabilize the chamber temperature, and its switching effect (ON/OFF) is more noticeable.

The temperature readings obtained by digitizing the ΔV_{be}s relative to the corrected digitally-constructed reference (for both approaches) are shown in

[4] Due to the odd behavior of the current ratio, approaches three and four will no be longer considered; furthermore, the current ratio for the first two approaches was taken from measurements only at 27°C, and it is not obtained for every temperature.

Figure 4.11. Here the peak at 0°C is more noticeable than in the previous measurements. Except for this outlier, errors below ±0.2°C are obtained, with a resolution of 0.15°C. In the CO_2 temperature range, accuracies of ±0.1°C are seen, with the same resolution as before.

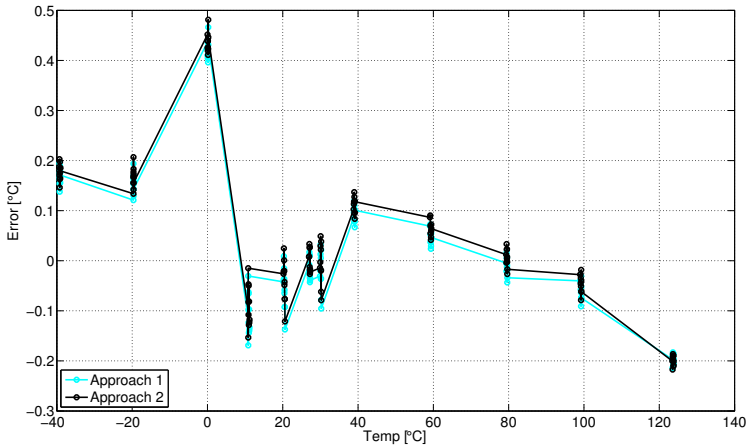


Figure 4.11: Temperature readings obtained with the corrected digitally-constructed reference voltage.

Besides the switching behavior of the oven at temperatures near 27°C, at other temperatures it can be noticed that the repeatibility of the readings is somehow compromised. This could be due to two reasons: first, temperature drift in the chip during an entire temperature measurement, which was calculated by measuring the temperature with the calibrated PT100 before ($PT100_1$) and after ($PT100_2$) a single temperature reading performed by the chip (see Figure 4.12). Although the temperature deviation is less than ±0.005°C, this difference could be translated to even greater errors in the temperature measurements; it must be remembered that V_{be} voltages and I_e currents are combined linearly in a digital algorithm, so if they are taken at different temperatures, even if the deviation is small, it could represent a bigger error in the temperature readings. The second reason is a consequence of an attempt to mitigate the previous one; in order to have lower temperature drift during a single temperature measurement, the conversion time of the ADC was modified to have faster measurements when the BJT Front-End was connected to the output, so the ADC performs less averaging, and more noise is present in the final conversion.

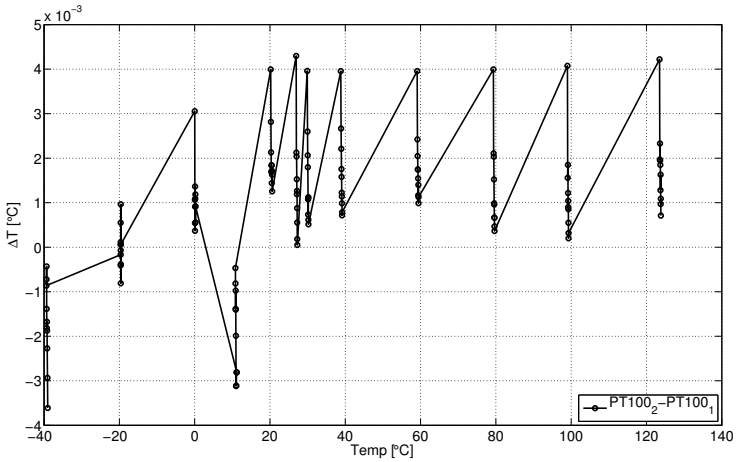


Figure 4.12: Aluminum block temperature deviation during a temperature reading performed by the DUT (i.e., difference between the temperature measured with the calibrated PT100 before and after the reading of the DUT).

4.3.2 Resistance Measurements

In this section, the measurements of the voltage and current of the external transducer (emulated with a PT100), are combined in order to obtained the load resistance.

Figure 4.13, shows the behavior of the PT100 over temperature, when measured with the multimeter; this will be used as reference when obtaining the PT100 readings with the DUT. The value of the PT100 resistance at room temperature is around 110Ω, and varies between -23% and 35% of the room temperature value.

The main idea of the resistance and power measurements is to be able to use the on-chip reference resistance to make the readings. In order to do so, temperature calibration should be made to correct for the nominal on-chip resistance value (1-point calibration), and its temperature coefficient (2-point calibration). In the algorithm, one can use the values used in the simulation models, but previous measurements on this kind of resistances (resNpolyProt) were performed by NXP, and differences between the mean and the standard deviation for the first-order temperature coefficient of around 400% were found. This is why this method was not implemented, and only the nominal resistance value is used in a first instance.

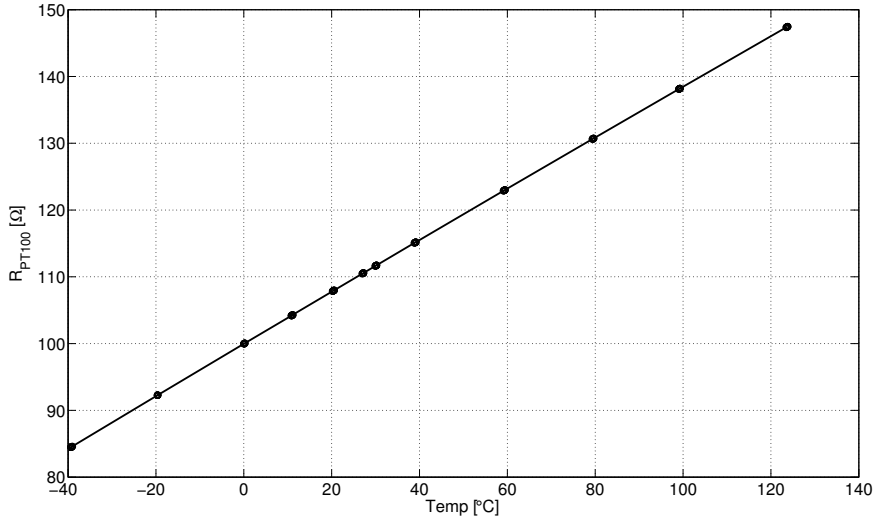


Figure 4.13: PT100 resistance vs Temperature (measured with the multimeter).

Two procedures are implemented for calibration over temperature; the first one involves only measurements with the DUT, using the high-precision resistors as reference to measure the current and as the load; the second one is by comparing the resistance measured by the DUT with the multimeter readings.

Calibration against precision resistors:

The calibration against an off-chip precision resistor is performed as folloes (see Figure 4.14 for reference):

- The DUT is used in three modes: 1) one of the precision resistors is used as the Transducer Front-End load, and the load current is measured with the off-chip reference resistor (blue curve); 2) the precision reference is kept as the load, and the on-chip resistor is used to measure the load current (pink curve); 3) the PT100 (uncalibrated one) is connected as the load and the on-chip resistor is used to measure the load current (black curve).
- Depending on how many temperatures are taken for calibration (1-point or 2-point calibration), a factor correction or a linear correction can be implemented. In the first case, the measured resistance with the first mode (blue line) is compared with the measured resistance with the second mode (pink line) at room temperature, and a correction factor is obtained as:

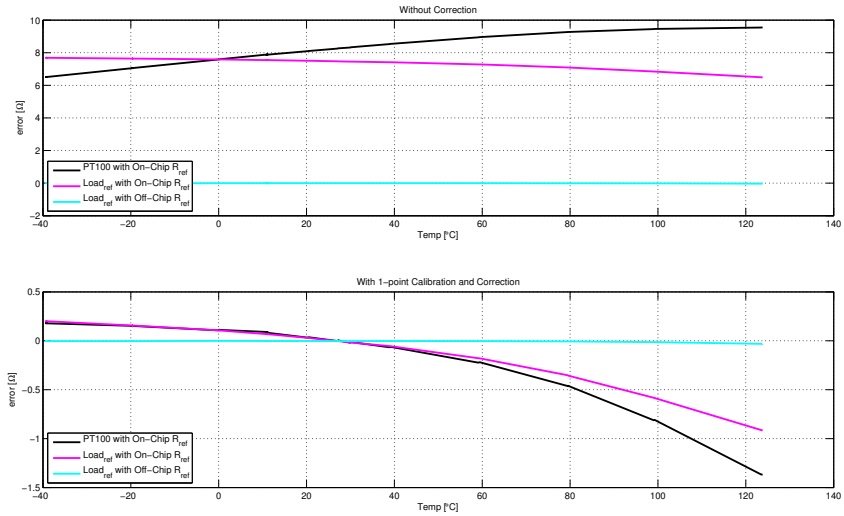


Figure 4.14: Resistance measurement errors with no correction (top), and 1-point calibration and correction (bottom).

$$c_R = \left.\frac{R_{blue}}{R_{pink}}\right|_{\text{T=27°C}} \tag{4.1}$$

where R_{blue} and R_{pink} are the resistances measured with the first and second modes, respectively.

If 2-point calibration is done, a linear correction can be made; the procedure is very similar as before, but the measurements at two temperatures are made, and two similar factors to the one obtained in the 1-point calibration are calculated. Then, a linear function can be obtained as:

$$f_R(T) = \alpha_1 \cdot T + \alpha_0 \tag{4.2}$$

where T is the temperature reading shown in section 4.3.1.

- Finally, the measured resistance of the PT100 with the on-chip reference resistance (black curve), is corrected by multiplying it with the correction factor c_R (for 1-point calibration) and with the correction function $f_R(T)$; the results of these corrections can be seen in Figures 4.14 and 4.15, respectively.

From Figure 4.15, where the CO_2 sensor temperature range is shown, one can notice certain pattern in the jumps of the measurements perfomed at each

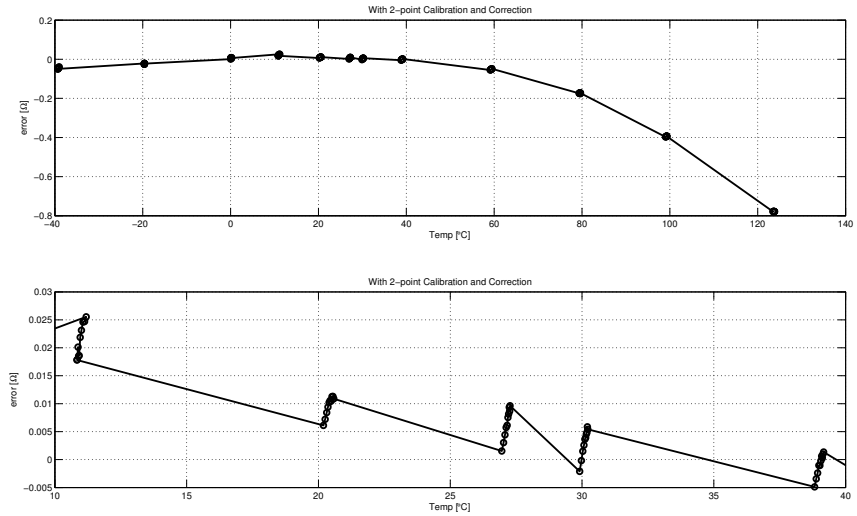


Figure 4.15: PT100 resistance measurement errors with 2-point calibration and correction: military temperature range (top), CO_2 sensor temperature range (bottom).

temperature. Since a pattern can be distinguished, it means that this error is not coming from noise. A likely explanation for this pattern is a temperature drift during the mesurements. An analysis were the temperature deviation within a single temperature measurement performed by the DUT was done in section 4.3.1. A similar reasoning is applicable here, but two effects should be analyzed; the temperature drift within a single measurement performed by the DUT, and the temperature drift between the DUT and multimeter measurements. To calculate these deviations, temperature measurements were done before and after every measurement case;[5] In contrast with the digitally-constructed reference and temperature sensor, these errors can easily be translated to resistance errors, if one uses the nominal resistance value and the temperature coefficients of a common PT100 [32]. Both, the temperature drift and the equivalent resistance deviation are shown in Figure 4.16.

Calibration against the multimeter:

After applying these two corrections to the resistance measurements shown in Figure 4.15, the black curve in Figure 4.17 can be obtained. The effect of this correction can be clearly seen, improving the measurement repeatiblity.

[5] $PT100_2$ and $PT100_3$ represent the temperature measured before and after the Transducer Front-End measurements (DUT), while $PT100_3$ and $PT100_4$ represent the temperature measured before and after the multimeter measurements.

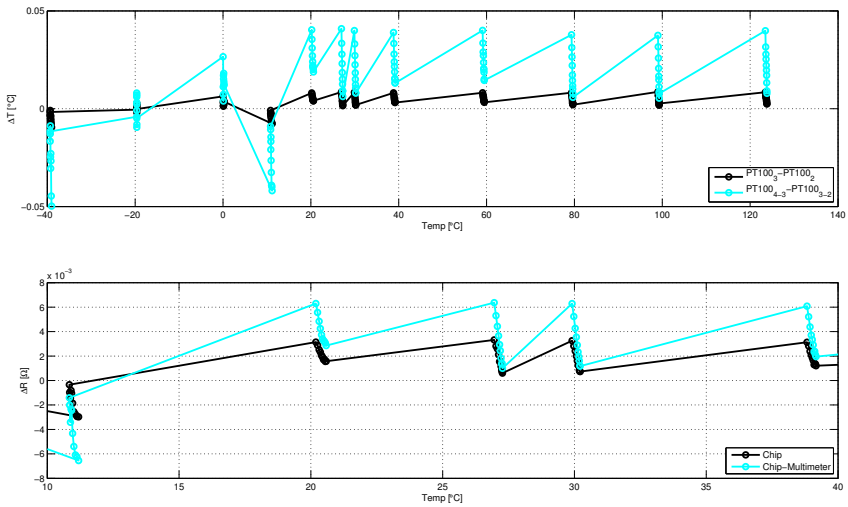


Figure 4.16: top: Temperature deviation ΔT (black: within a single DUT measurement, blue: between the measurements performed by the DUT and those performed by the multimeter). bottom: Resistance deviation (ΔR) as consequence of the ΔT.

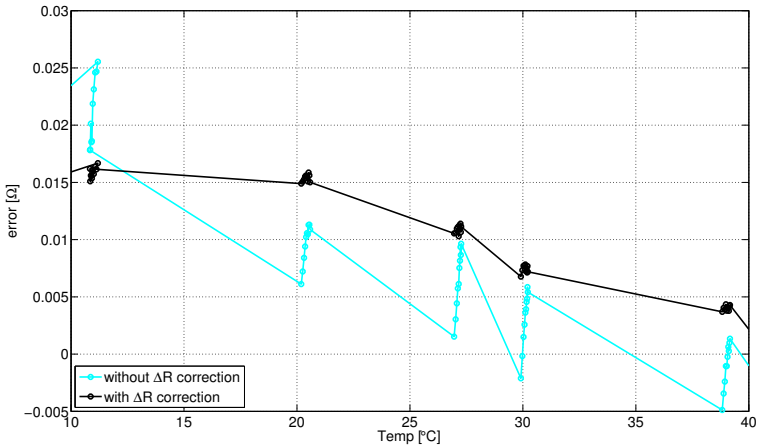


Figure 4.17: PT100 resistance measurement errors after correction for temperature drift.

As it was stated before, another method to correct the on-chip resistance nominal value and temperature coefficient, is to compare the measurement of the PT100 using this on-chip reference resistance, directly with the multimeter

measurements. By doing this, and a 2-point calibration and correction (in the same way as with the previous case), the curve in Figure 4.18 can be obtained.

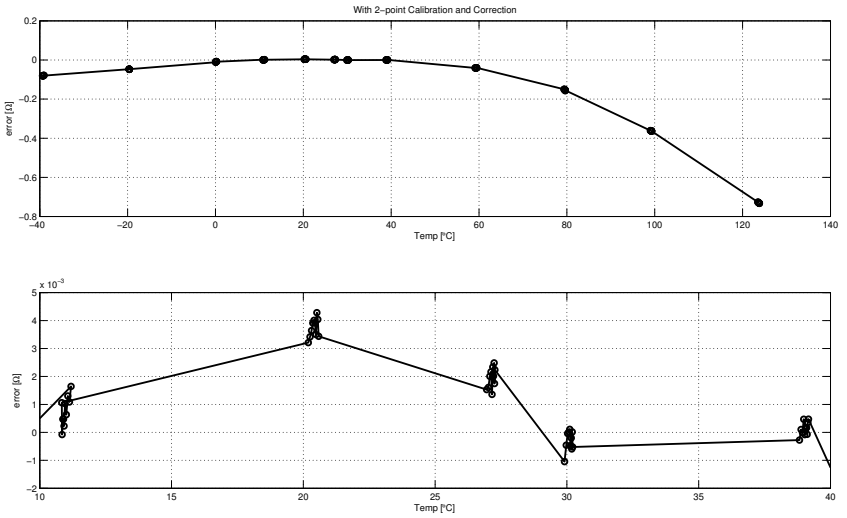


Figure 4.18: PT100 resistance measurement errors after 2-point calibration and correction, using the multimeter measurements as reference.

It is very interesting to compare the two calibration procedures, since different advantages can be obtained from each one of them; with the first one (using the external high-precision resistors and DUT), the time of calibration is much faster, since only involves measurements performed by the chip, which could translate to less production costs. If more accurate results are desired, the second approach presents better results, but the time needed for calibration will increase, increasing the final cost.

Figure 4.19 shows the error in ppm when the two different calibration approaches are used, after 2-point calibration and correction for the CO_2 sensor temperature range. When using the high-precision resistors and the DUT, accuracies between 20-160ppm can be achieved, while for the case when the multimeter is used, accuracies between -10ppm - 40ppm are possible; furthermore, resolutions of around 10ppm can be expected; in both cases, the resolution found is below 2mΩ. These values are very important for the CO_2 measurements, as it will be addressed in section 4.4.

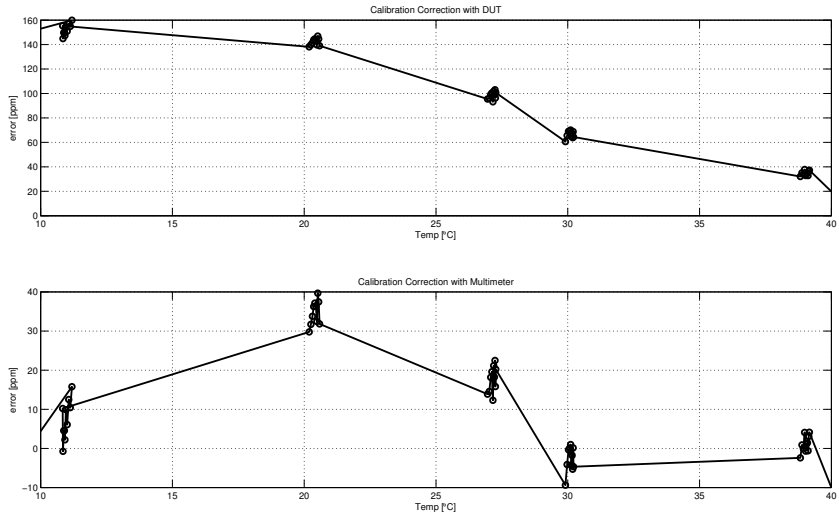


Figure 4.19: Error in the PT100 resistance measurements after 2-point calibration and correction: top: using high-precision resistors and the DUT; bottom: using the Multimeter.

4.3.3 Power Measurements

In this section, the measurements obtained for the load power consumption are shown and discussed.

Figure 4.20, shows the power consumption of the PT100 over temperature, when measured with the multimeter; this will be used as reference when obtaining the readings with the DUT.

It is interesting to see how accurate are the readings of the load voltage, to have an idea on how good the digitally-constructed reference voltage is. Figure 4.21 shows the measurements obtained with the DUT and the multimeter, and error obtained when comparing them.

It can be seen that the accuracy of the measurement performed by the DUT in the entire military range is quite good ($\pm 400\mu$V), but the noise associated with its measurements are larger than the initial design (three orders of magnitude larger). This could be due a combination of the noise added by the external DC source (see Figure 4.4), noise from the multimeter readings and, as it was discussed before, noise from the digitally-constructed voltage reference. Further investigation is needed.

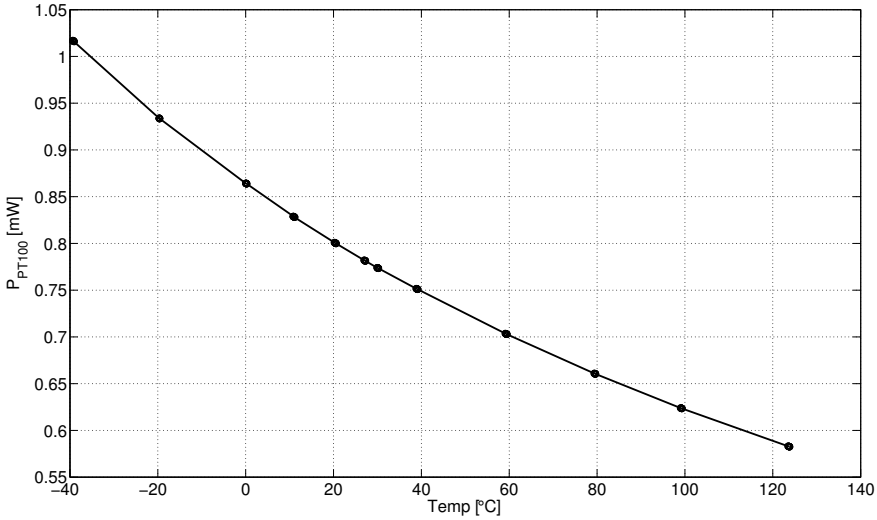


Figure 4.20: PT100 power consumption vs Temperature (measured with the Multimeter).

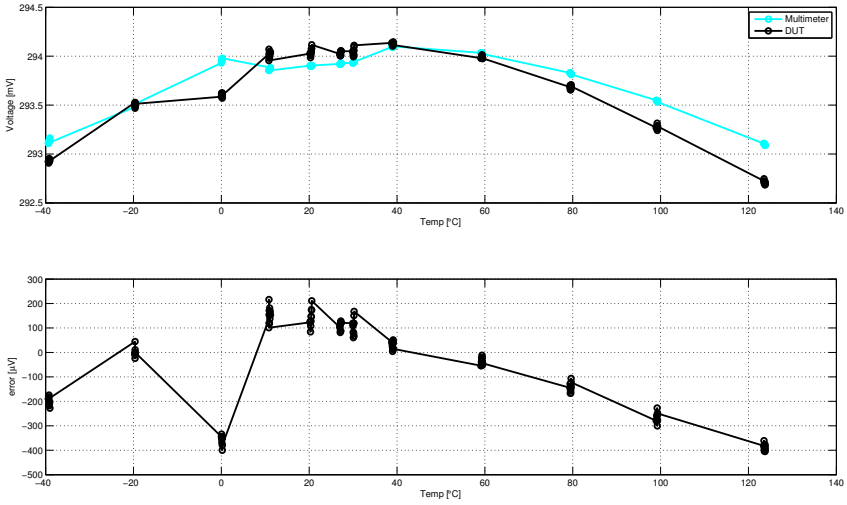


Figure 4.21: PT100 voltage measurements and errors (blue - Multimeter, black - DUT).

Now, the PT100 power measurement errors will be shown. Figure 4.22 shows the errors when no correction is applied, and when the 1-point calibration and correction on the measurement of the PT100 resistance is done. An accuracy of

$\pm 4\mu W$ is obtained, which is equivalent to $\pm 0.6\%$ (when comparing with the power dissipated at each temperature).

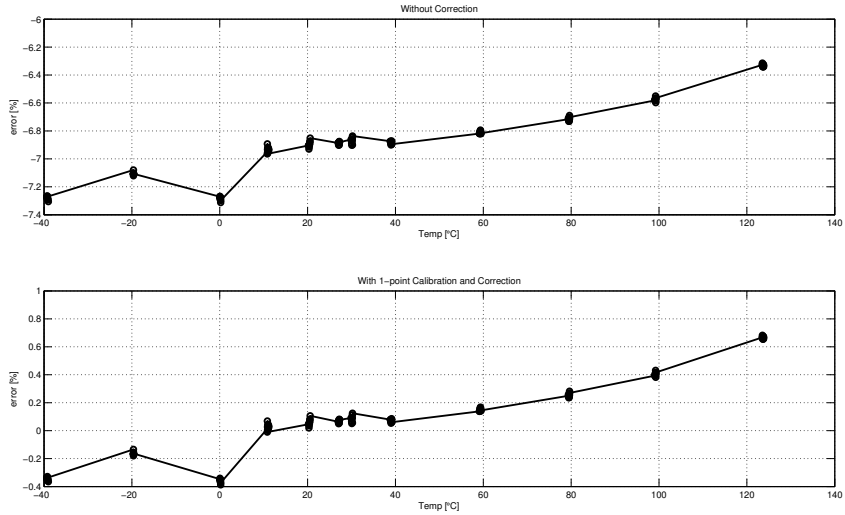


Figure 4.22: PT100 power consumption measurement errors: (top) no correction; (bottom) 1-point calibration and correction (using the correction applied in the transducer's resistance measured by the DUT).

The 2-point temperature correction of the measured transducer resistance is now used, to obtain the power dissipation readings. Figure 4.23 the error obtained when this correction is applied. As for the resistance measurement, the multimeter is used to do a 2-point calibration and correction in the power dissipation measurements (directly); the results can be seen in Figure 4.24.

It can be seen that both calibration procedures give very good measurement results when applying the corrections needed. Still, the calibration performed with the multimeter achieves better results, with an accuracy in the reading of $\pm 0.4\%$ in the military temperature range, and -0.04% - 0.08% in the CO_2 sensor temperature range. The resolution observed in this range is around 800nW in the worst-case (at 20°C), but further investigation is needed.

4.4 Estimation of the CO_2 Accuracy and Resolution

Since no CO_2 measurements have been presented, the possible CO_2 sensor accuracy and resolution will be estimated from the measurement results. One

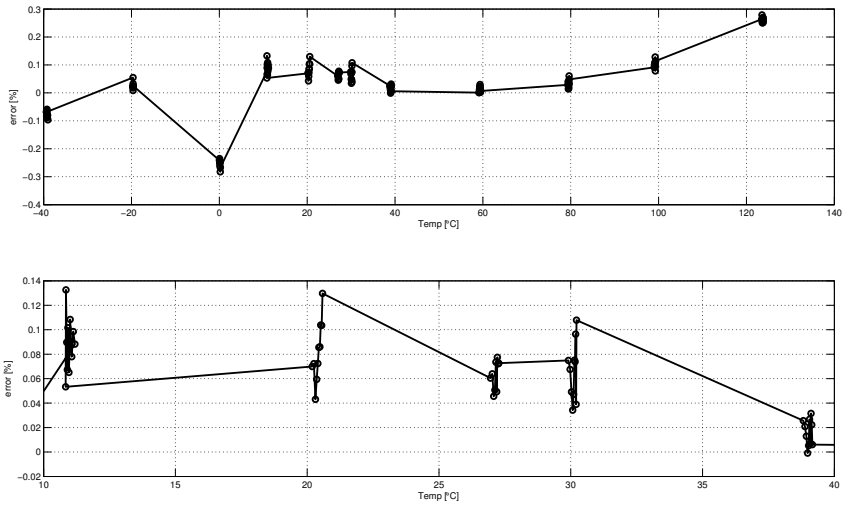


Figure 4.23: PT100 power consumption measurement errors with 2-point calibration and correction (using the correction applied in the transducer's resistance measured by the DUT).

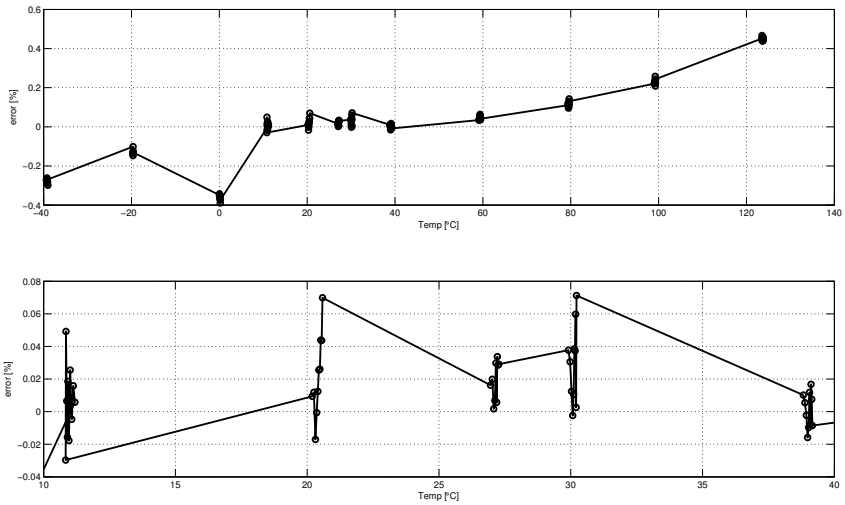


Figure 4.24: PT100 power consumption measurement errors with 2-point calibration and correction (2-point calibration and correction on the power measurement, using the multimeter).

can derive such estimations from equation (2.10):

$$\Theta = \left[\left(\frac{R_{load}}{R_o} - 1\right) - \alpha_R \cdot (T_{amb} - T_o)\right] \cdot \left(\frac{1}{\alpha_R \cdot P_{load}}\right) \tag{4.3}$$

The accuracy in the the thermal resistance (Θ) readings can be obtained as:

$$\frac{\Delta\Theta}{\Theta} = \left|\frac{\partial\Theta}{\partial P_{load}}\right| \cdot \Delta P_{load} + \left|\frac{\partial\Theta}{\partial R_{load}}\right| \cdot \Delta R_{load} + \left|\frac{\partial\Theta}{\partial T_{amb}}\right| \cdot \Delta T_{amb} \tag{4.4}$$

while the resolution, can be expressed in terms of the standard deviations as:

$$\sigma_\Theta^2 = \left|\frac{\partial\Theta}{\partial P_{load}}\right|^2 \cdot \sigma_{P_{load}}^2 + \left|\frac{\partial\Theta}{\partial R_{load}}\right|^2 \cdot \sigma_{R_{load}}^2 + \left|\frac{\partial\Theta}{\partial T_{amb}}\right|^2 \cdot \sigma_{T_{amb}}^2 \tag{4.5}$$

All the parameters needed for the calculation can be found in Table 1.1 (transducer's parameters) and from the values obtained in measurements. Table 4.1 shows the contribution to the accuracy and resolution of Θ, and the CO_2 sensor readings (ΔQ_{CO_2}), of each of the main ingredients to construct the CO_2 sensor.

Parameter	**Error**[a]	$\Delta\Theta/\Theta$ [b]	ΔQ_{CO_2} [c]	**Resolution**[a](σ)	σ_Θ [d]	$\sigma_{\Delta Q_{CO_2}}$ [e]
R_{load}	4mΩ/40ppm	301.65	761.6	2mΩ	7.69	380.8
P_{load}	600nW/0.06%	600.00	1514.9	800nW	40.8	2019.8
T_{amb}	0.1°C	1960.8	1950.5	0.15°C	100	4950.5
Total		**2862.4**	**7227**	**Total**	**155.64**	**7705**

[a] *Obtained from measurements.*
[b] *Error contribution to Θ [ppm].*
[c] *Error contribution to ΔQ_{CO_2} [ppm].*
[d] *Θ resolution [K/W].*
[e] *ΔQ_{CO_2} resolution [ppm].*

Table 4.1: Estimation of Θ and ΔQ_{CO_2} accuracies and resolution.

From this table, is clear that the estimation on the CO_2 sensor resolution is off one order of magnitude (x77) from the target specification (100ppm). The accuracy at this point is not a big concern, since it can be addressed by CO_2 calibration. It should be mentioned that this estimation uses peak-to-peak values, and no the actual standard deviation of the parameters; also, it can be seen that the main contributor of error is the temperature sensor, which may

not be well characterized due to the temperature drift effects mentioned in section 4.3.1.

Still, in a controlled environment (like in a gas chamber) where the temperature can be controlled in a very accurate way, with the power dissipation and resistance measurements, changes of 2055ppm can be detected, with an accuracy of 2276ppm.

4.5 Performance Comparison

In this section, a comparison between previously-published work in the constant power circuits and the measurements obtained will be presented.

	$P_{load_{max}} / P_{load_{min}}$ [mW]	$R_{load_{max}} / R_{load_{min}}$ [Ω]	Power Accuracy (%)
This work	**1/0.58**[a]	**148/85**[a]	**±0.06%**[b]
[9]	5.8/11	1.5k/0.5k	±1%[c]
[13]	10/0.5	675/225	±1%[c]
[14]	12/0.5	1.1k/0.9k	±0.2%[c]
[12]	10.8/0.48	1.5k/0.5k	±0.4%[c]

[a] *Values from -40°C to 125°C.*
[b] *Obtained over temperature variations (PT100 varying between 10°C and 40°C).*
[b] *Obtained over load variations.*

Table 4.2: Performance comparison with previous work.

The comparison is made based on the parameters described in [12]: the power dynamic range ($P_{load_{max}} / P_{load_{min}}$) and the resistance dynamic range ($R_{load_{max}} / R_{load_{min}}$); since the circuit presented in this work doesn't stabilize the power, but measures it, the accuracy that can be obtain with any of the two methods is included in order to have a fair comparison with previous work. The performance comparison is summarized in Table 4.2.

It should be mentioned that the prior work does not address the referencing problem that in this work is discussed and solved; also, there are no measurements over temperature in any of the reviewed papers.

A performance comparison of the digitally-constructed voltage reference and temperature sensor with prior work is not made because there is not enough

data available. Still more tests should be carried out in orther to have a full understand of the readings (this also apply for the resistance and power measurements).

4.6 Summary

In this chapter, the block diagram of the test chip has been presented, and all the test modes and control signals have been explained for the proper understanding of the different functionalities of this chip.

The use of two PCBs (one with the DUT and the other for the commercial ADC) was necessary, due to the ADC's operational temperature range. All the components in each PCB, as well as their functions, have been described in detail. Also, the experimental setup implemented in this project has been described; first, the oven that has been used to control the ambient temperature has been briefly described, followed by an explanation on the use of the multimeter's modes. Finally, a description of the method by means of which the transducer's behavior is emulated, to determine the accuracy of the Transducer Front-End, has been presented.

The measurements obtained from a single chip sample have been presented for the military temperature range. The results of the digitally-constructed voltage reference and temperature sensor have been analyzed; for the former a temperature coefficient of 9ppm/°C has been achieved, while the temperature sensor has reached an accuracy of $\pm$0.2°C, and a resolution of 0.15°C for a 1-point calibration and correction. Also, the measurements of the transducer's resistance (emulated by a PT100) and power dissipation have been shown. After a 2-point temperature calibration and correction, the resistance readings presented an accuracy ranging between -1mΩ to 4mΩ (-10ppm - 40ppm) with a resolution of around 2mΩ for the temperature range from 10°C to 40°C; for the power measurements, the circuit achieved an accuracy between -0.03% and 0.06%, with an 800nW of resolution, in the same temperature range.

In order to see how good a CO_2 sensor can be from the obtained measurements, an estimation on its resolution has been made. It was concluded that a thermal resistance accuracy of around 2862ppm can be achieved, with a resolution of 155.64[K/W], which would enable detection in the CO_2 levels in the air with an accuracy of around 0.72% with a resolution of 7705ppm. Although it is off from the target specification, it was discussed that if the power and resistance readings are used as a means of CO_2 detection, a resolution of 2055ppm with an accuracy of 2276ppm could be obtained.

Finally, a comparison with the state of the art of the constant power circuits has been presented, in which the resistance and power dynamic range, as well as the power accuracy of different work have been compared to the values obtained in this thesis.

Chapter 5

Conclusions

In this chapter, the key points of the architecture and methodology are presented, and the circuit design and the physical implementation (chip measurements) are summarized. This chapter is divided as follows: first the conclusions obtained from this project will be discussed, followed by a section in which an overview of the contributions made in this work is presented. Finally, a set of recommendations is given for future work.

5.1 Conclusions

In this thesis, a description of the CO_2 transducer have been provided, as well as a detailed explanation on the thermal-conductivity approach, to measure the CO_2 levels in the air. After showing the target CO_2 resolution and the transducer's parameters, the relative variation of its temperature and power consumption have been investigated, to see the stability needed in the constant power circuit, and the resolution of the temperature sensor, elements needed for the construction of the CO_2 sensor.

In order to see if any of the architectures in the prior work is capable of achieving the desired power stability, a study of the state of the art for constant

power circuits have been done. Also, a review of the state of the art of thermal-conductivity-based gas sensor readout circuits has been carried out in order to see the different approaches and their limitations.

Based on this study, a new architecture to measure and control the power dissipated in a load has been proposed. The problem of the reference voltage and reference resistance has been explained and a solution to this issue has been proposed, where a digitally-constructed reference is built by digitizing the base-emitter voltage of a single BJT. With the new architecture, a CO_2 sensor readout circuit has been developed, even more, it was concluded that the control of the power dissipated in the load is not mandatory, since it would be measured.

To obtain the set of specification for the circuit design, an accuracy analysis has been done, where the most important error sources are included; for this analysis, verilog models have been used, preliminary simulations have been performed, and a calibration procedure has been implemented.

With the set of specifications, a series of considerations have been made for the transistor-level design of two main blocks: the Transducer Front-End, in charge of driving the CO_2 transducer, and the "BJT Front-End", which provides the base-emitter voltages needed for the digitally-constructed voltage reference and temperature sensor. While the design of the Transducer Front-End was relatively straightforward, special care was taken in the case of the BJT Front-End, where two main topics have been discussed: the analog techniques implemented in the circuit, and the digital algorithm used to compensate for the errors in the base-emitter voltage. The main considerations for this block are summarized in the following items:

- To mitigate the variations in the forward current gain, it was decided to implement a PTAT/R biasing circuit with β_f compensation. Also, a proper BJT emitter current density has been selected, so to diminish the effect of the biasing on this parameter.
- A current-sense resistor has been included in the emitter of the main BJT device, in order to measure the biasing current. This current measurement is used in the digital algorithm to compensate for non-idealities of the base-emitter voltage.

Digital Domain:

- A DEM scheme has been designed to allow the circuit to use five different currents with an accurately-defined ratio to bias the main BJT device.

- The possibility of using five different currents gives the capability of digitizing different base-emitter voltages and emitter currents with a single transistor. A digital algorithm has been developed, where the digitized values of the V_{be}s and I_es are combined in different systems of linear equations, to compensate for the base-emitter non-idealites, and hence, construct a voltage reference and temperature sensor in the digital domain.

After the transistor-level design, the circuit has been fabricated in a 0.16μm CMOS technology, and put under test. A very complex experimental setup has been developed, for which two PCBs have been designed, and an FPGA test board is used to control, in an automatic way, every test mode on the chip and PCBs. The use of two PCBs (one with the DUT and the other for the commercial ADC) was necessary, due to the ADC's operational temperature range.

Due to time constraints, only measurements were performed for a single sample of the chip in the military temperature range. The digitally-constructed voltage reference presented a temperature coefficient of 9ppm/°C, while the temperature sensor achieved an accuracy of $\pm$0.2°C after a 1-point calibration and correction.

Also, measurements for the power dissipated in the transducer and its resistance have been presented and analyzed. After a 2-point temperature calibration and correction, the resistance readings presented an innacuracy ranging between -1mΩ to 4mΩ (-10ppm - 40ppm) with a resolution of around 2mΩ for the temperature range from 10°C to 40°C; for the power measurements, the circuit achieved an accuracy between -0.03% and 0.06%, with an 800nW of resolution, in the same temperature range.

In order to see how good a CO_2 sensor can be from the obtained measurements, an estimation on its resolution has been made. It was concluded that a thermal resistance accuracy of around 2862ppm can be achieved, with a resolution of 155.64[K/W], which would enable detection in the CO_2 levels in the air with an accuracy of around 0.72% with a resolution of 7705ppm. Although it is off from the target specification, it was discussed that if the power and resistance readings are used as a means of CO_2 detection, a resolution of 2055ppm with an accuracy of 2276ppm could be obtained.

After a comparison with the state of the art of constant power circuits, it was concluded that this work presents results of 1 order of magnitude better than the prior work. Furthermore, it tackles the referencing problem (which is never mentioned in the literature) in an innovative way.

Although the results obtained are promising, the time frame of the thesis project did not allow the full characterizaction and understanding of the chip's capabilities, and a lot of inconclusives results were obtained. Recomendations for future work are given in section 5.3.

5.2 Contributions

- ***A new method to measure thermal conductivity has been developed***
  Although a very similar methodology is implemented in [8], where the load power is measured as well, in this project the load voltage is not assumed, but measured, which should lead to better accuracy in the power readings as demonstrated. Also, no prior work mentioned the problem of the construction of a power reference, since it is provided externally by means of high-precision devices (voltages, currents and resistors). In this work, a solution is proposed and tested to construct a power reference without using precision off-chip devices, and even though the results have not reached the target, they are very promising.

- ***A digitally-constructed reference voltage and temperature sensor have been developed***
  In this work, a new way of constructing a reference voltage, and a temperature sensor has been proposed, developed and tested. It is based on the basic concept of a bandap voltage reference, where two base-emitter voltages are linearly combined, to obtained a reference independent of temperature. The difference with prior work is that this linear combination is not performed in the analog domain, but in the digital domain, by digitizing the base-emitter voltages of a single BJT with a high-precision ADC. Compensations techniques where developed in an algorithm, to mitigate the non-idealities of the BJT. From this new approach, it was also possible to digitally-construct a temperature sensor, which was used to compensate for temperature cross-sensitivity. Still, the method presented in this work is very "young" and more tests are needed in order to obtain the desire performance.

5.3 Recommendations

As mentioned, time constraints in this project did not allow the full characterization and understanding of all the test modes of the chip. Here, some of the recommendations for future work are summarized.

- The effect of the offset in the voltage readings should be taken into account. Although an attempt to correct for these errors was made, and the function is available on the PCB (by means of a system-level auto-zeroing), due to the use of external devices for this matter, the author considered that the signal path was not represented in the proper way by this mechanism, and additional errors could be added. A proposal would be to implement this system-level offset correction on-chip, by using either chopping or auto-zero.
- Although the FPGA was programmed to use DEM in the chip, the measured ratio deviates from the expected value, especially at high temperatures. First, it should be investigated by simulations, if there is any leakage path in the circuit, perhaps in the output multiplexer; then, one can measure if the DEM is actually working by setting, one by one, the different current sources to bias the main BJT and measuring them. An average can be obtained from this measurement, and it could provide information if the DEM actually works.
- Besides the offset correction, a gain correction at system-level should also be done, since a lot of external devices are in the output signal path (buffer, filters and ADC), which could compromise the readings.
- The chip should also be tested without any kind of DEM (or chopping) so to understand their effect on the final accuracy.
- One of the major problems in this project was to find a proper ADC to read the output of the chip. The selected one was the “Zoom-ADC" (as explained in Chapter 4, but due to time, this circuit couldn’t be implemented since it would first need further characterization. The entire design of this circuit was based on the input load, and sampling frequency of this ADC, so it is expected that better results are obtained with it. Also, this ADC should be faster than the one used in this project, which will further improve the measurement results (mainly for the BJT Front-End readings).
- Finally, the chip chould be put in a gas chamber for CO_2 measurements, so to see its real behavior in combination with a thermal-conductivity transducer. Only with the power and resistance readings, an estimation

of the CO_2 concentration can be made, as explained in section 4.4, and with the characterization of the chip at this point, a resolution of around 2000ppm should be obtained.

- Condensation in the chamber should be prevented around 0°C, so to have proper measurements near this temperature.
- In order to mitigate the temperature drift effect on the digitally-constructed reference and temperature sensor, the measurements could be arranged in a “common-centroid"-like sequence.
- More tests in the algorithm should be done. It would be interesting to see the relative importance of different non-idealities in the base-emitter voltages, by configurating the implemented code. Also, plots of the different V_{be}s and I_es over temperature should be done, so to understand how close they behave to the simulated case.

Appendix A

Verilog-A Models

A.1 Implemented codes

The codes that will be shown in this appendix were used to find the set of specs for the circuit design. The schematic used for the preliminary simulations can be seen in Figure A.1.

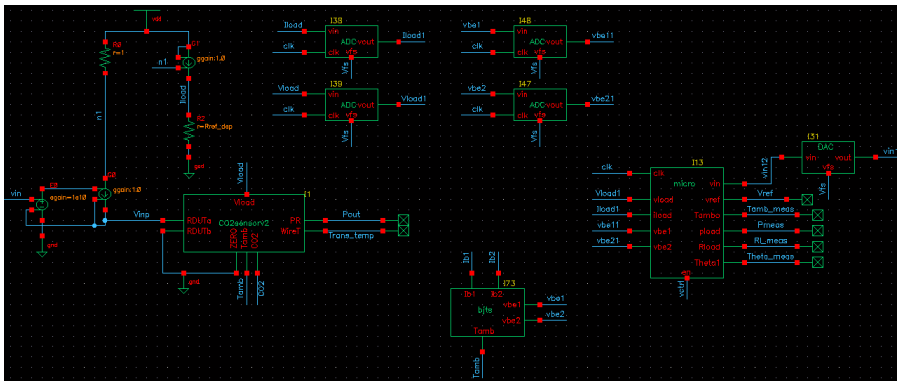


Figure A.1: Schematic.

A.1.1 Transducer's Model (CO2sensorv2 in schematic)

```
// VerilogA for CO2model, CO2sensorv2, veriloga

`include "constants.vams"
`include "disciplines.vams"

module CO2sensorv2(Vload, CO2, PR, RDUTa, RDUTb, Tamb, WireT, ZERO);

output Vload;
inout CO2, PR, RDUTa, RDUTb, Tamb, WireT, ZERO;
electrical Vload, CO2, PR, RDUTa, RDUTb, Tamb, WireT, Zero;

// PARAMATERS:
parameter real thetazeroppmT0 = 51k ;
parameter real c = 784.314p ;
parameter real alpha = 2.6m ;
parameter real T0 = 298 ;
parameter real Sco2 = 20.2m ;
parameter real R0 = 100 ;

// VARIABLES:
real Rload; // Transducer Resistance
real Rpar; // Parasitic Resistance
real iload; // Load current
real itemp; // Power is like current in temperature domain
real Rtherm; // Thermal Resistivity
real deltaT; // Temperature increase

analog begin

@(initial_step)
begin
Rload = R0;
Rpar = 1;
end

iload = I(RDUTa,RDUTb);

V(RDUTa,RDUTb) <+ iload * (Rload + Rpar) + white_noise( 4 * `P_K * V(WireT)
* (Rload + Rpar) , "thermal");
```

```
V(PR) <+ pow(iload,2) * Rload;

itemp = V(PR,ZERO);

Rtherm = thetazeroppmT0 + Sco2*V(CO2,ZERO) - V(ZERO);

deltaT = itemp * Rtherm;

V(WireT) <+ V(Tamb) + deltaT;

Rload = ( V(ZERO) + R0 ) * ( V(ZERO) + 1 + alpha*( V(WireT,ZERO) - T0
) ) - V(ZERO);

I(WireT,Tamb) <+ c * ddt(V(WireT,Tamb));

end

endmodule
```

A.1.2 ADC's Model

```
// VerilogA for Thesis, micro, veriloga

`include "constants.vams"
`include "disciplines.vams"

module adc(vin, vfs, clk, vout);

input vin, vfs, clk; // vfs = full scale voltage
output vout;
electrical vin, vfs, vout, clk;
parameter integer bits = 15;
parameter real clk_vth = 0.9;
parameter real inl = 0.5; // INL in LSB
parameter real vnoise = 0.5; // Integrated thermal Noise (Voltage)
in LSB

real vlsb, vo2;
integer vo1, rand;
//real vo1;
```

```
analog begin

@(initial_step)
begin
vo2 = 1e-12;
end

@(cross(V(clk)-clk_vth,+1)) // Sample
begin

vlsb = V(vfs)/pow(2,bits); // LSB

// INL & Quantization Noise
vo1 = V(vin)/vlsb + inl * sin(2*‘M_PI*V(vin)/V(vfs)) + vnoise;
vo2 = vo1; // Quantization

end

V(vout) <+ vo2;

end

endmodule
```

A.1.3 BJT's Model

```
// VerilogA for Thesis, bjts, veriloga

‘include "constants.vams"
‘include "disciplines.vams"

module bjts(Tamb, Ib1, Ib2, vbe1, vbe2);

// INPUTS & OUTPUTS:
input Tamb; // Ambient Temperature
input Ib1; // Bias current for BJT1
input Ib2; // Bias current for BJT2
output vbe1; // Vbe1
output vbe2; // Vbe2
```

```
electrical Tamb, Ib1, Ib2, vbe1, vbe2;

// PARAMETERS:
parameter real To = 298; // Typical ambient Temp (°K)
parameter real Vbg = 1.155; // Bandgap Voltage at T = 0K
parameter real Iso = 1e-16; // Saturation Current for the BJTs (T =
To)
parameter real betaf = 4.7; // Forward Current Gain
parameter integer n = 4; // Constant (related to the doping level)

// VARIABLES:
real Vto; // Vto = k*To/q
real Vt; // Vt = k*T/q
real ratio_betaf; // For the actual collector current
real Is; // Saturation Current

// ANALOG BEGIN
analog begin

@(initial_step)
begin

Vto = `P_K / `P_Q * To;
ratio_betaf = betaf/(betaf+1);

end

Vt = Vto * V(Tamb) / To;

// Declaration of the Saturation Current:
Is = ( Iso * pow( `M_E , Vbg/Vto ) ) * pow( V(Tamb)/To , n ) * pow(
`M_E , -Vbg/Vt );

// Declaration of the BE Voltages:
V(vbe1) <+ Vt * ln((V(Ib1) + 1e-28) * ratio_betaf/Is);
V(vbe2) <+ Vt * ln((V(Ib2) + 1e-28) * ratio_betaf/Is);

end


endmodule
```

A.1.4 DAC's Model

```
// VerilogA for Thesis, micro, veriloga

`include "constants.vams"
`include "disciplines.vams"

module dac(vin, vfs, vout);

input vin, vfs; // vfs = full scale voltage
output vout;
electrical vin, vfs, vout;
parameter integer bits = 15;
parameter real Vfs_nom = 0.8;

real vlsb, vo1, vlsb_nom;
integer vo2;

analog begin

@(initial_step)
begin

vlsb_nom = Vfs_nom/pow(2,bits);

end

if ($abstime < 10u)
begin
vo1 = V(vin);
end
else
begin
vlsb = V(vfs)/pow(2,bits);
vo2 = V(vin)/vlsb;
vo1 = vo2*vlsb_nom;
end

V(vout) <+ vo1;

end
```

```
endmodule
```

A.1.5 Microcontroller's Model (post-processing)

```
// VerilogA for Thesis, micro, veriloga

`include "constants.vams"
`include "disciplines.vams"

module micro(vload, iload, vbe1, vbe2, vin, pload, Rload, vref, Theta1,
Tambo, en, clk);

// INPUTS & OUTPUTS:
input vload;  // Load Voltage
input iload; // Load Current
input vbe1; // Base-Emitter Voltage for Ic1 (collector current 1)
input vbe2; // Base-Emitter Voltage for Ic2 (collector current 2)
input en; // Enable Signal (enables the output vin)
input clk; // Clock (to stablish the delay)
inout vin; // Control voltage Output
output pload; // Load Power read-out
output Rload; // Load Resistance read-out
output Theta1; // Theta1 read-out
output vref; // Reference Voltage Digitally created
output Tambo; // Measured Ambient Temperature

electrical vload, iload, vbe1, vbe2, vin, pload, Rload, vref, Theta1,
Tambo, en, clk;

// PARAMETERS:
parameter real tdel = 200u; // Signal Delay (or lattency)
parameter real Vin = 500m; // Initial value of the control voltage
vin
parameter real Pnom = 2.5m; // Nominal value of the load Power (with
the control loop)
parameter real Vfs_nom = 0.8; // Nominal Full-scale Voltage
parameter real bits = 15; // Number of bits of the ADC
parameter real bits_bjt = 15; // Number of bits of the ADC (for VBE)
parameter real Rref = 1; // Nominal value of the reference Resistance
parameter real Rload_nom = 100; // Nominal value of the load Resistance
parameter real TCR1 = 15u; // Nominal value of the TCR1 (load Res)
```

```
parameter real TCR2 = 500n; // Nominal value of the TCR2 (load Res)
parameter real clk_vth = 0.9; // Threshold voltage for the clock
parameter real k = 0.5; // k = Vrefo / Vbg
parameter real Vbg = 1.155; // Bandgap Voltage at T = 0K
parameter real Iso = 1e-16; // Nominal saturation current for the BJTs
(at To)
parameter real Ic2o = 50u; // Nominal collector current for the BJT
2 (at To)
parameter real ratio_Ic = 6; // Nominal collector current ratio for
the BJTs
parameter real To = 298; // Typical ambient Temp
parameter real alpha_r = 2.6m; // Nominal Tempo for the Load Resistance
parameter real betaf = 4.7; // Forward Current Gain (BJTs)
parameter integer n = 4; // Constant (related to the doping level; BJTs)

// VARIABLES:
real vout; // Output voltage (to vin pin)
real vout_past;  // Previous output voltage (read at
// the beggining, to calculate the next vout)
real trise;  // Rise time
real td;  // Delay time
real pout; // Power Load calculation (to pload1 pin)
real rl; // Resistance Load calculation (to Rload1 pin)
real theta1; // Theta1 calculation (to Theta1 pin)
real vlsb; // Nominal LSB voltage
real vlsb_bjt; // Nominal LSB voltage for the VBE
real vrefo; // Reference Voltage (to vref pin)
real vrefo1; // Reference Voltage (1st iteration)
real vrefo2; // Reference Voltage (2nd iteration)
real vrefo3; // Reference Voltage (3rd iteration)
real vrefo4; // Reference Voltage (4th iteration)
real vrefo5; // Reference Voltage (5th iteration)
real Vref_nom; // Reference Voltage Vref_nom = k * Vbg
real alpha; // Vbe1 coefficient for Vrefo
real beta; // Vbe1 coefficient for Vrefo
real rho; // Delta_vbe coefficient for Vrefo (initial)
real rho1; // Delta_vbe coefficient for Vrefo (1st iteration)
real rho2; // Delta_vbe coefficient for Vrefo (2nd iteration)
real rho3; // Delta_vbe coefficient for Vrefo (3rd iteration)
real rho4; // Delta_vbe coefficient for Vrefo (4th iteration)
real temp; // Measured Temperature
real temp1; // Measured Temperature (1st iteration)
real temp2; // Measured Temperature (2nd iteration)
real temp3; // Measured Temperature (3rd iteration)
```

```
real temp4; // Measured Temperature (4th iteration)
real temp5; // Measured Temperature (5th iteration)
real Rref_dep; // Reference Resistance with temperature dependency
real mr; // Ratio between the load Resistances
real Vto; // Vto = k*To/q
real ratio_betaf; // For the actual collector current (Nominal)
real Vbe1o; // BE1 Voltage at To (Nominal)
real Vbe2o; // BE2 Voltage at To (Nominal)
real vbe1_aux; // BE1 Voltage
real vbe2_aux; // BE2 Voltage
real delta_Vbe; // Vbe1 - Vbe2
real error; // Error between the nominal and digital Vrefo
real m1; // Slope of the Vbe1 (V/°K)
real m2; // Slope of the Vbe2 (V/°K)
integer l; // Counter

// ANALOG BEGIN
analog begin

@(initial_step)
begin


Vto = ‘P_K / ‘P_Q * To;
ratio_betaf = betaf/(betaf+1);


vlsb = Vfs_nom/pow(2,bits); // Calculation of the nominal LSB
vlsb_bjt = Vfs_nom/pow(2,bits_bjt); // Calculation of the nominal LSB
for the VBE

// Declaration of the BE Voltages at To:
Vbe1o = Vto * ln(Ic2o * ratio_Ic * ratio_betaf/Iso);
Vbe2o = Vto * ln(Ic2o * ratio_betaf /Iso);

// Calculation of the Vbe’s slopes:
m1 = (Vbg + Vto*(n-1) - Vbe1o)/To;
m2 = (Vbg + Vto*(n-1) - Vbe2o)/To;

// Calculation of the coefficients:
alpha = k*m2/(m2-m1);
beta = k*m1/(m2-m1);
rho = -(alpha-beta)*(n-1)/ln(ratio_Ic);
```

```
Vref_nom = k* ( Vbg + (n-1)*Vto ); // Nominal Vrefo value

end

if (($abstime < 1u) && (V(en) > 0.5) ) // Step Behavior for the output
voltage (Begin)
begin
vout = 0;
trise = 0;
td = 0;
end
else if (($abstime < 10u) && (V(en) > 0.5) )
begin
vout = Vin;
trise = 0;
td = 0;
end // Step Behavior for the output voltage (End)
else if (V(en) <= 0.5) // Control Voltage Off if En = 0
begin
vout = 0;
td = 0;
trise = 0;
end

////////////////////////////////
// Digital Reference Voltage:
////////////////////////////////

// Delta Vbe:
delta_Vbe = ( V(vbe1) - V(vbe2) ) * vlsb_bjt;

//////////////////
// 1st iteration
//////////////////
// Digital Vrefo:
vrefo1 = (alpha*V(vbe1) - beta*V(vbe2)) * vlsb_bjt + rho*delta_Vbe;
// Digital Construction

// Ambient Temperature Measurement:
     temp1 = delta_Vbe / (vrefo1 + 1e-28) * (Vref_nom/( ln(ratio_Ic)
* `P_K/`P_Q ));

// Delta_Vbe coefficient:
rho1 = -(alpha-beta)*(n-1)/ln(ratio_Ic) * ( 1 - ln(( temp1 + 1e-28
```

```
)/To) - To/( temp1 + 1e-28) );
//////////////////

// Several Iteration Calculation of Vrefo (with Temperature measurement):
//////////////////
// 2nd iteration
//////////////////
// Digital Vrefo:
vrefo2 = (alpha*V(vbe1) - beta*V(vbe2)) * vlsb_bjt + rho1*delta_Vbe;
// Digital Construction

// Ambient Temperature Measurement:
     temp2 = delta_Vbe / (vrefo2 + 1e-28) * (Vref_nom/( ln(ratio_Ic)
* `P_K/`P_Q ));

// Delta_Vbe coefficient:
rho2 = -(alpha-beta)*(n-1)/ln(ratio_Ic) * ( 1 - ln(( temp2 + 1e-28
)/To) - To/( temp2 + 1e-28) );
//////////////////

//////////////////
// 3rd iteration
//////////////////
// Digital Vrefo:
vrefo3 = (alpha*V(vbe1) - beta*V(vbe2)) * vlsb_bjt + rho2*delta_Vbe;
// Digital Construction

// Ambient Temperature Measurement:
     temp3 = delta_Vbe / (vrefo3 + 1e-28) * (Vref_nom/( ln(ratio_Ic)
* `P_K/`P_Q ));

// Delta_Vbe coefficient:
rho3 = -(alpha-beta)*(n-1)/ln(ratio_Ic) * ( 1 - ln(( temp3 + 1e-28
)/To) - To/( temp3 + 1e-28) );
//////////////////

//////////////////
// 4th iteration
//////////////////
// Digital Vrefo:
vrefo4 = (alpha*V(vbe1) - beta*V(vbe2)) * vlsb_bjt + rho3*delta_Vbe;
// Digital Construction

// Ambient Temperature Measurement:
```

```
     temp4 = delta_Vbe / (vrefo4 + 1e-28) * (Vref_nom/( ln(ratio_Ic)
* `P_K/`P_Q ));

// Delta_Vbe coefficient:
rho4 = -(alpha-beta)*(n-1)/ln(ratio_Ic) * ( 1 - ln(( temp4 + 1e-28
)/To) - To/( temp4 + 1e-28) );
//////////////////

//////////////////
// 5th iteration
//////////////////
// Digital Vrefo:
vrefo5 = (alpha*V(vbe1) - beta*V(vbe2)) * vlsb_bjt + rho4*delta_Vbe;
// Digital Construction

// Ambient Temperature Measurement:
     temp5 = delta_Vbe / (vrefo5 + 1e-28) * (Vref_nom/( ln(ratio_Ic)
* `P_K/`P_Q ));
//////////////////

// FINAL DECLARATION:
// Digital Vrefo:
vrefo = vrefo5;

// Ambient Temperature Measurement:
     temp = temp5;

////////////////////////////////

// Reference Resistance with Temperature Dependency:
Rref_dep = Rref * ( 1 + TCR1*(temp - To) + TCR2*pow((temp - To),2)
);

// Load Power Read-Out:
pout = V(vload) * V(iload) * pow(vlsb,2)/( pow(vrefo,2) + 1e-28)* (
pow(Vref_nom,2) / Rref_dep ); // With Digital Vref and Rref_dep
//pout = V(vload) * V(iload) * pow(vlsb,2)/( pow(vrefo,2) + 1e-28)*
( pow(Vref_nom,2) / Rref ); // With Digital Vref
//pout = V(vload) * V(iload) * ( pow(vlsb,2) / Rref ); // With nominal
ADC-LSB

// Load Resistance Read-Out:
rl = V(vload)/( V(iload) + 1e-28 ) * Rref_dep; // With Rref_dep
//rl = V(vload1)/( V(iload1) + 1e-28 ) * Rref; // With Rref
```

```
// Theta Read-Out:

// Theta3: It is obtained with just rl1 and P1 (also Tamb meas):
theta1 = ( (rl/Rload_nom - 1) + alpha_r * (To - temp) )/(alpha_r *
pout + 1e-28);

if ( (theta1 > 1G) )
begin
theta1 = 0;
end

// Closed Control Loop
@(cross(V(clk)-clk_vth,+1)) // Every rising Edge ...
begin
if (V(en) > 0.5)
begin
vout_past = V(vin);
vout = sqrt( Pnom / (pout + 1e-28) ) * vout_past;
trise = 0;
td = tdel;
end
end


// Declaration of the Output pins:
V(vin)   <+ transition(vout,td,trise);
V(pload) <+ transition(pout,td,trise);
V(Rload) <+ transition(rl,td,trise);
V(Theta1) <+ transition(theta1,td,trise);
V(Tambo)  <+ transition(temp,td,trise);
V(vref)   <+ transition(vrefo,td,trise);
end

endmodule
```

Appendix B

PCB Schematics and Layout

In this appendix, the schematics and layouts of the different PCBs used are presented. Due to the size of the schematics figures, they were divided in different parts, so the reader can identify each of the components inside the PCBs. All the designs were done in *Altium Designer Summer 09* software.

B.1 Main PCB

This section contains the schematic and layout for the Main PCB. The figures presented in this section are as follows:

- Figure B.1: shows the DUT with Switch IC used auto-zero at system level, and to set the test voltages (common-mode, and differential-mode). It also shows the reference voltage IC with the 8-bit DAC, as well as an external reference pin, to set the input of the Transducer Front-End. Another component shown in this figure is the reference resistance used for calibration purposes, and finally, the buffer at the output of the DUT is shown.

- Figure B.2: shows the DIP-40 socket where the external transducer chip will be connected. This chip contains 4 transducers: 2 sense transducers, and 2 reference transducers; manually, one can select one pair of transducers composed of one sense transducer and one reference transducer (with the 4x2 Headers). By programming (or manually), the user can select (with the help of MULT1) either the sense transducer or the reference transducer, for the measurements. The SWITCH component, is used to multiplexed the measurement of the transducer resistance, either with the multimeter (via the 4 SMB connectors shown in the figure) or with the DUT.
- Figure B.3: shows the input pins coming from the FPGA (actually, coming from the ADC PCB). It also shows an “Adapter" that is used to connect to an external board (developed by Ir. Zeyu Cai in the Electronic Instrumentation Group of TU Delft) for measurements in the climate chamber in Leuven.
- Figure B.4: shows the power management configuration.
- Figure B.5: shows the composite drawing of the PCB layout.
- Figure B.6: shows the assembly drawing of the PCB layout (Top view).
- Figures B.7, B.8, B.9 and B.10: show the final artwork prints of the PCB layout (Top, Mid-Layer1, Mid-Layer2 and Bottom views, respectively).

B.2 ADC PCB

This section contains the schematic and layout for the ADC PCB. The figures presented in this section are as follows:

- Figure B.11: shows the ADC with filtering components for its input and output pins. Also the reference voltage IC is shown, as well as the 8-bit DAC, and the filter network used afterwards.
- Figure B.12: shows the inout pins for the FPGA, the level-shifter component (and signals), and the signals going to the main PCB. It also shows an extra socket, which is to adapt the measurement setup in the climate chamber situated in Leuven.
- Figure B.13: shows the power management configuration.
- Figure B.14: shows the composite drawing of the PCB layout.

- Figure B.15: shows the assembly drawing of the PCB layout (Top view).
- Figures B.16 and B.17: show the final artwork prints of the PCB layout (Top and Bottom views, respectively).

B.3 Transducer PCB

This section contains the schematic and layout for the PCB used to measure the behaviour of the readout circuit by emulating the transducer with a PT100. The figures presented in this section are as follows:

- Figure B.18: shows a 4-way terminal, where the 4-wire connections of a PT100 RTD are plugged in; it also shows the 4-wire connection of a reference resistance [16], and the 40 pin connection to plug to the main PCB.
- Figure B.19: shows the composite drawing of the PCB layout.

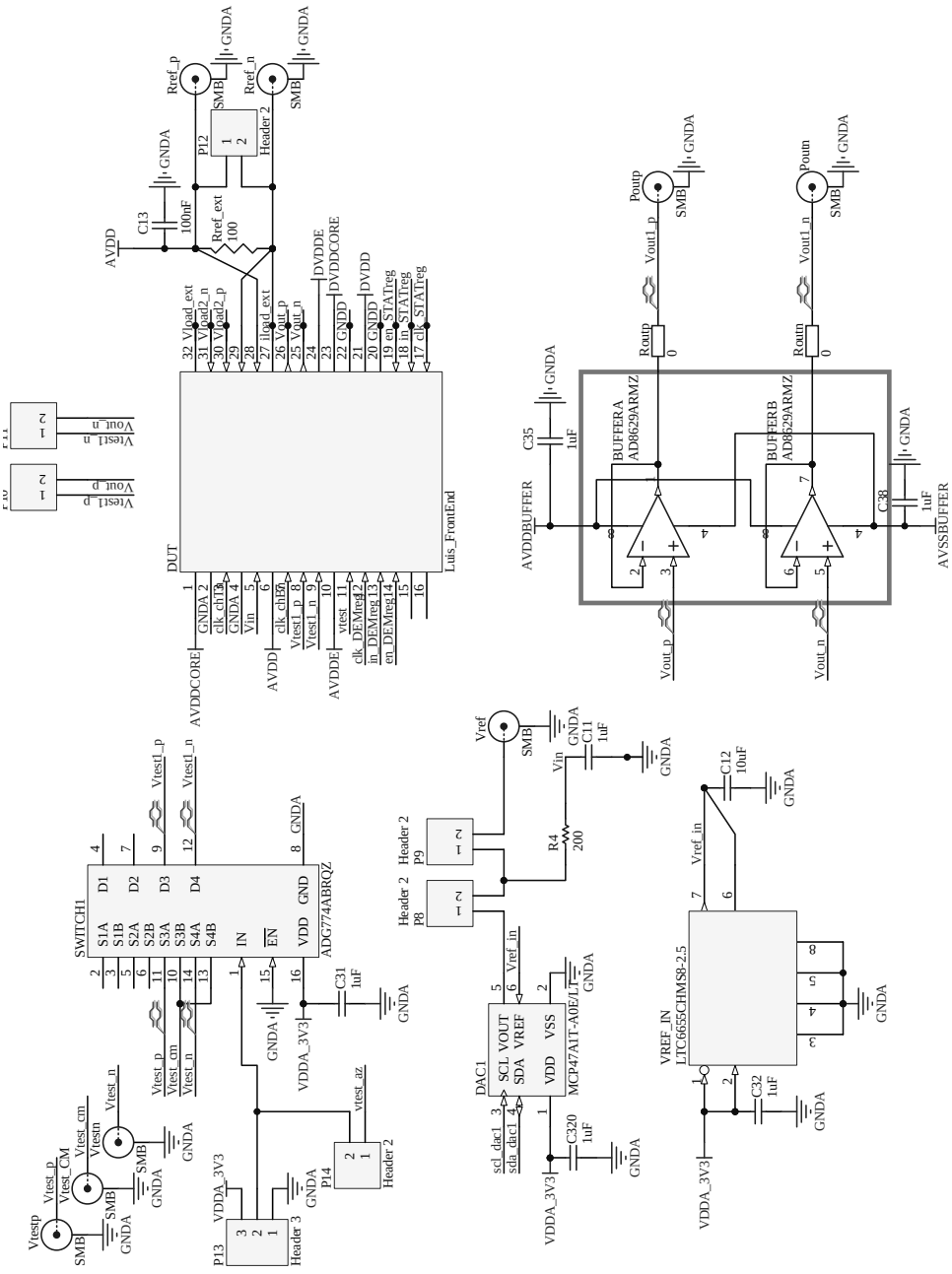


Figure B.1: Schematic of the ADC PCB (part 1).

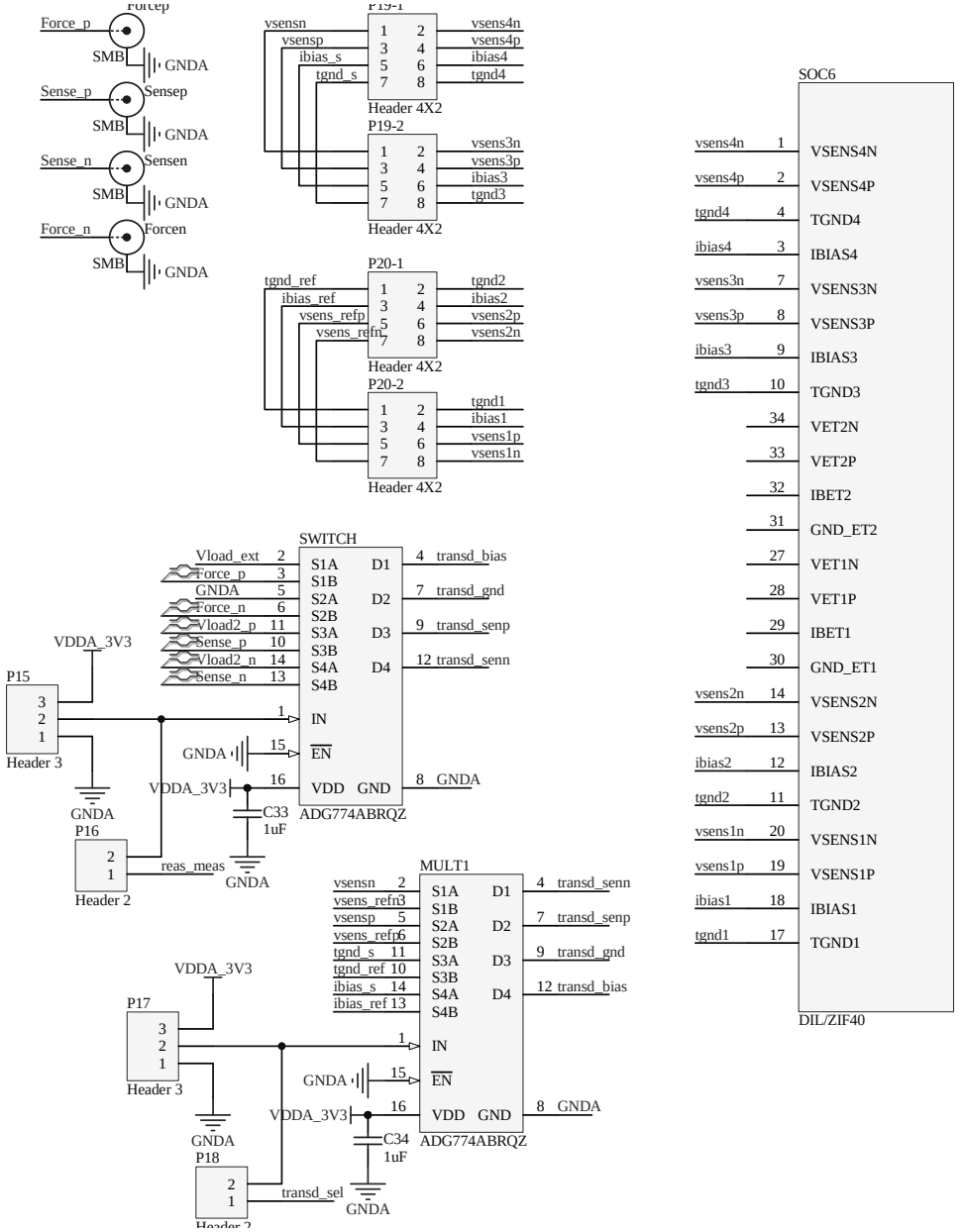


Figure B.2: Schematic of the ADC PCB (part 2).

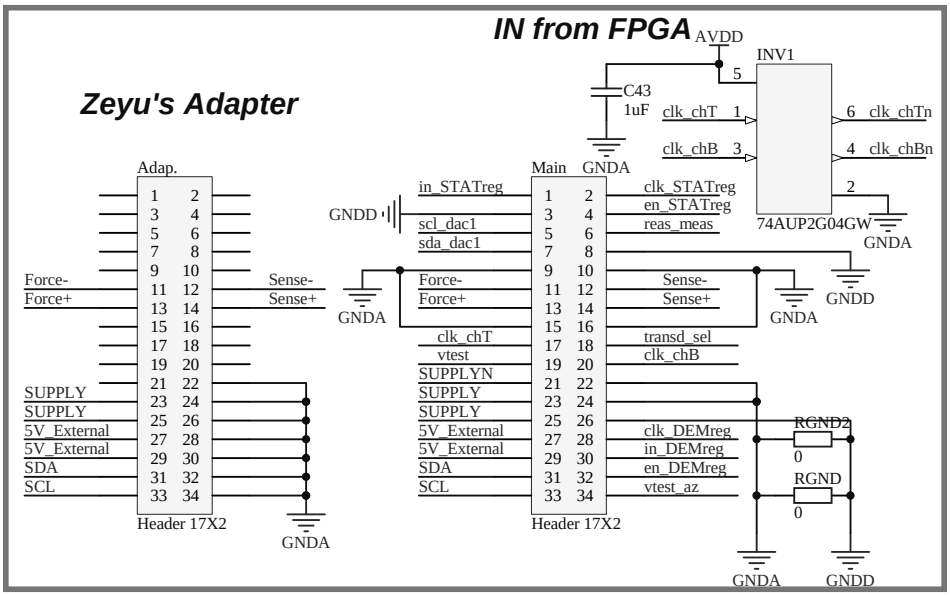


Figure B.3: Schematic of the ADC PCB (part 3).

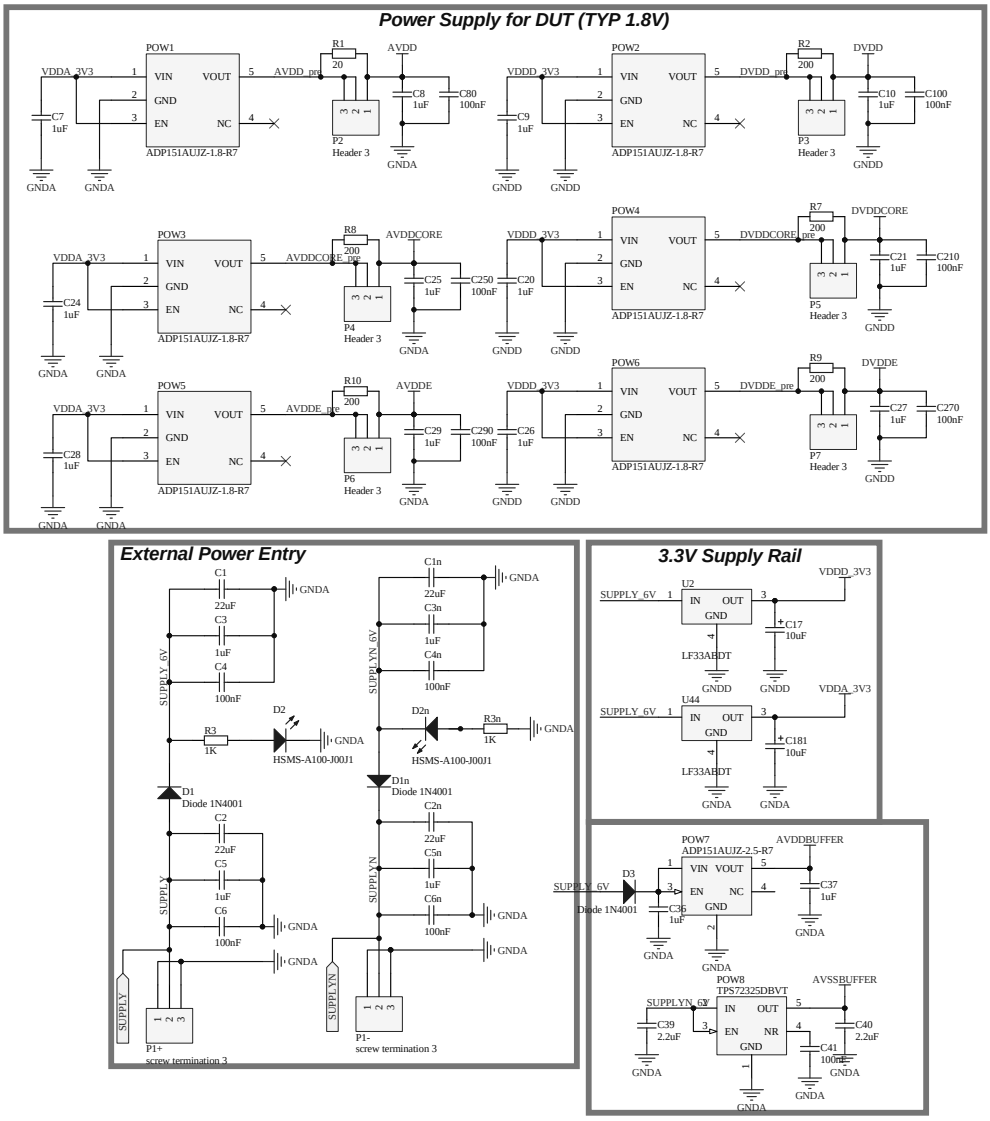


Figure B.4: Schematic of the ADC PCB (part 4).

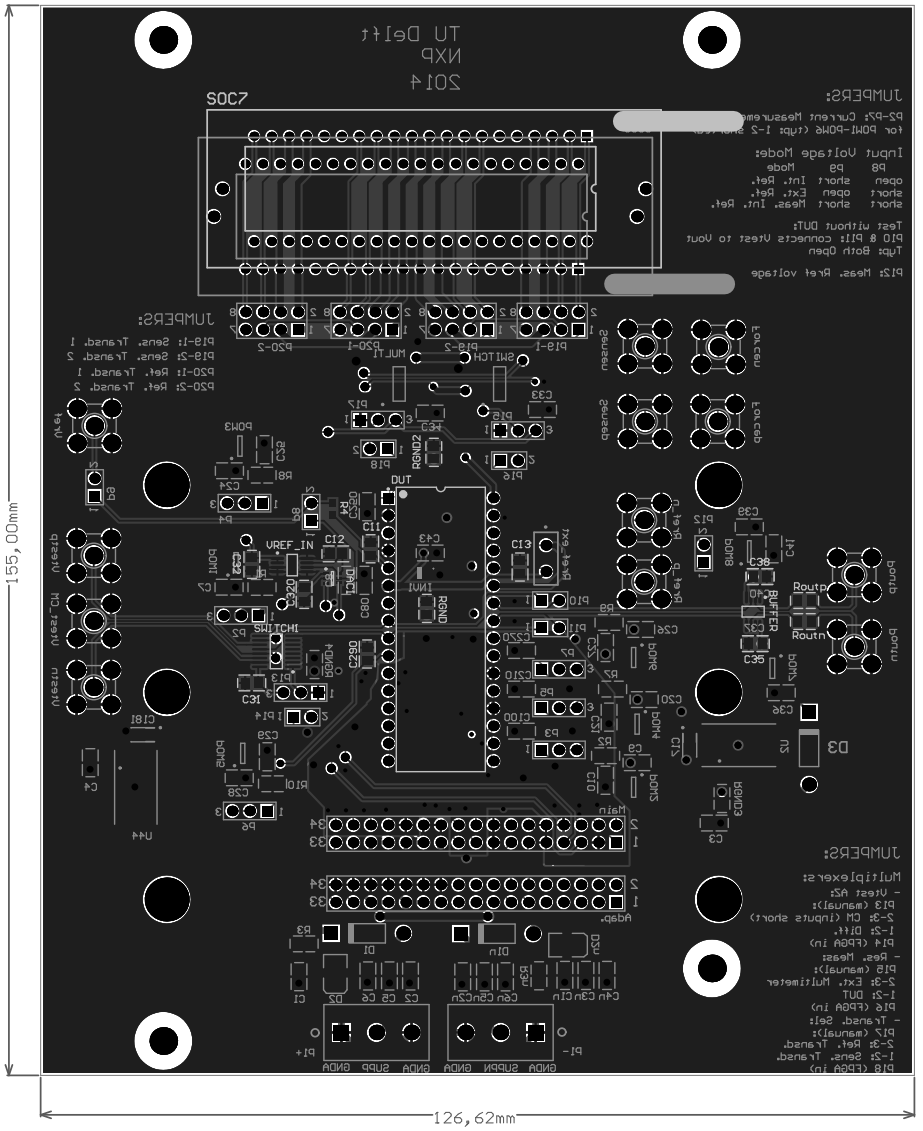


Figure B.5: Layout of the ADC PCB (Composite Drawing).

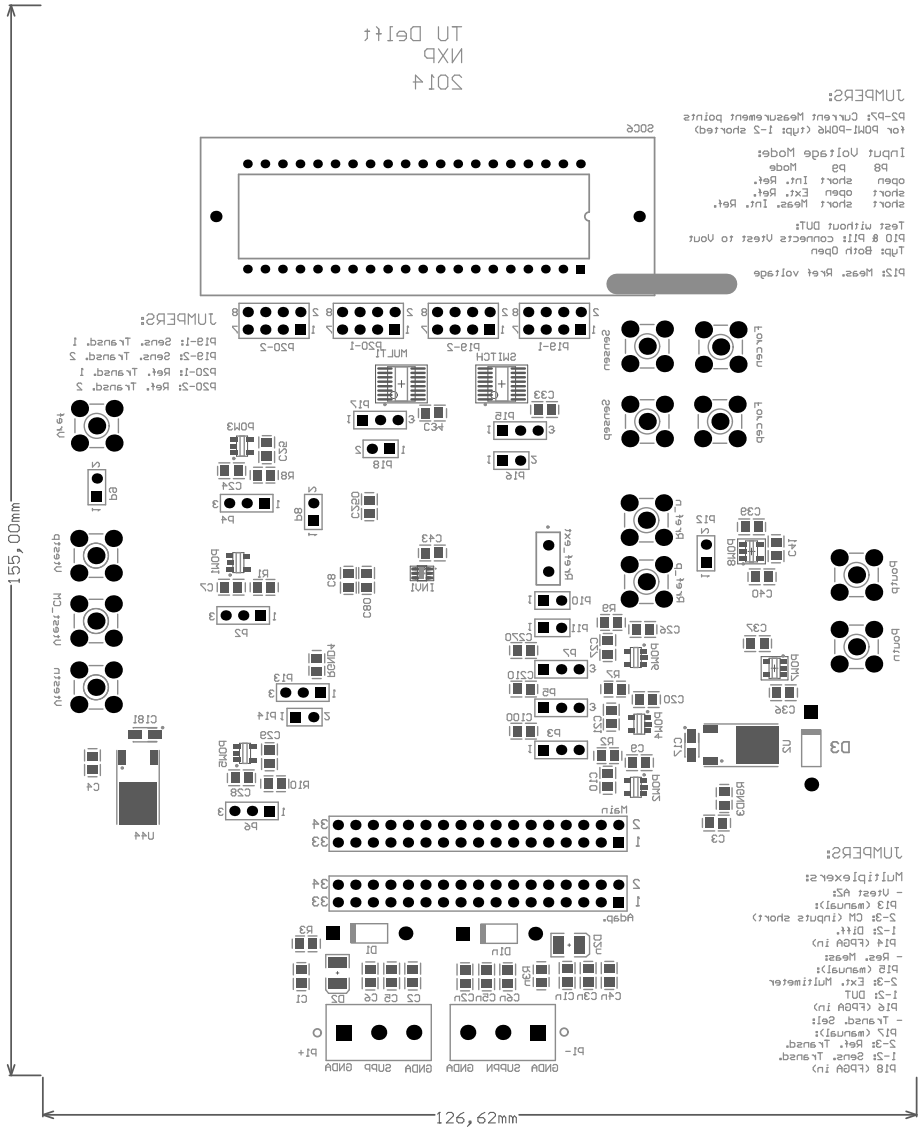


Figure B.6: Layout of the ADC PCB - Top (Assembly Drawing).

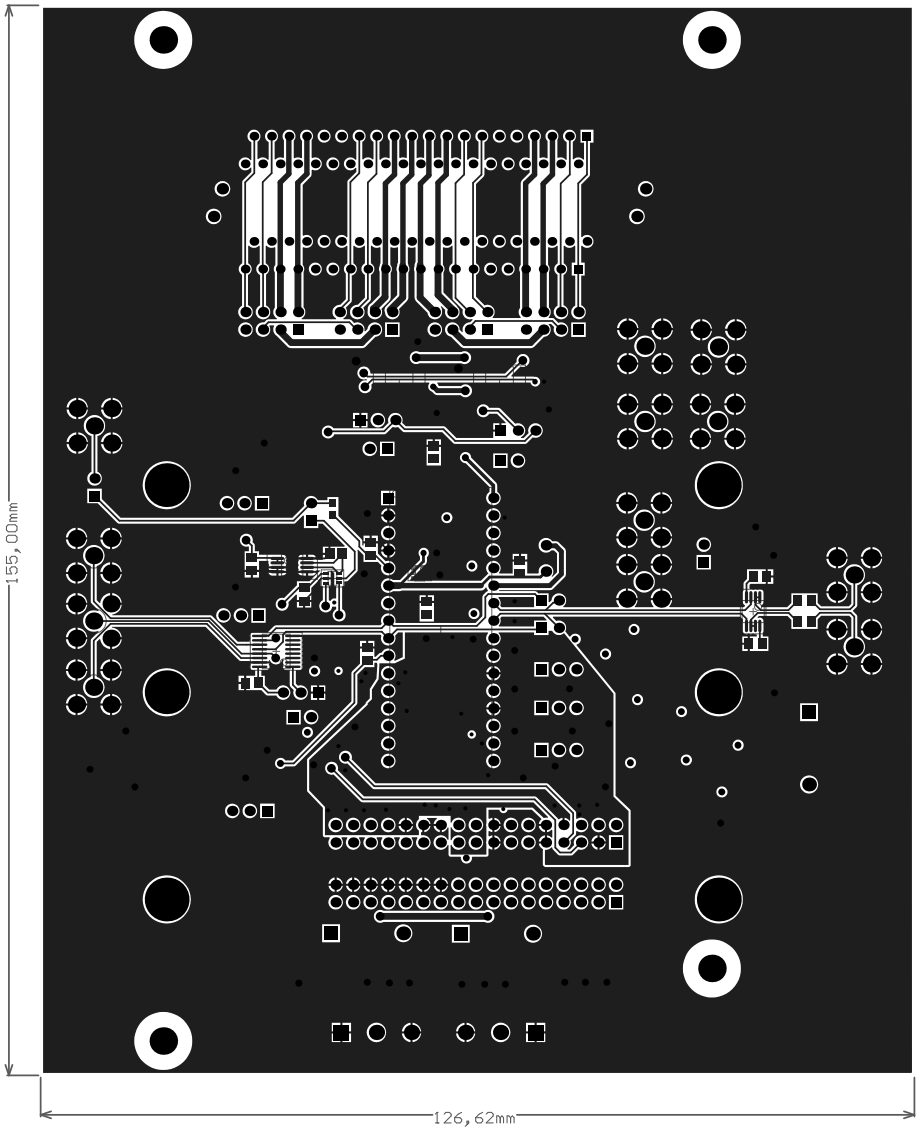


Figure B.7: Layout of the ADC PCB - Top (Final Artwork Print).

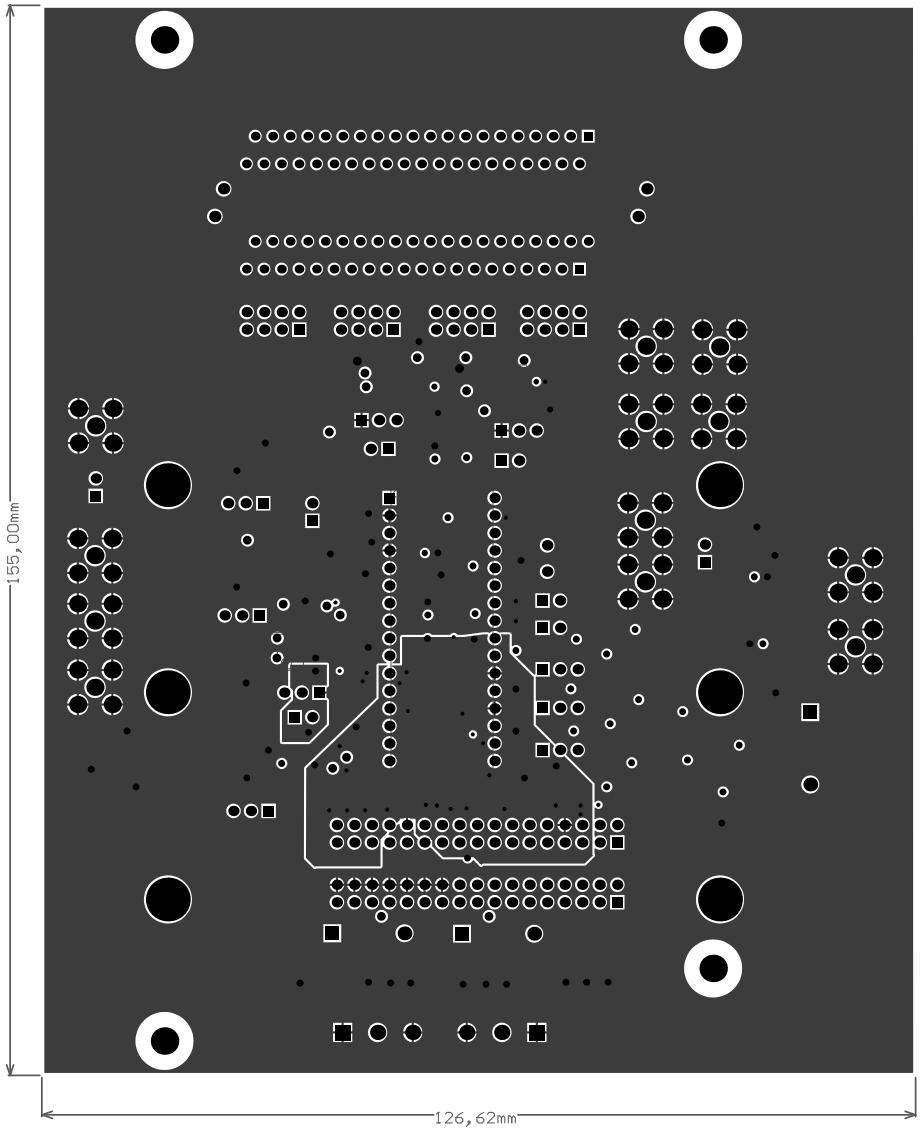


Figure B.8: Layout of the ADC PCB - Mid-Layer 1 (Final Artwork Print).

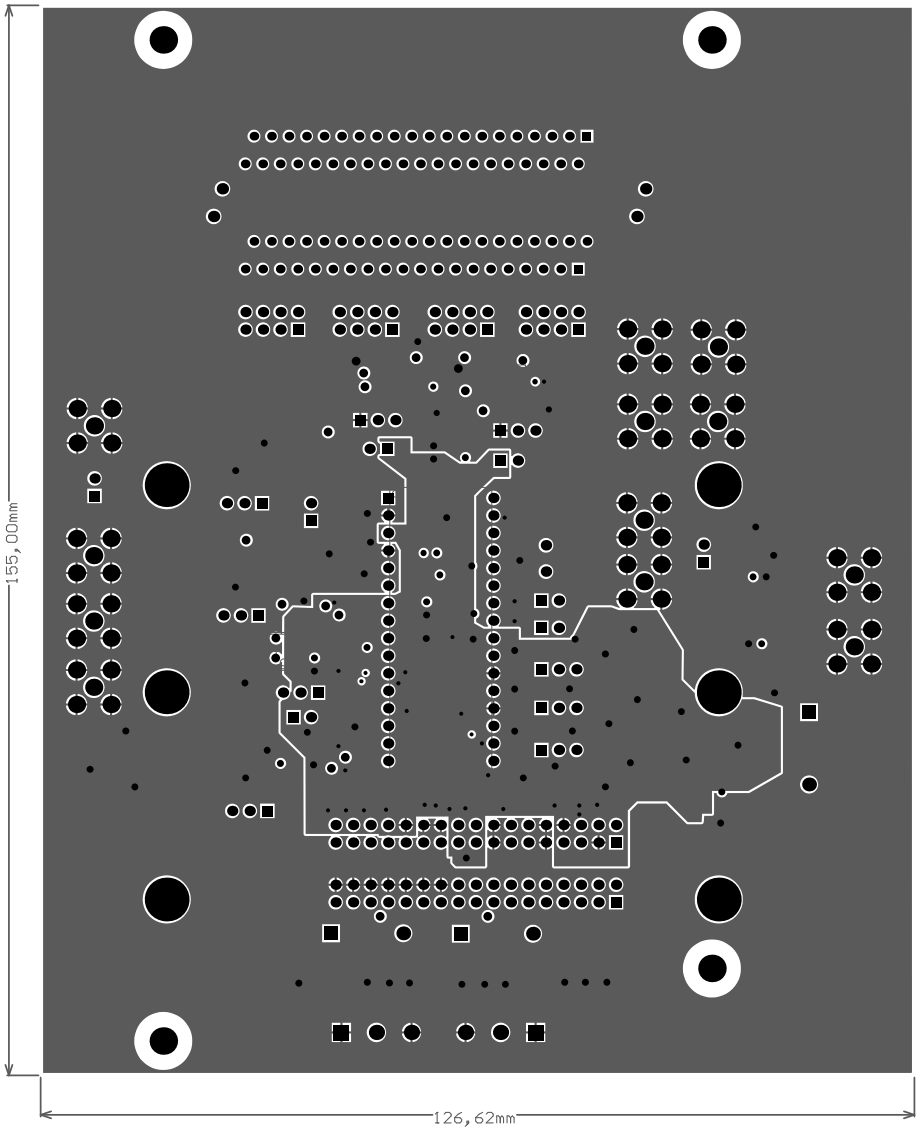


Figure B.9: Layout of the ADC PCB - Mid-Layer 2 (Final Artwork Print).

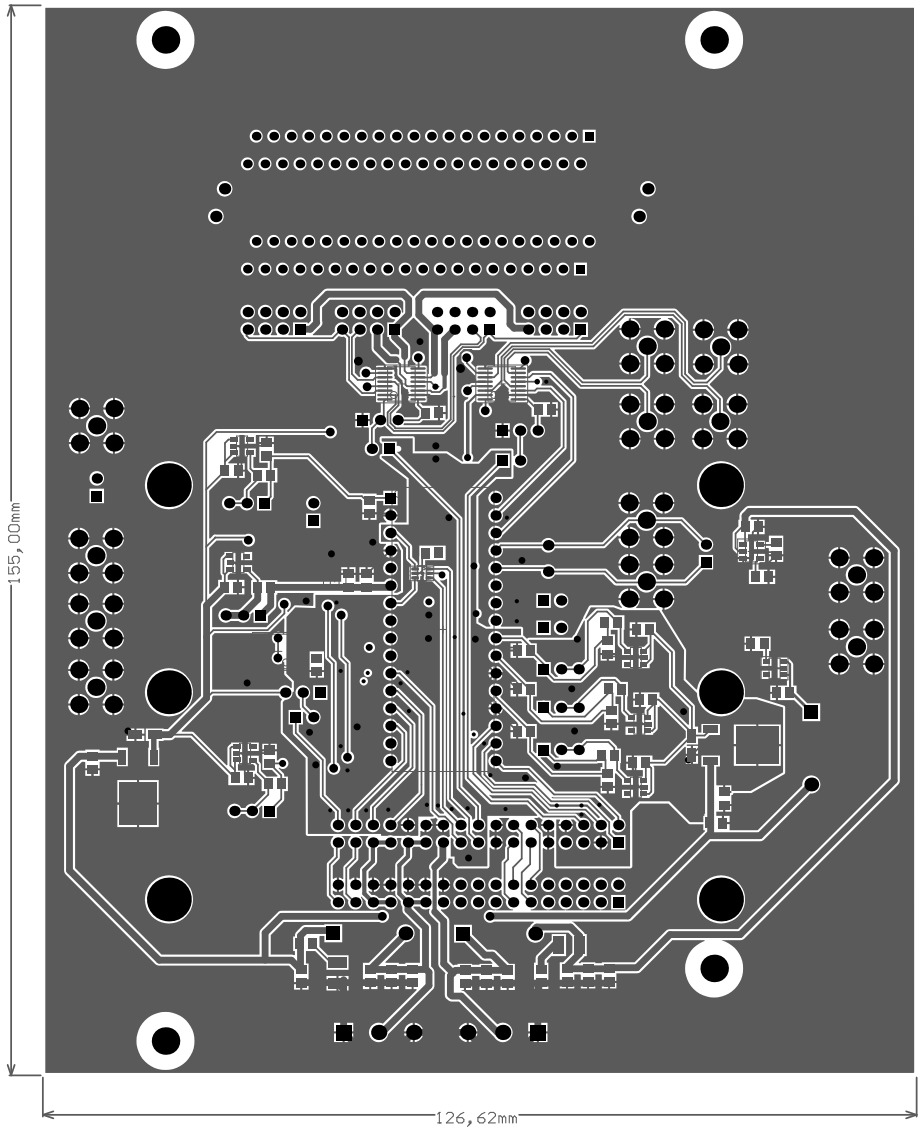


Figure B.10: Layout of the ADC PCB - Bottom (Final Artwork Print).

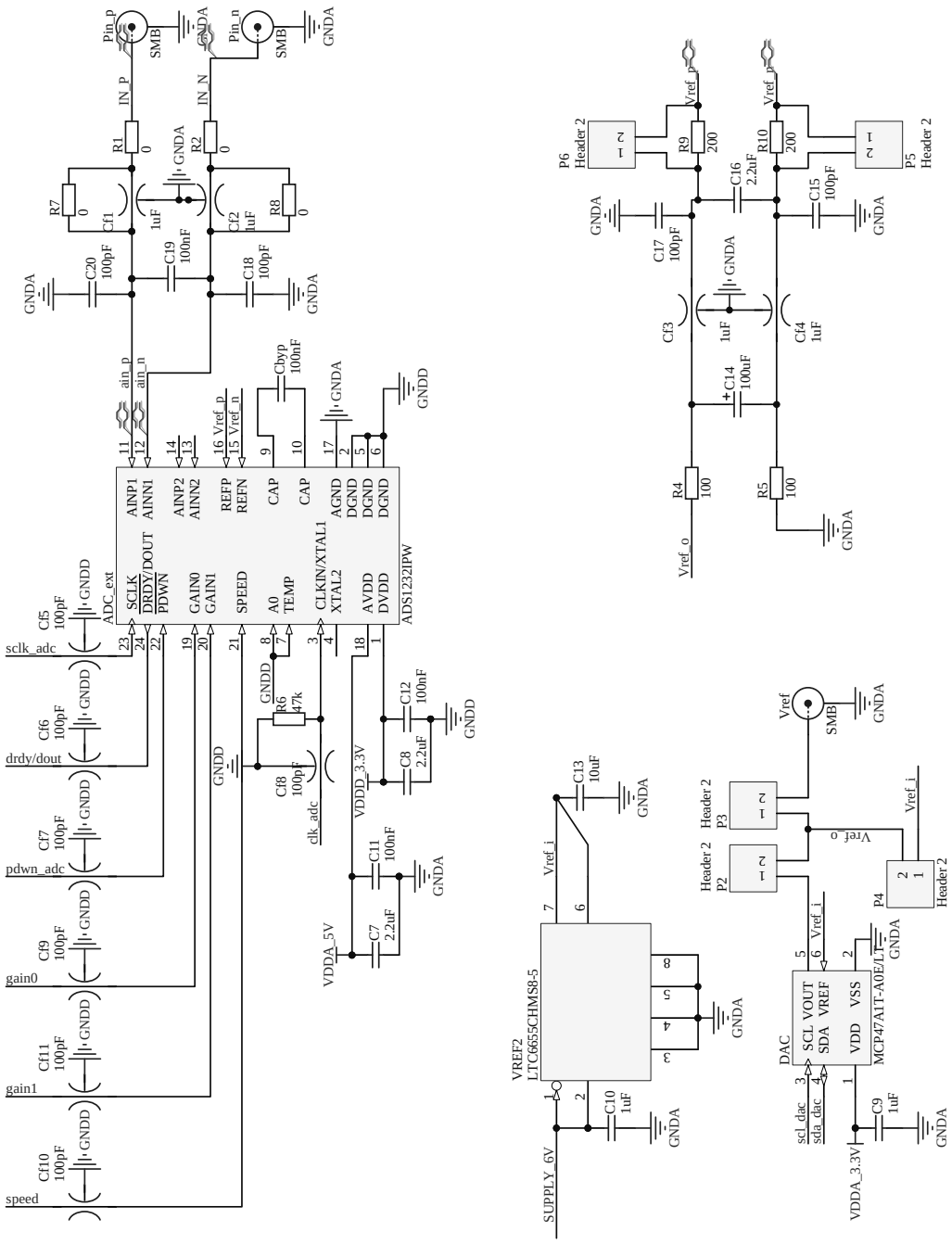


Figure B.11: Schematic of the ADC PCB (part 1).

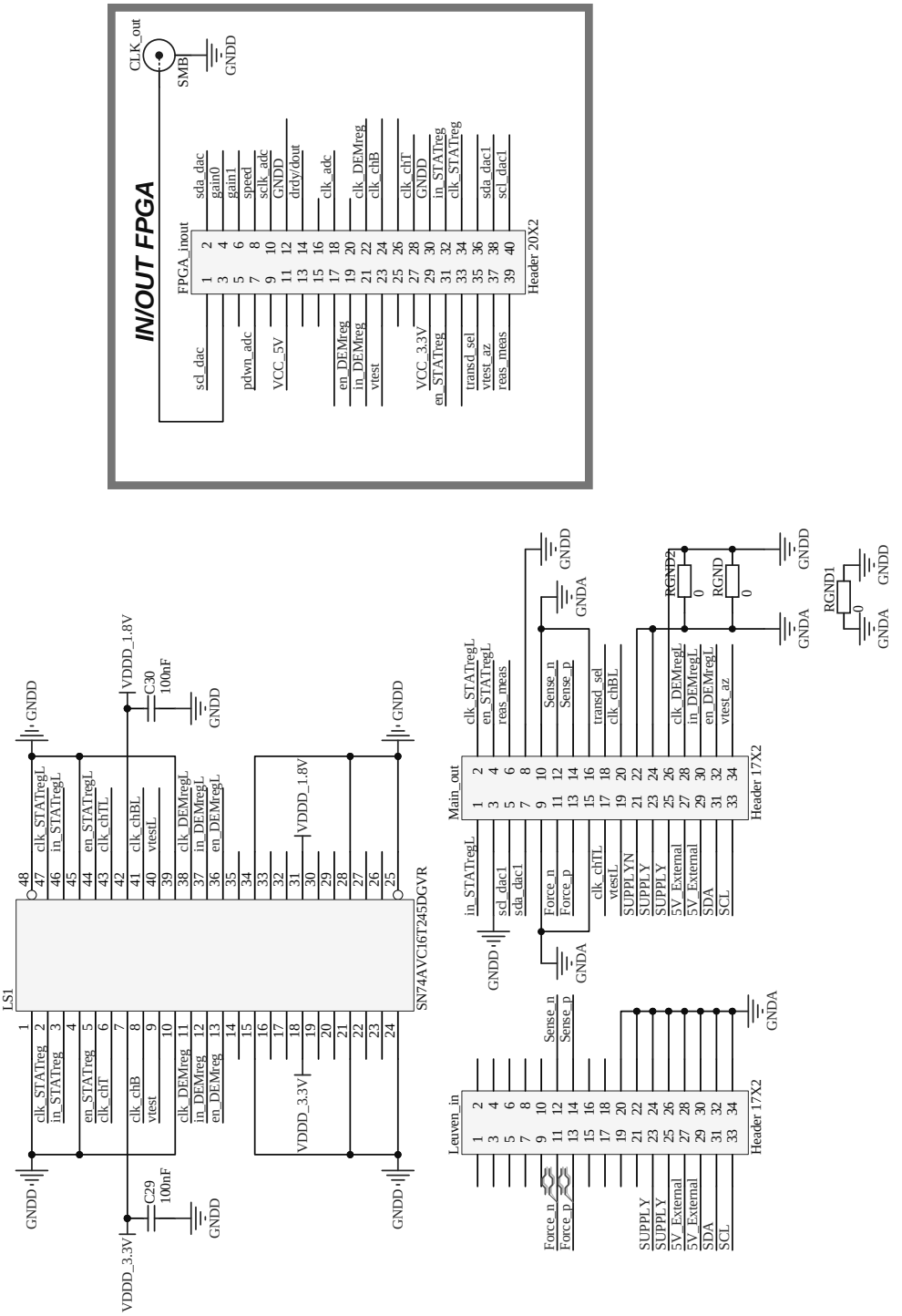
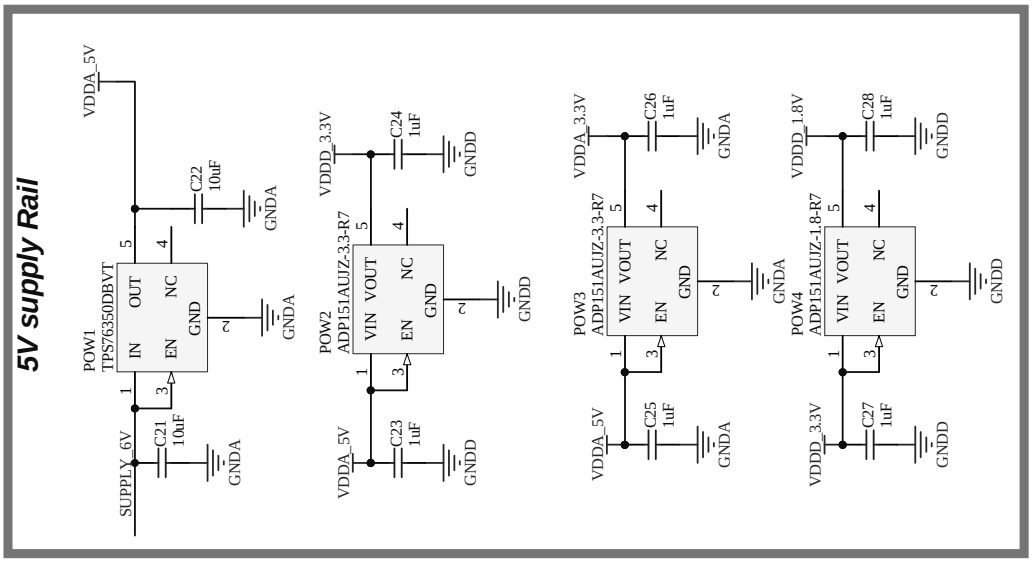


Figure B.12: Schematic of the ADC PCB (part 2).



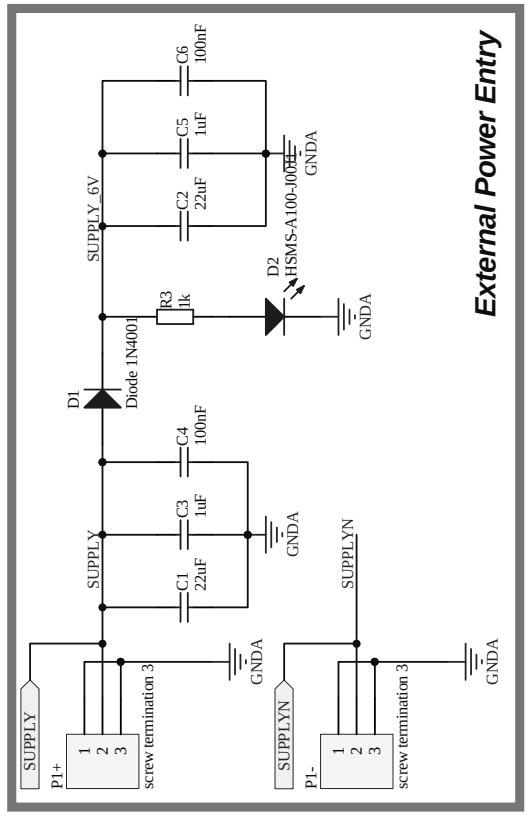


Figure B.13: Schematic of the ADC PCB (part 3).

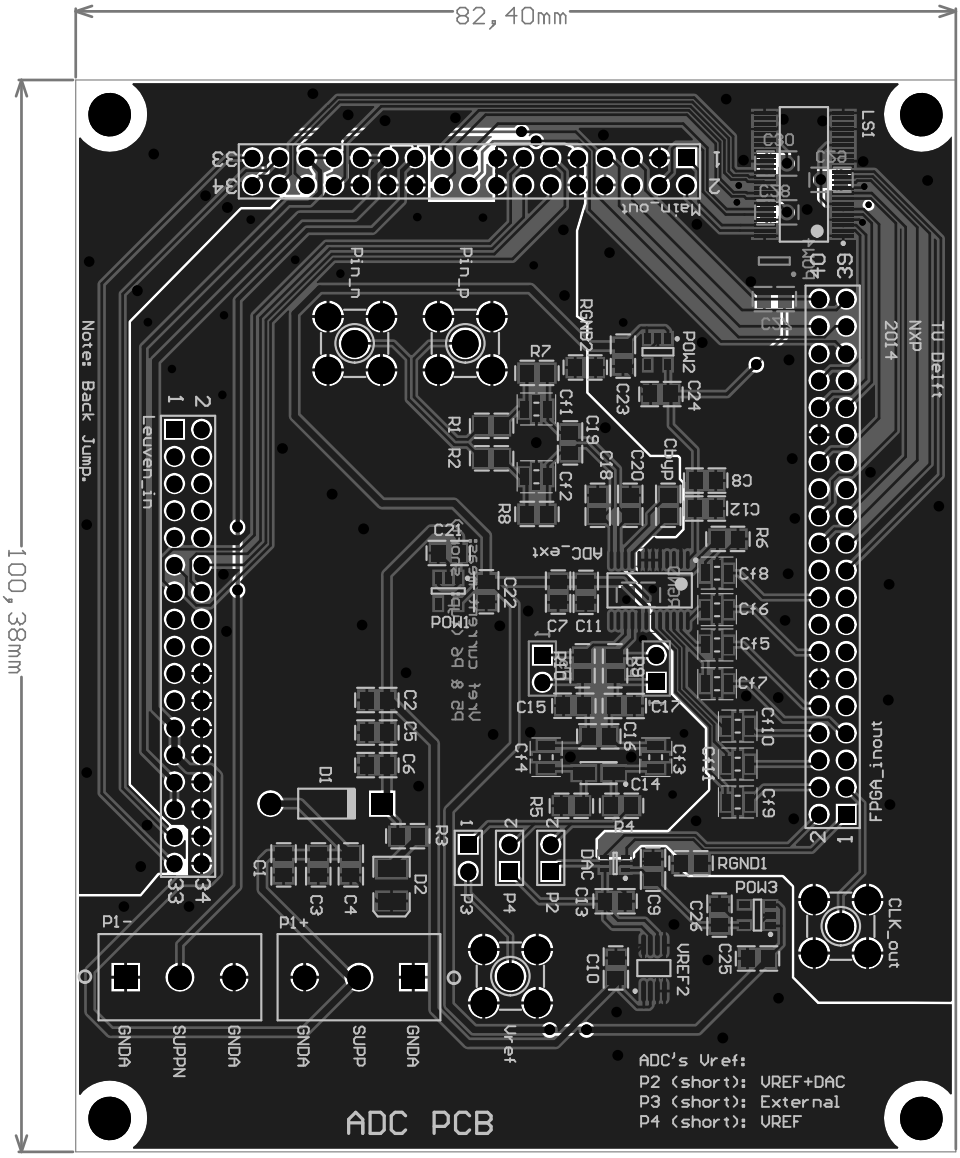


Figure B.14: Layout of the ADC PCB (Composite Drawing).

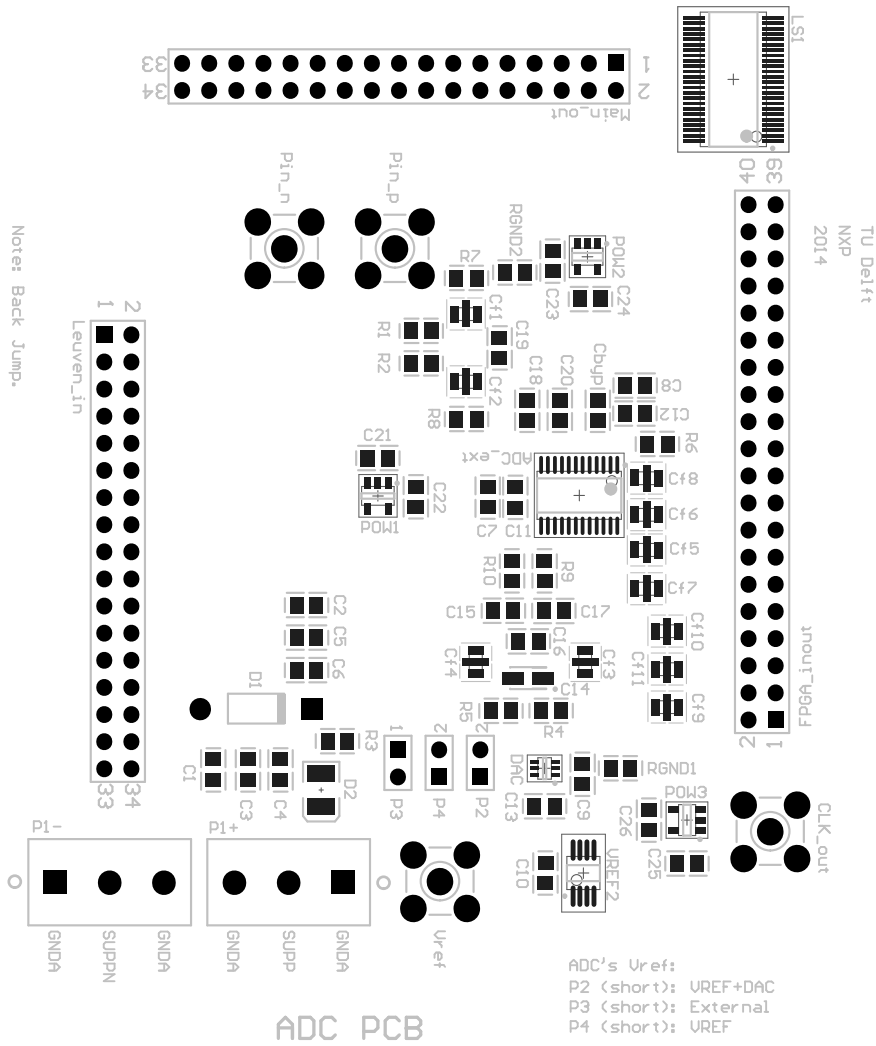


Figure B.15: Layout of the ADC PCB - Top (Assembly Drawing).

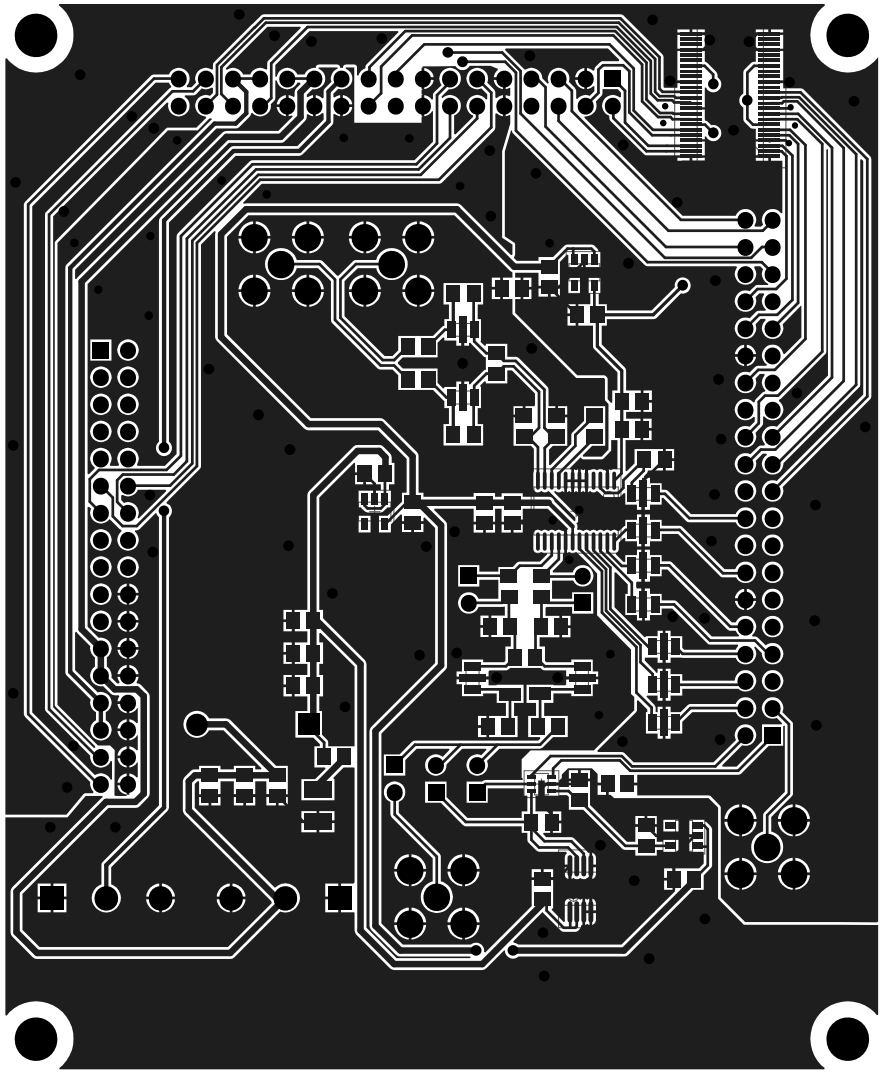


Figure B.16: Layout of the ADC PCB - Top (Final Artwork Print).

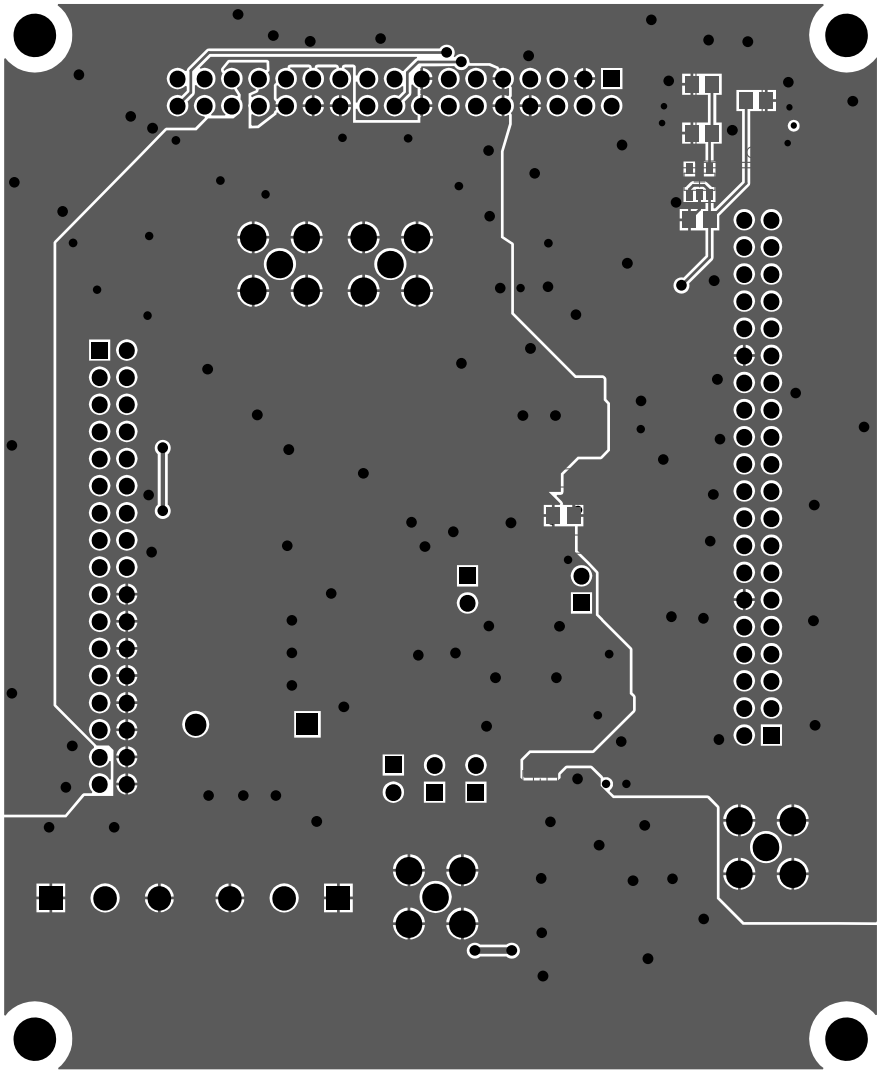


Figure B.17: Layout of the ADC PCB - Bottom (Final Artwork Print).

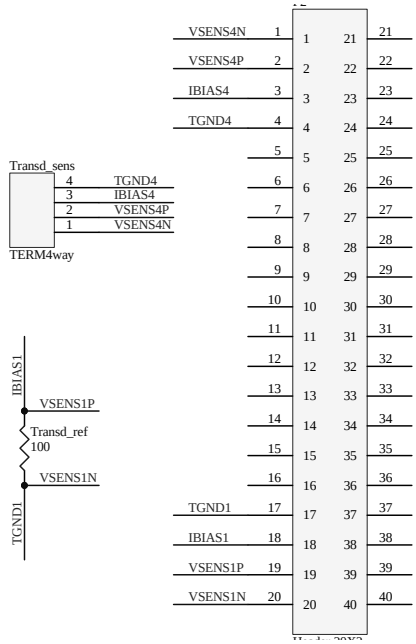


Figure B.18: Layout of the ADC PCB - Top (Final Artwork Print).

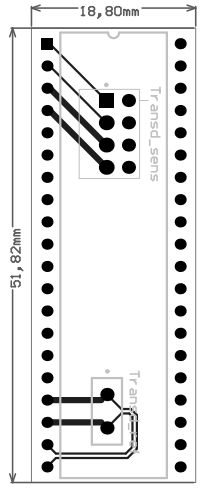


Figure B.19: Layout of the ADC PCB - Bottom (Final Artwork Print).

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