A 40.68-MHz, 200-ns-Settling Active Rectifier for mm-Sized Implants

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***Abstract*—This letter describes a fast-settling active rectifier for a 40.68 MHz wireless power transfer receiver for implantable applications. Fast-settling and low power are achieved through a novel direct voltage-domain compensation technique. The rectifier maintains high efficiency during load and link variations required for downlink communication. The system was fabricated in 40nm CMOS and achieves a voltage conversion ratio of 93.9% and a simulated power conversion efficiency of 90.1% in a 0.19 mm^2 area, resulting in a 118 mW/mm^2 power density while integrating the resonance and filter capacitors. The worst-case settling of the ON- and OFF-delay compensation in the active rectifier is 200 ns, which is the fastest reported to date.**

***Index Terms*—Active rectifier, adaptive delay compensation, biomedical implants, wireless power transfer (WPT).**

I. Introduction

Wireless power transfer (WPT) can reduce invasiveness in biomedical implants by eliminating the need for wires or batteries. Generally, these implants are limited by the power dissipated in the surrounding tissue, requiring careful design of the power management unit (PMU). Typically, the PMU implements a rectifier followed by a voltage regulator to provide a stable DC output. The rectifier stage is commonly implemented using comparator-based active structures to achieve high power conversion efficiency (PCE). These active rectifiers require adaptive ON/OFF delay compensation, rather than fixed delay schemes, to maintain optimal PCE under varying input and loading conditions [1], [2], [3], [4], [5], [6]. Adaptive delay compensation is generally accomplished with a feedback loop that consists of a sampling circuit and an error amplifier. The delay is then compensated with a delay line or by introducing offset into a zero-crossing comparator proportional to the error amplifier output (Fig. 1). To ensure system stability, the amplifiers are intentionally designed with low bandwidth [2], [3], [4], [7], [8], [9]. However, this low bandwidth inherently limits their response time during fast input or load variations. This is even more critical in implants where amplitude shift-keying (ASK) is used to transmit down-link data on the power carrier [1].

This letter presents an active receiver (RX) rectifier with rapid ON/OFF adaptive delay compensation for a 40.68 MHz inductive WPT. The rectifier design implements a novel direct voltage-domain compensation and eliminates the need for a slow feedback control loop while maintaining high PCE under fast input or load variations. The high resonance frequency enables on-chip integration of the RX resonance and filter capacitor, requiring only a coil as an external component. A prototype of the fast-settling rectifier achieved a measured voltage conversion ratio (VCR) of 93.9% and a simulated PCE of 90.1% that settles in less than 200 ns in a 0.19 mm^2 active area, which includes the resonant and filter capacitors.

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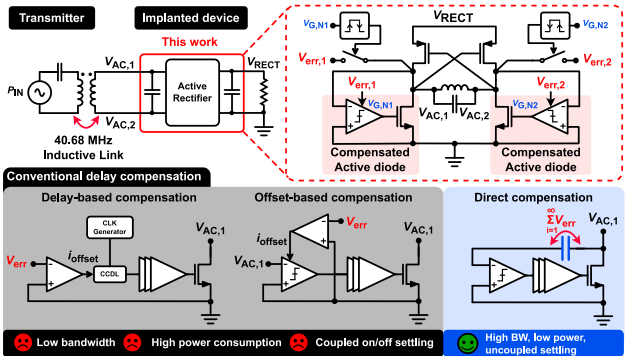

Fig. 1. System architecture of an active rectifier with conventional delay-compensation techniques and the proposed delay-compensation.

II. Active Rectifier With Delay Compensation

The delay compensation technique for the active rectifier in this work does not require a slow feedback control loop, as in previous works, to maintain system stability. Instead, it samples the error voltage (ΔV_S) at the switching instant and adds it in series to the input of the comparator to compensate for the delay directly [Fig. 2(a)]. This technique can achieve single-shot delay compensation in cases where a linear relationship exists between the comparator delay and the corresponding voltage in the AC input. The nonlinear relation between comparator delay and corresponding voltage error is what ultimately limits the maximum compensation speed. A few accumulation cycles are typically sufficient to account for the nonlinear relationship between the error voltage and the required comparator offset to fully compensate the delay (simulated worst-case settling < 200 ns). After system startup, this technique can continuously compensate for the delay in a single cycle (25 ns) over typical load and input variations (120 Ω–1 kΩ).

The delay compensation implementation is shown in Fig. 2(b) and (c), where each edge of the gate driving signals ($V_{GN,1}$, $V_{GN,2}$) has an independent compensation implementation. A sampling capacitor (C_S) captures the error voltage at the switching instance of the rectifier, which is then transferred to a compensation capacitor (C_C). A charge transfer circuit implements the sample-and-accumulate operation needed for the direct compensation technique using identical sampling and compensation capacitors. First, the polarity of the error voltage is determined to enable either the positive or negative charge-transfer current sources. Both capacitors are charged (discharged) in case of a negative (positive) voltage using nominally identical current sources. A zero-cross detector (ZCD) ends the charging period for both capacitors when the voltage in the sampling capacitor crosses 0 V. The result is that the charge in the sampling capacitor is added to the compensating capacitor—see the corresponding voltages V_S and V_C in Fig. 2(b) and (c). An additional safety circuit resets the compensation capacitor if it has an initial charge that disrupts the normal operation of the rectifier ($V_{G,N}$ is

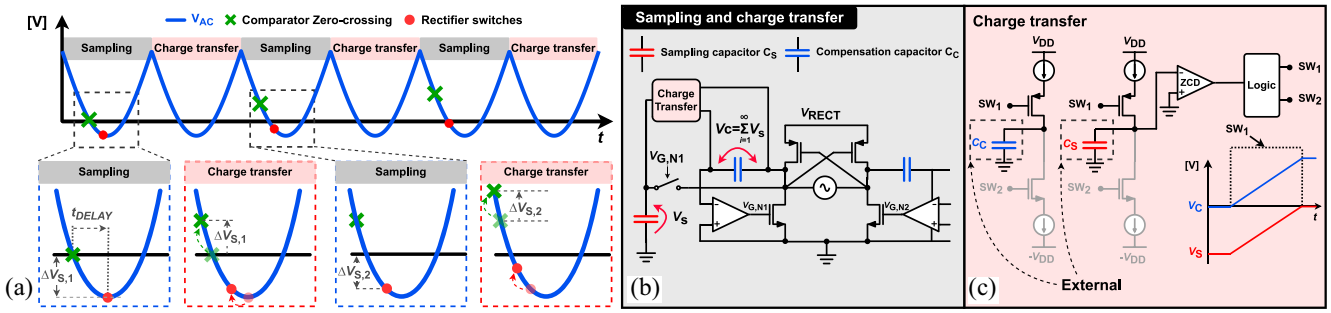

Fig. 2. (a) Proposed delay compensation, (b) simplified operation of the sample-and-accumulate, and (c) charge transfer process and transient waveforms of the voltage compensation.

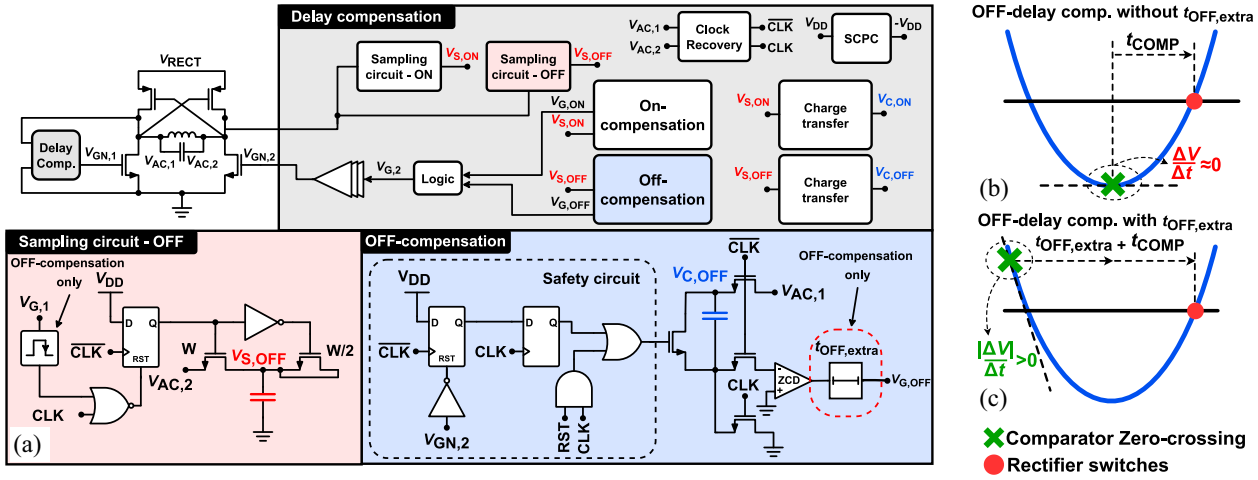

Fig. 3. (a) Schematic of the delay-compensated active rectifier with OFF-compensation circuitry shown in detail, (b) OFF-delay compensation without delay, and (c) OFF-delay compensation with additional delay.

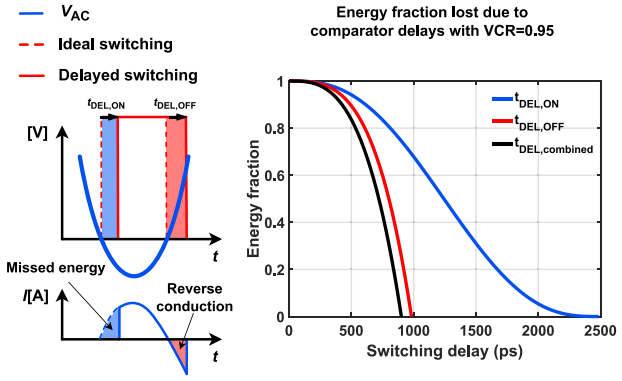

Fig. 4. Impact of comparator delay on rectifier efficiency.

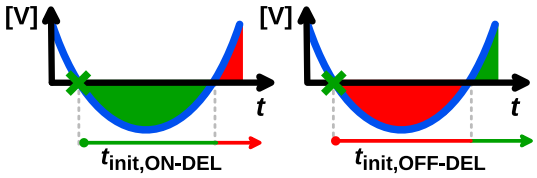

Fig. 5. Illustrated stability (green:stable, red:unstable) criterion for the initial delay of the ON- and OFF-compensation.

always 0). A detailed schematic of the delay compensation, including the safety circuit is shown in Fig. 3(a). The ZCD and the comparator for the active diode in the rectifier are implemented using auto-zeroed inverters [10]. Level shifters are used to switch the MOSFETs between the capacitors and the - V_{DD} rail and a switched-capacitor power converter (SCPC) generates - V_{DD} on-chip.

Setting identical compensation architectures for both ON- and OFF-delays would move the OFF-trigger point close to the trough of the AC input, where $(\Delta V/\Delta t)$ approaches zero, making the system sensitive to voltage errors [Fig. 3(b)]. To address this issue, the OFF-compensation scheme adds a delay line ($t_{OFF,extra}$), effectively shifting the OFF-trigger point to the same region as the ON-trigger point [Fig. 3(c)]. The compensation settles with a small residual delay < 200 ps Fig. 6(d), which is equivalent to <1% energy losses due to ON/OFF delay (Fig. 4).

The stability of the delay compensation scheme is guaranteed if there is negative feedback since the system implements proportional feedback. To maintain negative feedback, the sampled error voltage V_S must be negative (positive) for the ON (OFF) compensation at startup. This sets an upper (lower) bound on the initial uncompensated ON (OFF) delay—Fig. 5. For the ON compensation, the uncompensated comparator must trigger before V_{AC} reaches the second zero crossing to avoid sampling a positive error voltage V_S. For the OFF compensation, $t_{OFF,extra}$ needs to be large enough such that the delayed sampling instant happens after V_{AC} reaches the second zero crossing to avoid sampling a negative error voltage V_S. The

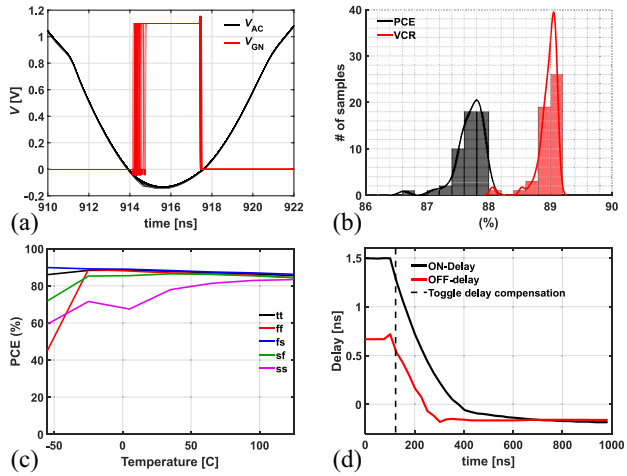

Fig. 6. Simulation results for, (a) Monte Carlo simulation for V_{GN} and V_{AC}, (b) Monte Carlo simulation for PCE and VCR, (c) PCE across corners and temperature, and (d) Post-layout simulated delay compensation settling speed on startup.

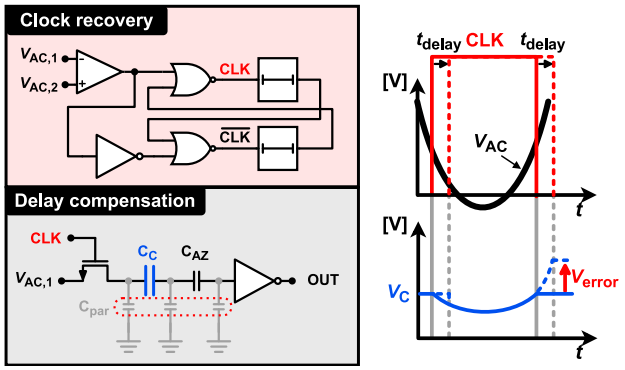

Fig. 7. Influence of clock-recovery delays and parasitic capacitances on the delay compensation scheme.

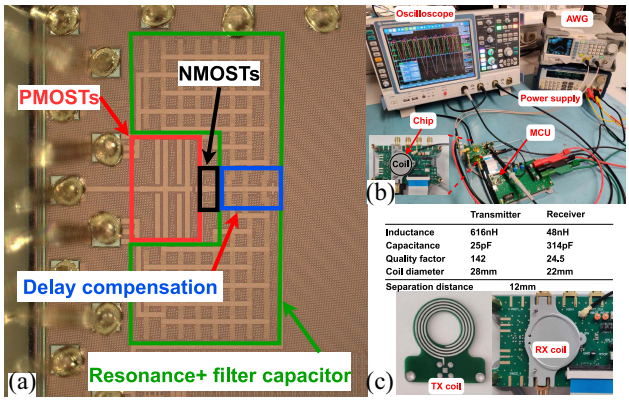

Fig. 8. (a) Chip micrograph, (b) Measurement setup in steady-state, and (c) Measured link parameters.

compensation capacitors C_C are reset in case of a runaway scenario using a safety circuit [Fig. 3(a)].

Post-layout simulations results of the active rectifier, including the on-chip resonance- and on-chip filter-capacitor, show that the overall system is sensitive to process variations in post-layout simulations (Fig. 6). The transient waveforms and PCE and VCR performance in Monte Carlo simulations and the PCE in process corners and

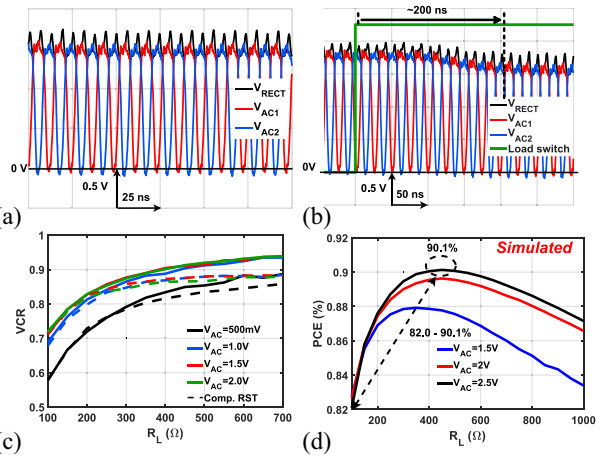

Fig. 9. Measurement results for, (a) steady state transient, (b) stepped load from 600 Ω to 300 Ω transient, (c) VCR versus R_L, and (d) Simulated PCE versus R_L.

over a –55–125° C temperature range are shown in Fig. 6(a)–(c), respectively, for V_{AC} = 1.5 V and R_L = 300 Ω. The degradation in performance for the slow-slow (ss) corner and some Monte Carlo runs are primarily caused by the implementation of the clock-recovery circuit. A delay or offset in the clock with respect to the ideal trigger point ($V_{AC} = 0$) impacts the delay compensation due to the parasitic capacitances in the compensation scheme. This effect is illustrated in Fig. 7 where it can be observed that an asymmetric switching of the compensation capacitor C_C between the compensation phase and charge transfer phase causes an offset that cannot be corrected in the current system. The clock recovery circuit consumes only 3 μW in the current design. A future implementation can allocate more power to account for PVT-induced variations. Finally, the simulated worst-case settling of the full system, from noncompensated to compensated, is shown in Fig. 6(d).

III. Measurement Results

The proposed design was fabricated in a 40 nm CMOS process, occupying a chip area of 0.19 mm^2. The measurement setup consists of a 616 nH PCB inductor and tunable capacitors driven by a power amplifier IC on the TX side, while an RX board containing the wire-bonded ASIC completes the link (Fig. 8). High-speed buffer ICs (LMH6559) were used to minimize parasitic loading and reduce interference from the inductive fields when measuring the AC signals in the link. The steady-state and settling behavior of the measured system are shown in Fig. 9(a) and (b). The active rectifier was co-designed with an SCPC. Therefore, the settling behavior was tested under the assumption of an external V_{DD}. The waveforms shown are of the standalone rectifier, with the integrated 500 pF output capacitance, leading to increased output ripple compared to an SCPC-connected scenario.

Rapid settling of the output can be observed with a load change from 600 Ω to 300 Ω. The output pole formed by the capacitance of the on-chip filter and the load (RC = 150 ns) limits the settling of the rectifier and is consistent with the measurement results. It can be concluded that the compensation loop is likely faster, or as fast, as the observed settling. The delay compensation circuitry consumes only 130 μW. The measured VCR shows a peak value of 93.9% with a 700 Ω load [Fig. 9(c)]. The PCE could not be measured due to complexities introduced by the on-chip capacitor and the UART communication interface, which made

TABLE I
COMPARISON WITH STATE-OF-THE-ART DESIGNS

	This work	[5] Lu,TBioCAS'14	[13] Pal,TCAS-II'20	[8] Luo,JSSC'23	[14] Luo,JSSC'24	[6] Ahn,TBioCAS'24
Technology	**40 nm**	350 nm	130 nm	180 nm	65 nm	250 nm
Frequency	**40.68 MHz**	13.56 MHZ	40.68 MHz	40.68 MHz	40.68 MHz	13.56 MHz
Total area	**0.19 mm2**	0.186 mm2	0.166 mm2	1.488 mm2	0.74 mm2	1.86 mm2
Output capacitance	**500 pF (On-chip)**	1.5 nF (External)	500 pF (External)	1.8 nF (On-chip)	220 nF + 470 nF (External)	3.2 nF (On-chip) +33 nF (External)
On-chip resonant cap	**Yes, 314 pF**	No	No	No	No	No
VCR (RL=500)	**92.0%**	89.0%	97.0%	96.3%	-	≈95.5%
Peak VCR	**93.8%**	93.0%	97.0%	96.3%	-	96.3%
Delay compensation	**ON/OFF (adaptive)**	ON/OFF (non-adaptive)	ON/OFF (non-adaptive)	ON/OFF (adaptive)	ON/OFF (adaptive)	ON/OFF (adaptive)
VAC Range	**0.5-2.5 V (External VDD)**	1.5-4.0 V	1-1.5 V	1.9-3.8 V	-	1.7-2.6 V
PCE (Max.)	**90.1%***	90.1%	93.2%	86.0%	90.1%	93.5%
Output Power (Max.)	**22.5 mW**	24.8 mW	9 mW	207 mW	60.5 mW	18.7 mw
Power density	**118 mW/mm2**	133 mW/mm2	54.2 mW/mm2	139 mW/mm2	82 mW/mm2	10.1 mW/mm2
Settling time	**≈200 ns**	≈500 ns (sim.)	≈500 ns-2 µs	≈20 µs	-	9.8 µs

* Post-layout simulated result

single-ended probing and direct driving of the chip impossible. The simulated PCE is shown in Fig. 9(d), with a peak efficiency of 90.1%.

IV. CONCLUSION

This work introduces a novel direct voltage-domain delay compensation technique for active rectifiers. The rectifier achieves VCR and PCE comparable to the state-of-the-art, with a high power density across a wide AC input range and occupies only 0.19 mm^2 (Table I). This performance is achieved while integrating the resonant capacitor on-chip and achieving the fastest delay compensation settling in literature (worst-case settling < 200 ns).

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