Phase-shift Switching Algorithm For PUC5 Inverters

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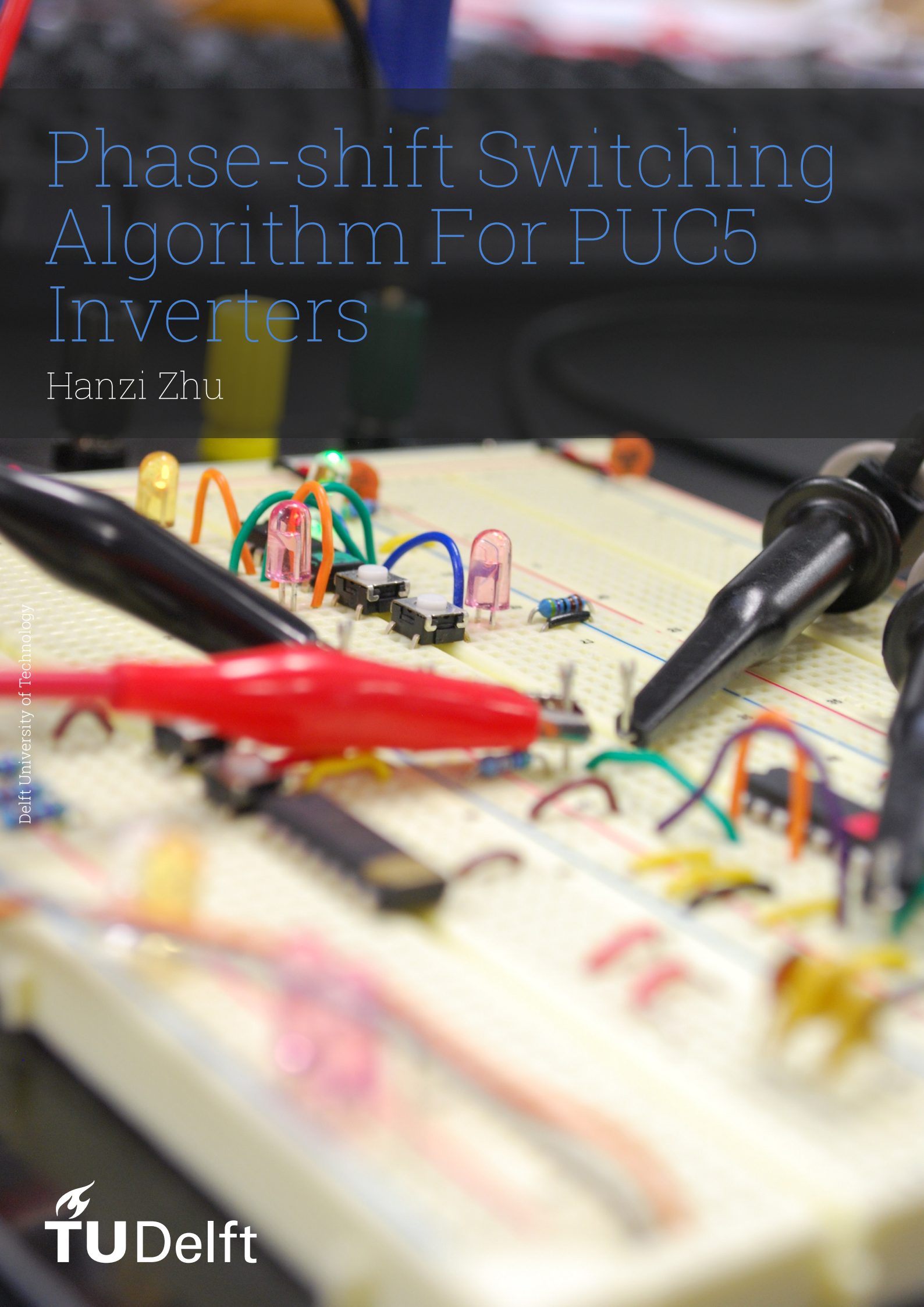

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by

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Preface

Multilevel inverters are widely used in industries for higher power applications due to low harmonic pollution and high efficiency. On the other hand, the phase-shift switching technique is well-known for its harmonic mitigation performance. However, phase-shift switching has not been regularly implemented on multilevel inverters due to complexity at a higher number of levels and difficulty in voltage balancing of the auxiliary capacitors in the configuration. In this project, the five-level Packed U-Cell inverter (PUC5) will be investigated to design and implement a phase-shift switching technique with an integrated voltage balancing algorithm. The developed technique will be implemented on the real-time simulator and hardware setup.

A literature review will be done on phase-shift switching algorithms and multilevel inverters. Afterward, a phase-shift switching algorithm with an integrated voltage balancing technique will be developed for the PUC5 inverter and simulated in Simulink. Hardware-in-the-loop (HIL) will be done using Opal-RT devices.

Hanzi Zhu
Delft, July 2024

Contents

1

Introduction

1.1. Motivation

Multilevel Inverters (MLI) are widely used in industries for higher power applications due to low harmonic pollution and high efficiency [1]. Therefore, they are widely utilized in energy conversion systems to enhance inverter efficiency and minimize the dimensions of output passive filters[2, 3, 4]. Among MLI topologies, Cascaded H-bridge (CHB), Neutral Point Clamped (NPC), and PUC5 are popular choices. Furthermore, the intricacy of control and modulation techniques for classic MLIs is significantly heightened with an increased number of voltage levels [5, 6, 7].

PUC5 inverter has many merits, including low complexity, modularity & scalability, and two redundant switching states to inherently regulate the auxiliary capacitor's voltage [8]. The classic PUC5 inverter is introduced in [9, 10, 11]. It regulates the capacitor voltage level at half of the DC voltage using the sensorless voltage balancing technique. However, this control method necessitates four level-shift (LS) triangular carriers. Besides, a switching states table is needed to generate switching signals. Additionally, one of the most important drawbacks of the PUC5 inverter with sensorless voltage balancing is that the output voltage ripple can not be ignored, which requires a matching large auxiliary capacitor to improve the output voltage quality. Due to the slow charging/discharging frequency and bulky auxiliary capacitor, the charging/discharging period is also significant. In [12], an LS-based modulation method aims to solve those issues. The proposed method uses two level-shift triangular carrier waves and logic gates. The number of triangular carriers is halved, and the switching states table is eliminated, resulting in a remarkable reduction in the complexity of the proposed modulation method. However, additional logic gates are introduced to generate appropriate pulses and perform the voltage balancing of the auxiliary capacitor.

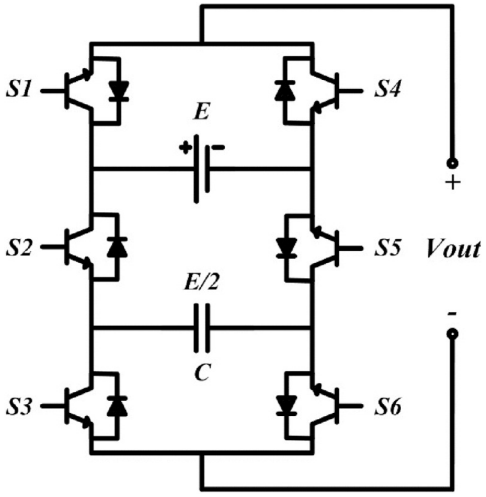

Figure 1.1: PUC5 Inverter topology

Although the phase-shift switching technique is well known for its harmonic mitigation performance, it has not been regularly implemented on multilevel Inverters due to the complexity at a higher number of levels and difficulty in voltage balancing of the auxiliary capacitors in the configuration [13, 14]. To further improve the performance of the PUC5 inverter, a phase-shift modulation method has been designed and implemented in [15] yet suffers the capacitor's slow voltage balancing and high voltage ripple. Thus, the goal of the project is to develop phase-shift switching algorithm with integrated fast voltage balancing for PUC5 converter.

1.2. Methodology and Objectives

A literature review will be done on multilevel inverters and switching algorithms. Afterward, a phase-shift switching algorithm with an integrated voltage balancing technique will be developed for PUC5 converter and simulated in Simulink. Hardware-in-the-loop (HIL) will be done using Opal-Rt devices. To conclude, the research objectives can be concluded as:

- Performing a literature review on phase-shift switching algorithms and multilevel inverters.
- Developing and applying a phase-shift switching algorithm with an integrated voltage balancing technique on the PUC5 inverter.
- Simulation and experimental test of the developed algorithm in the lab.

1.3. Thesis layout

Firstly, multilevel inverter topologies will be investigated and concluded in chapter 2. The report gives a thorough review of already existed MLI topologies and their pros and cons. Secondly, switching technologies will be discussed, and the report focuses on carrier-based modulation in chapter 3. Thirdly, improved PUC5 inverter switching technology will be discussed in chapter 4. The report will go through two existing improved PUC5 inverter switching methods, and propose a better one on top of predecessors' work. Finally, conclusion and future expectation will be discussed in chapter 6.

2

MLI topologies

Multilevel inverters, particularly in power electronics, offer several benefits over traditional two-level inverters. Many different multilevel inverter topologies have been invented and investigated. They can be classified in two main groups, as shown in Fig. 2.1, depending on the number of independent DC sources used in their structure. The most known and established topologies are the neutral point clamped (NPC), the cascaded H-bridge (CHB), and the Flying Capacitor (FC) inverters [16]. They are widely used in industry and already technically mature. A new topology with its special merits called PUC (Packed U-cell inverter) was introduced in [17]. In the beginning, it was introduced as a 7-level inverter [18]. After that, PUC5 was invented.

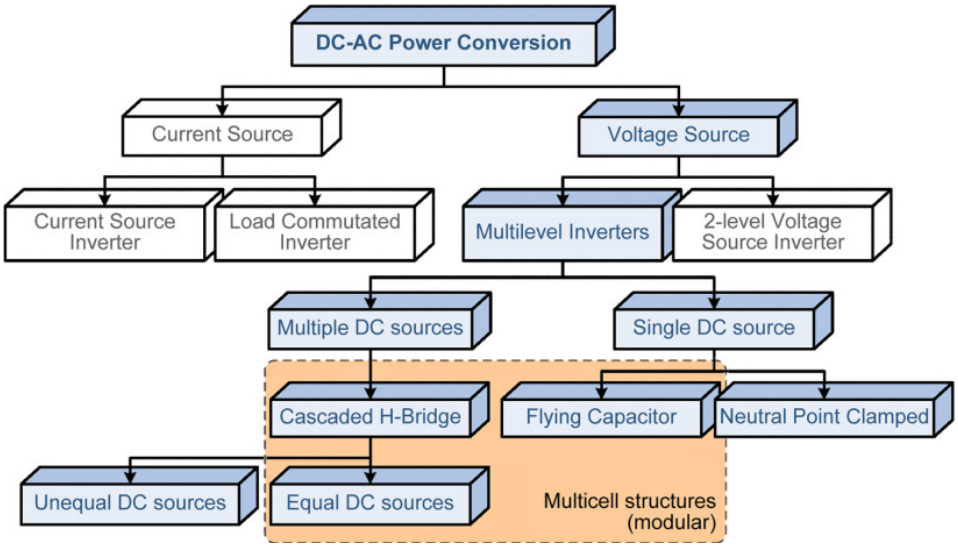

Figure 2.1: traditional classification of MLI [16]

This chapter will go through traditional MLI topologies, namely NPC, CHB and FC inverters. Then, PUC inverters will be discussed, from PUC7 inverter to PUC5 inverter. Switching methods will be introduced in the next chapter.

2.1. NPC inverter

A Neutral Point Clamped (NPC) inverter, also known as a diode-clamped multilevel inverter, is a type of multilevel power inverter that is widely used in high-power applications. It was first introduced in the 1980s and has since become a popular topology for converting electrical energy in various industrial and renewable energy systems. The key feature of a Neutral Point Clamped inverter is its ability to achieve higher voltage output with lower harmonic distortion compared to traditional two-level inverters. It achieves this by utilizing multiple voltage levels at its output, allowing for smoother and more sinusoidal waveform generation. Its general topology is shown as Figure 2.2 [19]. It's worth noticing that to differ from CHB inverter, its voltage level can be an either odd or even number.

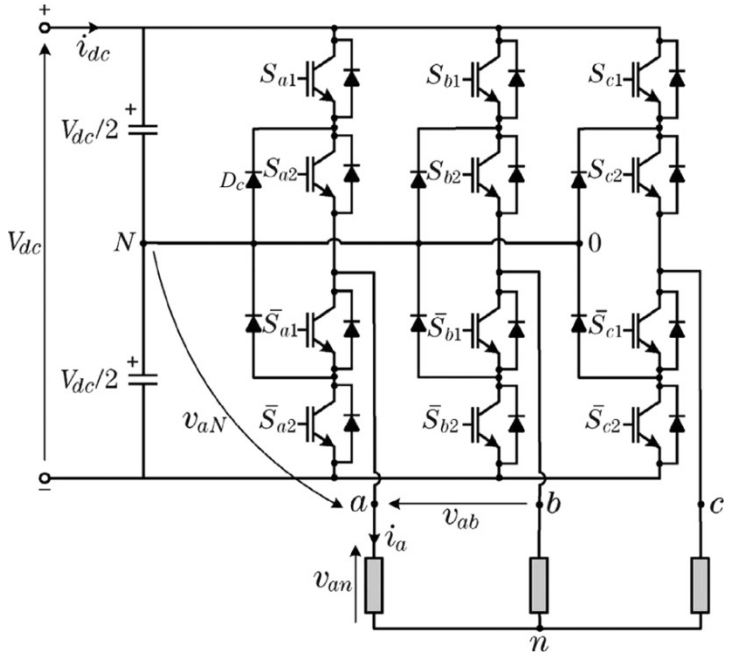

Figure 2.2: General topology of NPC inverter

The NPC multilevel inverter has a number of features and drawbacks, including

- More Redundant States.The term "Neutral Point Clamped" refers to the use of a midpoint or neutral point in the DC bus. This midpoint is clamped to a reference voltage, providing additional voltage levels and reducing the stress on the power semiconductors.
- Reduced Harmonic Distortion. The multilevel structure helps reduce the harmonic content in the output waveform, resulting in a more sinusoidal AC output. This is beneficial for applications where low harmonic distortion is crucial, such as in grid-tie inverters.
- Modularity and Scalability. The design of NPC inverters allows for modularity and scalability, making them adaptable to different power requirements.
- Increased Complexity. NPC inverters are more complex compared to traditional two-level inverters. The increased number of power semiconductor devices and the need for precise control strategies add complexity to the overall system.

2.2. CHB inverter

The Cascaded H-Bridge(CHB) Inverter stands as a sophisticated and versatile power electronics solution for high-voltage and high-power applications. This innovative inverter configuration is particularly well-suited for renewable energy systems, electric drives, and uninterruptible power supplies where precise voltage control and high efficiency are paramount.

At its core, the Cascaded H-Bridge Inverter comprises multiple H-Bridge modules connected in series, resembling a cascading structure. Each H-Bridge module consists of four power electronic switches, typically insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs), arranged in an H configuration. By varying the switching states of these switches, the inverter can generate a multilevel output voltage waveform, enabling better harmonic performance and reducing total harmonic distortion.

One of the distinctive features of the Cascaded H-Bridge Inverter is its ability to produce a stepped sinusoidal output voltage by combining the voltage levels of individual H-Bridge modules. This capability not only enhances the overall quality of the output waveform but also facilitates precise control of the output voltage, making it suitable for grid-tied applications and other situations demanding low harmonic distortion [20].

The advantages of the Cascaded H-Bridge Inverter include improved efficiency, reduced electromagnetic interference, and enhanced reliability due to its modular structure. Moreover, its scalability allows for customization according to the specific power requirements of diverse applications. Its topology is shown as Fig. 2.3.

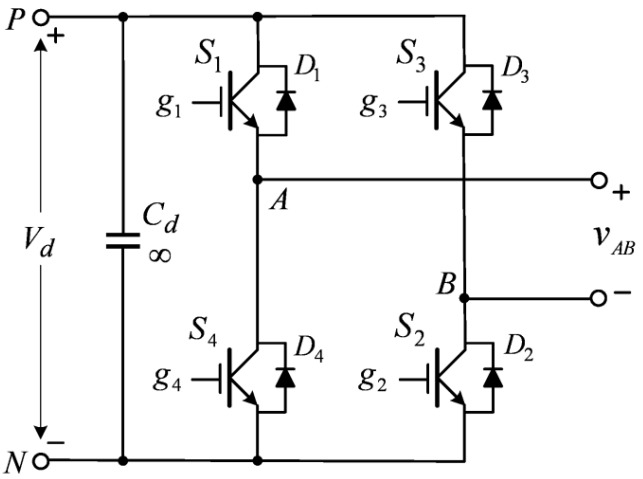

Figure 2.3: Topology of single-phase NPC inverter

Each topology shown in Fig. 2.3 is one cell in the multilevel CHB inverter. The number of voltage levels in a CHB inverter can be found from

$$m = 2H + 1 \tag{2.1}$$

Where H is the number of H-bridge cells per phase leg. And the voltage level mm is always an odd number. A single-phase seven-level CHB inverter is shown in Fig. 2.4.

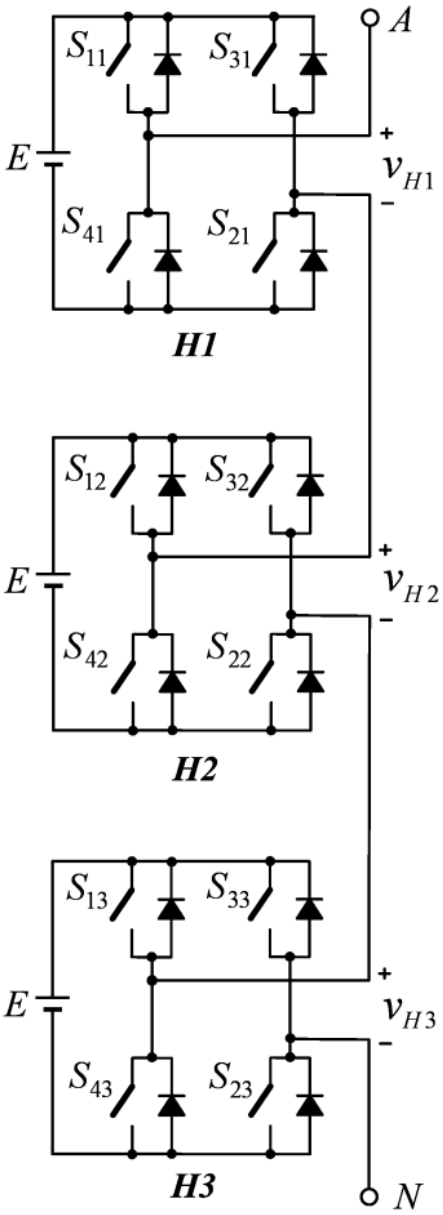

Figure 2.4: Topology of single-phase 7-level NPC inverter

Every module used in H-bridge circuit has independent source of DC voltage which are represented by E. All H-bridge cells output terminals are series connected, therefore, Equation 2.2 is utilized to get output voltage and Equation 2.3 is utilized to obtain number of levels in output voltage. In Equation 2.3, K represents the number of H - bridge cells, N represents the levels of output voltage.

$$V_{\text{out}}^{k} = \sum V_n = V_1 + V_2 + V_3 + V_4 \tag{2.2}$$

$$N = 2K + 1 \tag{2.3}$$

The CHB multilevel inverter has a number of features and drawbacks, including

- Modular structure.The multilevel inverter is composed of multiple units of identical H-bridge power cells, which leads to a reduction in manufacturing cost;

- Lower voltage THD and dv/dtdv/dt.The inverter output voltage waveform is formed by several voltage levels with small voltage steps. Compared with a two-level inverter, the CHB multilevel inverter can produce an output voltage with much lower THD and dv/dtdv/dt;
- High-voltage operation without switching devices in series.The H-bridge power cells are connected in cascade to produce high ac voltages. The problems of equal voltage sharing for series-connected devices are eliminated;
- Large number of isolated DC supplies.The DC supplies for the CHB inverter are usually obtained from a multipulse diode rectifier employing an expen sive phase shifting transformer;
- High component count.The multilevel CHB inverter uses numerous IGBT modules. A nine-level CHB inverter requires 64 IGBTs with the same number of gate drivers.

2.3. FC inverter

The Flying Capacitor (FC) inverter is similar to NPC inverter. Its general topology is shown in Fig. 2.5. The main difference between FC inverter and NPC inverter is that the clamping diodes in NPC inverter are replaced with capacitors. The zero voltage level cannot be directly generated. Instead, the zero voltage level is achieved by connecting the load to either the positive or negative rail through the flying capacitor, but with a polarity opposite to that of the DC link. Thus, though similarity in topology, it requires a different switching method. It's also worth noticing that different combination of switching can result in the same voltage level. Such switching redundancy increases the flexibility of the whole topology. [16]

Another important feature of FC inverter is its modular structure. It can achieve more voltage levels. Such modularity enables to see FC inverter as a MMC inverter for better performance [21].

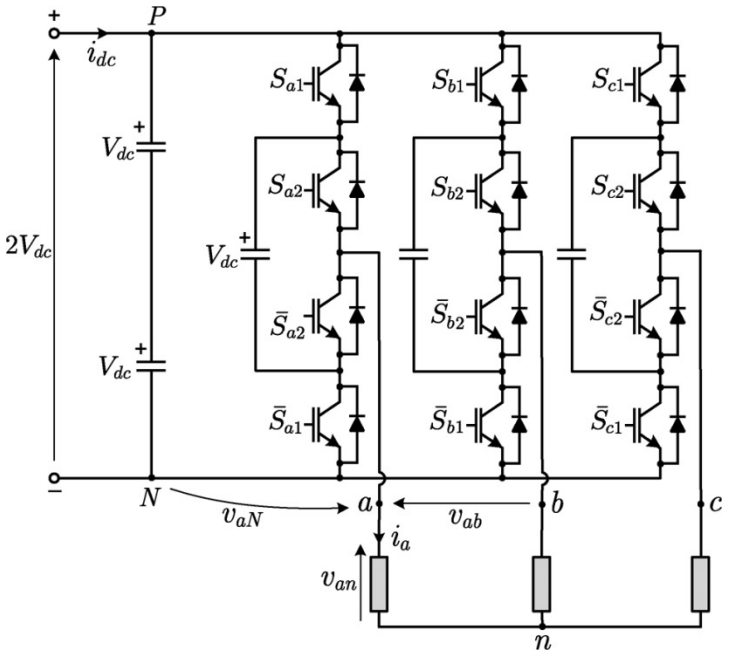

Figure 2.5: Topology of FC inverter

2.4. PUC inverter

PUC (Packed U-cell) topology was first introduced in [18]. It combines the advantages of the flying capacitor and the cascaded H-bridge topologies. The general topology of PUC inverter is shown in Fig. 2.6.

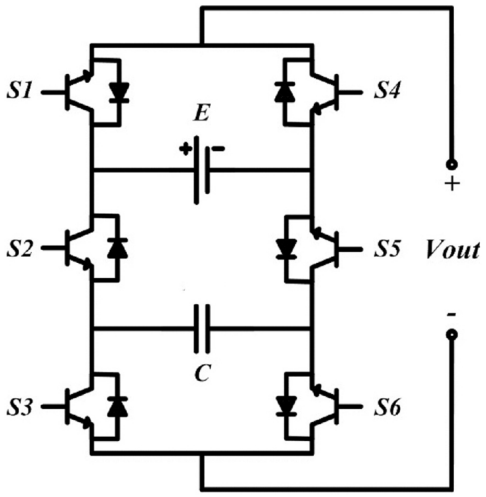

Figure 2.6: Topology of PUC inverter

With various axillary capacitor voltage level, two methods are most investigated, namely PUC5 and PUC7. By simply changing the ratio of capacitor voltage and DC voltage, the output voltage level varies as well. If the ratio equals 1/2, the output voltage level will be 5, which is PUC5 inverter. Similarly, if the ratio equals 1/3, the output voltage level will be 7, which is PUC7 inverter [22]. The output voltage level can be further extended by adjusting the ratio. However, the capacitor voltage balancing will be a serious issue as the output voltage level increases.

A significant benefit of PUC5 inverter is that its axillary capacitor is inherently balanced at 1/2 of the DC voltage level. Such sensorless voltage balancing character is much appreciated. Therefore, this report mainly studies PUC5 inverter.

The PUC multilevel inverter has a number of features and drawbacks, including

- Low Complexity. PUC inverters are simple which comprises fewer electrical components, compared with other topologies above.
- Modularity and Scalability. Just like NPC inverters, PUC inverters are adaptable to different power requirements.
- Redundant switching states Elimination the need for external voltage regulator of auxiliary capacitor decrease overall cost for the topology.

3

Switching technologies of MLI

Many different modulation algorithms have been adapted or developed depending on the application and the converter topology, each one having unique advantages and drawbacks. A classification of the most common modulation methods for multilevel inverters is presented in Figure 3.1. The modulation algorithms are here classified depending on the average switching frequency with which they operate, i.e., high or low. For high-power applications, high switching frequencies are considered those above 1 kHz.[23]

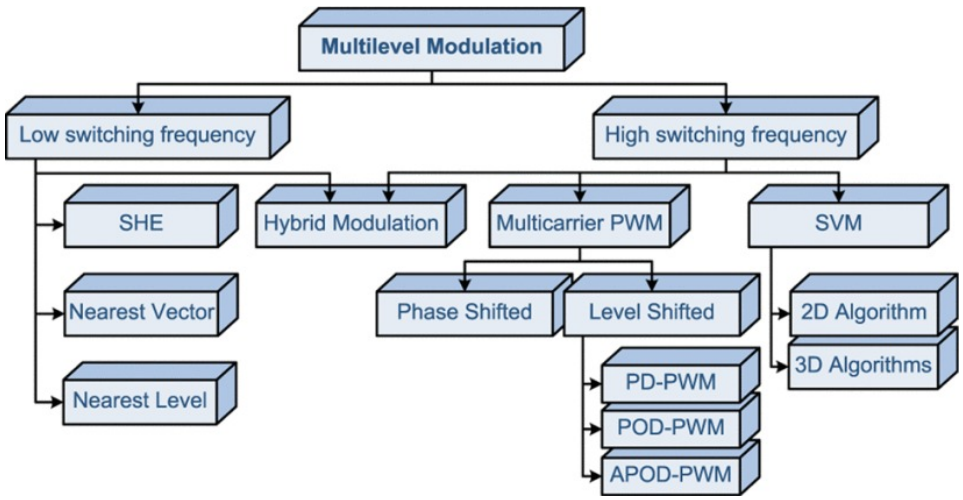

Figure 3.1: Switching techniques classified by switching frequency [16]

3.1. Selective Harmonic Elimination

Converters for very high-power application are usually controlled with low switching frequency algorithms, below 1 kHz. Selective Harmonic Elimination (SHE) is a technique in power electronics used to reduce or eliminate specific harmonics in the output waveform of inverters or converters. Harmonics, unwanted frequency components, can cause efficiency loss and interference. SHE selectively controls the switching times of power devices to cancel out specific harmonics, ensuring a cleaner, sinusoidal waveform. This is crucial in applications like motor drives and renewable energy systems where maintaining power quality is essential. SHE is implemented through mathematical optimization to find optimal switching angles, allowing engineers to tailor the harmonic content to meet standards and requirements.

Basically, in SHE, the Fourier coefficients or harmonic components of the predefined switched waveform with the unknown switching angles are made equal to zero for those undesired harmonics, while the fundamental component is made equal to the desired reference amplitude. This set of equations is solved offline using numerical methods, obtaining a solution for the angles. In 1973, the selected harmonic elimination method for PWM inverters was introduced for single-cell (two and three-level) inverters. This method is sometimes called a programmed PWM technique[24]. Then it was extended to multilevel series-connected PWM inverters as well[25]. Single-cell SHEPWM is illustrated in Figure 3.2.

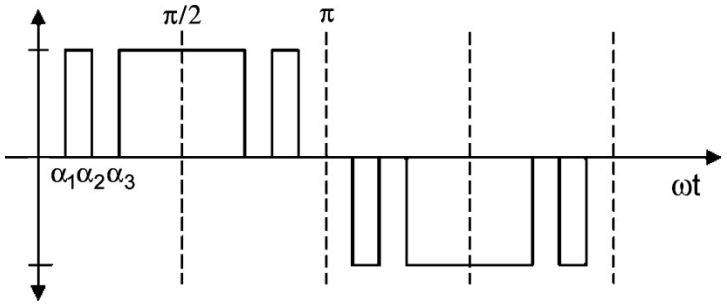

Figure 3.2: Waveform of single-cell SHEPWM

Owing to the symmetries in the PWM waveform, only odd harmonics exist. The Fourier coefficients of odd harmonics in triple-level programmed PWM inverters with odd switching angles are given by:

$$b_n = \frac{4E}{n\pi}\left[\cos n\alpha_1 - \cos n\alpha_2 + \ldots \ +(-1)^{j-1}\cos n\alpha_j + \ldots + \cos n\alpha_m\right] \tag{3.1}$$

where n is the harmonic order. Any m harmonics can be eliminated by solving m equations obtained in Equation 3.1. The correct solution must meet the condition:

$$0 < \alpha_1 < \alpha_1 < \ldots < \alpha_m < \frac{\pi}{2} \tag{3.2}$$

For a double-cell series-connected PWM inverter, each cell of the inverter switches m times per quarter cycle and produces a three-level {-1,0,1} PWM waveform, which results in a five-level inverter output {-2,-1,0,1,2}. Theoretically, $2m-2$ odd harmonics can be eliminated from the inverter's spectrum while keeping the fundamental components of both cells equal to each other. Even harmonics are not present due to the PWM waveform symmetry [25]. The switching angles must be obtained from the following system of 2m nonlinear transcendental equations:

$$\begin{gathered}\sum_{i=1}^{m}(-1)^{i+1}\cos\alpha_i = \frac{\pi}{4}M \\ \sum_{i=1}^{m}(-1)^{i+1}\cos\beta_i = \frac{\pi}{4}M \\ \sum_{i=1}^{m}(-1)^{i+1}\cos 3\alpha_i + \sum_{i=1}^{m}(-1)^{i+1}\cos 3\beta_i = 0 \\ \cdots \\ \sum_{i=1}^{m}(-1)^{i+1}\cos(4m-3)\alpha_i + \sum_{i=1}^{m}(-1)^{i+1}\cos(4m-3)\beta_i = 0\end{gathered} \tag{3.3}$$

where α_i's are the switching angles of the first cell, β_i's are the switching angles of the other cell, and M is the modulation index. The proposed model explicitly requires an even fundamental power sharing among cells. Convergence of numerical procedures used to solve 3.3 depends greatly on starting values of switching angles and requires a lot of computational power.

A reduced order Model is mentioned in [26]. Elimination of low order harmonics from only one cell, which will be called a general SHEPWM method, can be obtained by solving a system of m equations:

$$\begin{gathered}\sum_{i=1}^{m}(-1)^{i+1}\cos\alpha_i = \frac{\pi}{4}M \\ \sum_{i=1}^{m}(-1)^{i+1}\cos 3\alpha_i = 0 \\ \cdots \\ \sum_{i=1}^{m}(-1)^{i+1}\cos(2m-1)\alpha_i = 0.\end{gathered} \tag{3.4}$$

The first significant surplus harmonic from this cell has an amplitude $A_{2m}+1$.To eliminate $A_{2m}+1$ from the output spectrum of the inverter, the other cell must produce the $2m+1$ harmonic of an amplitude -$A_{2m}+1$. To preserve elimination of $2m-1$ low-order odd harmonics and to set the amplitude of the $2m+1$ harmonic to -$A_{2m}+1$, the number of switching angles in the second cell must be increased by one to $m+1$. The switching angles of the second cell fulfill the following system of $m+1$ equations:

$$\begin{gathered}\sum_{i=1}^{m+1}(-1)^{i+1}\cos\beta_i = \frac{\pi}{4}M \\ \sum_{i=1}^{m+1}(-1)^{i+1}\cos 3\beta_i = 0 \\ \cdots, \\ \sum_{i=1}^{m+1}(-1)^{i+1}\cos(2m-1)\beta_i = 0 \\ \sum_{i=1}^{m+1}(-1)^{i+1}\cos(2m+1)\beta_i = -\frac{(2m+1)\pi}{4}A_{2m+1}.\end{gathered} \tag{3.5}$$

By solving 3.4 and 3.5, an approximate outcome is obtained by solving 3.3, with much less mathematical computing.

To conclude, SHE has the following features:

- Improved Power Quality: SHE helps in achieving a cleaner output waveform with reduced harmonic distortion, leading to improved power quality.
- Reduced Electromagnetic Interference (EMI): By eliminating or minimizing specific harmonics, SHE can contribute to reducing electromagnetic interference.

- High Calculation Demand: Even by using an approximate way to solve equations, the calculation is still demanding. The calculation may not converge.

3.2. Nearest Vector Control

Nearest Vector Control (NVC) is introduced in [27] and [28]. The basic idea is to take advantage of the high number of voltage vectors generated by a multilevel converter by simply approximating the reference to the closest voltage vector that can be generated in the plane, without even need of modulation. Therefore, this method is referred to as nearest vector control instead of modulation, since no time average approximation of the reference is performed.

For an 11-level multilevel inverter, the state-space vectors are illustrated in Figure 3.3. Each dot is one of the possible voltage vectors generated by the inverter; they are surrounded by hexagons that represent the boundary of the area in which they are the closest available vector. The red dashed line is the voltage space vector reference $\mathbf{v}_s^*$ trajectory through the complex plane. Hence, when the reference falls into a certain hexagon, the corresponding vector will be generated by the inverter. The selected vectors according to the illustrative example are highlighted in blue [23].

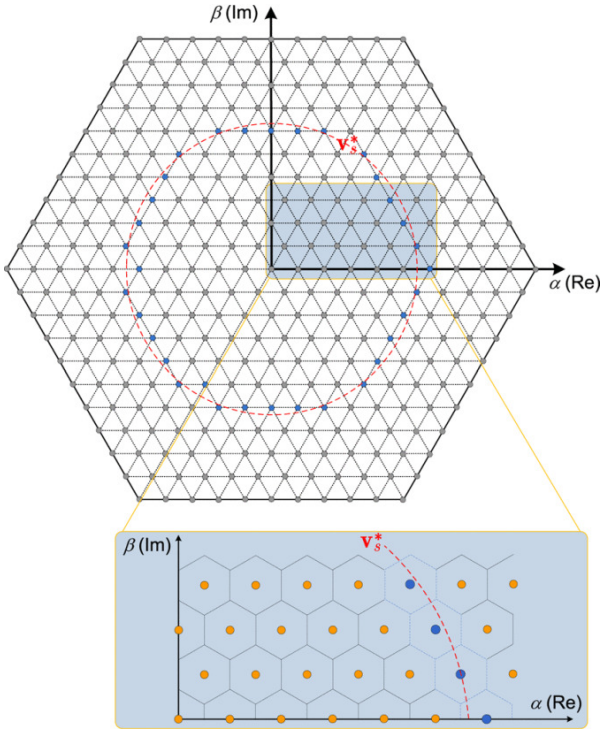

Figure 3.3: Multilevel nearest vector control operating principle [16]

To conclude, NVC has the following features:

- Reduced Commutations: No commutations are forced by a modulator. Thus, switching loss is reduced.
- Harmonics Problem: NVC does not remove low order harmonics, which reduce output quality.
- Limited Usage: NVC only applies to a high number of voltage levels (above 7). Otherwise, the application of the modulation method in a multilevel inverter with a lower number of levels would generate voltages and currents with high levels of distortion.

3.3. Nearest Level Control

To some extent, Nearest Level Control (NLC) is similar to Nearest Vector Control (NVC). It selects the nearest voltage level that can be generated by the inverter to the desired output voltage reference, instead of vectors. The three phases are controlled independently with their respective 120° phase shift. Unlike PWM methods, NLC methods eliminate the use of the triangular carrier wave, thereby allowing a lower switching frequency and simpler implementation. However, the conventional NLC method is especially suitable for an MMC with a relatively large number of SMs because this NLC scheme ensures adequate output quality. For MMCs with lower number of SMs, as are commonly used in medium voltage applications, the use of the conventional NLC method results in poorer quality waveforms than PWM strategies. In addition, as a direct modulation, the conventional NLC method does not include control of the circulating currents, thus resulting in a high root-mean-squared (rms) value of the circulating currents and a large SM capacitor voltage ripple [29]. The circuit configuration of the three-phase MMC is shown in Figure 3.4(a). Each phase leg of the MMC contains two arms with N identical series-connected half-bridge SMs per arm. Owing to the symmetry of the three-phase MMC, the analysis was carried out for each phase leg, as shown in 3.4(b).

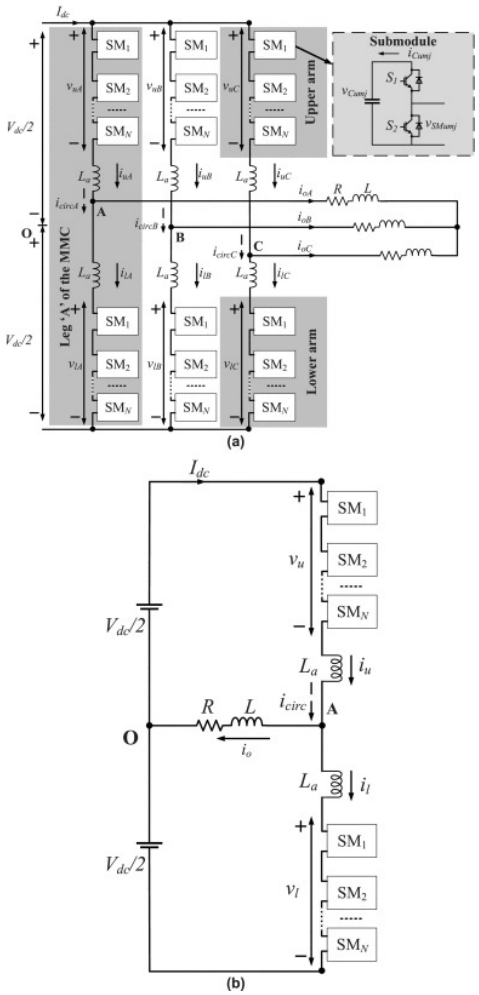

Figure 3.4: Circuit configuration of the MMC: (a) three-phase MMC and half-bridge SM; (b) single-phase MMC.

For the traditional NLC method, The upper and lower arm voltage references are first normalized by the nominal value of the SM capacitor voltage V_C^* ; then, the round function generates an integral number of inserted SMs corresponding to the nearest voltage level. The acquired number for the SMs is then sent to the voltage sorting algorithm, which generates the switching signals to operate the MMC. The numbers of inserted SMs in the upper and lower arms are calculated by:

$$\begin{aligned} N^*_{u_{-\text{final}}} &= \text{round}\left(N\frac{v^*_u}{V^*_C}\right), \\ N^*_{l_{-\text{final}}} &= \text{round}\left(N\frac{v^*_l}{V^*_C}\right), \end{aligned} \tag{3.6}$$

where

$$\begin{aligned} v^*_u &= \frac{V_{dc}}{2}\left[1 - \text{Mcos}\left(2\pi f_o t\right)\right] \\ v^*_l &= \frac{V_{dc}}{2}\left[1 + \text{Mcos}\left(2\pi f_o t\right)\right] \end{aligned}$$

To conclude, NLC has the following features:

- Easy Implementation: The traditional NLC is very easy to implement, for the algorithm is simple.
- Harmonics Problem: Although the voltage waveform is very similar to the one obtained with staircase modulation, it does not eliminate specific harmonics because it is not really a modulation. Just like NVC, harmonics reduce output quality.

3.4. Carrier-based Modulation

Generally, carrier-based modulation method can be divided into two categories: phase-shift modulation and level-shift modulation. For a multilevel inverter, to achieve m voltage levels requires $(m-1)$ triangular carriers.

3.4.1. phase-shift modulation for multilevel inverters

In phase-shift modulation, the carrier waves have the same frequency and the same peak-to-peak amplitude. The frequency modulation index $m_f = f_{cr}/f_m$ and the amplitude modulation index $m_a = \hat{V}_{mA}/\hat{V}_{cr}$ are identical among all carriers, where f_{cr} and f_m are the frequencies of the carrier and modulating waves, and $\hat{V}_{mA}$ and $\hat{V}_{cr}$ are the peak amplitudes of phase voltage and carrier voltage, respectively. But as its names suggests, a fixed phase shift exists between any two adjacent carrier waves, given by:

$$\phi_{cr} = 360°/(m-1) \tag{3.7}$$

For example, a 5-level inverter requires 4 carrier waves, whose adjacent phase shift is 90°. To better illustrate, 4 carrier waves are named as v_{cr1+}, v_{cr2+}, v_{cr1-}, and v_{cr2-}. Take v_{cr1+} and v_{cr1-} as one pair, while v_{cr2+} and v_{cr2-} as the other pair. [30].

The relationship between carrier waves and the reference wave is shown in Figure 3.5.

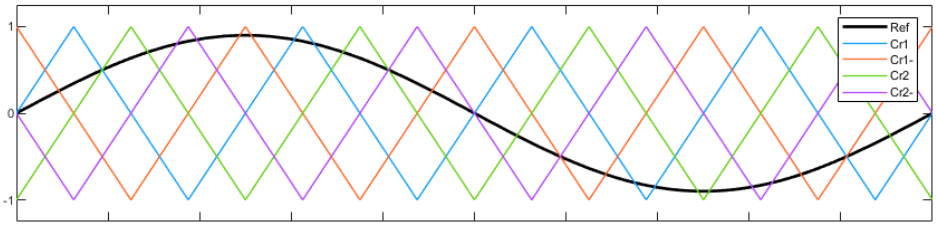

Figure 3.5: Waveform of phase-shift example

3.4.2. level-shift modulation for multilevel inverters

Similarly, the carrier waves have the same frequency and the same peak-to-peak amplitude in level-shift modulation. The $(m-1)$ triangular carriers are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index is the same as that for phase-shift modulation, which is $m_f = f_{cr}/f_m$. But the amplitude modulation index is changed into:

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}(m-1)} \quad \text{for } 0 \leq m_a \leq 1 \tag{3.8}$$

There are three schemes for level-shift multicarrier modulation: (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. In what follows, only IPD modulation scheme is discussed since it provides the best harmonic profile of all three modulation schemes[31]. Take the same example in the initialization of phase-shift modulation, in IPD modulation scheme, the waveform is shown in Figure 3.6-3.8.

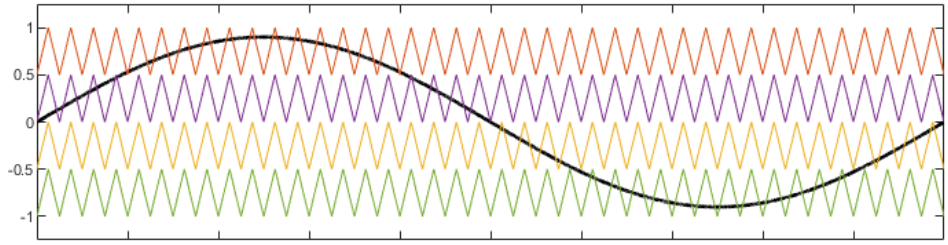

Figure 3.6: In-phase disposition level-shift modulation(IPD)

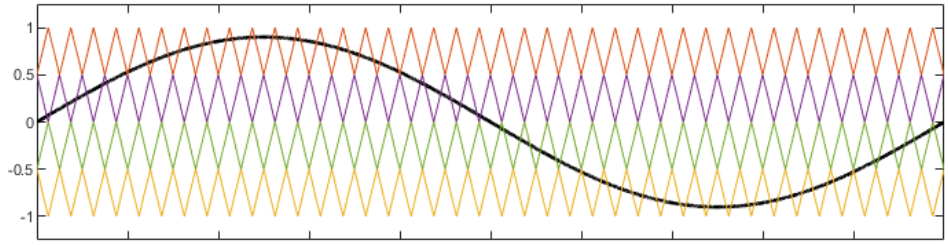

Figure 3.7: Alternative phase opposite disposition(APOD)

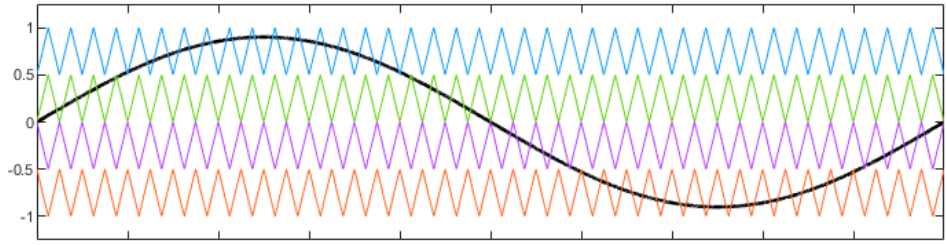

Figure 3.8: Phase opposite disposition(POD)

3.5. Space Vector Modulation

Space Vector Modulation (SVM) is a technique used in power electronics and motor control systems to generate high-quality waveforms for controlling three-phase voltage-source inverters (VSI). It is particularly employed in applications like variable speed drives, uninterruptible power supplies (UPS), and renewable energy systems.

The primary goal of Space Vector Modulation is to control the output voltage of the inverter by manipulating the magnitude and phase of the individual voltage vectors in the three-phase space. Unlike traditional modulation techniques that control the amplitude and frequency independently, SVM provides a more efficient way to control both parameters simultaneously.

In a three-phase system, the voltage vectors are represented as vectors in a two-dimensional space, often referred to as the "Clarke transform" space. These vectors are arranged to form a hexagon, and the center of the hexagon represents the zero voltage vector. A space vector is a mathematical representation of the three-phase voltages in a two-dimensional space. It represents both the amplitude and phase of the voltage. The concept of a space vector allows for more precise control of the output voltage. The hexagon in the Clarke transform space is divided into six sectors. Each sector corresponds to a specific voltage vector. By determining the sector in which the space vector lies, the control algorithm can choose the appropriate voltage vectors for modulation. The duration and magnitude of the space vector are adjusted to achieve the desired output voltage. By dynamically controlling these parameters, SVM optimally synthesizes the desired voltage waveform. Space Vector Modulation is widely adopted in industrial applications where precise control of three-phase inverters is essential for efficient and reliable operation. It plays a crucial role in achieving high-performance motor drives and power conversion systems.

For example, in a Neutral Point Clamped (NPC) multilevel inverter shown in Figure 2.2, to implement SVM, the relationship between switching states and terminal voltage should be determined in the beginning. The relationship is shown in Table 3.1. To note that only phase a is demonstrated. The other two phases follow the same path as phase a [32].

Table 3.1: Switching states and terminal voltage

Symbol	Switching States				Terminal Voltage
	S_{a1}	S_{a2}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-$V_{dc}/2$

For one phase, there are three different switching states, noted as P, O and N. Take the other two phases into consideration, there are in total 27 different switching states, as shown in Figure 3.9. As it suggests, there are 24 active vectors including 12 short vectors,6 medium vectors,6 long vectors and 3 null vectors.

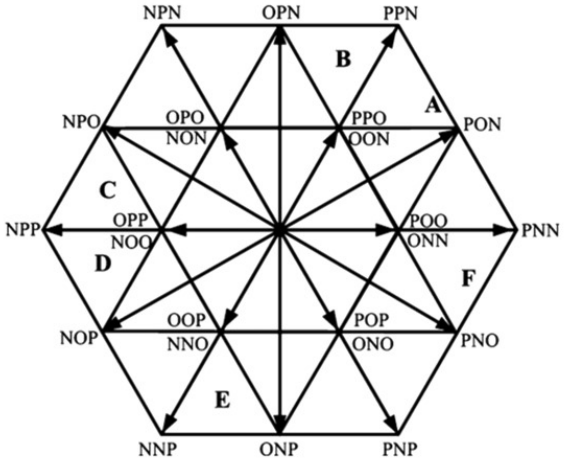

Figure 3.9: Switching states in three-phase SVM

The hexagon as a whole can be divided into six regions, noted as from A to F. Each region comprises four equilateral triangles. Take Region A as an example, it is shown in Figure 3.10.

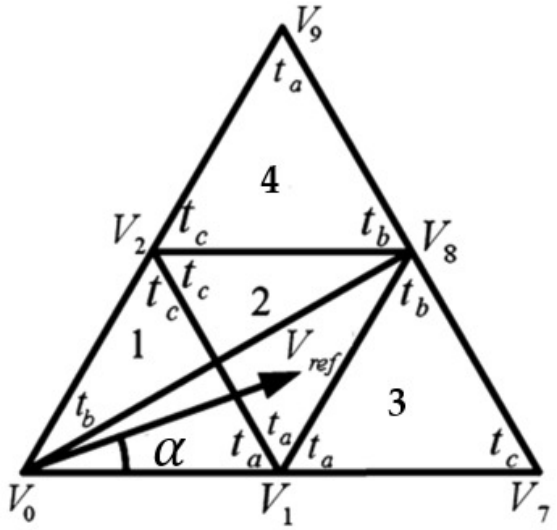

Figure 3.10: Region A

To synthesis the reference voltage V_{ref}, three closest vectors must be chosen. Here, when V_{ref} lands within equilateral triangle 2, V_{ref} should be disassembled with V_1, V_2, and V_8. To be more general, V_{ref} should consist of the vector of the three vertices of the equilateral triangle in which V_{ref} is located and the origin. To select an equilateral triangle in a mathematical way, Modulation Index(m_n) is defined. It is determined by:

$$m_n = \frac{V_{\text{ref}}}{\frac{2}{3}V_s} \tag{3.9}$$

$$m_1 = m_n\left(\cos\alpha - \frac{\sin\alpha}{\sqrt{3}}\right) \tag{3.10}$$

$$m_2 = \frac{2}{\sqrt{3}}m_n \sin\alpha \tag{3.11}$$

$$m_3 = m_1 + m_2 \tag{3.12}$$

If m_1, m_2 and $m_3 < 0.5$, then V_{ref} lies in equilateral triangle 1. If m_1 and $m_2 < 0.5$ and $m_3 > 0.5$, then V_{ref} lies in equilateral triangle 2. If $m_1 > 0.5$, then V_{ref} lies in equilateral triangle 3. If $m_2 > 0.5$, then V_{ref} lies in equilateral triangle 4.

As soon as the vectors are determined, the switching time T_s allocated to each vector t_a, t_b and t_c is determined as well. To take region A as an example, the switching time can be described in Table 3.2.

Table 3.2: Switching time for Region A

Region	t_a	t_b	t_c
1	$\frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}-\alpha\right)$	$T_s - \frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}+\alpha\right)$	$\frac{4}{\sqrt{3}}m_nT_s\sin\alpha$
2	$T_s - \frac{4}{\sqrt{3}}m_nT_s\sin\alpha$	$\frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}+\alpha\right) - T_s$	$T_s - \frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}-\alpha\right)$
3	$2T_s - \frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}+\alpha\right)$	$\frac{4}{\sqrt{3}}m_nT_s\sin\alpha$	$\frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}-\alpha\right) - T_s$
4	$\frac{4}{\sqrt{3}}m_nT_s\sin\alpha - T_s$	$\frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}-\alpha\right)$	$2T_s - \frac{4}{\sqrt{3}}m_nT_s\sin\left(\frac{\pi}{3}+\alpha\right)$

To conclude, the SVM flowchart is shown in Figure 3.11.

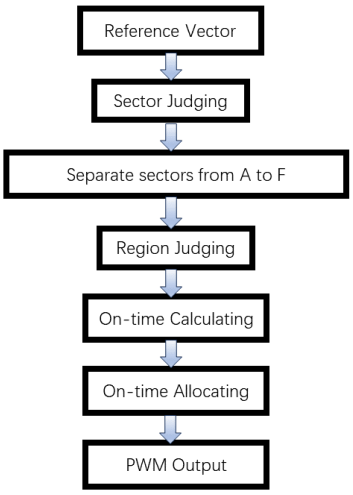

Figure 3.11: Flowchart of SVM

To conclude, SVM has the following features:

- Reduced THD: SVPWM avoids difficulties of using linear functions in a high dimensional space, also it effectively utilizes DC input voltage and reduces THD values.

- Reduction of Computation: Compared to carrier-based PWM algorithms because the number of carriers does not increase as the number of converter levels increases. This advantage makes the digital implementation of the algorithms easier.
- Modulation Time Limitation: To achieve a proper time average, the modulation period T_s is small, leading to high switching frequencies, comparable to carrier-based PWM (above 1 kHz), and therefore not useful for very high power applications.

4

Switching techniques and fast voltage balancing of PUC5 inverter

In chapter 2 and 3, the report have discussed pros and cons of different MLI topologies and corresponding switching technologies. By thoroughly reviewing topologies and switching technologies, the report concludes that PUC5 inverter with carrier-based modulation is a promising solution of multilevel inverters. The main benefits of such combination are covered in chapter 2 and 3. However, it's not enough with simple combination because:

- 4 carrier waves to generate 5 output voltage levels.
- A large axillary capacitor needed to reduce capacitor voltage ripple.
- Stagnancy of starting and response to DC voltage variation.
- Bulky output voltage filter.

In [12], a fast sensor-less voltage balancing and capacitor size reduction in PUC5 inverter based on level-shift modulation is introduced. On top of that, this report refines the method based on phase-shift modulation with better performance. This chapter will present both methods with further analyzation. Though the switching method varies, the general PUC5 switching states remain as Table 4.1.

Table 4.1: Switching States of PUC5 Inverter

Switching State	S_1	S_2	S_3	V_{out}	Capacitor Charge/Discharge
V_1	1	0	0	$+E$	\
V_2	1	0	1	$+E/2$	Charge
V_3	1	1	0	$+E/2$	Discharge
V_4	1	1	1	0	\
V_5	0	0	0	0	\
V_6	0	0	1	$-E/2$	Discharge
V_7	0	1	0	$-E/2$	Charge
V_8	0	1	1	$-E$	\

4.1. Improved switching method based on level-shift modulation

The proposed switching method based on level-shift modulation is shown in Fig. 4.1. Compared with traditional PUC5 inverter controlled by level-shift modulation, it reduces the number of carrier waves from 4 to 2. Moreover, it accelerates the charging/discharging frequency of the axillary capacitor from fundamental frequency to switching frequency. Thus, the capacitor responds to the change of DC voltage level much faster, and the capacitor voltage ripple at steady state is reduced significantly [12].

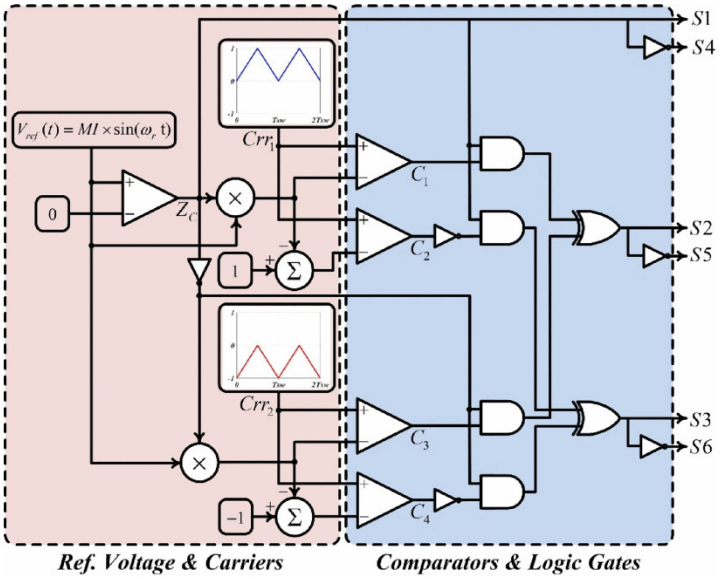

Figure 4.1: Proposed switching method based on level-shift modulation

In the proposed switching method, the zero-crossing comparator Z_C is utilized to detect the positive half-cycle of the reference voltage V_{ref} and to control switches $(S1, S4)$ at the fundamental frequency according to Table 4.1. Therefore, switches set $(S1, S4)$ will operate on a low frequency. The operation of Z_C and the control of switches $(S1, S4)$ can be described as follows:

$$\begin{aligned} Z_C &= \begin{cases} 1, & V_{\text{ref}} \geq 0 \\ 0, & V_{\text{ref}} < 0 \end{cases} \\ S_1 &= \overline{S_4} = Z_C \end{aligned} \tag{4.1}$$

The two level-shift carrier waves, namely $Crr1$ and $Crr2$, are respectively positive and negative triangular carriers. The comparison between $Crr1, Crr2$ and Z_C generates the desired signal output by:

$$\begin{aligned} C_1 &= \begin{cases} 1, & Crr_1 \geq Z_C \cdot V_{\text{ref}} \\ 0, & Crr_1 < Z_C \cdot V_{\text{ref}} \end{cases} \\ C_2 &= \begin{cases} 1, & Crr_1 \geq (1 - Z_C \cdot V_{\text{ref}}) \\ 0, & Crr_1 < (1 - Z_C \cdot V_{\text{ref}}) \end{cases} \\ C_3 &= \begin{cases} 1, & Crr_1 \geq \overline{Z_C} \cdot V_{\text{ref}} \\ 0, & Crr_1 < \overline{Z_C} \cdot V_{\text{ref}} \end{cases} \\ C_4 &= \begin{cases} 1, & Crr_2 \geq \left(-1 - \overline{Z_C} \cdot V_{\text{ref}}\right) \\ 0, & Crr_2 < \left(-1 - \overline{Z_C} \cdot V_{\text{ref}}\right) \end{cases} \end{aligned} \tag{4.2}$$

$$\begin{aligned} S_2 &= \overline{S_5} = (C_1 \cdot Z_C) \oplus \left(C_3 \cdot \overline{Z_C}\right) \\ S_3 &= \overline{S_6} = \left(\overline{C_2} \cdot Z_C\right) \oplus \left(\overline{C_4} \cdot \overline{Z_C}\right) \end{aligned} \tag{4.3}$$

The reference voltage and carriers $Crr1$ and $Crr2$ are compared in Fig. 4.2. It is clear that the essence of such modulation is based on level-shift method.

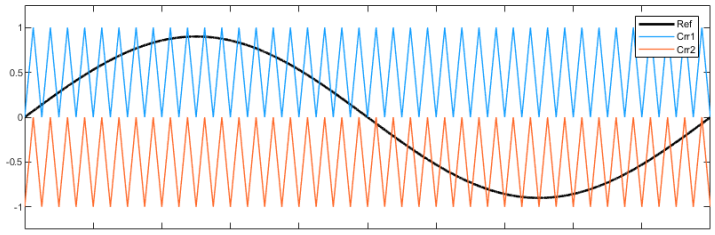

Figure 4.2: Proposed phase-shift modulation reference and carriers in [33]

Also, it's important to look into the relationship between Z_c and comparators, which is shown in Fig. 4.3.

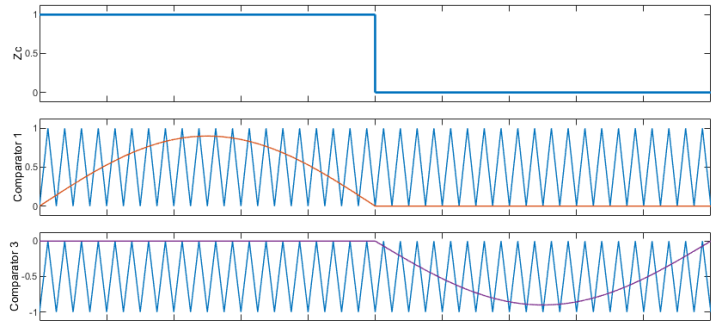

Figure 4.3: Proposed phase-shift modulation Z_c and comparators in [33]

The report can conclude that for each pair of comparators (comparator 1 and 2, 3 and 4), it only works in half of the cycle of reference voltage. Therefore, extra comparators and logic gates are required to combine the outcome from comparators of reference voltage and carriers and separate for each pair of switches.

4.2. Improved switching method based on phase-shift modulation

To optimize the performance of PUC5 inverter and reduce the size of the axillary capacitor, the key is to increase the charging/discharging frequency of the axillary capacitor. In section 4.1, the goal is achieved by a new switching method based on level-shift modulation plus comparators and logic gates to generate the desired gate signals. However, the added comparators and logic gates increase the complexity of the whole modulation. Since in the level-shift modulation, the carriers are compared in the same time domain, extra logic gates are required to separate the outcome of comparators for the switch pairs (S_2, S_5) and (S_3, S_6).

In [33], a PUC5 converter based on phase-shift modulation with reduced size of axillary capacitor is introduced. It follows the general PUC5 switching states in Table 4.1 and basic phase-shift modulation mentioned in section 3.4. However, it modifies the control method. The flowchart of its control method is shown in Fig. 4.4.

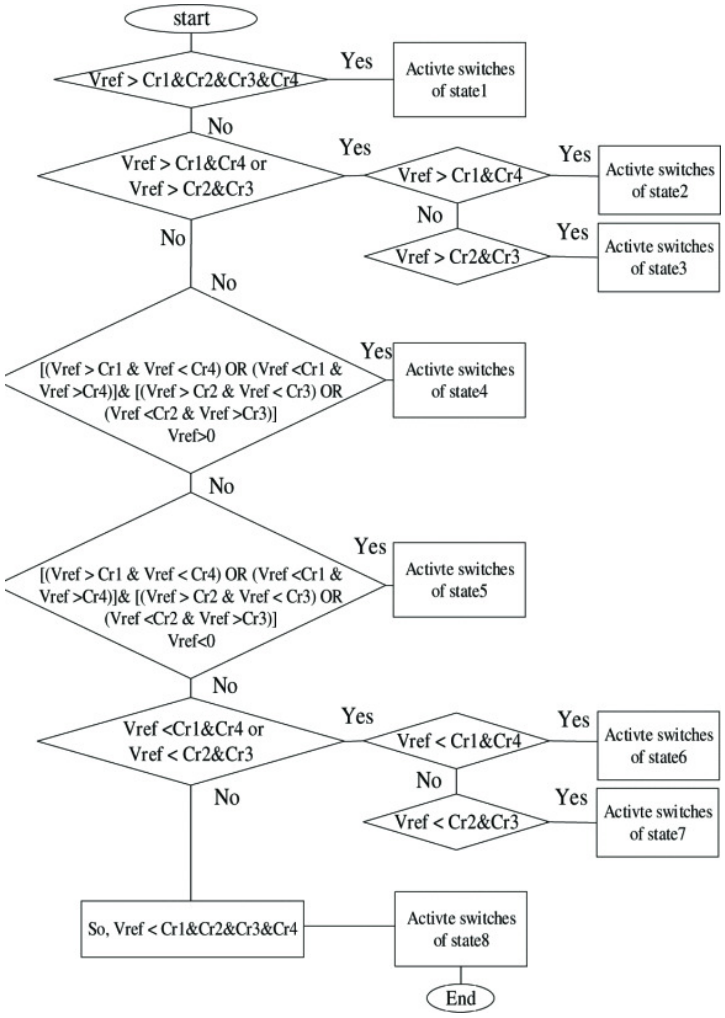

Figure 4.4: Proposed phase-shift modulation control logic for PUC5 Converter in [33]

4.3. Proposed switching method based on phase-shift modulation

Though the control method in the last section evades the extra logic gates, it requires 4 carrier waves and complex comparators judging criteria. In a way, it manually defines a modulation method by varying comparators for each occasion. It successfully rises the charging/discharging frequency and thus reduces the capacitor size nevertheless. On top of that, the report introduces an improved phase-shift modulation with better performance.

The proposed phase-shift modulation method is depicted in Fig. 4.5, which comprises only two phase-shift triangular carrier waves, $Cr1$ and $Cr2$, without complex logic gates or a switching table. Therefore, the proposed method doesn't require complex calculations or logic gates, making it easily implementable on affordable microcontrollers.

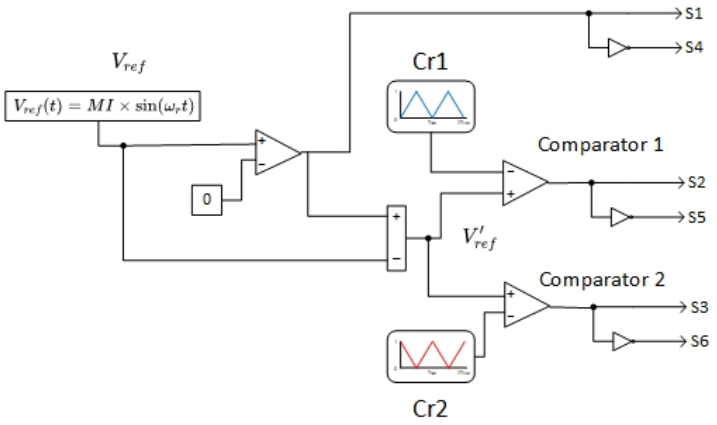

Figure 4.5: Proposed phase-shift modulation for PUC5 Converter

PUC5 Converter balances the capacitor voltage at the frequency of the reference voltage V_{ref}. The goal of this new scheme is to increase the balancing frequency from the fundamental frequency f_{ref} (50 or 60 Hz) to the switching frequency f_{sw} (in kilohertz). Given Table 4.1, the switching pattern of PUC5 Converter can be generalized as follows:

$S1$ is always on when the reference voltage is positive while off when the reference voltage is negative. $S4$ is complementary with $S1$. The pair of switches $S1$ and $S4$ only answer to the change of polarity of the reference voltage. Therefore, it uses low-frequency switches. For the other two pairs of switches, they are responsible for reference voltage tracking and capacitor voltage balancing. They need high-frequency switches. Charging and discharging happen in switching states V_2/V_3 and V_6/V_7, which only involve the transition of S_2 and S_3 with complimentary switching of S_5 and S_6. Thus, S_2 and S_3 are designed to have 180 ˚phase shift to ensure regular transition.

The proposed switching method utilizes a zero-crossing comparator (Z_C) to detect the positive half cycle of the reference voltage (V_{ref}) and control (S_1, S_4) at the fundamental frequency. The expressions for Z_C and (S_1, S_4) are as follows:

$$\begin{aligned} Z_C &= \begin{cases} 1, & V_{\text{ref}} \geq 0 \\ 0, & V_{\text{ref}} < 0 \end{cases} \\ S_1 &= \overline{S_4} = Z_C \end{aligned} \tag{4.4}$$

Decoupling the switching actions of S_1 from S_2 and S_3, the reference signal V_{ref} should be modified in a way to generate appropriate pulses for S_2 and S_3. Therefore, one can assume that V'_{ref} is a modification of V_{ref} with the switching matrix shown in Table 4.2. To generate those 4 states for S_2 and S_3 by standard PS modulation, 2 carrier waves are required (Cr1 and Cr2), which are shifted 180°.

Table 4.2: Desired switching modulation method

S_2	S_3	Modulation Method
0	0	$V'_{ref} < Cr1$ & $V'_{ref} < Cr2$
0	1	$V'_{ref} < Cr1$ & $V'_{ref} \geq Cr2$
1	0	$V'_{ref} \geq Cr1$ & $V'_{ref} < Cr2$
1	1	$V'_{ref} \geq Cr1$ & $V'_{ref} \geq Cr2$

According to Fig. 1.1, the relationship among output voltage V_{out}, DC link voltage V_1 and auxiliary capacitor voltage V_c can be written as below:

$$V_{out} = V_{d_c} - V_c \tag{4.5}$$

Here, one can decouple the mathematical model of the PUC5 converter into two switching parts [34]. It works when the switching frequency is high enough compared to the fundamental frequency [35] [36]. Therefore, the reference signals for generating required pulses of those decoupled parts can be written based on Eq. (4). V_{ref} represents the reference signal for output voltage, Z_c is assigned for the switching behavior of (S_1,S_4), so:

$$V_{ref} = Z_c - V'_{ref} \tag{4.6}$$

Thus, the modified reference signal V'_{ref} can be calculated as the following:

$$V'_{ref} = Z_C - Vref \tag{4.7}$$

Eq (6) is essential to generate the V'_{ref}, which will be modulated by Cr1 and Cr2 to generate the pulses for S_2 and S_3. The switching pattern, defined alternative function outputs, and output voltage waveform of the proposed modulation method are illustrated in Fig. 4.6.

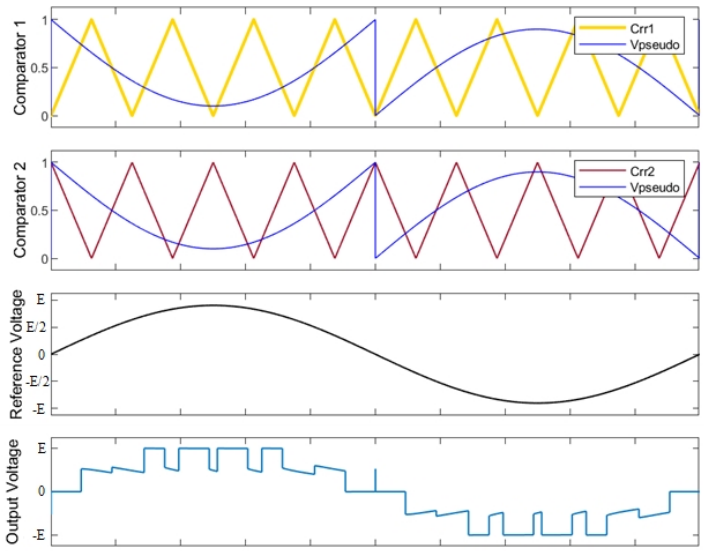

Figure 4.6: Switching pattern of the proposed modulation method, alternative reference voltage and output voltage of PUC5 Converter ($f_{ref} = 50Hz, f_{sw} = 200Hz$)

In the proposed modulation method, the DC capacitor undergoes charging and discharging in each switching period based on the load current direction and the switching operation. The voltage balancing process of the PUC5 converter capacitor in each PWM period is depicted in Fig. 4.7.

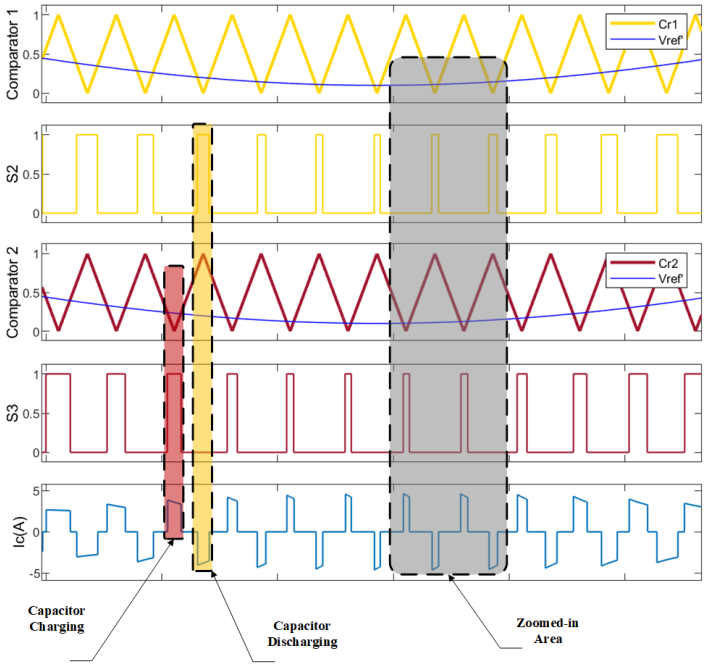

Figure 4.7: Balancing the Q_{charge} and $Q_{discharge}$ processes of the PUC5 converter capacitor in each PWM period ($f_{ref} = 50Hz, f_{sw} = 2000Hz$)

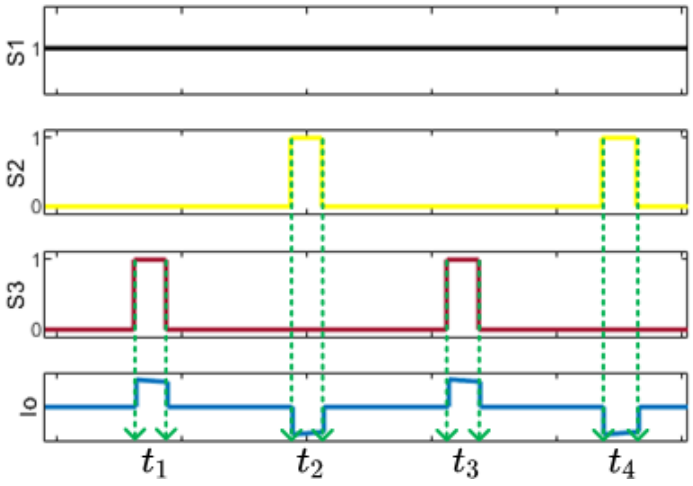

Figure 4.8: Zoomed-in capacitor pattern of one switching cycle from Fig. 4.7

To better illustrate the balancing process, a zoomed-in figure is depicted in Fig. 4.8. In this cycle, the reference voltage is kept positive, and S_1 is on. When S_2 is on while S_3 is off, during t_2 and t_4, the capacitor discharges. When S_2 is off while S_4 is on, during S_1 and S_4, the capacitor charges. Because the switching frequency f_{sw} is very high, the charging/discharging time is very short, and the change of capacitor current i_c can be taken as a constant. The electrical charge of the capacitor q is derived as:

$$q = \int i_c dt = i_c(t_1 + t_3 - t_2 - t_4) \tag{4.8}$$

$$= i_c(t_{sw3on} - t_{sw2on}) \tag{4.9}$$

Where t_{sw2on} and t_{sw3on} are the on time of switches S_2 and S_3 respectively. In steady state, as long as t_{sw2on} and t_{sw3on} are equal, the PUC5 converter capacitor voltage is always balanced at the voltage level of $E/2$. Since the negative reference voltage half cycle is mirroring with the positive cycle, the voltage balancing works as well.

4.4. Simulation results and discussions

MATLAB/Simulink is used to simulate a standalone system feeding RL load to verify the proposed modulation method and integrated fast sensorless voltage balancing technique. Parameters of the simulation are listed in Table 4.3. The conventional phase-shift modulation method and the proposed one have been implemented separately in the simulation for a fair comparison. Two simulations are tested: the capacitor voltage ripple in steady state and the transient behavior when DC voltage changes.

Table 4.3: Simulation parameters

DC source voltage	$200V$
RL load	$40\Omega, 10mH$
Switching frequency	$2kHz$
Capacitor	$100\mu F$
Modulation index	0.9

According to Table 4.1, the charging of the auxiliary capacitor only happens on the positive cycle of the reference voltage, and discharging happens on the negative cycle. It suggests that the auxiliary capacitor charges/discharges at the frequency of the reference voltage, which is very low. If the capacitor remains at merely $100\mu F$, the capacitor voltage ripple at steady state would be untolerable, as shown in Fig. 4.9.

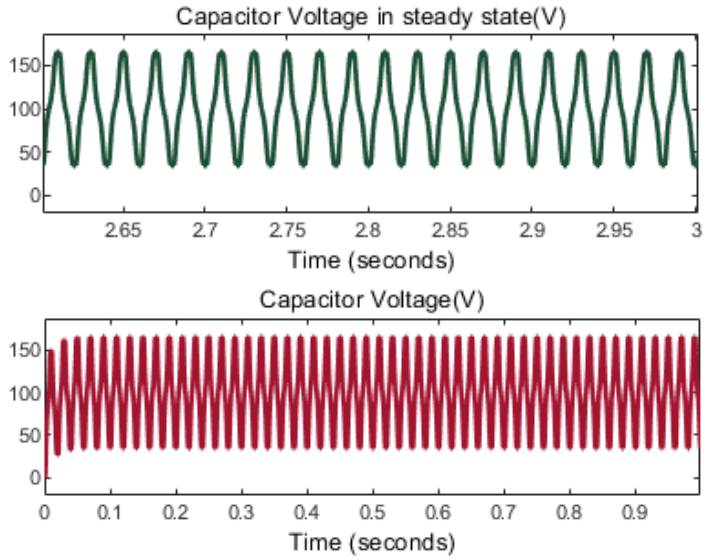

Figure 4.9: Capacitor voltage in the steady state of the basic phase-shift method

Steady-state simulation results of proposed phase-shift modulation method are shown in Fig 4.10. A smooth 5-level voltage waveform is generated at the output of the PUC5 inverter due to the accurate voltage balance of the auxiliary capacitor. Consequently, a low harmonic current is also drawn by the load.

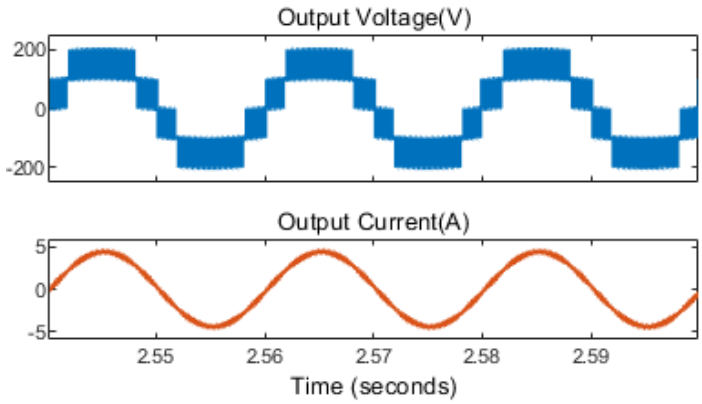

Figure 4.10: Output voltage and current of the proposed modulation method

To show the efficient functionality of the proposed switching technique in precise tracking of the reference voltage, a step change has been applied in the amplitude of the DC source. therefore, E has been changed from 200V to 300V and results are shown in Fig 4.11. It is clear that the capacitor voltage has been properly balanced at half of the DC source.

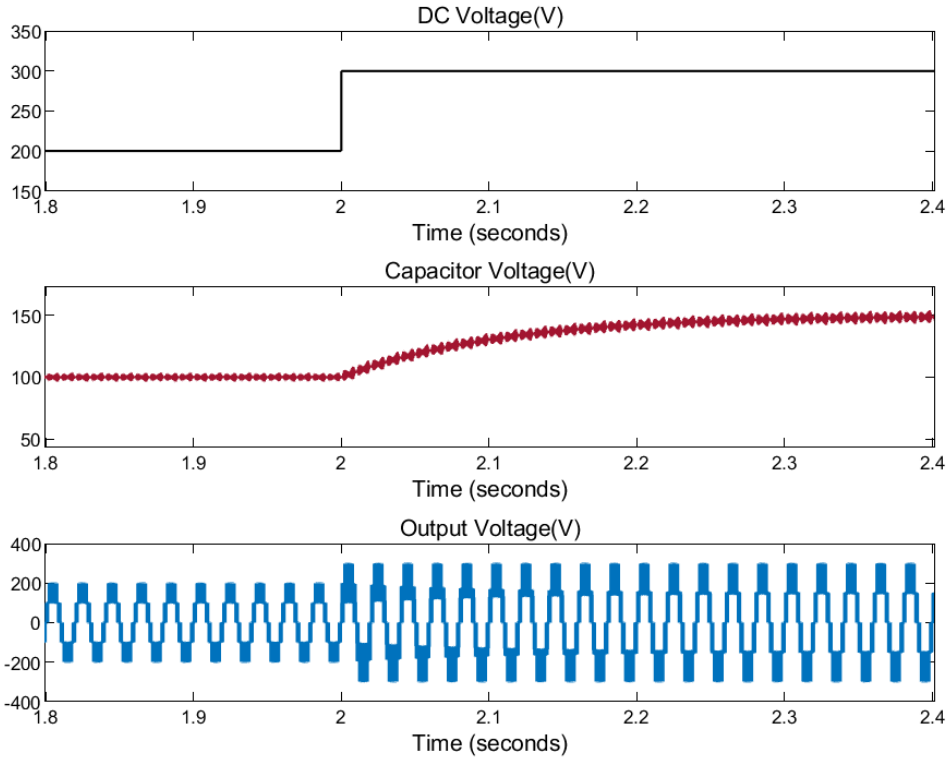

Figure 4.11: Sensorless voltage balancing in proposed modulation method

In the next test, the auxiliary capacitor's voltage ripple and the start-up charging time were measured, and this is shown in Fig. 4.12. It is clear that the capacitor voltage reaches the reference level in almost 0.3s with a peak-to-peak ripple of 7V.

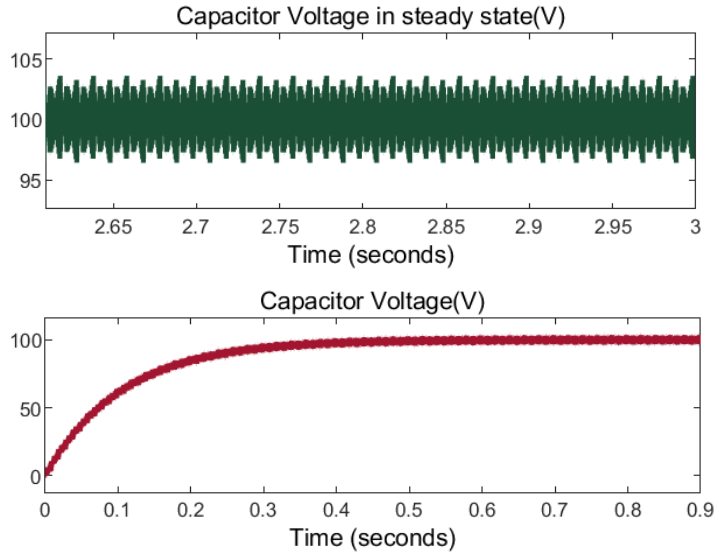

Figure 4.12: Capacitor voltage in the steady state of the proposed method

To achieve similar auxiliary capacitor voltage ripple, a PUC5 inverter modulated with classic phase-shift modulation requires a $2000\mu F$ capacitor. Even if a bulky capacitor is implemented, it takes longer to reach steady state as Fig. 4.13.

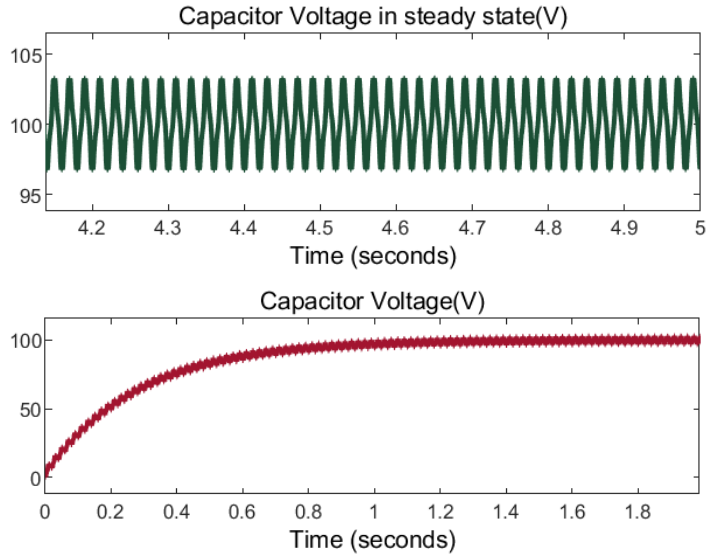

Figure 4.13: Capacitor voltage of the classic phase-shift modulation method

Eventually, to have a fair comparison with the conventional phase-shift modulation technique, a $2000\mu F$ capacitor replaced the $100\mu F$ as the auxiliary capacitor to have the same voltage ripple of almost 7V. Results are depicted in Fig. 4.12, showing the same amount of voltage ripple but a long start-up charging time of almost 1s. Moreover, the frequency of the charge/discharge transition is obvious from those figures. Obviously, the proposed technique charges/discharges the capacitor at the switching frequency, resulting in a significant reduction in the capacitor size. As shown here, the capacitor size has been reduced by 95% from $2000\mu F$ to $100\mu F$ after implementing the proposed switching technique.

Simulink model is used to primarily validate the feasibility and superiority over traditional carrier based modulation methods. Further comparison will be covered with hardware-in-the-loop test.

5

Hardware-in-the-loop simulation results

To solve mathematical functions and equations at a specific time-step, each variable or system state is determined sequentially based on the variables and states from the previous time-step. In a discrete-time simulation, the real time needed to compute all equations and functions representing the system at a given time-step may be either shorter or longer than the duration of the simulation time-step. Typically, when conducting offline simulations, the goal is to obtain results as quickly as possible. The speed at which the system can be solved depends on the available computational power and the complexity of the system's mathematical model [37].

Oppositely, during real-time simulation, the accuracy of computations depends not only on the precise dynamic representation of the system but also on the amount of time available to produce the results. For a real-time simulation to be valid, the real-time simulator must accurately generate the internal variables and outputs of the simulation within the same time frame that its physical counterpart would. It can be concluded that a real-time simulator is performing as expected if the equations and states of the simulated system are solved accurately and resemble its physical counterpart closely, without any occurrence of overruns.

Based on real-time simulation, hardware-in-the-loop (HIL) is achieved. HIL simulation is the standard for developing and testing the most complex control, protection and monitoring systems. HILs rise is the result of two major factors currently affecting product development across all industries: time-to-market and system complexity.

Testing of control systems has traditionally been carried out directly on physical equipment (i.e. plant) in the field, on the full system or on a power tested in a lab. While offering testing fidelity, this practice can be very expensive, inefficient and potentially unsafe. HIL testing offers an excellent alternative to traditional testing methods. When performing HIL simulation, the physical plant is replaced by a precisely equivalent computer model, running in real-time on a simulator appropriately equipped with inputs and outputs (I/Os) capable of interfacing with control systems and other equipment. In this way, the HIL simulator can accurately reproduce the plant and its dynamics, together with sensors and actuators, providing comprehensive closed-loop testing without the need for testing on real systems.

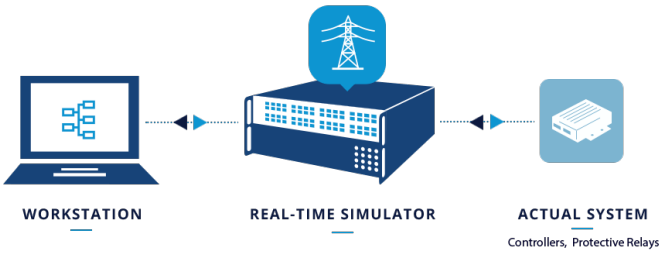

Figure 5.1: Hardware-in-the-loop Process

5.1. HIL implementation of PUC5 inverter

The HIL system used in the project is composed of a workstation and a real-time simulator OP4610XG, which is shown in Fig. 5.2. The OP4610XG is a compact, mid-range simulator that combines all OPAL-RTs strengths in high-performance Real-Time Rapid Control Prototyping and Hardware-in-the-loop simulation. The integration of a high-end AMD Ryzen 6-core processor with powerful Xilinxő Kintexő-7 FPGA provides great simulation power and sub-microsecond simulation time steps to maximize the accuracy of fast power electronic systems. It is fully compatible with RT-LAB and HYPERSIM.

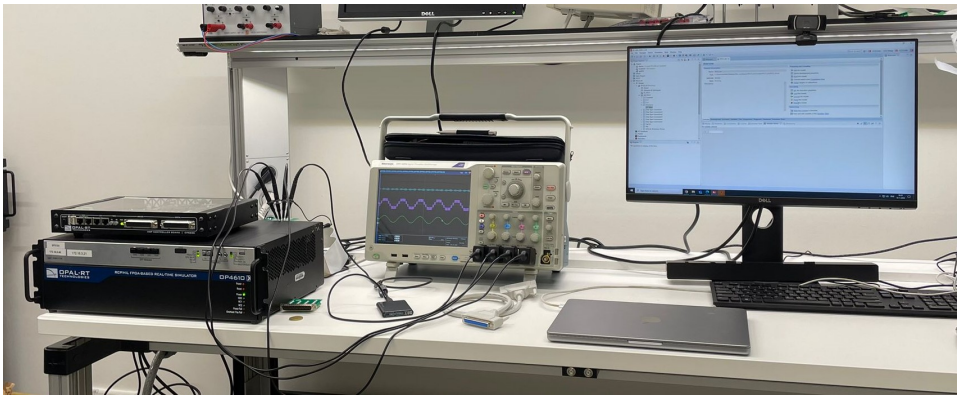

Figure 5.2: Hardware-in-the-loop Hardwares

The HIL models are built on Simulink and RT-LAB. To start with, a PUC5 converter model is configured in Simulink, and divided into two subsections SM (master subsystem) and SC (console subsystem) for further procedure. The topology is shown in Fig. 5.3

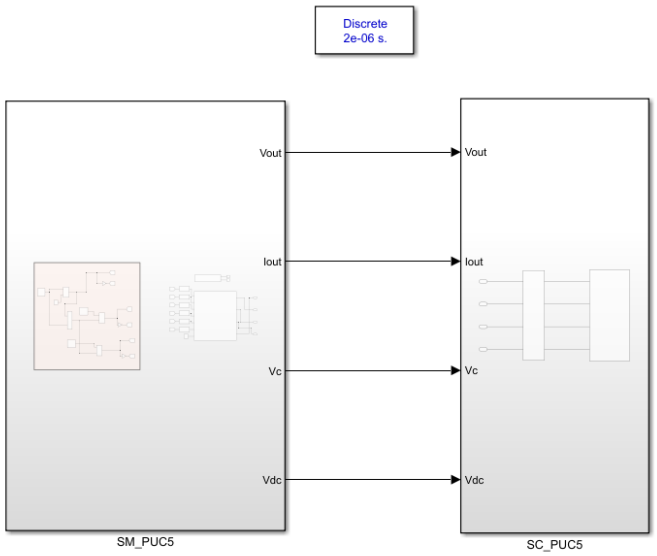

Figure 5.3: A Hardware-in-the-loop Simulink Model

The Console subsystem is the subsystem operating on the command station that enables you to interact with the system. It contains all the Simulink blocks related to acquiring and viewing data (scope, manual switch, To Workspace-type blocks, etc.). The blocks you need, whether it is during or after the execution of the real-time model, must be included in the Console subsystem. The console runs asynchronously from the other subsystems. Note that there can only be one Console per model. There is always one and only one master subsystem inside a model. It contains the computational elements of the model. To be more specific, SM in the project comprises the topology of PUC5 and modulation method.

To build PUC5 topology on FPGA for much faster solving speed, an electric Hardware Solver (eHs) is needed, which is shown in Fig. 5.4 Fig. 5.5.

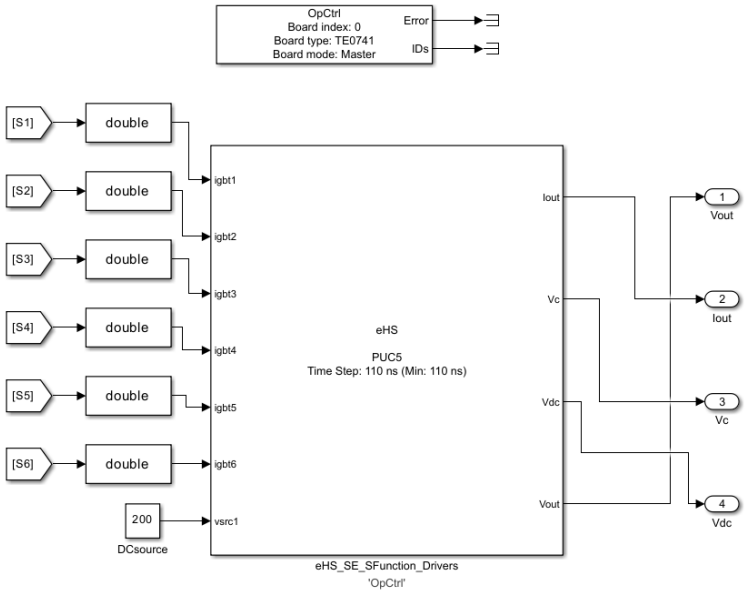

Figure 5.4: electric Hardware Solver for HIL, outside the block

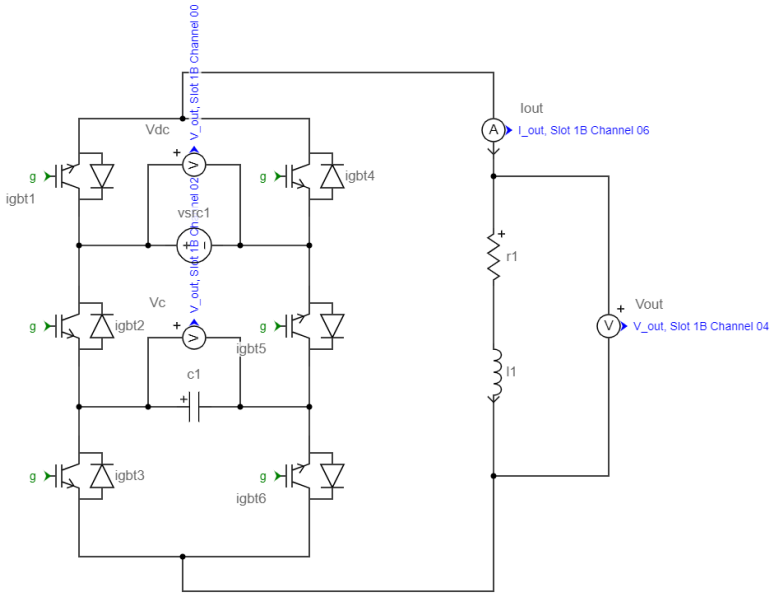

Figure 5.5: electric Hardware Solver for HIL, inside the block

The eHS solver is an FPGA-based technology developed by OPAL-RT for real-time power electronics simulation. Thanks to a convenient circuit schematic graphical user interface, the FPGA code is automatically generated, making FPGA-based simulation accessible to a large number of users.

The OPAL-RT electric Hardware Solver (eHS) is a powerful floating-point solver developed by OPAL-RT that enables users to simulate an electric circuit on an FPGA automatically, without having to write the mathematical equations. It combines the simplicity of building electric circuit models using either our OPAL-RT Schematic Editor or the Simscape Electrical Specialized Power Systems (SPS) Toolbox, PSIM, the PLECS Blockset, or NI Multisim software with the strength of OPAL-RT FPGA-based simulators to solve the currents and voltages within the circuit in real-time, with a sample time below 1s.

The switches receive signals from Simulink. Their parameters are defined as:

Table 5.1: switches parameters in eHs

R_{on}	0.01Ω
R_{off}	$10^5\Omega$
$Relaxation$	8
R_{damp}	$20\Omega/40\Omega$

Where R_{on} is the internal resistance when the switch is closed. R_{off} is the internal resistance when the switch is open. In eHS Gen5, switches introduced a delay in order to support interpolation. There can be one or two delay introduced depending on the solver strategy adopted. Furthermore, to mitigate this latency, a prediction is made on the measurements needed to compute the switches. Coupling of the switches model is done through voltage, and current injection, therefore depending on the stiffness of the circuit, a relaxation needs to be applied to the injection to ensure model stability. For switching frequency below 100kHz, prediction and relaxation parameters should be set to the minimum values explained below. In short, The relaxation parameters is related to the time it takes to reach steady state. This reduces the stiffness of the model, increasing its stability. However, a longer transition time also increases the error and losses in the model. Therefore, there is a balance between the accuracy of the model and its stability. From 1 to 10, the number is closer to 1, the better performance the model has. While the number is closer to 10, the better stability the model has. In the project, the stability is more appreciated, it is decided at 8. R_{damp} is the damping resistance. The equivalent circuit of a single switch consists of a controlled current source in parallel with a resistance, whose value shall be set by the user. If R_{damp} value is very high (closer to the blocking resistance R_{off}) the transition to the blocking state is more stable numerically, whereas if R_{damp} value is very small (closer to the conducting resistance R_{on}), the transition to conducting state is more stable. Therefore, the R_{damp} shall be placed between these extreme values. Besides, voltage error during transition is directly proportional to R_{damp}, while current error is inversely proportional to this value. The Opal technician suggests setting the R_{damp} to:

$$R_{\text{damp}} = \frac{V_{\text{switch}}}{I_{\text{switch}}} \tag{5.1}$$

where V_{switch} is the voltage across the switch just before it starts conducting and I_{switch} is the current through the switch just before it is blocked. Still, the equation is hard to use since V_{switch} and I_{switch} are not easy to settle. To precisely determine the value requires reiteration. However, it greatly increases unnecessary calculation. Therefore, the project proposes an approximate way to settle values, by calculate R_{damp} only in Simulink model and only steady state is considered. As a result, R_{damp} of S_1 and S_4 is settled at 40Ω and the other two pairs of switches are settled at 20Ω. Moreover, by changing different R_{Ramp}, only the output waveform quality is influenced. With proper setting, the spikes of waveform can be mitigated.

5.2. HIL results

Five switching methods are experimented and discussed: basic level-shift/phase-shift methods introduced in section 3.4 and fast sensorless level-shift/phase-shift methods introduced in chapter 4. First, the steady state will be examined. Then, raise the DC voltage from $200V$ to $300V$ to observe the transient behavior. The project is interested in two aspects of switching methods, the one is steady state performance and the other is transient behavior when DC voltage changes. As for the size of auxiliary capacitor, in the two slow phase-shift/level-shift methods, the capacitor size is $2000\mu F$, while in the fast phase-shift/level-shift methods, the capacitor size is $100\mu F$. The parameters of HIL are shown in Table 5.2.

Table 5.2: Simulation parameters of HIL

DC source voltage	$200V$
RL load	$40\Omega, 10mH$
Switching frequency	$2kHz$
Capacitor	$100\mu F/2000\mu F$
Modulation index	0.9

The HIL results are shown below, C1 shows DC voltage, C2 shows capacitor voltage and is intentionally put to lower scale to show the ripple of the auxiliary capacitor more clearly, C3 shows output voltage, C4 shows output current. And in total, five different modulation methods are compared:

- slow sensorless phase-shift method
- slow sensorless level-shift method
- fast sensorless level-shift method in [12]
- fast sensorless phase-shift method in [33]
- proposed fast sensorless phase-shift method

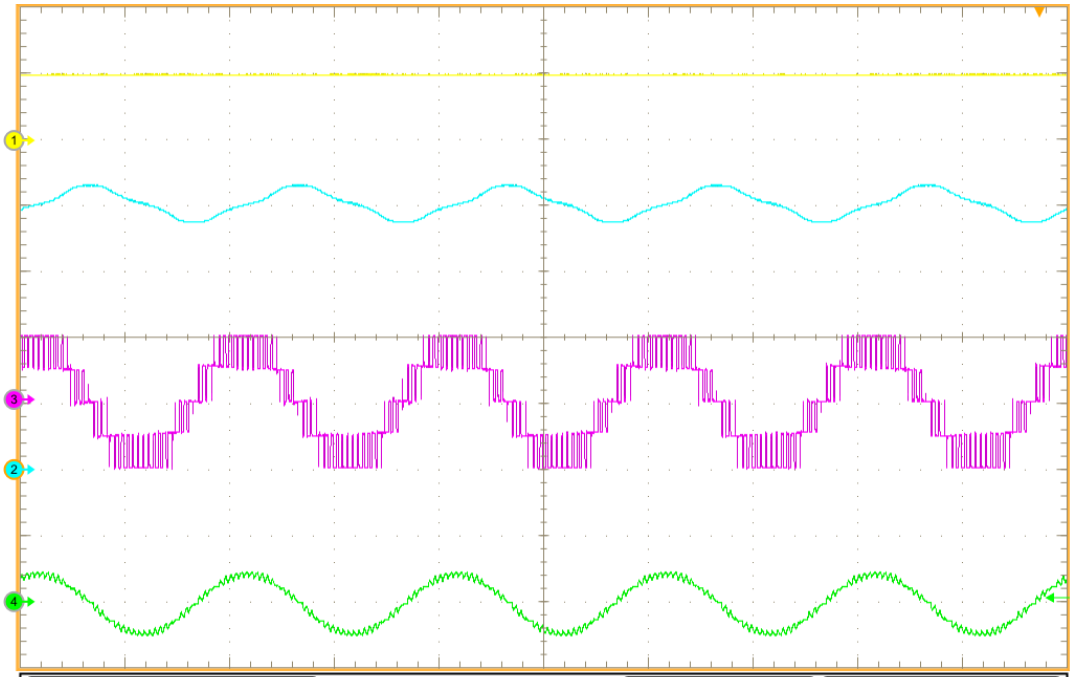

Figure 5.6: HIL result of steady state performance, slow sensorless phase-shift method
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

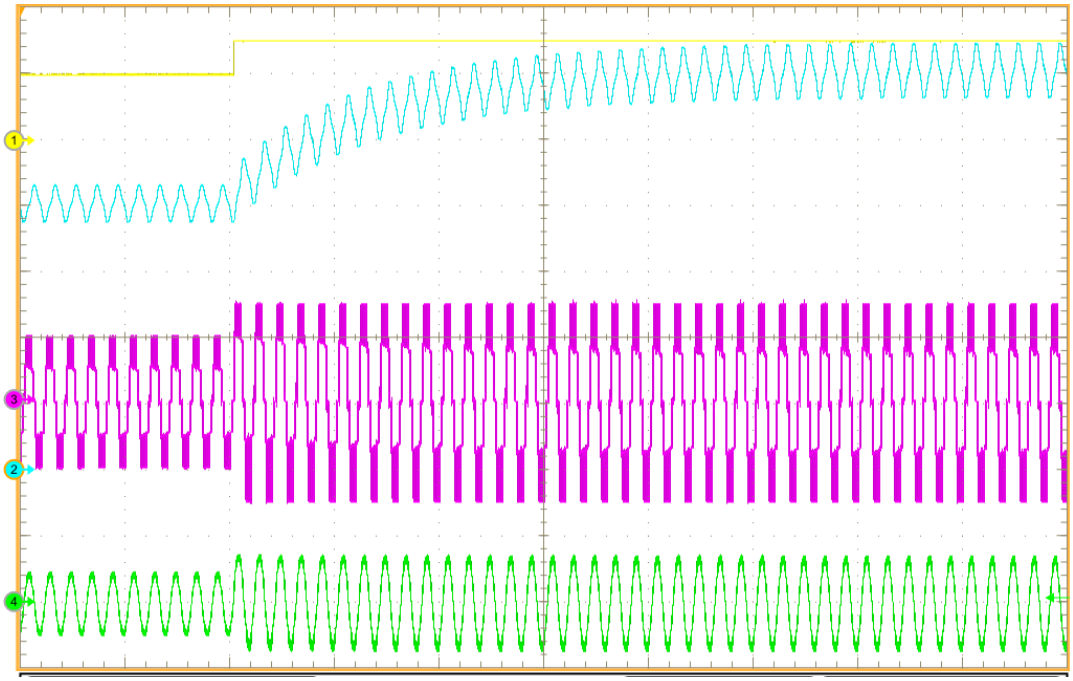

Figure 5.7: HIL result of transient behavior, slow sensorless phase-shift
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

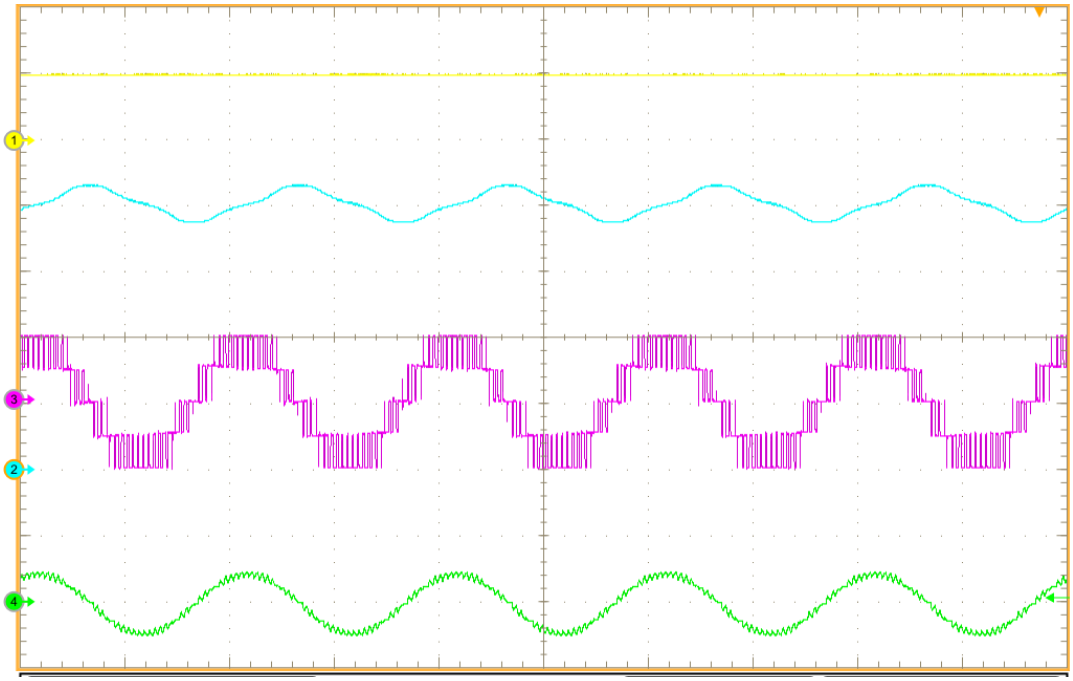

Figure 5.8: HIL result of steady state performance, slow sensorless level-shift
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

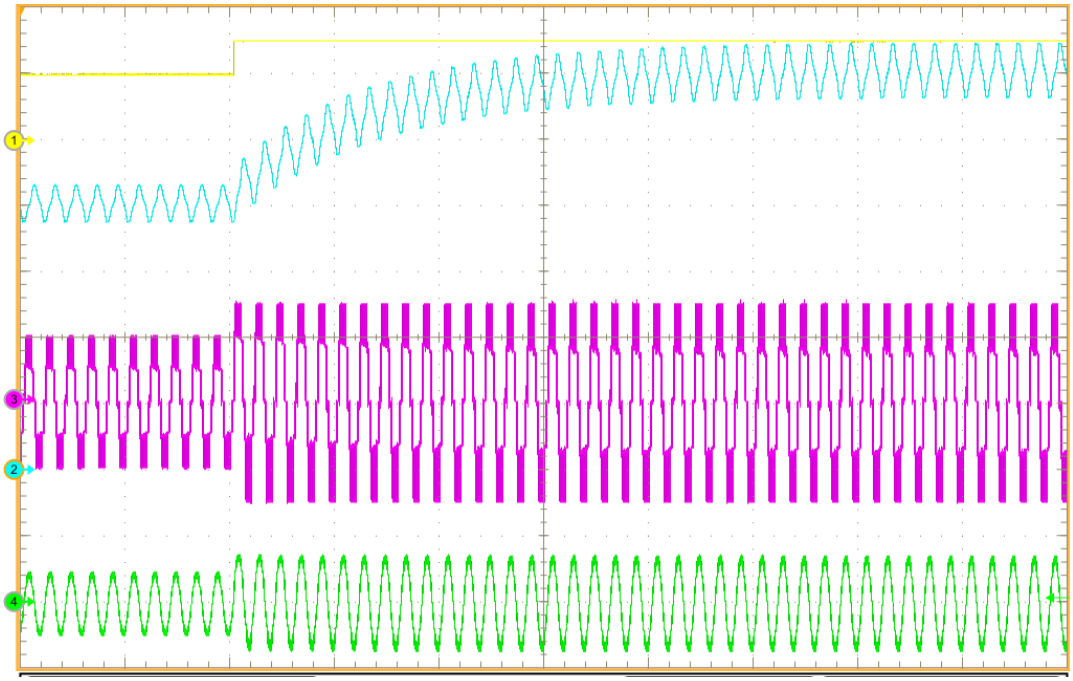

Figure 5.9: HIL result of transient behavior, slow sensorless level-shift
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

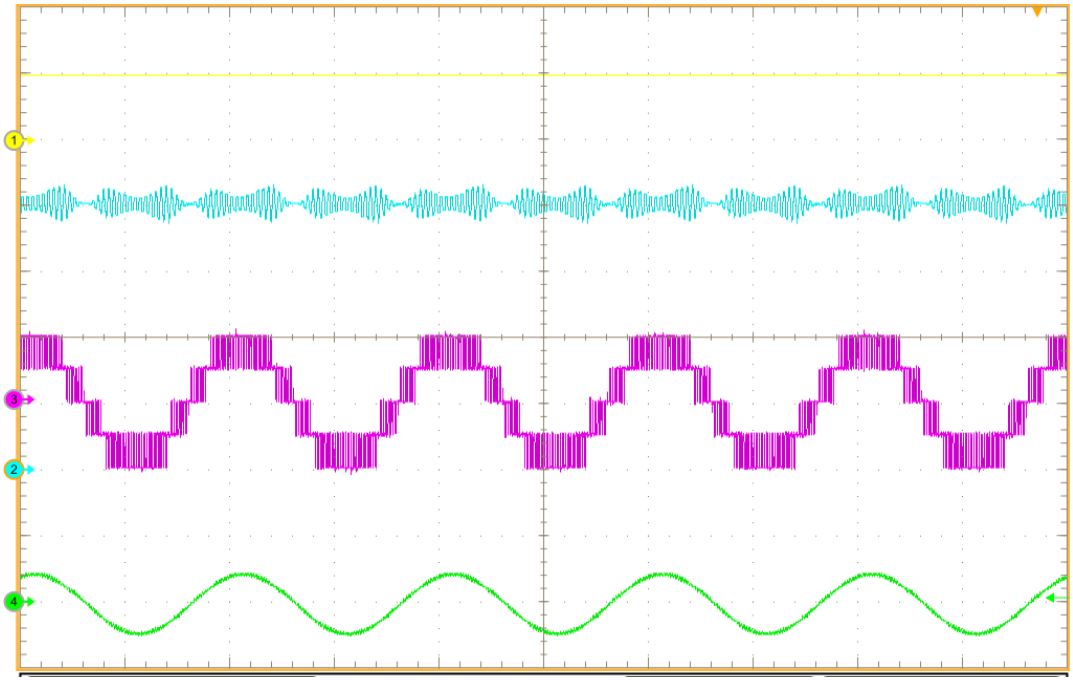

Figure 5.10: HIL result of steady state performance, fast sensorless level-shift in [12]
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

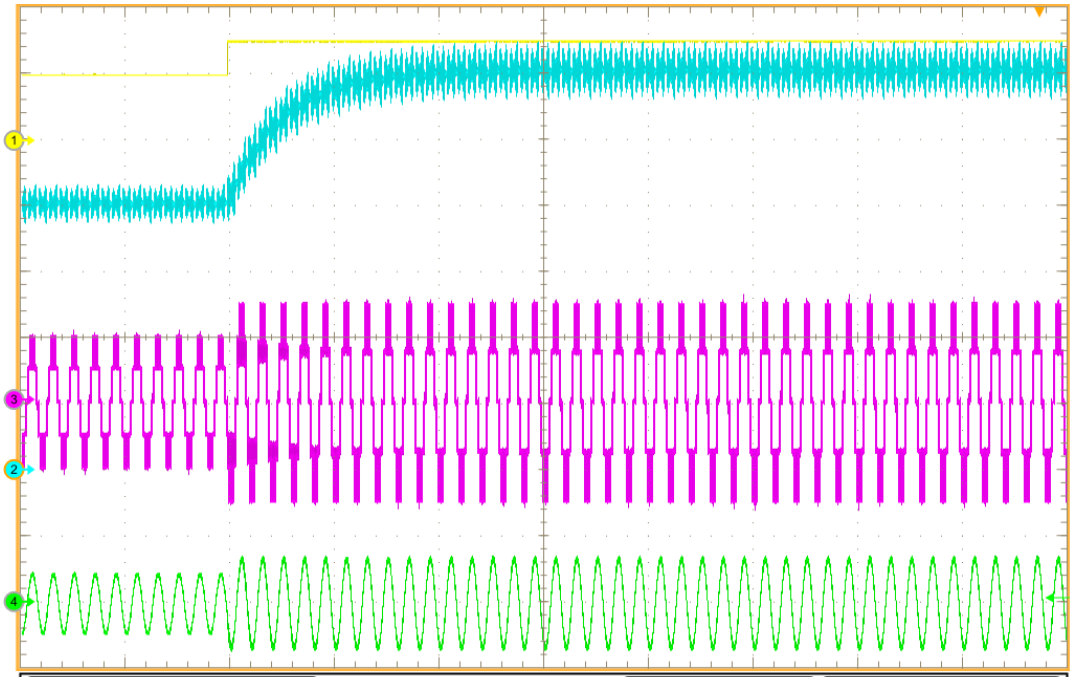

Figure 5.11: HIL result of transient behavior, fast sensorless level-shift in [12]
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

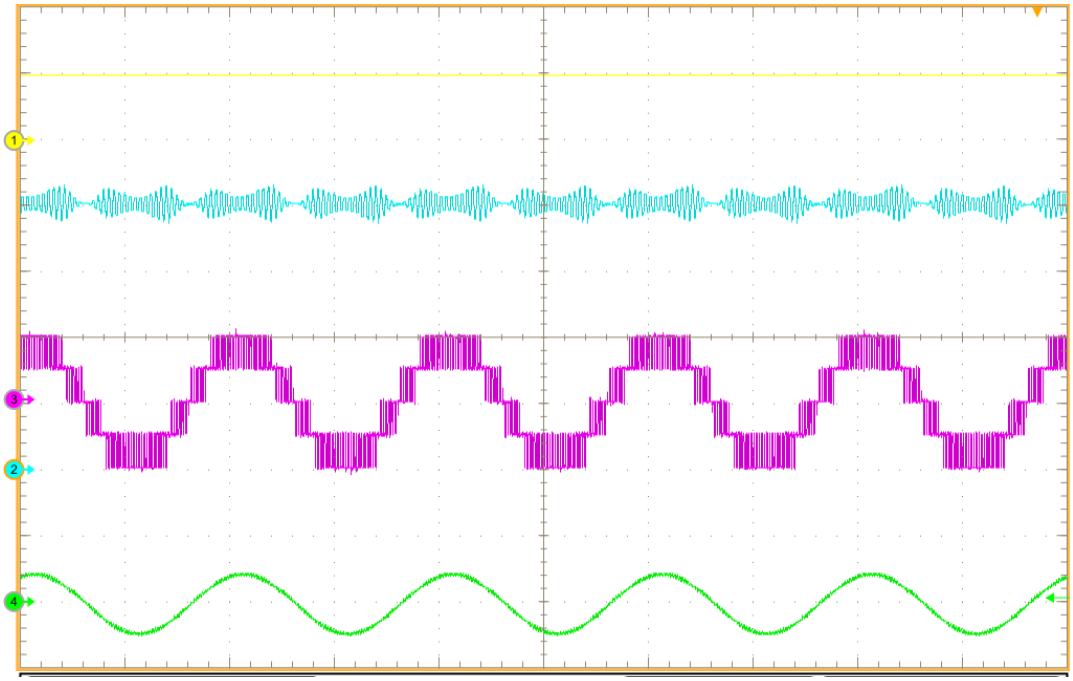

Figure 5.12: HIL result of steady state performance, fast sensorless phase-shift in [33]
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

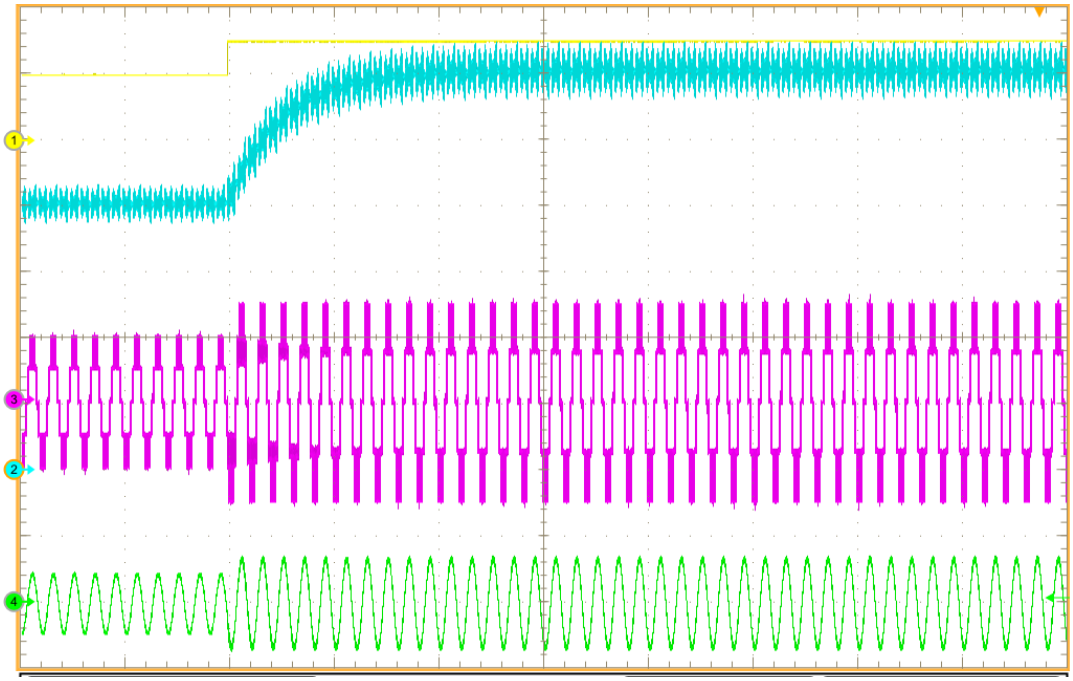

Figure 5.13: HIL result of transient behavior, fast sensorless phase-shift in [33]
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

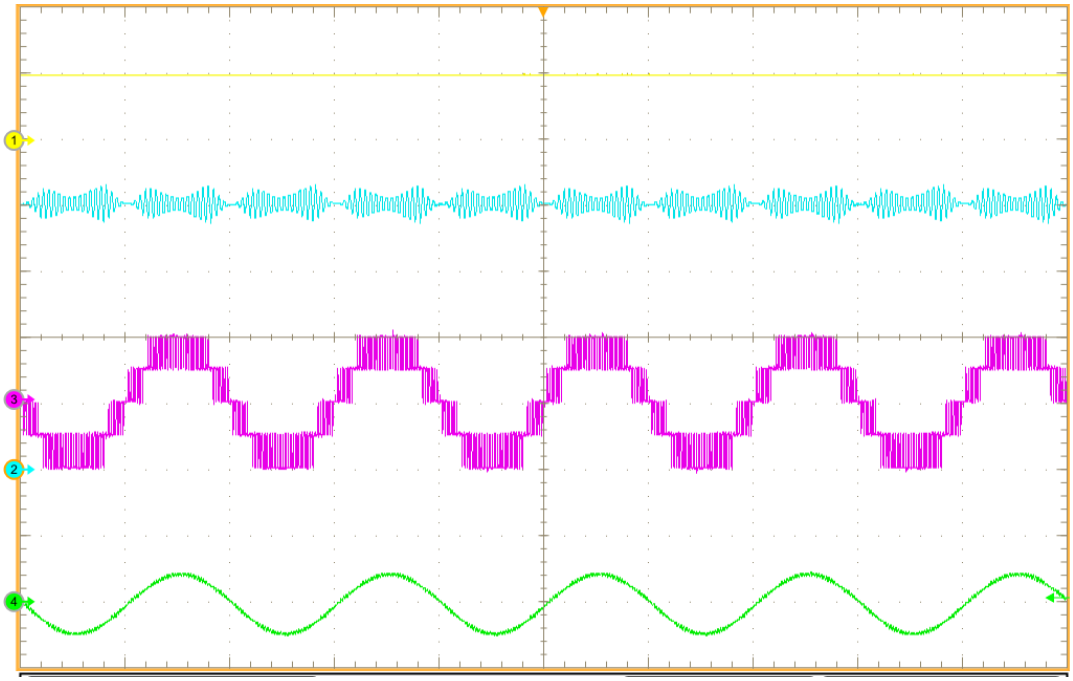

Figure 5.14: HIL result of steady state performance, proposed fast sensorless phase-shift
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

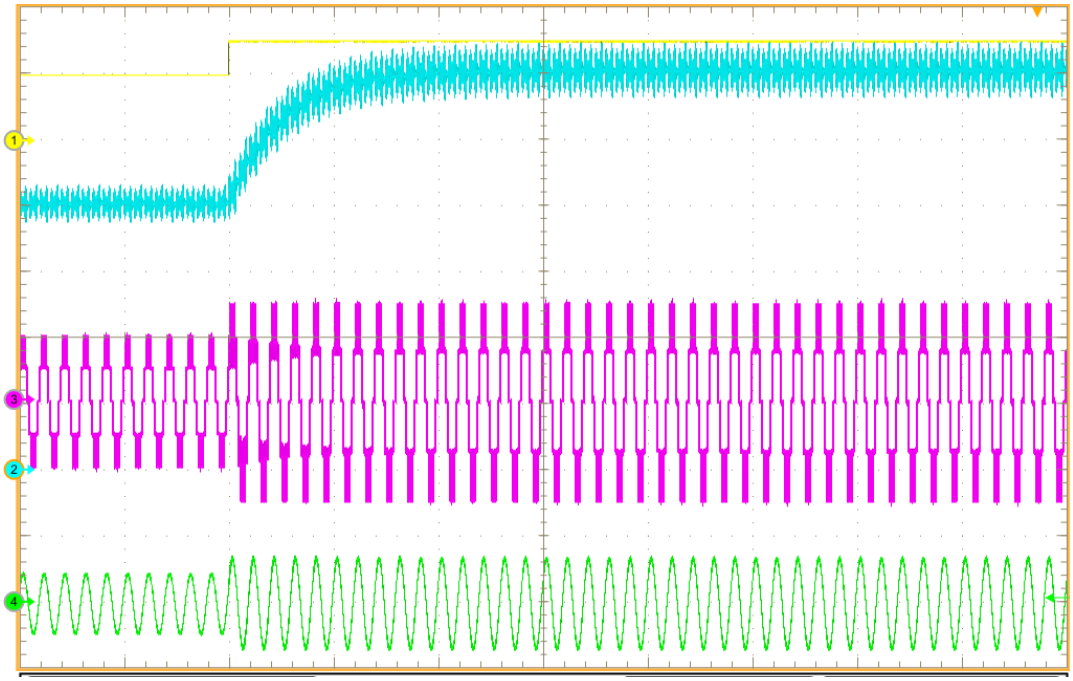

Figure 5.15: HIL result of transient behavior, proposed fast sensorless phase-shift
Ch1:200.0V/div, Ch2:25.0V/div, Ch3:200.0V/div, Ch4:10.0A/div

By comparing the result, it can concluded that all five switching methods are viable validated by hardware testing. For PUC5 converter modulated in traditional carrier based ways, the performance is almost the same. However, the slow transient behavior in Fig. 5.9 and Fig. 5.7 is not desirable. To decrease the capacitor ripple in steady state, a large auxiliary capacitor ($2000\mu F$) is needed. Therefore, their flaw can't be neglected. For the fast sensorless modulation methods, all three methods achieve similar outcomes: the auxiliary capacitor size is greatly reduced to $100\mu F$, the charging/discharging frequency is raised and thus the ripple of the auxiliary capacitor is minimized. The difference is the modulation topology itself. For the fast sensorless level-shift method in [12], it requires extra comparators and logic gates, which arises the concern of complexity and stability of the system. For the fast sensorless phase-shift method in [33], it uses a complex condition determination when comparing the carriers and the reference voltage. In a way, it also requires complex logic gates and extra comparators to achieve. Finally, for the proposed phase-shift modulation method, it evades complex logic gates and extra comparators, while achieves the desired performance for PUC5 inverter. To conclude, the pros and cons of above-mentioned five switching methods is compared in Table 5.3.

Table 5.3: HIL results comparison of five modulation methods

	complexity	capacitor size	transient behavior
slow sensorless phase-shift	low	large	bad
slow sensorless level-shift	low	large	bad
fast sensorless level-shift in [12]	high	small	good
fast sensorless phase-shift in [33]	high	small	good
proposed phase-shift	medium	small	good

6

Conclusion and Future work

6.1. Conclusion

This report gives a full review on multilevel inverter topologies and switching technologies of multilevel inverter. Among many options, PUC5 inverter with carrier-based modulation stands out for its simplicity and small size. However, the traditional carrier based modulation of PUC5 is flawed. Therefore, this report first gives a review on predecessors' attempt to improve the PUC5 inverter. Then, a fast voltage balancing with phase-shift modulation PUC5 inverter is proposed. It merges benefits of phase-shift modulation while evades the problem of slow charging/discharging frequency of auxiliary capacitor. The design is trialed in Simulink and confirmed its performance. Later, a thorough comparison of carrier-based modulation of PUC5 is conducted with hardware-in-the-loop simulation. As expected, the proposed method has the best overall performance.

6.2. Future work

This report only proposes a novel way to modulate the PUC5 inverter. However, it is an open-loop system and control is yet tested. In the future, different control methods should be implemented on the proposed PUC5 modulation method on different use cases.

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