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M.Sc. Thesis

Data Acquisition System Design for a 160x128 Single-photon Image Sensor with On-pixel 55 ps Time-to-digital Converter

Chockalingam Veerappan

Abstract

Time-resolved image sensors enabling picosecond resolutions over large formats are needed in many advanced imaging fields, from fluorescence lifetime imaging microscopy (FLIM) to positron emission tomography (PET). Integrated single-photon avalanche diode (SPAD) technology embodies the new frontiers of time-resolved imaging, namely better instrument response function, increased throughput and lower costs. SPADs have recently developed onto large arrays with increasing on-chip functionality. With larger array sizes however, the data generation rate has become a throughput bottleneck and thus necessitating an efficient data acquisition system.

In this thesis a data acquisition system was developed, for one of the largest single-photon imager ever devised with 160x128 pixels capable of detecting the time-of-arrival of single photons with picosecond resolution. To handle the gigabytes of data generated every second, techniques such as a column based event-driven system for photon-starved applications was implemented.

The thesis presents a test strategy and characterization methodology. Using the developed data acquisition system, the imager was tested and characterized successfully. To conclude, an example of a biological sample imaged with FLIM is shown as a demonstration of the potentialities of our system.

Data Acquisition System Design for a 160x128 Single-photon Image Sensor with On-pixel 55 ps Time-to-digital Converter

Thesis

submitted in partial fulfillment of the
requirements for the degree of

Master of Science

in

Microelectronics

by

Chockalingam Veerappan
born in Coimbatore, India

This work was performed in:

Circuits and Systems Group
Department of Microelectronics & Computer Engineering
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Delft University of Technology
Department of
Microelectronics & Computer Engineering

The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled **"Data Acquisition System Design for a 160x128 Single-photon Image Sensor with On-pixel 55 ps Time-to-digital Converter"** by **Chockalingam Veerappan** in partial fulfillment of the requirements for the degree of **Master of Science**.

Dated: 26 November 2010

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Chockalingam Veerappan
Delft, The Netherlands
26 November 2010

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1 Introduction

1.1 Motivation

Image sensors capable of resolving the time-of-arrival (TOA) of individual photons with high resolution are needed in several applications, such as Fluorescence lifetime imaging microscopy (FLIM), Forster resonance energy transfer (FRET), optical range finding, Positron emission tomography (PET) and Fluorescence correlation spectroscopy (FCS). For instance in fluorescence lifetime imaging microscopy application the lifetime of the fluorescent marker used to study a biological specimen is generally in the order of a few nanoseconds. However, due to fluorescence quenching, the observed lifetime in the fluorescence lifetime imaging application can drop down to less than 100 ps [1]. In FRET the observed fluorescence lifetime is generally in the range of 100 to 300 ps [1]. Hence, to resolve the fluorescence lifetime in these applications prompts the need for deep sub-nanosecond resolution in the instrument response function (IRF) of the overall optical system. This inturn requires new time-resolved image sensors with higher time resolution, increased throughput, and lower costs.

The general trend is to reach a picosecond time resolution with millions of measurements per second and an increasing image resolution. Photomultiplier tubes are capable of high time resolution over relatively large sensitive areas but lack imaging capability that is usually achieved via optical scanning. Multi-channel plates provide such capability but are still relatively bulky and costly. Solid-state avalanche photodiodes operated in Geiger mode, or single-photon avalanche diodes (SPADs), have existed for decades [2] and are increasingly adopted as a good compromise between cost and performance, especially after multi-pixel CMOS SPAD imagers have appeared [3, 4, 5].

As SPAD array sizes have grown, the on-chip readout bottle neck has also become evident leading to hybrid designs involving complex technological solutions [6] or more integration and more parallelism on-chip [7]. This trend has accelerated with the introduction of SPAD devices in deep-submicron CMOS [8] that have enabled the design of massively parallel arrays where the entire photon detection and TOA circuitry, is integrated on pixel [9, 10, 11]. This thesis revolves around one such imager also known as the *Megaframe 128* or *MF128*. The MF128 was developed in a project called as *Megaframe*, supported by the European Union within the Sixth Framework Program IST FET open.

The MF128 is one of the largest single-photon imager with 160x128 pixels capable of detecting the time-of-arrival of single photons with picosecond resolution; the chip was implemented in a 130nm CMOS technology. The pixel count in this imager is about twenty times larger than the state of the art in-pixel time-resolved imagers, proposed in [9, 10, 11]. Advantages in increasing pixel count come along with its own challenges. The major challenge that we anticipate in using the MF128 is the data generation rate.

For example the MF128 can generate about 1.28 GB/sec, while operating the imager at 50 kilo frames per second.

Further, since the MF128 being one of its kind ever realized to date with around 20,480 SPAD-TDC pixels, puts forth various interesting questions such as

1. What is the effect on the performance of the SPAD-TDC array on scaling?

2. What methodology can be used to analyze and study scaling?

3. And on what parameters does the scaling effect depend?

1.2 Contribution

This thesis concentrates on developing a data acquisition system for the MF128 imager that can be used for various applications such as wide field fluorescence lifetime imaging, positron emission tomography etc. However, in this thesis the developed data acquisition system is utilized mainly to study and characterize the MF128 imager. Furthermore, based on the knowledge gathered on the chip architecture, various methodologies to test the imager were proposed, implemented and tested using the data acquisition system. Hence, the test functions developed during the course of this thesis can be scripted later to automate the testing process of the imager. Finally the developed data acquisition system is used to perform wide field fluorescence lifetime imaging, where a pine pollen grain is observed.

The main contributions of this thesis are:

1. Development of a flexible data acquisition system for the MF128 imager.

    - Design and implementation of a column based event driven system to reduce the data rate for photon-starved applications.
    - Development of a fast data acquisition technique to perform code intensity test on all the pixels simultaneously. By implementing time interleaved sampling on the data generated by noisy pixels.

2. Development of various test methodologies to test various basic modules of the imager, with the aim of automating the test process later.

3. Study on the performance degradation of the SPAD-TDC array with scaling was carried out, after formulating a study methodology.

4. Backend tool to generate FLIM images based on the raw data collected from the MF128 imager was also developed.

1.3 Overview

The thesis is split in two parts. The first part describes the data acquisition system developed for the MF128 imager. The second part of the thesis presents the proposed test methodologies along with the testing and characterization results of the imager. Finally the results of the fluorescence lifetime imaging technique realized using the MF128 are presented.

The organization of the thesis is as follows: Chapter 2 elucidates the architecture of the MF128 imager. Where the internal design of the imager is analyzed using the top-down approach. Chapter 3 presents the architecture of the developed data acquisition system, explaining the various strategies used to optimize the data transfer rate.

Chapter 4 and Chapter 5 focus on the testing and characterization of the MF128 imager. Where Chapter 4 concentrates on the time-uncorrelated single photon counting (TUPC) mode and Chapter 5 focuses on the time-correlated single photon counting (TCSPC) mode. The test methodologies used to test and characterize the basic modules required for the TUPC mode is presented in Chapter 4. Further the characterization results of the imager in the TUPC mode are also presented. Chapter 5 discusses the test strategy used to test the TCSPC mode. Then it presents and explains the experimental results of the imager in TCSPC mode. Further, the fluorescence lifetime imaging technique realized using the developed data acquisition system is also presented in this chapter. Finally, Chapter 6 concludes the thesis, providing the summary of the results, along with the possible future directions.

2 MF128 Architecture

The aim of this chapter is to elucidate the study made on the internal design of the MF128 chip. In this study, the chip is analyzed by breaking it down into smaller modules. Conventionally, the method of analyzing a big design by breaking it into smaller modules is known as the top-down approach. This method of analysis will provide the insight into the internal architecture of the chip.

The organization of the chapter is the following: first the overview of the MF128 chip architecture is briefed in Section 2.1. Followed by this, the MF128 chip is studied by categorizing the internal modules of the chip, based on their functionality in Section 2.2. Further, each category is analyzed by breaking it into various basic functional units as discussed in Section 2.3, Section 2.4 and Section 2.5. The summary of the chapter is presented in Section 2.6.

2.1 Megaframe chip architecture overview

The MF128 chip is an image sensor with 160x128 pixels capable of measuring the time-of-arrival of single photons. To realize this functionality every pixel contains a single photon detector along with a time-of-arrival measurement unit. The block diagram of the imager is shown in Figure 2.1. The sensor is partitioned in four identical quadrants that are served by a balanced clock tree so as to minimize skews and ensure the fastest possible readout process. The ten bit data generated by every pixel is sent out serially using two independent serializers for every column. The region of interest (ROI) is programmable via vertical and horizontal registers that select a section of the pixel array that needs to be active. In addition to 128 rows of pixels, the MF128 has two additional header rows near the serializer. These header pixels were introduced to increase the readability of the generated data. The pixels in the header row are capable of generating ten bit data, with seven bits representing the frame count. The frame count is monitored in every header pixel using a seven bit counter.

The MF128 image sensor is designed to work in two different modes of operation, one the Time Uncorrelated Photon Counting (TUPC) mode or the intensity mode and second the Time-Correlated Single Photon Counting (TCSPC) mode. In the time-uncorrelated mode the sensor counts the number of photons arrived in a period of time. Whereas in the time-correlated mode the time-of-arrival of every detected photon is measured, with respect to a time reference. All configurations and control of the state of the chip are carried out using an I2C module.

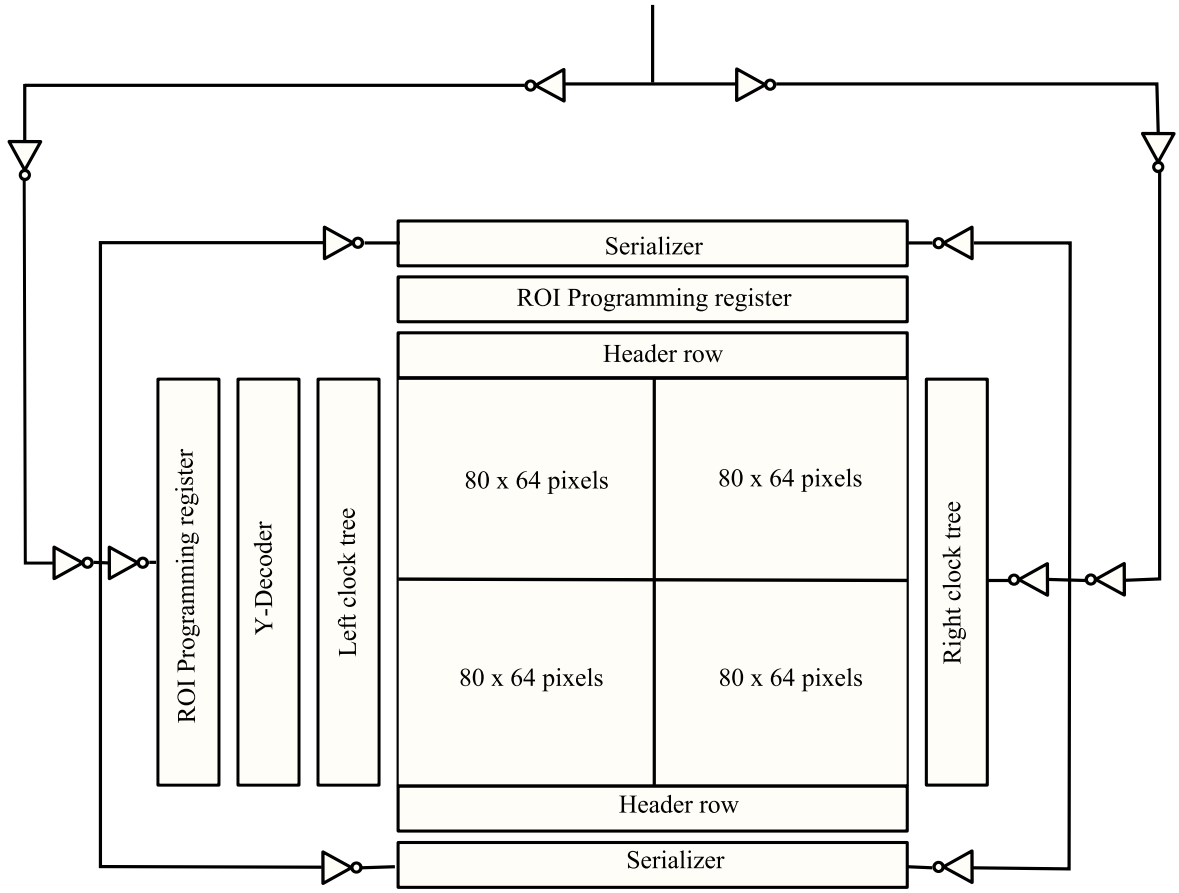

Figure 2.1: MF128 Block digram [12]

2.2 Categorization of internal modules

To realize an imager as defined in Section 2.1, the chip contains various modules. These modules can be classified into three categories based on their functionality, namely: a pixel array, a data readout system and the configuration system.

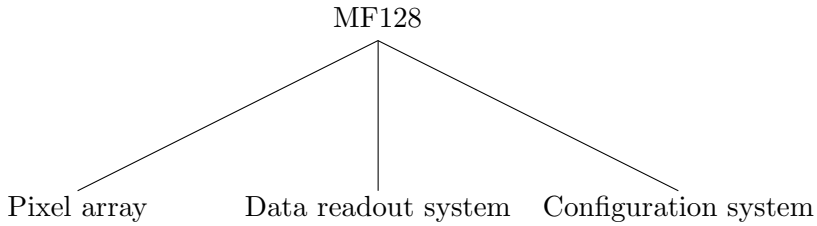

Figure 2.2: Categorization of internal modules

The functionality of each of the category is identified as follows:

1. Pixel array: The functionality of the pixel array is to detect and measure the time of arrival/intensity of the detected photon(s).

2. Data readout system: The readout system is used to read and communicate the measured data, from the pixel array to the interface circuitry located outside the chip.

3. Configuration system: The configuration system facilitates the user to configure and control the operating mode/conditions of the pixel array/readout system.

The three categories introduced in this section are elaborated in Section 2.3, Section 2.4 and Section 2.5 respectively.

2.3 Pixel array

The MF128 chip contains an array of 160x128 pixels (160 columns and 128 rows). Where, every pixel in the array is designed to detect and measure the photon arrival time/photon intensity, irrespective of other pixels. Since the functionality of every pixel is identical and independent of the other pixels, it is possible to define the architecture of one pixel and then extend it to the whole array. Therefore in this section the internal design of a single pixel is explained in detail.

Pixel Architecture

In the MF128 chip every pixel is designed to have its own photon detector, measurement unit and a 10 bit buffer. In addition to the detector and a measurement unit, every pixel incorporates circuitry that can facilitate the testability and the pixel activation/deactivation.

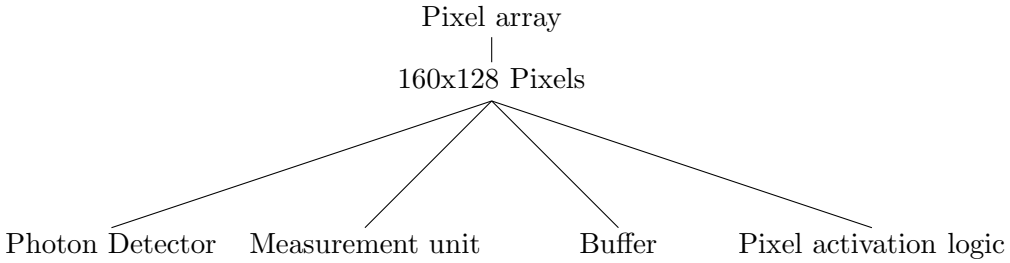

Figure 2.3: Pixel contents

2.3.1 The Photon detector

The detector implemented in the Megaframe chip is a single-photon detector called as Single Photon Avalanche Diode (SPAD). The design and implementation of the SPAD proposed by C. Niclass et al [13], M. Gersbach et al [14] and J.Richardson et al [8] for 130 nm CMOS technology is used in the megaframe MF128 chip.

SPAD

The SPAD is a PN junction photo diode, reverse biased above the breakdown voltage. In this mode of operation called as the geiger mode, a photo electron created in the depletion region might create an avalanche by impact ionization [15]. The high current resulting from the avalanche signifies the arrival of a photon. However, the avalanche current needs to be quenched, to avoid a thermal breakdown in the diode. To quench the avalanche two types of techniques [16] viz. active quenching and passive quenching are discussed in the literature. Of these two techniques the passive quenching technique [8] is used in the MF128 chip.

Quenching circuitry

In the MF128 chip a transistor, biased to act as a current source, is added in series to the SPAD. In this configuration, the current resulting from the avalanche increases the voltage drop across the transistor. This in turn reduces the voltage across the SPAD. As the bias voltage across the SPAD reduces to near breakdown voltage, the avalanche gets quenched [15]. After the avalanche gets quenched, the associated junction capacitance of the SPAD recharges to its original working condition through the quenching resistor. The total time required to quench and recharge the SPAD back to its working condition is called as the dead time of the SPAD.

During the avalanche and in the process of quenching and recharge, a voltage pulse is developed across the quenching resistor. This voltage pulse is used in the MF128 to detect the arrival of a photon. To map this voltage pulse to the conventional CMOS domain for further processing, an inverter is added.

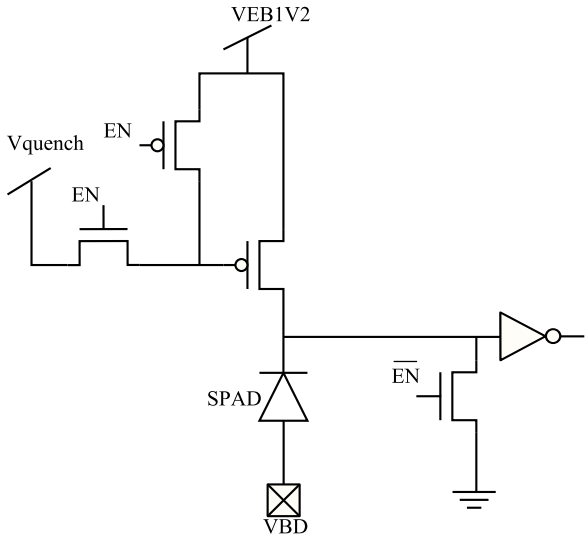

Figure 2.4: Photon detector or SPAD ensemble [12]

Figure 2.4 shows the passive quenching circuitry implemented in MF128 along with the SPAD. The pixel implemented in the MF128 chip offers the flexibility to vary the bias conditions of the SPAD.

The options available to the user to vary the SPADs bias conditions are:

1. Voltage across the SPAD (V_{op}) can be varied by changing V_{bd}.
2. Quenching current value can be adjusted by varying Vquench.
3. SPAD can be activated/deactivated by toggling the enable (EN) signal.

2.3.2 Measurement unit

The SPAD along with its quenching circuitry detects the arrival of a photon. For every detected photon, the detector generates a voltage pulse. This voltage pulse is used by the measurement unit, to measure the photon arrival time/ photon count. In the MF128 chip, the photon counting feature is incorporated into the time of arrival measurement module. The time-of-arrival measurement module is a time-to-digital converter (TDC). Because this module generates a digital code, that is proportional to the time difference between two signals viz., the START and the STOP signal. Where the START signal comes from the photon detector and the STOP signal comes from a reference clock. The researchers involved in designing the Megaframe chip designed three different TDC designs [10, 11, 9]. Of these three designs, in the MF128 chip the design proposed by Justin Richardson et al [10] is implemented. This design is briefed in the next paragraph.

Ring oscillator based TDC

The TDC used in the MF128 chip is based on a ring oscillator with fast start-up as shown in Figure 2.5. The ring oscillator gets activated whenever the START signal transits to a high state. And remains activated till the STOP signal goes high. The activated oscillator generates clock cycles via $B3$, $\overline{B3}$, which is then counted using a seven bit ripple-counter. The output of the seven bit ripple counter serves as a seven most-significant-bits of the measurement. The three least-significant-bits of the measurement are provided by the eight intermediate state of the ring oscillator. The intermediate states of the ring oscillator are latched using the control signal T and converted to a three bit binary code ($D0 : D2$) using a thermometer decoder as shown in Figure 2.6. The stop signal S, $\overline{S}$ is used to freeze the ring oscillator, while the rising edge of R resets the TDC. In TUPC mode the seven bit ripple counter is also used to count the detected photons.

Process Voltage and Temperature (PVT) compensation [10]

To reduce the jitter introduced by the supply voltage variations, a differential inverter with a NMOS based supply regulation is used as a delay element in the ring oscillator. The NMOS based supply regulation forms a part of the Process Voltage and Temperature (PVT) variations control loop. The PVT variations control loop is a closed loop calibration system implemented outside the pixel array, using the PLL architecture as shown in Figure 2.7. This calibration system is designed to lock the ring oscillator's output to a stable input clock, using a PLL. It is to be noted that the ring oscillator used in the PLL is identical to the ring oscillator implemented inside the TDC. The VCO voltage generated by the locked-in PLL loop is used to control the supply voltage of the ring oscillators in the TDC.

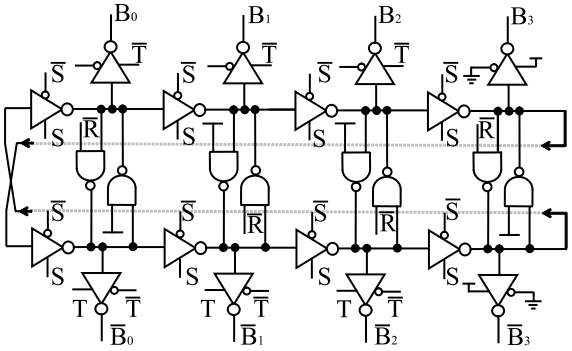

Figure 2.5: Ring oscillator schematic

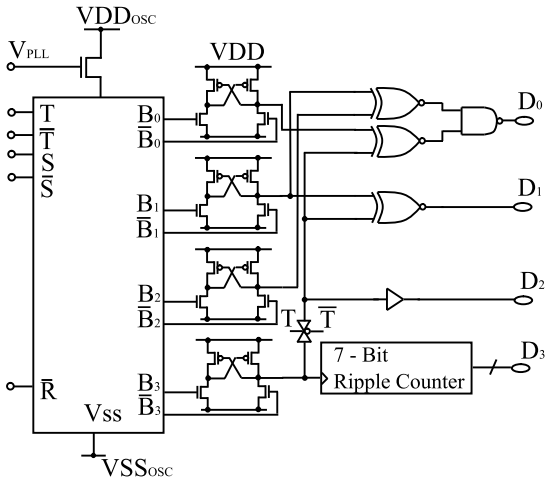

Figure 2.6: TDC schematic

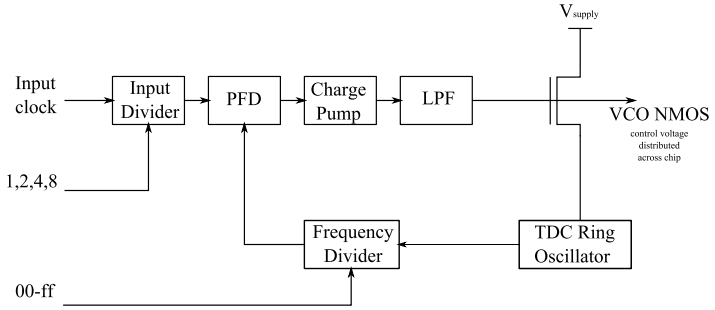

Figure 2.7: Process Voltage Temperature (PVT) variation control loop [10]

2.3.3 Buffer

Every pixel in the chip has a ten bit memory to store the measured data. The stored data is then communicated to the readout system.

2.3.4 Pixel enable / disable logic

The pixel activation logic in MF128 is designed to act in two levels. In the first level it is possible to activate the measurement unit alone. In the second level the whole pixel including the detector and the measurement unit can be activated.

The activation/deactivation logic depends on three signals viz., the ROW enable, the COLUMN enable and the global SPAD enable signal. Where the ROW enable and COLUMN enable signal comes from an on chip register that can be programmed by the user. And the global SPAD enable signal is provided by the user from outside the chip.

In the first level, the measurement unit is activated using the ROW enable and the COLUMN enable signal. Then in the second level, the entire pixel is activated using the global SPAD enable signal along with the ROW enable and COLUMN enable signal.

Figure 2.8: Pixel enable logic [12]

The implemented pixel activation/deactivation logic is shown in Figure 2.8.

2.3.5 Design for testability

To facilitate testability, every pixel contains two MUXs. One MUX is used to select an input to the TDC, while the other MUX is used to select a source for the pixel's output. The input to the TDC can either be from a photon detector or the TEST start signal that can be controlled externally by the user. The least significant bit in the pixels output can be controlled either directly by the photon detector output or by the LSB of the TDC. The select signals for the two MUXs are controlled using a user programmable register. Using the TEST start signal it is plausible to test the TDC by providing a known start signal. Whereas by monitoring the photon detector output it is possible to test the photon detector. Hence by using these two MUXs the photon detector and the TDC can be tested separately.

The overall pixel architecture with the entire set of control signals is shown in Figure 2.9

2.4 Readout system

The readout system in the megaframe chip is designed to collect and transfer the data, from the pixel to the circuitry located outside the chip. It is worth mentioning here, that every pixel in the MF128 chip generates 10 bits at a frame rate of one megahertz. The megaframe chip which contains 160x128 pixels including the header pixels will then generate 160x128x10 bits for every micro second. To handle this large amount of data, a robust readout system is required.

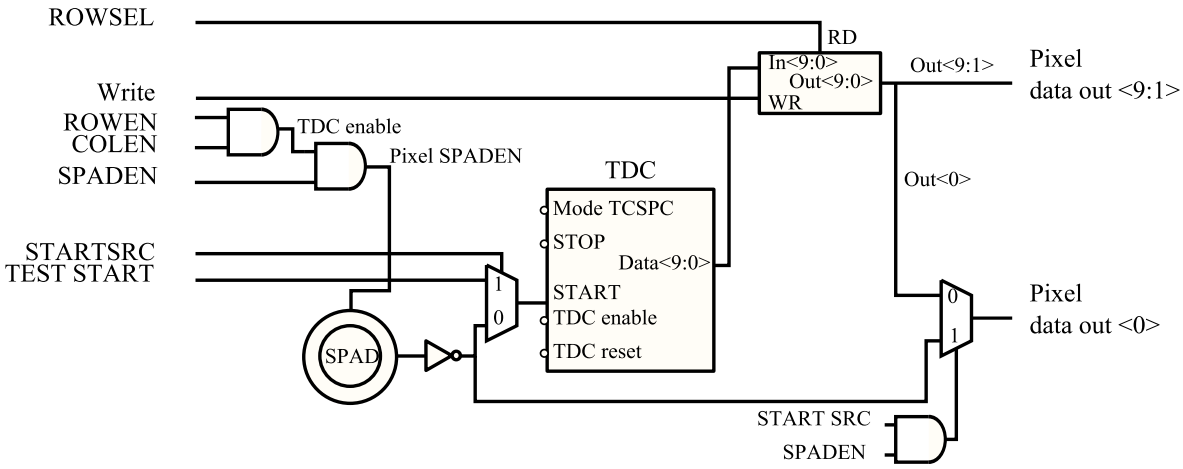

Figure 2.9: Pixel Architecture [12]

The readout system of the Megaframe chip is split into two identical halves, where each half of the readout system is responsible for the readout of one half of the pixels i.e. 160x64 pixels. These 160x64 pixels are organized into 160 columns and 64 rows. The output of every pixel in a column is connected to a common data bus. The serializer also connected to the data bus reads the 10 bit data from the data bus and converts it into a serial data. This serial data is finally transferred to the circuitry located outside the chip.

To facilitate the sharing of the data bus between the pixels in a column, a Y-decoder is implemented. The Y-decoder time multiplex's the data bus between the various pixels of a column. The time multiplexing is implemented, such that the row readout happens sequentially in a rolling shutter mode. The ROWSEL signal generated by the Y-decoder is used to read a particular pixel row as shown in Figure 2.10.

To synchronize the data readout, the Y decoder and the serializer uses three different clocks namely the data clock, the line clock and the frame clock. The data clock is used by the serializer to transfer the data serially. The line clock instructs the Y-decoder and serializer to read the next row. The frame clock instructs the Y-decoder that the frame readout is over. Since the data generated by every pixel is 10 bits, line clock is 10 times the data clock and the frame clock needs to be 65 times the line clock when all the rows are active.

2.4.1 Data compression technique

As mentioned earlier, the data generation rate in MF128 is very high. So to reduce the data transfer rate from MF128, two compression techniques are implemented on chip. The first technique is based on the IEM algorithm [17] and the second is an event-driven serializer that exploits the scarcity of the data in a frame. Since the on chip data compression techniques are not explored in this thesis, it is not explained in detail here. However, the detailed explanation of the same can be found in [12].

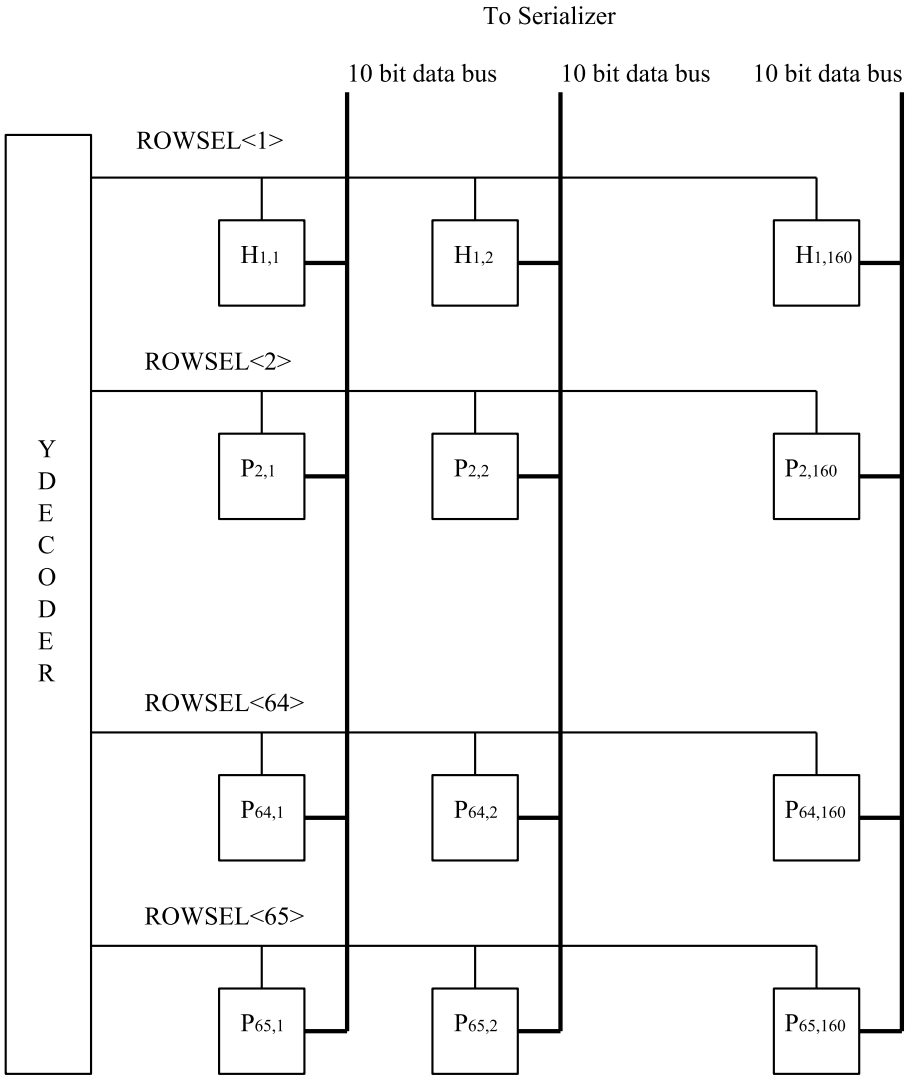

Figure 2.10: Simplified readout system

2.5 System configuration module

The pixel array and the readout system are designed such that it can be configured to work in various modes of operations. The configuration and control feasibilities available on chip are made visible to the user through a set of configuration registers. The configuration registers available on chip are designed to be programmed either using the inter integrated circuits (I2C) protocol or the serial interface.

2.5.1 I2C

The Megaframe chip contains a group of registers that can be configured using the I2C protocol [18]. To facilitate the communication a I2C slave module is implemented in the megaframe chip. In general the registers that are visible through the I2C communication are responsible to configure various modules. A tabulation listing various registers

along with its address and functionality is re-produced from [12] in Appendix A.

2.5.2 ROWEN/COLEN

In MF128, pixels in the region of interest can be activated using two registers viz. ROWEN and COLEN. The ROWEN and COLEN are two shift registers, each of width 130 and 160 bits respectively, where every bit in the ROWEN and COLEN register corresponds to a row and a column in the pixel array. Hence a specific pixel can be activated by configuring its corresponding row and column bit in the ROWEN and COLEN register. The ROWEN and COLEN registers are designed to be configured serially by the user.

2.6 Summary

- MF128 is designed to work in two modes of operation viz. time-uncorrelated and time-correlated single photon counting.
- Internal modules of the MF128 are categorized into three categories viz. pixel array, readout system and a configuration system.
- Pixel array contains 160x128 pixels. Where every pixel contains a photon detector and a TDC.
- Readout system is made up of two serializers and a Y-decoder.
- Configuration system contains a set of registers programmable either using a I2C protocol or serial communication.
- Additionally data compression techniques such as IEM and event driven serializer are implemented in MF128.

The top down approach followed in this chapter to analyze the MF128 imager is summarized pictorially in Figure 2.11.

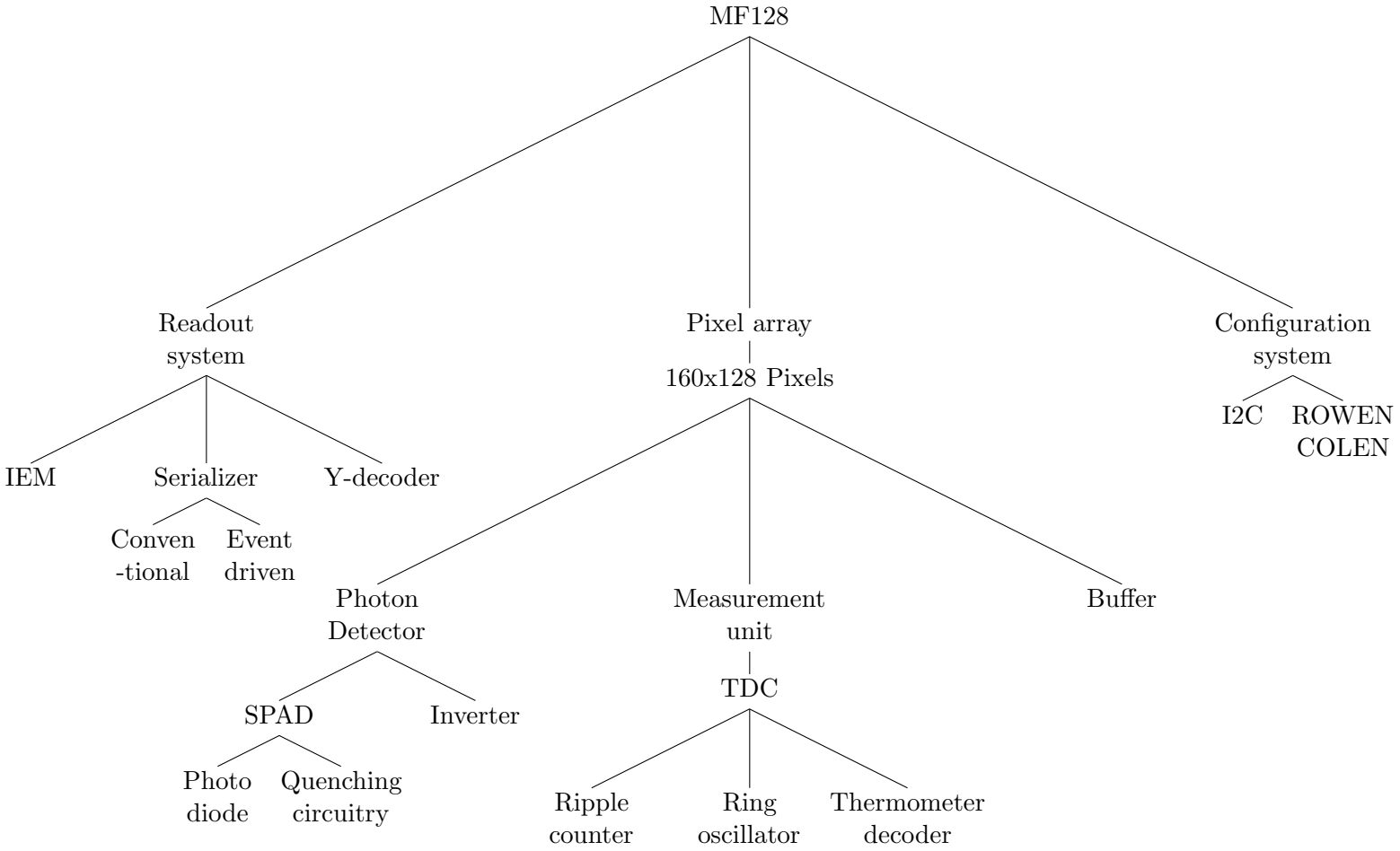

Figure 2.11: MF128 architecture summary

3 Data acquisition system

The goal of this chapter is to present the design of the data acquisition system developed for the MF128 imager. The MF128 is a time resolved imager, with 160x128 pixels capable of working in two different operating modes, namely the Time Un-correlated Photon Counting (TUPC) mode and Time Correlated Single Photon Counting (TCSPC) mode. Chapter 2 categorized the internal module of the imager into three categories namely the pixel array, readout system and the configuration system. Even though the pixel array forms the core of the imager, the configuration system and the readout system provide the user with the access to operate the chip. Hence in this chapter the configuration and readout system are analyzed to derive the specifications for the data acquisition system to control, configure and acquire data from the imager. Later the derived specifications are used to design a data acquisition system.

Organization of the chapter is as follows: In Section 3.1 the MF128 architecture is analyzed to obtain the specification for the data acquisition system. The derived specification where then used to analyze the available data acquisition system in Section 3.2. In Section 3.3 the hardware set-up realized for the MF128 is presented. Extending the discussion on the hardware setup, an overview of the developed data acquisition system is presented in Section 3.4. Following the overview a detailed design of the system is explained in Section 3.5and Section 3.6. Further , three application specific data compression techniques are presented in Section 3.7 . Finally, the chapter is summarized in Section 3.8.

3.1 Specification

3.1.1 Light source insensitivity

The MF128 imager can be operated with a variety of light sources, including high performance lasers (such as femtosecond lasers of the type Mira and MaiTai) and cheaper laser diodes. To accommodate the differing properties of these devices, a number of clocking options must be provided. Specifically, it should be possible to operate in a master mode, where the data acquisition system drives a pulse train into the illumination source, and a slave mode, where the output of a self-oscillating source is optically captured and used as the reference for the various system clocks. Figure 3.1 provides a simplified illustration of this configuration.

3.1.2 Requirements to communicate with the MF128 imager

As stated earlier, the data acquisition system is required to control, configure and acquire the data from the imager. Hence to design such a system, first it is important to understand the communication protocol the MF128 imager uses to communicate

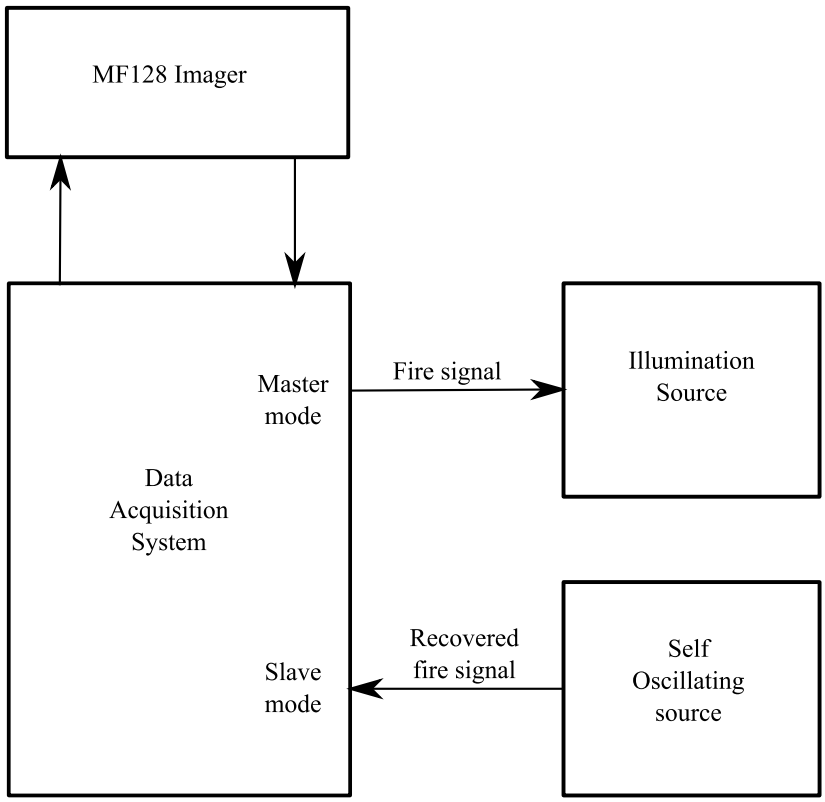

Figure 3.1: Light source control: Master/Slave mode

with the outside world. This information can be extracted from the Chapter 2 on the MF128 architecture.

The signal lines required to communicate with the MF128 imager can be classified into three categories, namely:

1. Control signals
2. Chip configuration signals
3. Data readout signals

The control signals

In MF128 five signals can be classified in this category, viz. the SPAD enable, TDC reset, write signal, TEST start and the external STOP. All these five signals are global signals routed to all the pixels in the array.

- *SPAD enable:*The SPAD enable signal is used to enable or disable the SPAD.
- *TDC reset:* The TDC reset signal is used to reset the measurement unit. Hence, this signal needs to be activated at the start of every frame, to reset the data measured in the previous frame.

- *Write:* This signal is used to write the measurement unit output on to a 10-bit buffer present inside every pixel, which is then used by the readout system. Therefore, this signal needs to be activated just before the end of every frame. Hence, the light exposure duration for every frame in MF128 imagers is defined as the time interval between the TDC reset and write signal.
- *TEST start:* As mentioned in Chapter 2, the TEST start can be used to test the measurement unit. Since this signal can be controlled directly from outside, it does not need to follow any specific protocol. Therefore, depending on the test vector this signal can be modified accordingly.
- *External STOP:* External STOP signal can be used either to provide the STOP signal for the measurement unit during its testing phase or when it is required to excite a light source i.e. while operating the light source as a slave to the data acquisition system.

Chip configuration signals:

As stated in Chapter 2, the MF128 imager contains two modules to facilitate the chip configuration. These two modules are I2C and ROWEN/COLEN.

- *I2C:* The I2C slave module in MF128 uses the I2C protocol for communication. Hence an I2C master module is required to establish the communication with the I2C slave implemented on-chip. In general I2C protocol requires two signals namely the SDA and SCL. Where the SDA is the data line and SCL is the clock line signifying the data communication. It should be noted that this module is designed to operate at 400 kHz. The detailed description of the I2C protocol can be found in [18].
- *ROWEN/COLEN:* The configuration register present in this module uses a serial communication. Hence each of these registers requires two signal lines namely, the data and the clock.

Data readout signals:

The data readout system implemented in the MF128 imager requires three signals, namely the data clock, line clock and the frame clock.

- *Data clock:* Data clock is used by the serializers on-chip to communicate the data. Hence the frequency of the data-clock determines the data rate from the imager.
- *Line clock:* Line clock is used to request the imager to send the next row of data. Therefore to ensure reliable data transfer the time period of the line clock needs to be at-least n times the data clock time period. Where n is the number of data bits per pixel. In MF128 while using the conventional serializer n is equal to 10 bits.
- *Frame clock:* Frame clock is used to signify the end of frame readout. Hence the time period of this clock needs to be at-least active row times the line clock time period.

Hence to ensure reliable data transfer from the imager, the signals presented in this section should follow the timing requirements presented in Figure 3.2.

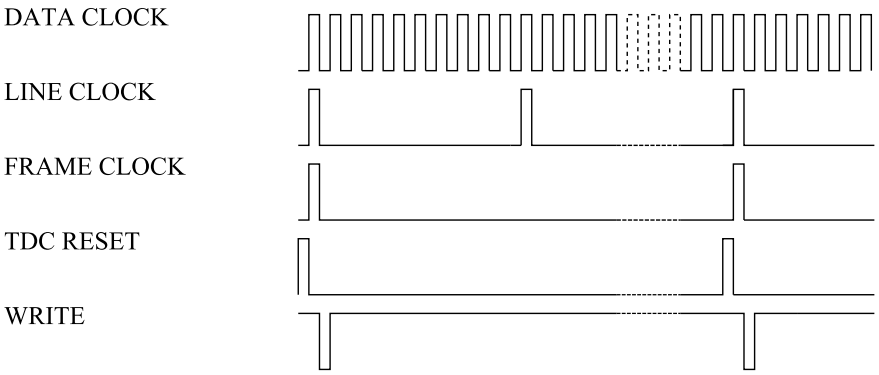

Figure 3.2: Data acquisition system: Timing diagram

However by generating signals as specified in Figure 3.2 will ensure a reliable data transfer from the imager, but it is equally important to ensure that the data is collected in the data acquisition system reliably as well. Hence to ensure a reliable communication, the data generated by the serializer needs to be sampled in the data acquisition system, at the same frequency as the data clock. Since the propagation delay introduced by the PCB is not known beforehand, it is required to have flexibility to vary the phase relation between the data clock and data sampling clock during the testing phase.

Since the MF128 can operate in various modes of operation and also depending on the configuration, the readout data rate can vary in wide range. Hence to control, configure and read data from the MF128 imager in real time, it is required to have a flexible data acquisition system.

3.2 Analysis on the earlier version of the imager

Before designing a data acquisition system for the MF128 imager, a study was carried out on the earlier version of the MF128 imager also called as the MF32. From the study it was found that the MF32 is a 32x32 on-pixel time resolved imager, following a similar architecture as MF128. The study revealed that the MF32 imager also has an I2C module, similar but a scaled down version of the MF128 readout system and a same set of control signals. However the difference between the two imagers is that the MF128 has 160x128 pixels, whereas the MF32 has 32x32 pixels. Further, the functionality of the I2C configuration register of MF32 is different from MF128. For example, in MF32 pixels in the region-of-interest (ROI) were enabled using the register available in I2C, on the other hand the MF128 uses a separate module also called ROWEN/COLEN to activate the pixels in ROI. Furthermore, the MF128 has on-chip compression techniques such as IEM and event-driven serializer, in contrast to MF32.

Since the I2C communication, control signals and the data readout signals are identical in MF128 and MF32, and also because the MF32 data acquisition system is designed to provide the required flexibilities to control, configure and read data from the imager,

it was decided that upgrading the MF32s data acquisition system to the MF128 would be the right choice. Rather than developing the whole new system for the MF128.

3.3 Hardware setup

The hardware platform used to develop the data acquisition system is shown in Figure 3.3. It is based on a Broaddown4 board [19] from Enterpoint featuring a dual Virtex-4 FPGA and fast communication modules.

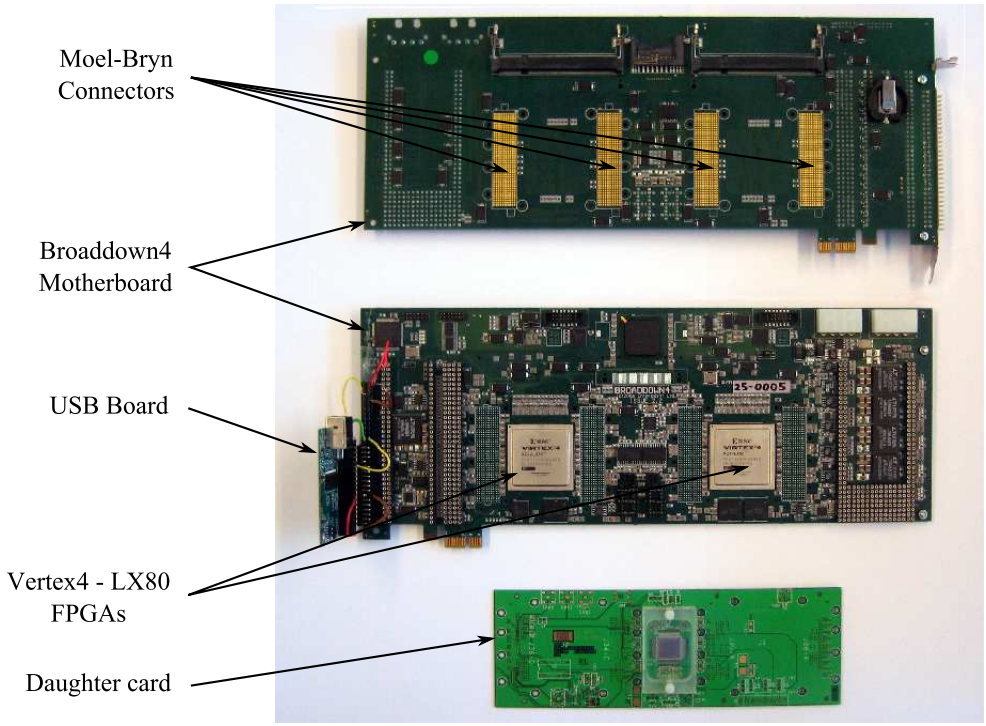

Figure 3.3: Hardware setup

The MF128 sensor is mounted on a daughter card in chip-on-board style, while a USB link is implemented as an add-on module, is also visible in Figure 3.3. The dual Virtex-4 FPGA acts as a mother board controlling the daughter card with MF128 sensor.

Four Moel-Bryn connectors have been used to connect the motherboard with the daughterboard. Considering the number of available pins in the motherboard, daughterboard is designed such that control signals and one half of the columns are connected to one FPGA and the other half is connected to the other FPGA.

3.4 Data acquisition system top-level design

The data acquisition system developed for the MF128 is divided in two parts viz. the firmware and the software. The firmware is used to control the MF128 and the software is used to control the firmware based on the user commands. Hence, the firmware is

realized in the field programmable gate array (FPGA) and the software is realized using the Visual C++ programming language. The communication between computer and FPGA is established using a USB interface. The top-level architecture of the developed data acquisition system for the MF128 imager using the MF32 design as it backbone, is briefed in this section.

Data acquisition system overview

To satisfy the requirements stated in Section 3.1, the data flow between the software, firmware and the MF128 chip is established as shown in Figure 3.4. The software receives the commands from the user, on how to control the chip. These commands are then carried over to FPGA through the USB interface. The firmware loaded in the FPGA decodes these commands to generate the control/configuration signals. Further the data collected from the MF128 in the FPGA, is transferred to the computer on-request through the USB interface.

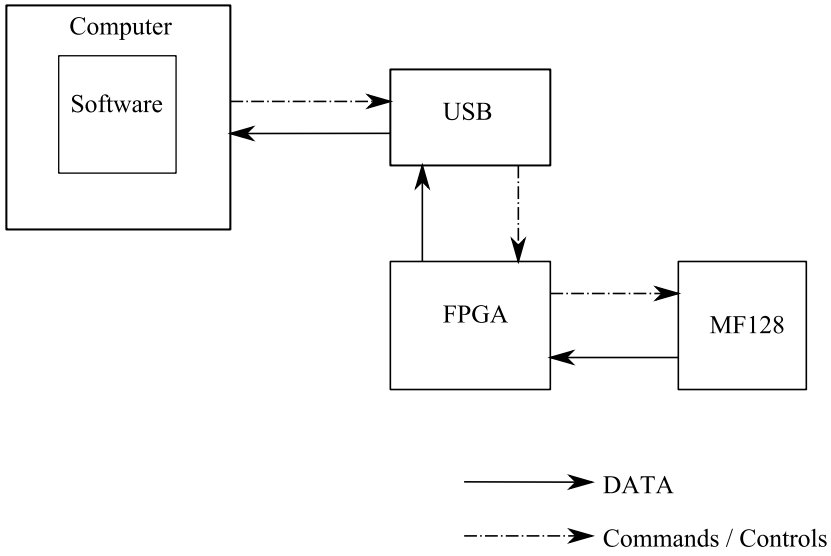

Figure 3.4: Data acquisition system overview

3.4.1 Firmware Architecture

The MF128 chip communicates with different interfaces and standards. Various modules with different functionalities were designed on FPGA to communicate and monitor the MF128 chip. These modules are connected using the Wishbone Bus interface [20] as shown in Figure 3.5. As all of these module need to be controlled by the user through software. The USB interface that comes under the direct control of the user acts as a master.

To facilitate the flexibility in controlling the MF128s functionality from the software, the design of every slave module connected to the wishbone bus is partitioned into two parts viz. the wishbone bus interface and the functional unit. The wishbone bus interface contains a set of programmable registers that can be configured from

the software. These registers are in-turn designed to generate control signals to the functional unit. Hence, by controlling the functionality of the functional unit it is possible to control the MF128 imager as required by the user through the software.

The main modules are the following:

- *Deserializer:* It is the module used to treat the data flowing from the MF128 chip and to reorganize them in a fashion that is compatible to display and further processing.
- *T-Piece:* It is the module that collects data from the serializer and packetizes it to transfer the data to the computer. This module also implements data compression techniques to reduce the data transfer rate from the FPGA to computer.
- *I2C bridge:* It is the module that programs the on-chip I2C so as to configure the chip.
- *Control generator module:* It is the module that generates the control signals used to control other modules and also to monitor for errors in other modules.
- *USB communication module* It is the module that enables the communication between the FPGA and the PC workstation.

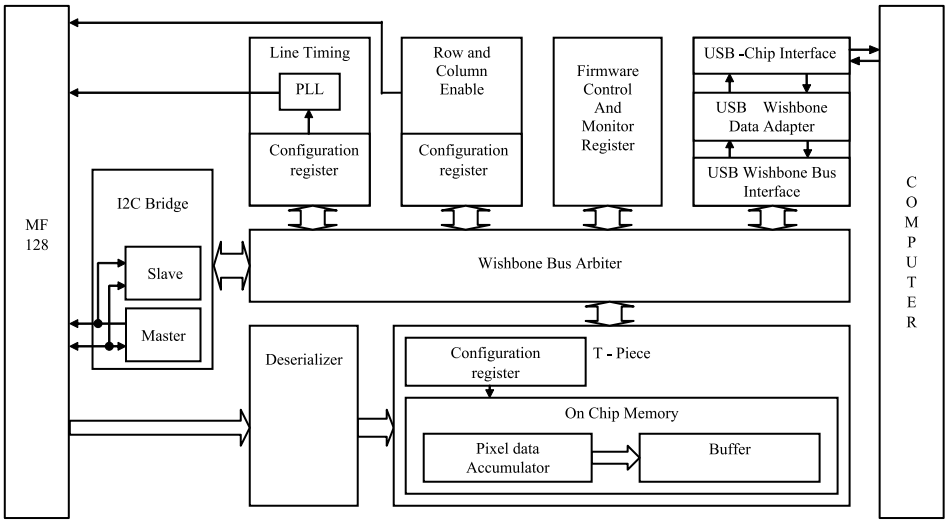

Figure 3.5: Firmware Architecture

The Block diagram representing of the firmware design for the data acquisition system is shown in Figure 3.5. The detailed explanation for each of these modules is presented in Section 3.5.

3.4.2 Established communication protocol between the firmware and software

The main functionality of the software is to receive commands from the user and send it across to the firmware loaded in the FPGA. In addition it is also designed to collect

the data from the MF128 through the FPGA. Hence, the communication between the firmware and software can be divided into two parts, namely the upstream communication and the downstream communication. Since the data acquisition system is designed such that the software acts as a master to the firmware, the upstream communication is always preceded by the downstream communication. Hence, to initiate a data transfer from FPGA to computer, a command needs to be sent from the software to the firmware.

Downstream communication

The software initiates the data transfer either upstream or downstream, by sending three words of width 32 bit length each. These three words represent the command, address and data. The command represents whether the software wants to read, write, abort or acknowledge. Address represents the address of the slave and the register, where the data needs to written in the slave. Hence by transferring three words it is possible to write data into the FPGA, provided the instruction in the command word corresponds to a write operation.

Upstream communication

As stated earlier the upstream communication is initiated by a downstream communication of sending three words as described earlier. On receiving a read command from the software, the firmware sends a header packet, along with the packet size it wishes to send. The software responds to the header packet with an acknowledgement. Then the firmware starts streaming the data.

3.5 Firmware design

A brief overview of the firmware design was presented in Section 3.4. This section will explain in detail the functionalities of the various modules.

3.5.1 USB communication

USB communication plays a vital role in creating a high-speed communication from the software to the FPGA and vice-versa. Since the motherboard is not provided with an on-board USB communication module. An ad-hoc USB communication board is required, which can convert the data coming from FPGA to the USB standards. From the market study, it was found that USB interface board offered by ELRASOFT [21] matched all the requirements and also more importantly it uses the same USB communication chip from Cypress [22] as used in MF32 mother board. This particular feature of the board will allow us to use most of the USB interface modules designed for the MF32. One major change required when compared to MF32 is that, in MF32 the USB communication is used by the PC to program the FPGA, as well as to control the loaded firmware. Whereas in the MF128 motherboard board, there is a separate JTAG connector specially meant for the FPGA configuration. Hence, the USB communication is required only to control the loaded firmware. To satisfy the above stated requirements a new configuration file for USB chip was designed.

USB interface module

The USB interface module in the firmware is designed to provide the physical interface between FPGA and USB chip. To match the timing requirements put forth by the USB chip. It was decided to use the 48 MHz clock generated by USB chip rather than using the clock generated by FPGA itself, this module is also responsible for generating the required control signals and presenting the data to the USB chip.

The USB communication chip from Cypress used in the data acquisition system require the data to be transferred in packets of 16 bits. Since the implemented wishbone bus architecture is 32 bit wide. The USB interface takes up the responsibility of combining the two 16 bit word into one 32 bit word during the downstream communication i.e. from PC to FPGA, and also it is responsible to de-packetize the 32 bit data coming from the wishbone bus into two 16 bit word during the upstream communication i.e. from the FPGA to PC.

USB Wishbone adapter module

The USB Wishbone adapter module monitors for the incoming data. As stated earlier the software initiates the data transfer with a packet containing three words representing command, address and data. The USB wishbone bus adapter decodes this packet and uses the command information to either block the upstream or downstream USB communication depending upon the command. Further this module is responsible to transfer the data reliably from the USB clock domain (48 MHz) to FPGA clock domain (32 MHz).

USB Wishbone BUS interface module

The USB Wishbone BUS interface module acts as a master on the BUS. Further, it is responsible for communicating the data to other module as per the Wishbone Bus standards. This module receives the configuration data stream from the software through the USB Wishbone adapter. The configuration data received from the software can be a data that needs to be written to a specific module connected to the bus or a request to read data from a module. Depending upon whether it is write or read, request the state machine designed inside the module will request the arbiter for an access to communicate with the required module.

Every slave module connected to the wishbone bus is designed such that it has a wishbone bus interface and a set of register that can be configured from the software using the wishbone bus.

3.5.2 Line timing

The Line timing module acts as a slave in the wishbone bus. This module is designed to generate signals such as line clock, data clock, frame clock, TDC reset, write, SPADEN, TEST start and the external stop signal.

This module uses the PLL available in FPGA to generate data clock. Then the generated data clock is used as a base clock to generate other signals. Further, this module not only generates clock and control signal to control the MF128, but also it

generates clocks for other modules in the firmware, such as DATA sample clock used in deserializer unit.

3.5.3 I2C

The I2C module acts as a slave in the Wishbone Bus. The main purpose of this module is to act as a master in I2C bus to communicate with I2C slave module that is on MF128 chip. As shown in Figure 3.5, the FPGA firmware is designed to contain both, I2C bus master and slave. This replication is made for two purposes, one to ease the testing process for I2C communication between firmware and software. Two, at runtime data that is sent to I2C slave in MF128 is also send to the on chip I2C slave module. This allows us to monitor the configuration file loaded into the chip, and also to use the configuration data for other modules in the firmware.

3.5.4 ROWEN/COLEN

The ROWEN/COLEN module is used to transfer ROW enable and COLUMN enable data serially to the MF128 chip. This module receives the data from the software through the wishbone bus and then uses serial shift register to transfer the data to the MF128 imager. The design is made such that the ROWEN and COLEN registers can be programmed in parallel.

3.5.5 Data pipeline path

The Data pipeline path is used to read the data generated by the MF128. It consists of two units, de-serializer and a T-Piece.

De-serializer

The De-serializer is designed to convert the serial data generated by the MF128 into a data word of 10 bits. This module also tags the 10 bit data with the ROW number, frame count and the operational mode of the MF128 chip. These tags are used by the downstream blocks to collect and align the data for a particular pixel. Each serializer in the MF128 is assigned with a separate deserializer in the FPGA.

T-piece

The main purpose of the T-piece is to collect the data from the deserializer and send it across to the computer. Hence this module contains a buffer that is be used to collect the data from the deserializer. Design is made such that the every pixel in the MF128 has its own 16-bit buffer. In FPGA these buffers were mapped to the block RAM available inside the FPGA. However it should be noted that the design presented in this section, is a very basic design that be adapted to all mode of operation. The problem with this approach is that the data generated by the MF128 is about 1.28 GB/sec, but the achieved USB communication speed with the current hardware setup is about 20 MB/sec. Hence due to the communication bottleneck most of the data generated by the MF128 is lost. However to reduce the impact of the communication bottleneck, three different techniques implemented in this thesis is presented in Section 3.7.

3.6 Software

Various abstraction levels

The main objective of the software is to communicate the users instructions to the firmware. Hence, it is designed to establish a two way communication between the software and the firmware. To realize these functionalities, the software is designed in three levels of abstraction namely:

1. Physical layer
2. Data processing layer
3. User interface

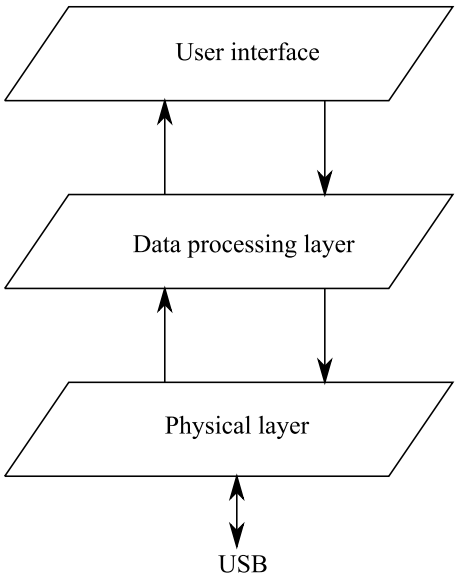

Figure 3.6: Software: Abstraction layer

- *Physical layer:* The physical layer uses the LibUSB library and creates a physical communication between the software and the USB interface chip. Hence this layer hides the USB communication interface from the other layers.
- *Data processing layer:* The data processing layer is designed to generate packets based on the instructions received from the user interface. In this layer the packets are generated to satisfy the requirements presented in Section 3.4. Further, the generated packet is transmitted to the firmware through the physical layer. Additionally, this layer is responsible to decode the data packet received from the firmware to be displayed in the user interface.
- *User Interface:* A graphical user interface (GUI) was created to receive commands and display the information received from the data processing layer. The command received from the GUI is communicated to the data processing layer to generate data packets for the firmware.

3.7 Application specific data-throughput optimization techniques

In Section 3.5 a generalized design for the T-Piece module is presented. The drawback with this design is that it is requires every collected frame to be transferred to the computer. As stated in Section 3.5, the difference in data generation rate (1.28 GB/sec at 50 kcps) and data transfer rate (20 MB/sec) prohibits the transfer of every generated frame of data to the computer. Hence, in this technique around 64 frames of data is lost for every frame of data collected. This corresponds to around 98.43% of the generated data is lost due to the communication bottleneck. Hence a better technique is required to reduce the data loss. This section explains three techniques implemented in this thesis to reduce the impact of the data communication protocol. However it is critical to understand that these three techniques are application specific.

3.7.1 Data accumulators for TUPC mode

In time un-correlated single photon counting mode, during the characterization phase for example to measure the dark count rate [23] (DCR), it is important to accumulate numerous frames of data to obtain a statistically reasonable result. Also in photon starved applications for example in fluorescence life time imaging microscopy (FLIM) to obtain an intensity image, it is required to accumulate frames of data.

To accommodate such applications, in the developed data acquisition system two levels of accumulators are incorporated for every pixel. In the first level an accumulator is realized in the firmware and in the second level another accumulator is realized in the software. The first level accumulator realized in the firmware is designed using a 16 bit memory mapped to a block RAM available in the FPGA. This 16 bit memory is used to store the accumulated value. Since the MF128 generates 7-bits of valid data in TUPC mode, using 16 bit memory will allow us to accumulate 512 frames of data. To obtain a statistically reasonable result, for most of the applications it is required to accumulate thousands of data frame. To accommodate this requirement a second level of accumulator is incorporated in the software. Hence by using this technique any number of frame data can be accumulated. However it is important to accept that the accumulator in the software can also overflow.

In this design a 16 bit accumulator used inside the FPGA has effectively reduced the data transfer rate by a factor of 320 times. Hence the required data transfer rate using this method is about 4 MB/sec, which is far below the available USB communication bandwidth i.e. 20 MB/sec. Hence this method can be effectively used to accumulate data in the TUPC mode.

The implemented architecture for the accumulator based design is shown in Figure 3.7.

3.7.2 Column based event driven system

The MF128 imager is designed for photon starved applications. In photon starved applications the number of photon detected per second is about 40-60 k counts/sec. Hence, in the photon starved applications the number of photon detected in the pixel

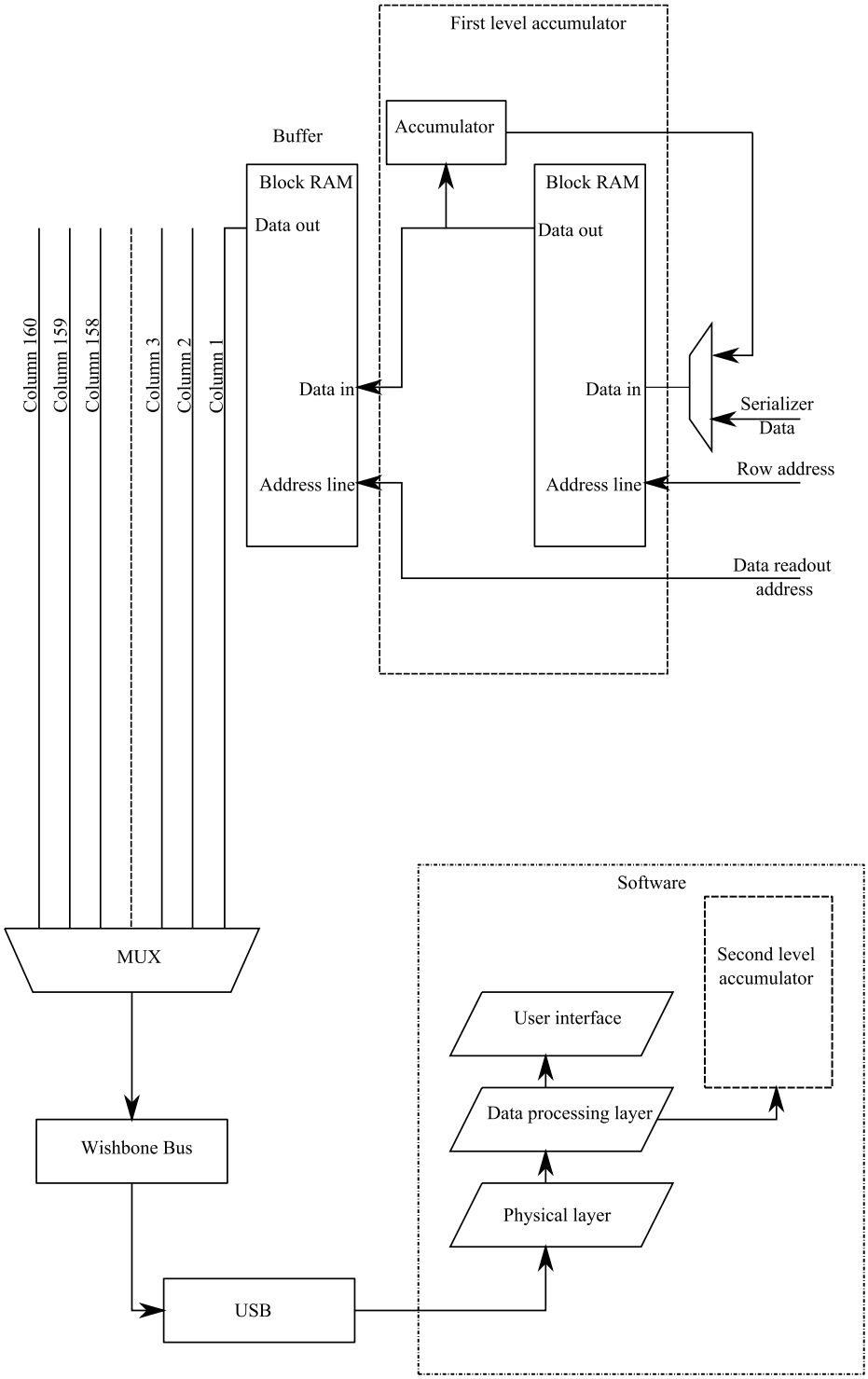

Figure 3.7: Accumulator based design

array for every frame running at 50 kcps is very less. In time correlated single photon counting mode the number of events observed across the array is very less. Hence in this thesis a technique called as event driven system is implemented. In this method only the pixels that have detected a SPAD trigger event are transferred to the computer. However, the drawback in this method is that the address of the pixels also needs to transferred to the computer. An address needs to contain the row and column information of the pixel. For MF128 the overhead corresponds to about 15 bit/pixel. To reduce this overhead the column based event driven system is implemented. In this technique the column information is preserved while transferring the data to the computer. Thus the overhead can be reduced by 8 bits/pixel. The drawback with this method is that an unequal numbers of pixels can be activated across the column, then there is possibility that a data with no information in transferred from few columns. Hence this technique is better adapted to the application where the light is uniformly distributed across the array. For example, in characterizing the imager to obtain instrument response function (IRF). The implemented column based event driven system is shown in Figure 3.8.

3.7.3 Time interleaved sampling on high DCR pixels for code-density test

In code-density test the TDC is characterized for non-linearity error, while the imager is configured in the TCSPC mode. In this test the TDC output is monitored for a long time until the statistically sufficient data is collected. Since the experiment is carried out in dark, the observed TDC output is very rare. The rate of occurrence of the TDC output is proportional to the dark count rate of the pixel. The experimental results of the DCR distribution across the array is shown in Figure 3.9, with varying number of active pixel columns.

From the DCR distribution plot it can be found that the distribution of DCR across the pixels remains the same irrespective of number of active column of pixels. Hence extrapolating this observation it can be said that the DCR distribution across every column will also be identical. Since the event rate is very less and also the count rate distribution across every column is almost identical, it is possible to conclude that the column based event driven technique is ideal to this experiment.

Further on observing the DCR distribution across the array, it can be ascertained that around 30 % of the pixels have DCR greater than 200 Hz. Hence, by performing the code density test using the column based event driven system might result in a situation where an unequal number of counts is observed for various pixels in the column. Therefore, to ensure that every pixel has received at-least a minimum number of photon counts, the frame collection time for this experiment should depend on the low DCR pixel. However, it should be noted that the high DCR pixels might have reached sufficient count much earlier that the low DCR excess. Hence the communication bandwidth is used to obtain no extra information. Moreover, it should be noted that the data readout bottleneck introduced by the USB communication is going to be very high. Hence it is important to reduce the generated data rate such that video streaming is possible.

As stated earlier by default it is required to collect data till a statistically sufficient data is collected for the low DCR pixel. However the high DCR pixel might have

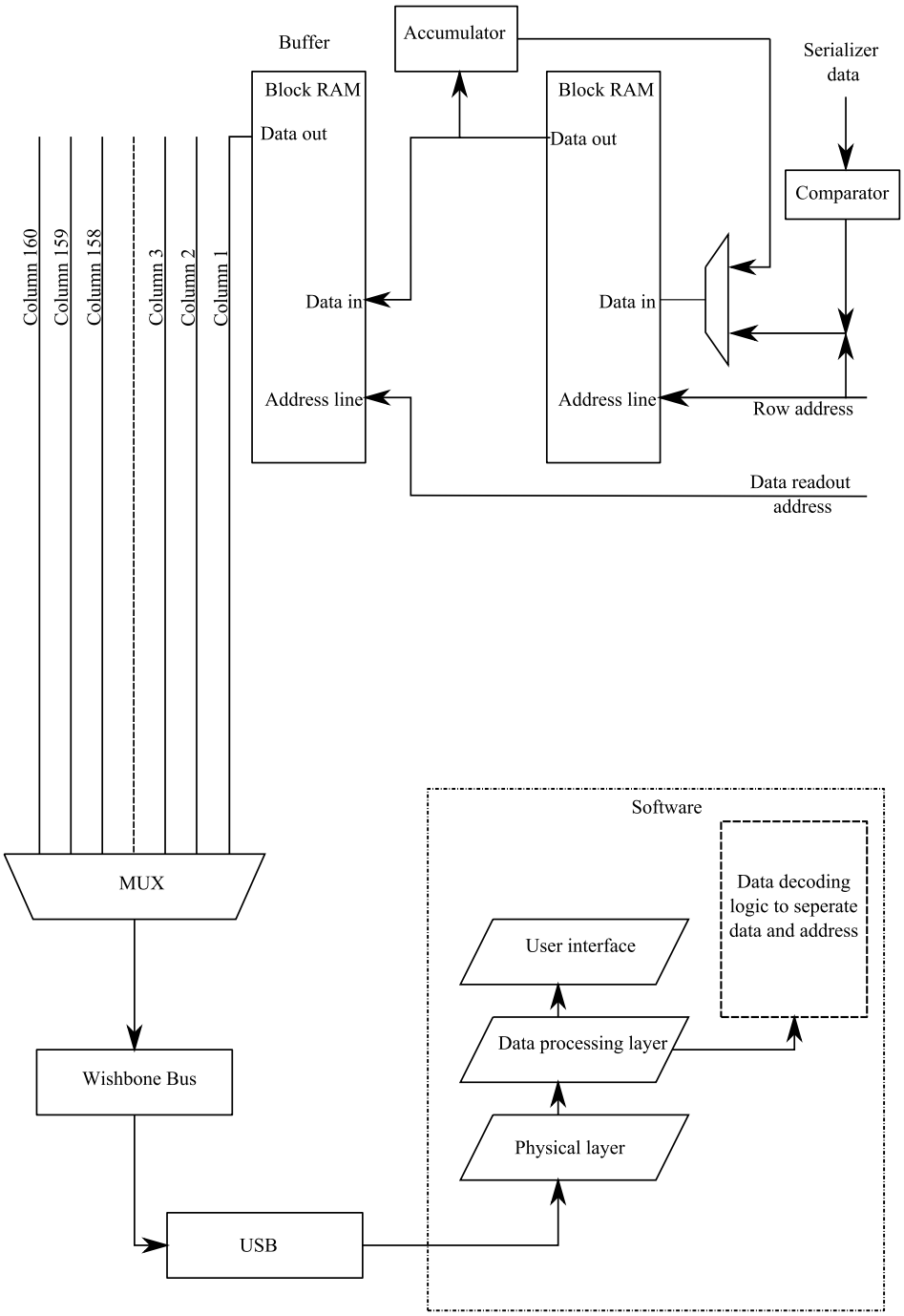

Figure 3.8: Column based event driven system

received a sufficient data much earlier than the low DCR pixel. Hence these high pixels tend to occupy the data communication bandwidth for nothing. To solve this issue, the time interleaved sampling technique on high DCR pixel is implemented. In this method the data generated by the high DCR pixel is sampled at a very low rate, such that the count rate observed by the high DCR pixel and low DCR pixel is the same.

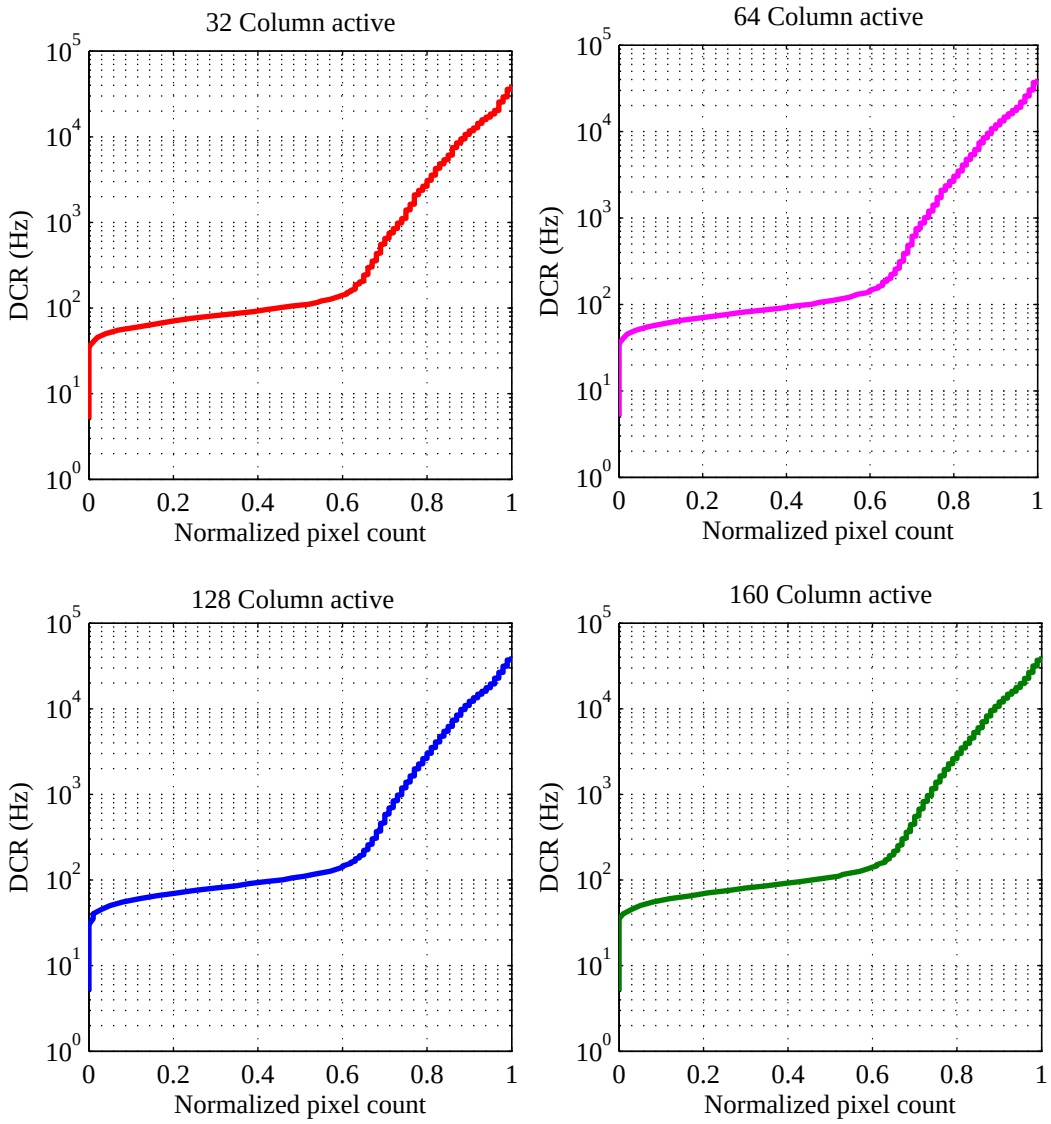

Figure 3.9: DCR distribution: With various number of pixel columns enabled at room temperature and 0.96 V excess bias voltage

One plausible solution could be to use the property of the TDC in MF128. The TDC present in every pixel is designed to measure to the first event of a frame, after the first event all other events are not considered. Hence by sufficiently increasing the time period of the frame clock, we tend to achieve equal count across the array. However the problem with increasing the time period of the frame iathat it will result in increasing the number of pixel data that need to be transmitted. This might hinder the video streaming and hence a dead time will be introduced between every frame of data sent across to the computer. Hence to alleviate this situation, two level of sampling on high DCR pixel is carried out. First is by using the TDC property and the other is by using the technique described here. In this technique first the high DCR pixel's location is

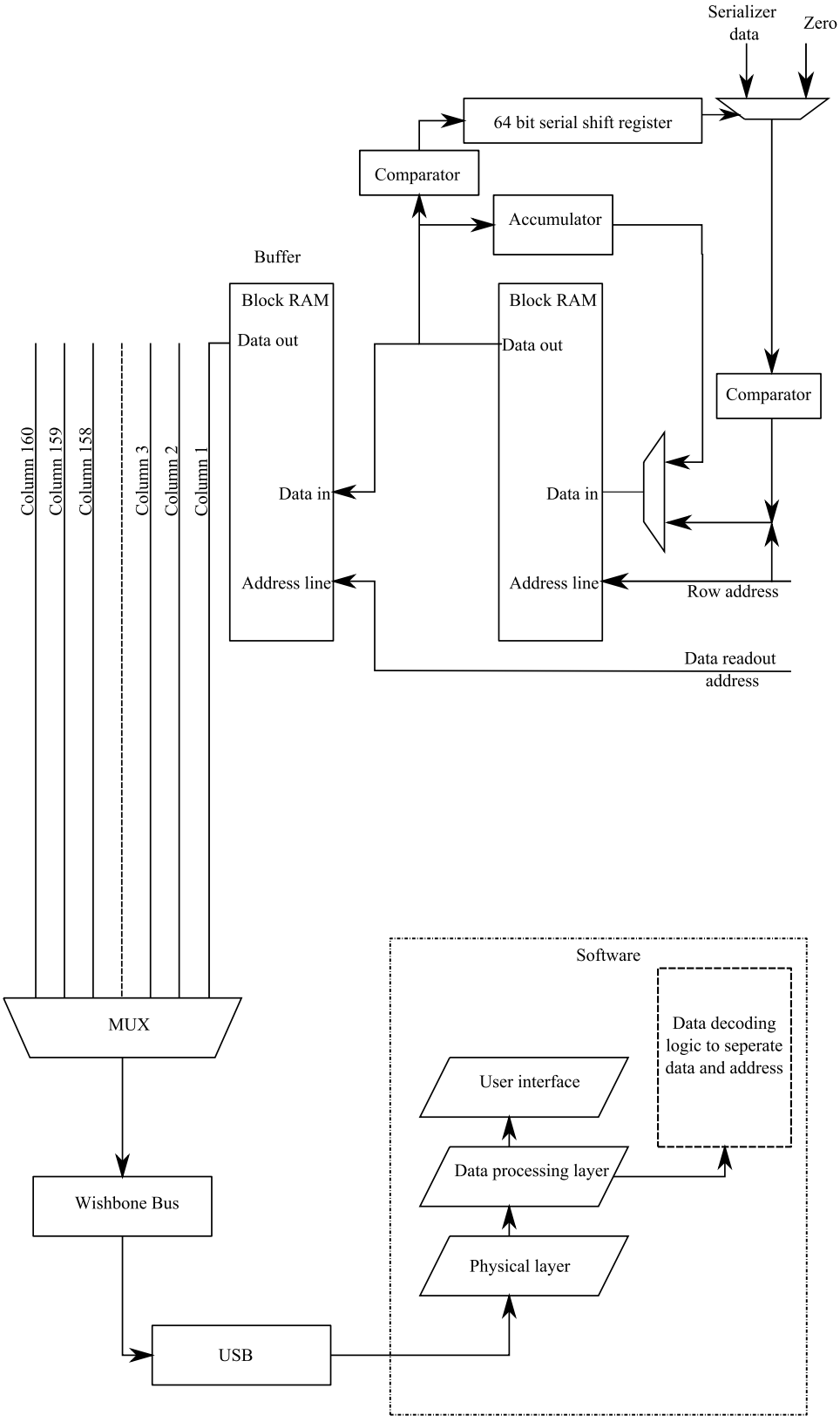

Figure 3.10: Time interleaved sampling system

stored in the memory and then the data received for these pixels and allowed to be transferred to the computer in a round-robin method. Hence using the time-interleaved sampling on the data generated by the high DCR pixels, we tend to achieve equal count rate across the array.

Hence by using the column based event driven system, the time-interleaved sampling technique on high DCR pixels and using the TDC's property of measuring only once per frame period, it is plausible to achieve significant speed-up in the code density test. The block diagram representation of the the implemented design is shown in Figure 3.10.

3.8 Summary

- The developed data acquisition system consists of firmware and software.
- Firmware is realized in FPGA and software is realized using Visual C++.
- Software receives commands from the computer and sends it across to the FPGA. Also it is capable to receive data from the FPGA.
- Firmware receives the commands from the software and controls the MF128 accordingly.
- Firmware is based on wishbone bus architecture.
- Communication between firmware and software is achieved using the USB interface.
- Impact of data throughput bottleneck introduced by the USB is reduced by implementing techniques such as data accumulators, Column based event driven system and time interleaved sampling on high DCR pixels for code-density test.

Time-Uncorrelated Photon Counting

4

In the second part of the thesis the MF128 imager is tested and characterized, using the data acquisition system developed in Chapter 3. Based on the two functional operating modes of the chip, the testing and characterization of the imager is split in two stages. In the first stage, the chip is tested in Time-Uncorrelated Photon Counting (TUPC) mode. Then in the second stage, the chip is tested in Time-Correlated Single Photon Counting (TCSPC) mode. The two testing stages are elaborated in Chapter 4 and in Chapter 5 respectively.

The test methodology followed in Chapter 4 and Chapter 5 is the bottom up approach. In the bottom-up approach first the basic functional modules are tested. Then the basic modules are grouped together at various levels and tested accordingly. The procedure of testing the chip by grouping the components is followed until the desired operating mode of the chip is tested. Of the two operating modes of the imager this chapter concentrates on TUPC mode.

The overview of the chapter is as follows: This chapter starts with a brief introduction to the TUPC mode in Section 4.1. In Section 4.2 a test strategy developed to test the TUPC mode is explained. Then in Section 4.3, the test methodologies used to test the basic modules are elaborated along with their experimental results. Section 4.4, presents the methodology used to test the TUPC mode. Then in Section 4.5 and Section 4.6, the characterization results of the MF128 imager in TUPC mode is presented. Further extending into the application domain, a 2-D picture taken using the MF128 imager is presented in Section 4.7. Finally the chapter is summarized in Section 4.8.

4.1 TUPC overview

In the Time Uncorrelated Photon Counting (TUPC) mode the MF128 imager is designed to measure the incident light intensity. In MF128 the light intensity is measured in terms of the photon count. However it should be noted that the photon count measured in MF128 is not equal to the incident photon flux. The percentage of the incident photons detected is proportional to the fill factor and the photon detection probability (PDP) of the detector. The fill factor in MF128 is about 1%. And the maximum expected photon detection probability based on the previous version of the imager [8] is about 27.5%. Hence, a certain percentage of incident photons is lost due to the inherent property of the imager. Furthermore, the measured photon count includes the counts introduced by the dark noise of the detector.

4.2 Test strategy

In TUPC mode the MF128 measures the incident light intensity in-terms of the photon count. Hence, to detect and measure the incident light intensity it is desired to activate the photon detector and the ripple counter. Additionally, the configuration system and the readout system are required to activate and read the measured data from a pixel. Hence, to functionalize the TUPC mode the photon detector, the ripple counter, the configuration system and the readout system need to be functioning.

To ease the testing and debugging process, it is important to first test the basic modules independently. Hence to test and functionalize the basic components in isolation, either one of the two approaches as described here can be used. The first approach applies to the modules, where it is possible to isolate its input and output from the other module. For such a module, the input test vector and the output can be controlled/monitored directly from outside the chip. The second approach applies to the modules where its input and output cannot be separated from the other modules. For such a module the input test vector and the output can be controlled/observed indirectly using the other modules. However, it is to be taken care that the modules involved in the input and output of the test vector need to be tested beforehand, so that the module under study can be tested reliably. Hence before proceeding with the basic module testing, it is vital to formulate a test strategy based on the inter-module dependency.

4.2.1 Inter-module dependency

The inter-module dependency can be extracted from Chapter 2 on MF128 architecture. From the MF128 architecture, it is understandable that the I2C module is required to configure and activate other modules. Hence it is vital to first test the I2C module. The module that depends only on the I2C module functionality is the readout system viz. the serializer and the Y-decoder. As the input data to the serializer can be generated using the header row by enabling the entire array of pixels using the I2C module. Once the readout system and the I2C configuration module are tested, the ripple counter can be tested using the TEST start signal. The unavailability of the data read back feature in the configuration registers of the ROWEN/COLEN module, necessitates a need to test its functionality indirectly by observing its output response. The output response of the ROWEN/COLEN module is the pixel activation. Hence by observing the pixel activation the ROWEN/COLEN module can be tested. After functionalizing the ROWEN/COLEN module finally the photon detector can be tested by monitoring its output directly on the oscilloscope.

Based on the component dependency analysis carried out in the previous paragraph, we can conclude that the basic components required for the TUPC mode can be tested systematically by following the test sequence summarized in Figure 4.1.

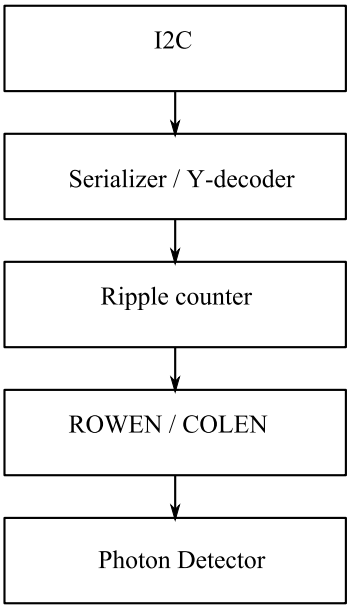

Figure 4.1: Test strategy

4.3 Module test

This section elaborates in detail the test methodology used to test the basic components, required for the TUPC mode. The sequence in which these components are tested and presented in this section follows the test plan derived in Section 4.2.

4.3.1 I2C

At a very high abstraction level the I2C module can be visualized as a memory module. The configuration registers inside the module provides the user with the read and write access. From the users perspective the I2C registers differs from conventional memory in terms of the communication protocol used to communicate the data to the memory. The configuration registers use I2C protocol for data communication. The I2C protocol requires two signal lines namely the SDA and the SCL for the data communication, where the SDA is the data line and the SCL is the clock line signifying the data communication. In addition to the SDA and SCL, the MF128 requires another clock line. This additional clock line is required to drive the I2C module itself. Hence in this thesis, the additional clock line is referred to as I2C module's core clock. Through experiments it was found that the I2C module's core clock is connected internally to the frame clock of the readout system.

Testing methodology

The test methodology followed to test the I2C module is very similar to the approach followed to test a memory. In this approach a known data is written into the memory and read back to compare it with the expected data. Since the data communicated to the chip is in a serial fashion. It makes sense to use data with alternating zeros and

ones. The data generated with this sequence can test the delay mismatch in the SDA and SCL lines. The delay mismatch can be introduced either due to PCB or inside the chip. However, this input test vector will not test the stuck-at faults in the registers. The stuck at faults in the registers, can be tested by introducing an additional test vector where the input data can be an inverted version of the previous test vector.

Results and discussion

From the initial failures in testing the I2C module and from the HDL code that was used to generate the I2C module in MF128, we found that in MF128 the I2C module's core clock is used to sample the incoming SDA and SCL lines. Since the I2C communication is designed to operate at 400 kHz, the sampling clock needs to be at-least twice the frequency of the incoming data to satisfy the nyquist criteria. It should be noted that in MF128 the I2Cs core clock is connected internally to the frame clock. Therefore, to write or read data from the I2C register, the frame clock needs to be at-least at 800 kHz. To modulate the frame clocks frequency to 800 kHz the number used for active row in the software can be reduced. To precisely calculate the number (N) that needs to be used for active row in the software to enable I2C communication depends on the data clock frequency. The number (N) can be calculated by using the formula given below.

$$\mathrm{N} = \frac{\text{Data clock frequency}}{\text{Data width per pixels} \times 800\ \text{kHz}} \tag{4.1}$$

Data width per pixel in MF128 is 10 bit

4.3.2 Serializer and Y-decoder

The readout system of the MF128 chip contains the serializer and Y-decoder. It should be noted that the serializer and Y-decoder are coupled in such a manner that their functionalities cannot be tested separately. Hence the complete readout system needs to be tested simultaneously.

Testing methodology

To test the readout system, the data generated by the header row can be exploited. The header pixel contains one seven bit counter. The counter output is then appended with two ones in the front and a zero in the last. The final ten bit data generated in the header pixel is then readout out using the readout system. It should be noted that the counter inside the header pixel is designed to count the frame clock. Therefore, the readout system can be validated by monitoring header pixels data for a two consecutive frames. However, to activate the header row the ROWEN/COLEN module is required. Since this module is not yet tested, one possible solution could be to use the I2C configuration register. Using the I2C configuration register it is possible to activate all row and/ or columns. Activating all rows and columns will end up in activating all the pixels. Since the entire array of pixel is active, the readout system will then read the entire array. To avoid any possible misinterpretations in the header pixels data, it

is important to force other pixels data to zero. The pixels other than in the header row can be made to read zero by connecting the input of the measurement unit to the ground. This can be achieved by using TEST start signal as input to the measurement unit and grounding it externally.

As stated earlier the readout system can be validated by comparing the header pixels data from two consecutive frames. But the problem with this approach is that it requires two consecutive frames to be monitored. Since it is not possible to collect two consecutive frames of data in the computer because of the data communication bottleneck, this approach cannot be automated.

Another approach could be to make use of the developed data acquisition system and the property of the header pixel. The seven bit counter present inside the header pixel is designed to overflow to zero after every 128 frames. Hence by configuring the accumulator present inside the data acquisition system to accumulate 128 frames of data, we can make the accumulator corresponding to the header pixel to read a constant value. Therefore by using this approach it is possible to avoid streaming every frame of data to the computer. Thus the communication bottleneck introduced by the data acquisition system can be circumvented.

Results and discussion

Based on the proposed test methodology for the readout system, the Y-decoder and serializer was tested successfully. While analyzing the experimental data, an interesting observation was made. The observation is that the data received in the FPGA from the MF128 is delayed in time, with respect to the frame clock that was originally generated by the FPGA for the data readout. Delay difference observed between the generated frame clock and the received data is about four data clock cycles. The reported delay of four clock cycles was observed when the data clock used was running at 16 MHz. To understand whether the delay was introduced because of the signal propagation or because of the pipelining, the experiments were repeated with the data clock frequency of 32 MHz. The results for the delay difference from the experiment were still at four data clock cycles. Of the four data clock cycle delay, it was found that one clock cycle delay was introduced because of a pipelining stage introduced while transmitting the frame clock from the FPGA. The remaining three clock cycle delay might be introduced because of the clocked on-chip readout system.

4.3.3 Ripple counter

The 7-bit ripple counter located inside the TDC is used to count photons in TUPC mode and in TCSPC mode it generates seven course bits for the time measurement. In either of the modes the ripple counter counts the incoming pulses. The only difference between the two modes is the pulse generation source.

Testing methodology

As stated in Chapter 2 on MF128 architecture, the measurement unit present inside every pixel can be tested using the TEST start signal. Hence, to test the ripple counter

the measurement unit needs to be configured in the TUPC mode. In this configuration the TEST start signal will be connected to the ripple counter. Further, by activating the readout system and the entire array of pixels using I2C module, the ripple counter can be tested by generating a known number of pulses per frame using the TEST start signal. Moreover, to test the full range of the ripple counter, the experiments can be extended by sweeping the number of pulses per frame from 0 to 127.

Results and discussion

The experiments were conducted by providing a known number of pulses to the counter using the TEST start signal. The counter output is then monitored and compared with the expected value. The complete range of the ripple counter was tested by sweeping the pulse count in the TEST start signal from 0 to 127. To get an idea on the working of the ripple counter for pulse counts greater than 127, the experiments were extended by sweeping the input pulse count till 255.

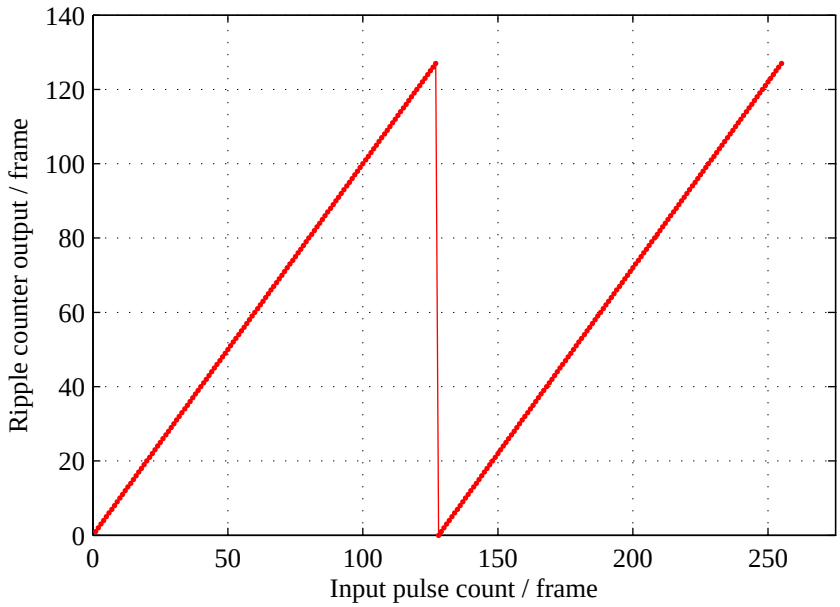

Figure 4.2: Ripple counter test results

The experimental results presented in Figure 4.2 imply that the ripple counter is indeed working as desired. From the observed periodicity in the counts, it is possible to conclude that the counter overflows to 0 after reaching 127.

4.3.4 ROWEN/COLEN

The ROWEN/COLEN module is used to activate a group of pixels in the pixel array. It contains two serial shift registers each of width 160 and 130 bits respectively. To configure the two registers two signal lines are provided, one is the data and other is the clock.

Testing methodology

As stated already in Section 4.2, because of the unavailability of the read feature in the ROWEN/COLEN registers, we need to test it indirectly by reading the pixel data. To ease the testing process and to make it systematic, the header row and the rows near it can be activated. The technique of using rows near the header row will help us to localize the activated rows with respect to the header row, during the analysis of the experimental data. From the extracted spatial location of the activated row and based on which column the data is collected from, it is possible to localize the spatial location of the activated pixel in the array. The spatial location of the activated pixel can then be compared with the expected location, to test the functionality of the ROWEN/COLEN module. Since the data communicated to the ROWEN/COLEN is in a serial fashion, it makes sense to test it with alternating zeros and ones. Using this test vector the propagation delay in the lines can be tested. To test for stuck-at faults, a second set of test vector can be used, which can be an inverted version of the earlier test vector.

Results and discussion

The ROWEN/COLEN module was tested after configuring the ripple counter to count a known value using the TEST start signal. The output data was accumulated for 128 consecutive frames. The 128 consecutive frames were accumulated to localize the header row. By comparing the location of the active pixels with the expected results, it was found that the ROWEN/COLEN module was functioning as desired.

4.3.5 Photon detector

The photon detector implemented in every pixel contains a SPAD along with its quenching circuitry. The output of the SPAD is connected to an inverter. The inverter output is then used by the measurement unit. To bias the SPAD to work in the Geiger mode, the SPAD needs to be reverse-biased above the breakdown voltage. The magnitude of the voltage applied in excess to the diode's breakdown voltage is called as the excess bias voltage. In MF128 the voltage applied across the SPAD can be controlled using the two voltage input lines viz. V_{bd} and V_{eb} respectively, as shown in Figure 2.4. The biasing circuitry around SPAD is designed such that the V_{eb} needs to be set at 1.2 V and V_{bd} can be of any value in the range 0 - 14.25 V. By controlling V_{bd} the bias voltage applied across the SPAD can be varied.

Testing methodology

In MF128 imager, the photon detector can be tested by monitoring the inverter's output directly in the oscilloscope. To monitor the inverter's output outside the imager, the measurement unit and the readout system needs to be bypassed. Furthermore, it should be taken care that only one row of pixels are active. The module configuration and the selective pixel activation can be achieved using the I2C module and the ROWEN/COLEN module respectively.

The photon detector can generate a voltage pulse either when it detects a photon or due to a dark noise. The dark noise is a random event generated by a photon detector, when the detector is placed in dark. For a given SPAD the dark noise depends on the temperature and the applied excess voltage [15], whereas the photon detection probability (PDP) of a SPAD depends on the applied excess bias voltage and the wavelength of the incident light [15].

Since the SPAD implemented in MF128 is very similar to [8], we can also expect a similar performance in MF128. For the SPAD reported in [8] the observed count rate is about 50 events per second with a 0.6V excess bias voltage. Further, the PDP reported in [8] reached a maximum at 490nm wavelength with a 1.4V excess bias voltage. Figure 4.3 reproduces the PDP results reported in [8].

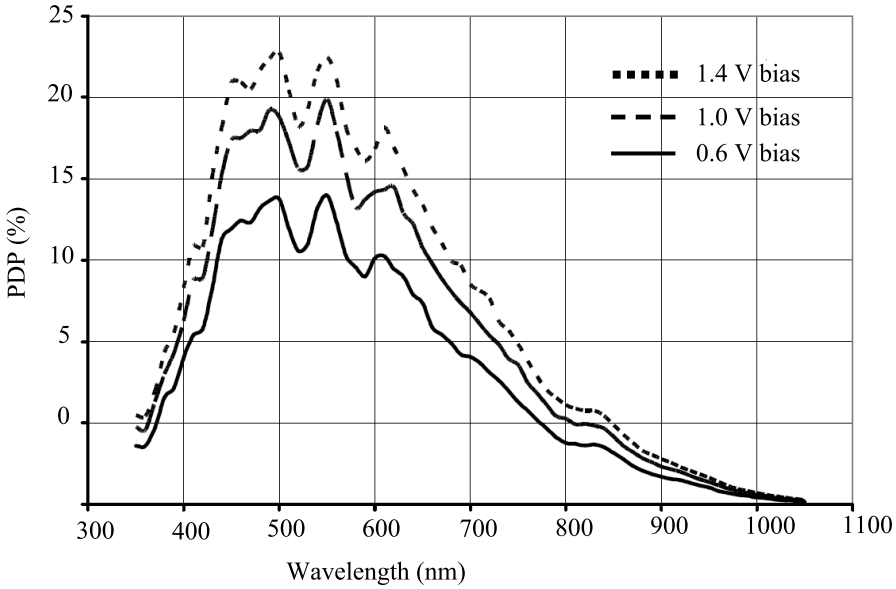

Figure 4.3: Photon detection probability (PDP) [8]

From Figure 4.3 and from [15] it can be inferred that the PDP of the SPAD will increase with the excess bias voltage. Hence varying the excess bias voltage the functionality of the SPAD can be tested, by monitoring for increase in output pulse count per second. However before testing the SPAD the breakdown voltage of the diode needs to be determined.

Since the breakdown voltage of the SPAD is not known beforehand, a test needs to be carried out. The breakdown voltage can be approximately evaluated by sweeping the voltage across the SPAD. The voltage at which the SPAD start to trigger events correspond approximately to the sum of the diodes breakdown voltage and the inverter's threshold voltage. The designed threshold voltage of the inverter is 0.6 V. In this experiment, the intensity of the light needs to be maintained such that it does not saturate the SPAD and also it should not be dark. The problem in SPAD getting saturated with light is that the inverter's output is always going to remain at logic one. On the other hand when the SPAD is placed in dark, we might end up increasing the error in estimating the breakdown voltage, as the SPAD trigger events are very rare in

the dark.

The photon detector in MF128 is designed to detect the light in the visible range. To quantitatively test the detector for various light conditions, three different light intensities can be used. Three light intensities can be in dark, with less light and with very high intensity of light. In dark an ideal detector should not trigger, but because of the noise a few events can be expected. In less light condition, the detector will trigger more than in the dark. In very high light conditions, the inverter output will always remain at logic one, because of the SPAD getting saturated with light. In all these experiments it is important to bias the SPAD above the breakdown voltage.

In MF128 the inverter output is sampled by the line clock internally inside the chip at the serializer. So, it is important to run the line clock at a very high frequency, such that every event triggered by the SPAD is captured. Since the expected dead time of SPAD is 100 ns [8], by generating the line clock at-least at 10 MHz, it is possible to capture all the trigger events of the SPAD.

Results and discussion

Test 1: Breakdown voltage calculation

The experiment was carried out to obtain the breakdown voltage. From the experiment it was found that the SPAD trigger events started to appear at the output of the inverter, when the voltage across the SPAD was about 14.06V. This corresponds to the breakdown voltage of approximately 13.46 V. It is to be noted that the breakdown voltage reported here is obtained from one SPAD. The assumption here is that the breakdown voltage is almost constant across the array, as all the SPADs are identical. However the variation in the breakdown voltage across the pixel array is studied in detail in Section 4.5.6.

Test 2: In varying light conditions

Experiments were carried out after biasing the SPAD by approximately 1.0 V above the breakdown voltage. The output of the inverter sampled by the line clock is observed in three different light viz. in dark, medium light intensity and high light intensity. Since the observed event rate is very less in dark, and higher in less light and saturated in very high light intensity, it is possible to conclude quantitatively that the SPADs are detecting light as expected.

Test 3: Varying excess bias voltage

The experiment of observing the SPAD output was repeated reduced less light, by varying the excess bias voltage. As expected the SPAD trigger rate increased with the excess bias voltage, until the SPADs get saturated. From all these experiments it can be inferred that the SPAD is working as desired.

4.4 TUPC test

Section 4.3 went over the various test methodologies used to test the basic modules required for the TUPC mode. This section will extend the testing process, by integrating the basic modules to test and functionalize the TUPC mode.

4.4.1 Test methodology

For the TUPC mode to be operational the output of the photon detector needs to be coupled to the ripple counter input. In this configuration the ripple counter will count the number of detected photons. The required configuration for the TUPC mode can be achieved using the I2C and ROWEN/COLEN module.

To validate the functionality of the TUPC mode, the test methodology used to test the photon detector can be used. That is by biasing the SPAD roughly 1 V above the breakdown voltage and using three different light conditions viz. no light (dark), medium light intensity and high light intensity. In no-light condition the output of the pixel should correspond to the dark counts of the pixel. In medium light condition the output of the pixel should correspond to the light intensity. In high light condition the output of the detector should read zero, because of the SPAD getting saturated.

4.4.2 Results and discussion

After configuring the MF128 chip as required for the TUPC mode, the three experiments were carried out. As expected the output photon count of the pixel was very less in the dark, and slightly higher in medium light intensity and zero at high light intensity. However, there was a mismatch in the expected value in few pixels especially in the dark, where the dark noise of the pixel was much higher than the normal pixels. The detailed study on the dark noise is carried out in Section 4.5.

4.5 Dark noise characterization

Section 4.3 and Section 4.4 explained in detail the various test methodologies used to test and functionalize the TUPC mode. In this section the TUPC mode of operation is used to characterize the MF128 imager for the dark noise. Further, using the TUPC mode the breakdown voltage of the SPAD is evaluated. Finally, the observed correlation between the breakdown voltage and dark noise is explained.

4.5.1 Dark noise overview

As stated earlier the dark noise is a random event generated by a photon detector in the dark. The generated dark noise can be due to two reasons viz. trap assisted thermal generation noise and band-to-band tunneling noise [23]. For a given SPAD the trap assisted thermal generation noise will increase with temperature. Whereas the band-to-band tunneling noise depends on the electric field applied across the depletion region. Hence the band-to-band tunneling noise will increases with the bias voltage applied across the SPAD. In literature dark noise of a photon detector is characterized

using the Dark Count Rate (DCR). The DCR is defined as the number of SPAD trigger events observed in one second, when the photon detector is placed in dark. The DCR of a photon detector determines the lower limit for the light intensity that can be detected reliably. Since the MF128 is aimed at the photon-starved applications, it becomes important to have pixels with low dark count rate.

4.5.2 Experimental Setup

In TUPC mode of operation, the pixels of the array are activated and allowed to count for the duration of a frame. The result of the counting procedure is stored in the on-pixel buffer that is eventually read out. Since the observed dark events are statistical in nature, it requires numerous frames of data to be accumulated to obtain a statistically relevant result. To realize the frame accumulation two levels of accumulators are implemented in the data acquisition system, as explained in Chapter 3. Hence by utilizing these accumulators available in the data acquisition system it is possible to accumulate any number of frames. Therefore by operating the imager in TUPC mode and using the accumulators available in the data acquisition system, it is possible to spot hot pixels, i.e. pixels whose SPAD is exhibiting high DCR. The overall dark count analysis yields the DCR distribution across the array and a histogram of the DCR.

4.5.3 Dark count rate uniformity

The DCR uniformity is evaluated by plotting the histogram of the DCR statistical distribution over all the pixels in the array. To study DCR uniformity an experiment was conducted in the dark at 25^{o}C with the excess bias voltage of 0.73V. The experimental result of the DCR uniformity is shown as a histogram in Figure 4.4. In Figure 4.4, the breakdown voltage of the SPAD is assumed to be about 13.25 V. This breakdown voltage is derived using the technique described in Section 4.5.6.

The plot of Figure 4.4 shows that at an excess bias voltage of 0.73 V, around 70% of the pixels have a DCR better than 150 Hz. The spatial distribution of the DCR across the pixel array is shown in Figure 4.5.

4.5.4 Effect of DCR on electrical noise (Supply or substrate induced)

To understand the effect of electrical noise on the DCR, an experiment was carried out. In this experiment the DCR of the pixel is observed by varying the number of columns activated. Deactivation of a column results not only in the suppression of the corresponding I/O pad but also the SPAD and the pixel circuitry on that column. The experimental result is produced in Figure 4.6. From the negligible variation in DCR with respect to number of columns active it can be inferred that the DCR is exclusively due to intrinsic SPAD DCR mechanisms (trap-assisted and tunneling) and decoupled from the electrical noise (supply or substrate induced).

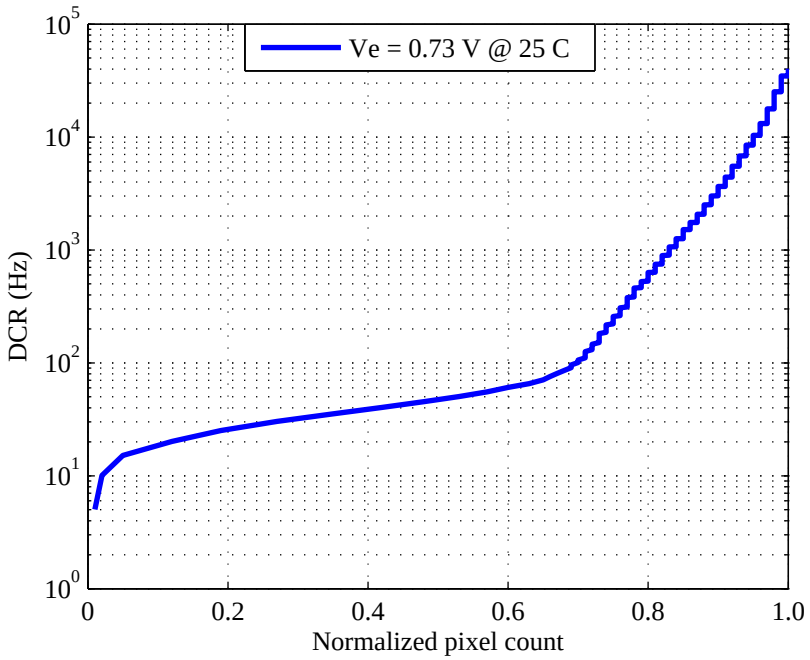

Figure 4.4: DCR histogram at 25^{o}C and 0.73V excess bias voltage

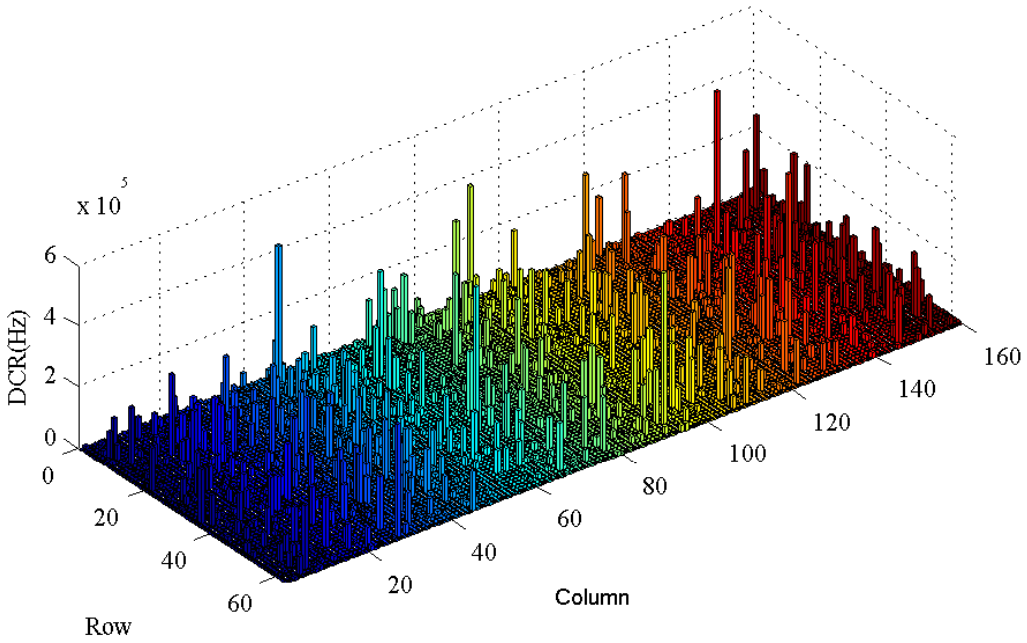

Figure 4.5: DCR spatial distribution at 25^{o}C and 0.73V excess bias voltage

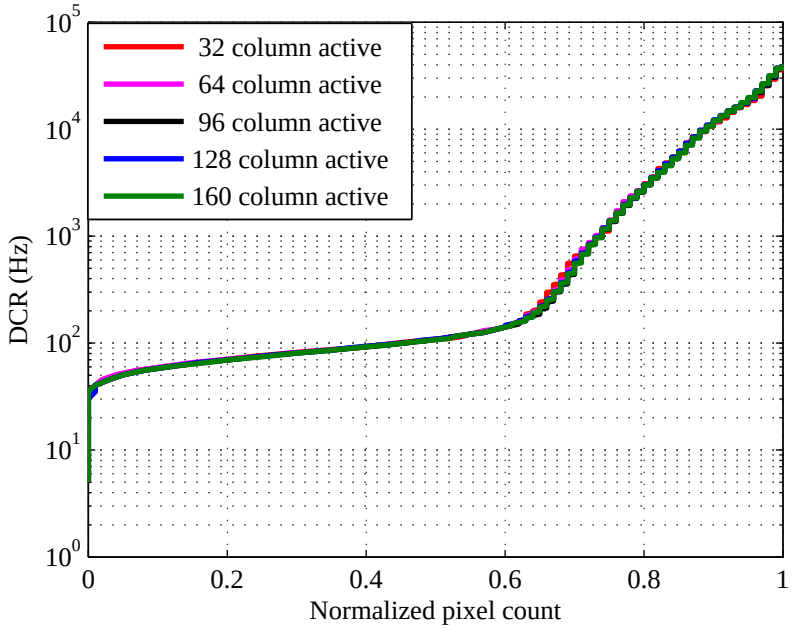

Figure 4.6: Impact on DCR of active columns at room temperature and 0.96V excess bias voltage

4.5.5 Effect of DCR on temperature and excess bias voltage

As stated earlier, the DCR of a photon detector is contributed by two sources of noise namely the trap assisted thermal generation noise and the band to band tunneling noise. These two sources of noise depend on the excess bias voltage and the temperature. Hence to study the dependence of the DCR on the temperature and excess bias voltage, a set of experiments were carried out. In these set of experiments 160x64 pixels were active.

The experimental results of the DCR distribution at various temperatures is shown in Figure 4.7. In these plots the voltage across the SPAD (V_{op}) is used to represent the excess bias voltage, to give a fair comparison between the observed DCR at various temperatures, as the SPAD breakdown voltage can vary with temperature.

From the summary of the experimental results shown in Figure 4.8, it can be infered that the median DCR of the pixel array reduces with the SPAD bias voltage and with the temperature as expected. From the plot, it can be observed that the median DCR of the pixel can reduce to around 20 Hz at 10 C and when the voltage across the SPAD is about 14.25 V. From these results it can be infered that the DCR of the SPAD observed in room temperature correpond mainly to the trap assisted thermal generation noise.

4.5.6 SPAD breakdown voltage extraction

For the SPAD array designed as in MF128, where there is no access to the individual SPADs to obtain the I-V characteristics, the breakdown voltage of the SPAD could be extracted using the observed count rate vs V_{op} plot. In this method the breakdown

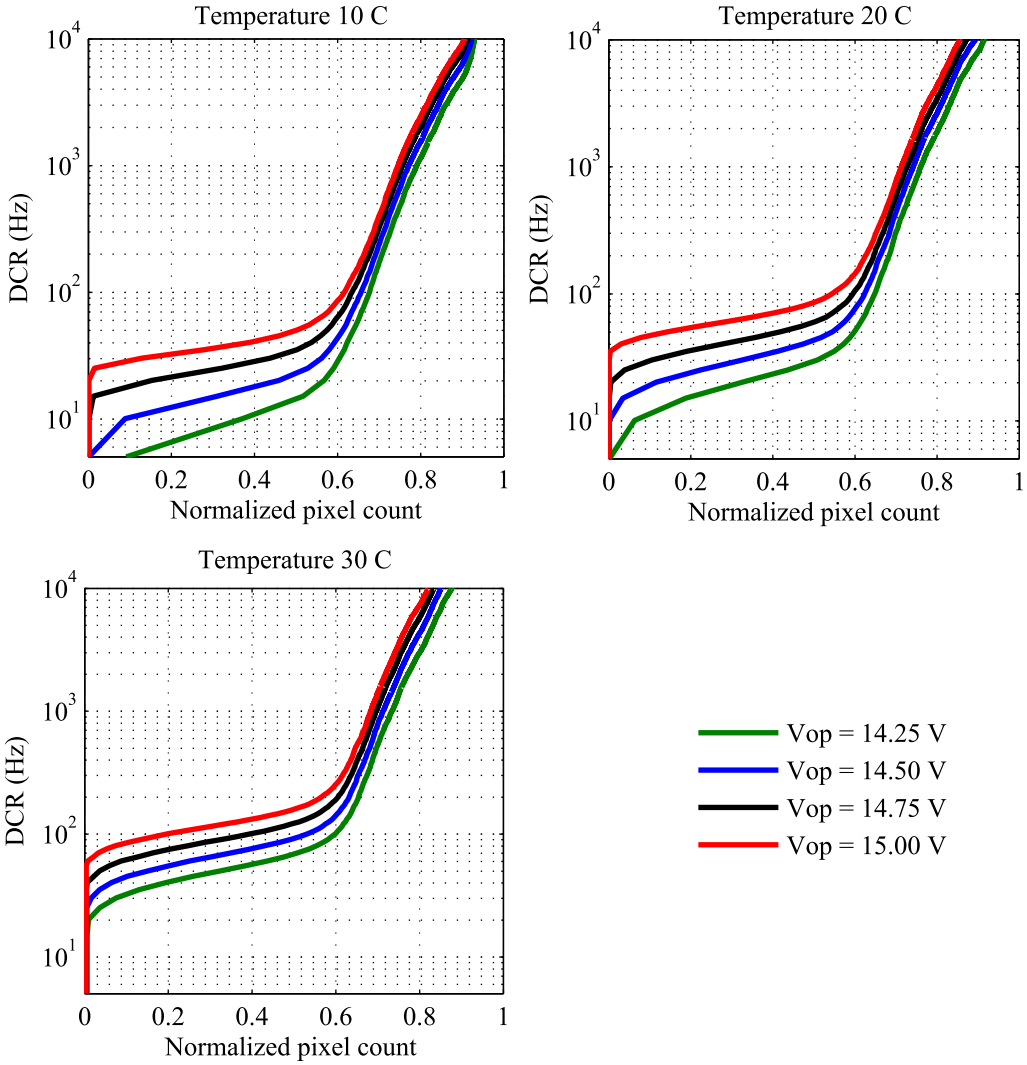

Figure 4.7: DCR distribution varying temperature and excess bias voltage

voltage can be identified, by extrapolating the linear line fitted to the data points in the count rate vs V_{op} plot, the V_{op} voltage at which the fitted line intersects is the breakdown voltage of the SPAD.

The count rate vs V_{op} plot can be obtained using either of the two different experiments listed below.

1. By observing the dark count variation with V_{op}.
2. By observing the photon count variation with V_{op}.

Of the two possible methods, it was found from experiments that the relation between the DCR and V_{op} is not linear. As the DCR depend on the trap assisted thermal

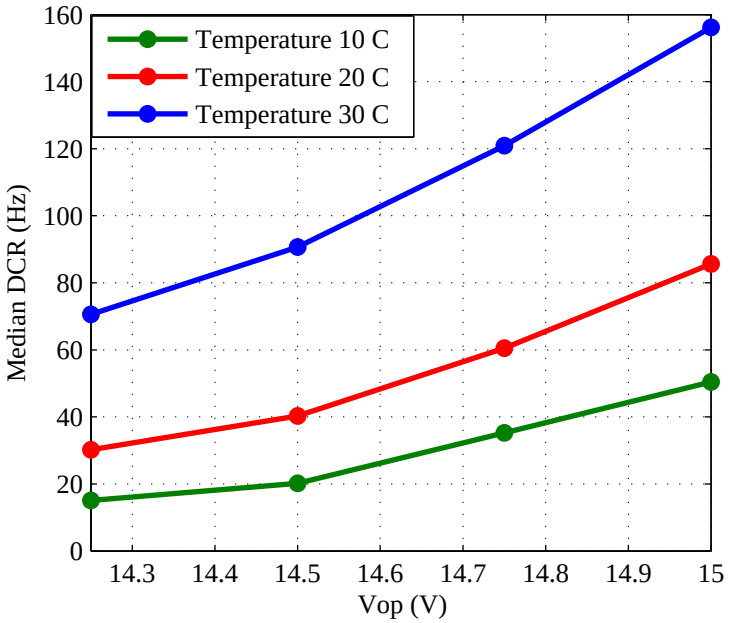

Figure 4.8: Median DCR vs V_{op} at various temperatures

generation noise and the band-to-band tunneling generated noise. At very low excess bias voltage the trap assisted thermal noise is a contributing factor and at high excess bias voltage tunneling induced noise starts to contribute towards DCR. Due to this complex relation between the DCR and the excess bias voltage, DCR vs V_{op} tend to be non-linear. This can be observed from the experimental results shown in Figure 4.8.

Whereas the relation between the photon count rate and V_{op} is linear, provided the excess bias voltage and the light intensity is not very high to saturate the SPAD. Hence by using very less light, it is possible to obtain approximately a linear relation between the count rate and V_{op}.Thus from the linear plot the breakdown voltage of the diode can be exteacted reliably.

Figure 4.9 shows the experimental results of the breakdown voltage distribution. These results were obtained with the light intensity correponding to 4000 counts/second at 13.95 V across the SPAD.

From Figure 4.9 it can be inferred that around 27% of pixels have a higher breakdown voltage that the remaining pixels. This interesting observation can be due to two reasons:

1. Due to the variation in the available bias voltage across the array.
2. Due to manufacturing process variation.

To understand whether the cause for a high breakdown voltage pixel is due to the variation in the available bias voltage across the array, the spatial distribution of the breakdown voltage is analyzed using Figure 4.10. From Figure 4.10, it is understandable that the spatial distribution of the high breakdown voltage pixel does not follow any specific pattern. Hence this possibility can be ruled out.

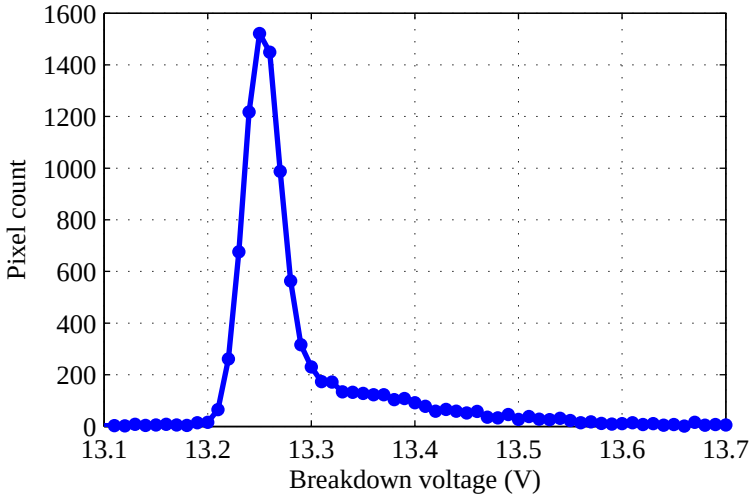

Figure 4.9: SPAD breakdown voltage distribution

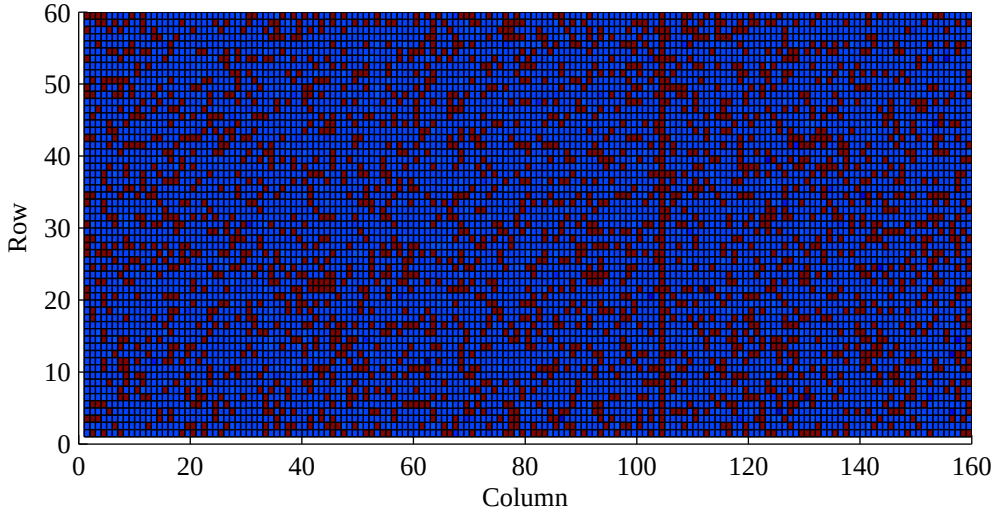

Figure 4.10: Spatial distribution of high threshold voltage (>13.3V) pixels

To understand whether the process variation is a cause for the high breakdown voltage, a study was carried out by comparing the DCR distribution with the breakdown voltage distribution. Interestingly, it was found the high DCR pixels got mapped one to one with the high breakdown voltage pixels. The correlation between high DCR pixel and high breakdown voltage pixel is shown in Figure 4.11. Hence it can be concluded that the cause for the high breakdown voltage and high DCR pixel is due to the manufacturing process variations.

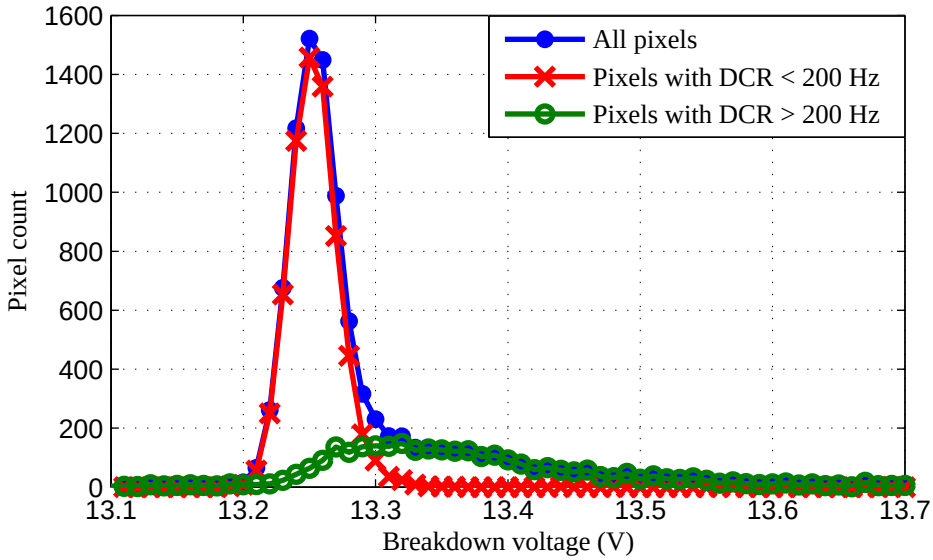

Figure 4.11: Correlation between high DCR pixel and high threshold voltage pixels

4.6 Impact of digital noise

To investigate the impact of the digital noise in TUPC mode, a set of experiments were carried out. These experiments were designed to understand the effect on the observed count rate, while increasing the activity of the circuitry. The variation in the circuitry activity is induced by varying the number of active columns and the light intensity. To compare the variations induced in the count rate at various intensities of light, a data analysis was carried by evaluating the percentage increase in count rate with respect to one column active.

The experimental result is shown in Figure 4.12. From Figure 4.12 it can be inferred that the percentage variation in the count rate is negligible with the increasing count of active columns. Hence we can conclude that the effect on digital noise on the TUPC mode of operation is negligible.

4.7 2-D picture

A qualitative analysis of MF128's TUPC operating mode was conducted by illuminating an object with a white diffused uniform light through a 50mm objective, F/2.8 (in the F/5.6 position), focused to infinity. With a sufficiently wide lens with respect to the size of the sensor and a high-quality objective, it can be assumed that the lens attenuation is uniform across the sensor and that the optical/chromatic aberrations introduced by the lens are negligible. Figure 4.13 shows an image of a mannequin illuminated by a 50W incandescent lamp. The resulting image is obtained summing all the frames produced by MF128 during the exposure time of 4ms.

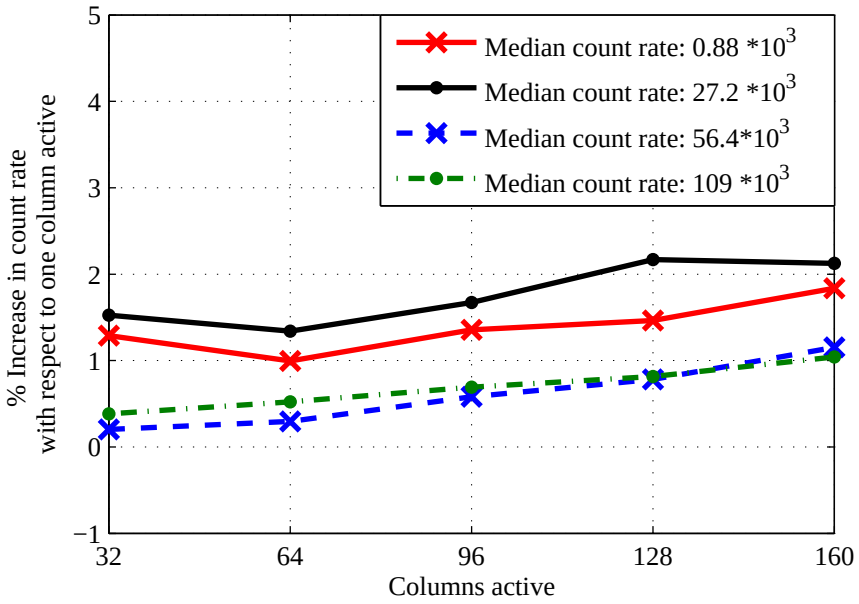

Figure 4.12: Impact of digital noise on TUPC mode

Figure 4.13: Mannequin image

4.8 Summary

- The TUPC mode in MF128 imager requires photon detector, ripple counter, configuration system and the readout system.
- All modules required for the TUPC mode are tested
- The median dark count rate of the imager is characterized as 50 Hz at 25^{o}C with a excess bias voltage of about 0.73 V.

- For a SPAD array as in MF128, the breakdown voltage of the photo diodes can be determined using the count rate vs V_{op} plot obtained in photon starved condition.
- Manufacturing process variation can be a reason for the high DCR pixels.
- Impact of digital noise on the imager in TUPC mode is found to be negligible.

Time-Correlated Single Photon Counting Mode

5

In time-correlated single photon counting (TCSPC) mode, MF128 is designed to measure the arrival time of a photon. To realize the time-of-arrival measurement, each pixel contains a time-to-digital converter. The time-to-digital converter measures the time difference between the photon detector output and a reference clock. Therefore, to functionalize the TCSPC mode it is important to ensure that the photon detector, time-to-digital converter (TDC), configuration system and the readout system are functioning as desired. Since all modules, other than the TDC are tested in Chapter 4, this chapter concentrates on testing and characterization of the TDC before functionalizing the TCSPC mode.

Organization of the chapter is as follows: In Section 5.1, the test methodology used to test the TDC is presented along with its experimental results. In Section 5.2 a study carried out to understand the behavior of the TDC with increasing pixel count is presented. Followed by it in Section 5.3 and Section 5.4, the characterization results of the TDC are presented. Further, in Section 5.4 the unexpected spike observed in the code density test is analyzed for its cause and drawbacks. The timing resolution measurement results for the MF128 imager are presented in Section 5.6. Section 5.7 extends the study carried out in Section 5.2, under realistic scenario. Further, in this chapter the Fluorescence Life Time Imaging Microscopy (FLIM) technique realized using the MF128 imager is presented. Finally the chapter is summarized in Section 5.8.

5.1 Time-to-digital converter

A time-to-digital converter is a functional module that converts the time difference between two signals into a discrete digital code. The digital output generated by the TDC is proportional to the time difference between the two input signals, provided the quantization error introduced by the TDC is negligible. Therefore, the functionality that needs to be tested in a TDC is whether the TDC measures the time difference between the signals precisely.

The TDC present in the MF128 is designed to convert the time difference between the START and the STOP signals into a 10-bit digital code. In the reverse START-STOP technique used in MF128, the START signal comes from the photon detector and the STOP signal comes from a reference clock.

5.1.1 Test methodology

As mentioned in Chapter 2, by configuring the pixel accordingly it is possible to connect the START signal of the TDC to the TEST start signal. By generating a TEST start and STOP signal with a known time difference ($D1$), we can quantitatively test the

TDC. However, to determine the measured time difference, the resolution of the TDC needs to be known. Since the TDC resolution is not known beforehand, one plausible solution could be to repeat the experiment with another set of START and STOP signals, with a time difference equal to $D2$. By dividing the known input time difference ($D2$) by the TDC generated output code, the resolution of the TDC can be estimated. Using the estimated TDC resolution the measured time difference ($M1$) for the first experiment can be calculated. By comparing the measured time difference ($M1$) with the known time difference ($D1$) the functionality of the TDC can be verified.

However, it should be noted that the resolution measurement technique introduced in the previous paragraph suffers from the timing jitter introduced by the TDC and the START-STOP signal. Furthermore, the non-linearity and the quantization error introduced by the TDC will also affect the measurements. However, the error introduced by the jitter can be significantly reduced by calculating the statistical mean of the TDC measurement, by observing the TDC output many times.

To test the TDC in isolation, the resolution of the TDC is approximately estimated using the technique described above. Even though, it is plausible to estimate the TDC resolution more accurately using the SPAD, as explained in Section 5.4.

5.1.2 Results and discussion

The experiments were carried out using the two different sets of START/STOP signals. To avoid any possible TDC scaling effects, the number of active TDCs in this experiment was maintained at four. In the ideal case the number of active TDC should be one, but because of limitations imposed by the readout system, four TDCs are activated. It should be noted that the restriction of using at least four rows was obtained when the data clock was running at 16 MHz. To get a statistically reasonable result in this experiment 1000 frames of data were accumulated, the results are shown in Figure 5.1.

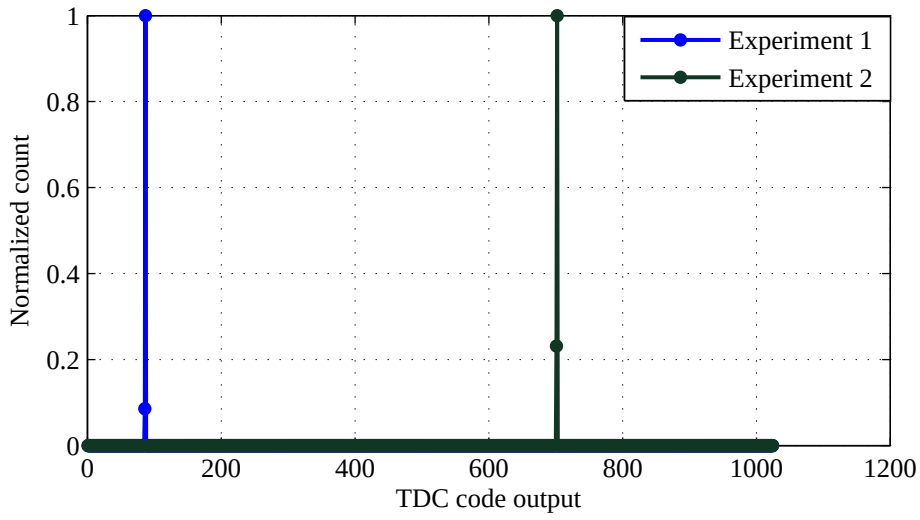

Figure 5.1: Experimental results to test the TDC functionality

The actual time difference between the START and STOP signal in the first exper-

iment is 4.75 ns and for the second experiment is 38 ns. The measured, mean TDC code output for the experiment one is 87 and for experiment two is 702. The estimated resolution from the second experiment is 54.13ps. Using the estimated resolution, the measured time difference for the first experiment is calculated as 4.709ns. By comparing the measured and the actual time difference of the first experiment, it can be conclude that the TDC is functioning as desired.

5.2 Study on scaling active TDCs: Using TEST start-stop signal

5.2.1 Experiment

To study the TDC scaling effect using the TEST start and the STOP signals, one half of the TDC array (ie., 160x64 pixels) was computed. In MF128, the TEST start and the STOP signal for all the TDCs in the pixel array were generated from the same source. Hence an identical TDC output is expected from all the pixels in the array.

To reduce the statistical noise effects, the experiments were repeated thousand times and the mean value of the TDC output code was considered. The mean TDC code output distribution across the one half of the array is shown in Figure 5.2.

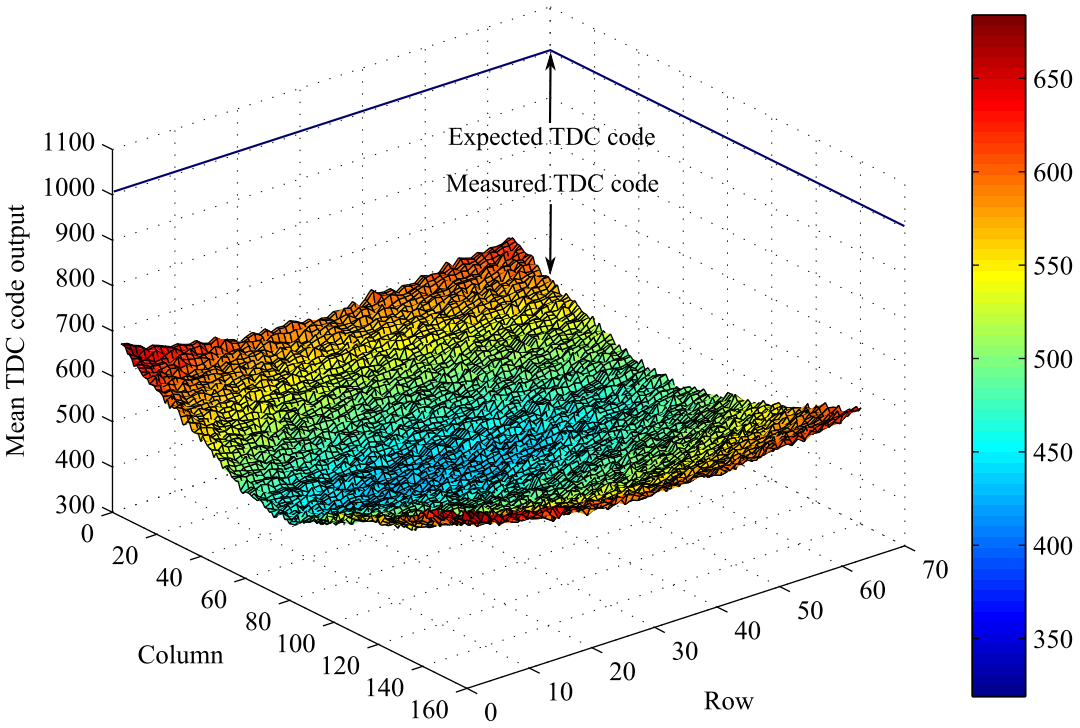

Figure 5.2: Mean TDC code output distribution across the pixel array with 160x64 pixels active, using TEST start - STOP signal

5.2.2 Analysis

From Figure 5.2 two observations can be made:

1. The measured TDC output code is far below the expected value of 1000.
2. The measured TDC output code is not uniform across the array.

Hypothesis: The reason for the measured TDC output code to be less than the expected value could be because of the IR drop in the power line. As the IR drop becomes significant the effective voltage available for a TDC gets reduced from its designed value. The reduction in supply voltage for a TDC will decrease the ring oscillator frequency. Furthermore, the frequency reduction in the ring oscillator will degrade the TDCs resolution and hence the measured TDC code output.

The non-uniformity in the measured TDC bin value across the array could be because of two reasons. One, the propagation delay difference between the TEST start and STOP signal might follow the same trend as observed in Figure 5.2, due to the routing. The other reason could be the voltage sag introduced in the power line because of the IR drop.

Hypothesis evaluation: To evaluate the hypotheses, a set of experiments were carried out. In the first set of experiments, the output of the TDC was monitored by slowly increasing the number of active TDCs. As stated in Chapter 2, a TDC can be activated by enabling its corresponding row and column in the array. In these experiments 64 rows were enabled and the columns enabled were then increased in the steps of 32 from left to right. To reduce the impact of the shot noise a statistical mean of 1000 measurements was used. Column one is observed in all the experiments and then plotted in Figure 5.3.

Figure 5.3 implies that as the number of active columns increases the measured mean TDC code value decreases. The observed decrease in TDC bin value with increasing the active columns can be correlated to the ring oscillator frequency with its supply voltage reduction. This gives us strong evidence that the observed difference between the expected TDC code output and the measured TDC output is because of the IR drop in the power line.

The second set of the experiments were performed to understand whether the variation across the array is because of the propagation delay in the TEST start and/or STOP clock. In these experiments 64 rows and one column were enabled. The parameter that was varied in this experiment was the location of the active column. The location of the active column for this experiment was swept from the left to right.

The experimental results shown in Figure 5.4, imply that the difference between the measured and the expected value is negligible. Also it can be observed that the variation across the array as a function of position is not that significant. This implies that the variation in the TDC value observed across the array in Figure 5.2 is not caused by the propagation delay of the TEST start and the STOP signal.

As stated earlier the other hypothesis could be because of the voltage sag introduced in the power line, due to IR drop. If this hypothesis is valid then almost identical variations in the TDC output code should be observed in all part of the array. Furthermore, the variation in the TDC output code should become severe as we keep increasing the

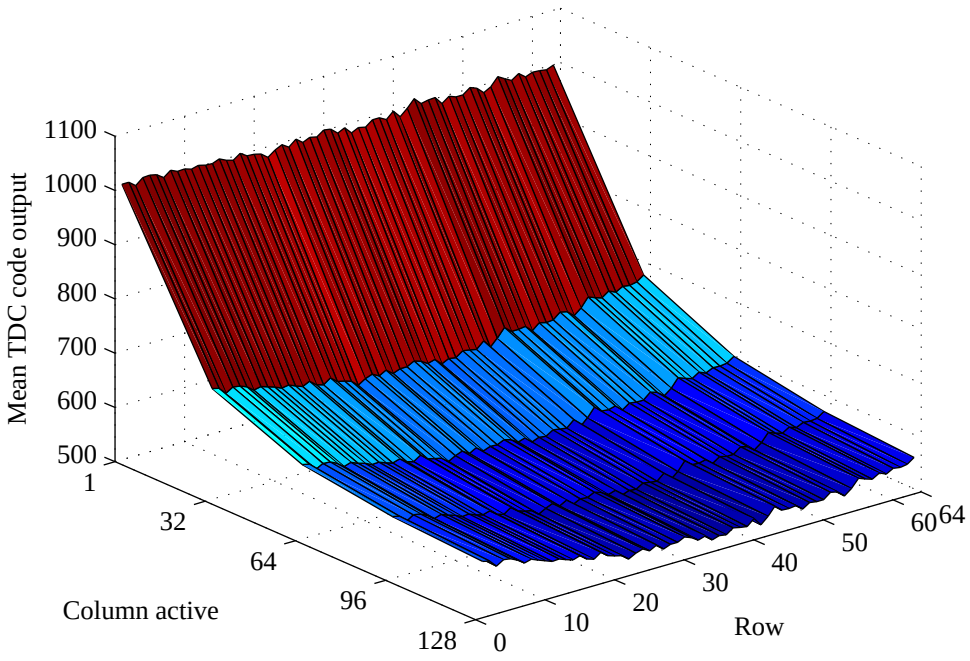

Figure 5.3: Effect on mean TDC code output on column 1, with increasing active column

active columns. To test it a group of (64 rows x 32 columns) TDCs were made active in different parts of the array. From the experimental results shown in Figure 5.5 and in Figure 5.6, it is clear that almost equal variation in TDC output code is observed in different parts of the array. Further, by comparing Figure 5.6 and Figure 5.2, it can be seen that the variation in TDC output code across the array becomes worse as the number of active TDC is increased. These two results supports that the cause for dip in TDC output is because of the voltage sag.

If the voltage sag is the cause for the TDC output code variation then the propagation delay of the START and the STOP signal will also get affected. Thus the observed variation in the TDC output code across the array in Figure 5.2 is because of both the supply voltage variation and also due to the variation in the propagation delay of the START/STOP signal.

5.2.3 Inference

It is vital to understand that the experiments carried out using the TEST start and STOP emulated a worst-case scenario of activating all the TDCs at the same time. However, in photon-starved applications for which the MF128 was designed, it is unlikely to reach a state where all the TDCs are active at the same time, as the intensity of the light available for these application is not high enough to activate all the TDCs concurrently.

An interesting observation is that as the number of active TDC increases the TDC

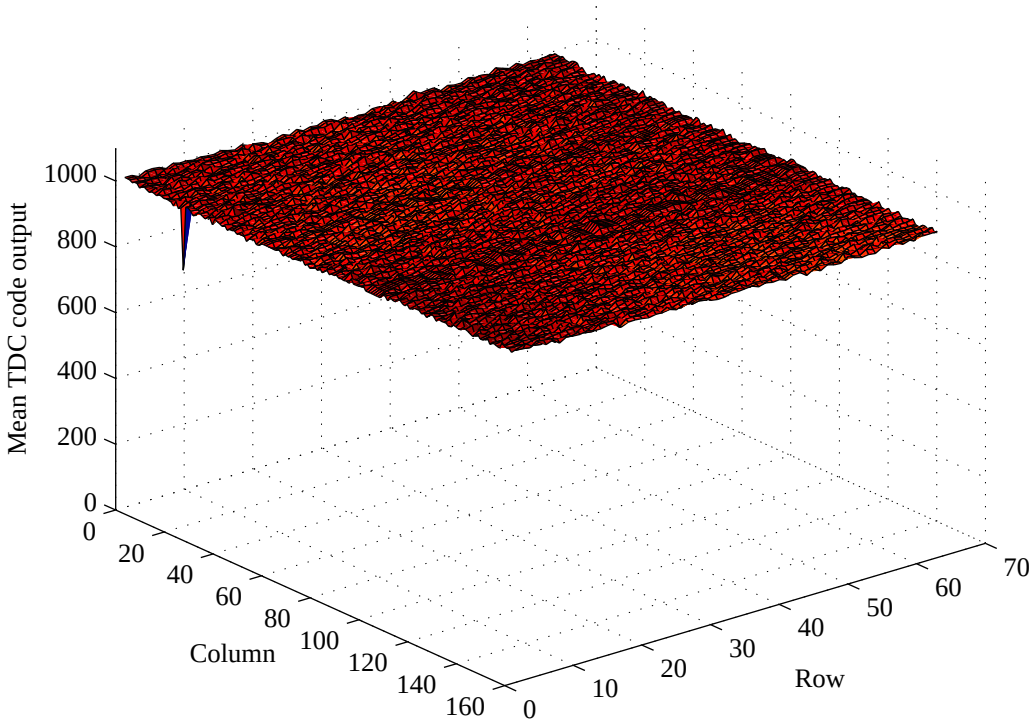

Figure 5.4: Mean TDC code output observed with one column active at a time

error also increases. In real time the number of TDCs active at a time depends on the intensity of the light and also the number of enabled pixels. Therefore, the evidence implies that in MF128 the TDC performance depends indirectly on the intensity of the light and also on the number of pixels enabled. To understand the relation between the TDC performance, light intensity and enabled pixel count a study was carried out in Section 5.7.

5.3 TDC jitter measurement using electrical impulse

To measure the TDC jitter, the TEST start and the STOP signal are generated with a known time difference between them. In this experiment to avoid any scaling effect, only four TDCs were enabled. Since the TDC is based on a ring oscillator there is a high chance that the TDC might be affected by the multiplicative error. To evaluate the multiplicative error two different experiments were performed. These two experiments were designed such that the TDC output is at the two extreme ends of the TDC range. The experimental results of the two experiments are shown in Figure 5.7.

It is to be noted that the plot in Figure 5.7, is obtained from the data collected over 1000 frames. The observed difference in full width half maximum (FWHM) in two experiments can be attributed to the multiplicative error introduced by the ring

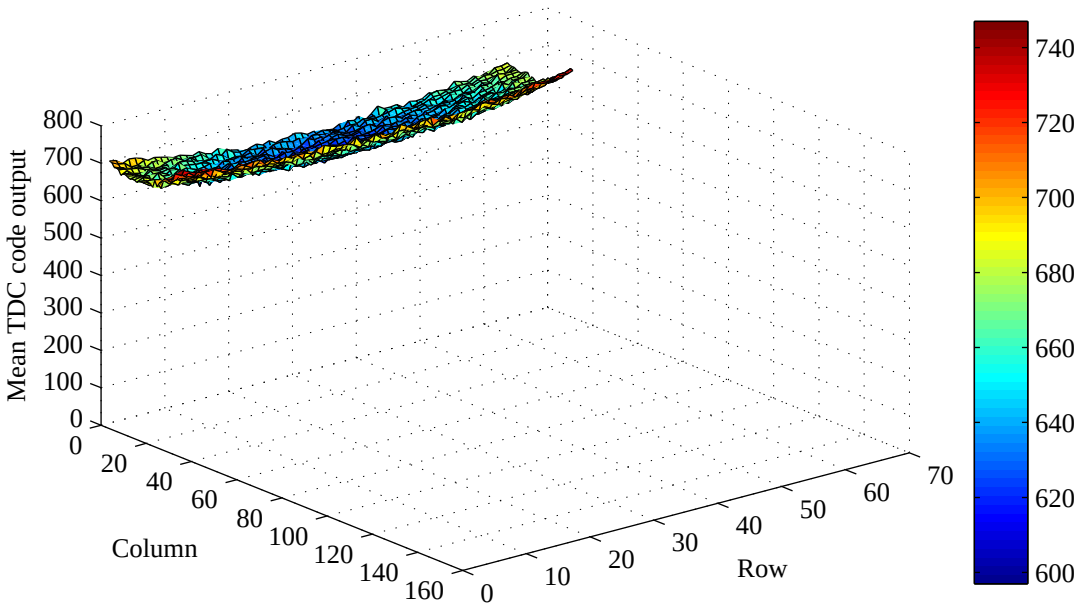

Figure 5.5: Mean TDC output code distribution across the pixel array, with 32x64 pixels acive at one extreme of the array

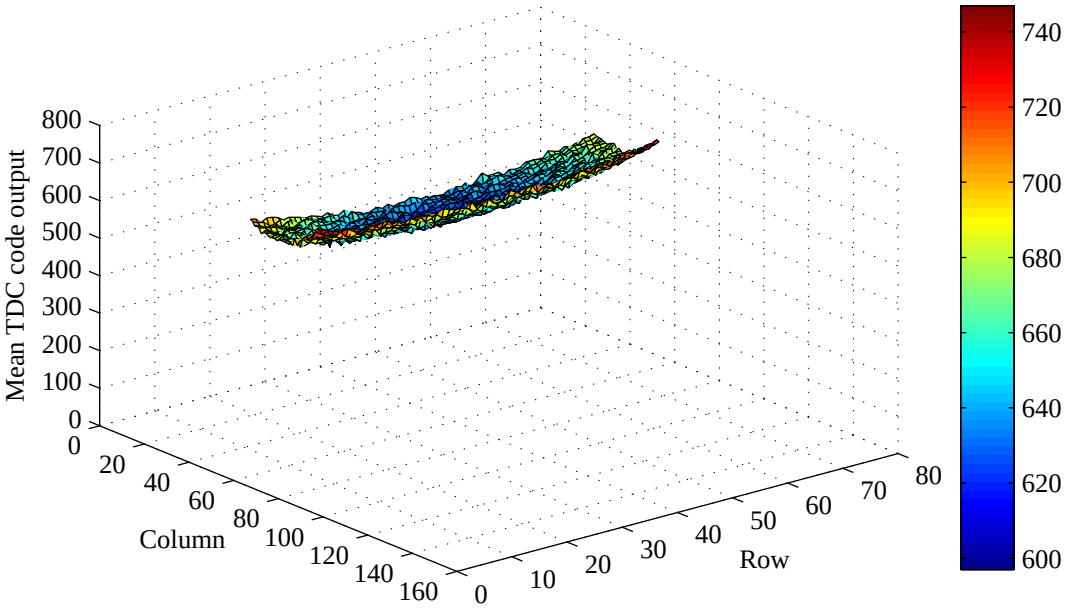

Figure 5.6: Mean TDC output code distribution across the pixel array, with 32x64 pixels acive in the center of the pixel array

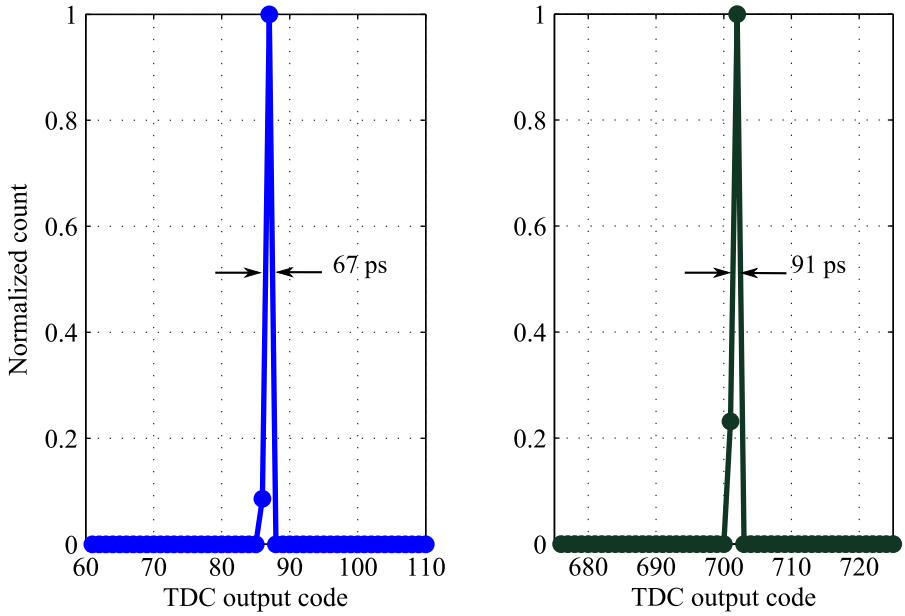

Figure 5.7: TDC jitter measurement

oscillator. It is important to comprehend that the FWHM observed in this experiment is contributed by two sources of jitter one from the START/STOP signal and other by the TDC itself. In this experiment the jitter introduced by the START and STOP is considered to be negligible.

5.4 Code density test

5.4.1 TDC output range test

Test Methodology

In the previous section, the TDC functionality was tested only for a few TDC outputs. To test the TDC for all possible outputs, the code density test [24] can be used. In the code density test, a start signal having a uniform probability of occurrence across the TDCs range is used. Hence in this test, a histogram formed from the TDC output monitored for a sufficiently long time is expected to have a uniform distribution of counts across all the TDC bins in the histogram. Therefore, a TDC can be tested by monitoring the uniformity of the counts across the TDC bins.

However, in reality the histogram formed from the TDC output will have non-uniformities in the TDC bin counts. The non-uniformity in the counts is due to the TDCs non-linearity and the shot noise introduced due to the insufficient collection of data. The error introduced by the shot noise can be made insignificant by sufficiently increasing the data accumulation time. For a monotonic TDC, the error introduced due to the non-linearity can be one order of magnitude higher or lower than the mean count observed across the TDC bins. Therefore to incorporate the non-linearity, an

error margin can be introduced. The error margin can be one order of magnitude higher or lower than the mean counts observed across the TDC bins.

In MF128, the START signal having approximately a uniform probability distribution of occurrence across the TDC range can be generated using the photon detector output. The photon detector, either placed in dark or under a diffused light can generate a START signal having approximately a uniform probability distribution. In general a photon detector with SPAD either placed in dark or under a diffused light has a poissonian time-of-arrival, thus it will have an exponential probability distribution. The exponential probability distribution function [25] is defined as

$$f(\lambda, t) = \begin{cases} \lambda e^{\lambda t} & \text{t} \geq 0 \\ 0 & \text{t} < 0 \end{cases} \tag{5.1}$$

Where λ is the photon count rate

From Equation 5.1 it can be inferred that the decay rate of the exponential function depends on the photon count rate of the SPAD. Therefore by maintaining low count rate it is possible to attain approximately a uniform distribution across the TDC range.

When using the SPAD as a source of start signal, the data accumulation time for a TDC will depend on whether the experiment is carried out in the dark or under diffused light. In the dark, the data collection time depends on the DCR of the pixel. Under diffused light it depends on the intensity of the light. In either of the scenarios, the data accumulation time reduces by increasing the count rate. However, it is to be noted that when the count rate increases, the probability distribution function tend to deviate more from the uniform distribution as explained earlier. Therefore a subtle trade-off between the photon count rate and data accumulation time need to be made.

Results and discussion

The TDC connected to the SPAD is observed in dark for about eight hundred thousand frames of data with a frame rate of 25 kfps. The histogram formed from the data collected for one of the pixel is shown in Figure 5.8. The dark count rate of the observed pixel is about 3.7 kHz. Using Equation 5.1 we can estimate the error introduced due to the exponential decay of the distribution function. For a pixel having a count rate of 3.7 kHz and the TDC range in the order of approximately 55ns will have a 0.0203% decrease in count from the first bin to the last TDC bin. Since the difference in the distribution across the TDC bins is negligible, we can assume that the distribution is uniform across the TDC range.

The experimental results shown in Figure 5.8, it can be inferred that there is an unexpected spike in the histogram. Other than the spike the counts observed for other TDC bins are within the error bound.

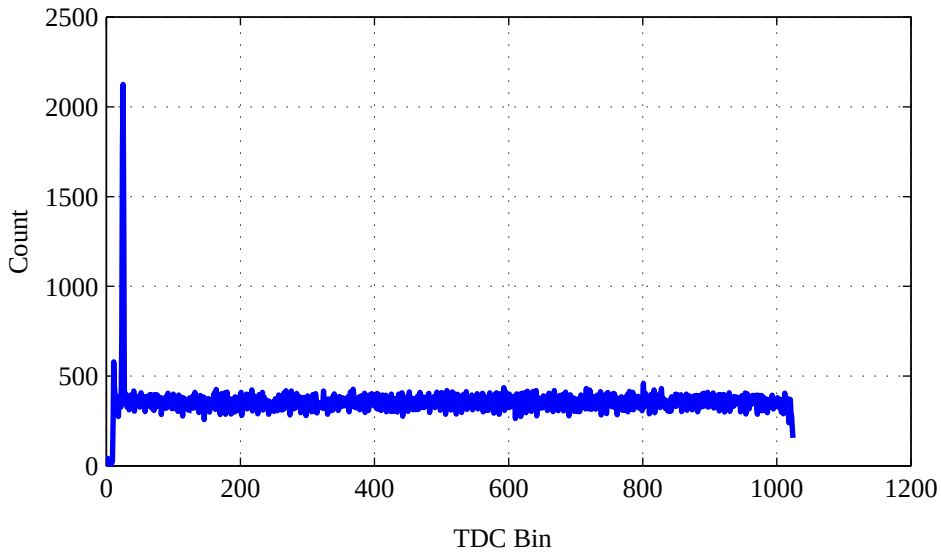

Figure 5.8: Code density test output

5.4.2 Unexpected spike

Understanding the spike cause

A series of experiments were carried out to understand the spike cause. A general observation from these experiments, as shown in Figure 5.9 is that the location of the spike in the histogram is not fixed. This observation implies that the spike is not introduced because of the TDCs non-linearity.

Unexpected experiment and interesting observation

In one of the experiment carried out in the TCSPC mode fortunately the SPAD was switched off. In this configuration, the output across the array followed a pattern very similar to the experimental results obtained using the TEST start and the STOP signal. Since in this experiment both the known sources of the start signal (the test start and the SPAD) are switched off, it is unclear from the START signal for this experiment is originating from.

To understand the source generating the START signal an experiment was carried out to measure the time difference between the START pulse and the STOP signal. In this experiment four pixels were made active to avoid any possible scaling effects. The experimental results revealed that the TDC reset might be the source of the START signal. To validate the observation, an experiment was performed by varying the delay difference between the TDC reset and the STOP clock. The results of the experiment supported the previous observation of the TDC reset being the source of the START signal.

To understand how the TDC reset is coupled to the START signal, a detailed study on the pixel architecture was carried out. From the study it was found that when the

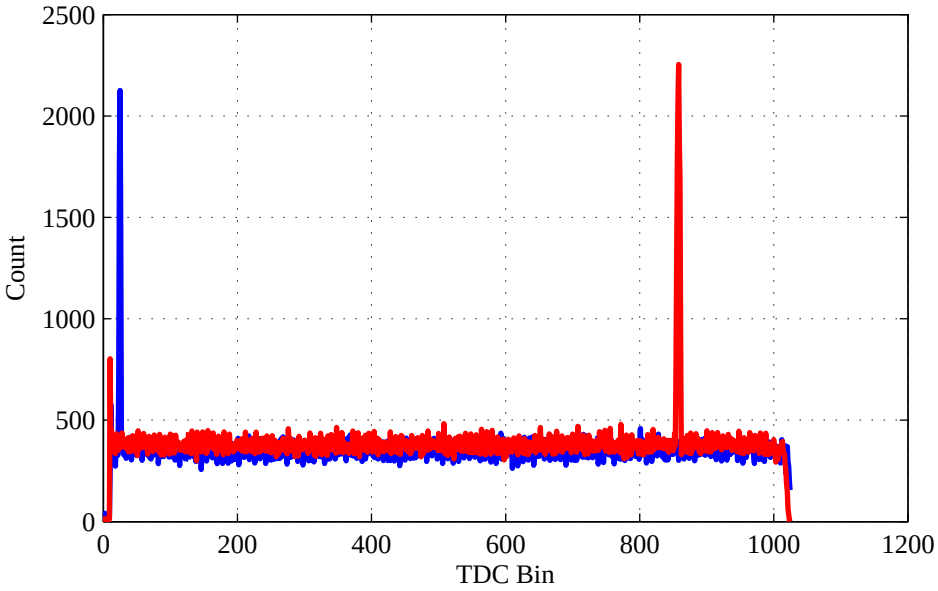

Figure 5.9: Code density test: variation in the location of the spike

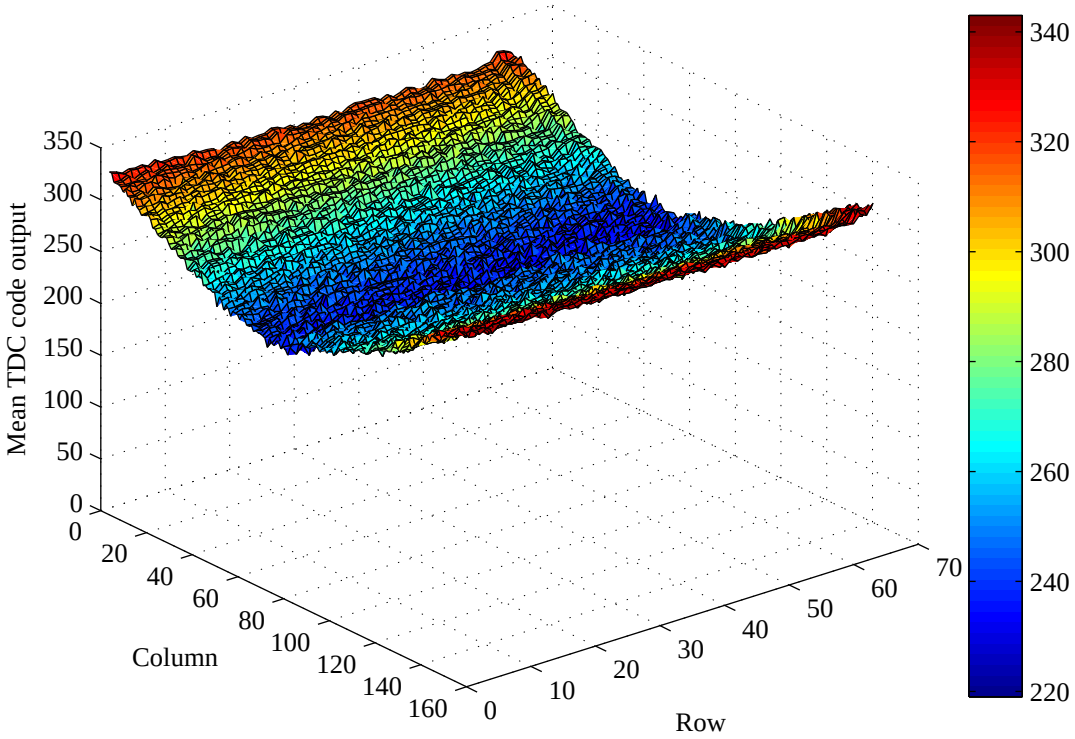

Figure 5.10: Mean TDC code output in TCSPC mode with SPAD off

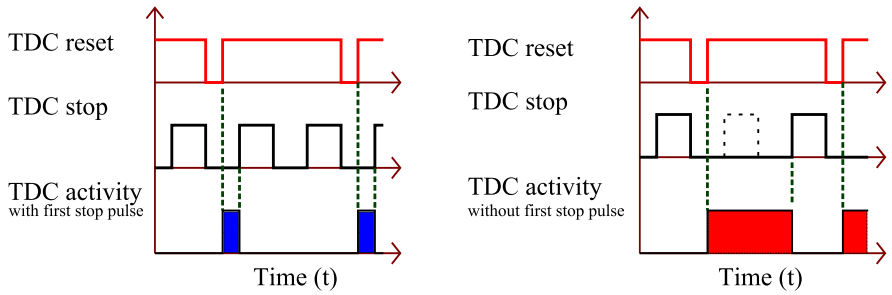

Figure 5.11: Timing diagram: showing different time difference between the TDC reset and stop clock, used to study the spike cause

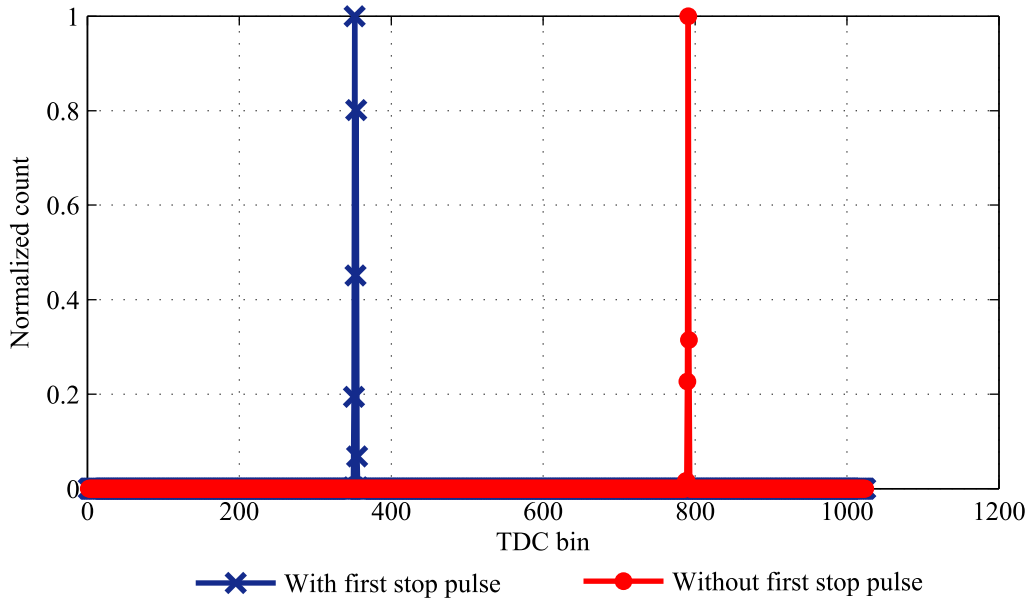

Figure 5.12: Experimental results of two different experiments with different delay between the TDC reset and stop clock, with SPAD off

SPAD is off, the inverter output is always high. In other words when the SPAD is off the TDC start signal is always high. Based on this, we can hypothesize that when the TDC is brought out of the reset, the TDC starts measuring on seeing the START signal in the high state.

From the pixel architecture it can be interpreted that when the SPAD is on, the TDC start signal is high only when the SPAD triggers. Extrapolating the observation made in the previous paragraph, it is possible to hypothesize that the observed spike in Figure 5.8 is due to the SPAD getting triggered just before the TDC is brought out of the reset.

If this hypothesis is true, the location of the spike in the histogram plot corresponds to the time difference between the TDC reset and the first stop pulse after the TDC reset. To verify the hypothesis, an experiment was carried out by removing the first

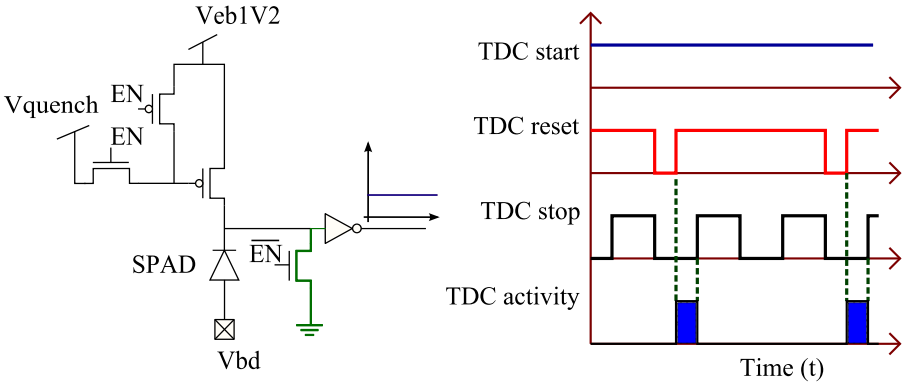

Figure 5.13: Pixel architecture analysis to understand the spike cause

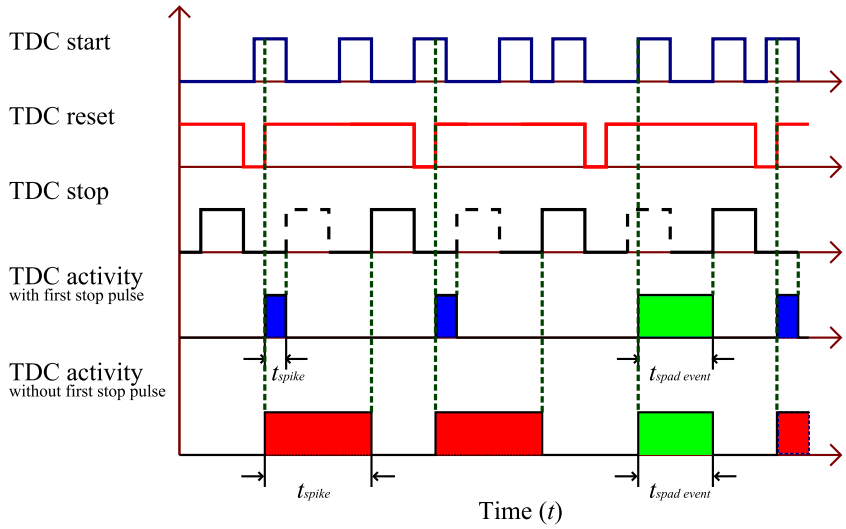

Figure 5.14: Timing diagram: showing the spike cause with and without first stop pulse after TDC reset

stop pulse after the TDC reset. In this experiment, as expected the spike location got modulated to the far end of the TDC range as shown in Figure 5.15. This observation proves that the cause for the unexpected spike is the SPAD being trigged just before the rising edge of the TDC reset. Hence, it can be concluded that the location of the spike in the histogram depends on the time difference between the TDC reset and the first stop pulse after the TDC reset.

Drawbacks of the spike

Time-correlated measurements are used in range-finding applications and biological applications such as FLIM. In all applications related to the TCSPC mode the spike might lead to the misinterpretation of the actual data. Thus it is important to remove this spike from the region of interest.

Plausible solution

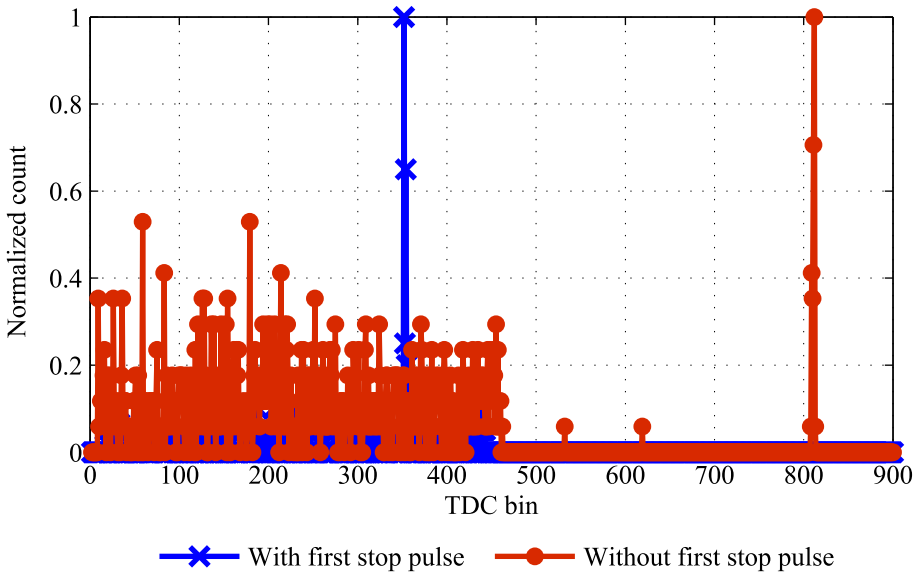

Figure 5.15: Experimental results with SPAD on: Before and after removing first stop pulse after TDC reset

1. Spike modulation technique

One solution to remove the TDC reset spike is to engineer the readout timing such that the spike is re-located to the TDC bins that are of no interest to us. For example when using the STOP clock with a frequency of about 40 MHz the number of used TDC bins is less than the half of the total. Hence, by removing the first stop pulse after the reset will modulate the spike to the after end of the TDC range. Experimental results with and without the first stop pulse is shown in Figure 5.15.

The drawback in this solution is that when the first stop pulse after the TDC reset is removed, the exposure time of the STOP clock coming just after the TDC reset is increased. Increasing the exposure time for a stop pulse will certainly increase the probability of number of active TDC at most by a factor of two in our case. This can affect the TDC performance as the number of active TDC increases. However, the increase in exposure time is significantly less in absolute terms, and also the intensity of light is very low for our applications. Hence we can neglect this effect.

The other drawback in this method is that the modulated spike location depends on the stability of the TDC resets timing with respect to that of the STOP clock. To study the stability of the TDC reset, experiments were conducted under different light intensities. To differentiate the instability of the STOP clock and the TDC reset, a time correlated light source was used. With the a time-correlated light source, the histogram formed using the TDC output observed for a long time will have two spikes one corresponding to the TDC reset and other corresponding to the light source. The spike corresponding to the light source is called as an optical spike. Under a time-correlated light source, the instability of the STOP clock and the TDC reset can be distinguished. The instability in the STOP clock can be observed as a variation in

the location of the optical spike in the histogram. On the other hand, the TDC reset instability can be evaluated by removing the variation of the STOP clock from the TDC induced spike variation.

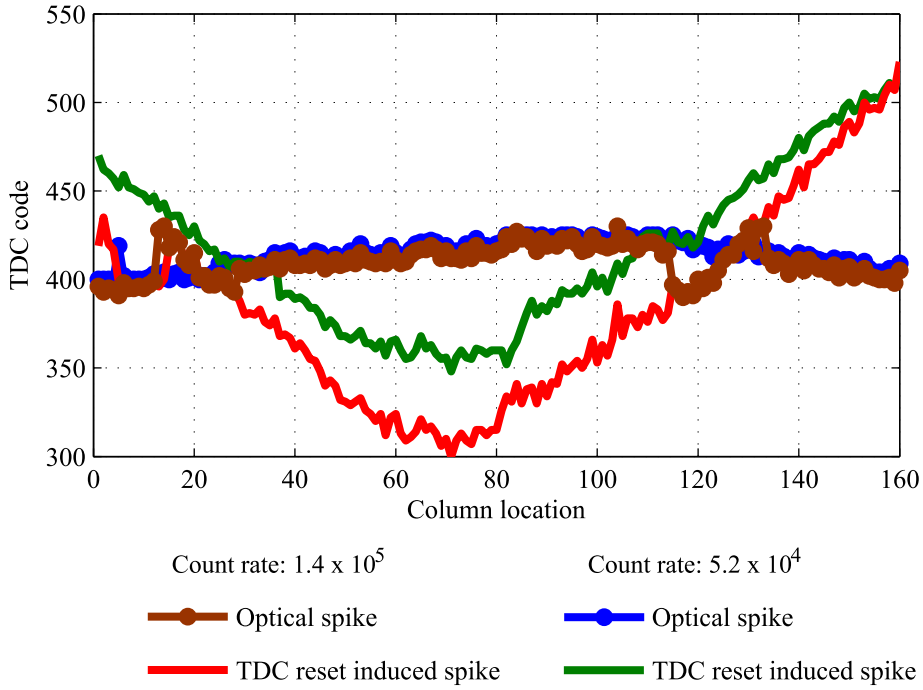

Figure 5.16: TDC reset instability

A summary of the experimental results is presented in Figure 5.16. The experimental results imply that the variation in the location of the optical spike is negligible. Although there is a shift in the location of the optical spike as we move across the column. This shift in optical spike can be due to the propagation delay of the STOP signal, entering the imager from either ends of the chip. Assuming that the shift in the optical spike location across the column is due to the propagation delay, it can be inferred that the propagation delay of the STOP clock is stable with increasing light intensity.

In contrast the TDC reset induced spike varies across the column. Furthermore, the variation in the TDC reset induced spike becomes more pronounced as the light intensity increases. This observation can be extrapolated to a scenario where the variation of TDC reset induced spike can interfere with the TDC bins that are of interest to us. Hence it can be conclude that the technique of modulating the TDC reset spike will not be effective for applications with high light intensities.

Other observation

The increase in the variation of the TDC reset induced spike with the light intensity can be due to digital noise effect. From Figure 5.16 it can be comprehended that the temporal position of the TDC reset varies across the columns. This implies that the light exposure time for a pixel varies with its spatial position. Because in MF128 the

exposure time for every frame is defined as a time period between the TDC reset and the write signal. The variation in the TDC reset induced spike location is roughly 200 LSBs, when the median count rate is about 5.2 x 10^2. For a frame clock running at 25 kHz, the variation of 200 LSBs with 55ps of TDC resolution corresponds to about 0.0275 % of the frame period. Even though the error percentage is negligible, it should be noted that this error can go up when either increasing the frame rate or the light intensity. It is vital to accept that the argument on the exposure time period variation depends also on the stability of the write signal as well.

2. Spike diffusion technique

Another possible solution could be to use two uncorrelated clock sources to generate the TDC reset and the STOP clock. In this setup because of the drift between the two clock sources, the time interval between the TDC reset and the first STOP pulse varies randomly. Due to the generated randomness in the time interval between the TDC reset and the STOP pulse, the TDC reset spike will be scattered across the TDC bins. Thus the TDC reset spike can be diffused. However a problem with this method is that the diffused TDC reset spike will be seen as a white noise, increasing the noise floor in the histogram, which was originally contributed by the DCR and the background noise. The increase in noise floor will cause the loss of one or more LSBs in the TDC range depending on the intensity of the light.

Analyzing the drawbacks of the two methods, it is possible to conclude that the TDC reset spike diffusing method is comparatively better that the TDC reset spike modulation technique, because losing one or more LSBs due to the increase in noise floor is better than misinterpreting the collected data itself.

5.4.3 TDC resolution measurement

The minimum time interval that can be measured using a TDC is called as the resolution of the TDC. A technique used to measure the TDC resolution using the TEST start and the STOP signal is presented in Section 5.1. The other technique to measure the TDC resolution is by using the results of the code density test.

Methodology

As explained in Section 5.4, in a code density test the TDC bins in the histogram will be populated with almost equal counts. For a TDC using STOP clock, the observed TDC output code will correspond to the start pulse appearing from just after the previous stop pulse to the current stop pulse. Therefore, the number of bin that gets populated is directly proportional to the time period of the STOP clock. The proportionality constant in the above relation is the TDC resolution. Therefore by knowing the STOP clock period and the number of populated bins the resolution of the TDC can be determined.

$$TDC_{resolution} = \frac{\text{STOP clock period}}{\text{Number of populated bins}} \tag{5.2}$$

The TDC resolution measurement technique explained in Section 5.1 suffers from START-STOP signal jitter, quantization error and the non-linearity error. On the other hand in using the code density test to measure the TDC resolution, the jitter of the START signal becomes insignificant as the data is collected for a large number of frames. The non-linearity and quantization error introduced by the last observed bin in the code density can increase or decrease the populated TDC bin count by one. The error introduced in the TDC bin count can be made negligible, by increasing the STOP clock period. Therefore by using the code density test the error introduced by the clock jitter, TDCs non-linearity and the quantization error can be reduced significantly. Hence, the code density is comparatively better than the method using the TEST start and STOP signal. However in using the code density test, it is important to avoid using very high intensity of light. The problem of using high light intensity is that it can degrade the TDC resolution measurement, due to the TDC scaling effect as predicted in Section 5.2.

Results and discussion

The experimental results of the TDC resolution measured across the array is shown in Figure 5.17. This experiment was performed with a light intensity corresponding to the count rate of about 16kHz.

From the TDC resolution distribution across the array, two inferences can be made:

1. The FWHM variation in the TDC resolution across the array is 2.7 ps.
2. The median TDC resolution considering 160x64 TDC is 55.64 ps.

5.4.4 TDC non-linearity measurement

The TDCs non-linearity is defined by two terms viz. the differential non-linearity (DNL) and the integral non-linearity (INL). The differential non-linearity defines the deviation of a TDC bin duration from the average TDC bin duration. On the other hand the integral non-linearity measures the deviation of the actual measurement from the expected output. Hence, the integral non-linearity for every TDC bin can be calculated by integrating the DNL of the preceding bins.

Methodology

The non-linearity error for a TDC can be evaluated using the code density test [26, 27]. In the code density test for an ideal TDC when observed for a sufficiently long time will have equal count in all the TDC bins of the histogram. However, due to the variation in the TDC bin duration, the counts observed across the TDC bins are not constant. The percentage variation in the TDC bin count with respect to the average bin count will correspond to the DNL of that particular bin. Hence the INL and DNL for a TDC can be evaluated using the code density test results and equations [26] given below.

$$DNL_i = \frac{C_i - \overline{C}}{\overline{C}} \tag{5.3}$$

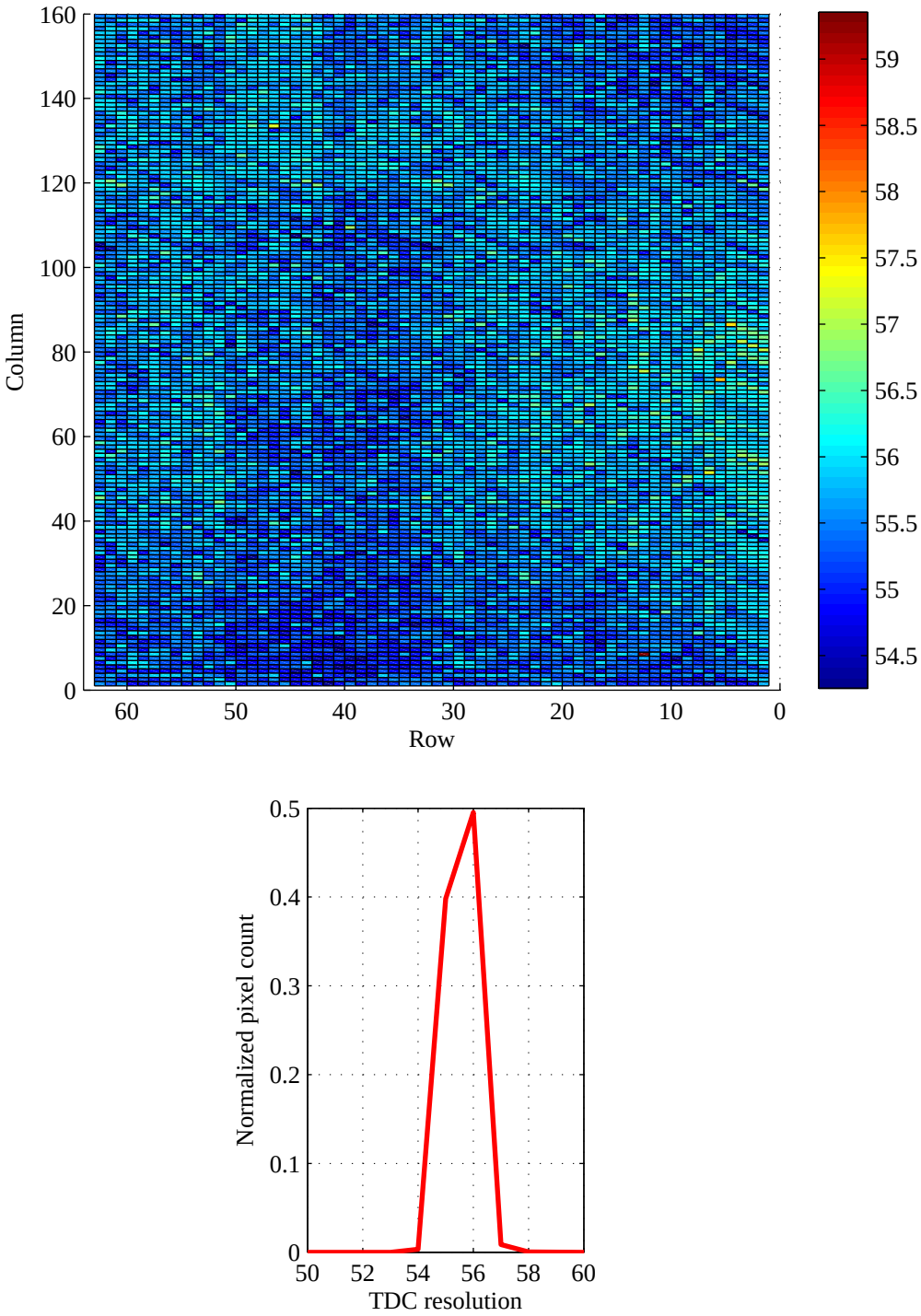

Figure 5.17: Resolution distribution

Ci : number of counts in bin i
$\overline{C}$: mean counts across all the bins
INL of the TDC can be calculated from the DNL measurement using

$$INL_i = \sum_{j=1}^{i} DNL_j \tag{5.4}$$

Results and Discussion

To eliminate the TDC scaling effects as described in Section 5.2, the experiment was carried out in dark. Furthermore, to reduce the shot noise introduced due to insufficient collection of data, the data accumulation time was sufficiently increased. The experimental result for the DNL and INL measurement for one pixel is shown in Figure 5.18. The dark count rate of this pixel is 3.7 kHz. The data accumulation period for this experiment is about eight hundred thousand frames of data, with each frame running at 25 kHz. As pointed out in Section 5.4, for a pixel with a count rate of about 3.7 kHz the error introduced by the exponential decay of the PDF is in the order of 0.0275%. Since the error percentage is negligible it can be assumed that the distribution is uniform across the TDC range.

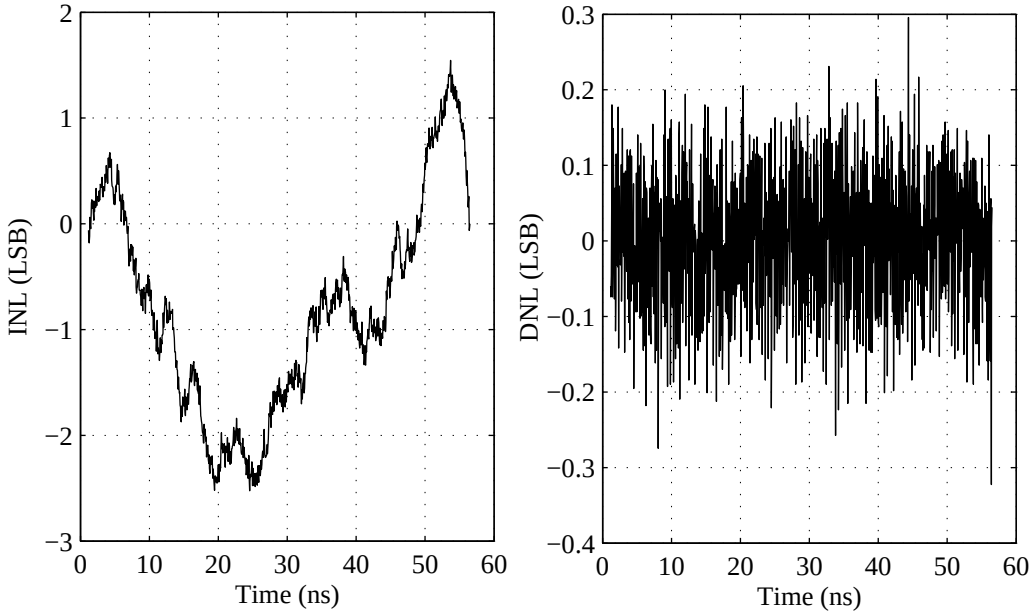

Figure 5.18: INL and DNL

5.5 TCSPC test

In the previous sections the MF128 was tested in TCSPC mode using an un-correlated light source. This section will explain the test methodology used to test and characterize

the MF128 with a time correlated light source. Using a time-correlated light source it is possible perform a time-of-arrival measurement.

5.5.1 Test methodology

The functionality that needs to be tested in the TCSPC mode is the photon time-of-arrival measurement. In MF128 the time-of-arrival measurement is made using the STOP clock as a reference. Hence to perform the time-of-arrival measurement it is important to maintain a constant phase relation between the stop clock and the light source. Even though a constant phase relationship is maintained, it is impossible to exactly know the phase difference between the light source and the stop clock in advance. Therefore to test the time-of-arrival measurement two experiments are required. In the first experiment the phase difference between the light source and the stop clock can be determined. In the second experiment photon time-of-arrival measurement can be tested, provided the light source is displaced by a known distance from the first experiment. Hence, by evaluating the difference in the time-of-arrival measurements from two experiments and using the speed of light, it is possible to measure the distance to which the source has moved. By comparing the actual distance with the measured distance the photon time-of-arrival measurement can be tested.

5.5.2 Results and discussion

In this experiment the pulsed laser was used as a source of light. The light pulse emitted by the laser was in-sync with the STOP clock. To avoid any scaling effect one column of the pixels were activated. The experimental result of the experiment conducted in two different positions of the laser is shown in Figure 5.19.

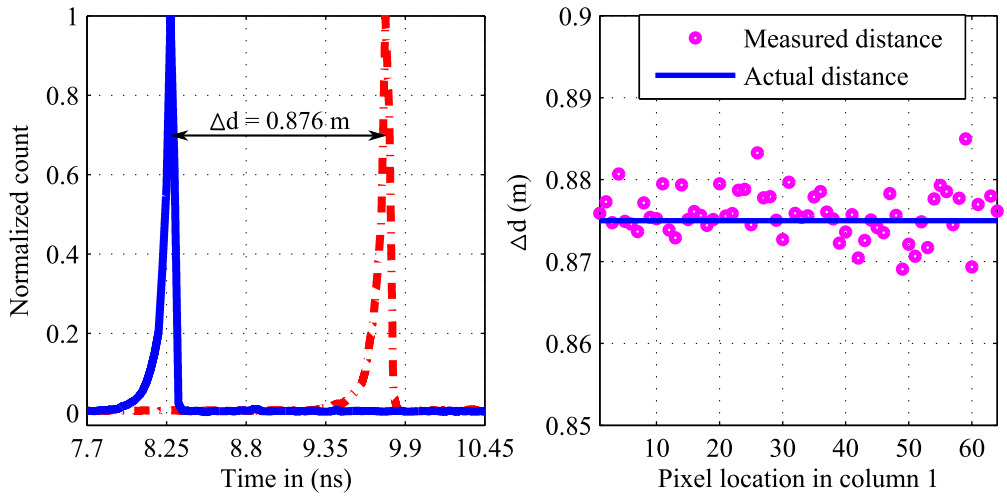

Figure 5.19: TCSPC testing: In the left plot, blue and red curves represents the optical spike captured in two different positions of the laser. Plot in the right compares the measured and the actual distance the laser has moved.

The experimental results imply that the error between the measured and the actual distance is almost negligible. This proves that the time of arrival measurement is working as desired.

5.6 Timing resolution

In the timing resolution measurement for the MF128 imager the timing jitter of the whole experimental setup is evaluated. In the MF128 experimental setup the timing jitter can be introduced from various sources such as the photon detector, TDC, STOP clock and the light source.

The jitter introduced by the photon detector reveals the statistical fluctuation in the time interval between the photon arrival and the TDC start signal generation [15, 14]. For the SPAD based detector as in MF128, the photon detector jitter contains two components viz. gaussian and an exponential component [28]. The gaussian component is due to the statistical nature of the avalanche process initiated by a photo electron generated in the depletion region of the diode [28]. On the other hand the exponential component is due to the photon electron/hole created outside the depletion region, when it needs to diffuse to the depletion region to initiate an avalanche [29]. The jitter introduced by the gaussian component depends on the ionization coefficient of the electrons and holes in the depletion region. Hence by increasing the ionization coefficient the gaussian contributed jitter can be reduced. This can be achieved by increasing the excess bias voltage of the SPAD [15].

To evaluate the timing resolution for every pixel in MF128 an experiment was carried out using a pulsed light source. In this experiment a self-oscillating laser source with the inherent jitter of about 20ps was used. The clock in-sync with the light source generated by the laser is used as a STOP clock. To avoid any possible scaling effect four pixels were made active during the measurements. The experiment was carried out using two different light wavelengths viz. 405nm (blue) and 637nm (red). To study the effect of the excess bias on the jitter, the experiments were repeated at three different excess bias voltages.

The experimental results obtained after collecting three hundred thousand frames of data with the frame rate of 25 kHz is shown in Figure 5.20. Figure 5.20 depicts the performance of one pixel. From Figure 5.20 it can be ascertained that by increasing the excess bias voltage the timing jitter is reduced. This observation is in line with the theory explained earlier in this section.

5.7 Study on scaling active TDCs: Under light

In Section 5.2 the effect of activating TDCs simultaneously was studied. Even though the study made in Section 5.2 emulated an unrealistic scenario of activating all the TDCs at the same time, it helped us to understand that the performance of the TDC can degrade when the number of active TDCs increases. In TCSPC under light the number of TDCs working simultaneously depends on the intensity of the light and the number of pixels enabled. This observation motivates us to study the performance of

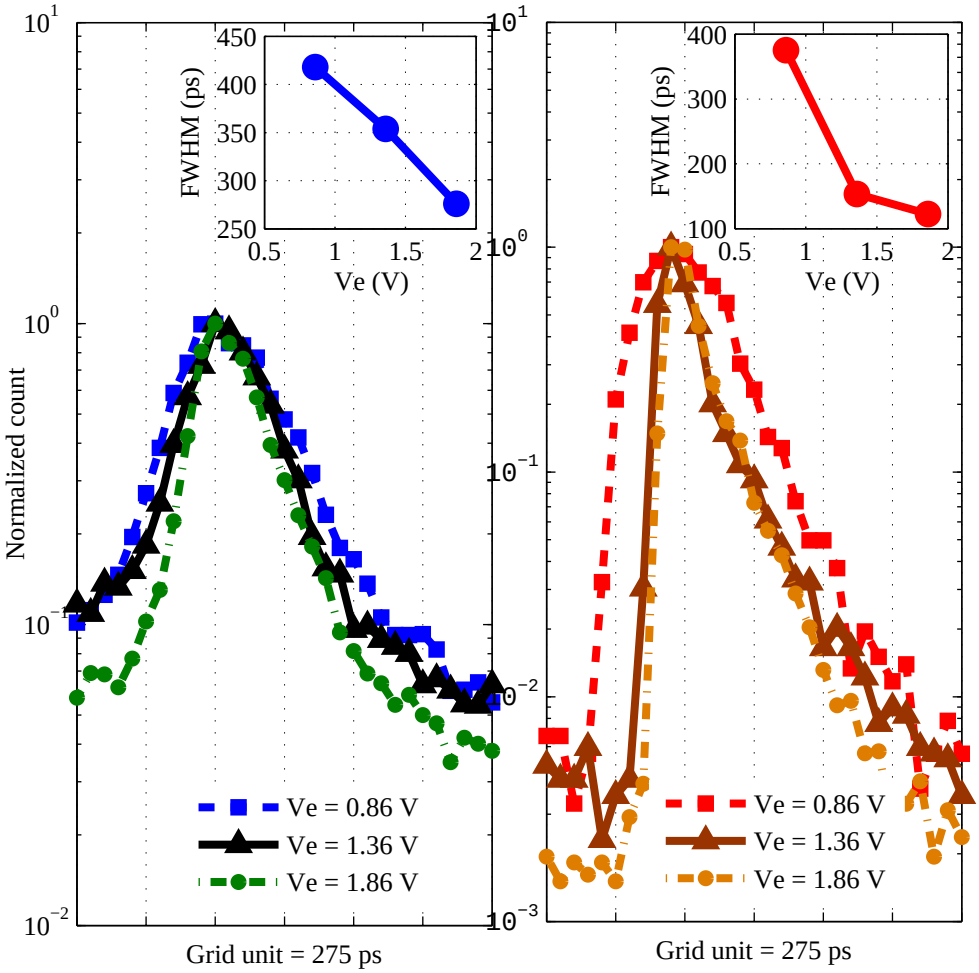

Figure 5.20: Jitter measurement varying excess bias voltage (V_e)

the TDC under various light intensities and with various counts of the enabled pixels.

When performing the TCSPC experiment using a time-correlated light source, an optical spike corresponding to the time correlated photon is created in the histogram. The performance degradation of a TDC due to the increase in active pixels can be seen either as a shift in the location of the optical spike and/or as an additional source of jitter. The shift in the optical spike to the left becomes pronounced when the IR drop in the line is significant. However if the IR drop is not that significant to shift the optical spike, then the scaling of active TDCs can affect the jitter measurements. Therefore the effect of increasing the active TDCs can be studied by measuring the shift in optical spike location as well as the variation induced in its jitter. This technique of analyzing the TDC scaling effect is referred as *TDC scaling jitter-optical spike location measurement technique* in this thesis.

To emulate the real time scenario of increasing the simultaneously working TDCs, the experiments were conducted under various light conditions and also by varying the

number of enabled columns. Figure 5.21 shows the experimental result of a pixel while varying the number of enabled columns. It is to be noted that this experiment was conducted in the photon-starved regime, with a photon count rate of 17 kHz. From Figure 5.21 it can be observed that even under the photon-starved condition there is a progressive shift in the centroid of the optical spike to the left. Also we can observe an increase in the optical spike jitter with the increase in enabled columns. Since both the performance parameters degraded with the increase in the enabled columns, we can infer that the cause for the performance degradation is due to the TDC scaling.

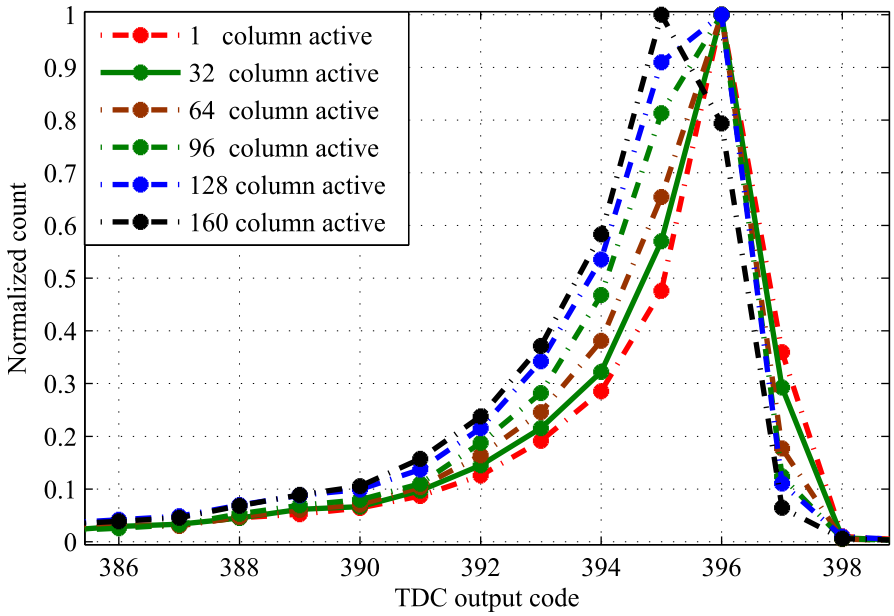

Figure 5.21: Effect on optical spike with increasing number of active pixels

However in the above stated example fortunately both the performance parameter degraded with the increasing column. But there is plausibility that the optical spike location can degrade and the jitter measurement can show a better performance. This situation will arise when the IR drop becomes significant. When the IR drop becomes significant the TDC resolution will also degrade. Hence the number of TDC bin measured for the jitter will reduce. To evaluate the jitter in terms of time units, resolution of the TDC needs to be known. Since it is not plausible to track the variation in the TDC resolution in real time, we decided to use the TDC resolution measured under the optimal conditions. Using the TDC resolution measured under optimal conditions for evaluating the jitter will result in overestimating the jitter measurement. Therefore based on the measured jitter and the shift in the optical spike it is not possible to study the TDC scaling effect under all feasible scenarios. Hence a better technique to evaluate the TDC scaling effect is required.

One plausible technique to characterize the TDC scaling effect could be to measure the time span ($t_{timespan}$) covered by the optical spike obtained under the optimal and worst-case scenario. As shown in Figure 5.22. The definition of the optimal and worst

case scenario depends on the parameter that is used to study the TDC scaling effect. As stated earlier the TDC scaling effect can be studied either by increasing the light intensity or by increasing the enabled pixels. For studying the TDC scaling effect using light intensity, the optimal condition is when the light intensity is low and the worst case scenario is when the light intensity is very high. On the other hand, for the TDC scaling study based on the enabled pixels count, the optimal condition is when fewer TDCs are enabled and the worst-case being when all the TDCs are enabled. Furthermore, the time span between the two edges of the spike can be measured at the fifty percent of their corresponding spike peak. The advantage of using fifty percent of the spike peak is that it will help us to compare the variation introduced by the TDC scaling with the generally reported FWHM jitter performance. This technique to characterize the TDC scaling effect is referred as the *TDC scaling time-span measurement technique* in this thesis.

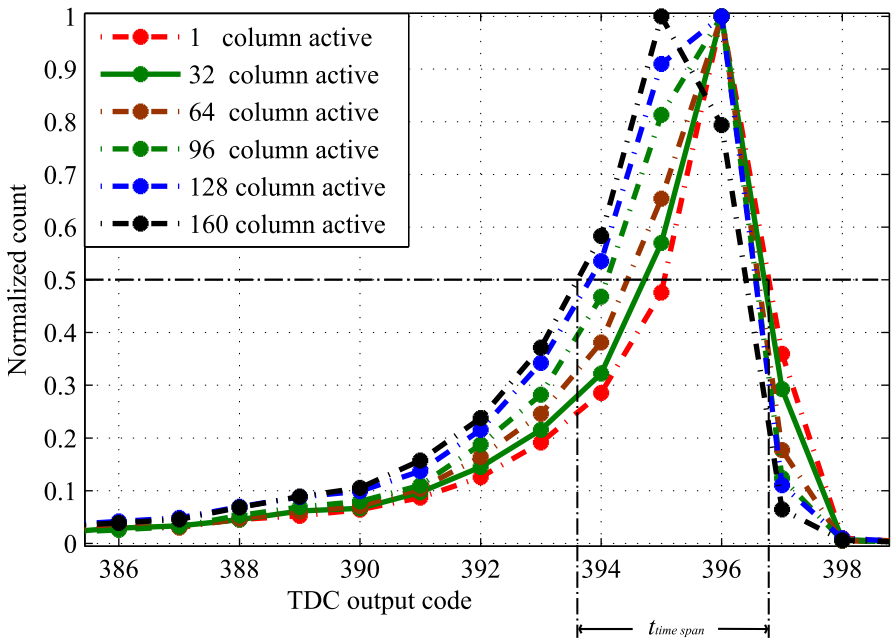

Figure 5.22: TDC scaling time-span measurement technique

To appreciate the effectiveness of the analysis technique introduced earlier, a comparative study is carried out between the *TDC scaling jitter-optical spike location measurement technique* and the *TDC scaling time-span measurement technique*.

TDC scaling jitter-optical spike location measurement technique

Figure 5.23 and Figure 5.24 summarizes the result from the set of experiments carried out to study the scaling effect. It should be noted that the results produced in Figure 5.23 and Figure 5.24 is obtained by considering the data from one column of the pixels. The one column was considered to give a fair comparison between the results obtained by activating 1, 80 and 160 columns.

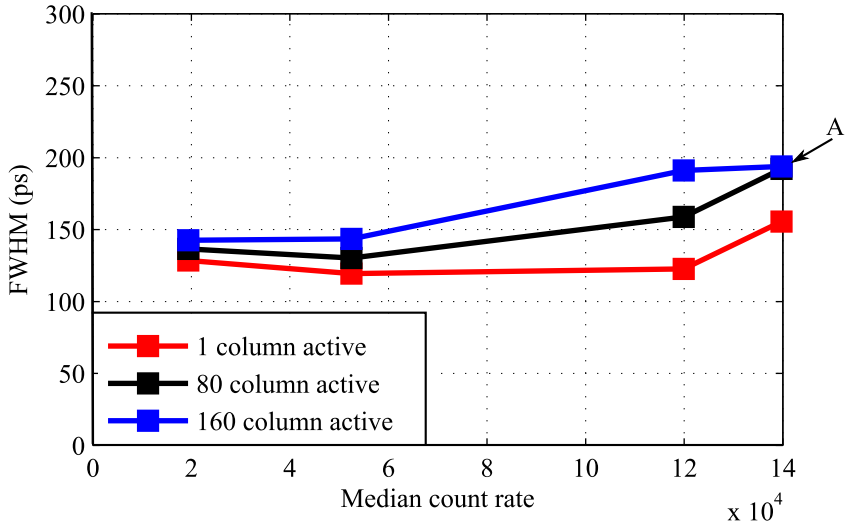

Figure 5.23: TDC scaling jitter-optical spike location measurement technique: Jitter variation

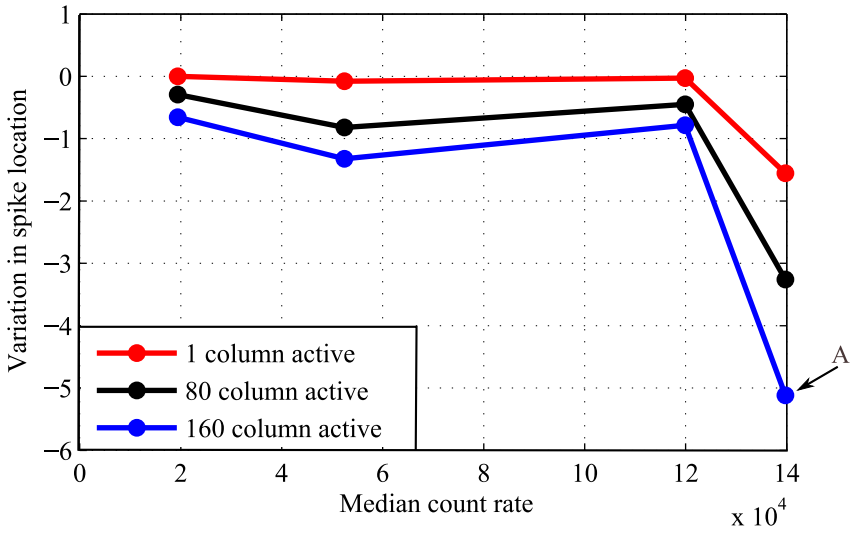

Figure 5.24: TDC scaling jitter-optical spike location measurement technique: Optical spike location variation

From the experimental results produced in Figure 5.23 and Figure 5.24, it can be ascertain that for data point 'A', the FWHM measurement is better than the previous data point. But the variation in the spike location is worse than the earlier data point. This conflicting observation is due to a misinterpretation of the TDC resolution as explained earlier. Hence analyzing the jitter and variation in spike location can mislead us in understanding the TDC scaling effect.

However this technique can be used to quantitatively analyze the TDC scaling

effect by observing first the variation in the location of the spike and then the jitter measurement. If there is a significant variation in the location of the optical spike, then we can comprehend that there is TDC scaling effect. On the other hand, when there is not much significant variation in the location of the optical spike, then we can analyze the jitter variation to understand the TDC scaling effect. Hence this technique can be used to understand the TDC scaling effect quantitatively.

TDC scaling time-span measurement technique

The experimental result produced in Figure 5.23 and Figure 5.24 is re-analyzed using the time span measurement technique introduced earlier. The parameter that was used to analyze the TDC scaling effect is the number of enabled columns. In this analysis the optimal scenario is when 1 column of pixels are enabled and the worst case scenario being 160 columns enabled. The result of the analysis is shown in Figure 5.25.

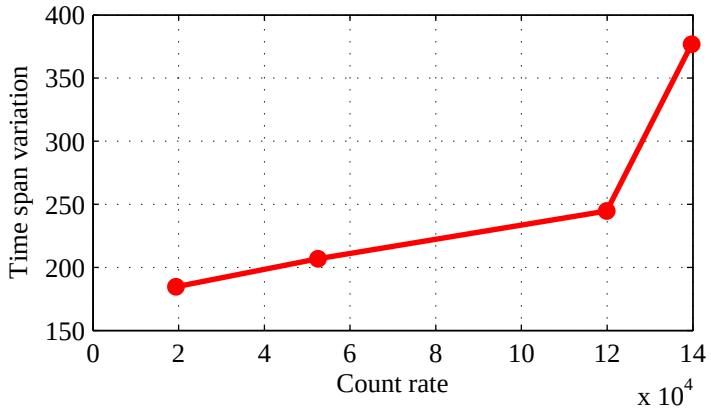

Figure 5.25: Without PLL: Using TDC scaling time-span measurement technique

Figure 5.25 clearly shows that there is a quite a significant variation introduced by TDC scaling. Since TDC scaling time-span measurement technique captures even the slightest variation introduced in the optical spike location and its jitter, this analysis method can be reliably used to study the TDC scaling effect.

Activating PVT control loop

The scaling effect that we saw in the previous sub section was due to a very small variation in the supply voltage. In MF128 a phase locked loop (PLL) based process, voltage and temperature (PVT) control system is implemented on-chip. Therefore by activating the PVT control system it should be possible to control the effect of the power supply variation on the TDC. To understand the effectiveness of the PVT control system, a set of experiments were carried out by varying the number of enabled columns under different light intensities. The summary of the experimental results analyzed using the *TDC scaling time-span measurement technique* is shown in Figure 5.27, along with experimental result of one pixel in Figure 5.26. From the experimental results it can be comprehended that the PVT control loop indeed stabilized the variations to a good extent.

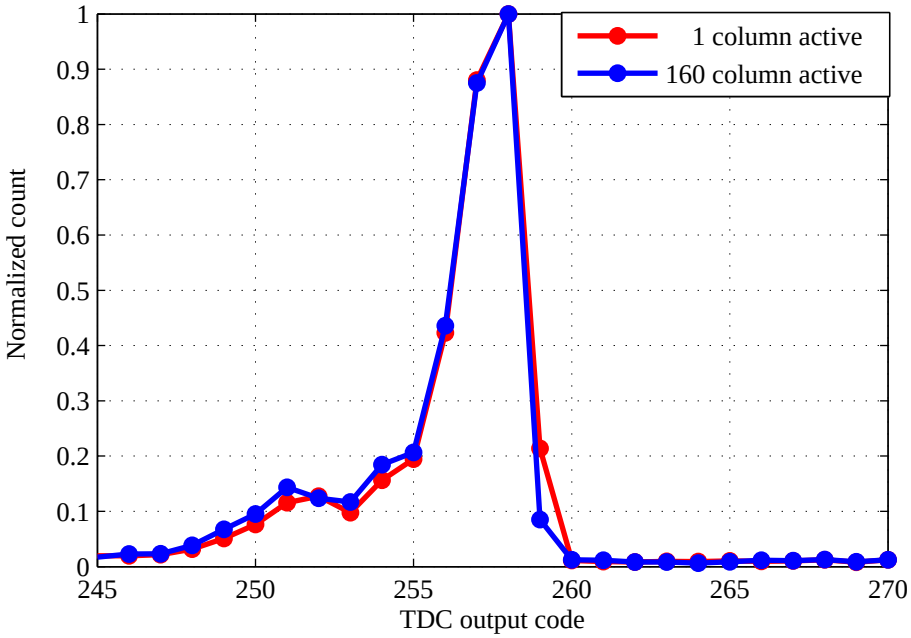

Figure 5.26: With PLL: Measurement result of one pixel with photon count rate being 17 kHz

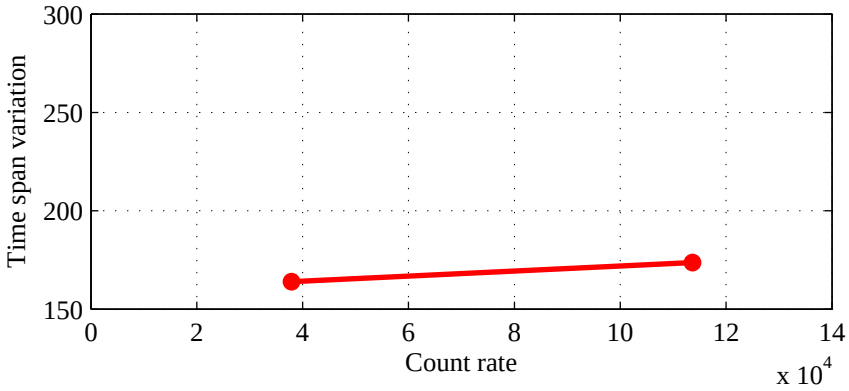

Figure 5.27: With PLL: Using TDC scaling time-span measurement technique

Timing measurement: Uniformity across the array

Figure 5.28 and Figure 5.29 show the temporal position of the optical spike and its jitter distribution across the array. These results were obtained by activating all the pixels, when the median photon count rate was about 6 kHz. It should be noted that this experiment was carried out using the blue laser (405 m), with PVT enabled.

Figure 5.28 shows a gradual variation in the temporal position of the optical spike toward the center of the array. This variation can be correlated to the propagation delay of the STOP signal entering the array from either ends of the imager.

From Figure 5.29, it is possible to understand that the variation in the FWHM

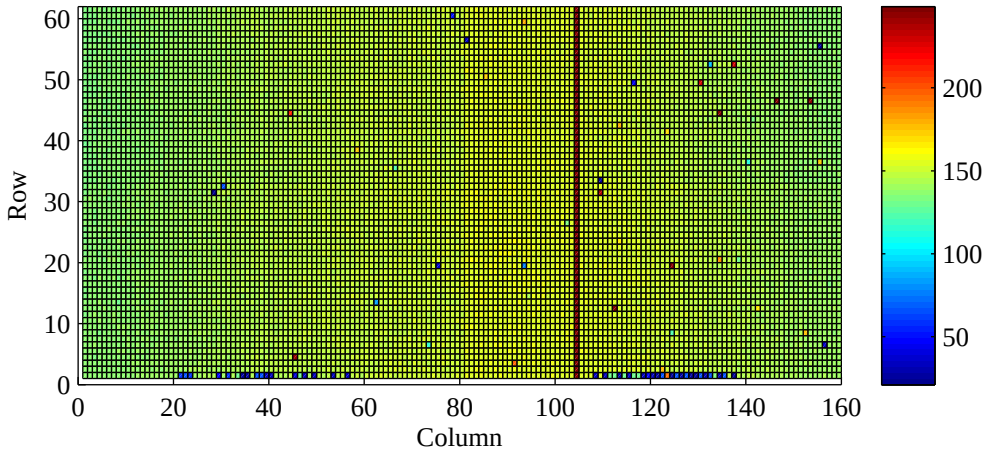

Figure 5.28: Temporal position of the optical spike in terms of TDC output code when the TDC resolution is about 90 ps

measurement across the array is negligible. However, there are few pixels scattered across the array showing very high FWHM value. These pixels correspond to the high DCR pixels. Since the photon count rate in this experiment is very less, the noise floor introduced by the DCR and the background noise increases to a level such that FWHM cannot be determined.

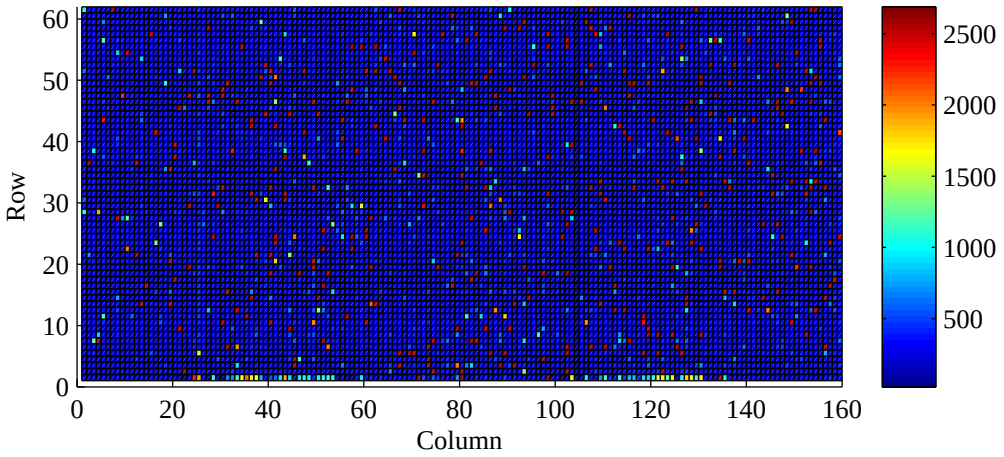

Figure 5.29: FWHM distribution

5.8 Fluorescence Life Time Imaging Microscopy(FLIM)

The MF128 image sensor capability of resolving the time-of-arrival of individual photons was tested and characterized in previous sections. This section focuses on exploiting one of the potential applications of the time-resolved imager ie., Fluorescence Life Time Imaging Microscopy(FLIM) application [30] . In FLIM a biological sample stained with

one or more fluorescent dye is observed under the microscope, where the fluorescent property of the dye is analyzed for its lifetime. The lifetime of the fluorescent dye depends on the biological specimen and its environment [1]. Hence by analyzing the variation in the lifetime of the fluorescent dye biologist can study the properties of the specimen [31, 32, 33]. The lifetime of the fluorescent dye can follow either first order or higher order exponential decay, depending on the specimen under study.

The lifetime of the fluorescent material can be measured from the histogram formed by observing the arrival time of the photons in TCSPC mode of operation. In FLIM, the observed photons are emitted from the fluorescent dye, by exciting the specimen with a pulsed laser source. In MF128 since every pixel has its own photon detector and a TDC, it is possible to simultaneously monitor the fluorescent lifetime in all the pixels.

5.8.1 Biological sample

In this experiment a Bisaccate Pine pollen grain (Carolina Biological Supply Company, NC, USA) was used. The sample was stained using a 2-dye system, Harris hematoxylin and phloxinein, with different lifetimes. Figure 5.30 shows the structure of the pollen grain.

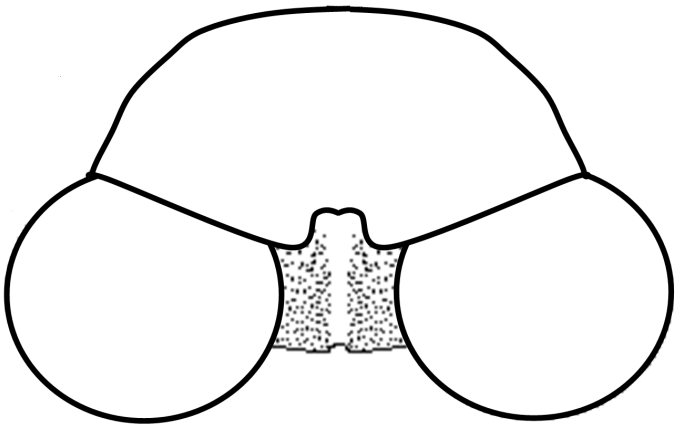

Figure 5.30: Pollen grain structure [34]

5.8.2 Optical setup

For FLIM the MF128 was mounted on a microscope (BX51IW, Olympus, Japan). The blue laser source was used at an average optical power of 2mW. The biological sample was illuminated through a microscope objective (20x, 0.45 NA, MPlanFL N, Olympus, Japan), via a standard dichroic beam splitter. The reflected beam was redirected to the sensor via the beam splitter and filters. Figure 5.31 shows the optical setup used in the experiment.

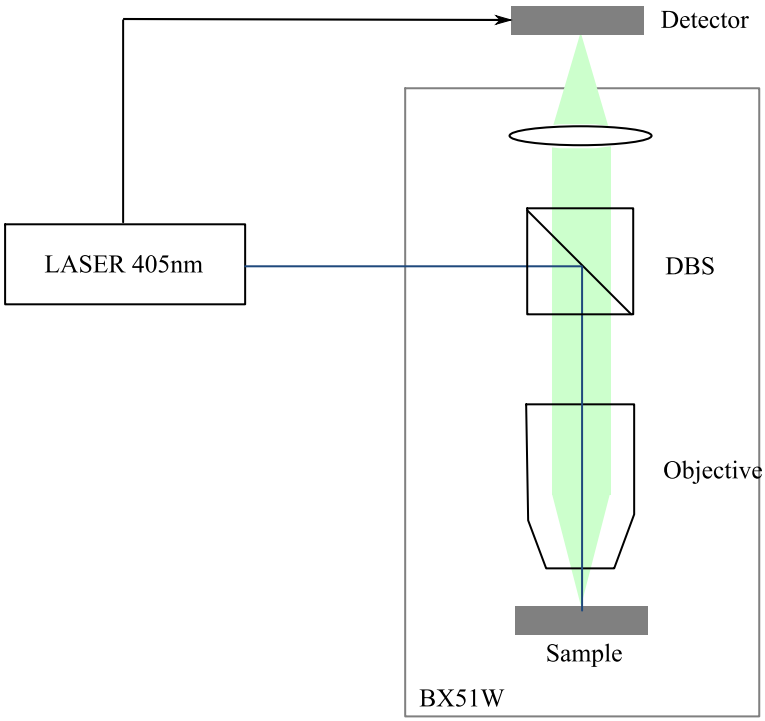

Figure 5.31: Optical setup [35]

5.8.3 MF128 configuration

For FLIM experiment the MF128 is configured in TCSPC mode. In this configuration a laser is used as master providing the STOP clock to the MF128 chip. It should be noted that the STOP clock generated by the laser source is in-sync with the light pulse emitted by the laser running at 40 MHz.

5.8.4 Data analysis

As stated earlier for FLIM, the lifetime of the fluorescent material needs to be determined. Histogram obtained from the time-of-arrival measurement needs to be analyzed for the lifetime. Since the fluorescent dye used in this experiment follows a double exponential decay, the histogram data is fitted to a double exponential decay function. The fluorescence lifetime (τ_m) is obtained by evaluating the weighted average of the decay time from different exponential components (τ_i) [36].

$$\tau_m = \sum_{i=1}^{N} a_i \tau_i / \sum_{i=1}^{N} a_i$$

The exponential curve fitting and lifetime calculation was performed after removing the noise floor introduced by the DCR of the pixel and the background noise. The intensity image is obtained by evaluating the area under the histogram curve.

5.8.5 Experimental results

To analyze the TDC scaling effect, an experiment was carried out in TUPC mode to understand the available light intensity. From the experimental results produced in Figure 5.32, it can be asertain that the average count rate across the array is 2.2x10^4 Hz.

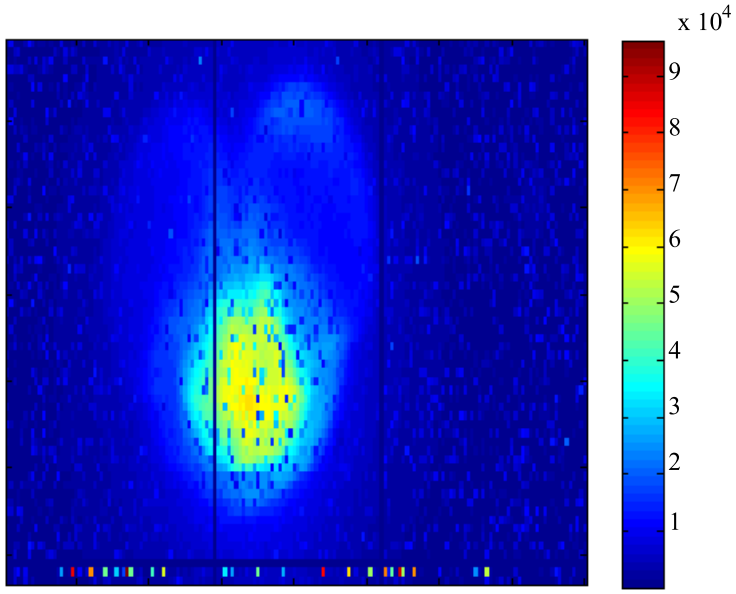

Figure 5.32: Count rate

By comparing the observed count rate with the TDC scaling results in Figure 5.25, we can infer that for the observed light intensity the TDC scaling effect is negligible. Hence the FLIM experiment was carried out by enabling all the pixels (160x64 pixels) simultaneously.

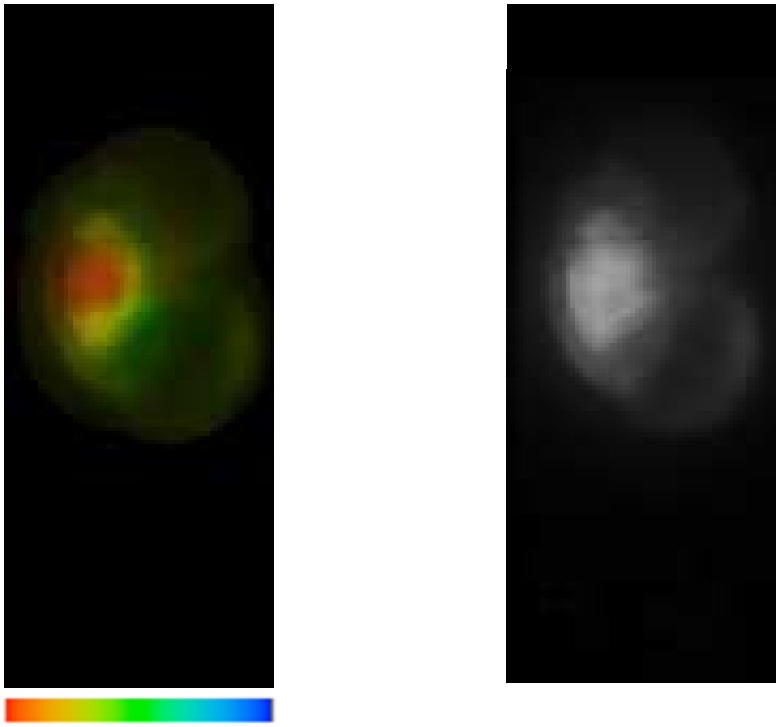

Figure 5.33: FLIM: Bisaccate Pine pollen grain

Figure 5.33 shows the resulting intensity and FLIM images and scales, respectively. The FLIM color code corresponds to a lifetime estimated using a double exponential fit on the data obtained from 300,000 measurements per pixel. It should be noted that in Figure 5.33 high DCR pixels are removed through median filtering.

5.9 Summary

- TDC was tested successfully in various operating modes.
- An unexpected spike in the code density test was observed: spike modulation technique and spike diffusion technique were discussed as a solution.
- Comparing the drawback of the spike modulation technique and spike diffusion technique, it was found that the spike diffusion technique is better than the spike modulation technique.
- Through experiments it was found that the TDC reset signal is not stable with increasing circuit activities.
- To study the scaling of active TDCs, a TDC scaling time-span measurement technique was proposed
- The TDC performance was found to degrade with light intensity and enabled

pixels. However PVT control loop compensates for the TDC performance degradation.

- FLIM experiment was performed using MF128 and the developed data acquisition system.

6 Conclusion

6.1 Summary

In the course of this thesis a data acquisition platform was developed for the MF128 time resolved imager. The backbone architecture for this data acquisition system was ported from the earlier version of the imager, after careful study. The developed platform in addition to the data acquisition is also capable of configuring and controlling the MF128 imager. The control, configuration and data acquisition for the MF128 was achieved by partitioning the work load between the software and the firmware. The work load partitioning was implemented such that the software was designed to interpret the users commands and the firmware was designed to execute the softwares instructions. To reduce the data transfer rate from the FPGA to computer, a column based event-driven technique was realized. This technique finds its application in photon-starved applications where the number of SPAD trigger events observed for a frame is reduced. Further to speed up the data acquisition in performing the code density test simultaneously for all the TDCs, a time interleaved sampling on data generated by the high DCR pixel was implemented.

In the second phase the developed data acquisition system was used to test and characterize the MF128 imager. The test methodologies to test the various basic functional modules of the imager were proposed, implemented and tested. These test methodologies were designed such that the input test vector and its response can be controlled and monitored using the developed data acquisition system. Hence, by scripting the developed test functions in software the test process of the imager can be automated.

Further, in this thesis during the characterization phase the dark count rate of the pixel was monitored and reported at various temperatures and excess bias voltages. In this characterization process around thirty percent of the pixels were tagged as noisy pixels (>200 Hz). Later, while evaluating the breakdown voltage of the SPAD we found that the noisy pixels have a different breakdown voltage. Hence, it was inferred that the cause for the high DCR pixel can be due to the variation in the chip manufacturing process.

Furthermore, the unexpected spike observed while performing the code density test was studied in this thesis. Through this study the reason for the occurrence of the unexpected spike was identified. Further, to remove the unexpected spike from the region of interest two solutions were discussed viz. *spike modulation technique* and the *spike diffusion technique*. An analysis was carried out to compare the pros and cons of these two techniques. From the analysis it was found that the *spike diffusion technique is better* than the spike modulation technique.

The MF128 is one of the largest on-pixel time resolved imager, with an array of about 160x128 TDCs capable of working in parallel. Hence in this thesis a study was

carried out to understand the behavior of the TDC with the number of active pixels. To emulate the real time scenario, the experiments were carried out under various light intensities and by varying the number of enabled pixels. From the experimental results it was inferred that the variation introduced in the TDC performance due to the scaling of active pixels cannot be captured as a FWHM variation. Hence a technique called as *TDC scaling time-span measurement technique* was introduced in this thesis.

Finally, the MF128 imager and the developed data acquisition system were used to perform Fluorescence Life Time Imaging (FLIM) experiment. In this experiment a pine pollen grain was observed. The results of the experiments carried out to characterize the MF128 imager is summarized in Table 6.1.

	Parameter	Min.	Typ.	Max.	Unit
Pixel	Median DCR @ Ve = 0.62 V		50		Hz
	FWHM jitter (637nm)		140		ps
	1 sigma jitter non-uniformity		27		ps
	TDC meaurement range		55		ns
	TDC resolution (LSB)		55		ps
	TDC DNL/INL		0.3 / 2.5		LSB
	Fill factor		1		%
System	Clock frequency		16	32	MHz
	Chip size		11.0x12.3		mm2
	Total I/O bandwidth		51.2		Gbps
	Power dissipation		550		mW
	CMOS Process		130nm		-
FLIM experiment	Frame rate		25	50	kfps
	Laser source average power		2		mW
	Target area		125x50		m^2

Table 6.1: MF128 Imager performance summary [1]

6.2 Future work

The future work can be broadly classified in the following directions.

1. The data compression techniques such as IEM module and event driven serializer available on-chip can be tested and characterized.

2. Application specific data compression techniques can be incorporated in the data acquisition system. For example in FLIM application histograms can be created in FPGA [37], so that the FPGA-PC communication bottle neck can be circumvented.

3. The data acquisition system can be extended to simultaneously acquire data from two halves of the chip using the two FPGAs.

I2C Register map

A

Index	Bit	Name	Description
100d	(7:0)	IEMFIRST(7:0)	IEM window position
101d	(1:0)	IEMFIRST(9:8)	IEM window position
	(5:2)	IEMWIDTH(3:0)	IEM window width
	(7:6)	unused	
102d	(7:0)	IEMLAST(7:0)	IEM window position
103d	(1:0)	IEMLAST(9:8)	IEM window position
	2	COARSEMODE	IEM on
	3	RAWMODE	IEM off
	4	COMPRESSION	New serialiser enable signal
			Use this to switch compression on/off
	(7:5)	unused	
104d	0	FORCE_COLEN_HIGH_N	Force signals for COLENs
	1	FORCE_COLEN_LOW_N	Force signals for COLENs
	2	FORCE_ROWEN_HIGH_N	Force signals for ROWENs
	3	FORCE_ROWEN_LOW_N	Force signals for ROWENs
	(7:4)	unused	
105d	(7:0)	unused	
106d	(7:0)	unused	
107d	0	PLLLOCK	PLL lock state monitoring
	(7:1)	unused	
108d	0	MODETCSPC	0 – photon counting
			1- TCSPC
	1	STARTSRC	Selects TDC start signal source
			0=SPADs
			1=TESTSTART
	2	STOPSRC	Selects TDC stop signal source
			0=OPTCLK
			1=EXTSTOP
	3	PLLSRC	Selects device PLL source clock
			0=OPTCLK
			1=EXTCLK
	4	YDECBP	Allows Y decoder to be bypassed
			0=Y decoder operating
			1=ROWSEL activated

Index	Bit	Name	Description
	5	SERBP	Allows serialisers to be bypassed
			0=serialisers operating
			1=column LSBs connected to op pads
	6	SERGATINGBP	Serializer gating
			0=Gated when not required
			1=Permanently enabled
	7	SOFTRESETN	Active low soft reset
			0=System in soft reset
			1=System operating
109d	0	COUNTENABLE	Enable for TDC coarse counter
	1	MODEMUTEON	TDC SPAD mute signal
	2	SEROUTALIGN	Serialiser output alignment
			0=photon counting mode
			1=time correlated mode
	(7:3)	unused	
110d	0	PLLENABLE	PLL enable
	(2:1)	DIVCTRL (1:0)	PLL input clock divider
			00 = No division
			01 = divide by 2
			10 = divide by 4
			11 = divide by 8
	(4:3)	PDIV1 (1:0)	PLL P1 divider ratio.
	(6:5)	PDIV2 (1:0)	PLL P2 divider ratio.
	7	SSCG_CONTROL	PLL SSC enable.
111d	(7:0)	NDIV (7:0)	PLL N divider ratio

Table A.1: MF128: I2C Register Map [12]

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List of Publications

[1] C. Veerappan, J. Richardson, R. Walker, D.U. Li, M.W. Fishburn, Y. Maruyama, D. Stoppa, F. Borghetti, M. Gerbach, R.K. Henderson, and E. Charbon "A 160x128 Single-Photon Image Sensor with on-pixel 55ps 10bit Time-to-Digital Converter," in *IEEE International Solid-State Circuits Conference*, 2011,