# Energy-efficient integrated circuits for piezoelectric energy harvesting

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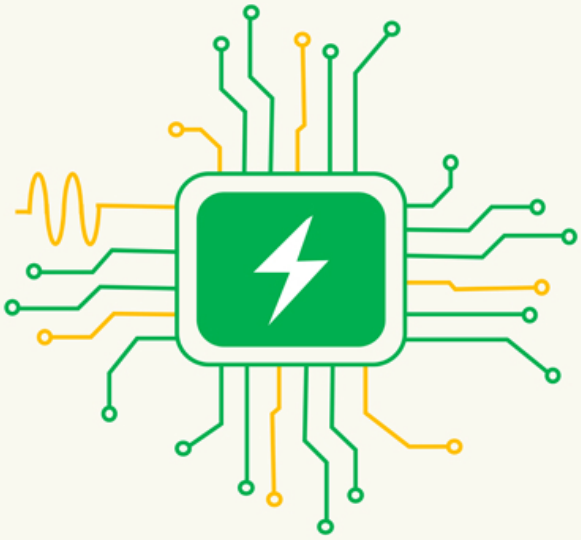
# ENERGY-EFFICIENT INTEGRATED CIRCUITS FOR PIEZOELECTRIC ENERGY HARVESTING



Xinling YUE

# Propositions

accompanying the dissertation

**Energy-Efficient Integrated Circuits for Piezoelectric Energy Harvesting**

by

**Xinling YUE**

1. Rather than being a free lunch, energy harvesting is often a very expensive one (*This proposition pertains to this dissertation*).
2. The duty-cycle-based MPPT technique proposed in this thesis greatly simplifies the design of piezoelectric energy harvesters (*This proposition pertains to this dissertation*).
3. The output power of an energy harvesting system is mainly limited by its transducers and not by its interface electronics (*This proposition pertains to this dissertation*).
4. Messaging apps like WhatsApp and WeChat improve communication efficiency but distance people from one another.
5. By amplifying misinformation and polarization, social media has done public discourse more harm than good.
6. Reviewers of journals and conferences should be paid for the time and expertise they invest in the review process.
7. Free will is fast becoming an illusion as social media algorithms increasingly determine human behaviour.
8. Artificial intelligence will exacerbate social inequality.
9. Collaboration with industry is essential for doing an impactful PhD in engineering.
10. Technology makes people's lives more convenient, but not always happier.

These propositions are regarded as opposable and defendable and have been approved as such by the promotor, prof. dr. K.A.A. Makinwa and copromotor dr. S. Du.

# ENERGY-EFFICIENT INTEGRATED CIRCUITS FOR PIEZOELECTRIC ENERGY HARVESTING

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology

by the authority of the Rector Magnificus prof.dr.ir. T.H.J.J. van der Hagen
Chair of the Board for Doctorates
to be defended publicly on
Thursday 4 September 2025 at 17:30 o'clock

by

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This dissertation has been approved by the promotors.

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Dr. S. Du, Delft University of Technology, copromotor

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Dr. F. Tavernier, KU Leuven

Dr. A. Cathelin, STMicroelectronics

Prof.dr. G.Q. Zhang, Delft University of Technology, reserve member

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# Chapter 1 Introduction

## 1.1 Motivation

The Internet of Things (IoT) has permeated almost every part of our daily lives, fundamentally altering human society. One of its main drivers has been the development of wireless sensors, which can be used in wireless networks, thus providing real-time information about the physical world to distributed and increasingly intelligent systems. As shown in Fig. 1-1, wireless sensor networks have become ubiquitous and are used in smart homes, wearables, healthcare, infrastructures, industrial applications, and smart farming. In smart homes, for instance, wireless sensors monitor parameters such as temperature, humidity, air quality, sound, and light intensity, ensuring optimal living conditions. In the healthcare sector, wireless sensors have revolutionized patient care by facilitating continuous monitoring, delivering real-time health data to doctors and nurses, and enabling timely and informed medical interventions. In industrial automation, wireless sensors are used to monitor the condition of vital equipment and environmental parameters, such as pressure, liquid level, flow rate, and vibration, thus enhancing operational efficiency and safety.

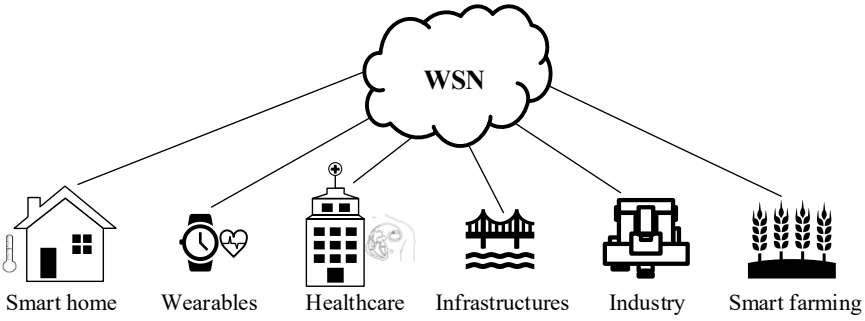


Fig. 1-1. Wireless sensor node (WSN) applications.

Wireless sensors are often powered by electrochemical batteries, whose reliability and storage capacity then determine the sensor's operational life. For example, the LIS3DH, a low-power 3-axis accelerometer intended for IoT applications, dissipates 28μW during normal operation [1-1]. This results in an operational life of about 4

months when it is powered by a 35mAh CR1220 coin-cell battery. This can obviously be increased by using a larger battery or by replacing/recharging it more frequently. However, a large battery is undesirable in portable wireless sensors, while battery replacement is impractical or costly in applications such as implantable medical devices or autonomous sensors in remote areas. As a result, there is a need for low-cost, sustainable, and environmentally friendly alternatives to traditional batteries.

## 1.2 Energy Harvesters

Energy harvesters extract energy from their environment and convert it into electrical energy for use in other electronic devices. As such, they are a promising alternative to the use of batteries in wireless sensors. Table 1-1 lists common environmental energy sources, such as heat, light, electromagnetic waves, and vibration, which are suitable for powering electronic devices.

Thermoelectric generators (TEGs) are based on the Seebeck effect, which refers to the ability of thermocouples to generate a voltage from a temperature difference [1-2][1-3][1-4]. As shown in Table 1-1, TEGs are particularly effective at harvesting industrial waste heat, which can have power densities as large as $3\mu W/K^2/cm^2$. In contrast, the power densities associated with harvesting human body heat are much lower, in the order of $0.03\mu W/K^2/cm^2$. TEGs do not have moving parts, ensuring high reliability and minimal maintenance requirements. However, they require large and continuously available temperature gradients to operate effectively and are thus not well-suited for use in infrastructure monitoring or smart agriculture.

Table 1-1. Different types of energy harvesting systems.

| Harvester | | Power Density | Scenario | Ref. |
|---|---|---|---|---|
|  | Thermal | Conventional: 3 μW/K$^2$/cm$^2$ | Industrial heat | [1-19] |
| | | CMOS Compatible: 0.026 μW/ K$^2$/cm$^2$ | Human body | |
|  | Solar | Outdoor: 15 mW/cm$^2$ | Rooftop (sunny days) | [1-20] |
| | | Indoor: <10 μW/cm$^2$ | Light | |
|  | RF | GSM Network: 0.1 μW/cm$^2$ | Mobile phone | [1-21] |
| | | Wi-Fi Network: 0.01 μW/cm$^2$ | Wi-Fi, radar, RFID | |
|  | Vibration | Electromagnetic: 4 μW/cm$^2$ | Motor, transformer | [1-22] |
| | | Piezoelectric: 500 μW/cm$^2$ | Road, human motion | [1-23] |

Photovoltaic (PV) harvesters use sunlight or artificial lighting to create electricity via the photovoltaic effect [1-5] [1-6]. Thanks to their high energy efficiency, mature fabrication process, and reliability without employing any moving parts, they have been dominantly employed worldwide in the past decade for renewable energy generation. As shown in Table 1-1, they can achieve power densities as high as 15mW/cm² in direct sunlight, making them well-suited for use in autonomous systems. However, their power density drops dramatically (to less than 10μW/cm$^2$) under indoor lighting conditions.

Radio frequency (RF) energy harvesters convert electromagnetic waves into electrical power [1-7] [1-8] [1-9] [1-10]. Since RF signals are ubiquitous in urban environments due to the presence of radio, television, and cellular networks, RF energy harvesters are well-suited for use in smart homes. Unfortunately, the low energy density of RF signals (typically less than 0.1μW/cm$^2$) limits their use in industrial and healthcare applications, as well as in remote rural or mountainous settings.

Last, but not least, vibrational energy harvesting (VEH) involves the conversion of kinetic energy, in the form of mechanical motion or vibration, into electrical energy. Compared to other energy sources, kinetic energy, can be readily harvested: from door handles and light switches, from human body motion, from building/bridge/tunnel vibrations, from rotating machines, and from wind or wave motion. Furthermore, vibra-

tion energy harvesting offers advantages such as low maintenance costs, simple construction, and often, continuous output power. Therefore, the main focus of this thesis will be on the design of vibration energy harvesters.

## 1.3 Vibrational Energy Harvesters

Vibrational energy can be harvested by electromagnetic, electrostatic, triboelectric, or piezoelectric harvesters. Electromagnetic generators are based on the principle of electromagnetic induction [1-11][1-12]. Their main components are a moving magnet and/or coil. Mechanical force changes the position of the magnet or coil, changing the magnetic flux through the coil and generating an induced current. Electromagnetic generators are widely used in large-scale power generation scenarios, such as motors and transformers in industries, which are not suitable for powering wireless sensors.

Electrostatic energy harvesters are devices that convert mechanical energy into electrical energy using variable capacitors. The basic principle is that, under either the charge-constrained or voltage-constrained condition, mechanical motion (e.g., vibration or displacement) changes the capacitance of the device, thereby altering the stored electrostatic energy and inducing current flow in the external circuit [1-13][1-14]. However, this approach typically requires an external bias to enable energy conversion. A special form of electrostatic energy harvesting is electret-based electrostatic energy harvesting, in which a variable-capacitance structure incorporates an electret material with an intrinsic electric field, thus eliminating the need for an external bias and enabling self-startup [1-15]. Nevertheless, electret-based devices still face limitations in powering wireless sensors, including low power density, high output impedance, strong dependence on precise mechanical gaps and packaging integrity, and possible charge decay of the electret under high-humidity or high-temperature conditions [1-13][1-15][1-16].

Triboelectric nanogenerators (TENGs) are an energy harvesting technology based on the triboelectric effect and electrostatic induction, in which two materials with dif-

ferent electronegativities undergo periodic contact–separation or relative sliding, leading to electron transfer and charge separation, and subsequently generating electrical output through an external circuit [1-17][1-18]. TENGs feature high output voltage, mechanical flexibility, and versatile material/structural design, and in recent years have been widely explored in areas such as wearable electronics, environmental monitoring, and infrastructure health monitoring [1-17]. However, issues such as surface wear and lifetime degradation caused by contact–sliding interfaces, as well as charge leakage under humid environmental conditions, remain significant challenges [1-19][1-20][1-21]. Moreover, the commercialization of TENG front-end devices is still limited, with no large-scale or standardized products available [1-17]. These factors make current TENG technology unsuitable for providing stable and reliable power to most wireless sensor systems.

Piezoelectric transducers (PTs) are based on the piezoelectric effect [1-22][1-23][1-24][1-25], which refers to the ability of certain crystals or ceramics to generate an electric field when subjected to mechanical pressure [1-34][1-35] or stress [1-35][1-36]. They usually contain a piezoelectric layer sandwiched by two metal layers as electrodes, which offer significant advantages in size, weight, power density ($500\mu W/cm^2$), and cost over other vibrational generators. Moreover, PTs can be made in various shapes, for instance, cantilever beams [1-37] [1-38], flat circular discs [1-39] [1-40], stacked structures [1-41], etc., making them easy to integrate into different devices with simple structures. Piezoelectric devices can also be fabricated in micro-mechanical systems (MEMS) technology to achieve high-integration levels with CMOS power-conditioning circuits for miniaturization [1-48]. Hence, PTs are well-suited for use in miniature low-power vibrational energy harvesting systems. However, integrating them into wireless sensors requires efficient interface circuits, as will be discussed in the next section.

## 1.4 Interface Circuits for Piezoelectric Energy Harvesting

### 1.4.1 A Basic PT Interface Circuit

Piezoelectric transducers (PTs) produce AC current in response to mechanical changes and thus can be modelled by an AC current source ($I_P$) connected in parallel with a capacitor ($C_P$). An interface circuit is then required to convert this AC signal into the stable DC supply voltage required by most electronic systems.

The basic block diagram of a PT interface circuit is shown in Fig. 1-2. The PT's AC output voltage is first converted into a DC voltage $V_{REC}$ by a rectifier and then stored on a capacitor $C_{REC}$. However, the magnitude of $V_{REC}$ will not be stable, as it depends on the amount of energy harvested by the PT. Therefore, a DC-DC regulator is required to generate a stable output voltage $V_{OUT}$. It does this by controlling the ON/OFF time or switching frequency of a number of switching elements connected between $C_{REC}$ and $C_{OUT}$, which, in turn, regulate the energy transfer between $C_{REC}$ and an output capacitor ($C_{OUT}$).

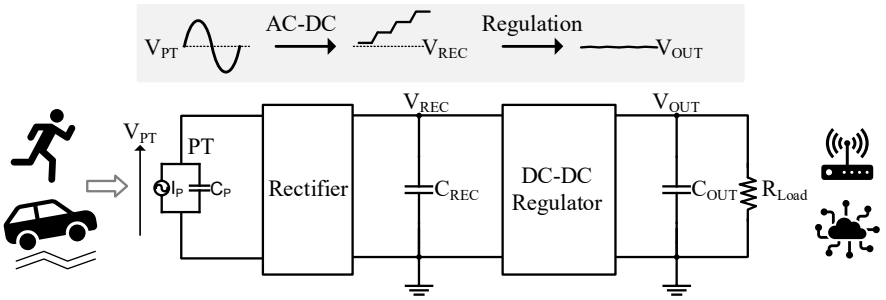


Fig. 1-2. A basic interface circuit topology of a piezoelectric energy harvesting system.

### 1.4.2 Rectifier Efficiency

A key metric of a PEH is its power delivery efficiency, which, in turn, depends on the efficiency of each block in Fig. 1-2. The efficiency of modern DC-DC regulators

is typically quite high, above 90% [1-12]. However, the efficiency of the rectifier is often much lower, and thus needs to be improved.

The efficiency of a rectifier is related to its output voltage ($V_{REC}$). When $V_{REC}$ is low, the output power is low since the output current will typically also be low. Conversely, when $V_{REC}$ is high due to light loading, or in other words, when the output current is again low, the output power is also low. Fig. 1-3 shows the output power of a typical rectifier as a function of $V_{REC}$ [1-22][1-23][1-24]. As $V_{REC}$ increases, the output power initially increases, peaks, and then decreases. The point at which the rectifier's output power peaks is called the maximum power point (MPP). To ensure effective power conversion, the ratio of the rectifier's output power to the power value at the MPP should be in excess of 90% [1-44][1-45].

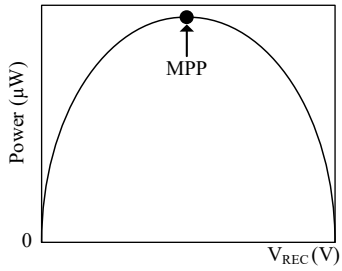


Fig. 1-3. Rectifier's output power over rectifier's output voltage ($V_{REC}$).

### 1.4.3 The Maximum Power Point Tracking Technique

To ensure that a rectifier's output power is always close to its MPP, so-called maximum power point tracking (MPPT) techniques are used. As shown in Fig. 1-4, this requires additional circuit blocks: an MPP monitor and an additional DC-DC converter. The input energy from the source is first harvested by the rectifier; therefore, the MPP monitor is connected to the rectifier to identify its MPP. The DC-DC converter then maintains the output voltage at a certain level. They work together to maintain the output of the rectifier at the MPP.

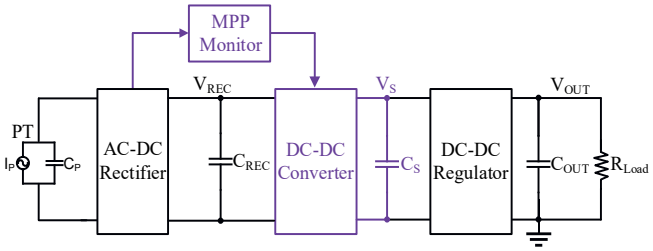


Fig. 1-4. A maximum power point tracking (MPPT) technique in the PEH system.

The interaction between the MPP monitor and DC-DC converter is illustrated in Fig. 1-5. If the MPP monitor detects that the rectifier's output power is below the MPP, the DC-DC converter is turned off. As a result, $V_{REC}$ increases due to the supply of charge from the PT, causing the rectifier's output power to approach the MPP. Once the monitor detects that the output of the rectifier has reached the MPP, the DC-DC converter is activated. This transfers energy from $C_{REC}$ to the storage capacitor ($C_S$), thus raising the storage voltage ($V_S$) and simultaneously decreasing $V_{REC}$. In this way, the interaction between the MPP monitor and the DC-DC converter ensures that the rectifier's output power remains close to the MPP.

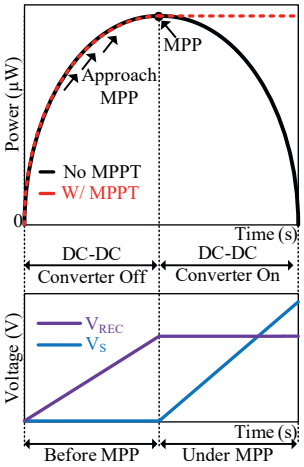


Fig. 1-5. Plots of rectifier's output power w/ and w/o MPPT (top); $V_{REC}$ and $V_S$ under MPPT (bottom).

### 1.4.4 Challenges of PT Interface Circuits

This section discusses the design challenges associated with the two main blocks of a PT interface circuit, the rectifier and the MPP tracker (MPPT). It also analyses the energy losses caused by cascading the various blocks of the system architecture shown in Fig. 1-4.

#### 1.4.4.1 Challenge 1: Size and Efficiency of Rectifiers

The rectifiers used in PEH systems can be categorized into passive and active types, each with their own pros and cons.

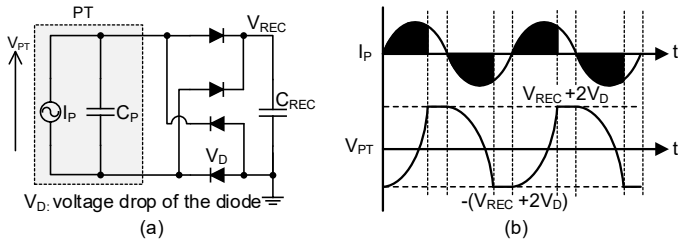


Fig. 1-6. A full-bridge rectifier (a) and its waveform (b).

Passive rectifiers generally employ a number of diodes. The most common type is the full-bridge rectifier (FBR). Fig. 1-6 shows the combination of an FBR and a PT, together with the PT current, $I_P$ and the voltage across its capacitance $C_P$ ($V_{PT}$). $V_{REC}$ is the voltage across the rectifier capacitor ($C_{REC}$), and $V_D$ is the voltage drop across a diode. When changes its polarity, the polarity of $V_{PT}$ flips, and over the next half vibrational cycle, it increases until it reaches the threshold voltage ($\pm(V_{REC}+2V_D)$) necessary to turn on one pair of diodes. Unfortunately, reaching this voltage uses up some of the charge provided by the PT and thus limits the amount of charge transferred to $C_{REC}$. As a result, the power delivery efficiency of the combination of a PT and a conventional FBR is quite limited [1-46].

To achieve higher power delivery efficiency, active bias-flip rectifiers have been developed, which modify the process of charge transfer in an FBR [1-22] [1-23][1-

24]. In a synchronized switch harvesting on inductor (SSHI) rectifier, a switched inductor is added before the FBR to rapidly flip the voltage across $C_P$. Fig. 1-7 shows an SSHI rectifier (a), its waveforms (b), and a plot of its output power (c). When $I_P$ = 0, the inductor is connected in parallel with $C_P$ via switches Φ. The inductor and $C_P$ then form a resonant loop, in which charge goes into the inductor and then returns to $C_P$ to flip the polarity of $V_{PT}$. When $V_{PT}$ has completely reversed, the switches are turned off. Compared to the operation of a conventional FBR, the presence of the inductor significantly reduces the time required to reverse the polarity of $V_{PT}$, allowing $I_P$ to deliver more charge to the output. In [1-22], the use of an FBR resulted in a maximum output power of 13μW, which increased to 68μW when a bias-flip SSHI rectifier was used, demonstrating a 5× power enhancement.

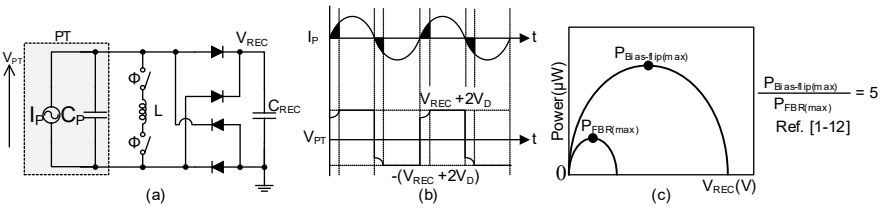


Fig. 1-7. An SSHI rectifier (a), waveforms (b), and output power (c).

Although an SSHI rectifier can generate more output power than an FBR from a given PT, it typically requires a large inductor with values ranging from a few hundred microhenries to several millihenries [1-22][1-48][1-49]. Integrating such an inductor on a chip is impractical, while employing an off-chip inductor leads to system volumes measured in cubic centimeters, which are unsuitable for use in compact wireless sensors, e.g., in bioelectronic sensors intended for in vivo applications. To address this challenge, the design of compact bias-flip rectifiers that do not need large inductors (or capacitors) will be investigated.

### 1.4.4.2 Challenge 2: Sensitivity and Complexity of the MPPT

As discussed in section 1.3.3, a maximum power point tracker (MPPT) identifies the MPP of a rectifier and then maintains its output power at this optimum level. However, swiftly and accurately locating the MPP with simple, low-power circuitry is a major challenge. Currently, two widely used MPPT algorithms are the fractional open-circuit voltage (FOCV) and the perturb and observe (P&O), each with their own advantages and disadvantages.

The FOCV algorithm requires the computation of the optimal rectifier output voltage ($V_{MPP}$) corresponding to the theoretical MPP. It then regulates $V_{REC}$ to match this $V_{MPP}$. As shown in Fig. 1-8, $V_{MPP}$ can be expressed as a function of the PT's open-circuit voltage ($V_{OC}$) and a parameter ($\eta_F$) that depends on the rectifier's characteristics. This relationship, which will be discussed in detail in Chapter 2, is expressed as $V_{MPP} = \frac{V_{OC}}{1-\eta_F}$ [1-50]. Since $V_{MPP}$ depends on $V_{OC}$, implementing the FOCV algorithm requires periodically disconnecting the PT from the rectifier to sample $V_{OC}$ periodically, leading to energy losses [1-51]. Moreover, because $V_{MPP}$ depends on $\eta_F$, and $\eta_F$ is sensitive to the circuit's parasitic resistances and capacitances, additional calibration is required to ensure an accurate estimation of $V_{MPP}$.

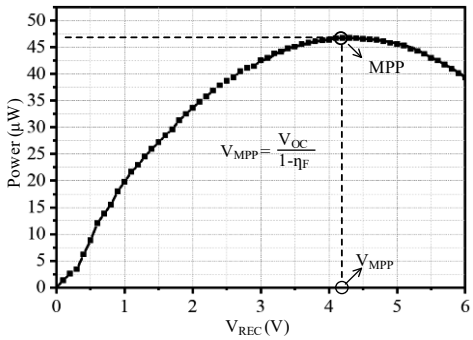

Fig. 1-8. Fractional open-circuit voltage algorithm for MPPT.

The P&O algorithm adjusts the rectified output power in small steps towards the MPP, operating independently of $\eta_F$ and $V_{OC}$. As shown in Fig. 1-9, if the power measured at the current step is higher than that of the previous step, the algorithm continues

advancing to the next step; otherwise, it returns to the previous step. This iterative process continues until the MPP is reached. In a steady state, the algorithm oscillates around the MPP, enabling robust and continuous MPPT.

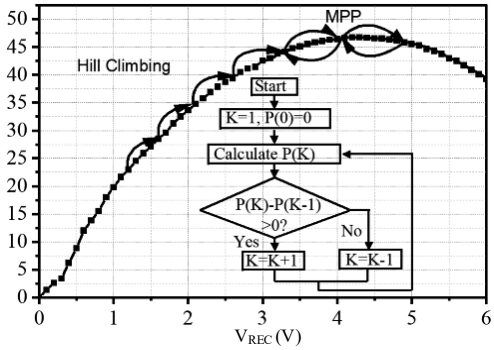


Fig. 1-9. Perturb and observe algorithm for MPPT.

However, measuring the rectified output power in small increments requires complex circuitry. Typically, the rectifier's output voltage is sampled at each incremental step, and a current sensor detects the output current. These values are then digitized by an analog-to-digital converter (ADC) and sent to a microcontroller unit (MCU) to calculate the current output power. Then, the MCU compares this value with the previous one to determine whether the MPP has reached [1-52]. This complex system increases power consumption and cost.

To address the limitations of the FOCV and P&O techniques, this thesis will investigate the development of new MPPT algorithms.

### 1.4.4.3 Challenge 3: Low End-to-End Efficiency

Current PT interface circuits typically have low end-to-end (E2E) efficiency, typically 60%-80%, due to cascaded energy losses [1-48] [1-49] [1-54] [1-55]. As shown in Fig. 1-10, energy from the PT flows through three key blocks before reaching the output capacitor that powers the load: a rectifier, a DC-DC converter for MPPT, and a DC-DC regulation block. Even if each block achieves an efficiency of 90%, the combined losses of the three stages will reduce the E2E efficiency to approximately

72.9%. As previously discussed, however, each block is essential to the system's performance, making it impractical to remove any of them outright. Achieving an E2E efficiency exceeding 90% while preserving the functionality of all blocks remains a significant challenge. To address this, new system architectures will be developed to integrate the required functionality (rectifier, MPPT, and DC-DC regulation) into fewer blocks to eliminate cascaded losses. The goal will be to achieve greater than 90% E2E efficiency, and thus significantly improve the state-of-the-art.

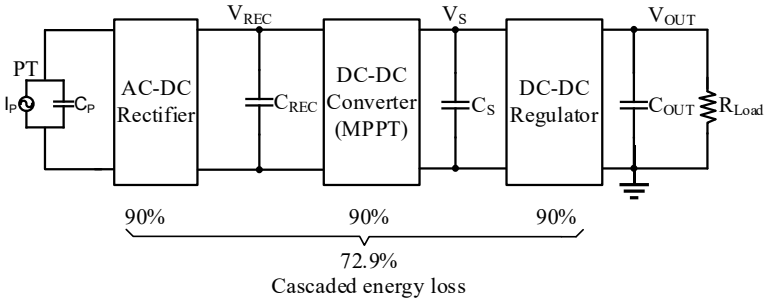


Fig. 1-10. Cascaded energy loss in the interface circuit.

The above-mentioned challenges faced by the rectifiers, MPPT, and E2E efficiency will be separately addressed in this dissertation.

## 1.5 Thesis Organization

The primary goal of this thesis is to design energy-efficient interface circuits for PEH systems. The structure of the thesis is organized as follows:

**Chapter 2**: A comprehensive literature review of integrated circuits for rectifiers and MPPT techniques is presented, highlighting their strengths and weaknesses. This review sets the stage for understanding the current state of the art and the gaps this research aims to fill.

**Chapter 3**: Describes the design of an innovative bias-flip rectifier aimed at minimizing system volume, making it more compact and efficient for powering bio-implantable devices. This development seeks to optimize performance while ensuring suitability for the unique constraints of bio-implant applications.

**Chapter 4:** A novel MPPT technique is presented that streamlines circuit implementation by eliminating the drawbacks of conventional MPPT techniques. A comprehensive theoretical analysis, along with detailed system architecture, operational principles, and measurement results, are provided to support the effectiveness and efficiency of the approach.

**Chapter 5**: This chapter introduces an innovative single-stage rectifier architecture that effectively eliminates cascaded energy losses, achieving an end-to-end efficiency (E2E) of over 90%. This chapter provides an in-depth overview of the system's design, measurement results, and a comprehensive comparative analysis with traditional multi-stage architectures, highlighting the superior performance and efficiency of the proposed solution.

**Chapter 6**: The concluding chapter summarizes the main contributions of the thesis, discusses the broader implications of the research, and proposes potential directions for future work in the field of energy-efficient PEH systems.

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# Chapter 2 Literature Review

## 2.1 Introduction

This chapter reviews existing interface circuits commonly used in piezoelectric energy harvesting (PEH) systems. First, the equivalent circuit model of a piezoelectric transducer (PT) is described, in order to provide a foundational understanding of its electrical behaviour. Next, some common rectifier topologies and maximum power point tracking (MPPT) techniques are presented, which improve energy conversion and delivery efficiency. Finally, prior cascaded system architectures in PEH systems are analyzed.

## 2.2 Equivalent Circuit of a Piezoelectric Transducer

A piezoelectric transducer (PT) converts mechanical energy into electrical energy through the direct piezoelectric effect. As shown in Fig. 2-1, a PT consists of a piezoelectric layer sandwiched between two electrode layers, which are mounted on a substrate. Bending the PT induces mechanical strain in the piezoelectric layer, which is then converted into electric charge.

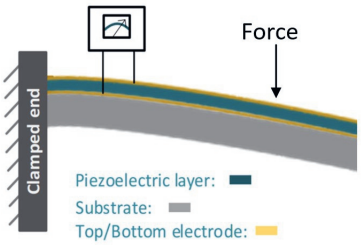


Fig. 2-1. Cantilever beam piezoelectric transducer.

A PT can be modeled as a mechanical system coupled to an electrical system, resulting in the equivalent circuit shown on the left of Fig. 2-2 [2-1][2-2]. In the mechanical system, $\sigma_{IN}$ is the stress induced in the PT by the external forcing function, $F(t)$. $L_M$ represents the mechanical mass. $C_M$ is the effective spring stiffness. $R_M$ denotes the mechanical loss. The output of the mechanical system is denoted by $\sigma_P$, which is the response of the PT to the excitation $\sigma_{IN}$. The transformer represents the

conversion of strain into a current $I_P$, and its turns-ratio $n$ represents the charge constant of the piezoelectric material. In the electrical system, the capacitor $C_P$ represents the plate capacitance of the piezoelectric material, which is the capacitance between the two parallel electrode layers in Fig. 2-1. The governing equation of the overall system can be derived as follows [2-3]:

$$L_M\ddot{u}(t) + R_M\dot{u}(t) + C_M u(t) + nV_{PT}(t) = F(t) \tag{2.1}$$

$$-n\dot{u}(t) + C_P\dot{V_{PT}}(t) = -I_L \tag{2.2}$$

where $u(t)$ and $\dot{u}(t)$ are the displacement and velocity of the PT, respectively. The generated current $I_P$ is calculated as $I_P = n\dot{u}(t)$. $I_L$ is the current flowing to the load. $V_{PT}$ is the voltage across $C_P$.

For a weakly coupled PT, the interaction between the mechanical and electrical systems is minimal, and the mechanical vibration is the dominant factor. Without considering dielectric losses, a vibrating PT can then be approximately modelled as a current source $I_P$ in parallel with a capacitor $C_P$, as shown on the right side of Fig. 2-2. This model is widely applicable to most PEH systems [2-4][2-5][2-6].

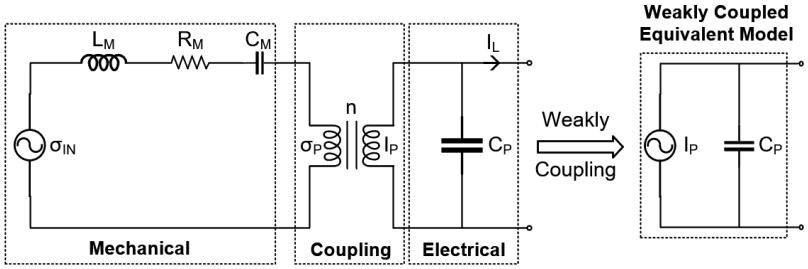


Fig. 2-2. Equivalent model of a piezoelectric transducer.

Since the output of a vibrating PT is an AC signal, an interface circuit is required to generate a DC output. The amount of power that can be extracted depends on the interface circuit, and throughout the thesis, we will use the power output of a full bridge rectifier (FBR) as a reference. The performance of some improvements on the standard FBR will be discussed in the following sections.

## 2.3 Rectifiers

### 2.3.1 Diode Rectifiers

Diode rectifiers are widely used in PEH applications due to their simplicity and ease of implementation [2-4]. However, their performance is limited by the forward voltage drop of the diodes, as discussed in Section 1.4.4.1. To mitigate this, [2-5] describes a full bridge rectifier (FBR) based on Schottky diodes, since these have lower forward voltage drops (~0.2V) than conventional diodes (0.7V). Alternatively, [2-6] proposed the replacement of the diodes of an FBR with diode-connected MOSFETs. This "active diode" configuration improves power conversion efficiency by 49% compared to a conventional FBR. Another way to mitigate the effect of the diode forward voltage drop is by using a voltage-doubler (VD) rectifier, which halves the voltage drop across the rectifier [2-7], as shown in Fig. 2-3. In this topology, when the PT voltage ($V_{PT}$) is positive, the top diode and capacitor $C_{REC1}$ are activated to harvest energy. Conversely, when $V_{PT}$ is negative, the bottom diode and capacitor $C_{REC2}$ are engaged. However, a VD rectifier requires two capacitors connected in series, resulting in greater bulk and lower effective load capacitance.

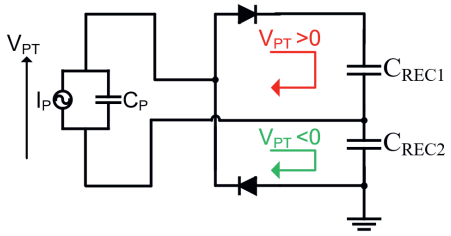


Fig. 2-3. Voltage doubler topology.

For both FBR and VD rectifiers, the polarity of $V_{PT}$ must be flipped by the charge generated by the PT. Even if the diode forward voltage drop is reduced to 0V, a significant amount of charge will still be wasted during the flipping process. This wasted energy limits power rectification efficiency. Therefore, recycling the wasted energy during voltage flipping is essential to enhancing energy conversion efficiency.

### 2.3.2 Active Rectifiers

*a) Synchronized switch harvesting on inductor (SSHI) rectifier:*

To recycle the wasted energy associated with voltage flipping, a Synchronized Switch Harvesting on Inductor (SSHI) rectifier uses an inductor to form an RLC tank that assists in $C_P$ flipping, significantly improving power conversion efficiency, as discussed in Section 1.4.4.1 [2-8][2-9]. This configuration is illustrated in Fig. 2-4.

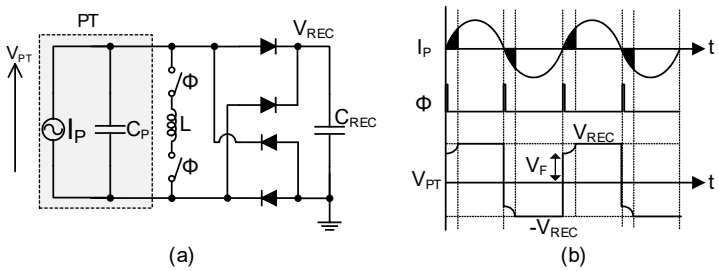


Fig. 2-4. An SSHI rectifier and its waveform.

The flipping efficiency, $\eta_F$, of an SSHI rectifier is defined as the ratio of the flipped voltage $V_F$, to the maximum output voltage $V_{REC}$, assuming that the diode forward voltage is 0V. Flipping efficiencies of 50%-70% were achieved in [2-8] and [2-9], resulting in 2 to 8 times more output power than with a conventional FBR. However, to achieve high flipping efficiency, conventional SSHI rectifiers require a large inductor, making them unsuitable for use in portable devices. Additionally, the inductor's finite resistance will dissipate heat during the flipping period—an undesirable effect, particularly for implantable devices. To address this, [2-10] and [2-11] proposed multi-step SSHI rectifiers, which perform flipping in multiple steps to reduce the current in the inductor. They achieve voltage flipping efficiencies of 80%-90% using relatively small (47μH and 10μH) inductors, respectively. Despite their efficiency, SSHI rectifiers are limited by high costs and heat generation, posing challenges for wearable and implantable devices. To overcome these limitations, alternative flipping methods are required that eliminate the need for bulky inductors.

*b) Synchronized switch harvesting on capacitors (SSHC) rectifier:*

A Synchronized Switch Harvesting on Capacitor (SSHC) rectifier eliminates the need for bulky inductors by employing flying capacitors to flip the PT voltage [2-13][2-14][2-15][2-16][2-17]. A one-stage SSHC rectifier and its waveform are shown in Fig. 2-5. $C_1$ is the flying capacitor, controlled by $\Phi_{1p}$, $\Phi_0$, and $\Phi_{1n}$. During $\Phi_{1p}$, the charge is transferred from $C_P$ to $C_1$. During $\Phi_0$, the remaining charge in $C_P$ is cleared, and during the $\Phi_{1n}$, the $C_1$ is again connected to $C_P$, to flip the voltage $V_{PT}$. Similarly, when the polarity of $V_{PT}$ needs to be flipped from negative to positive, the order of the $\Phi_{1p}$ and $\Phi_{1n}$ phases is reversed. This innovative approach eliminates bulky inductors. Unfortunately, it has a limited flipping efficiency (33.3%) due to the hard-charging loss between $C_P$ and $C_1$ [2-13], resulting in only 2 times more output power than with a conventional FBR.

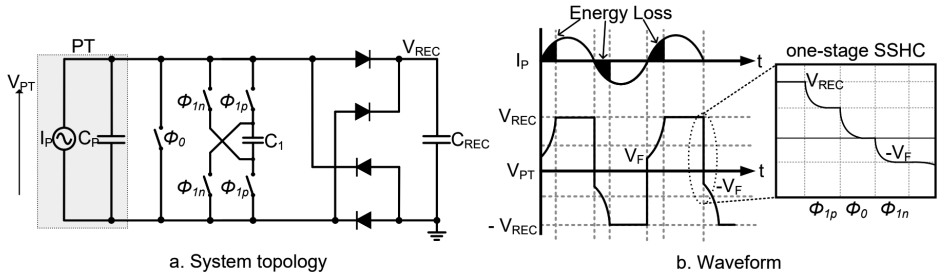


Fig. 2-5. One-stage SSHC rectifier and its waveform.

In order to minimize the hard-charging loss, multiple flying capacitors can be employed to flip PT voltage. As shown in Fig. 2-6, $C_1$ to $C_K$ are the flying capacitors, controlled by *2K+1* phases (*4K+1* switches): $\Phi_{1p}$, … $\Phi_{Kp,}$ $\Phi_0$, $\Phi_{Kn}$, … $\Phi_{1n}$. During the first *K* phases, the PT shares its charge with *K* flying capacitors: $C_1$ to $C_K$. During $\Phi_0$, the remaining charge in $C_P$ is cleared, and during the next *K* phases, the flying capacitors are again sequentially connected to $C_P$, but with the phases reversed, to flip the voltage $V_{PT}$. Similarly, when the polarity of $V_{PT}$ needs to be flipped from negative to positive, the order of the *2K+1* phases is reversed. This technique reduces hard-charging loss in a 1-stage SSHC rectifier, achieving up to 8 times more output power

than with a conventional FBR, and resulting in a more compact and cost-effective solution for PEH systems.

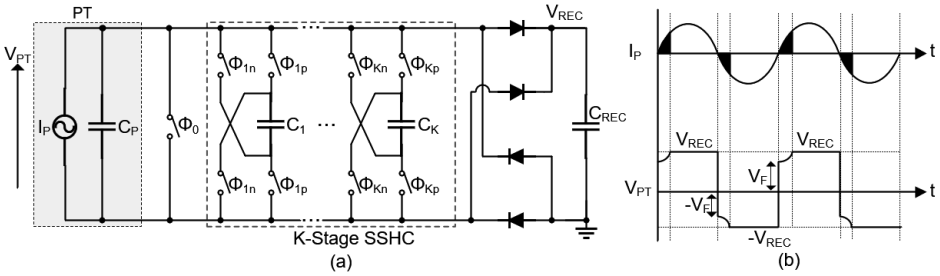


Fig. 2-6. K-stage SSHC rectifier and its waveform.

Despite these advantages, *K*-stage SSHC rectifiers still face several challenges [2-13]. To increase their flipping efficiency, both the stage number (*K*) and the size of the flying capacitors ($C_K$) must be increased. In [2-16], ideal capacitors and switches were used to evaluate the flipping efficiency for various combinations of *K* and $C_K$. Assuming that all the flying capacitors are equal ($C_1 = C_2 = \ldots = C_K$), $\eta_F$ can be expressed as follows:

$$\eta_F = \frac{KC_K}{C_P + (K+1)C_K} \tag{2.3}$$

Increasing $C_K$ relative to $C_P$ also increases $\eta_F$. However, since commercial off-the-shelf PTs typically have large intrinsic capacitances, often in the order of a few tens of nano Farads, it is usually impractical to realize the required flying capacitors on-chip due to their size.

Some studies have demonstrated fully integrated rectifiers, but they generally operate with small PTs. In [2-18], a fully integrated 6-stage SSHC rectifier was proposed with a total on-chip flying capacitance of 1.74nF. Although it achieved 71% flipping efficiency, it was combined with a small PT ($C_P$ = 78pF) with limited output power. Subsequently, [2-19] and [2-20] proposed fully integrated 8-stage SSHC rectifiers, both with total on-chip flying capacitance of 4nF, achieving 78% flipping efficiency. These designs partitioned the PT into 8 equal regions and then connected each region

in series or individually to the rectifier during flipping. This reduces the effective capacitance connected to the rectifier and thus the required flying capacitance. However, these designs were designed for use with MEMS (microelectromechanical systems) PTs with total $C_P$ values of only 2.4nF and 1.94nF, respectively, and are not suitable for use with larger PTs capable of milliwatt-level output power.

In [2-21], a fully integrated frequency-tuning SSHC rectifier with 800pF total flying capacitance was developed for a 28.8-nF $C_P$. However, this design had low flipping efficiency (<30%) and required a 1MHz clock to control the switching of the flying capacitors and an external clock for system operation. Its maximum output power was just 28μW due to the limited flipping efficiency and clock operating frequency. In fact, most SSHC rectifiers rely on a number of off-chip capacitors to achieve high output power, which inevitably increases the system volume and the number of external connections. Achieving high flipping efficiency while reducing the flying capacitance of the rectifier without sacrificing the $C_P$ capacitance remains a critical and unsolved challenge.

## 2.4 Maximum Power Point Tracking Techniques

As discussed in Section 1.4.4.2, the use of the maximum power point tracking (MPPT) technique is essential to maximize the output power of a rectifier. The two most commonly employed MPPT variants are the fractional open-circuit voltage (FOCV) [2-22][2-23][2-24][2-25][2-26][2-28] and perturb and observe (P&O) [2-30][2-31][2-32][2-33][2-34] techniques. This section discusses their operational principles, benefits, and limitations.

### 2.4.1 Fractional Open Circuit Voltage MPPT

Due to its simplicity, the FOCV MPPT technique is the most widely used MPPT method in PEH systems [2-22][2-23]. The maximum power point (MPP) is determined from the theoretical relationship between the rectifier's output power ($P_{OUT}$) and its output voltage ($V_{REC}$). This relationship is given by [2-22]:

$$P_{OUT} = 2f_p C_P V_{REC}(2V_{OC} - V_{REC} \times (1 - \eta_F)) \tag{2.4}$$

where $f_p$ is the resonant frequency of the PT, and $V_{OC}$ is its open circuit voltage. From this equation, we can obtain the expression for the optimal $V_{REC}$ ($V_{MPP}$) corresponding to the MPP as follows [2-24]:

$$V_{MPP} = \frac{V_{OC}}{1 - \eta_F} \tag{2.5}$$

It is a function of the open circuit voltage, $V_{OC}$, and the flipping efficiency, $\eta_F$. By regulating $V_{REC}$ to match $V_{MPP}$, the FOCV technique achieves MPPT.

Fig. 2-7 shows the topology of a system that implements the FOCV MPPT technique. It consists of an open circuit voltage ($V_{OC}$) sampler, a $\eta_F$ calibration block, an MPPT monitor, an AC-DC rectifier, a buck-boost DC-DC converter, a regulator, a rectified capacitor ($C_{REC}$), a storage capacitor ($C_S$) and an output capacitor ($C_{OUT}$). The $V_{OC}$ sampler periodically samples the PT's open-circuit voltage, $V_{OC}$, and a $\eta_F$ calibration block calculates an accurate $\eta_F$. The sampled $V_{OC}$ and accurate $\eta_F$ are fed to the MPPT monitor to calculate the theoretical MPP voltage ($V_{MPP}$). When $V_{REC}$ reaches the $V_{MPP}$, the DC-DC converter transfers extra energy from $C_{REC}$ to $C_S$, preventing $V_{REC}$ from rising further. Since the output voltage ($V_S$) across $C_S$ fluctuates during the MPPT process, an additional DC-DC regulation stage is implemented to ensure a stable and consistent output voltage ($V_{OUT}$), suitable for powering wireless sensors.

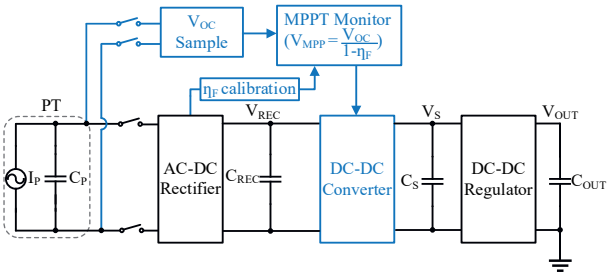


Fig. 2-7. Fractional open circuit voltage (FOCV) MPPT topology.

Unfortunately, the need to calculate $V_{MPP}$ in the FOCV MPPT technique presents several challenges for circuit implementation.

First, the periodic sampling of the open-circuit voltage ($V_{OC}$) introduces energy losses. For example, in [2-25], $V_{OC}$ was sampled once every 20 vibration cycles and achieved 70% MPPT efficiency. However, the sampling resulted in a 5% energy loss. In [2-26], the $V_{OC}$ sampling rate was reduced to once every 2046 vibration cycles (approximately every 14.6 seconds), resulting in a higher MPPT efficiency of 77%. However, increasing the sampling interval reduces the system's ability to track rapid changes in excitation conditions, limiting its responsiveness to environmental variations and potentially degrading overall performance.

Second, the flipping efficiency ($\eta_F$) of an active rectifier is not constant, which complicates the accurate determination of $V_{MPP}$. For instance, in an SSHI rectifier, $\eta_F$ is dependent on several circuit parameters and can be expressed as [2-27]:

$$\eta_F = e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C_P}-1}}} \tag{2.6}$$

Here, L is the inductance, and R is the resistance of the switches and inductor in the RLC tank, and $C_P$ is the PT capacitance. Variations in L and R can significantly affect $\eta_F$ and, by extension, $V_{MPP}$. To address this, some FOCV MPPT implementations measure $\eta_F$ using external components. The measured information is then used to determine the relationship between $V_{REC}$ and $V_{OC}$ at the MPP [2-25] [2-26]. However, these approaches are quite complicated and so, in other designs, $\eta_F$ is simply assumed to be constant. For example, in [2-28], $\eta_F$ was fixed at 80% for $V_{MPP}$ calculation, ignoring its dependence on the rectified voltage ($V_{REC}$), leading to inaccurate $V_{MPP}$ tracking. In reality, $\eta_F$ increased by 5% to 10% as $V_{REC}$ increased from 2V to 5V [2-29]. Since $\eta_F$ appears in the denominator of equation (2.5), such changes cause significant shifts in $V_{MPP}$. These dependencies on external components and the challenges in pre-

cisely estimating $\eta_F$ limit the scalability and integration of FOCV-based MPPT circuits. They also pose a significant barrier to realizing compact, high-efficiency PEH systems.

### 2.4.2 Perturb & Observe MPPT

As introduced in Section 1.4.4.2, the P&O algorithm is another widely adopted method for MPPT in PEH systems. Unlike the FOCV method, P&O eliminates the need for the periodic sampling of the open-circuit voltage ($V_{OC}$) and bypasses the need for flipping efficiency ($\eta_F$) calibration [2-30][2-31]. Instead, it adjusts the rectifier's operating point incrementally by perturbing system parameters and observing the corresponding changes in output power. This iterative process helps the system converge towards the MPP.

However, the step-by-step adjustment inherent to P&O requires precise measurement of the rectified output power, typically involving both current and voltage sensing. Implementing this functionality often leads to complex circuit designs and higher power consumption. For example, in [2-32], a flyback converter's peak inductor current and voltage were measured using a high-precision current sensor and an analog-to-digital converter (ADC). The digitized data was then processed by a microcontroller unit (MCU) executing the P&O algorithm to locate the MPP. While this approach achieved an MPPT efficiency exceeding 94%, it required multiple complex components, increasing system complexity and energy overhead.

In another example, [2-33] employed a mixed-signal approach where the input voltage and current were multiplied using a MOSFET operating in the sub-threshold region to estimate the output power. This method achieved a high MPPT efficiency of 99.9%, but it still necessitated precise analog design and careful calibration to maintain accuracy and efficiency. Similarly, the work in [2-34] proposed a method to evaluate PEH output power by counting the switching time of a DC-DC converter. Although this solution was fully implemented in analog circuitry, it consumed nearly 10%

of the harvested energy just for MPPT control, which is substantial for low-power energy harvesting systems.

These examples illustrate a common trade-off in P&O-based MPPT techniques: while they offer accurate and adaptive tracking, they rely on complex circuit implementations—often including current sensors, ADCs, MCUs, and transient power measurement blocks. This complexity results in higher power consumption and poses significant challenges for system integration and scalability in compact, low-power energy harvesting applications.

## 2.5 Cascaded System Architecture

In a PEH system, the output regulator plays a critical role. As discussed in Section 1.4.4.3, it directly drives the load by transferring energy from the storage capacitor to the output capacitor. Despite its importance, this stage is often neglected in many PEH designs, which typically focus only on improving the rectifier and/or the MPPT. For example, [2-18][2-19][2-20][2-21][2-35] focus on optimizing rectifier performance, while [2-30][2-31][2-32][2-33][2-34] focus primarily on MPPT techniques.

Typical PEH systems consist of a rectifier, an MPPT and an output regulator to provide a stable output voltage. However, this multi-stage approach often results in lower overall power conversion efficiency. For instance, [2-36] and [2-37] describe three-stage system architectures that use low-dropout (LDO) regulators. Although the LDOs ensured stable power delivery, the systems achieved only modest power conversion efficiencies, ranging from 50% to 80%. Furthermore, the efficiency of LDO regulators decreases significantly when the voltage difference between the storage capacitor and the output capacitor increases, leading to higher energy losses.

In [2-38], a DC-DC regulator was used to generate stable output voltages. However, its power conversion efficiency was not reported and is presumed to be low. This presumption is based on its relatively modest power gain (reported 4.5× in the paper) compared to a full-bridge rectifier (FBR), indicating limited overall efficiency.

Similarly, [2-39] used a trickle charger to generate regulated output voltages of 1.8V and 1.35V. However, its power conversion efficiency was quite low, approximately 58% when the storage voltage changed from 1.2V to 1.8V, with an average efficiency of around 65%.

In summary, cascaded system architectures often suffer from reduced power conversion efficiency, which is mainly due to the compounded losses associated with their multiple stages. Therefore, developing system architectures with fewer cascaded stages is a promising direction for future research. Such approaches could significantly enhance the end-to-end efficiency and practicality of PEH systems.

## 2.6 Conclusion

This chapter reviewed the key interface circuits used PEH systems, including diode-based and active rectifiers, MPPT techniques, and cascaded system architectures. While active rectifiers such as SSHI and SSHC improve power extraction efficiency, they often require bulky inductors or large flying capacitors, limiting their integration and scalability. Existing MPPT methods, including FOCV and P&O, face trade-offs between complexity, energy loss, and tracking accuracy. Additionally, conventional cascaded architectures result in compounded energy losses, limiting overall end-to-end efficiency. Therefore, the main challenges in PEH interface design remain: achieving high-voltage flipping efficiency with compact circuits, implementing low-power, accurate MPPT schemes, and improving system-level efficiency by reducing cascaded losses. Addressing these challenges is critical for enabling highly integrated and energy-efficient PEH systems, which is the focus of the following chapters.

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# Chapter 3 A Synchronized Switch Harvesting Rectifier with Reusable Storage Capacitors [1]

## 3.1 Introduction

As discussed in Chapter 2.3.2, most synchronized switch harvesting on capacitors (SSHC) rectifiers for piezoelectric energy harvesting (PEH) require large capacitors to achieve high output power, leading to large system volumes. To address this issue, this chapter proposes a synchronized switch harvesting on shared capacitors (SSHSC) rectifier, which achieves synchronized voltage flipping without dedicated flying capacitors [3-1]. In an SSHC rectifier, at least 8 flying capacitors and 1 energy storage capacitor are required for good efficiency [3-2]. In the proposed SSHSC rectifier, no dedicated flying capacitors are present; instead, the energy storage capacitors are intermittently used as flying capacitors. As a result, the proposed rectifier only requires 3 off-chip capacitors, occupying significantly less volume and requiring fewer I/O connections than conventional SSHC rectifiers.

## 3.2 Theoretical Analysis of the Proposed Rectifier

### 3.2.1 Flying Capacitors Used in a Typical SSHC Rectifier

Fig. 3-1 shows the topology of a typical *K*-stage SSHC rectifier. It employs a full bridge rectifier (FBR) that consists of four cross-connected MOSFETs and an active diode. This generates a rectified voltage ($V_{REC}$) across the storage capacitor, $C_{REC}$. As discussed in Chapter 2.3.2, the voltage on the piezoelectric transducer (PT) can then be efficiently flipped with the help of *K* flying capacitors $C_1$ to $C_K$ and *4K+1* switches.

[1] This chapter is based on the journal paper: X. Yue and S. Du, "A Synchronized Switch Harvesting Rectifier with Reusable Storage Capacitors for Piezoelectric Energy Harvesting," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 9, pp. 2397-2606, Sept. 2023.

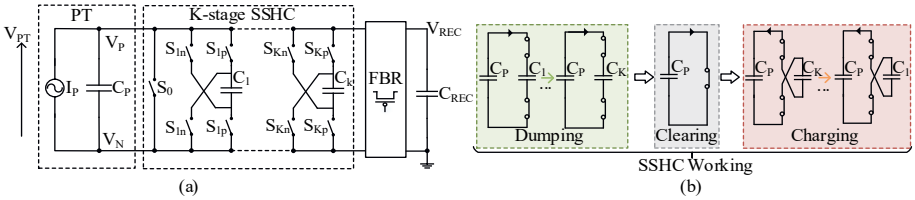



Fig. 3-1. (a) Topology of the typical K-stage SSHC rectifier, (b) SSHC working process.

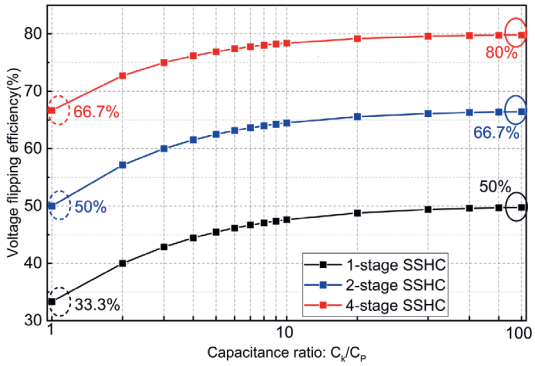



Fig. 3-2.Voltage flipping efficiency of 1-, 2- and 4-stage SSHC rectifiers with different flying capacitor ratios.

According to equation (2.3) in Chapter 2.3.2, increasing $C_K$ enhances flipping efficiency. As shown in Fig. 3-2, however, the relationship eventually saturates. For instance, while increasing the capacitance ratio $C_K/C_P$ from 1 to 10 significantly increases the flipping efficiency, further increases have only limited effect.

Considering the trade-off between circuit complexity and flipping efficiency, four flying capacitors, with $C_K >> C_P$, are a good choice. In a typical SSHC rectifier, this will result in a complex circuit with 17 switches, as shown in Fig. 3-3.

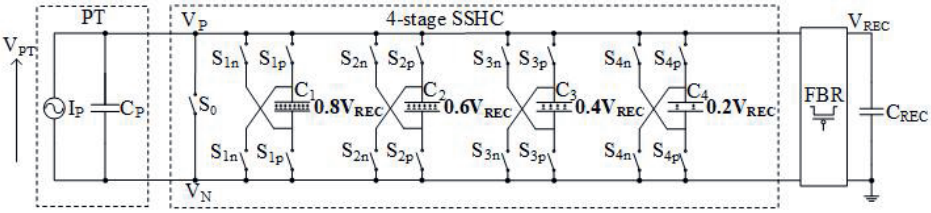



Fig. 3-3. Voltage levels across the large flying capacitors of a typical 4-stage SSHC rectifier.

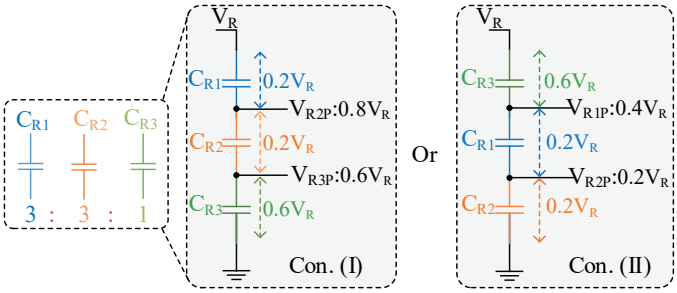
### 3.2.2 Storage Capacitor Sharing in the Proposed SSHSC Rectifier

*a) Proposed capacitor sharing concept:*

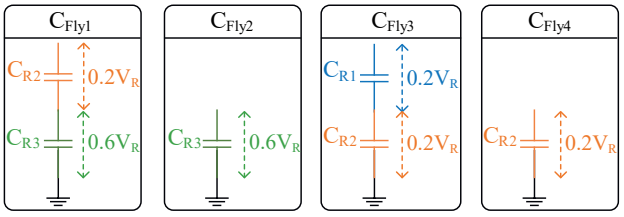
In an SSHC rectifier, the flying capacitors flip the voltage on the PT by draining charge from $C_P$ and then sequentially dumping it back with reverse polarity. Therefore, they act as temporary charge reservoirs. As discussed in the previous section, increasing their size will increase the flipping efficiency. However, the largest capacitors in an SSHC rectifier are the storage capacitors, which store the harvested energy when the rectifier is in cut-off state. This indicates that the storage capacitors could also be used to flip the voltage across the PT, since this only happens when the rectifier is cut-off. Using the storage capacitors to sequentially perform the non-conflicting operations of storing energy and flipping voltage would simplify the system by obviating the need to employ dedicated flying capacitors.

If the storage capacitors are to be used as temporary flying capacitors, their voltage should not be significantly changed by the flipping process, which imposes a specific requirement for the storage capacitance ratio. With four flying capacitors and $C_K >> C_P$, the steady-state voltages across $C_1$, $C_2$, $C_3$, and $C_4$ are $0.8V_{REC}$, $0.6V_{REC}$, $0.4V_{REC}$, and $0.2V_{REC}$. These voltages must also be provided by the dual-use storage capacitors. To achieve this, instead of a single storage capacitor, the proposed SSHSC rectifier employs three series-connected storage capacitors, $C_{R1}$, $C_{R2}$, and $C_{R3}$, such that $C_{R1}$: $C_{R2}$: $C_{R3}$ = 3:3:1 as shown in Fig. 3-4. Denoting the voltage across the three capacitors as $V_R$, two connection configurations are used: Con. (I) (following the sequence from the top $V_R$ to $C_{R1}$→$C_{R2}$→$C_{R3}$ to ground) and Con. (II) (following the sequence from the top $V_R$ to $C_{R3}$→$C_{R1}$→$C_{R2}$ to ground). Con. (I) is the default configuration when the capacitors are used for energy storage. The voltages across $C_{R1}$, $C_{R2,}$ and $C_{R3}$ are then $0.2V_R$, $0.2V_{R,}$ and $0.6V_R$ due to the 3:3:1 ratio of $C_{R1}$, $C_{R2,}$ and $C_{R3}$. Therefore, in Con. (I), $V_{R2P}$ and $V_{R3P}$, the voltage at the positive plates of $C_{R2}$ and $C_{R3}$, provide the voltage levels of $0.8V_R$ and $0.6V_R$ for the 1- and 2-stage flipping. In Con. (II), $V_{R1P}$ and $V_{R2P}$, the positive plates of $C_{R1}$ and $C_{R2}$, provide the voltage levels of $0.4V_R$ and $0.2V_R$

for the 3- and 4-stage flipping. Therefore, the four virtual flying capacitors used in the 4-stage SSHSC rectifier are $C_{Fly1}$ ($C_{R2}$ and $C_{R3}$ in series), $C_{Fly2}$ ($C_{R3}$ only), $C_{Fly3}$ ($C_{R1}$ and $C_{R2}$ in series), and $C_{Fly4}$ ($C_{R2}$ only). The 4 voltage levels $V_{Fly1}$, $V_{Fly2}$, $V_{Fly3}$, and $V_{Fly4}$ provided by the virtual flying capacitors $C_{Fly1}$, $C_{Fly2}$, $C_{Fly3}$, and $C_{Fly4}$ are $0.8V_R$, $0.6V_R$, $0.4V_R$, and $0.2V_R$, which are the same as those generated by the dedicated flying capacitors of the traditional SSHC rectifier shown in Fig. 3-3.




(a) Voltage levels generated by the storage capacitors




(b) Four virtual flying capacitors for voltage flipping

Fig. 3-4. Configurations and combinations of three storage capacitors to form four virtual flying capacitors to be used in a 4-stage SSHSC rectifier.

*b) Theoretical analysis*:

As in a traditional SSHC rectifier, the voltage flipping is done in 3 phases: dumping, clearing, and charging. After each phase, the PT voltages $V_{PT}$ and $V_{Fly1}$, $V_{Fly2}$, $V_{Fly3}$, $V_{Fly4}$ are updated. To guarantee efficient flipping while maintaining the energy stored on the three storage capacitors, their voltages should remain the same before and after flipping. To check this assumption, a detailed theoretical analysis is performed in the following section:

First, the voltages across PT, $V_{PT}$, in the 1st stage with the virtual capacitor, $C_{Fly1}$, can be calculated as

$$\begin{aligned} \text{before dumping: } & V_{PT} = V_R, V_{Fly1} = 0.8 \times V_R \\ \text{after dumping: } & V_{PT} = V_{Fly1} = \frac{V_R \times C_P + 0.8 \times V_R \times C_{Fly1}}{C_{Fly1} + C_P} \\ & = 0.8 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly1}} = 0.8 \times V_R + \alpha_1 \end{aligned} \tag{3.1}$$

Where the voltage increment, $\alpha_1 = \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly1}}$. This is extremely small, since $C_{Fly1}$, which consists of storage capacitors, is significantly larger than $C_P$.

In the next phase, charge is dumped from $C_P$ to $C_{Fly2}$. The PT voltage ($V_{PT}$) variations in this phase are

$$\begin{aligned} \text{before dumping: } & V_{PT} = 0.8 \times V_R + \alpha_1, V_{E2} = 0.6 \times V_R \\ \text{after dumping: } & V_{PT} = V_{Fly2} = \frac{(0.8 \times V_R + \alpha_1) \times C_P + 0.6 \times V_R \times C_{Fly2}}{C_{Fly2} + C_P} \\ = 0.6 \times V_R + & \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly2}} + \frac{\alpha_1 \times C_P}{C_P + C_{Fly2}} = 0.6 \times V_R + \alpha_2 + \frac{\alpha_1 \times C_P}{C_P + C_{Fly2}} \end{aligned} \tag{3.2}$$

Where $\alpha_2 = \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly2}}$. Once more, $C_{Fly2} \gg C_P$, means that $\alpha_2$ is extremely small, while the third term in (3.2) is negligibly smaller due to the multiplication by $\alpha_1$. Therefore, (3.2) can be approximated as

$$V_{PT} = V_{Fly2} \approx 0.6 \times V_R + \alpha_2 \tag{3.3}$$

Similarly, after the dumping in the 3rd and 4th phases, the voltages on the capacitors can be expressed by the following equations.

$$V_{PT} = V_{Fly3} = \frac{(0.6 \times V_R + \alpha_2) \times C_P + 0.4 \times V_R \times C_{Fly3}}{C_{Fly3} + C_P}$$
$$= 0.4 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly3}} + \frac{\alpha_2 \times C_P}{C_P + C_{Fly3}}$$
$$= 0.4 \times V_R + \alpha_3 + \frac{\alpha_2 \times C_P}{C_P + C_{Fly3}} \approx 0.4 \times V_R + \alpha_3 \quad (3.4)$$

$$V_{PT} = V_{Fly4} = \frac{(0.4 \times V_R + \alpha_3) \times C_P + 0.2 \times V_R \times C_{Fly4}}{C_{Fly3} + C_P}$$
$$= 0.2 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly4}} + \frac{\alpha_3 \times C_P}{C_P + C_{Fly4}}$$
$$= 0.2 \times V_R + \alpha_4 + \frac{\alpha_3 \times C_P}{C_P + C_{Fly4}} \approx 0.2 \times V_R + \alpha_4 \quad (3.5)$$

Where $\alpha_3 = \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly3}}$ and $\alpha_4 = \frac{0.2 \times V_R \times C_P}{C_P + C_{Fly4}}$. Therefore, after dumping charge from $C_P$ to the 4 virtual flying capacitors, the voltage changes in the four virtual flying capacitors are approximately $\alpha_1$, $\alpha_2$, $\alpha_3$, and $\alpha_4$, respectively, which are all very small values. After dumping, the remaining charge in $C_P$ is cleared to zero in the following phase, resulting in $V_{PT} = 0$. The sequence of the charge charging back to $C_P$ follows the reverse sequence compared with the dumping. The voltage across the PT after the 1st phase of charging is expressed as

$$-V_{PT} = V_{Fly4} = \frac{0.2 \times V_R \times C_{Fly4} + \alpha_4 \times C_{Fly4}}{C_{Fly4} + C_P}$$
$$= 0.2 \times V_R - \alpha_4 + \frac{\alpha_4 \times C_{Fly4}}{C_{Fly4} + C_P} \approx 0.2 \times V_R \quad (3.6)$$

The approximation in the last derivation step in (3.6) can be made because $C_{Fly4} >> C_P$, and so the two $\alpha_4$ terms cancel. Therefore, after this charging phase, the voltage across PT and $C_{Fly4}$ goes back to $0.2V_R$, which is the voltage before $C_{Fly4}$ was used in the 4th dumping phase. This explains why the voltage across the $C_{Fly4}$ does not change during the voltage flipping process. Similarly, the voltage of the second, third, and fourth flipping phases can be written as follows

$$-V_{PT} = V_{Fly3} = 0.4 \times V_R - \alpha_3 + \frac{\alpha_3 \times C_{Fly3}}{C_{Fly3} + C_P} \approx 0.4 \times V_R \quad (3.7)$$

$$-V_{PT} = V_{Fly2} = 0.6 \times V_R - \alpha_2 + \frac{\alpha_2 \times C_{Fly2}}{C_{Fly2} + C_P} \approx 0.6 \times V_R \quad (3.8)$$

$$-V_{PT} = V_{Fly1} = 0.8 \times V_R - \alpha_1 + \frac{\alpha_1 \times C_{Fly1}}{C_{Fly1} + C_P} \approx 0.8 \times V_R \quad (3.9)$$

According to this analysis, the voltages across all four virtual flying capacitors after flipping, as given in (3.9), (3.8), (3.7), and (3.6), are the same as their voltages before flipping, as given in (3.1), (3.2), (3.3), and (3.2). Furthermore, the analysis shows that the voltage flipping efficiency is 80%, based on the values of $V_{PT}$ before and after flipping, as given in (3.9). The proposed SSHSC rectifier can thus achieve a high voltage flipping efficiency at 80% while maintaining the voltages across the storage capacitors. These two results confirm our proposition that an SHSC rectifier can be realized without using dedicated flying capacitors.

## 3.3 Proposed Synchronized Switch Harvesting Rectifier

### 3.3.1 Topology and System Operations

The detailed flipping process of the proposed SSHSC rectifier is shown in Fig. 3-5. When the bridge rectifier is conducting, the three storage capacitors follow the connection Con. (I) in Fig. 3-4. When the bridge rectifier is cut-off, and $V_{PT}$ needs to be flipped, the three storage capacitors are reconfigured for use as the four virtual flying capacitors. Fig. 3-5 shows the 9 phases (#1 to #9) that are used to flip $V_{PT}$ from positive to negative. To flip $V_{PT}$ from negative to positive, the phase order simply starts from #9 and ends at #1. In phase #1, by closing $\Phi_a$, $C_P$ is connected in series with $C_{R2}$ and $C_{R3}$ ($C_{R2}$+$C_{R3}$), which provides the $0.8V_R$ voltage level, so the charge in $C_P$ dumps to $C_{R2}$ and $C_{R3}$. After the 1st dumping, the voltage across $C_P$ and $C_{R2}$+$C_{R3}$ is very close to $0.8V_R$ thanks to their large capacitance. Then, $C_{R3}$ provides $0.6V_R$ for the second stage dumping, as shown in Fig. 3-5 (#2), and $C_P$ dumps the charge to $C_{R3}$, and $V_{PT}$ is finally stabilized at $0.6V_R$. To generate $0.4V_R$ and $0.2V_R$ for 3- and 4-stage flipping, the connection of the three storage capacitors is changed from Con. (I) to Con. (II) in

Fig. 3-5 (#3) and (#4) respectively. $C_P$ is connected and dumps charge to $C_{R1}$ and $C_{R2}$ in Fig. 3-5 (#3) and $C_{R2}$ in Fig. 3-5 (#4), respectively, stabilizing at $0.4V_R$ and $0.2V_R$. After dumping, in phase $\Phi_0$, the remaining charge in $C_P$ is cleared, and the voltage on the PT is inverted by reversing the dumping sequence: from (#6) to (#9). From (#6) to (#9) in Fig. 3-5, the charge is flipped back from $C_{R2} \rightarrow C_{R1} + C_{R2} \rightarrow C_{R3} \rightarrow C_{R2} + C_{R3}$ to $C_P$, where the storage capacitors provide -0.2VR, -0.4VR, -0.6VR, and -0.8VR, respectively, for charging $C_P$.

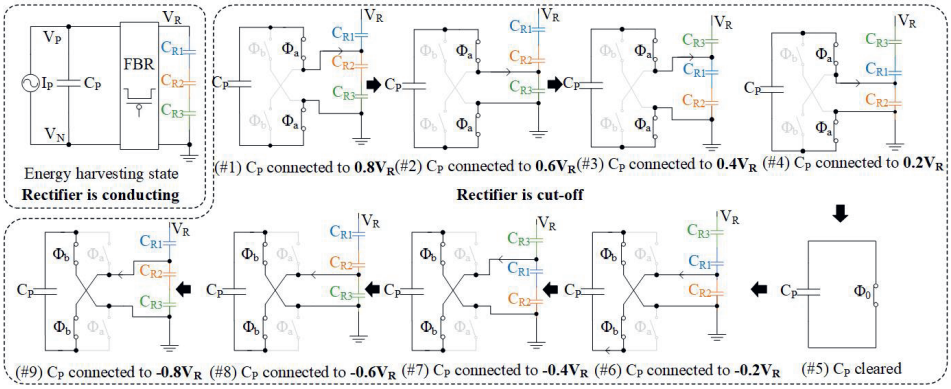



Fig. 3-5. The working flow of the proposed SSHSC rectifier: the rectifier is being conducted for energy extraction; the rectifier is being cut off for flipping $V_{PT}$ in 9 phases.

### 3.3.2 System Architecture

Fig. 3-6 shows the system architecture of the proposed SSHSC rectifier. It includes five main parts: an FBR, a "switch I" block and its associated control block, a "switch II" block and its associated control block. The "switch I" block performs the voltage flipping process in 9 phases, while the "switch II" block creates virtual flying capacitors with 3 storage capacitors corresponding to the 9 flipping phases. When it is time to flip the PT voltage, the FBR block will generate a synchronized signal, *SYN*. As an indicator, the *SYN* is fed to the "switch II control" block, which will generate $S_{R1}$ and $S_{R2}$ to decide the configurations of the storage capacitors, as in Fig. 3-4. After the configuration is fixed, the *SYN* is fed to the "switch I control" block to generate the switch control signals for the switches in the "switch I" block. Through the pulse generation, PG, pulse sequencing, PS, block, and some OR gates, the control signals

are generated. Through the level shifters, the signals $\Phi_a$, $\Phi_b$, $\Phi_0$, $S_{R3P}$, $S_{R2P}$, and $S_{R1P}$ are used to drive the switches in the "switch I" block. Unlike typical SSHC rectifiers, the synchronized switches $\Phi_a$ and $\Phi_b$ in "switch I" are used repeatedly in every flipping stage, decreasing the number of switches. The circuit details of the level shifter, (LS), pulse sequencing, (PS), cell, delay cell, and transmission gate are also presented in Fig. 3-6.

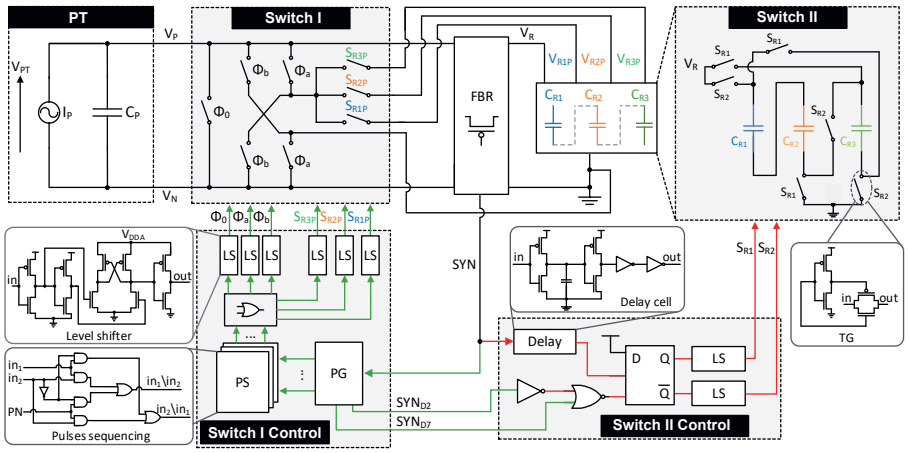



Fig. 3-6. The system architecture of the proposed SSHSC rectifier.

The $V_{PT}$ flipping moment from positive to negative and the corresponding switch control signals are shown in Fig. 3-7. It has 9 flipping phases from (#1) to (#9) and follows the voltage levels from $0.8V_R \rightarrow 0.6V_R \rightarrow 0.4V_R \rightarrow 0.2V_R \rightarrow 0 \rightarrow -0.2V_R \rightarrow -0.4V_R \rightarrow -0.6V_R \rightarrow -0.8V_R$. The $S_{R1}$ and $S_{R2}$ are used to decide if Con. (I) or Con. (II), shown in Fig. 3-4 (a), is used. The $S_{R1}$ is high during (#3) to (#7), which is exactly in 3- and 4-stage flipping and PT voltage clearing periods; otherwise, $S_{R2}$ always keeps high. The $S_{R1P}$, $S_{R2P}$, and $S_{R3P}$ are used to decide which positive plates of $C_{R1}$, $C_{R2}$, and $C_{R3}$ are connected to $V_P$ to generate 4 voltage levels for charging, as the same as introduced in Fig. 3-4. The $\Phi_a$, $\Phi_b$, and $\Phi_c$ drive only one group of synchronized switches to connect the effective capacitors to $C_P$ for flipping instead of dedicated switches for every flying capacitor.

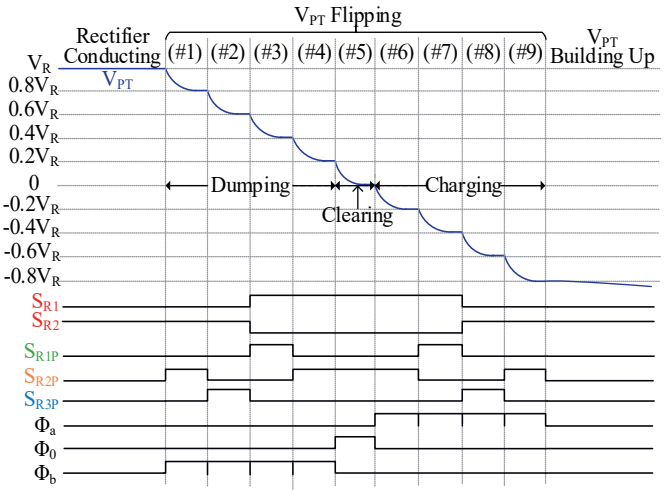



Fig. 3-7. PT voltage flipping moment and the associated control signals for switches.

## 3.4 Circuit Implementation

### 3.4.1 FBR implementation

This section presents the implementation of the FBR, the pulse generation block, and the switch bulk regulation block. To reduce its voltage drop, the FBR consists of 4 cross-connected MOSFETs and an active diode [2-10], as shown in Fig. 3-8. When the $I_P$ current is zero, the FBR becomes non-conductive, and $V_1$ becomes lower than $V_R$; the comparator is triggered, and a rising edge in the synchronized signal, *SYN*, is generated, indicating the starting time for flipping. The offset in the comparator caused by random mismatch at the zero-crossing of $I_P$ is about 7mV, resulting in an acceptable delay in the *SYN* signal due to the low (130Hz) vibration frequency.

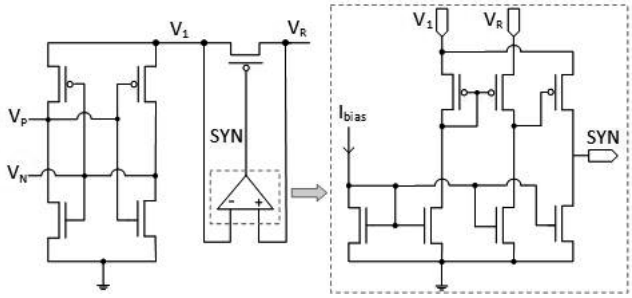
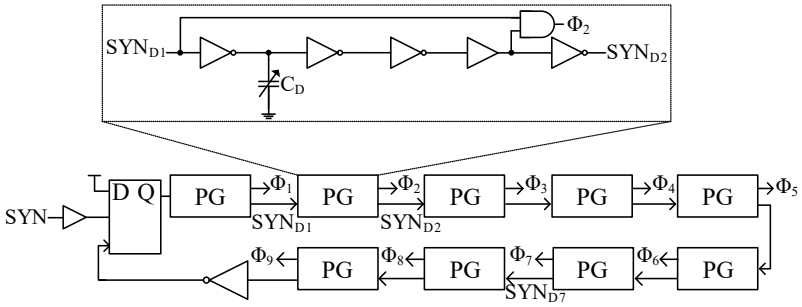
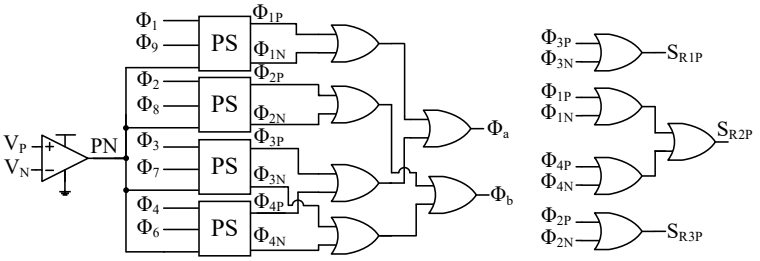



Fig. 3-8. The 4 cross-connected MOSFETs and active diode in the FBR block.




(a) Pulses generation for each switch control in every stage during flipping




(b) Pulses generation for one group shared switch

Fig. 3-9. Pulse generation (PG) block in "switch I control."

### 3.4.2 Pulse Generation Block

The *SYN* signal is fed to the pulse generation (PG), as shown in Fig. 3-9 (a). Through a PG cell, the switch control signals $\Phi_1 \rightarrow \Phi_9$ and their corresponding delayed $SYN_D$ are generated, where the PG cell is composed of two weak inverters and an adjustable capacitor array $C_D$. The generated output control signals $\Phi_1 \rightarrow \Phi_9$ are fed to a pulse sequencing (PS) block where the sequence of the pulses is decided by

the PN generated in Fig. 3-9 (b), which indicates the flipping sequence (positive to negative or vice versa). Because only one group of switches is shared between different stages, after sequencing, the output control signals $\Phi_1$ to $\Phi_9$ are fed to some OR gates to generate $\Phi_a$, $\Phi_b$, $S_{R1P}$, $S_{R2P}$, and $S_{R3P}$ as shown in Fig. 3-9 (b).

### 3.4.3 Supply Voltage Selector for Switches

Fig. 3-10 shows the supply voltage selector for the transmission gate switches used in the "Switch I" and "Switch II" blocks to achieve $V_{DDA}$ = max ($V_{DD}$, $V_R$). This is important to ensure the switches are fully turned ON or OFF for proper operation. In this circuit, there are two large power switches, $M_1$ and $M_2$, whose gates are controlled by the output of a comparator, as shown on the right. When $V_{DD} > V_R$, the output of the comparator is high, resulting in $M_1$ and $M_3$ in the open state and $M_2$ in the off state. Therefore, $V_{DDA} = V_{DD}$. Similarly, when $V_{DD} < V_R$, $V_{DDA}$ is connected to $V_R$.

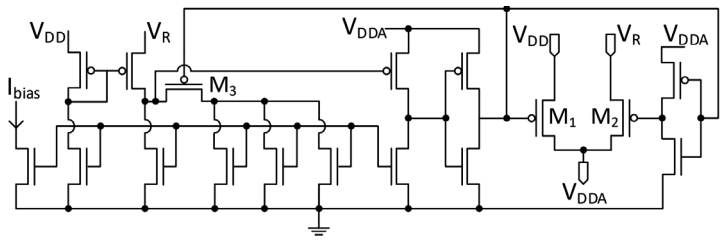



Fig. 3-10. Supply voltage selector for switches of the SSHSC rectifier.

## 3.5 Measurement Results

### 3.5.1 Measurement Setup

The proposed SSHSC rectifier was fabricated using a 180-nm BCD process and occupies 0.18 $mm^2$ of active area. Fig. 3-11 shows the measurement setup (left) and chip micrograph (right). The chip was tested with a 22nF commercial PT (PEH-S128-H5FR-1107YB), which was installed on a shaker (LDS V450) and excited at a resonance of 130Hz.

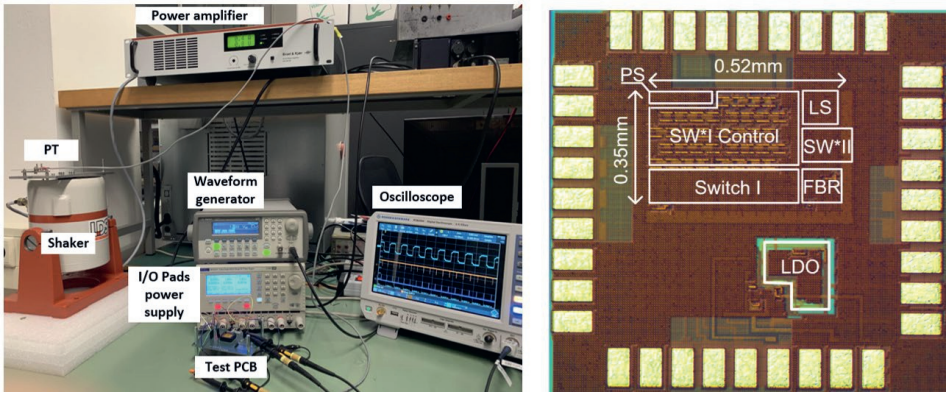



Fig. 3-11. Measurement setup and chip micrograph.

### 3.5.2 Measured Voltage Waveforms and Related Control Signals

Fig. 3-12 (top) shows the measured waveforms of $V_{PT}$, $S_{R1}$, and $S_{R2}$ and their zoomed-in versions during voltage flipping. The $V_R$ is flipped from −4.7V to 3.63V, indicating 78% voltage flip efficiency ($\eta_F$). The voltage flipping is performed in 9 phases with $\Phi_a$, $\Phi_0$, and $\Phi_b$ switching signals, as shown in Fig. 3-12 (d), where the flipping moment for each phase is around 9μs. $S_{R1}$ ($S_{R2}$) switches from low to high (high to low) at the end of #2.

In Fig. 3-12 (c), the three voltages, $V_{R1P}$, $V_{R2P}$, and $V_{R3P}$, are the voltages on the positive plates of the three storage capacitors, $C_{R1}$, $C_{R2}$, and $C_{R3}$, respectively. Due to the limited number of oscilloscope probes, the three switch-controlling signals, $\Phi_a$, $\Phi_0$, and $\Phi_b$, are ORed and shown as the fourth signal at the bottom. When $V_{PT}$ is not being flipped, the capacitors are configured according to Con. I in Fig. 3-4 and the measured voltage of $V_{R1P}$, $V_{R2P}$ and $V_{R3P}$ are 4V, 3.2V, and 2.4V, respectively, as shown in Fig. 3-12 (c). This indicates that the voltages across the three storage capacitors, $C_{R1}$, $C_{R2}$, and $C_{R3}$, are 0.8V, 0.8V, and 2.4V, with a voltage ratio of 1:1:3, which accurately matches their designed capacitance ratio of 3:3:1. The zoomed-in voltage flipping moment is shown in Fig. 3-12 (d), where the phases #1-#9 correspond to the phases #1-#9 in Fig. 3-3.

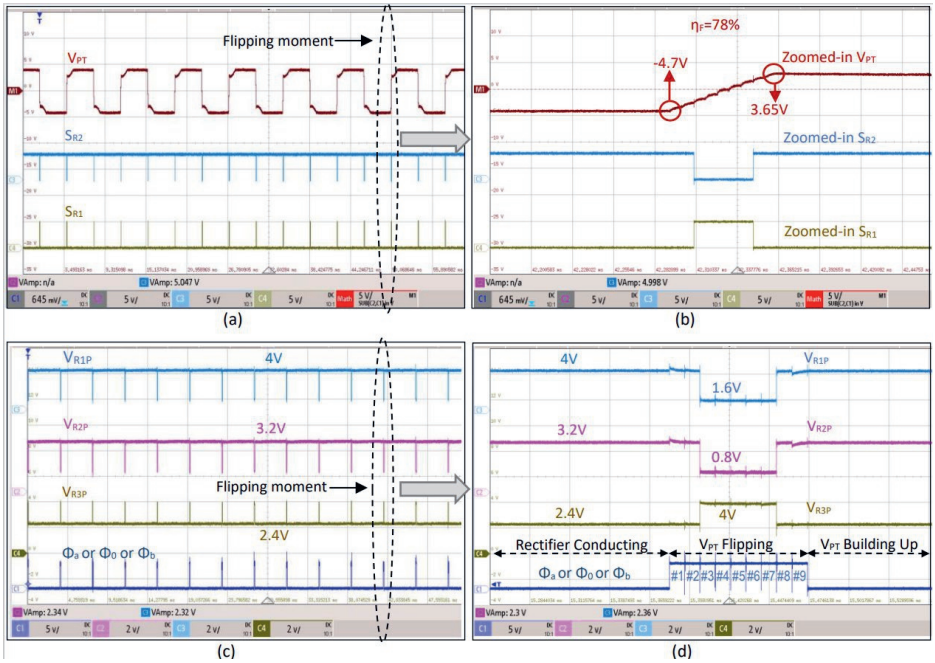



Fig. 3-12. Measured waveform: (a) $V_{PT}$ and switch control signals $S_{R2}$ and $S_{R1}$, and (b) their zoomed-in versions during flipping moment, (c) voltage at positive plates of three storage capacitors, $V_{R1P}$, $V_{R2P}$, $V_{R3P}$, and ORed version of flipping signals, OR($\Phi_a$, $\Phi_0$, $\Phi_b$), and (d) their zoomed-in versions during flipping moment.

During phases #1, #2, #8, and #9, the storage capacitors follow the same connection as in the energy harvesting state: Con. I in Fig. 3-4 (a). Therefore, the voltage levels at the positive plates of $V_{R1P}$, $V_{R2P}$, and $V_{R3P}$ are 4V, 3.2V, and 2.4V, respectively, as in the rectifier conducting state. During phases #3, #4, #3, #6, and #7, the connection of three storage capacitors is reconfigured from Con. I to Con. II (Fig. 3-4 (a)). Thus, the positive plate voltages of $V_{R1P}$, $V_{R2P}$, and $V_{R3P}$ are changed to 1.6V, 0.8V, and 4V since the ground is now temporarily connected to the bottom plate of $C_{R2}$ instead of $C_{R3}$. However, the voltages across $C_{R1}$, $C_{R2}$, and $C_{R3}$ maintain their values: 0.8V, 0.8V, and 2.4V.

Fig. 3-13 presents the rectified output voltage, $V_R$, with 3V open circuit voltage amplitude from the PT ($V_{OC}$) and 78% flip efficiency ($\eta_F$). To verify that the proposed SSHSC rectifier can adopt storage capacitors with different sizes and that the voltage ratio is not affected by the inevitable inherent leakage in the capacitors over a long

time of operation, two sets of storage capacitors are chosen as $C_{R1}$, $C_{R2}$, and $C_{R3}$: (1) 10μF, 10μF and 3.3μF, and (2) 100μF, 100μF and 33μF. All the capacitors have the same SMD package: 0803 (2012 Metric). Smaller SMD packages generally have smaller maximum capacitances. Since the optimal $C_R$ is application dependent, the proposed technique may require higher overall capacitance, leading to the use of larger SMD packages and increasing volume. Fig. 3-13 (a) shows the output voltage for the capacitor set (1), as $V_R$ is charged from 0V to 4.7V. During the cold start-up period, $V_R$ exhibits some fluctuations due to the weak gate-driving voltage of the switches controlled by $S_{R1}$ and $S_{R2}$. After start-up, the SSHSC rectifier is engaged, and the $V_R$ increases faster. The spikes of the $V_R$ are caused by the switching moment of $S_{R1}$ and $S_{R2}$ due to the temporary disconnection to the ground, which will be fully recovered in 1−2ns. The bottom plate effect is negligible since the three storage capacitors are off-chip implemented. When the capacitance of the storage capacitors is increased by 10× larger with the capacitor set (2), the measured rectified voltage, $V_R$, is shown in Fig. 3-13 (b). It has a similar waveform as Fig. 3-13 (a), indicating that the steady-state rectified voltage and flipping operation are not affected as long as the three storage capacitors have a ratio of 3:3:1. However, with the larger capacitor set, a longer time is needed to build up $V_R$.

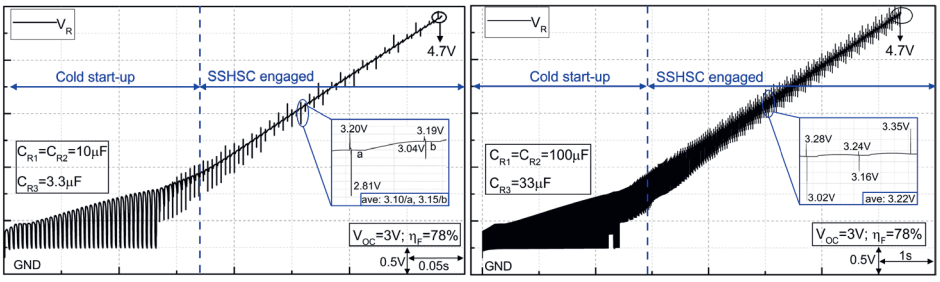



Fig. 3-13. Measured output voltage, $V_R$, with different storage capacitor sets: (a) $C_{R1} = C_{R2} =$ 10μF and $C_{R3} = 3.3$μF; (b) $C_{R1} = C_{R2} = 100$μF and $C_{R3} = 33$μF.

### 3.5.3 Output Performance Analysis

The measured output power from the proposed SSHSC rectifier and FBR is shown in Fig. 3-14 left. The proposed SSHSC rectifier generates a maximum of 72µW and 130µW with $V_{OC}$ = 2V and $V_{OC}$ = 3V, respectively, while the FBR can only generate 9.3µW. The proposed SSHSC rectifier achieves 7.38× maximum power enhancement compared to an FBR with the same input condition at $V_{OC}$ = 2V. The rectified power in a range of $V_{OC}$ is presented in Fig. 3-14 right. The measured maximum power from the proposed SSHSC rectifier is 289.3µW when $V_{OC}$ is 6V.

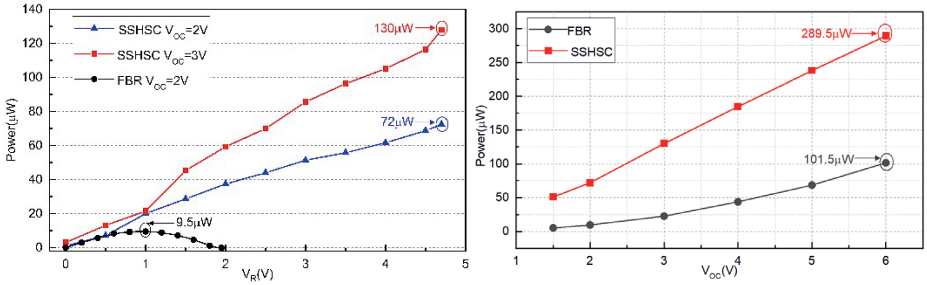



Fig. 3-14. Measured output power of the proposed SSHSC rectifier and an FBR for output voltage $V_R$ varying between 0V and 4.73V (left) and open circuit voltage $V_{OC}$ varying between 1.3V and 6V (right).

A comparison between the proposed SSHSC rectifier and the state-of-the-art is presented in Table 3-1. For a large commercial PT with a 22nF-$C_P$, the proposed SSHSC rectifier uses three off-chip storage capacitors for voltage flipping instead of additional flying inductors or capacitors. As a result, it is the smallest active rectifier design, with a compact area of 0.18mm$^2$. The measured power consumption of the chip is 0.37µW. The SSHSC rectifier has the highest output power enhancement of 7.38× compared to a conventional FBR. This work also has the smallest volume for the off-chip components compared with other SSHI or typical SSHC rectifiers, thanks to the proposed capacitor-sharing technique.

Table 3-1: Performance comparison with previous work.

| | ISSCC'16 [3-4] | JSSC'17 [3-2] | JSSC'17 [3-6] | ISSCC'19 [3-7] | JSSC'19 [3-5] | JSSC'22 [3-8] | **This work [3-1]** |
|---|---|---|---|---|---|---|---|
| Technology | 0.35μm | 0.35μm | 0.18μm | 0.18μm | 0.18μm | 0.18μm | **0.18μm** |
| Technique | P-SSHI | SSHC | FCR | SPFCR | SSHI | Inductive | **SSHSC** |
| PT Type | Mide-V21BL | Mide-V21BL | P5A4E | PPA1021 | PPA1021/1022 | PPA1021 | **P-1803B** |
| $C_P$ | 26nF | 45nF | 80pF | 22nF | 14/22nF | 19nF | **22nF** |
| $V_{OC}$ | 2.45V | 2.5V | 1* | - | 1.5V | 1V | **2-3V** |
| Frequency | 134Hz/229Hz | 92Hz | 110KHz | 200Hz | 441/432Hz | 146Hz | **130Hz** |
| Dimension | 1.3mm$^2$ | 2.9mm$^2$ | 1.73mm$^2$ | 0.2mm$^2$ | 0.54mm$^2$ | 3.3mm$^2$ | **0.18mm$^2$** |
| Power Con-sumption | - | 1.7μW | 8.5μW | 4μW | 2μW | 0.75μW | **0.57μW** |
| $\eta_F$ | 89% | 80% | 85% | 84% | 79% | 69% | **78%** |
| Output Power | 21.4μW @1.25V | 161.8μW @2.5V | 50.2μW @1V | 64μW @0.19g | 100-120μW @2V | 10.2μW @1V | **130μW @3V** |
| $P_{IC}/P_{FBR}$ | 4.4× | 2.7×-9.7× | 4.83× | 6.5× | 4.48× | 3.68× | **7.58×** |
| Off-Chip Components | 1L+2C+2R | 9C | 1C | 5C | 1L+1C | 1L+1C | **3C** |

*: Estimated value; -: Not reported.

## 3.6 Conclusion

Conventional SSHI and SSHC rectifiers typically rely on large off-chip passive components to achieve efficient voltage flipping in piezoelectric energy harvesting (PEH) systems. SSHI rectifiers require bulky inductors, while SSHC rectifiers often need at least eight off-chip flying capacitors—especially when used with commercial PTs that have large intrinsic capacitance ($C_P$). Fully integrated SSHC solutions are limited to MEMS-based PTs with very small $C_P$ (in the sub-nanoFarad range), which restricts their output power and makes them less suitable for many IoT applications.

To address these limitations, a synchronized switch harvesting on shared capacitors (SSHSC) rectifier is proposed. This targets general-purpose PTs with large intrinsic capacitances and eliminates the need for dedicated flying capacitors. Instead, it reuses three storage capacitors, with a 3:3:1 capacitance ratio, as temporary flying capacitors during the voltage-flipping process. Measurement results demonstrate that the proposed SSHSC rectifier achieves a voltage flipping efficiency of 78% and a maximum output power of 289.3μW. Compared to a conventional full-bridge rectifier (FBR), the SSHSC rectifier delivers a 7.58× improvement in energy extraction, highlighting its potential for use in compact, high-efficiency energy harvesting systems.

## References

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# Chapter 4 A Bias-Flip Rectifier with Duty-Cycle-Based MPPT [2]

## 4.1 Introduction

In piezoelectric energy harvesting (PEH) systems, as discussed in Chapter 2.4, maximizing rectifier output power requires the use of maximum power point tracking (MPPT). Conventional MPPT techniques, such as the fractional open-circuit voltage (FOCV) [4-1][4-2][4-3][4-4], and perturb and observe (P&O) algorithms [4-5][4-6][4-7][4-8] have significant limitations, such as the need for open circuit voltage ($V_{OC}$) sampling, flipping efficiency ($\eta_F$) calibration, and complex power calculation. To address these challenges, this chapter introduces a duty-cycle-based (DCB) MPPT algorithm. By regulating the rectifier's conduction time at a fixed duty cycle, the DCB method eliminates the drawbacks of FOCV and P&O, offering a simpler, more accurate, and more robust MPPT solution.

## 4.2 Analysis of the Proposed DCB MPPT Algorithm

### 4.2.1 System Topology of the Proposed DCB MPPT

Fig. 4-1 shows the proposed DCB MPPT topology. The system has four key components: a synchronized switch harvesting on inductor (SSHI) rectifier, a DC-DC buck-boost converter, a cut-off (*CO*) signal sampler, and an MPPT controller. During operation, the rectifier alternates between conducting and cut-off states, producing a *CO* signal that indicates its current state. The duty cycle of this *CO* signal ($D_{CO}$) is a key metric for MPPT. When $D_{CO}$ is less than 50%, it suggests that the rectified voltage ($V_{REC}$) is below the MPP, and the DC-DC converter remains off, allowing $V_{REC}$ to rise. When $D_{CO}$ exceeds 50%, indicating $V_{REC}$ is above the MPP, the DC-DC converter is

[2] This chapter is based on the journal paper: X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa and S. Du, "A Bias-Flip Rectifier with Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 6, pp. 1771-1781, June 2024.

activated to transfer excess energy from $C_{REC}$ to the storage capacitor $C_S$, bringing the system back towards its optimal operating point.

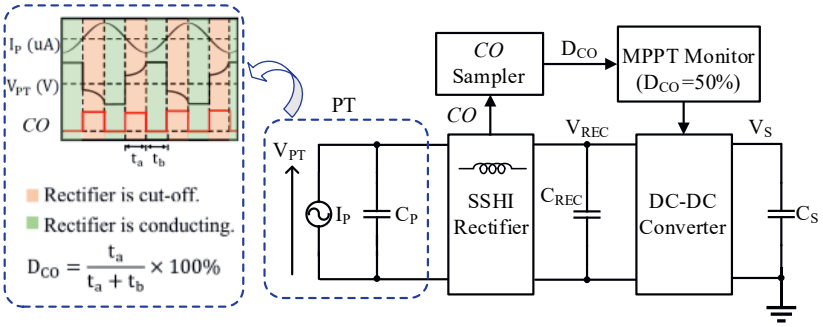


Fig. 4-1. Simplified diagram of the proposed DCB MPPT technique.

### 4.2.2 Theoretical Analysis of the Proposed DCB MPPT Algorithm

The proposed DCB MPPT algorithm exploits the relationship between the MPPT efficiency, $\eta_{MPPT}$, and the duty cycle of the rectifier's *CO* signal, $D_{CO}$ [4-9]. When a weakly coupled PT vibrates at its natural frequency, it can be modeled as a current source, $I_P$, in parallel with a capacitor, $C_P$. The current source, $I_P$, can then be expressed as [4-9]:

$$I_P = I_0 \sin(\omega t) \tag{4.1}$$

Where $I_0$ is the amplitude and ω is the excitation frequency.

The total generated charge, $Q_{total}$ from the PT, in a half vibration period, $\frac{T}{2}$, can be expressed by

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin(\omega t) dt = \frac{2I_0}{\omega} \tag{4.2}$$

The open circuit zero-to-peak voltage amplitude, $V_{OC}$, can be expressed as

$$V_{OC} = \frac{1}{2}\frac{Q_{total}}{C_P} = \frac{I_0}{\omega C_P} \tag{4.3}$$

Assuming that the diode voltage drop, $V_D$, of the bridge rectifier is zero, and noting $\eta_F$ as the voltage flipping efficiency of the bias-flip rectifier, the charge wasted in a half vibration period is

$$Q_{waste} = C_P V_{REC}(1 - \eta_F) \tag{4.4}$$

The remaining charge will flow into the output capacitor $C_{REC}$. This amount of charge, $Q_{SSH}$ can be expressed as

$$Q_{SSH} = Q_{total} - Q_{waste} = Q_{total} - C_P V_{REC}(1 - \eta_F) \tag{4.5}$$

By combining (4.2) and (4.4), the $Q_{SSH}$ can be written as

$$Q_{SSH} = C_P(2V_{OC} - V_{REC}(1 - \eta_F)) \tag{4.6}$$

The equation above shows the extracted charge in a half vibration period, T/2. Thus, the extracted power, $P_{SSH}$, for the active synchronized switch rectifier can be approximately written as

$$P_{SSH} = 2f_P C_P V_{REC}(2V_{OC} - V_{REC}(1 - \eta_F)) \tag{4.7}$$

When setting its derivative to $V_{REC}$ at 0, it can be found that the peak power at the maximum power point (MPP), $P_{MPP}$, is obtained as follows

$$P_{MPP} = \frac{2C_P f_P V_{OC}^2}{1-\eta_F} \tag{4.8}$$

By setting $\eta_{MPPT}$ as the MPPT efficiency, it is the ratio between actual output power, given by (4.7), and the peak power at MPP, given by (4.8). This is expressed as

$$\eta_{MPPT} = \frac{P_{SSH}}{P_{MPP}} \tag{4.9}$$

Substituting (4.7) and (4.8) into (4.9), this can be expressed as

$$\eta_{MPPT} = \frac{V_{REC}\times[2V_{OC}-V_{REC}(1-\eta_F)](1-\eta_F)}{V_{OC}^2} \tag{4.10}$$

Substituting (4.3) into (4.10), (4.10) can be rewritten as

$$\eta_{MPPT} = \frac{V_{REC}\times[2\frac{I_0}{\omega C_P}-V_{REC}\times(1-\eta_F)](1-\eta_F)}{[\frac{I_0}{\omega C_P}]^2} \tag{4.11}$$

(4.11) shows the MPPT efficiency of the rectifier for a given vibration amplitude, $I_0$ (or $V_{OC}$), and voltage bias-flip efficiency, $\eta_F$. We will then replace these two variables with the rectifier cut-off duty cycle.

We define $D_{CO}$ as the cut-off duty cycle of the rectifier, as shown on the left of Fig. 4-1. During the cut-off period, some charge will be wasted to build up the PT voltage. We define $t_{off}$ as the cut-off time (the same as $t_a$ in Fig. 4-1), and $t_{on}$ (the same as $t_b$ in Fig. 4-1) denotes the conducting time of the rectifier in a half-vibration period. Assuming the bias-flip operation happens exactly at the zero-crossing moment of the current source $I_P$, the total wasted charge $Q_{waste}$ in the cut-off time can be written as

$$Q_{waste} = \int_0^{t_{off}} I_0 \sin(\omega t)dt \tag{4.12}$$

Considering that the duty cycle $D_{CO} = \frac{t_{off}}{t_{on}+t_{off}}$ and the half cycle is expressed by $t_{on} + t_{off} = \frac{T}{2}$, $t_{off}$ can be written as

$$t_{off} = D_{CO} \times (t_{on} + t_{off}) = \frac{D_{CO}T}{2} \tag{4.13}$$

Substituting (4.13) into (4.12), (4.12) can be written as

$$Q_{waste} = \int_0^{t_{off}} I_0 \sin(\omega t)dt = \int_0^{\frac{D_{CO}T}{2}} I_0 \sin(\omega t)dt = \frac{I_0}{\omega}(1-\cos(\pi D_{CO})) \tag{4.14}$$

While (4.4) gives the wasted charge in a half period from the perspective of the rectifier output, (4.14) gives the same wasted charge from the perspective of the input. Combining (4.4) and (4.14), we have

$$V_{REC}(1-\eta_F) = \frac{I_0(1-\cos(\pi D_{CO}))}{\omega C_P} \tag{4.15}$$

Substituting (4.15) into (4.11), the $\eta_{MPPT}$ can be rewritten as

$$\eta_{MPPT} = \frac{2\frac{I_0}{\omega}(1-\cos(\pi D_{CO}))\times I_0}{\frac{\omega}{\left(\frac{I_0}{\omega}\right)^2}} - \frac{\left[\frac{I_0}{\omega}(1-\cos(\pi D_{CO}))\right]^2}{\left(\frac{I_0}{\omega}\right)^2}$$

$$= 2\times(1-\cos(\pi D_{CO})) - [1-\cos(\pi D_{CO})]^2 \tag{4.16}$$

After simplification, (4.16) can be expressed as

$$\eta_{MPPT}(D_{CO}) = 1 - cos^2(\pi D_{CO}) \tag{4.17}$$

By setting the derivative of (4.17) to 0, we find that the MPPT efficiency will be theoretically 100% when $D_{CO}$ = 50%. This can also be seen by plotting the MPPT efficiency versus $D_{CO,}$ shown in Fig. 4-2. This relation between the MPPT efficiency and the rectifier cut-off duty cycle provides a clean and simple way to achieve MPPT in piezoelectric energy harvesting. Unlike conventional FOCV and P&O algorithms, the proposed DCB algorithm only needs to regulate $D_{CO}$ at 50% without considering the vibration amplitude $V_{OC}$ or voltage flip efficiency $\eta_F$. Moreover, due to the squared cosine relationship, it is robust to sensing errors in $D_{CO}$. For instance, with a ±5% error in $D_{CO}$, the MPPT efficiency $\eta_{MPPT}$ remains above 97%, as illustrated in Fig. 4-2.

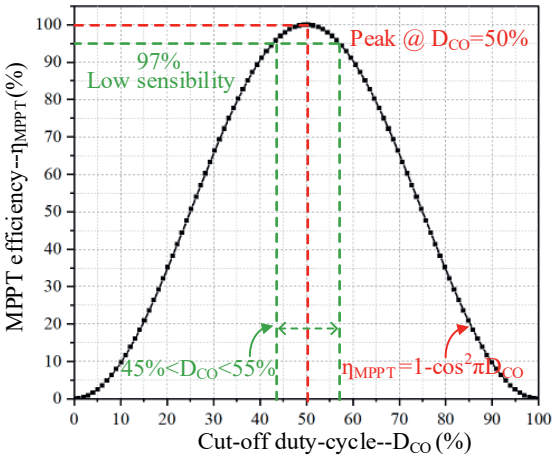


Fig. 4-2. The equation plotting of the MPPT efficiency as a function of the cut-off duty cycle.

## 4.3 Proposed DCB MPPT Technique

### 4.3.1 System Flowchart

The flowchart of the proposed DCB MPPT technique is shown in Fig. 4-3. It begins by sampling the duty cycle, $D_{CO}$, during every *CO* period. If the measured $D_{CO}$ < 50%, energy harvested by the PT charges the rectifier output capacitor $C_{REC}$, thus increasing its voltage, $V_{REC}$, towards the MPP, resulting in an increasing $D_{CO}$. Conversely, if the measured $D_{CO} \geq$ 50%, this means that $V_{REC}$ is equal to or exceeds the $V_{MPP}$. Consequently, some of the energy stored in $C_{REC}$ is transferred to the storage capacitor $C_S$ via a DC-DC buck-boost converter to maintain $V_{REC}$ around $V_{MPP}$ by regulating $D_{CO}$ to around 50%. The DC-DC converter operation is shown on the right of Fig. 4-3. Initially, a slightly lower voltage level, denoted as $V_{RECS}$, is set as the lower threshold of the hysteresis window for $V_{REC}$. The energy conversion process involves two steps: first, dumping the energy from the rectified capacitor, $C_{REC}$, to the sharing inductor, $L_M$, and then it is subsequently transferred from $L_M$ to the storage capacitor $C_S$. The buck-boost conversion operates for multiple cycles until $V_{REC} < V_{RECS}$. An on-chip oscillator (*OSC*) clocks the energy transfer timing to prevent a large current flow

through the inductor. This flow repeats until the next time when $D_{CO}$ exceeds 50%, thereby achieving MPPT.

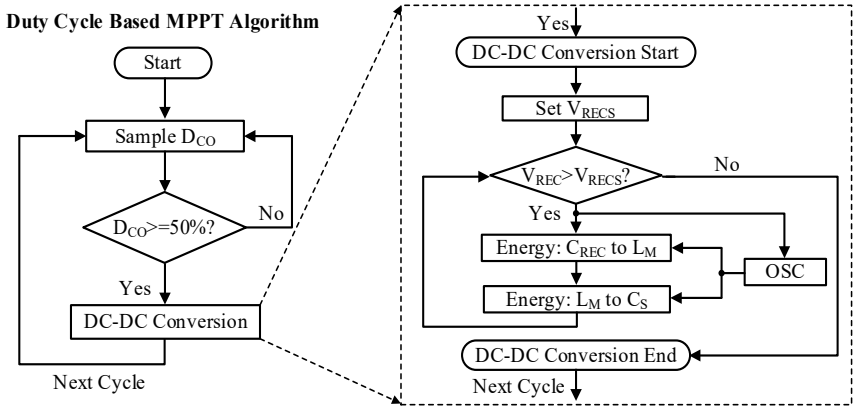


Fig. 4-3. The working flow of the proposed DCB MPPT system.

### 4.3.2 System Architecture

The proposed system architecture comprises an SSHI rectifier with its dedicated control block, a buck-boost DC-DC converter, and an MPPT controller, as shown in Fig. 4-4. The SSHI rectifier comprises an FBR, an active diode, and an off-chip inductor, $L_{M,}$ shared with the buck-boost DC-DC converter. When there is a need to flip the voltage across the PT ($V_{PT}$), the bridge rectifier switches from the conducting mode to the cut-off mode; this transition causes the *CO* signal to have a rising edge, which is utilized to generate an SSHI flipping pulse through the control logic I and pulse generation block. The *CO* signal is first processed by the control logic I block to generate a stable synchronized signal, *SYN*. During the DC-DC conversion period, the *SYN* is affected by the MPPT ending signal, referred to as *END*. When the *END* signal is high, the *SYN* remains low and disables the pulse generation block. The generation and explanation of the *END* signal are presented in Fig. 4-6, which will be explained in the next section. The pulse generation block generates a pulse when the *SYN* signal experiences a rising edge. Following the level shifters, the resulting pulse, denoted as $\Phi$, briefly connects $L_M$ across the PT, initiating a closed RLC loop to flip

the PT voltage, $V_{PT}$. The MAX block selects a higher voltage to serve as the power supply for the level shifters.

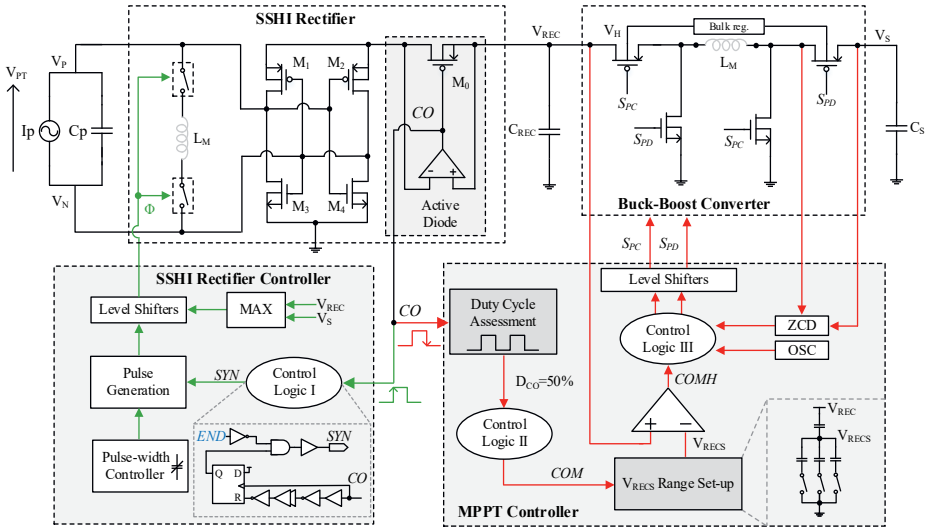


Fig. 4-4. The system architecture of an SSHI rectifier with the proposed DCB MPPT technique.

In addition to its usage in the control of the SSHI rectifier, the *CO* signal is also transmitted to the MPPT controller, as illustrated on the right side of Fig. 4-4. The falling edge of the *CO* triggers the MPPT controller to avoid the conflict between the two blocks. The MPPT controller consists of seven main blocks: a duty cycle assessment block, two control logic blocks, a $V_{RECS}$ range set-up block, a zero-crossing detection (*ZCD*) block, an on-chip oscillator (*OSC*), and level shifters.

The duty cycle $D_{CO}$ is measured by a duty cycle assessment block and fed to the control logic II. If $D_{CO}$ exceeds 50%, a *COM* signal is generated through the control logic II and sent to a $V_{RECS}$ range set-up block. To prevent $V_{REC}$ from dropping excessively, a hysteresis window is established with a lower voltage threshold, $V_{RECS}$, which is a fraction of the initial rectified voltage $V_{REC}$. The upper hysteresis threshold is automatically set to $V_{MPP}$ based on $D_{CO}$ = 50%, eliminating the need for an explicit voltage threshold. The $V_{RECS}$ range set-up block, implemented as a capacitor array, will be described in the circuit implementation section. The rectified voltage $V_{REC}$ and

sampled low hysteresis $V_{RECS}$ are compared to generate a signal, *COMH*, fed to the control logic III block. This block combines the outputs of an on-chip *OSC* and a *ZCD* block. The *ZCD* block prevents the reverse current while transferring the energy from $L_M$ to $C_S$. After passing through the level shifters, the switching signals $S_{PD}$ and $S_{PC}$ control the buck-boost DC-DC converter. The buck-boost converter uses the shared inductor, $L_{M,}$ to transfer DC energy from $C_{REC}$ to $C_S$ in multiple steps, following the same process as introduced in the flowchart of the DC-DC conversion process in Fig. 4-3. Therefore, the MPPT is achieved by regulating the duty cycle, $D_{CO}$ at 50%.

## 4.4 Circuit Implementations

### 4.4.1 Circuit Diagram of the MPPT Controller Block

Fig. 4-5 illustrates the MPPT controller block. In the duty cycle sampler block, the duty cycle, $D_{CO}$, is sensed using two equal on-chip capacitors, $C_{RGL}$ and $C_{RGR}$, as shown in the top-left of Fig. 4-5. When *CO* is high, $C_{RGL}$ is charged by an on-chip current source, $I_{RG}$, to $V_H$, while $C_{RGR}$ is charged to $V_L$ when *CO* is low. To cope with a wide range of PT vibration frequencies, which is half of the *CO* frequency, $C_{RGL}$ and $C_{RGR}$ can be adjusted in 8 steps between 5.4pF and 42.4pF. The resulting $V_H$ and $V_L$ voltages are compared to generate the *PO* signal, indicating the $D_{CO}$ polarity around the 50% target. *PO* stays low when $D_{CO} \geq 50\%$; otherwise, a pulse is generated. The $C_{RGL}$ and $C_{RGR}$ are reset by a short pulse, $S_{CV}$, at the end of each *CO* period. When *PO* stays low, meaning that $D_{CO}$ exceeds 50% (or $V_{REC}$ exceeds $V_{MPP}$), a DC-DC enable signal, *COM*, is generated to start the DC-DC conversion. The lower hysteresis threshold, $V_{RECS}$, is generated by a switched capacitor voltage divider. In this design, $V_{RECS}$ can be regulated from $97\% \times V_{REC}$ to $99.5\% \times V_{REC}$ by tuning $ex_1$, $ex_2$, and $ex_4$ to adjust the ripple of $V_{REC}$ during DC-DC conversion. The rectified voltage $V_{REC}$ and its low hysteresis voltage are compared to generate a *COMH* signal, which turns to high when $V_{REC} < V_{RECS}$. Control logic III generates the DC-DC conversion control signals through the level shifters to drive the switches in the DC-DC conversion loop by

combining *COMH* and other signals generated by the *OSC* and *ZCD* blocks. Further details about the circuitry of control logic III will be presented in the following.

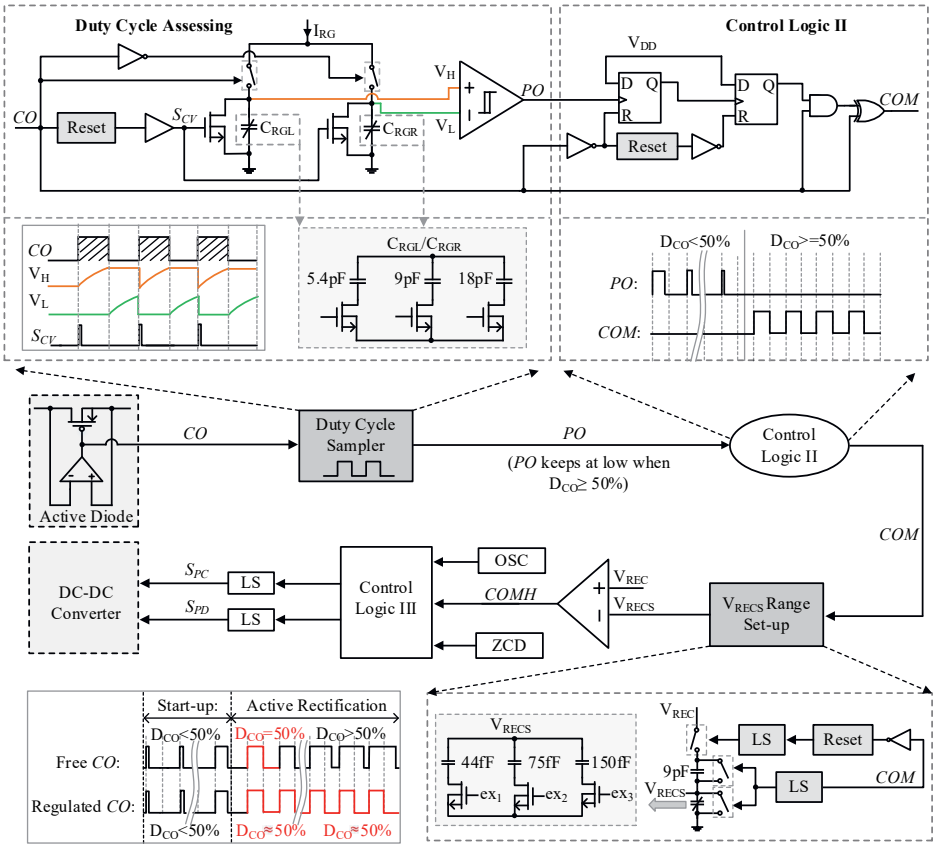


Fig. 4-5. Detailed circuit diagrams of the MPPT controller block.

### 4.4.2 Circuit Details of the Control Logic III Block

The detailed circuit implementation of the control logic III block is shown in Fig. 4-6. It combines the output signals of *OSC*, *ZCD*, *CO*, and *COMH* together to generate two DC-DC conversion control signals, $S_{PC}$ and $S_{PD}$. On top of Fig. 4-6, the zero-crossing detection (ZCD) compares the voltages between the switch, which connects the right end of the inductor $L_M$ and storage capacitor $C_S$, to prevent the reverse current flowing out of $C_S$. When the voltage of the left end of the switch is lower than the

right point, a DC-DC conversion stopping signal, *STD*, will generate a rising edge. This process repeats in every energy dumping period between $L_M$ and $C_S$. The MPPT ending signal, *END*, is affected by *STD*, *COMH*, and *CO*, indicating that the results of *ZCD* decide the MPPT period, the DC-DC rectified low window voltage of MPPT, and the cut-off duty cycle, respectively. When the *END* generates a rising edge, it means that DC-DC conversion in the current MPPT period has finished and will be restarted until the next MPPT comes.

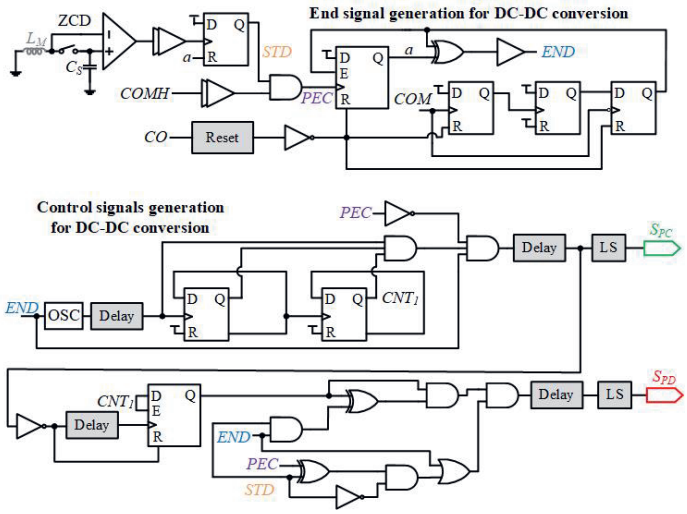


Fig. 4-6. Circuit diagram of the Control Logic III block.

The bottom of Fig. 4-6 shows how the DC-DC converter control signal, $S_{PC}$, and $S_{PD}$ are generated. Its ending time is mainly decided by the *END* signal and clocked by an on-chip oscillator, *OSC*. Through the level shifters, the $S_{PC}$ and $S_{PD}$ are finally generated. The $S_{PC}$ controls the time of dumping energy from the rectified capacitor $C_{REC}$ to the inductor. $S_{PD}$ is the time for the inductor to dump energy into the storage capacitor. The $S_{PC}$ is shorter than $S_{PD}$, and both are determined by the oscillator and a counter's signal, $CNT_1$, as shown in Fig. 4-6.

### 4.4.3 Biasing Current Generation

As shown in Fig. 4-7, an on-chip constant-Gm biasing circuit is used to provide a stable bias current across process corners and variations [4-10]. Transistors $M_5$ and $M_7$ (with a 1:4 W/L ratio) are biased in weak-inversion to establish a well-defined $\Delta V_{GS}$ across a resistor $R_b$. An auxiliary amplifier, consisting of a common-source stage ($M_3$) with a diode-connected load ($M_4$), equalizes the $V_{DS}$ of $M_6/M_8$, making the bias circuit less sensitive to power supply fluctuations [4-11]. To enable more current options, the biasing resistor $R_b$ can be tuned from 1MΩ to 5MΩ in 1MΩ steps. The start-up circuitry on the left prevents the circuit from settling into a zero-current state. Finally, the output stage provides stable biasing currents for the load circuits.

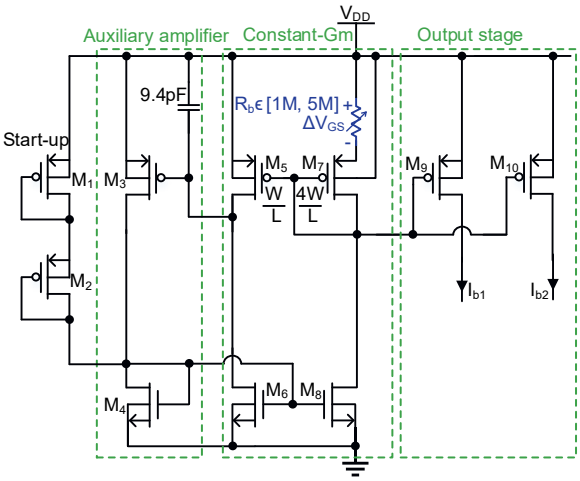


Fig. 4-7. Biasing current generation for the system.

## 4.5 Measurement Results

### 4.5.1 Measurement Setup

The experimental setup and a chip micrograph are shown in Fig. 4-8. The proposed circuit was fabricated in a 180-nm BCD process with an active area of 0.47mm$^2$. The chip contains seven main blocks: a tunable $D_{CO}$ sampling block, a power supply selector, a DC-DC converter, level shifters, a bias current generation

block, an SSHI rectifier, and a tunable $V_{RECS}$ generation block. The chip was tested with a 43nF commercial PT (PEH-S128-H5FR-1107YB), which was installed on a shaker (LDS V450) and excited at a resonance frequency of 240Hz during the experiments.

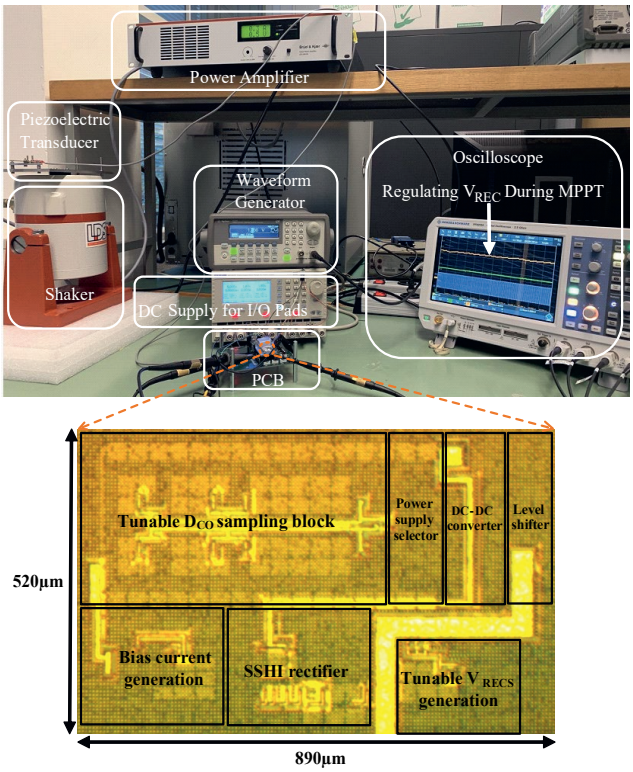


Fig. 4-8. Experimental setup in the Lab and chip microphoto.

### 4.5.2 Measured Waveforms During the MPPT Transient Time

Fig. 4-9 shows the measured waveform of $V_S$ and $V_{REC}$. The system starts from the cold state with a vibration excitation level equivalent to $V_{OC}$ =1.5V. An inductor of $L_M$ = 27µH is employed. In the beginning, $V_{REC}$ increases steadily because the initial duty cycle $D_{CO}$ is less than 50%, and the DC-DC converter is disabled. Once $V_{REC}$ reaches the first optimal voltage according to MPP, $V_{MPP1}$ (around 2.6V), $D_{CO}$ achieves 50%. The DC-DC converter then enables the MPPT controller to regulate

$D_{CO}$ at 50% (or $V_{REC}$ at 2.6V) during the $MPPT_1$ period by transferring the extra harvested energy to $C_S$. This DC-DC conversion results in a rising $V_S$. To observe the tracking ability of the proposed MPPT technique with varying $V_{OC}$, the vibration excitation level is increased to $V_{OC}$ = 2V. As expected, $V_{REC}$ increases to track the higher MPP due to the larger excitation. This is because $D_{CO}$ becomes less than 50% once $V_{OC}$ is increased, which makes the system regulate $D_{CO}$ back to 50%. To achieve this, the DC-DC converter is disabled to let $V_{REC}$ increase until $D_{CO}$ reaches 50% again. This indicates that the proposed circuit can sense the vibration excitation variation by measuring $D_{CO}$ in only a half vibration cycle after the variation occurs and start to track the new MPP. Once $D_{CO}$ reaches 50% again, which means $V_{REC}$ achieves the new MPP, the DC-DC converter starts to operate to maintain $V_{REC}$ at this new MPP by regulating $D_{CO}$ at 50%. The new MPPT period at this higher excitation level is labeled as $MPPT_2$.

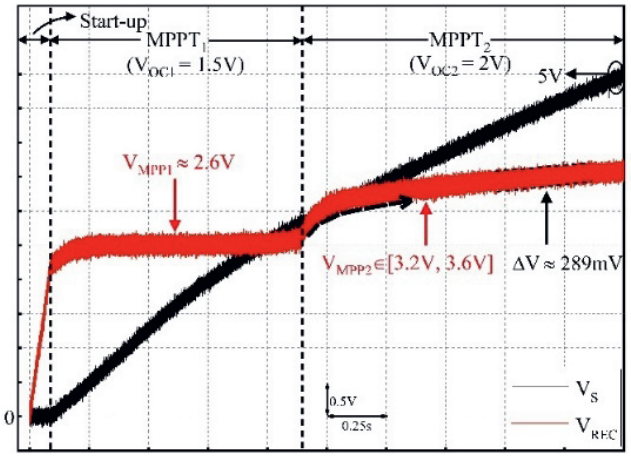


Fig. 4-9. Measured waveform of $V_S$ and $V_{REC}$ during the MPPT transient time with input 1.5-V and 2-V $V_{OC}$.

The slightly increased slope of $V_{MPP2}$ during the $MPPT_2$ period is because the voltage $V_S$ that powers the bias-flip switches is replaced by $V_{REC}$ when $V_S > V_{REC}$. The MAX block in Fig. 4-4 selects a higher voltage for the power supply of the level shifters, which lowers the conducting resistance of the bias-flip switches. This slightly increases the voltage flipping efficiency and, consequently, the optimal rectified

voltage $V_{MPP}$ increases, as explained by the equation: $V_{MPP} = \frac{V_{OC}}{1-\eta_F}$. These observations indicate that the proposed DCB MPPT algorithm can automatically track the MPP regardless of system and environmental parameters. The convergence time of MPPT is mainly affected by the capacitance of $C_{REC}$; the larger the $C_{REC}$ is, the longer the convergence time is needed. The $V_{REC}$ voltage ripple during MPPT is around 289mV, which can be configured by adjusting the hysteresis window.

The zoomed-in $V_{REC}$ during the $MPPT_2$ period is picked up in Fig. 4-10. The $V_{REC}$ stabilizes at approximately 3.42V. To prevent excessive voltage drop, $V_{REC}$ is gradually reduced in multiple DC-DC conversion steps. Each DC-DC working period consists of two phases, controlled by signals $S_{PC}$ and $S_{PD}$. These signals regulate the charging time from $C_{REC}$ to $L_M$ and $L_M$ to $C_S$, respectively. Control logic III, illustrated in Fig. 4-6, generates the $S_{PC}$ and $S_{PD}$ signals. In the bottom part of Fig. 4-10, the duration of $S_{PC}$ is shown to be approximately 1.4μs. This timing control ensures the suitable charging of the different components within the DC-DC conversion process.

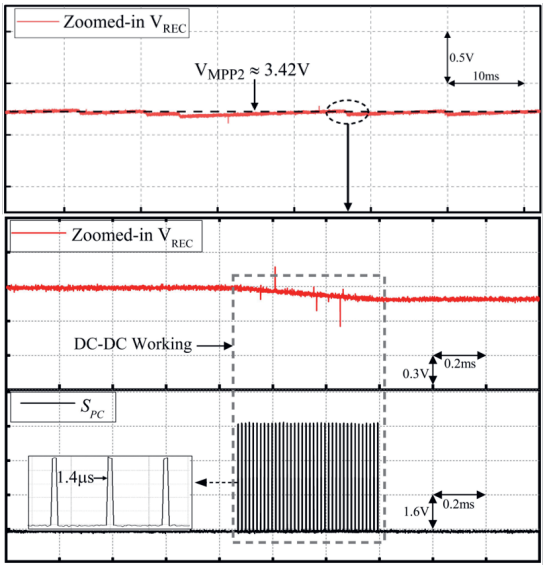


Fig. 4-10. Zoomed-in waveform of $V_{REC}$, $S_{PC}$ of a DC-DC conversion moment during MPPT.

### 4.5.3 Measured PT Voltage and *CO* Signal

Fig. 4-11 presents the measured PT voltage, $V_{PT}$. The amplitude of $V_{PT}$ aligns with $V_{REC}$ depicted in Fig. 4-9. When $V_{OC}$ is increased from 1.5V to 2V, the MPPT process is reflected by the $V_{PT}$ shown in the zoomed-in waveform at the bottom. In this specific measurement scenario, $C_{REC}$ is 10μF. It takes approximately 0.2s for the system to achieve the new MPP after the $V_{OC}$ changes. Less time is needed if a smaller $C_{REC}$ is used. The peak-to-peak value of $V_{PT}$ has changed from 5.2V to 6.4V due to the increase in $C_{REC}$.

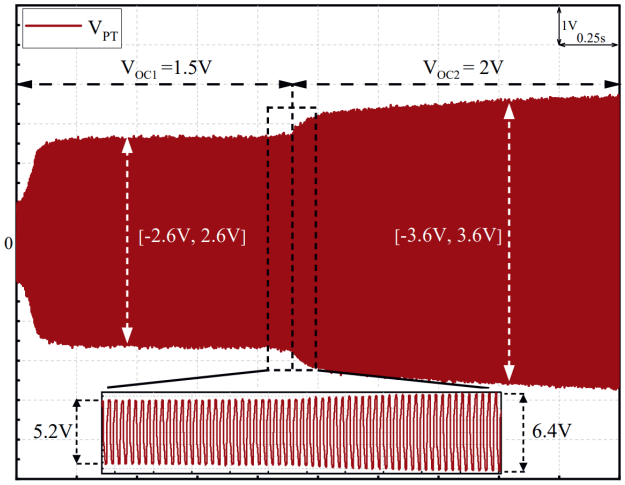


Fig. 4-11. Measured waveform of $V_{PT}$ during the MPPT transient time.

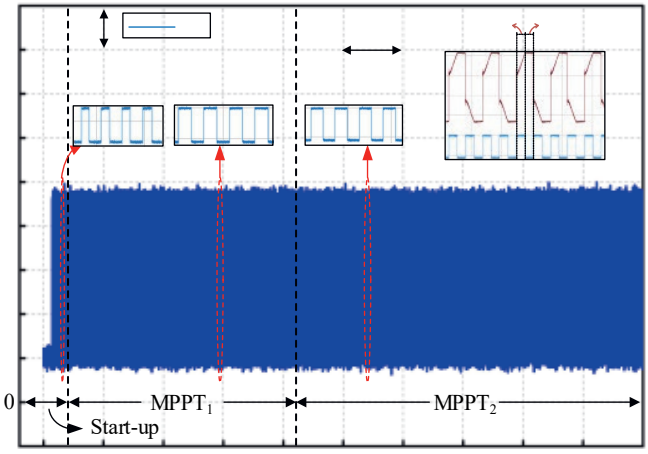


Fig. 4-12. Measured cut-off signal *CO* during the transient time.

Fig. 4-12 shows the cut-off signal, *CO*. During the start-up period, the duty cycle of *CO*, $D_{CO}$, is less than 50%. As $D_{CO}$ approaches 50%, the maximum power point (MPP) is getting closer. In the $MPPT_1$ period, the $D_{CO}$ is around 49.98%; in $MPPT_2$, the $D_{CO}$ is around 50.19%. Both values are very close to 50%. The top right sub-figure zooms in on the waveforms of $V_{PT}$ and *CO*. It demonstrates that when *CO* is high, the rectifier is in a cut-off state, and $V_{PT}$ gradually builds up. When *CO* switches to low, $V_{PT}$ is clamped at $V_{REC}$, indicating the onset of the conducting state. Therefore, 50% denotes the rectifier's on/off time ratio, which is also reflected by the waveform of $V_{PT}$.

### 4.5.4 Performance Analysis

Fig. 4-13 presents the measured output power of the SSHI rectifier as a function of $D_{CO}$. It can be observed that the output power varies with different duty cycles and reaches a peak at an optimal duty cycle. The measured optimal $D_{CO}$ of the peak power of the SSHI rectifier is 48.52% and 47.58% for $V_{OC}$ = 1.5V and $V_{OC}$ = 2V, respectively, slightly lower than the theoretical value of 50%. The shift in the optimal duty cycle from 50% to a slightly lower value is primarily caused by the active rectifier's non-zero voltage drop and the *CO* signal's inaccuracy. Despite the actual duty cycle not being exactly 50%, this work still adopts 50% as the regulation target. By regulating

$D_{CO}$ at 50%, the measured MPPT efficiencies for the two measurement conditions are 99.9% and 99.7%, close to the peaks at 48.52% and 47.58% duty cycle, respectively. This indicates that the DCB MPPT technique exhibits strong robustness to errors in the duty cycle ($D_{CO}$), consistent with the analysis shown in Fig. 4-2 based on the cosine-squared relationship. The measured output power values of the SSHI rectifier at $V_{OC}$ =1.5V and $V_{OC}$ =2V are 69.9μW and 124.9μW, respectively.

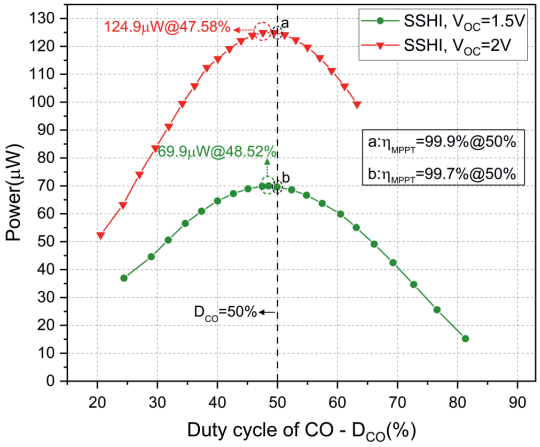


Fig. 4-13. The output power of an SSHI rectifier versus the duty cycle, $D_{CO}$.

Since the optimal MPPT efficiency is only related to the $D_{OC}$, to verify that the proposed DCB MPPT technique is independent of voltage flipping efficiency, $\eta_F$, and open-circuit voltage amplitude, $V_{OC}$, Fig. 4-14 shows the MPPT efficiency over different $\eta_F$ and $V_{OC}$ by changing the off-chip inductor and vibration excitation level. The range of flipping efficiency spans from 20% to 60%, with a step size of 10%. The peak MPPT efficiency reaches 97%, and the average value remains around 96% for high flipping efficiency values. In the second sub-figure, the $V_{OC}$ varies from 1.2V to 2V with a step size of 0.2V. The highest MPPT efficiency is achieved at 98% when $V_{OC}$ = 1V. These results demonstrate that the DCB MPPT technique is independent of varying flipping efficiency $\eta_F$ and open circuit voltage $V_{OC}$, and it maintains a high tracking efficiency in large variation ranges of $\eta_F$ and $V_{OC}$. Due to process limitations (maximum device breakdown voltage at 5V), $V_{OC}$ and $\eta_F$ cannot be set too high,

according to the relationship $V_{MPP} = \frac{V_{OC}}{1-\eta_F}$, since they could push $V_{MPP}$ above 5V, the process cannot achieve the MPP. For measurements in a wider range of $V_{OC}$ and $\eta_F$, a process with high-voltage devices or off-chip high-voltage switches can be used in future works.

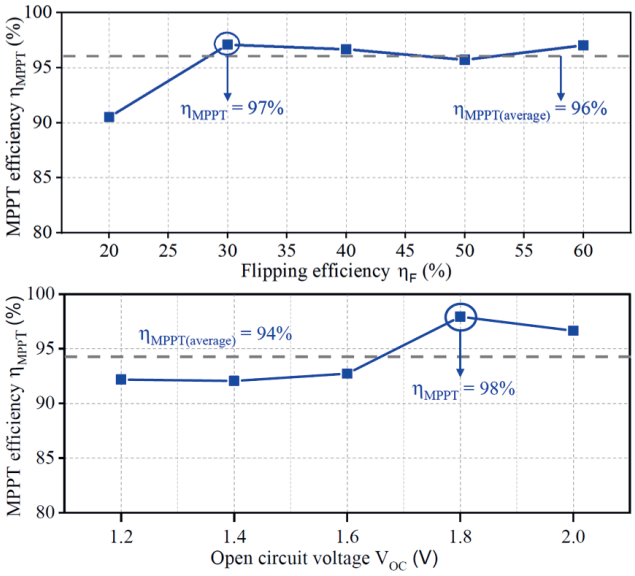


Fig. 4-14. MPPT efficiency versus $\eta_F$ and $V_{OC}$.

Fig. 4-15 shows the true optimal $D_{CO}$ in wide ranges of $\eta_F$ and $V_{OC}$. To obtain the true optimal $D_{CO}$ values, the MPPT block is disabled, and the system operates solely as an SSHI rectifier. In this way, the rectified output power can be measured in a range of $V_{REC}$ to find the peak, and the true optimal $D_{CO}$ can be calculated from the *CO* signal at the power peak. The two sub-figures show that the true optimal $D_{CO}$ values remain close to 50% regardless of $\eta_F$ and $V_{OC}$. The worst-case $D_{CO}$ values are 48.10% at $\eta_F$ = 60% and 48.89% at $V_{OC}$ = 1.4V. However, this deviation has a minimal impact on the actual peak MPPT efficiency due to the robustness of the proposed MPPT algorithm against $D_{CO}$ errors. Therefore, even when regulating the $D_{CO}$ always at 50%, the peak MPPT efficiency can still be very high, demonstrating the effectiveness of the proposed MPPT algorithm and its ability to tolerate $D_{CO}$ errors.

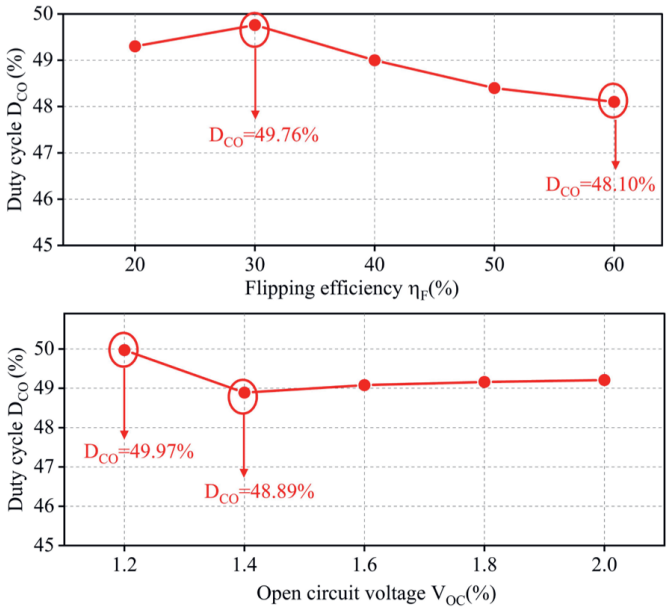


Fig. 4-15. The true optimal duty cycle for different $\eta_F$ and $V_{OC}$.

Fig. 4-16 shows the output power of the FBR and SSHI rectifier for different rectified voltage levels. The measurements are conducted with a fixed open circuit voltage amplitude $V_{OC}$ = 2V. The peak output power the FBR achieves is 36.9μW, with the corresponding $V_{MPP}$ around 1V. On the other hand, the SSHI rectifier, when configured with inductances of 27μH, 56μH, and 120μH, demonstrates significantly higher peak output powers of 124.9μW, 192μW, and 272.5μW, respectively. This figure clearly illustrates the remarkable improvement in output power achieved by the SSHI rectifier compared to the FBR. Specifically, the SSHI rectifier with 120μH inductance exhibits a 748% energy extraction enhancement compared to the FBR.

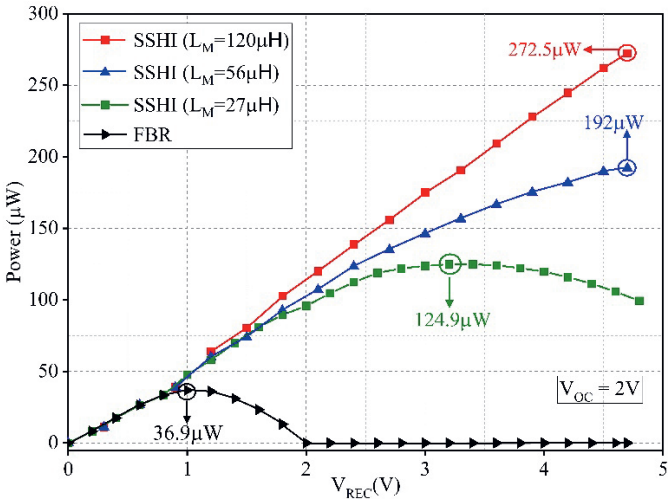


Fig. 4-16. The output power of FBR and SSHI rectifiers versus output voltage $V_{REC}$.

Table 4-1 compares the proposed DCB MPPT design and state-of-the-art MPPT techniques in energy harvesting systems. The previous works mainly focused on FOCV or P&O methods, while this work introduces the use of the duty cycle for MPPT. The DCB MPPT technique offers a simplified approach to achieving MPPT, as it is based on a straightforward equation and relies solely on the duty cycle of the rectifier. This translates into simpler circuit implementations, resulting in a compact chip area of only 0.47mm$^2$. It can enable continuous MPPT without the need for power-hungry sensors. This further simplifies the overall system design and reduces complexity. Furthermore, the proposed DCB MPPT design offers the advantage of very low quiescent current consumption at only 0.17μA. This low power requirement ensures minimal energy loss and maximizes system efficiency. Another noteworthy design aspect is its independence from the system and environmental parameters, such as $V_{OC}$ and $\eta_F$. This makes the DCB MPPT technique versatile and adaptable to different energy harvesting scenarios without extensive parameter tuning. It boasts a flipping efficiency of 82% and 98% peak MPPT efficiency. The DCB MPPT design offers a 748% power extraction enhancement compared to an FBR.

Table 4-1: Performance comparison with previous work.

| | JSSC'15 [4-1] | ISSCC'16 [4-2] | ISSCC'19 [4-3] | VLSI'19 [4-5] | ISSCC'20 [4-6] | ISSCC'22 [4-12] | **This work [4-9]** |
|---|---|---|---|---|---|---|---|
| Technology | 0.35μm | 0.35μm | 0.18μm | 0.13μm | 600nm | 65nm | **0.18μm** |
| Technique | Comparator based | P-SSHI | SPFCR | P-SSHI | PSECE | SECE | **SSHI** |
| PT Type | Mide-V21BL | Mide-V21BL | PPA1021 | PPA1021/1022 | - | - | **P-1107YB** |
| $C_P$ | 11nF | 26nF | 22nF | 20nF | 24nF | 24nF | **42nF** |
| $V_{OC}$ | 2V | 1.25V | 1.4V | 3V | - | - | **1.2-2V** |
| Frequency | 100Hz* | 134.6Hz | 200Hz | 100Hz | 56Hz | - | **230Hz** |
| MPPT Tech. | FOCV | FOCV | FOCV | P&O | P&O | FOCV | **DCB** |
| Continuous MPPT? | No | No | No | Yes | Yes | No | **Yes** |
| $V_{OC}$ Sampling? | Yes | Yes | Yes | No | Yes | Yes | **No** |
| MPPT Eff. | 99% | - | - | 97% | 94% | 80% | **98%** |
| Chip Area | 5.5mm$^2$ | 1.3mm$^2$* | 0.21mm$^2$ | 1.07mm$^2$ | 14mm$^2$ | 3.11mm$^2$ | **0.47mm$^2$** |
| $P_{IC}/P_{FBR}$ | 100% | 440% | 650%-930% | 417% | 328% | 320% | **738%** |

*: Estimated value; -: Not reported.

## 4.6 Conclusion

This chapter introduced a novel duty-cycle-based (DCB) MPPT algorithm and its integration with an SSHI rectifier. A simple equation was derived, showing that MPPT efficiency depends solely on the rectifier's duty cycle and is independent of other system parameters such as $V_{OC}$ or $\eta_F$. Based on this principle, a bias-flip rectifier with DCB MPPT was proposed, achieving MPPT by regulating the rectifier's cut-off duty cycle at 50%. This approach simplifies circuit implementation, reduces power consumption, and eliminates the need for complex sensing or calibration. Experimental results demonstrate a peak MPPT efficiency of 98%, with strong robustness to duty cycle errors and ultra-low power operation, validating the effectiveness of the proposed technique.

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# Chapter 5 A Single-Stage Bias-Flip Rectifier with Highly-Digital Duty-Cycled-Based MPPT [3]

## 5.1 Introduction

As mentioned in Section 2.5, the cascaded efficiency loss of conventional 3-stage system architectures for piezoelectric energy harvesting (PEH) results in low end-to-end efficiency [5-1] [5-2]. To improve this, this chapter introduces a single-stage bias-flipping maximum power point tracking (MPPT) regulating rectifier (BMRR). It uniquely integrates active bias-flip rectification, MPPT, and output voltage regulation into a single stage, as shown in Fig. 5-1. It can thus efficiently deliver harvested energy from a piezoelectric transducer (PT) to the output capacitor ($C_{OUT}$) in a single stage, eliminating cascaded energy loss and achieving a significant improvement in end-to-end efficiency [5-3].

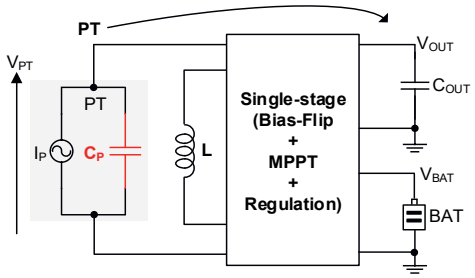



Fig. 5-1. Proposed single-stage bias-flipping MPPT regulating rectifier.

[3] This chapter is based on the journal paper: X. Yue, S. Du "A Single-Stage Bias-Flip Regulating Rectifier with Fully Digital Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting," *IEEE Journal of Solid-State Circuits*, Dec 2024.

## 5.2 Topology and Operations of the Proposed Single-Stage Rectifier

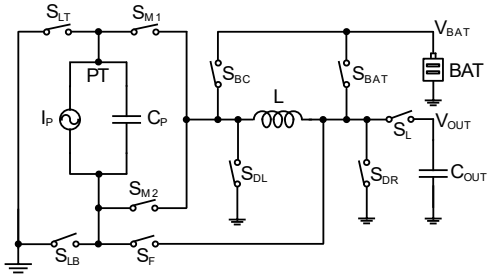



Fig. 5-2. Power stage topology of the proposed BMRR.

As shown in Fig. 5-2, the proposed BMRR consists of 10 power switches, an inductor, an output capacitor $C_{OUT}$, and a battery (BAT). By appropriately controlling the switches as illustrated in Fig. 5-3, the circuit can be configured in various modes that perform active bias-flip rectification, MPPT, and output voltage regulation.

In mode (a), at the zero-crossing moment of $I_P$, the inductor is used to flip $V_{PT}$ by closing $S_{M1}$ and $S_F$. The PT can then efficiently transfer power to the output capacitor $C_{OUT}$ and the load.

When the PT-generated power ($P_{PT}$) $\leqslant$ load-consumed power ($P_{LOAD}$), $C_{OUT}$ is directly charged by the PT in either mode (b) or mode (c), depending on PT polarity. Each mode consists of two steps. In the first step (red path), energy is transferred from the PT to the inductor. In the second step (blue path), energy is transferred from the inductor to the output capacitor $C_{OUT}$.

When $P_{PT} > P_{LOAD}$, part of the PT-generated power is transferred to BAT in either mode (d) or mode (e), depending on the PT polarity, to regulate $V_{OUT}$. Each of these modes also consists of two steps: one to energize the inductor (red path) and one to discharge it into BAT (blue path). If the PT-generated power is insufficient to supply the load-consumed power, $V_{OUT}$ can still be regulated by switching to mode (f) and transferring the stored energy in BAT to $C_{OUT}$.

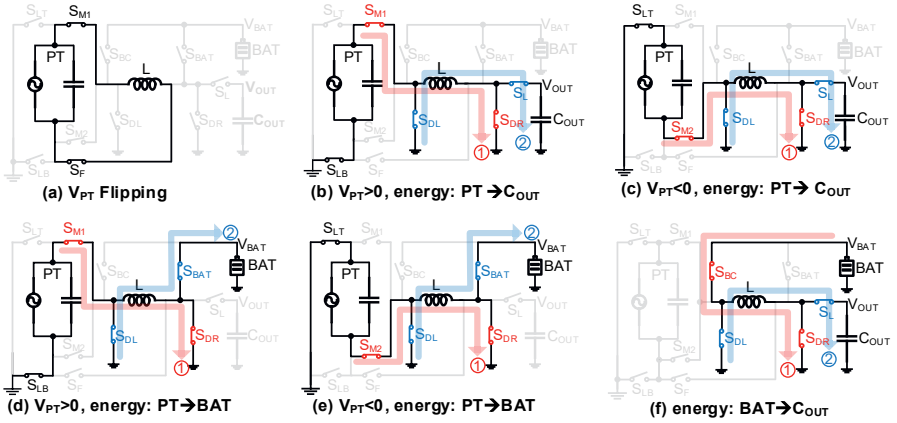



Fig. 5-3. Operation modes and current flowing paths of the proposed BMRR.

## 5.3 Comparisons with Conventional 3-Stage Systems

This section compares the operation and performance of the proposed single-stage system with that of a conventional 3-stage system by analysing the PT waveform ($V_{PT}$) and computing the power conversion efficiency (PCE).

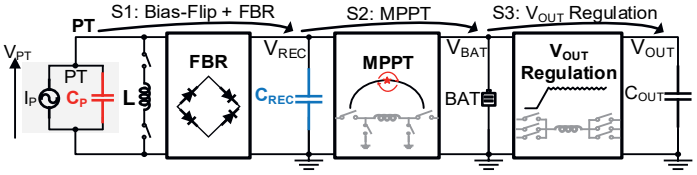



Fig. 5-4. A conventional topology of a 3-stage system architecture.

### 5.3.1 Operation Comparison

A conventional three-stage PEH system is shown in Fig. 5-4. It comprises three power stages, an AC-DC bias-flip rectifier, an MPPT block, and an output voltage regulator with storage elements $C_{REC}$, BAT, and $C_{OUT}$ connected at each stage's output, respectively.

Fig. 5-5 shows the PT waveform ($V_{PT}$) in a conventional PEH system (top) and in the proposed BMRR (bottom). In a conventional system, the rectified voltage $V_{REC}$

increases slowly from 0V to reach the maximum power point voltage, $V_{MPP}$. This startup process is prolonged due to the time required to charge the relatively large capacitor $C_{REC}$. This extended tracking and convergence time exists in conventional MPPT algorithms, such as Perturb & Observe (P&O), fractional open circuit voltage (FOCV), and conventional duty-cycle-based (DCB) algorithms. This chapter proposes a stabilized DCB MPPT technique, which distinguishes itself from the DCB MPPT technique proposed in Chapter 4. In this approach, the duty cycle of the cut-off time of the AC-DC rectifier is regulated to 50% to track the MPP. However, a capacitor ($C_{REC}$) is needed to stabilize the output power variations around the MPP. Unfortunately, $C_{REC}$ is typically at the microfarad level, resulting in prolonged startup times, as depicted in the top left of Fig. 5-5. When $V_{REC}$ is low, the rectifier's cut-off duty cycle is small and gradually converges to 50% over an extended startup time, during which $V_{REC}$ slowly increases to its steady-state. If the open circuit voltage $V_{OC}$ increases from 1V to 2V, due to a change in the external excitation level, the duty cycle will decrease below 50% since $V_{REC}$ is still at the $V_{MPP}$ corresponding to $V_{OC}$ = 1V. A considerable amount of time is then needed to charge $V_{REC}$ to the new $V_{MPP}$.

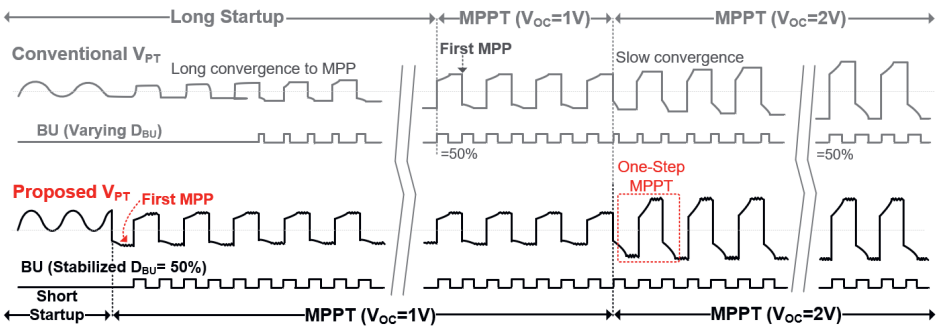



Fig. 5-5. PT voltage ($V_{PT}$) of a conventional bias-flip rectifier and the proposed BMRR.

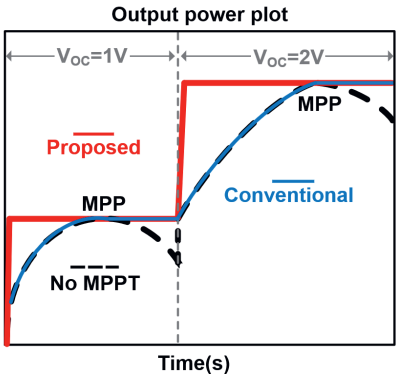



Fig. 5-6. The output power of the proposed BMRR, conventional SSHI with MPPT, and conventional SSHI with no MPPT.

With the proposed stabilized DCB MPPT technique, the PT is temporarily disconnected from the interface circuit to allow $V_{PT}$ to jump to the MPP within a half-vibration period, rather than waiting many periods as in conventional DCB designs. The $V_{PT}$ waveform in the proposed BMRR is shown at the bottom of Fig. 5-5. The duty-cycle is directly regulated to 50%, ensuring that the first MPP is achieved from the beginning. If the external excitation abruptly changes, e.g., from 1V to 2V, the proposed rectifier will quickly respond and work at the new MPP in the next half period. Correspondingly, the output power plot versus time is shown in Fig. 5-6. Without MPPT, the output power increases and then decreases. With conventional MPPT, the output power slowly rises to the MPP, where it is maintained. However, by using the proposed technique, the BMRR quickly forces the output power to the MPP.

### 5.3.2 Power Analysis of a Conventional 3-Stage System

The power conversion efficiency (PCE) of a conventional three-stage PEH system is shown in Fig. 5-4. In the first stage, an SSHI rectifier is used to flip the PT voltage. The flipped voltage ($V_F$) can then be expressed by [5-3]:

$$V_F = (V_{REC} + 2V_D)\eta_F \tag{5.1}$$

where $V_D$ is the forward voltage drop of a diode in a full-bridge rectifier, and $\eta_F$ is the flipping efficiency. The voltage loss ($V_L$) after flipping can be written as

$$V_L = (V_{REC} + 2V_D) \times (1 - \eta_F) \tag{5.2}$$

Hence, the charge flowing into $C_{REC}$ is

$$Q_{SSHI} = Q_T - C_P \times V_L = C_P(2V_{OC} - V_L) \tag{5.3}$$

The input power flowing into the rectifier is expressed by

$$P_{IN,REC} = 2f_P C_P \times (V_{REC} + 2V_D)(2V_{OC} - V_L) \tag{5.4}$$

While the ideal rectifier output power transferred to the rectified capacitor $C_{REC}$ is

$$P_{OUT,REC} = 2f_P C_P V_{REC}(2V_{OC} - V_L) \tag{5.5}$$

Therefore, the AC-to-DC power conversion efficiency (PCE) of a conventional bias-flip rectifier, noted as $\eta_{REC}$, can be expressed as

$$\begin{aligned} \eta_{REC} &= \frac{P_{OUT,REC}}{P_{IN,REC}} = \frac{2f_P C_P V_{REC}(2V_{OC} - V_L)}{2f_P C_P (V_{REC} + 2V_D)(2V_{OC} - V_L)} \\ &= \frac{V_{REC}}{V_{REC} + 2V_D} \end{aligned} \tag{5.6}$$

In the second stage, the charge stored in $C_{REC}$ is transferred to BAT using a typical buck-boost DC-DC converter. Similarly, in the third stage, the energy stored in BAT

is transferred to a regulated output capacitor, $C_{OUT}$, through another buck-boost DC-DC converter. The PCE of a buck-boost converter depends on many factors, including its voltage conversion ratio (VCR), loop resistance, switching frequency, inductors, etc. For well-designed inductor-based buck-boost converters, the PCE is usually between 90%-95%. To simplify our calculations and focus only on the PCE of the system level, it is assumed that the two buck-boost converters in the second and third stages in Fig. 5-4 have the same efficiency, noted as $\eta_{DCDC}$. Therefore, the end-to-end (E2E) efficiency ($\eta_{E2E-conv}$) of a conventional 3-stage architecture is given as

$$\begin{aligned}\eta_{E2E-conv} &= \eta_{REC} \times \eta_{DCDC} \times \eta_{DCDC} \times \eta_{MPPT} \\ &= \frac{V_{REC} \times \eta_{DCDC}^2 \times \eta_{MPPT}}{V_{REC} + 2V_D}\end{aligned} \tag{5.7}$$

where $\eta_{MPPT}$ is the MPPT efficiency. This efficiency depends on how well the real-time $V_{REC}$ tracks the actual MPP voltage, $V_{MPP}$, where $V_{MPP} = \frac{V_{OC}}{1-\eta_F} - V_D$ according to [5-3]. For a well-designed MPPT block, which ensures that $V_{REC}$ closely tracks $V_{MPP}$, $\eta_{MPPT} \approx 1$. Hence, (5.7) can be approximated as:

$$\eta_{E2E-conv} \approx \frac{V_{MPP} \times \eta_{DCDC}^2}{V_{MPP} + 2V_D} \tag{5.8}$$

### 5.3.3 Power Analysis of the Proposed Single-Stage BMRR

The proposed BMRR transfers energy from the PT directly to $C_{OUT}$, via a single DC-DC conversion stage, thus eliminating the need for a full-bridge rectifier. As illustrated in Fig. 5-3, each DC-DC conduction path in the BMRR only includes two power switches, which is also the case in conventional buck-boost converters. As a result, the DC-DC power conversion efficiency (PCE) of the BMRR will be comparable with that of standard buck-boost converters, previously denoted as $\eta_{DCDC}$. Assuming that the MPPT efficiency is very close to 1, the end-to-end PCE of the proposed BMRR can be written as

$$\eta_{E2E-prop} = \eta_{DCDC} \times \eta_{MPPT} \approx \eta_{DCDC} \tag{5.9}$$

Based on (5.8) and (5.9), the ratio between the end-to-end PCE of the proposed BMRR and the conventional 3-stage system is given by:

$$\frac{\eta_{E2E-conv}}{\eta_{E2E-prop}} = \frac{V_{MPP}}{V_{MPP} + 2V_D} \times \eta_{DCDC} \tag{5.10}$$

Since both terms in this equation are less than 1, the end-to-end PCE of the proposed BMRR is higher than that of a conventional three-stage system.

## 5.4 Proposed System Architecture and Flowchart

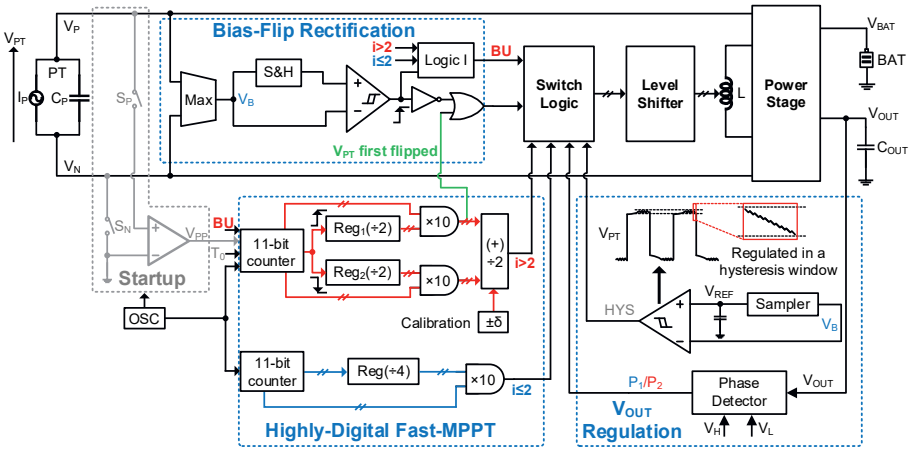



Fig. 5-7: System architecture of the proposed single-stage BMRR.

Fig. 5-7 shows the system architecture of the proposed BMRR, which consists of a power stage (Fig. 5-2), a bias-flip rectification control block, a highly-digital fast-MPPT block, a $V_{OUT}$ regulation block, a startup block, switch control blocks, and level shifters. During the startup, the vibration period ($T_0$) is sampled to find a 50% $V_{PT}$ build-up duty cycle ($D_{BU}$) for MPP. $V_P$ is connected to a comparator, while $V_N$ is grounded, allowing $T_0$ to be determined by a digital counter. After finding $T_0$, the first flipping moment of $V_{PT}$ can then be set to $T_0/2$ during the next vibration period. After

flipping, the MPPT block allows $V_{PT}$ to build up for another $T_0/4$ (corresponding to $D_{BU} = 50\%$) to climb to its first MPP voltage.

When $V_{PT}$ reaches the MPP, the MPP voltage $V_{MPP}$ is sampled, and $V_{PT}$ is regulated to this voltage. If $V_{PT}$ moves away from the MPP, e.g., if $C_P$ is discharged, the build-up signal, BU, goes high, indicating that the polarity of $V_{PT}$ needs to be flipped and built up again towards the next MPP. After another $T_0/4$, BU goes low, and $V_{PT}$ reaches the MPP again. To efficiently maintain MPPT, a new vibration period (T) is digitally sampled and updated at every rising edge of BU. The periodically refreshed T/4 is used to set the next build-up time of $V_{PT}$ (or ON time of the BU signal), so that it builds up directly to the MPP after flipping. The reason for letting $V_{PT}$ build up for exactly T/4 is based on the $D_{BU} = 50\%$ rule of the DCB MPPT algorithm (as discussed in Chapter 2). Since BU is only available after the first flipping, the T/4 time for the first 2 MPPs is calculated from $T_0$. From the 3rd MPP, a real-time T is measured for each vibration period and refreshed at each rising edge of *BU*.

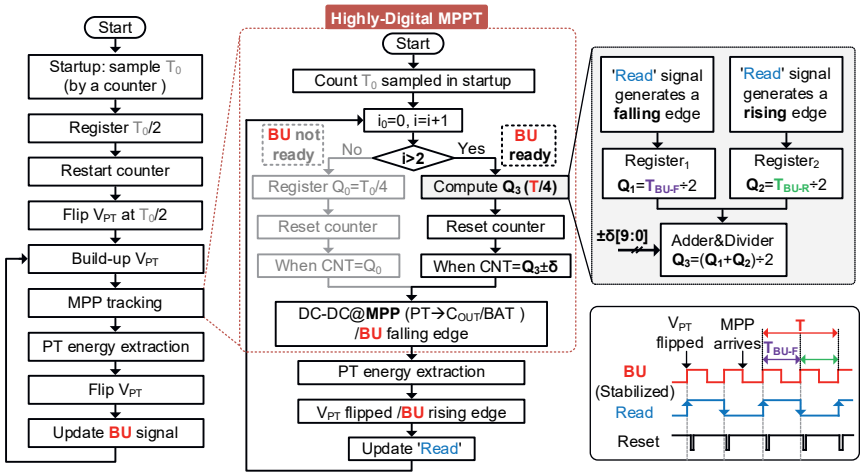



Fig. 5-8. Operational flowchart of the proposed system.

The $V_{OUT}$ regulation block uses a hysteresis window, set by $V_H$ and $V_L$, to regulate $V_{OUT}$. There are three modes to charge $C_{OUT}$: modes (b), (c), and (d). A phase detector decides which mode to use and generates control signals depending on the power level

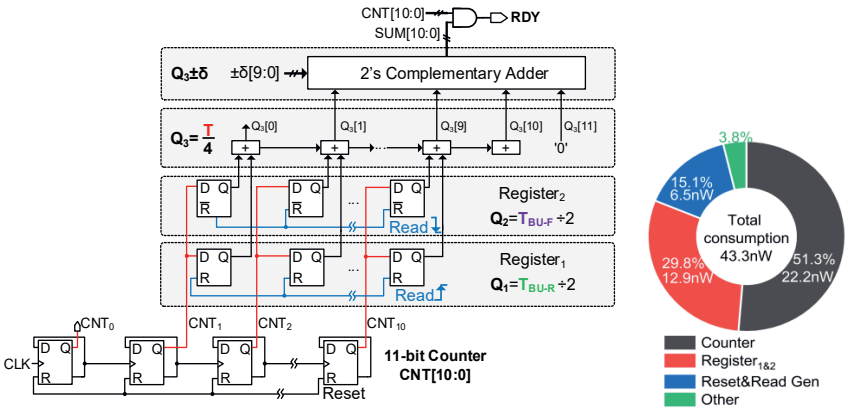
and PT polarity. Finally, digital signals generated by the bias-flip rectification, MPPT, and $V_{OUT}$ regulation blocks are fed into the switch logic block to drive the power stage after level shifters.

The system operational flowchart is shown in Fig. 5-8. The left flowchart illustrates the system-level operations. The system commences by sampling the vibration period, followed by three subsequent steps: PT voltage bias-flipping, MPPT, and energy extraction. The detailed MPPT operations are shown in the middle, where the first 2 MPPs are found through the left path when the *BU* signal is not ready. Upon reaching a steady state, the MPP is tracked via the right path when *BU* is ready. The right part of Fig. 5-8 shows the procedure for determining the 50% duty cycle. The bottom right shows the waveform of the *BU*, Read, and Reset signals. In steady operation, the rising edge of *BU* corresponds to the PT voltage flipping moment, while its falling edge signifies the arrival of the MPP.

## 5.5 Circuit Implementation

### 5.5.1 Highly-Digital MPPT Circuit Implementation

Fig. 5-9 (a) shows the implementation of the digital circuit that determines T/4, i.e., the build-up time of $V_{PT}$ to achieve $D_{BU}$ = 50%. To determine T/4, a 10-bit counter CNT [10:0] continuously counts the clock (CLK) cycles within each *BU* period—an on-chip-generated clock of 50 kHz drives the counter. The counter is reset at every *BU* rising edge, and its 1-bit-right-shifted (halved) output is alternatively stored in two registers, $Q_1$ and $Q_2$. Then, $Q_1$ and $Q_2$ are averaged to obtain T/4. The averaging operation of two adjacent *BU* periods, stored in $Q_1$ and $Q_2$, removes the error between them and obtains an accurate T/4. The final T/4 can be externally adjusted by a 10-bit signal δ[9:0] (in the range of [-512, 511]) and a 2's complementary adder to manually set $D_{BU}$ in a wide range from 15% to 75%. This calibration ability allows system performance to be measured in non-MPP conditions. By employing a highly-digital MPPT technique, the whole MPPT block consumes only 43.3nW, as shown in Fig. 5-9(b), where the counter occupies the largest proportion.




(a). Digital circuit implementation (b). MPPT power consumption

Fig. 5-9. Proposed stabilized DCB MPPT technique.

Fig. 5-10 shows the circuit implementation responsible for generating the counter-control signals featured in Fig. 5-9. This configuration directs the $V_{PP}$ and $BU$ signals into the reset block and D-flip-flops, where $V_{PP}$ is the result of comparing $V_P$ and $V_N$ during the startup state. These components collaborate to yield the final Reset and Read signals, pivotal for regulating the counter operation outlined in Fig. 5-9. The Read signal undergoes updates upon the occurrence of a rising edge in the $BU$ signal. Conversely, after reading the registered clocks, the Reset signal is triggered. The reset block's specifications are outlined at the top of the diagram. The weak inverters have a width-to-length (W/L) ratio of 0.22μm/10μm.

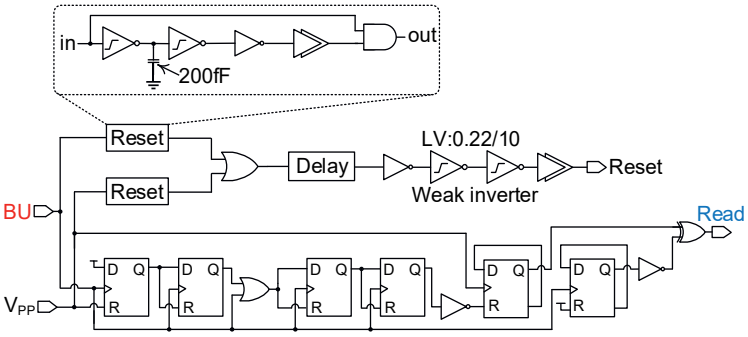



Fig. 5-10. Digital MPPT control block for generating Reset and Read signals.

### 5.5.2 Output Voltage Regulation Block

Fig. 5-11 shows the $V_{OUT}$ regulation block, which is crucial in determining the direction of energy flow in the system. The logic controls, depicted on the left side of the diagram, produce outputs that dictate the energy flow paths of the system. The switch logic section's top two paths signify the energy flow from the battery (BAT) to the output capacitor $C_{OUT}$. In contrast, the middle paths represent the energy flow from the piezoelectric transducer (PT) to the BAT. The bottom paths depict the energy transfer from the PT to $C_{OUT}$. After passing through the level shifters, the output signals drive the switches in the power stage.

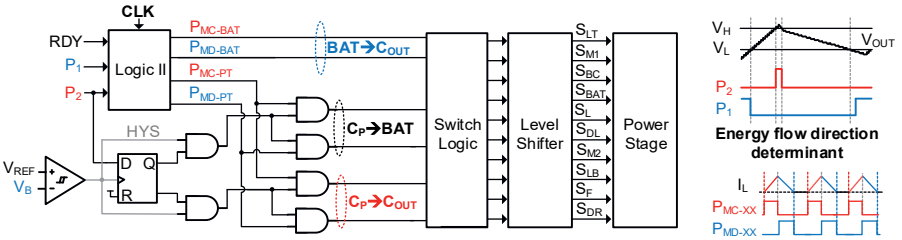



Fig. 5-11. The output regulation block of the proposed single-stage rectifier.

The input signals, $P_1$ and $P_2$, indicate whether $V_{OUT}$ reaches its hysteresis lower boundary, $V_L$, or higher boundary, $V_H$, respectively. When $P_2$ is high, $V_{OUT}$ does not need to be charged, and the PT energy goes into BAT; otherwise, PT-generated energy is transferred into $C_{OUT}$. When $P_1$ is high, it indicates that the PT-harvested power is too low to sustain the load, so BAT is engaged to charge $V_{OUT}$ until it reaches $V_H$. The HYS signal generated by a hysteresis comparator in Fig. 5-12 assists in determining where the PT-generated energy flows. The signals $P_1$, $P_2$, and $RDY$ are used to generate inductor charging phases, $P_{MC-XX}$ (either $P_{MC-PT}$ or $P_{MC-BAT}$), and inductor-discharging phases $P_{MD-XX}$ (either $P_{MD-PT}$ or $P_{MD-BAT}$), to drive the switch matrix for power transfer operations. The $RDY$ signal indicates whether the MPP arrives.

Fig. 5-12 presents the detailed circuits of the hysteresis comparator, which is crucial in regulating the PT voltage. The ratio between the widths of transistors ($M_1$ and $M_2$) and ($M_3$ and $M_4$) determines the hysteresis window. The top PMOS pair ($M_5$ and

$M_6$) calibrates the ratio in a wide range. When the $H_{EN}$ is high, the $M_5$ and $M_6$ are off, resulting in a smaller window. Otherwise, the $M_5$ and $M_6$ are connected in series with $M_1$ and $M_2$, respectively, leading to a larger window. Fig. 5-13 shows a current-starved on-chip oscillator. Its output, CLK, of 50KHz, is provided to the counters to count the vibration period and determine the MPP. The biasing current is 7.5nA, and the total consumed power is around 67.5nW.

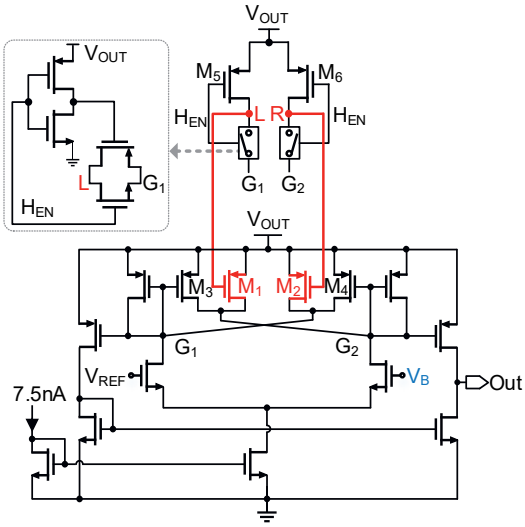


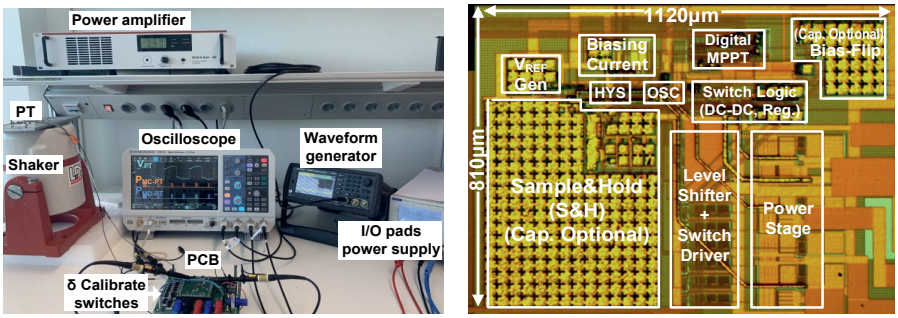

Fig. 5-12. Hysteresis comparator for PT voltage regulation.

## 5.6 Measurement Results

### 5.6.1 Measurement Setup

Fig. 5-13 shows the measurement setup and chip micrograph. The chip was fabricated in a 180nm BCD process. The active chip area is 0.91mm$^2$. The measurements use two commercial piezoelectric transducers to validate the proposed system's operations better. The chip was tested using two commercial piezoelectric transducers (PTs): a 23 nF PT (S129-H5FR-1803YB) and a 116 nF PT (S128-J1FR-1808YB). Both were mounted on a shaker (LDS V450) and excited at their respective resonance

frequencies of 133 Hz and 120 Hz. The employed battery is a SEIKO MS621FE, whose output voltage ranges between 3V and 3.5V.




a). Measurement setup b). Chip micrograph

Fig. 5-13. Experimental setup and chip microphoto.

### 5.6.2 Measurement Waveform of PT Voltage

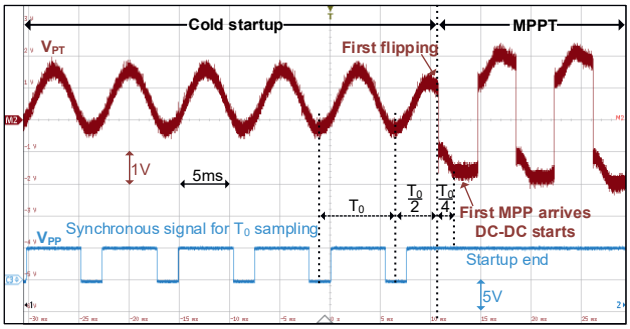



Fig. 5-14. Measured the PT Voltage waveform during startup.

Fig. 5-14 shows the waveform of $V_{PT}$ and a status signal $V_{PP}$ in the very first several vibration periods after excitation starts. Initially, the vibration period $T_0$ is examined for the first several free oscillations of $V_{PT}$. After $T_0$ is sampled and determined, the first flipping moment of the PT voltage occurs after $T_0/2$ in the following period. After another $T_0/4$ period, the MPP arrives, and DC-DC conversion starts operating to regulate the PT voltage, indicating the finishing of the startup period. As shown in Fig. 5-14, the startup period consists of only 5 vibration periods. This period could potentially be optimized to as few as 2 periods. Once the startup period is complete,

the system transitions into a stable operating state, maintaining $V_{PT}$ regulation and bias-flipping.

Fig. 5-15 shows the PT voltage, $V_{PT}$, and the flipping signal during the steady state. The zoomed-in figure at the top right displays the behaviour of the PT voltage during a flipping moment. During this time, the PT voltage is flipped from -1.6V to 1.4V, representing an 87.5% voltage flipping efficiency.

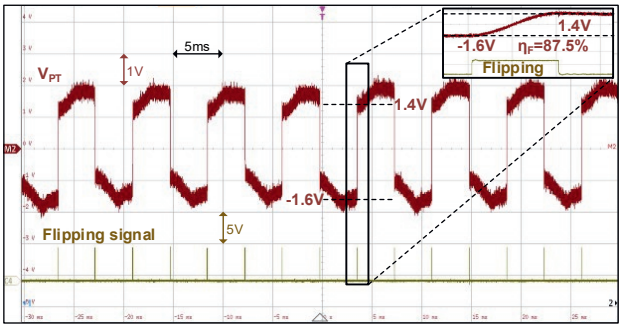



Fig. 5-15. Measured the PT Voltage waveform during the steady state.

Fig. 5-16 provides a detailed view of the PT voltage during the build-up and regulation periods. The waveform shows a measured *BU* duty cycle, $D_{BU}$, of approximately 49.87%. The right part of the figure shows the control phases, $P_{MC-PT}$ and $P_{MD-PT}$. The $P_{MC-PT}$ represents the phase during which charge is transferred from the PT to energize the inductor, while $P_{MD-PT}$ shows the inductor-discharging phase.

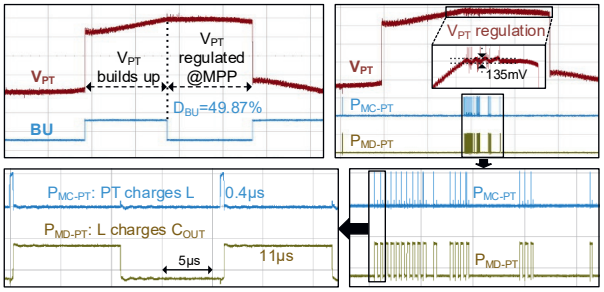



Fig. 5-16. Zoomed-in waveform of the PT voltage and related control phases.

### 5.6.3 Measured PT Voltage Waveform During MPPT

Fig. 5-17 shows the waveform of PT voltage $V_{PT}$ and $BU$. The proposed system was designed to achieve MPPT in response to changes in external excitation levels. Initially, the PT's open circuit voltage ($V_{OC}$) is 0.8V, and the flipping efficiency is 60%, corresponding to an MPP voltage $V_{MPP}$ of around 2V. When the $V_{OC}$ increases to 1.2V, the flipping efficiency rises to 65% in the steady state since the higher gate-driving voltage reduces the switch resistance in the bias-flip loop. It can be observed that the duty cycle of $BU$ is anchored to 50% to regulate $V_{PT}$ towards the new $V_{MPP}$ of around 3.4V automatically.

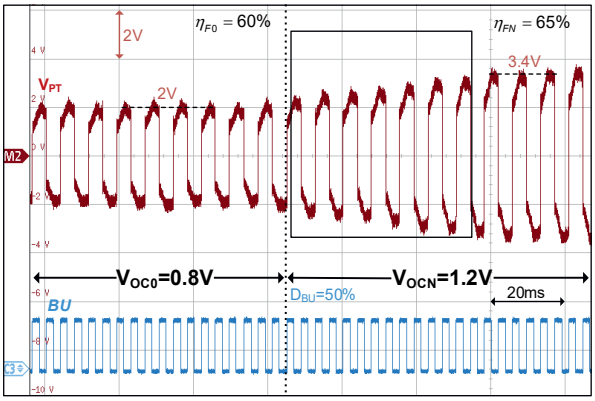



Fig. 5-17. System transient waveform of PT voltage and $BU$ signals under different external excitation levels.

### 5.6.4 Measured Waveform During Output Regulation

Fig. 5-18 shows the waveforms of $V_P$, $V_{OUT}$, $P_{MD-PT}$, and $P_{MD-BAT}$ under different load conditions. The $P_{MD-PT}$ and $P_{MD-BAT}$ represent the inductor-discharging phases from the PT and the battery, respectively. The left figure shows that when the load resistance is 1MΩ, the system maintains an output voltage of 5V with a small ripple of 37mV and a load current of 5μA. In contrast, the right figure of Fig. 5-18 shows the waveform in a heavier load condition with a load resistance of 50KΩ, which results in a larger maximum output voltage ripple of 127mV. The zoomed-in waveform

on the bottom reveals that $P_{MD-PT}$ and $P_{MD-BAT}$ last 11µs and 3µs, respectively. The output of the on-chip 50KHz oscillator is shown at the bottom left.

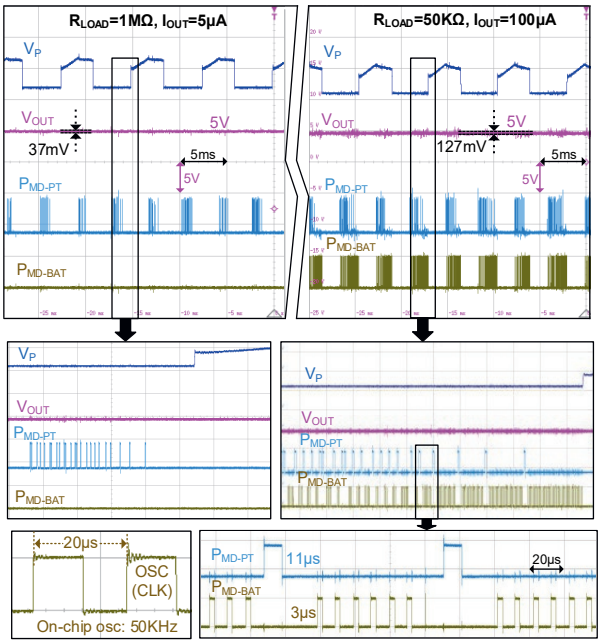



Fig. 5-18. Measured $V_{OUT}$ regulation in different loading conditions.

## 5.7 Performance Analysis

Fig. 5-19 presents the relationship between output power and the *BU* signal duty cycle, $D_{BU}$, for the proposed BMRR under different open circuit voltages $V_{OC}$. The figure aims to determine the optimum duty cycle for maximum power output, with $V_{OC}$ at 1.5V and 2V, exhibiting the same voltage flipping efficiency of 60%. This data was acquired by manually configuring the external signal δ [9:0] to stabilize $D_{BU}$ at a specific value in a broad range from 15% to 75%, as detailed in Fig. 5-9. The results prove that for different $V_{OC}$ values, the optimum $D_{BU}$ for achieving maximum output power is around 50%, which matches the theory of the DCB MPPT algorithm.

Fig. 5-20 shows the output power of the proposed BMRR over 15s of time starting from a static PT with $V_{OC}$ changed in the middle, similar to the phenomenon shown

in Fig. 5-17. The measurements demonstrate the effectiveness of the fast-MPPT technique. Initially, following the startup phase, the output power swiftly rises to 10μW

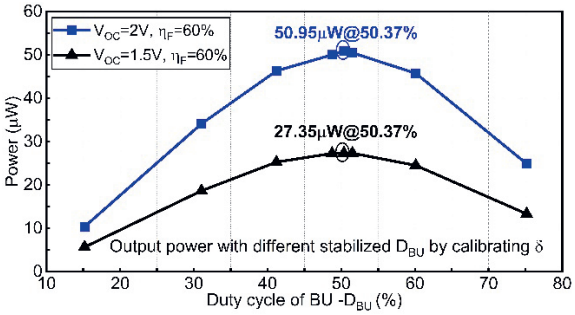



Fig. 5-19. Output power versus $D_{BU}$ for different $V_{OC}$ voltages.

within a timeframe of 15ms to 38ms (2-5 vibration periods). This rapid increase is attributed to the implementation of the proposed fast-MPPT technique. Subsequently, when the open circuit voltage transitions from 0.8V to 1.2V, the output power rapidly surges from 10μW to 30μW. This rapid power increase underscores the responsiveness and efficiency of the BMRR rectifier in adapting to changes in the external environment, thereby maximizing power extraction from the energy source.

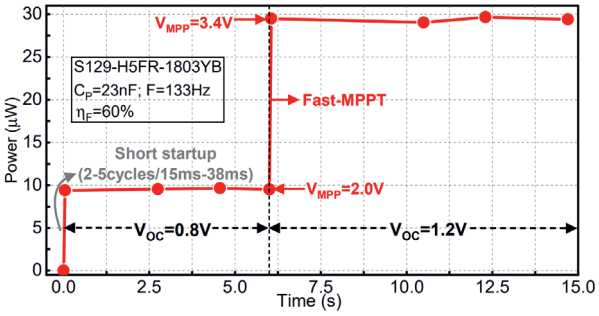



Fig. 5-20. Output power versus time with increasing $V_{OC}$.

Fig. 5-21 exhibits the measured MPPT efficiency and acceleration level as a function of the open circuit voltage $V_{OC}$. The data reveals remarkable efficiency metrics, with a maximum MPPT efficiency reaching an impressive 99.9%, while the average MPPT efficiency stands at 99.79% in a wide range of $V_{OC}$ from 0.4V to 2V. These results underscore the efficacy of the highly-digital MPPT design. The chip leverages

a 180nm BCD process featuring CMOS transistors with a maximum rating of 5V. The acceleration measurements complement these efficiency figures, with the minimum

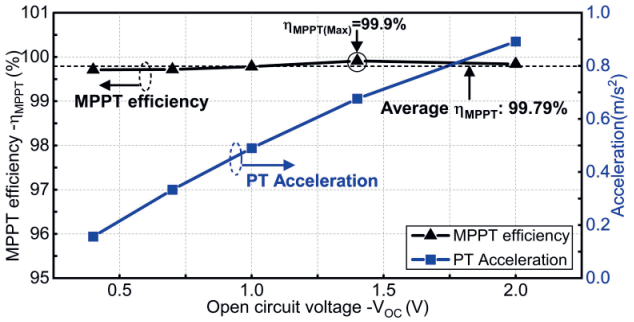



Fig. 5-21. MPPT efficiency and excitation acceleration levels over $V_{OC}$.

acceleration level at 0.2m/s$^2$ corresponding to $V_{OC}$ of 0.4V and the maximum acceleration measured at 0.9m/s$^2$ corresponding to $V_{OC}$ of 2.0V. Such performance metrics highlight the robustness and versatility of the chip design in adapting to varying operating conditions while consistently achieving high levels of efficiency.

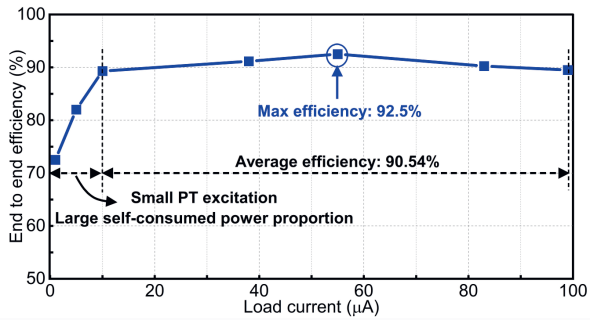



Fig. 5-22. End-to-end (E2E) efficiency with different load current.

Fig. 5-22 provides the measured end-to-end efficiency of the proposed BMRR for various load currents. Notably, the measurements indicate a peak end-to-end efficiency of 92.5% with the load current at 55μA. The system achieves an average efficiency of 90.54% in a wide load current range from 10μA to 100μA. The end-to-end efficiency tends to be relatively low at lower load current due to a higher proportion of self-consumed power. These results underscore the efficacy of the proposed single-

stage BMRR in achieving high end-to-end efficiency from the energy harvester to the load.

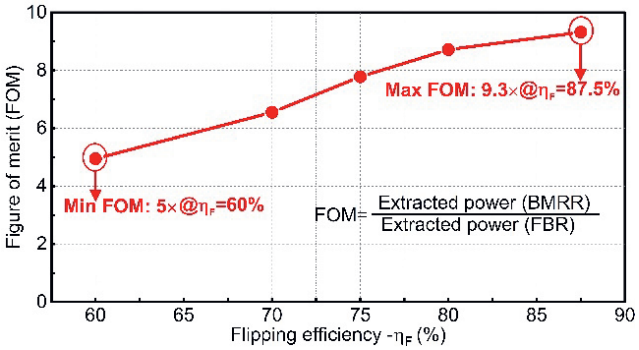



Fig. 5-23. Power extraction enhancement compared to an FBR.

Fig. 5-23 depicts the figure of merit (FOM) concerning flipping efficiency, where the FOM is defined as the ratio of the extracted power with the proposed BMRR to that of an FBR. With flipping efficiency ranging from 60% to 87.5%, the FOM exhibits corresponding variations from 5× to 9.3×. Therefore, the BMRR achieves the energy extraction enhancement of up to 9.3× compared to an FBR.

Table 5-1 compares the performance of the proposed BMRR with prior work. Rather than trying to optimize the performance of either the rectifier stage or the MPPT stage, the BMRR achieves high end-to-end efficiency by integrating bias-flip rectification, MPPT, and output regulation in a single stage. Compared to the conventional DCB MPPT proposed in Chapter 4 [5-1], which determines the duty cycle by comparing the sampled voltage across two identical capacitors, the stabilized DCB MPPT offers greater accuracy due to its digital sampling method. Additionally, by forcing the duty cycle to 50% instead of waiting for it to naturally reach this value, the startup time is significantly shortened, enabling a more efficient one-step MPPT. Measured results show a maximum output end-to-end power conversion efficiency of 92.5% and power extraction enhancement of 9.3×, highlighting its superior performance in PEH systems.

## 5.8 Conclusion

This chapter proposes a single-stage bias-flipping MPPT regulating rectifier (BMRR) for piezoelectric energy harvesting. The proposed system integrates bias-flip rectification, MPPT, and output regulation in only one stage, eliminating intermediate stages and minimizing energy loss. The proposed highly-digital MPPT technique is based on a stabilized 50% DCB method, which ensures MPPT is achieved shortly after the system starts operating, typically within several vibration cycles. The proposed architecture removes the capacitor connected to the output of a conventional rectifier, guaranteeing a one-step MPPT and short startup. Thanks to the single-stage BMRR, the energy extraction performance is enhanced by 9.3× compared to an FBR, and a 92.5% end-to-end efficiency is achieved.

Table 5-1: Performance comparison with prior works.

| | JSSC'17 [5-2] | ISSCC'20 [5-4] | AICSP'22 [5-5] | ISSCC'22 [5-6] | ISSCC'23 [5-7] | ISSCC'23 [5-1] | **This work [5-3]** |
|---|---|---|---|---|---|---|---|
| Technology | 0.35μm | 0.6μm | 0.18μm | 0.18μm | 0.18μm | 0.18μm | **0.18μm** |
| Energy | EM | Piezo | Piezo | Tribo | Piezo | Piezo | **Piezo** |
| Frequency | 64.4Hz* | 56Hz | 120Hz | 250Hz | 130Hz | 230Hz | **133Hz/120Hz** |
| Technique | NVC | SECE | Recycling SL | MCS-BF | ES-SSHI | SSHI | **BMRR** |
| Dimension | 1.3mm$^2$ | 14mm$^2$ | 0.275mm$^2$ | 5.9mm$^2$ | 1.21mm$^2$ | 0.47mm$^2$ | 0.91mm$^2$ |
| $\eta_F$ | No | No | 70% | 69% | 91%/84% | 82% | **87.5%** |
| FBR Required? | Yes | Yes | No | Yes | No | Yes | **No** |
| Cold Start? | Yes(5s) | Yes(4s) | No | N/R | No | No | **Yes(15ms)** |
| $C_{REC}$ Existed? | Yes | No | No | Yes | Yes | Yes | **No** |
| MPPT | CAC | P&O | No | No | No | DCB | **Stabilized DCB** |
| MPPT Circuit | Analog | Hybrid | N/R | N/R | N/R | Analog | **Highly-Digital** |
| Features | Rec.+MPPT+Reg. | Rec.+MPPT | Rec. | Rec. | Rec. | Rec.+MPPT | **Rec.+MPPT+Reg.** |
| Cascaded No. | 3 | 2 | 1 | 1 | 1 | 2 | **1** |
| E2E PCE | 90% | 94% | 76% | 70.7% | N/R | N/R | **92.5%** |
| $P_{IC}/P_{FBR}$ | 1× | 3.28× | 2.5×-12× | 3.14× | 11.7×-6.4× | 7.38× | **9.3×** |

*: Estimated value; N/R: Not reported.

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# Chapter 6 Conclusions and Outlook

This dissertation presents the development of three active rectifiers aimed at improving the power conversion efficiency of piezoelectric energy harvesting (PEH) systems. First, a synchronized switch harvesting on shared capacitors (SSHSC) was proposed to minimize system size (Chapter 3). Second, a bias-flip rectifier incorporating a duty-cycle-based (DCB) maximum power point tracking (MPPT) technique was introduced, offering simple circuit implementation, accurate tracking, and low power consumption (Chapter 4). Third, a single-stage bias-flip rectifier with a fully digital DCB MPPT was developed to reduce the energy loss caused by cascaded system architectures (Chapter 5).

This chapter summarizes the key findings of the dissertation and outlines directions for future research.

## 6.1 Main Findings

The main findings of this thesis are summarized as follows:

- An SSHSC rectifier architecture was developed, which reduces the number of off-chip capacitors required from 9 to 3 without sacrificing flipping efficiency. This results in a compact design with a maintained efficiency of 78%, representing a significant improvement over previous rectifiers (Chapter 3).
- A duty-cycle-based (DCB) MPPT technique was developed, which simplifies MPPT by fixing the duty cycle at 50%. Unlike traditional fractional open circuit voltage (FOCV) and perturb & observe (P&O) methods, this technique does not require voltage sampling or complex calculations and achieves robust and consistent performance across varying conditions (Chapter 4).
- A single-stage bias-flip rectifier architecture was developed, which enables direct energy transfer from PT to load, achieving 92.5% end-to-end efficiency. It eliminates the need for intermediate energy storage, a departure from conventional

multi-stage systems, and enables significantly faster start-up and MPPT convergence (Chapter 5).

❖ Furthermore, a digital implementation of the DCB MPPT technique achieves both low power (43.3nW) and near-ideal MPPT efficiency (99.9%). This demonstrates the feasibility of fully integrated, self-powered energy harvesting systems for low-power applications (Chapter 5).

## 6.2 Comparisons with the State-of-the-Art

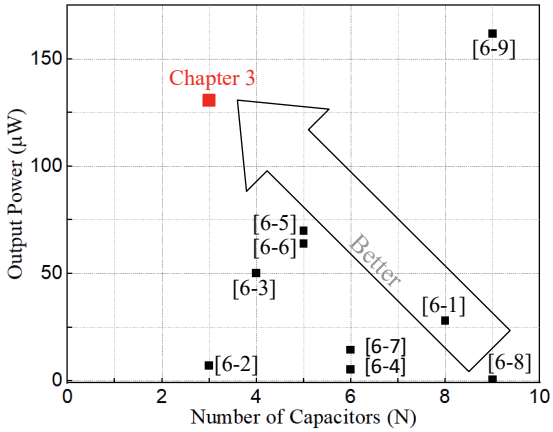


Fig. 6-1. Output power and the number of their capacitors in recent reputable publications.

Fig. 6-1 compares the output power and the number of capacitors used in recent capacitor-based rectifiers. As shown, most of them use 4 to 8 capacitors, while their output power remains below 75μW. Notably, the rectifier in [6-9] delivers higher output power (160μW), but requires 9 capacitors. In contrast, the design described in Chapter 3 delivers 130μW while using only 3 capacitors, significantly reducing circuit complexity and system size.

Table 6-1 compares the proposed DCB algorithm introduced in Chapter 4 with two widely used MPPT techniques: FOCV and P&O. Unlike FOCV, DCB does not require open-circuit voltage sampling or efficiency calibration, simplifying control logic and reducing hardware overhead. Compared to P&O, DCB achieves the lowest

power consumption and lowest circuit complexity, making it particularly suitable for low-power and resource-constrained systems. It also demonstrates high robustness to parameter variations, contributing to its reliability in practical applications. However, it should be noted that DCB assumes a sinusoidal input waveform, which may limit its applicability in certain environments. Despite this constraint, DCB provides a compelling balance of efficiency, simplicity, and robustness, highlighting the innovation and practical value of this work.

Table 6-1. Pros and cons comparison table of different MPPT algorithms.

| **MPPT Algorithm** | **FOCV** | **P&O** | **DCB** |
|---|---|---|---|
| $V_{OC}$ Sampling? | Yes | No | No |
| $\eta_F$ Calibration? | Yes | No | No |
| Current Sensing Required? | No | Yes | No |
| Continuous MPPT? | No | Yes | Yes |
| Robustness | Low | High | High |
| Circuit Complexity | Low | High | Low |
| Power Consumption | Low | High | Low |
| Support Arbitrary Excitation? | No | Yes | No |

Fig. 6-2 illustrates the end-to-end efficiency and power enhancement relative to a conventional full-bridge rectifier (FBR). Prior works typically implement only the rectifier stage or combine the rectifier with MPPT and output regulation in a loosely integrated manner, leading to limited overall efficiency and modest power gains. In contrast, Chapter 5 introduces a fully integrated single-stage interface circuit that achieves up to 92.5% end-to-end efficiency and a 9.3× improvement in output power. Compared to recent publications, the proposed design in Chapter 5 demonstrates clear advantages and distinguishes itself from the state of the art.

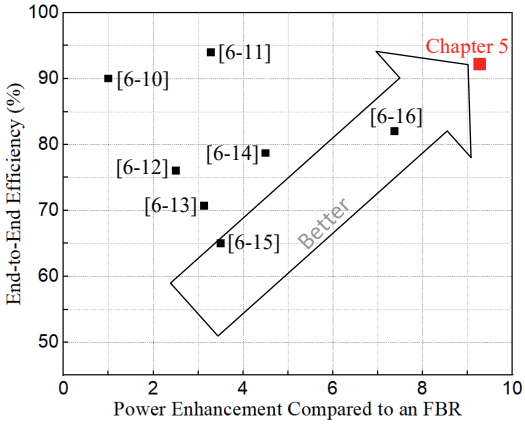


Fig. 6-2. End-to-end efficiency and power enhancement comparison in recent publications.

## 6.3 Future Work

While this dissertation proposes innovative rectifier architectures that address system miniaturization, efficient MPPT, and the reduction of cascaded energy losses, several promising directions remain for future research.

### 6.3.1 Fully Capacitive Rectifier With Output Regulation

Although the SSHSC rectifier introduced in Chapter 3 effectively minimizes system volume without compromising energy flipping efficiency, it does not support output regulation or MPPT. As a result, it cannot be used to directly power wireless sensors. Implementing both MPPT and output regulation typically requires a DC-DC stage, which in turn relies on either bulky inductors or multiple dedicated capacitors. Capacitors are generally preferred over inductors thanks to the high-quality on-chip capacitors. However, existing capacitive DC-DC converters suffer from limited voltage conversion ratios [6-1] [6-17], and the need for separate capacitor banks for MPPT and regulation paths [6-18] [6-19], making full on-chip integration challenging.

Future research should investigate a fully capacitive rectifier that supports rectification, MPPT, and output regulation using a shared capacitor array. These capacitors

would serve dual purposes: participating in voltage flipping and DC-DC energy transfer. Therefore, the total number of passive components could be reduced.

Two key considerations should guide this design:

- **Capacitor sizing and switching frequency**: The capacitance values and the switching frequency must be co-optimized. Higher switching frequencies require smaller capacitors but increase power consumption, while lower frequencies demand larger capacitors and reduce harvesting efficiency. Ideally, the switching frequency should be adaptively tuned based on the level of external excitation: higher under strong excitation and lower under weak conditions.

- **Stage sequencing and path optimization**: Since rectification, MPPT, and output regulation share the same capacitor array, the control logic must select the optimal energy transfer path to minimize hard-charging losses. A smart switching controller should dynamically determine the most efficient route for transferring energy from the PT to the output capacitor.

### 6.3.2 MPPT under Non-Ideal Sinusoidal Excitation

The DCB MPPT algorithm proposed in Chapter 4 and conventional FOCV-based techniques assume that the external excitation is a pure sinusoidal waveform. In practice, however, real-world vibrations are often non-ideal sinusoidal or irregular, making these methods ineffective due to inaccurate MPP estimation.

Future research should focus on developing MPPT methods suitable for non-sinusoidal excitation conditions. One promising direction is to digitize the PT input signal using an ADC and perform real-time signal analysis. By extracting key features, such as waveform shape, peak intervals, or dominant frequencies, the system can bet-

ter characterize the PT behaviour and dynamically adjust its control strategy to accurately track the true maximum power point. This would significantly enhance energy harvesting efficiency under realistic operating conditions.

### 6.3.3 Power Limit Analysis and Possible Solutions

According to Equations (4.7) and (4.8), the maximum extracted power from a bias-flip rectifier is highly dependent on the flipping efficiency. If it is 100%, the maximum power theoretically approaches infinity. However, in reality, the output power is constrained by several factors. First, as the flipping efficiency nears 100%, the PT voltage increases indefinitely, as described by Equation (2.5). Unfortunately, this excessively high PT voltage suppresses the PT's mechanical vibrations due to the inverse piezoelectric effect, thereby reducing the induced charge generated by the normal piezoelectric effect [6-20][6-21]. Second, this theoretically infinite voltage is practically limited by the device breakdown voltage and significant leakage current, preventing the system from achieving the theoretical maximum power [6-22].

For future work, two potential approaches can be considered to push the output power higher. First, to address the issue of high PT voltage, a series-stacked chip array connected in parallel with the PT can be explored. This would evenly distribute the PT voltage across the stacked chips, ensuring that each operates within its breakdown voltage limit while also reducing leakage for each individual chip. Second, off-chip high-voltage switches can be co-integrated with on-chip control blocks to further mitigate high-voltage stress on on-chip devices, improving the power limit.

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## Summary

This thesis presents the design, circuit implementation, and measurement results of energy-efficient interface circuits for piezoelectric energy harvesting (PEH).

**Chapter 1** introduces the background and motivation for this work. It begins by discussing various application scenarios for wireless sensors and emphasizes the critical need for a sustainable power supply to ensure their long-term operation. Energy harvesting systems are identified as a promising alternative to traditional batteries, with piezoelectric energy harvesting standing out as an ideal solution due to the ubiquitous presence of ambient vibrations in the environment. Since efficient energy conversion requires dedicated interface circuits, the chapter reviews typical circuit architectures and highlights three main challenges in the state-of-the-art: the trade-off between system size and rectifier efficiency, the sensitivity and complexity of maximum power point tracking (MPPT) algorithms, and low end-to-end efficiency due to cumulative energy losses in cascaded architectures.

**Chapter 2** provides a comprehensive review of existing interface circuits commonly used in PEH systems. To enhance the output power efficiency of rectifiers, various active rectification techniques have been proposed, such as Synchronized Switch Harvesting on Inductor (SSHI) and Synchronized Switch Harvesting on Capacitor (SSHC). However, SSHI requires bulky inductors, while SSHC depends on multiple dedicated flying capacitors, increasing the system's overall volume. The chapter also introduces two widely used MPPT techniques—Fractional Open-Circuit Voltage (FOCV) and Perturb and Observe (P&O). Both approaches have their respective drawbacks: FOCV requires open-circuit voltage sampling and flipping efficiency calibration, which results in discontinuous tracking and energy loss; P&O, on the other hand, relies on complex circuitry and consumes significant power. Finally, the chapter analyzes the issue of cascaded energy losses in current system architectures, which leads to relatively low end-to-end efficiencies, typically ranging from 50% to 80%.

**Chapter 3** addresses the challenge of minimizing rectifier volume without compromising efficiency by proposing a synchronized switch harvesting rectifier that utilizes reusable storage capacitors. In this design, three capacitors are shared to function both as energy storage elements and as temporary flying capacitors during the energy harvesting and piezoelectric transducer (PT) voltage flipping phases. These capacitors are dynamically reconfigured into nine connection states during the flipping period, effectively replicating the functionality of conventional SSHC flying capacitors. This sharing and reconfiguration technique significantly reduces system size. Measurement results show a PT voltage flipping efficiency of 78%, demonstrating the design's potential for compact, high-efficiency energy harvesting applications.

**Chapter 4** proposes a duty-cycle-based (DCB) MPPT algorithm to overcome the limitations of the FOCV and P&O techniques. The DCB algorithm establishes a direct relationship between the rectifier's on-off duty cycle and its maximum power point (MPP). Mathematical analysis shows that maintaining a 50% duty cycle allows the system to operate at its MPP. Unlike FOCV, this approach eliminates the need for open-circuit voltage sampling and flipping efficiency calibration. It also avoids the complex power computations and hardware overhead associated with P&O. In addition to its simplicity, the DCB method offers robust tracking performance. Experimental results demonstrate a peak MPPT efficiency of up to 98%, with an average tracking efficiency of 94%.

**Chapter 5** presents a single-stage bias-flip rectifier to address the issue of cascaded energy loss in conventional PEH system architectures. This design transfers energy directly from the PT to the output capacitor, reducing intermediate losses. By fixing the rectifier's on-off duty cycle at 50% to achieve MPPT, the need for a separate rectified capacitor is eliminated, resulting in a shorter startup time and faster MPPT response. Experimental results show an end-to-end efficiency of up to 92.5%, with energy extraction performance improved by a factor of 9.3× compared to a full-bridge rectifier (FBR).

**Chapter 6** summarizes the main findings of the thesis and compares the proposed designs in Chapters 3, 4, and 5 with the current state-of-the-art. It also outlines potential directions for future work, including 1) the development of a fully capacitive rectifier with output regulation, 2) MPPT strategies under non-ideal sinusoidal excitation conditions, and 3) power limit analysis and corresponding optimization techniques.

# Samenvatting

Dit proefschrift presenteert het ontwerp, de circuitimplementatie en de meetresultaten van energie-efficiënte interfacecircuits voor piëzo-elektrische energieterugwinning (PEH).

**Hoofdstuk 1** introduceert de achtergrond en motivatie van dit werk. Het begint met een bespreking van verschillende toepassingsscenario's voor draadloze sensoren en benadrukt de cruciale noodzaak van een duurzame energievoorziening om hun langdurige werking te waarborgen. Energieterugwinningssystemen worden geïdentificeerd als een veelbelovend alternatief voor traditionele batterijen, waarbij piëzo-elektrische energieterugwinning zich onderscheidt als een ideale oplossing vanwege de alomtegenwoordige aanwezigheid van omgevingsvibraties. Omdat efficiënte energieconversie speciale interfacecircuits vereist, bespreekt dit hoofdstuk gangbare circuitarchitecturen en benadrukt het drie belangrijke uitdagingen in de huidige stand van de techniek: de afweging tussen systeemgrootte en gelijkrichterefficiëntie, de gevoeligheid en complexiteit van maximum power point tracking (MPPT)-algoritmen, en de lage end-to-end efficiëntie als gevolg van cumulatieve energieverliezen in cascadestructuren.

**Hoofdstuk 2** geeft een uitgebreid overzicht van bestaande interfacecircuits die vaak in PEH-systemen worden toegepast. Om de uitgangsvermogensefficiëntie van gelijkrichters te verbeteren, zijn verschillende actieve rectificatietechnieken voorgesteld, zoals *Synchronized Switch Harvesting on Inductor* (SSHI) en *Synchronized Switch Harvesting on Capacitor* (SSHC). SSHI vereist echter omvangrijke inductoren, terwijl SSHC afhankelijk is van meerdere speciale vliegende condensatoren, wat het totale systeemvolume vergroot. Het hoofdstuk introduceert ook twee veelgebruikte MPPT-technieken: *Fractional Open-Circuit Voltage* (FOCV) en *Perturb and Observe* (P&O). Beide methoden hebben hun nadelen: FOCV vereist het bemonsteren van de open-klemspanning en een efficiëntiekalibratie van het spanningsomklappen, wat leidt tot discontinue tracking en energieverlies; P&O daarentegen berust op complexe schakelingen en verbruikt aanzienlijk vermogen. Ten slotte wordt het probleem van cascaderende energieverliezen in huidige architecturen

geanalyseerd, wat resulteert in relatief lage end-to-end efficiënties, doorgaans variërend van 50% tot 80%.

**Hoofdstuk 3** behandelt de uitdaging om het volume van de gelijkrichter te minimaliseren zonder efficiëntieverlies, door een gesynchroniseerde switch-harvestinggelijkrichter voor te stellen die herbruikbare opslagcondensatoren benut. In dit ontwerp worden drie condensatoren gedeeld en functioneren ze zowel als energieopslagcomponenten als tijdelijke vliegende condensatoren tijdens de energieoogst- en spanningsomklapfasen van de piëzo-elektrische transducer (PT). Deze condensatoren worden dynamisch geherconfigureerd in negen verbindingsstaten tijdens de omklapperiode, waardoor de functionaliteit van conventionele SSHC-vliegende condensatoren effectief wordt nagebootst. Deze deel- en herconfiguratietechniek vermindert de systeemgrootte aanzienlijk. Meetresultaten tonen een PT-spanningsomklapefficiëntie van 78%, wat de potentie van het ontwerp aantoont voor compacte en hoogefficiënte energieoogsttoepassingen.

**Hoofdstuk 4** stelt een duty-cycle-gebaseerd (DCB) MPPT-algoritme voor om de beperkingen van FOCV- en P&O-technieken te overwinnen. Het DCB-algoritme legt een directe relatie tussen de aan/uit-duty-cycle van de gelijkrichter en zijn maximum power point (MPP). Wiskundige analyse toont aan dat het handhaven van een duty-cycle van 50% het systeem in staat stelt op zijn MPP te werken. In tegenstelling tot FOCV elimineert deze methode de noodzaak van open-klemspanningbemonstering en efficiëntiekalibratie van het spanningsomklappen. Het vermijdt ook de complexe vermogensberekeningen en hardware-overhead die bij P&O horen. Naast eenvoud biedt de DCB-methode een robuuste trackingprestatie. Experimentele resultaten tonen een piek-MPPT-efficiëntie tot 98%, met een gemiddelde trackingefficiëntie van 94%.

**Hoofdstuk 5** introduceert een enkeltraps bias-flipgelijkrichter om het probleem van cascaderende energieverliezen in conventionele PEH-architecturen aan te pakken. Dit ontwerp brengt energie rechtstreeks over van de PT naar de uitgangscondensator, waardoor intermediaire verliezen worden verminderd. Door de aan/uit-duty-cycle van de gelijkrichter op 50% vast te zetten om MPPT te realiseren, vervalt de noodzaak van een aparte gelijkgerichte condensator, wat resulteert in een kortere opstarttijd en

snellere MPPT-respons. Experimentele resultaten tonen een end-to-end efficiëntie tot 92,5%, met een 9,3× verbetering in energie-extractie vergeleken met een full-bridge rectifier (FBR).

**Hoofdstuk 6** vat de belangrijkste bevindingen van het proefschrift samen en vergelijkt de voorgestelde ontwerpen uit Hoofdstukken 3, 4 en 5 met de huidige stand van de techniek. Het schetst ook mogelijke richtingen voor toekomstig onderzoek, waaronder: 1) de ontwikkeling van een volledig capacitieve gelijkrichter met uitgangsregeling, 2) MPPT-strategieën onder niet-ideale sinusvormige excitatiecondities, en 3) vermogenslimitanalyse en bijbehorende optimalisatietechnieken.

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# List of Publications

## Journal Papers

1. **Xinling Yue**, Sijun Du, “An Adaptive 2-Mode Bias-Flip Rectifier with Lowered Cold-Startup Voltage Requirement for Multiple Piezoelectric Energy Harvesting,” in *IEEE Transactions on Power Electronics (TPE)*, 2025.

2. **Xinling Yue**, Sijun Du, “A Single-Stage Bias-Flip Regulating Rectifier with Fully Digital Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting,” in *IEEE Journal of Solid-State Circuits (JSSC)*, 2025.

3. Wenyu Peng, **Xinling Yue**, Sijun Du, “A Fully Integrated Bias-Flip Rectifier with Electrostatic Charge Boosting for Triboelectric Energy Harvesting,” in *IEEE Journal of Solid-State Circuits (JSSC)*, 2024.

4. Jing Wang, Yi Yang, Sijun Du, **Xinling Yue**, Xun Liu, Jun Han, Xiaoyang Zeng, and Zhiyuan Chen, “Enhancing Efficiency in Piezoelectric Energy Harvesting: Collaborative-Flip Synchronized Switch Harvesting on Capacitors Rectifier and Multioutput DC-DC Converters Utilizing Shared Capacitors,” in *IEEE Journal of Solid-State Circuits (JSSC)*, 2024.

5. **Xinling Yue**, Jiarui Mo, Zhiyuan Chen, Sten Vollebregt, Guoqi Zhang, Sijun Du, “A Fully Integrated Sequential Synchronized Switch Harvesting on Capacitors Rectifier Based on Split-Electrode for Piezoelectric Energy Harvesting,” in *IEEE Transactions on Power Electronics (TPE)*, 2024.

6. **Xinling Yue**, Sundeep Javvaji, Zhong Tang, Kofi A. A. Makinwa, Sijun Du, “A Bias-Flip Rectifier with Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting,” in *IEEE Journal of Solid-State Circuits (JSSC)*, 2023.

7. **Xinling Yue**, Sijun Du, “A Synchronized Switch Harvesting Rectifier with Reusable Storage Capacitors for Piezoelectric Energy Harvesting,” in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 58, no. 9, pp. 2597-2606, Sept. 2023.

8. **Xinling Yue**, Sijun Du, "Performance Optimization of SSHC Rectifiers for Piezoelectric Energy Harvesting," in *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, vol. 70, no. 4, pp. 1560-1564, April 2023.

## Conference Papers

9. **Xinling Yue**, Wenyu Peng, Sijun Du, "A Fully Integrated Adaptive-MPP-Shifting Rectifier for Piezoelectric Energy Harvesting Outputting 580μW at 10V-$V_{OC}$," in *2025 IEEE Custom Integrated Circuits Conference (CICC)*, Boston, USA.

10. Yuchen Wei*, **Xinling Yue***, Zhiyuan Chen, and Sijun Du, "An Inductor-less Capacitor-less Synchronous Piezoelectric-Electromagnetic Hybrid Energy Harvesting Platform with Coil-Sharing Scheme," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, CA, USA, (***Equal Credit Authors***).

11. Shunmin Jiang*, **Xinling Yue***, Yuchen Ma, Chao Wang, and Sijun Du, "A Rectifier-less Piezoelectric Energy Harvesting Interface with a Sense & Track MPPT Achieving Single-Cycle Convergence and 568% Shock Power Improvement," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, CA, USA, (***Equal Credit Authors***).

12. **Xinling Yue**, Yiwei Zou, and Sijun Du, "An MPPT-Integrated Bias-Flip Rectifier for Piezoelectric Energy Harvesting," in *2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*, Bruges, Belgium.

13. **Xinling Yue**, and Sijun Du, "A Single-Stage Bias-Flip Regulating Rectifier with Fully-Digital Fast-MPPT for Piezoelectric Energy Harvesting Achieving 9.3X Power Enhancement and 92.5% End-to-End Efficiency," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, USA.

14. **Xinling Yue**, Yiwei Zou, and Sijun Du, "A Resonant Synchronized Switch Harvesting Rectifier with Bias-Flip Charge Recycling for Piezoelectric Energy Harvesting Achieving 13.9x Power Enhancement," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, USA.

15. Wenyu Peng, **Xinling Yue**, Lukasz Pakula, Sijun Du, "A Capacitor-Based Bias-Flip Rectifier with Electrostatic Charge Boosting for Triboelectric Energy Harvesting Achieving Auto-MPPT at Breakdown Voltage and 14X Power Extraction Improvement," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, CA, USA.

16. Wenyu Peng, **Xinling Yue**, Willen Driel, Guoqi Zhang, Sijun Du, "A 70-V Fully Integrated Dual SSHC Rectifier for Triboelectric Energy Harvesting with Full-Digital Duty-Cycle-Based MPPT Achieving 598% Power Extraction Enhancement," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, USA.

17. **Xinling Yue**, Sundeep Javvaji, Zhong Tang, Kofi A. A. Makinwa, Sijun Du, "30.3 A Bias-Flip Rectifier with a Duty-Cycle-Based MPPT Algorithm for Piezoelectric Energy Harvesting with 98% Peak MPPT Efficiency and 738% Energy-Extraction Enhancement," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, pp. 442-444.

18. **Xinling Yue**, Yiwei Zou, Zhelun Chen, Sijun Du, "A Reconfigurable Cold-Startup SSHI Rectifier with 4X Lower Input Amplitude Requirement for Piezoelectric Energy Harvesting," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, Austin, TX, USA, pp. 649-653.

19. **Xinling Yue**, Sijun Du, "A 2-Mode Reconfigurable SSHI Rectifier with 3.2X Lower Cold-Start Requirement for Piezoelectric Energy Harvesting," in *2022 IEEE International Conference on Electronics Circuits and Systems (ICECS)*, Glasgow, UK, pp. 1-4.

20. **Xinling Yue**, and Sijun Du, "Voltage Flip Efficiency Optimization of SSHC Rectifiers for Piezoelectric Energy Harvesting," in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1-5.

## About the Author

Xinling Yue joined the Electronic Instrumentation Laboratory at Delft University of Technology in December 2020 in Delft, Netherlands, where she spent 4 years pursuing a Ph.D. degree in Microelectronics. Her current research is focused on energy-efficient power management integrated circuits and systems, which include energy harvesting, AC/DC rectifiers, DC/DC converters, and maximum power point tracking techniques.

Her research has resulted in several first-authored publications, including papers presented at the IEEE International Solid-State Circuits Conference (ISSCC) and the Custom Integrated Circuits Conference (CICC), and articles published in the IEEE Journal of Solid-State Circuits, etc. She received the Best Student Paper Award at the 2022 IEEE International Conference on Electronics Circuits and Systems; the Student Travel Grant Award at the 2022 IEEE International Symposium on Circuits and Systems and the 2023 ISSCC; and the 2023-2024 SSCS predoctoral achievement award.

She has been a reviewer for the IEEE Journal of Solid-State Circuits, IEEE Transactions on Power Electronics, IEEE Transactions on Circuits and Systems I, IEEE Transactions on Circuits and Systems II: Express Briefs, and Nature Communications, etc.