Voltage Supply for Liquid Crystal Reconfigurable Intelligent Surface Biasing

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Abstract

Liquid Crystal Reconfigurable Intelligent Surfaces (LC-RIS) are crucial for future millimeter-wave and terahertz wireless systems due to their ability to dynamically control electromagnetic waves. As LC-RIS requires very fast operation, an appropriate voltage supply with good response time must be developed to adjust each element independently. In this work, we present the design and implementation of a custom voltage supply tailored for LC-RIS applications. Our system integrates four daisy-chained LTC2688 digital-to-analog converters (DACs), providing 64 independently adjustable voltage outputs. We achieve a worst-case update time of 273 μs for all outputs, using a Raspberry Pi Pico as the SPI master with minimal C code. The voltage supply meets critical system demands, including the generation of 1 kHz square waveforms, a voltage range of $\pm$10 V, and sub-millisecond response times, while maintaining ease of control through a programmable interface. We also developed a dedicated on-board power supply to meet the LTC2688's multiple power rail requirements, enabling the entire system to operate from a single external input between 3.7 V and 18 V. Furthermore, our design is scalable, allowing multiple boards to be daisy-chained for larger LC-RIS arrays. Our solution demonstrates a compact, fast, and scalable voltage control system suitable for high-performance LC-RIS platforms. **Keywords:** Liquid Crystal Reconfigurable Intelligent Surface; Digital-to-analog converter; LTC2688; Voltage Supply.

1 Introduction

A Liquid Crystal Reconfigurable Intelligent Surface (LC-RIS) is a type of electromagnetic meta-surface that has the capability to manipulate and redirect electromagnetic waves, acting like a tunable reflect-array. Recently, LC-RISs have gained widespread attention, emerging as an essential device for upcoming millimeter wave and terahertz wireless systems [1–5]. While demonstrations of reflect-arrays and predictions regarding their tunability date back to 1963 [6], their large-scale application in mobile networks has only recently been considered [7]. For example, a LC-RIS can establish a link between a transmitter and multiple receivers, even when an obstacle blocks the direct line-of-sight path.

Although extensive research has explored the benefits and challenges of LC-RIS from a signal processing perspective, relatively few practical hardware implementations have been reported. This gap highlights significant limitations in current technology, particularly the inherent trade-offs between bandwidth, response time, and signal loss, which constrain the performance and scalability in real-world applications [8]. In recent implementations of LC-RIS, such as the architecture described in [9], significant limitations remain in terms of responsiveness and scalability. Specifically, the tuning latency of individual radiating elements is relatively high (72 ms), which hinders the system's ability to adapt quickly to dynamic wireless environments, limiting the system to static environments.

Furthermore, the current method of using digital-to-analog converters (DAC) to supply voltage for independently tuning each element introduces considerable delay and lacks efficiency, particularly as the number of controllable elements increases. These limitations underscore the need for an improved control infrastructure. Therefore, this work investigates the following research question:

> *"What is a scalable, low-latency hardware-software solution for controlling high-speed LC-RIS systems?"*

This overarching research question can be decomposed into several sub-questions addressing different technical challenges:

- **Hardware selection**: What design (a DAC or another approach) can provide at least 50 independent output channels with $\geq$ 7-bit resolution?
- **Signal generation**: How can that design produce stable output in the range of $\pm$10 V, represented by a 1 kHz square waveform on all channels simultaneously while still allowing independent control of each?
- **Latency and real-time control**: Can the chosen architecture guarantee a system response time $<$1 ms, and what additional latency is introduced by host-computer software control?
- **Performance validation**: Which measurement methods and instruments will verify sub-millisecond response and high-fidelity square waves, and what tools ensure rigorous, repeatable quantification of waveform quality and timing accuracy?

2 Problem Description

2.1 Background

An LC-RIS (Liquid Crystal–Reconfigurable Intelligent Surface) is a planar array of liquid-crystal cells whose refractive index can be electrically tuned to control the phase and amplitude of incident electromagnetic waves. By programming voltages across the surface, it enables dynamic beam steering and wavefront shaping without mechanical movement.

LC-RIS systems hold promise for diverse applications, including mm-Wave, THz, and visible light communication [10, 11], where LC technology is already well established. However, implementing LC-RIS at mm-Wave frequencies presents challenges due to the inherently slow response times (in the order of milliseconds), temperature sensitivity, and moderate insertion loss of LC materials.

From a hardware perspective, it consists of numerous radiating elements placed on a surface, which can be individually tuned so that they can propagate an electromagnetic wave (EM) in a desired direction. Because of constructive and destructive interferences, this principle is at the heart of how RIS steer beams and shape radiation patterns.

The system that this research paper will focus on is the one presented earlier by Neuder et al. [9]. The presented LC-RIS

is based on an architecture with compact defected delay lines that provide continuous, 360-degree tunability, exhibiting response times of 72 milliseconds, insertion losses below 7 dB, and a 6.8 GHz (10.9%) bandwidth at 62 GHz, all while utilizing a lossy glass substrate and gold as a conductor.

2.2 Current Voltage Biasing Setup

The LC-RIS system uses the Texas Instruments DAC60096EVM evaluation module for voltage biasing [12], controlled via Python. This board integrates the DAC60096, a low-power, 96-channel, 12-bit DAC [13], offering un-buffered bipolar outputs up to ± 10.5 V. It supports simultaneous update/clear and external triggers for generating square waves. However, this evaluation board is now discontinued and introduces significant latency compared to newer alternatives.

A DAC converts binary input into continuous analog voltage. The resolution N defines the number of discrete levels (2^N) over a given voltage range. The least-significant bit (LSB), the smallest output change, is:

$$LSB = \frac{V_{max} - V_{min}}{2^N}$$

For a 12-bit DAC over 30 V, each step is about 7.32 mV. Figure 1 illustrates how resolution affects waveform fidelity, showing the relationship between digital input codes and quantized output levels.

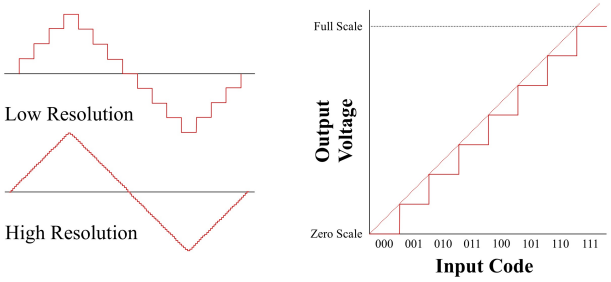

Figure 1: Effect of DAC resolution on output waveform and voltage levels.

Each DAC channel biases one LC-RIS radiating element, enabling precise per-element control for dynamic EM wave manipulation.

2.3 Formal Problem Description

The objective of this research is to design, develop, and integrate a novel voltage supply architecture tailored for the reference LC-RIS system. The proposed solution aims to address the limitations of the existing DAC60096EVM-based configuration, which suffers from high latency and limited availability. The new design must satisfy or surpass the following performance criteria to ensure suitability for high-speed, high-resolution RIS tuning:

- **Scalability:** Independent voltage control for at least 50 output channels to support dense meta-surface arrays;
- **Software Integration:** Full controllability via a software interface, preferably through a Python script for ease of integration with existing control scripts;
- **Signal Generation:** Capability to output square-wave signals at frequencies up to 1 kHz for dynamic modulation of the RIS elements;
- **Voltage Range:** Support for bipolar output voltages with a minimum range of ± 10 V;
- **Resolution:** Minimum effective resolution of 7 bits to ensure adequate tuning granularity;
- **Response Time:** Voltage update latency of less than 1 ms to enable real-time reconfiguration;
- **Form Factor:** Compact hardware design with a footprint preferably smaller than 15 cm $\times$ 15 cm to facilitate integration into existing LC-RIS platforms.

3 System Design and Implementation

3.1 Survey of Alternative Solutions

Before evaluating alternative voltage generation schemes to replace the DAC60096EVM, the system's output requirements must be clearly defined. The desired architecture must support an arbitrary number of independent channels, each capable of producing a 1 kHz square waveform at user-adjustable amplitudes, with amplitude transitions completed in under 1 ms.

The initial approach seeks a direct DAC replacement that matches the DAC60096's channel count yet offers improved response time. A survey of current products (e.g., Analog Devices' DAC selection guide) reveals a scarcity of standalone DACs providing more than 50 channels, rendering such replacements impractical [14].

An alternative architecture employs one or more microcontrollers to generate the square waveform via general-purpose input/output (GPIO) pins. For instance, three Raspberry Pi Pico boards (each featuring a 133 MHz core and 23 GPIOs) could collectively provide 69 independent outputs [15]. However, the fixed logic-level amplitudes (0 V/3.3 V) violate the +-10 V requirement. This limitation can be addressed by appending a level-shifting amplifier stage and an adjustable voltage divider, in which a digital potentiometer replaces one resistor to vary the amplitude dynamically. Although functional, this solution multiplies component count and control-pin overhead, as each channel requires an amplifier, potentiometer, and dedicated interface lines.

Component count may be reduced by replacing GPIO-based waveform sources with a single fixed-frequency oscillator, such as the LTC6900C (1 kHz-20 MHz). The oscillator's output can drive multiple level-shifter/divider pairs, simplifying PCB layout and reducing micro-controller pin usage. Nevertheless, digital potentiometers exhibit limited speed (optimized for DC or slow adjustments), poor tolerance ($\pm 20\%$), and temperature-dependent drift [16, 17]. A multiplying DAC can fulfill the role of a precision, high-speed digital potentiometer without these drawbacks [18].

A more scalable topology employs multiple lower channel DACs, each individually controllable yet connected via

a daisy-chain SPI bus. In a daisy-chain configuration, each slave device propagates its input command (DIN) to its output (DOUT) one command cycle later, executing the command only upon reception of a rising edge on active-low CS. This scheme enables every DAC in the chain to receive distinct commands while requiring only three micro-controller signals (SS, SCK, MOSI) for control.

Once a suitable DAC family is selected, the generation of the required square waveform can leverage the device's native toggle mode. Many multi-register DACs offer two voltage registers (A and B) per channel. By programming Register A with the high-level amplitude and Register B with 0 Volts, and then applying an external 1 kHz clock signal, the DAC alternates its output between the two levels, producing the desired square wave.

3.2 Detailed DAC Specifications

A suitable DAC must be chosen from the many devices available on the market. To make an informed decision, it is essential to understand how DACs operate, the various architectural topologies they employ, their settling-time characteristics, and the parameters that define their output amplitude. In addition, common sources of output error, such as transition glitches, thermal and quantization noise, and power-supply coupling, must be identified, and appropriate mitigation strategies (for example, output filtering, segmentation, or dithering) should be considered. The SPI digital-communication interface is also critical: timing diagrams from DAC data-sheets must be interpreted, and the overall system response time estimated by combining SPI-transfer latency with analog settling time.

There are several DAC architectures available. In this paper, only one of the available topologies is discussed: the R-2R ladder DAC, which is going to also be used in the current solution implemented in this research project. The R-2R ladder DAC (Figure 2 consists of a repeating network of resistors of values R and 2R. Each digital input bit switches its node to the reference voltage (logic "1") or ground (logic "0"), generating binary-weighted currents that sum at the output node to produce an analog voltage. Because all resistor ratios are identical, the DAC achieves excellent linearity, low noise, and constant ladder impedance. However, simultaneous bit-switching can produce glitch impulses, and the instantaneous reference current varies with the input code, placing demands on the reference buffer.

In an ideal DAC, the output voltage would follow a perfectly linear transfer function. In reality, however, no DAC is ideal: each device exhibits some level of overall error. Six typical error components contribute to this non-ideal behavior: zero-scale error, full-scale error, integral nonlinearity (INL), differential nonlinearity (DNL), offset error, and gain error. In addition, any DAC's observed error can be influenced by signal-chain components external to the DAC itself (e.g., source impedance, buffer amplifiers, or PCB layout).

Multi-channel DACs often support daisy-chain operation to minimize micro-controller I/O. In this mode, all chip-select (CS) pins are tied to one line, and MOSI and SCLK are shared. While CS is low, each device shifts 16 bits into its register and passes subsequent bits from its DOUT to the next device's DIN. Once CS returns high, all devices simultaneously latch and execute their new codes; raising CS early aborts the transfer. Figure 3 shows a 3-DAC chain with 16-bit instructions.

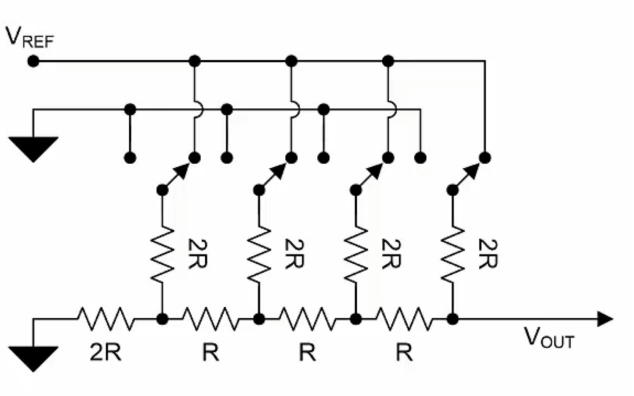

Figure 2: R-2R ladder DAC architecture.

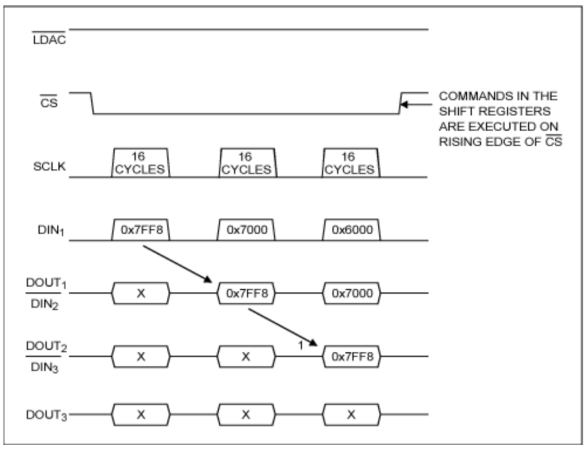

Figure 3: SPI daisy-chain timing for three 16-bit DAC instructions.

Finally, the timing characteristics, throughput speed and settling time, dictate the practical sample rate of any DAC. Throughput speed is limited by the serial interface: for an SPI-based device with clock frequency f_{SCLK} and N_{bits} per word, the minimal digital transfer time is N_{bits}/f_{SCLK} , plus any required chip-select setup and hold times. However, after latching a new code, the DAC's internal ladder and output amplifier require a finite settling time, t_{settle}, to reach within a specified error band (often +-1 LSB or +-2 LSB) of the final value. In high-accuracy applications, t_{settle} typically exceeds the digital transfer interval. For instance, a 16-bit, 50 MHz SCLK DAC like the MAX5717 might achieve a theoretical digital update interval of approximately 480 ns but requires 0.75 μs to settle. Therefore, even though the SPI interface could nominally permit a 2 Msps update rate, the effective sample rate is limited to about 1.33 Msps by the settling time.

3.3 DAC Chip Selection

The LTC2688 (16 channel, 12-bit resolution, $\pm 10/\pm 15$ V output range) was chosen to replace the discontinued evaluation board of the DAC60096 [19]. Eight-channel alternatives (LTC2666, DAC61408) would require twice the devices, increasing PCB area and daisy-chain latency. The AD5516-3 (36 μs settling, 93 μs for 64 channel SPI update) and DAC61416 (higher bipolar zero, gain, DNL/INL errors) under-perform relative to the LTC2688's 21 μs settling and 62 μs throughput. Its superior speed, integration density, and accuracy make the LTC2688 optimal for the LC-RIS system.

One distinguishing feature of the LTC2688 is its dual input registers (A/B) and hardware toggle pins, enabling rapid waveform switching or dithering. In this work, toggle mode generates a 1 KHz square wave. Its SPI interface accepts logic levels down to 1.71 V, runs up to 50 MHz, and supports daisy-chain operation. SPI transactions consist of a 32-bit instruction word, which can represent for example to set the value of a channel of the DAC. After each update, the analog output settles within tolerance in approximately 21 μs. By daisy-chaining four LTC2688s, one can address 64 channels over a single SPI bus. Updating all channels involves sending four consecutive 32-bit frames at 50 MHz (one per device) for each channel index, for a total of 16 repeats. Thus, the total update time in the daisy-chain configuration becomes:

$$t_{frame} = (t_{SCLK} \cdot N_{bits} \cdot N_{devices} + t_{CS,high})$$

$$t_{update,daisy} = t_{frame} \cdot N_{channels} + t_{settle}$$

The legacy DAC60096EVM system requires two SPI commands per channel, resulting in greater transmission overhead. Additionally, the maximum SPI clock frequency of this board is 32 MHz. Its per-channel update time is longer, and the analog settling time is approximately 65 μs. The total update time of updating 64 channels, including settling, can be estimated using the above equation at 161 μs. To update only one channel, the update time would be 67 μs.

In contrast, the proposed system using the LTC2688 achieves the same 64 channels update in 62 μs. To update only one channel, it would update in just 24 μs, as the analog settling time is approximately 21 μs. Moreover, the daisy-chain configuration simplifies wiring and allows scalable expansion without a proportional increase in control overhead.

3.4 Power Supply

To meet the LTC2688's precision requirements, the system uses a two-stage regulation scheme [20, 21]. A switching regulator provides coarse bipolar rails, followed by linear post-regulation for low noise.

The LTM8049 μModule delivers isolated ± 18.5 V from a 3.7 to 18 V input [22], minimizing board area and confining switching noise. The LT3032 LDO then regulates this to ± 18 V with high PSRR and low output noise [23].

A separate 5 V analog logic rail is supplied by the low-noise LT1763-5 [24]. The digital logic supply (1.71 to 5 V) is jumper-selectable from either the SPI master or the analog logic rail.

A shared LT6656-4.096 reference replaces the DACs' internal references for consistent output across devices [25].

Finally, a 1 kHz toggle signal is generated by the LTC6900 oscillator, providing low-jitter switching independent of the host [26].

3.5 PCB and Circuit Schematic

The design, based on Analog Devices' DC2873A reference, was captured in the EasyEDA software, placing four LTC2688 DACs in a daisy-chain to yield 64 outputs, alongside the LTM8049, LT3032, LT1763-5 and LT6656 regulators. A single 8-pin SPI header provides control, while jumpers enable bypassing each regulator for external supplies and in-circuit debugging. Multiple boards can be daisy-chained via SPI pass-through headers. Layout follows each IC's datasheet: close-placed bulk and ceramic decoupling caps, a continuous ground plane (with isolated DAC outputs) for efficient thermal dissipation, separated analog and digital routing, thermal reliefs, an error-flag LED for each DAC, and MUX-pin headers for per-channel testing. Finally, the completed schematic was laid out, routed for controlled impedance, exported as Gerbers and stencil, and assembled via lead-free reflow (peak 235 °C) to produce functional prototypes.

Board dimensions are 121.9 mm × 103.3 mm, satisfying the project's mechanical constraints. The total cost for a five-board panel was €29.22, with an additional €6.14 for the stencil; population of all power-supply and DAC components incurred approximately €250 in parts. Complete BOMs (Bill of Materials), detailed PCB assembly drawings are available in the appendix of this thesis, and the Gerber files are available in the accompanying GitHub repository [27].

3.6 SPI Communication Implementation

To interface with four LTC2688 DACs in a daisy-chain configuration—thereby generating synchronized per-element voltages and a 1 kHz square-wave across the LC-RIS—the SPI command set defined in the LTC2688 datasheet must be employed [19]. Each SPI transaction consists of a 32-bit word structured as follows:

- **Bits [31:28]**: 4-bit operation code
- **Bits [27:24]**: 4-bit channel/address field
- **Bits [23:8]**: 16-bit data payload
- **Bits [7:0]**: 8-bit padding (can be used for error detection - cyclic redundancy check)

A complete daisy-chain update requires transmitting four consecutive 32-bit words (one per DAC), for a total of 128 bits.

The following commands are used to configure and drive the DAC chain:

- **Select register A/B** (opcode 9): choose the active register for subsequent writes
- **Write toggle/dither enable** (opcode 11): enable per-channel toggle or dither modes
- **Configure channel settings** (opcode 15): specify toggle-pin source (e.g. TGP0) and output span (e.g. ± 15 V)

- **Write code and update channel** (opcodes 4 and 15): load 16-bit voltage code into the selected register and update the output
- **No operation** (opcode 32): maintain current state (used to pad inactive devices in the chain)

At power-up a single broadcast sequence configures all DACs for a ±15 V span using TGP0 as the 1 kHz clock (opcode 15), selects register B (opcode 9) and writes mid-scale code 2048 to every channel (opcode 15), then re-selects register A (opcode 9) and enables toggle mode (opcode 11). Thereafter each channel alternates at 1 kHz between its A (high) and B (low) register values. Either register may be updated at any time by issuing a burst of four 32-bit commands—one per DAC — without disabling toggle mode or reconfiguring the hardware.

Complete implementation of the SPI communication protocol is available in the thesis's GitHub repository [27].

4 Experimental Setup and Results

The LC-RIS control system was evaluated in two phases: first, verifying the power supply rails and the 1 kHz reference clock; second, characterizing the LTC2688 DAC array under dynamic conditions. All measurements were performed with a Rigol DS1054Z oscilloscope.

4.1 Reference Voltage Configuration

The external reference LT6656 was omitted due to the PCB footprint mismatch; each LTC2688 used its internal 4.096 V reference via jumper selection.

4.2 Power Supply Verification

To confirm the analog and logic power rails of the DAC, a 12 V input was applied to optimize the efficiency of the LTM8049 to generate ± 18.5 V. The following supplies were measured, which directly power the LTC2688s, as depicted in figure 4:

- **+18 V Analog Rail:** Supplies the positive analog voltage for the LTC2688. Supplied by the positive output of the LT3032. Measured at 17.8 V.
- **–18 V Analog Rail:** Supplies the negative analog voltage for the LTC2688. Supplied by the negative output of the LT3032. Measured at –18.2 V.
- **+5 V Logic Rail:** Provides the analog logic voltage level for the LTC2688. Supplied by the output of the LT1763. Measured at 5.01 V.

These measured voltages satisfy the LTC2688's ±17.2 V minimum requirement for ±15 V DAC output operation. As for the analog logic voltage range, the LTC2688 requires a voltage between 4.75 and 5.25 Volts, which is also satisfied.

4.3 Reference Clock Verification

The LTC6900 output measured 994 Hz (Figure 5), providing a stable near 1 kHz toggle for the DAC register toggle operation. As it is powered from the digital voltage logic coming from the SPI master, the low base is centered around 0 V and the top base of the signal at the logic level of the SPI master, in this case 3.3 V.

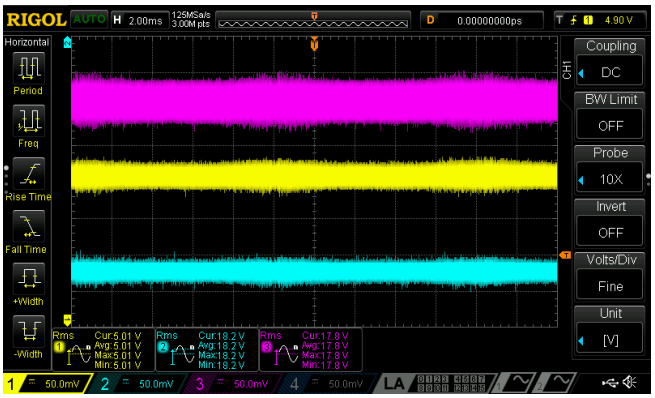

Figure 4: Oscilloscope traces of +17.8 and -18.2 analog rails (pink/blue) and 5.01 V logic rail (yellow).

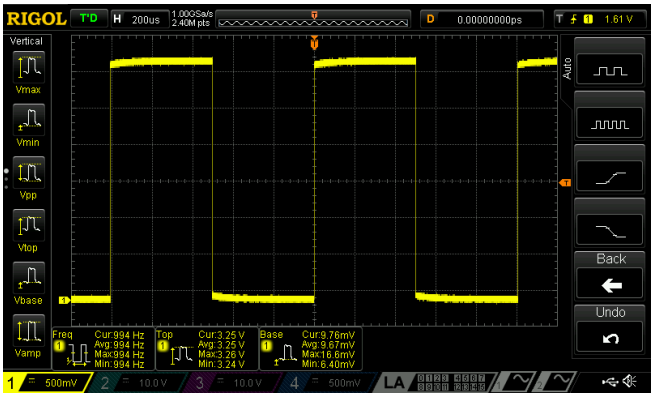

Figure 5: LTC6900 oscillator output (994 Hz).

4.4 DAC Dynamic Performance

The LTC2688 DAC array's dynamic performance was evaluated via waveform accuracy, linearity, and latency tests to assess its suitability for real-time beam steering and reconfigurable surfaces. Experiments included static single-channel updates for fixed-voltage accuracy; accuracy comparisons across daisy-chained DACs using internal references; 1 kHz square-wave generation via register toggling; best-case latency tests with single-channel extreme-voltage switching; and worst-case latency assessments through full-array cycling. These measurements inform the design's limitations and optimization strategies for practical deployments.

Static Channel Update

A single LTC2688 channel was programmed to an arbitrary digital code to evaluate static output characteristics, including offset error and noise, without toggle-mode enabled. Figure 6 shows the output when the channel is set to code 200 (nominal –13.54 V), yielding a voltage of –13.59 V. The measured duty cycle is exactly 50 %, indicating equal time spent at the two quantized levels.

The output oscillates between –13.60 V and –13.57 V, characteristic of quantization noise. In this case, for an LSB size of 7.324 mV, the peak quantization error is half an LSB (±3.662 mV). Figure 6 places vertical cursors at the upper

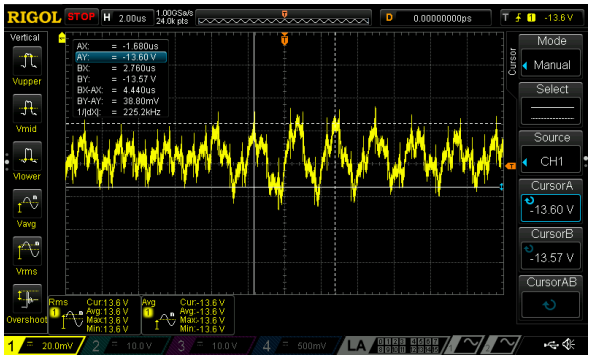

Figure 6: Static output with code 200: expected –13.54 V, measured –13.58 V.

and lower noise extrema, confirming that the observed ±15 mV deviation closely aligns with the theoretical quantization error, with the remaining discrepancy likely attributable to noise introduced by the measuring device.

The full transfer characteristic was obtained by sweeping the code from 0 (–15 V) to 4095 (+15 V). Figure 7 plots the sampled output (blue dots) against the ideal linear response (orange line). One systematic errors is evident: offset error (vertical shift at the majority of codes). This error can be calibrated (see Section 6).

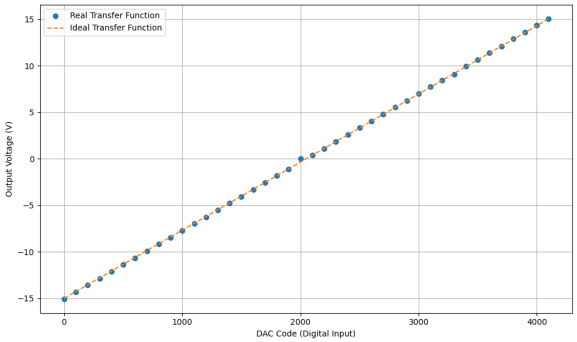

Figure 7: Sampled transfer function (blue) vs. ideal response (orange) for codes 0–4095.

Impact of Using Internal Reference

Employing the LTC2688's internal voltage reference introduces device-to-device variations in the output voltage at a given digital code, owing to tolerances in the internal reference circuits. An external reference was not feasible in this setup due to footprint mismatches; therefore, the inherent variations are characterized here. Figure 8 shows the outputs of four daisy-chained LTC2688 channels, all set to code 0. The maximum deviation between RMS (root mean square) voltages is 100 mV.

Square-Wave Signal Generation

The LTC2688 was configured in toggle-mode operation to generate a 1 kHz square waveform by alternately loading two DAC registers (register A and register B) with digital codes 0 and 2890, corresponding to output voltages of 0 V and 6.17 V,

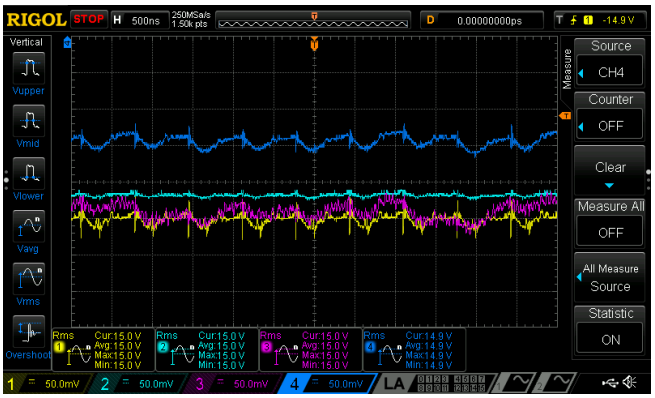

Figure 8: Measured outputs for four LTC2688 devices in a daisy-chain, each set to code 0 (nominal -15 V): -15.05 V (yellow), -15.04 V (pink), -15.02 V (aqua), -14.95 V (blue).

respectively. A 1 kHz clock signal was applied to the DAC's toggle pin, yielding a measured waveform frequency of 992 Hz. Figure 9 presents the captured waveform; note the presence of a small offset error, with the low-level RMS voltage measured at –20 mV and the high-level RMS voltage at 6.22 V.

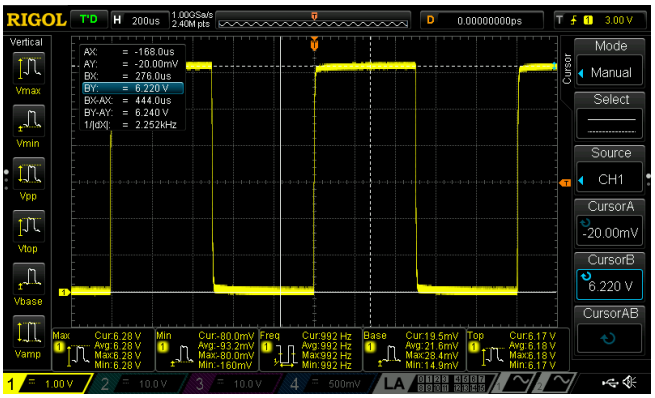

Figure 9: Square-wave output of a single LTC2688 channel (code 2890), expected +6.17 V, measured at +6.22 V with frequency of 992 Hz.

Figure 10 illustrates the waveform when switching between codes 0 and 4095 every 117.6 ms, while maintaining toggle-mode active continuously. This switching pattern reflects the dynamic voltage changes required by the LC-RIS in practical operation, where channel voltages must be updated periodically to steer electromagnetic waves.

Response Time – Best and Worst Case Scenarios

This subsection quantifies the overhead introduced by different hardware platforms and software environments used to drive the SPI master interface (see Table 1). Measurements were performed on a Raspberry Pi 5, a Raspberry Pi Pico, and a PC equipped with an FT232H USB-to-SPI converter. Three code variants were evaluated on each platform:

1. **Minimalist implementation**: SPI commands are defined explicitly as byte sequences (e.g., enable toggle

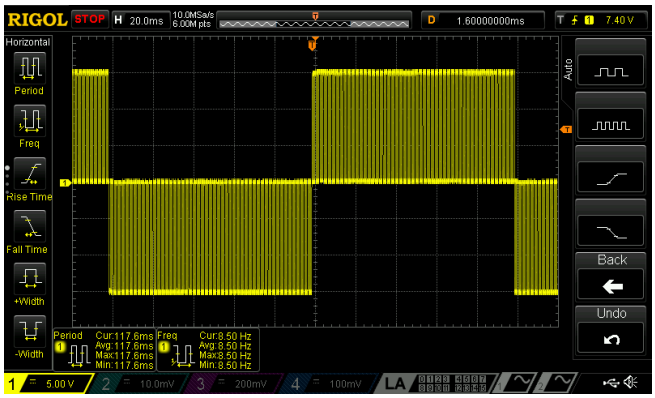

Figure 10: Square-wave output of a single LTC2688 channel, toggling between codes 0 and 4095 every 117.6 ms.

mode, select ±15 V output range, set channel output).

2. **Object-oriented (OO) framework**: All LTC2688 instructions (per the datasheet) are encapsulated in classes, including logic for mapping logical channel indices to daisy-chain positions and a command queue for batch updates.
3. **Minimalist C**: The minimalist approach re-implemented in C (for Raspberry Pi 5 and Pico only) to isolate driver-level overhead from interpreter overhead.

All tests used an SPI clock frequency of 25 MHz. Response times include both the SPI transaction duration and the DAC settling time (21 μs for full-scale transitions).

In analyzing the bast-case scenario of the response time, only one channel on a single LTC2688 is updated. Each SPI transaction remains 128 bits long (32 bits per device), with no-operation commands issued to the other three devices in the daisy chain. Full-scale code transitions (0 to 4095) were employed to capture the maximum settling-time component.

When analyzing the worst-case scenario, all 16 channels on all four daisy-chained LTC2688 devices are updated. Since each 128-bit instruction can configure one channel per DAC, a complete update of all channels requires 16 sequential instructions.

Raspberry Pi 5 tests employed the `spidev` driver under Linux. Context switching and interrupt handling inherent in `spidev` introduce significant overhead for short SPI transfers. The OO Python framework adds approximately 0.6 ms relative to the minimalist Python code, while the difference between minimalist C and Python is minimal—indicating that driver overhead dominates over language execution speed.

On the Raspberry Pi Pico, the minimalist MicroPython code achieves performance comparable to the Raspberry Pi 5's Python implementation ($\approx$ 39 μs difference). Direct access to the hardware SPI peripheral in the minimalist C implementation approaches the ideal response times. In contrast, the OO MicroPython framework incurs substantial latency ($\approx$81 ms) due to interpreter overhead and data-structure management on the resource-constrained Pico.

Measurements using the FT232H and the Adafruit Blinka USB-to-SPI library on a PC reveal best-case response times of 1.4–1.5 ms. USB host controller polling (High-Speed mode) imposes a minimum round-trip latency of approximately 1 ms. The OO Python implementation adds another 200–300μs. Given the theoretical USB-2.0 HS wire-rate of 480 Mb/s, substantial performance improvements may be achievable via lower-level drivers or native code.

Device	**Best Time** μs	**Worst Time** μs
Ideal	26	103
Raspberry Pi 5 (minimalist C)	50	813
Raspberry Pi 5 (minimalist Python)	60	974
Raspberry Pi 5 (OO Python)	99	1600
Raspberry Pi Pico (minimalist C)	40	273
Raspberry Pi Pico (minimalist MicroPython)	57	935
Raspberry Pi Pico (OO MicroPython)	3680	82120
PC + FT232H (minimalist Python)	1430	24050
PC + FT232H (OO Python)	1780	24250

Table 1: SPI response time comparison across platforms at 25 MHz.

5 Responsible Research

All stages of the investigation—including the specification of performance targets, selection and evaluation of DAC architectures, design and simulation of the power-supply circuitry, and hardware validation—are documented in full. Circuit schematics, PCB layouts, firmware source code, simulation files, and raw measurement data have been archived in the project repository [27], ensuring that each step of the development process can be traced and reproduced.

5.1 Principles

This work complies with the five core principles of the Netherlands Code of Conduct for Research Integrity—honesty, scrupulousness, transparency, independence, and responsibility [28].

- **Honesty:** Design decisions are reported sequentially, from the initial problem statement and evaluation of alternative DAC chips to the final choice of a daisy-chain solution based on four LTC2688 devices. Power-supply performance was verified by LTspice simulation (Analog Devices) and by direct measurement on the assembled board; results confirm compliance with all specifications.

- **Scrupulousness:** Professional instrumentation (Rigol DS1054Z oscilloscope) was used for waveform and timing measurements, with export of raw data for figure generation. Circuit schematics and PCB layouts were created in EasyEDA and subjected to systematic review.
- **Transparency:** All design artifacts - Gerber files, circuit schematics, PCB layouts, LTspice simulation files, firmware code, and configuration instructions (including jumper settings) - are publicly accessible in the thesis GitHub repository. Accompanying documentation explains how to reproduce, customize, and extend the system.
- **Independence:** Component selection and architectural choices are grounded in objective criteria derived from datasheets, performance benchmarks, and peer-reviewed literature. Each decision is supported by empirical or theoretical evidence.
- **Responsibility:** As the impact of an improved voltage supply for the LC-RIS to improve the responsiveness has been noted, we need to also consider tradeoffs of the current design. The proposed design delivers 64 channels at an estimated cost of €285, compared to the discontinued DAC60096EVM (96 channels, €300 - €315). Daisy-chain capability enables scalable expansion. Datasheet analysis predicts a two-to-three-fold improvement in settling time, and firmware optimizations ensure a response time below 1 ms, satisfying the response time requirement ($\geq$ 50 channels) and future growth.

5.2 Reproducibility

Complete access to all artifacts — source code, Gerber files, schematics, and simulation projects — ensures that the voltage-supply system can be replicated or adapted. Detailed README files describe board functionality, jumper configurations, firmware operation, and guidelines for parameter adjustments. Assembly recommendations advocate the use of professional reflow equipment or contract manufacturing services to mitigate the risk of soldering defects.

5.3 Ethics

The primary objective of this research is to develop an improved voltage-supply system that enhances the responsiveness of the reference LC-RIS platform. However, the potential for malicious exploitation of LC-RIS technology necessitates careful ethical consideration. An LC-RIS operates by redirecting an incident electromagnetic wave through constructive and destructive interference: by applying specific phase shifts across its passive elements, it can steer a high-intensity beam in a desired direction. Conversely, an adversary could configure the surface to impose destructive phase relationships, thereby increasing noise or entirely canceling a target signal. This technique, known as destructive beamforming, can severely degrade communication links by reducing the signal-to-noise ratio below recoverable levels.

Moreover, a low-cost, reconfigurable intelligent surface can execute such attacks without emitting any additional signals, effectively jamming communications while evading conventional detection mechanisms, particularly if the attacker possesses accurate channel state information [29]. While simple jamming can be countered by boosting transmit power or improving receiver sensitivity, stealthy destructive beamforming presents a far more insidious threat that is difficult to detect or mitigate. Further research is therefore required to develop reliable detection methods, resilient communication protocols, and robust countermeasures against malicious LC-RIS deployments.

6 Discussion

6.1 Accuracy and Precision

The channel outputs exhibit deviations from ideal behavior, including noise, offsets, and transient responses that degrade signal quality. Figure 8 reveals a systematic offset between the programmed and measured values. Additionally, gain errors may be present in other DAC devices. The LTC2688 provides per-channel commands for offset and gain adjustment; by calibrating each channel individually, the transfer function can be aligned closely with the target output.

Quantization noise is determined by the DAC's least significant bit (LSB) size. Mitigation strategies include selecting a DAC with higher resolution or reducing the full-scale voltage range. Since constraining the voltage range is impractical in this application, increasing resolution is the preferred approach, albeit with longer settling times. The LTC2688's 16-bit resolution corresponds to a quantization step of ± 228.88 μV, while its full-scale settling time is 28 μs for a full-scale code change.

Using the internal reference voltage introduces device-to-device variation at identical digital codes, necessitating individual calibration for offset and gain errors across the daisy-chain. An external reference can standardize the voltage across all DACs and permits flexibility in the output range. However, external references can increase susceptibility to noise and represent a single point of failure. Providing the option to select either the internal or an external reference voltage enhances design flexibility and supports alternative system configurations.

6.2 DAC Response Time

Table 1 summarizes the measured response times for various SPI master implementations. Any software abstraction—user interfaces, complex data structures, or high-level libraries—introduces latency that deviates from the ideal response. A minimal implementation on a Raspberry Pi Pico, which operates without an operating system and supports real-time execution, yields a worst-case response of 273 μs when programmed in C, comfortably below the 1 ms requirement.

USB-to-SPI converters and general-purpose operating systems (e.g., Windows or Linux) introduce additional latency due to driver overhead and scheduling non-determinism. To minimize response time, the SPI master must operate as close to the hardware as possible: chip-select timing should be managed manually, interrupts should be minimized, and ded-

icated low-level SPI routines should replace high-level abstractions.

Further investigation may explore the trade-offs of different hardware platforms and operating environments, as response times can range from hundreds of microseconds to several milliseconds depending on system architecture.

6.3 Thermal Considerations

Thermal management is critical for both the LTC2688 and the LTM8049 power module. Heatsinks and forced convection (fans) are recommended, particularly for the LTM8049, which dissipates substantial power despite a copper ground plane for heat spreading. If the device temperature exceeds 125 °C, the LTM8049 engages thermal shutdown, disabling switching and discharging its soft-start capacitor until the module cools. Repeated activation of thermal shutdown may compromise long-term reliability.

The LTC2688 includes internal overtemperature protection at approximately 160 °C; each channel has an independent temperature sensor that drives the shared FAULT pin low. LEDs connected to each FAULT pin provide a visual indication of thermal or communication faults. The LTM8049's power good (PG) output signals proper operation by remaining high; a low level indicates a fault on the power rail.

6.4 LTC6900 Frequency

The LTC6900 was configured for a 1 kHz output using a 2 MΩ resistor, as specified in the datasheet. However, due to component tolerances, the measured frequency was 992 Hz. To correct for such deviations, an adjustable resistor can be added in place of or in series with the fixed resistor. This allows fine-tuning of the resistance to precisely calibrate the output frequency to 1 kHz, compensating for variations in resistor and IC tolerances.

6.5 Scalability and Feature Extensions

The system architecture supports flexible feature enhancements and expansion. The existing LTC2688 devices can operate in 16-bit mode with minimal firmware modification to accommodate the wider data width. Dedicated headers and jumpers enable the substitution of power rails ($\pm$18 V analog, 5 V logic, 4.096 V reference, and the LTC6900 oscillator output) with external sources for improved performance or redundancy.

The LTC6900 oscillator frequency can be selected among preset values (1 kHz, 10 kHz, or 100 kHz) via jumpers or configured over a 1 kHz to 20 MHz range by choosing appropriate resistor values, as specified in the datasheet. This flexibility allows the system to adapt to different modulation requirements without extensive circuit redesign.

Multiple boards can be daisy-chained by routing the SPI data output of the last DAC on one board to the data input of the first DAC on the next board, while sharing the clock and chip-select signals. With the current 273 μs response time per board, four boards can be chained and still meet the 1 ms update constraint. Optimizations in SPI interface timing and firmware can further reduce overall latency.

7 Conclusions and Future Work

This work presents the design and implementation of an alternative voltage supply system for the LC-RIS platform developed by Neuder et al.[9], intended to replace the discontinued and slow-response DAC60096 evaluation board. The proposed system addresses several key technical requirements, including: independent control of at least 50 voltage output channels, software programmability (preferably Python-compatible), generation of a 1 kHz square waveform, voltage range of at least ± 10 V, a minimum resolution of 7 bits, and rapid voltage updates with a response time below 1 ms.

The solution employs four LTC2688 digital-to-analog converters configured in a daisy-chain arrangement. Each LTC2688 offers 16 output channels with 12-bit resolution and configurable voltage ranges of ± 10 V or ± 15 V, yielding a total of 64 independently controlled channels. With a full-range voltage settling time of 21μs and an SPI clock of up to 50MHz, the theoretical minimum time to update all channels is approximately 62 μs.

An LTM8049-based supply generates a bipolar $\pm$18 V rail for the LTC2688, the LT1763 provides a 5 V analog rail, and an LTC6900 oscillator produces a 994 kHz square-wave register-toggle signal. The LTC2688 output measures 992 Hz, in close agreement with the 1 kHz design target.

The overall response time of the system is highly dependent on the performance of the SPI master interface. While the hardware supports fast updates, software overhead introduced by high-level abstractions can significantly degrade performance. The best experimental response time, using a Raspberry Pi Pico with minimal C-based firmware and a 25 MHz SPI clock, achieved an update latency of 273μs—considerably above the theoretical limit of 103μs. This result suggests that substantial improvements are possible through further optimization of the firmware and communication protocol.

Future work includes exploring more efficient low-level SPI implementations, potentially leveraging FPGA-based controllers or real-time micro-controller platforms to approach the theoretical speed limits. Additional considerations could include the thermal management of the power supply components, integration with software libraries for dynamic control, and experimental validation of the LC-RIS behavior under fast-switching voltage waveforms in real-world electromagnetic scenarios.

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A Appendix

This appendix provides all supporting technical documentation relevant to the LTC2688 board developed for this research project. The information herein includes:

- **Circuit Schematics**: Detailed schematics of the LTC2688-based system, illustrating the daisy-chained configuration of the four DACs. It also includes the power supply management circuitry essential for stable and precise operation of the board.
- **Bill of Materials (BOM)**: A comprehensive list of all components used in the design and assembly of the board. This includes part numbers, quantities, values, package types, and manufacturers to facilitate sourcing and replication.
- **PCB Footprint and Layout**: The layout and footprint design of the PCB, highlighting placement of each component, signal routing, and power distribution. This section is critical for understanding board assembly and potential modifications.
- **Function Description**: Detailed functional overview of each key component and interface on the LTC2688-based system board, outlining their roles in power management, signal routing, and control configuration.

This appendix serves as a complete reference for both replication and future development efforts related to the LTC2688-based power supply solution for the LC-RIS system.

A.1 Circuit Schematic

Figures 12 through 17 present the detailed circuit schematics of the LC-RIS system, offering a comprehensive overview of the electrical architecture that enables its functionality. These schematics illustrate the configuration of the on-board power supply, which includes the integration of the LTM8049 for dual-rail voltage generation with the post-processing offered by the LT3032 LDO and the LT1763 low-dropout regulator for stable analog logic supply. The figures also highlight the jumper-based selection mechanisms that allow for flexible switching between internal and external power sources for the various supply rails, reference voltages, and logic levels, ensuring compatibility and adaptability depending on system requirements. Additionally, the schematics depict the daisy-chain topology employed to connect four LTC2688 DACs in series, enabling coordinated signal output across all radiating elements. The synchronization of these DACs is achieved through the use of an LTC6900 oscillator, which generates a stable clock signal used to operate the system in toggle mode. This architectural arrangement ensures precise timing control and programmable signal behavior necessary for the dynamic electromagnetic wave manipulation performed by the metasurface.

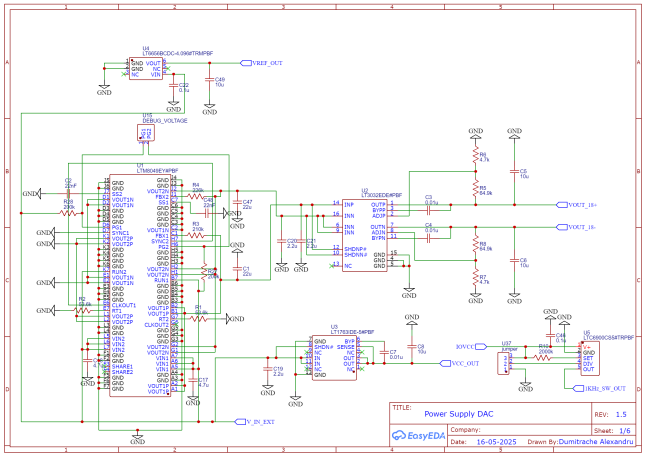

Figure 11: Circuit Schematic (Sheet 1) - Power supply

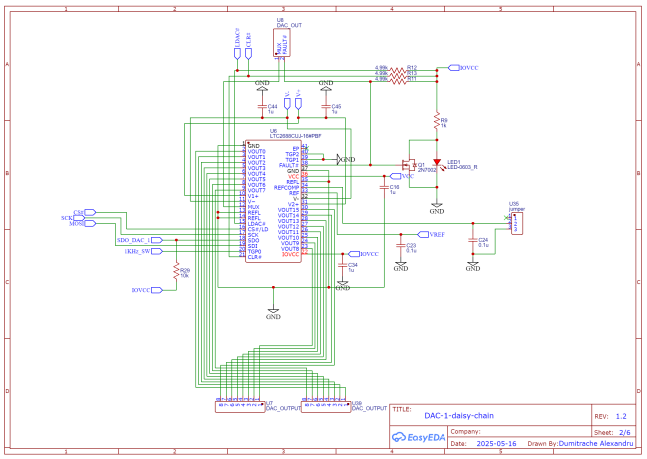

Figure 12: Circuit Schematic (Sheet 2) - DAC 1 in daisy-chain

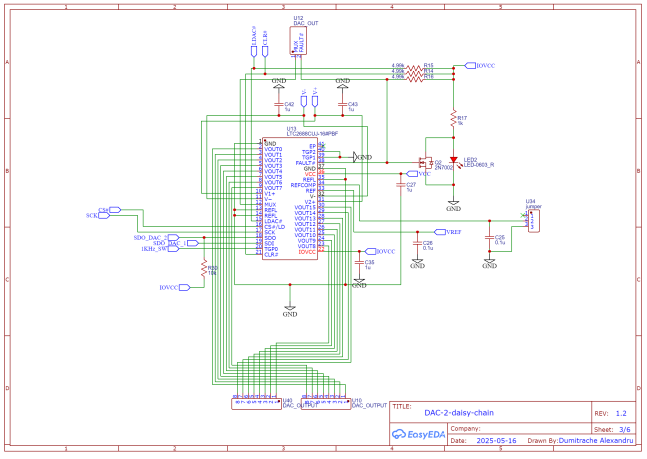

Figure 13: Circuit Schematic (Sheet 3) - DAC 2 in daisy-chain

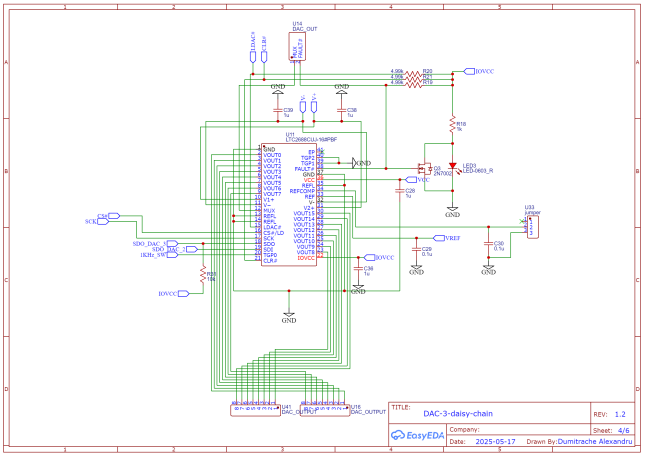

Figure 14: Circuit Schematic (Sheet 4) - DAC 3 in daisy-chain

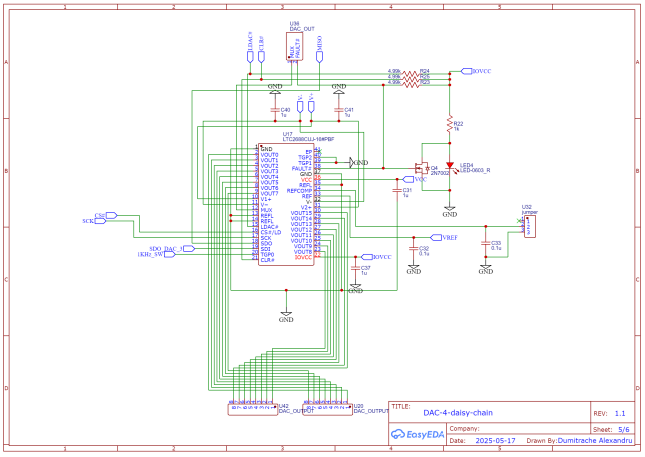

Figure 15: Circuit Schematic (Sheet 5) - DAC 4 in daisy-chain

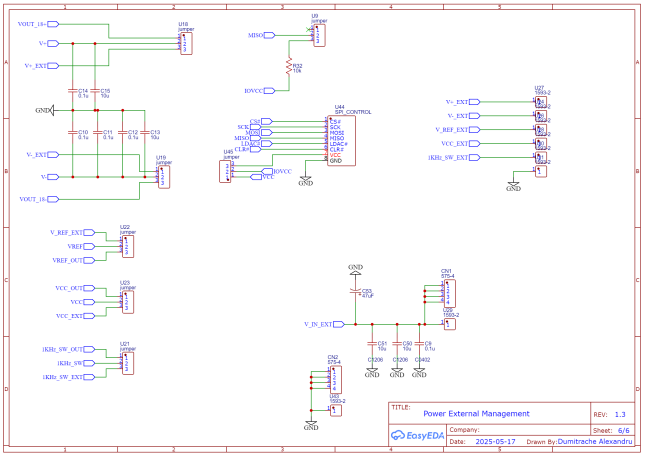

Figure 16: Circuit Schematic (Sheet 6) - Power external management

Table 2: LTC2688-based System Bill of Materials

ID	Designator	Part Description	Footprint
1	C1, C47	Ceramic Capacitor 22μF, 25V	1206 (3216 Metric)
2	C2, C48	Ceramic Capacitor 22nF, 25V	0603 (1608 Metric)
3	C3, C4	Ceramic Capacitor 0.01μF, 25V	0402 (1005 Metric)
4	C7	Ceramic Capacitor 0.01μF, 10V	0402 (1005 Metric)
5	C8	Ceramic Capacitor 10μF, 10V	0402 (1005 Metric)
6	C9	Ceramic Capacitor 0.1μF, 25V	0402 (1005 Metric)
7	C10, C11, C12, C14, C22,	Ceramic Capacitor 0.1μF, 25V	0603 (1608 Metric)
8	C23, C24, C25, C26, C29, C30, C32, C33, C46	Ceramic Capacitor 0.1μF, 10V	0402 (1005 Metric)
9	C19, C20, C21	Ceramic Capacitor 2.2μF, 25V	0805 (2012 Metric)
10	C38, C39, C40, C41, C42, C43, C44, C45	Ceramic Capacitor 1μF, 25V	0603 (1608 Metric)
11	C16, C27, C28, C31, C34, C35, C36, C37	Ceramic Capacitor 1μF, 10V	0603 (1608 Metric)
12	C5, C6, C13, C15, C50, C51	Ceramic Capacitor 10μF, 25V	1206 (3216 Metric)
13	C17, C18	Ceramic Capacitor 4.7μF, 25V	0603 (1608 Metric)
14	C49	Ceramic Capacitor 10μF, 10V	1206 (3216 Metric)
15	Q1, Q2, Q3, Q4	MOSFET 2N7002	SOT-23_L2.9-W1.3-P0.95-LS2.4-BR
16	LED1, LED2, LED3, LED4	Red, clear, light emitting diode (LED)	0603 (1608 Metric)
17	R1, R2	Resistor 1%, 1/10 W, 53.6k	0603 (1608 Metric)
18	R3	Resistor 1%, 1/10 W, 210k	0603 (1608 Metric)
19	R4	Resistor 1%, 1/10 W, 226k	0603 (1608 Metric)
20	R5, R8	Resistor 1%, 1/10 W, 64.9k	0603 (1608 Metric)
21	R6, R7	Resistor 1%, 1/10 W, 4.7k	0603 (1608 Metric)
22	R9, R17, R18, R22	Resistor 1%, 1/10 W, 1k	0603 (1608 Metric)
23	R10	Resistor 1%, 1/10 W, 2000k	0603 (1608 Metric)

continued on next page

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ID	Designator	Part Description	Footprint
24	R11, R12, R13, R14, R15, R16, R19, R20, R21, R23, R24, R25	Resistor 1%, 1/10 W, 4.99k	0603 (1608 Metric)
25	R27, R28	Resistor 1%, 1/10 W, 200k	0603 (1608 Metric)
26	R29, R30, R31, R32	Resistor 1%, 1/10 W, 10k	0603 (1608 Metric)
27	U1	LTM8049EY#PBF	BGA-77_L15.0-W9.0-R11-C7-P1.27-TL
28	U2	LT3032EDE#PBF	DFN-14_L4.0-W3.0-P0.50-BL_ADI_DE14MA
29	U3	LT1763IDE-5#PBF	DFN-12_L4.0-W3.0-P0.50-BL-EP
30	U4	LT6656BCDC-4.096#TRMPBF	TSOT-23-6_L2.9-W1.6-P0.95-LS2.8-BR
31	U5	LTC6900CS5#TRPBF	SOT-23-5_L3.0-W1.7-P0.95-LS2.8-BL
32	U6, U11, U13, U17	LTC2688CUJ-12#PBF	QFN-40_L6.0-W6.0-P0.50-TL-EP4.5-1
33	U8, U12, U14, U36	DAC debug pins, FAULT and MUX	2 pin connector
34	U7, U10, U16, U20, U39, U40, U41, U42	DAC output	8 pin connector
35	U15	LTM8049 power good debug	2 pin connector
36	U9, U18, U19, U21, U22, U23, U32, U33, U34, U35, U37, U45	Jumper selection	3 pin connector with jumper
38	U24, U26, U27, U28, U29, U30, U31, U43	Terminal Turret Connector Single End 3.96mm Tin	1593-2
39	U44	SPI header	8 pin connector
40	CN1, CN2	Banana Jack Connector Standard	575-4

A.2 BOM

The Bill of Materials (BOM) for the LTC2688 system is detailed in table 2, which lists all the necessary components required for the design and assembly of the circuit. The table includes the designator, part description, and the corresponding footprint for each component. The total estimated cost for acquiring all components shown is approximately **€250**, considering standard distributor pricing as of the time of documentation.

A.3 PCB and Footprints

This section presents the finalized Printed Circuit Board (PCB) design and the associated component footprints for the LTC2688 daisy-chain based voltage supply system. Figure 17 shows a detailed 3D render of the fully assembled PCB, highlighting the layout and positioning of key components such as ICs, connectors, resistors, capacitors, and status LEDs. This visual representation offers a clear view of the board's architecture and interconnections.

Figure 18 provides a comprehensive PCB footprint layout, which indicates the designated placement locations for all components used in the circuit. Each position is labeled with its unique reference designator (e.g., U13, R20, LED1), corresponding directly to entries in the previously defined Bill of Materials (BOM), in table 2. This ensures a streamlined and accurate assembly process, allowing the user to identify the exact position and orientation of each component on the board. The use of labeled footprints significantly enhances manufacturability and reduces the risk of placement errors.

Together, these figures serve as a practical guide for assembling and verifying the hardware implementation of the system.

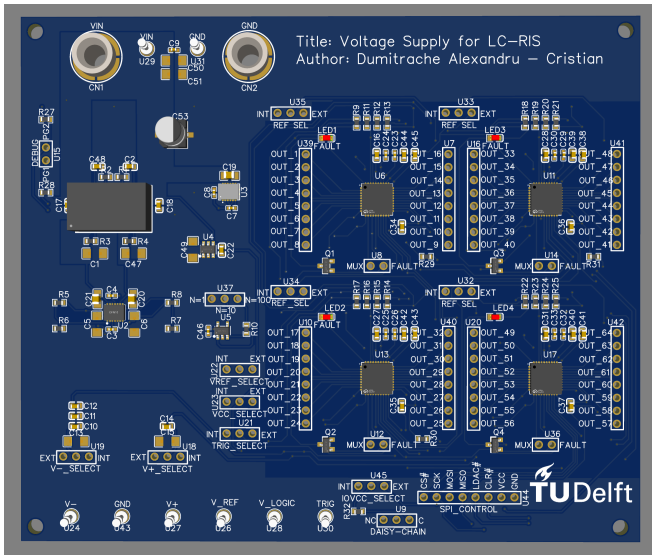

Figure 17: Render of the PCB design of the LTC2688 daisy-chain based system

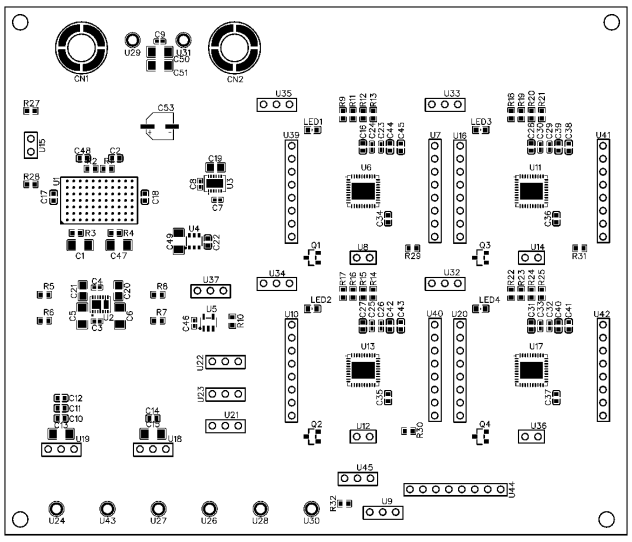

Figure 18: PCB footprint layout indicating the designated placement positions for components such as connectors, integrated circuits, resistors, capacitors, LEDs, and transistors on the board. Each component is labeled with its reference designator to guide accurate assembly.

A.4 Function Descriptions

This section provides a detailed overview of the functional components and configuration options of the LC-RIS system's control board (table 3).

The configuration of the power distribution, signal routing, and logic control is achieved through a structured set of onboard connectors, jumpers, voltage regulators, and communication interfaces. The board accepts a primary input voltage ranging from 3.7 V to 18 V via connector CN1, and distributes this power internally through a series of regulators and bypass options. External or internally generated power rails for analog and logic levels are selectable through multiple jumpers, offering flexibility during integration and testing.

The table presented in this section enumerates each key component and interface on the board, organized by designator and functional signal. Each entry includes a formal and precise explanation of its role in system operation. This includes external reference voltage selection (e.g., U26, U22), SPI communication and logic level interfacing (U44, U45), internal oscillator configuration for toggle mode (U30, U37), and the daisy-chain control and output signal routing for the DACs (U7, U10, U16, U20, U39, U40, U41, U42).

Diagnostic features such as power-good indicators (U15) and fault status LEDs (U8, U12, U14, U36) enable operational monitoring and facilitate debugging. The system also allows for flexible configuration of voltage references and logic domains per DAC channel, ensuring adaptability to a range of application scenarios.

Altogether, this structured description serves as a reference for developers and engineers to correctly power, interface, and configure the LC-RIS system for experimental or operational use.

Table 3: LTC2688-based System Function Descriptions

Designator	Part Name	Part Description
CN1, U29	VIN	Primary power input for the board. Accepts a voltage in the range of 3.7 V to 18 V to supply power to all board components.
CN2, U31, U43	GND	Common electrical ground reference for all power and signal circuits.
U24	V-	External negative analog supply rail for the LTC2688 DACs. To activate, set jumper U19 to the EXT position. Recommended input range: -17.5 V to -22 V.
U27	V+	External positive analog supply rail for the LTC2688 DACs. To activate, set jumper U18 to the EXT position. Recommended input range: +17.5 V to +22 V.
U26	V_REF (VREF)	External voltage reference input for the LTC2688 DACs. Activate by setting jumper U22 and jumpers U32–U35 to EXT. Acceptable input range is -0.3 V to VCC.
U28	V_LOGIC (VCC)	External Analog logic voltage supply for the LTC2688s. Connect via jumper U23 set to EXT. Operates within 4.75 V to 5.25 V.
U30	TRIG	External square wave signal input used to toggle between registers in the LTC2688 during toggle mode. The signal should swing between 0 V and IOVCC (determined by U44's SPI header).
U44	SPI Interface and IOVCC	Provides SPI control signals: CS, SCK, MOSI, MISO, LDAC, CLR, VCC, and GND. VCC defines the digital logic level for the LTC2688s. If U45 is set to EXT, VCC is supplied externally via SPI header. If unavailable, set U45 to INT to use internal voltage.
U15	LTM8049 PG Debug	Provides two Power-Good (PG) indicators for positive and negative rails, signaling proper operation of the LTM8049 module. Outputs reflect VIN level when operating correctly.
U8, U12, U14, U36	LTC2688 MUX and FAULT Pins	Each LTC2688 has dedicated FAULT and MUX pins. The FAULT pin is pulled up to IOVCC and indicates error status. When triggered, corresponding LEDs (LED1–LED4) are activated. MUX pin allows channel selection via SPI.
U7, U10, U16, U20, U39, U40, U41, U42	OUT0–OUT63	Analog voltage outputs from each DAC channel on the LTC2688 devices in daisy-chain configuration.
U9	Daisy-Chain Selector	Sets board daisy-chain functionality. Leave jumper at NC for standalone mode. Set to C when chaining multiple boards.

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Designator	Part Name	Part Description
U45	IOVCC Selector	Supplies digital logic voltage for the LTC2688s. Select EXT to use voltage from SPI header. Select INT to use internal VCC (analog logic supply). Voltage must be less than analog VCC and greater than 1.71 V.
U21	TRIG Selector	Routes toggle signal (TGP0) to LTC2688s. Select EXT to use external signal via U30. Select INT to use internal oscillator from LTC6900.
U22	VREF Selector	Configures voltage reference source for LTC2688 DACs. Set to EXT to use external reference from U26. Set to INT to use on-board LT6656 reference.
U23	VCC Selector	Configures analog logic supply source for the LTC2688s. Set to EXT for external 5 V source. Set to INT to use on-board LT1763 regulator.
U37	LTC6900 Frequency Selector	Determines frequency of the internal LTC6900 oscillator. Set to N=100 for 1 kHz, leave jumper open for 10 kHz, or set to N=1 for 100 kHz output.
U19	V- Selector	Selects source for negative analog rail of the LTC2688s. Set to EXT for external supply or INT to use LTM8049 rail via LT3032.
U18	V+ Selector	Selects source for positive analog rail of the LTC2688s. Set to EXT for external supply or INT to use LTM8049 rail via LT3032.
U32, U33, U34, U35	Reference Voltage Selector	Selects voltage reference (internal or external) for each LTC2688. Set to INT for internal DAC reference, or EXT to use shared V_REF input.