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Impact and mitigation of SRAM read path aging

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ABSTRACT

This paper proposes an appropriate method to estimate and mitigate the impact of aging on the read path of a high performance SRAM design; it analyzes the impact of the memory cell, and sense amplifier (SA), and their interaction. The method considers different workloads, technology nodes, and inspects both the bit-line swing (*BLS*) (which reflect the degradation of the cell) and the sensing delay (*SD*) (which reflects the degradation of the sense amplifier); the voltage swing on the bit lines has a direct impact on the proper functionality of the sense amplifier. The results with respect to the quantification of the aging, show for the considered SRAM read-path design that the cell degradation is marginal as compared to the sense amplifier, while the *SD* degradation strongly depends on the workload, supply voltage, temperature, and technology nodes (up to 41% degradation). The mitigation schemes, one targeting the cell and one the sense amplifier, confirm the same and show that sense amplifier mitigation (up to 15.2% improvement) is more effective for the SRAM read path than cell mitigation (up to 11.4% improvement).

1. Introduction

CMOS technology scaling is well known for causing crucial reliability challenges on electronics reliability [1-3]; e.g., it reduces their lifetime. A general practice in industry is the use of conventional guard-band and application of extra design margins to counteract for the Bias Temperature Instability (BTI) effect. Accurate estimation of such effect is vital for achieving an optimal design. Clearly, an electronic system comprises of various parts; hence, accurate BTI estimation requires to evaluate not only *all* the various parts of the system, but also the way they *communicate with each other*, and how they all provide to the complete degradation of the system. For example, when it comes to SRAMs, estimating the effect of BTI by only focusing on the memory array, or by only integrating the individual effects of each components, will lead to optimistic or pessimistic results.

Several publications have investigated the impact of reliability on individual SRAM components. Kumar et al. [4] and Carlson et al. [5] analyzed the impact of negative Bias Temperate Stability (NBTI) on the read stability and the Static Noise Margin (SNM) of SRAM cells. Bansal et al. [6] presented insights on the stability of an SRAM cell under the worst-case conditions and analyzed the effect of NBTI and PBTI (positive BTI). Khan et al. [7] performed BTI analysis for FinFET based memory cells for different SRAM designs using SNM, Read Noise Margin (RNM) and Write Triple Point (WTP) as metrics. Menchaca et al. [8] analyzed the BTI impact on different sense amplifier designs implemented on 32 nm technology node by using failure probability (i.e., flipping a wrong value) as a reliability metric. Agbo et al. [9-12] investigated the BTI impact on SRAM drain-input and standard latch-type sense amplifier design, while considering process, supply voltage, and temperature (PVT) variations in the presence of varying workloads and technology nodes. Rodopoulos et al. [13] proposed and investigated the pseudo-transient atomistic-based BTI model with built-in workloads while considering various supply voltages and temperatures. Other research focused on mitigation schemes. For example, Kraak et al. [14] and Pouyan et al. [15] investigated the mitigation of SA offset voltage degradation by considering periodic input switching. Gebregiorgis [16] investigated a low cost self-controlled bit-flipping scheme which reverses all bit positions with respect to an existing bit.

From the above, we conclude that not much work is published on aging, while taking into account all the memory components and thus their interactions, and the effect of mitigation methodologies on the whole memory. Li et al. [17] studied the lifetime estimation of each individual transistor for the *entire* SRAM and for various reliability mechanism (i.e., HCI, TDDB, NBTI). However, this investigation did not require the workload, which has been demonstrated to have a large effect on the degradation rates [13, 18, 19]. In our previous work [20],

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we analyzed the impact of aging in the read path of a 32 nm high performance SRAM design for different workloads. However, the impact of aging on different supply voltages, temperatures, technology nodes, and varying device drive strengths based on *BLS*, *SD*, and energy (E) metrics on the memory read path are yet to be explored. In addition, effective mitigation schemes are not proposed. The above clearly shows that an appropriate approach (that accurately predicts the impact of aging, workloads, and PVT) is needed. Hence, this analysis is crucial to help memory designers understand which of the memory parts to focus on during design for an optimal and reliable design.

In this paper, we set up a step towards this, and we propose an *accurate* method to estimate the impact of Bias Temperature Instability (BTI) on the read path consisting of an SRAM cell and sense amplifier (SA). This enables not only optimal designs (in terms of design margins), but also the development of appropriate design-for-reliability schemes. The proposed method uses the *Atomistic Model* for aging (which is a calibrated BTI model [21, 22]) and considers the *workload dependency* (as the aging variations are strongly workload dependent [18, 19]). To measure both the impact of the cell and SA appropriate workloads are defined while using the bit-line voltage swing, SA *SD*, and energy as metrics. In addition, we analyze different mitigation schemes and their effectiveness.

The rest of the paper is organized as follows. Section 2 provides the SRAM simulation model, and explains BTI mechanism and its model. Section 3 provides the analysis framework and performed experiments. Section 4 analyzes impact of aging on the read path. Section 5 proposes and evaluates the mitigation schemes. Finally, Section 6 and Section 7 discusses the results and concludes this paper, respectively.

2. Background

This section briefly presents the simulation model; it consists of the critical SRAM components in the read path. Finally, it discusses the BTI mechanism and its model.

2.1. Simulation model

Fig. 1 shows the simulation model, which is divided into four parts (i.e., precharge circuitry, 6T cell, SA precharge and the SA). The W/L ratio of each transistor considered for aging is included in the figure. Capacitances are also added to the bit-lines to model the impact of other cells sharing the same column as the simulated cell. Here we assume a 512 × 128 memory array. During a read operation, first the bit lines are precharged (using precharge circuit), and thereafter one of the bit lines is discharged through one of the cell's pull down transistors of the SRAM 6T cell. The voltage difference/swing is then amplified by the SA to produce the output.

The SA precharge is used to precharge and equalize the data-lines *DL* and *DLBar* to identical voltages before the SA amplifies a small voltage difference between *BL* and *BLBar* during read operations, and produces the output at *Out* (*DL*) and *Outbar* (*DLBar*). The positive feedback loop (created by cross-coupled inverters) ensures low amplification time and produces the read value at its output. Because the considered design is high performance, the cell has *strong pull-down* transistors to speed-up the formation of the swing between the bit-lines during read operation.

It is worth noting that only aging in the cell and the sense amplifier are considered; the cell precharge circuit and the SA precharge circuit are ignored due to their relative large transistor sizes (i.e., less affected by BTI).

2.2. Bias Temperature Instability

The Bias Temperature Instability (BTI) mechanism takes place inside MOS transistors and increases the absolute threshold voltage (V_{th}) value of the transistors [23, 24]. The V_{th} increment in a PMOS transistor

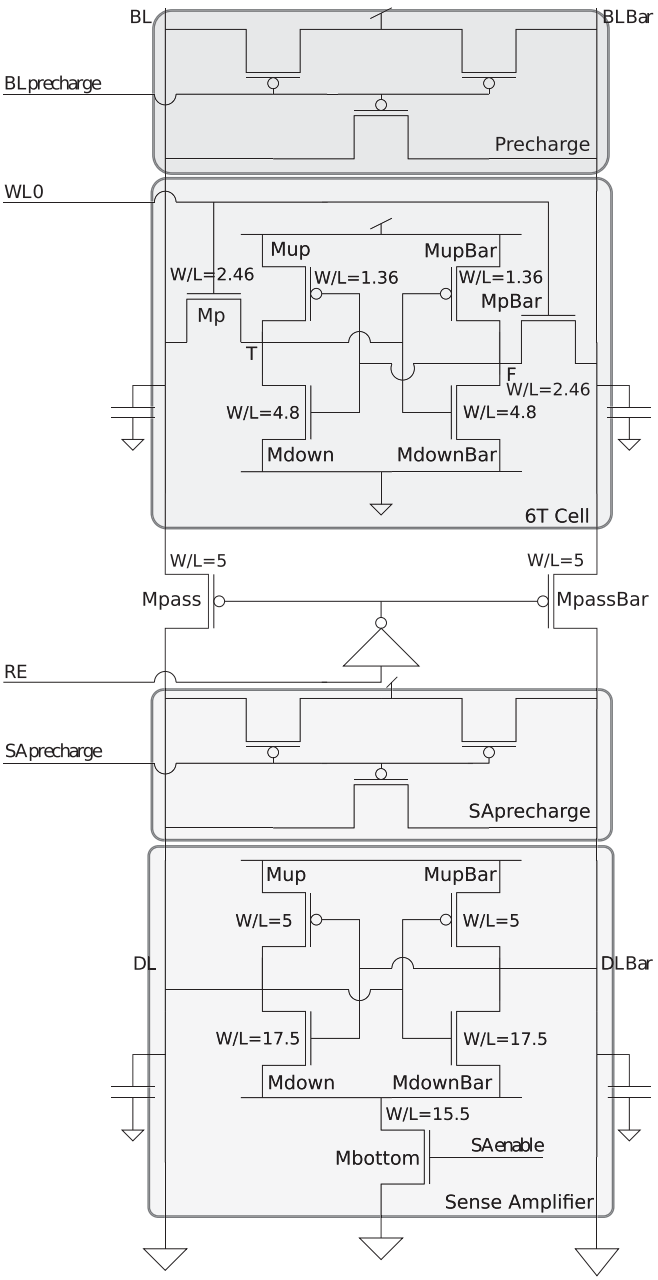

Fig. 1. Simulation setup.

occurs under *negative* gate *stress* and is referred to as NBTI, while in an NMOS transistor this occurs under *positive* gate *stress*, and is known as PBTI. Note that for a MOS transistor, there are two BTI phases, i.e., the stress phase and the relaxation phase.

Exhaustive efforts have been put to understand and model BTI appropriately [23-25]. The two most known models are the reaction-diffusion (RD) model proposed by Alam et al. [23], and the atomistic model proposed by Kaczer et al. [21]; the first is deterministic and the second is probabilistic. In this work, we use the atomistic model as it provides more accurate results than the RD model [26]. The atomistic model is based on the capture and emission of single traps during stress and relaxation phases of NBTI/PBTI respectively. The threshold voltage shift ΔV_{th} of the device is the accumulated results of all the capture and emission of carriers in gate oxide defect traps. The probabilities of the defect occupancy in case of capture P_C and emission P_E are defined by [26]:

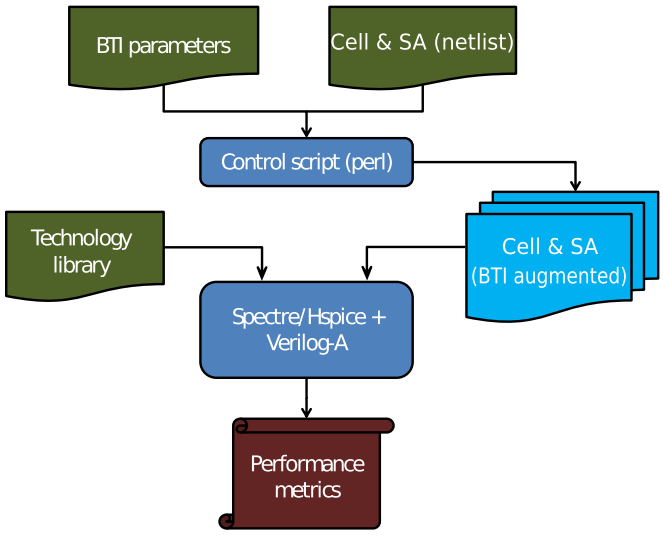

Fig. 2. Analysis framework.

$$P_C(t_{STRESS}) = \frac{\tau_e}{\tau_c + \tau_e}\left\{1 - \exp\left[-\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)t_{STRESS}\right]\right\} \quad (1)$$

$$P_E(t_{RELAX}) = \frac{\tau_c}{\tau_c + \tau_e}\left\{1 - \exp\left[-\left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)t_{RELAX}\right]\right\} \quad (2)$$

where τ_c and τ_e are the mean capture and emission time constants, and t_{STRESS} and t_{RELAX} are the stress and relaxation periods, respectively. Furthermore, BTI induced V_{th} is an integral function of Capture Emission Time (CET) map [7], workloads, duty factor and transistor dimensions, which gives the mean number of available traps in each device, the model also includes the impact of temperature in [21, 22].

3. Analysis framework

This section presents the analysis framework and the conducted experiments.

3.1. Framework flow

Fig. 2 depicts our generic simulation framework to evaluate the BTI impact on the cell and SA designs. It uses Spectre simulator and has the following components.

Input: The general input blocks of the framework are the technology library, cell and sense amplifier design, and BTI input parameters.

- Technology library: In this work we use three technology nodes, they are 45-nm, 32-nm, and 22 nm and are obtained from PTM library card [27]. Note that in general any library card can be used.
- Cell and SA designs: Generally, any memory cell and sense amplifier design can be used. In this paper, we focus only on the design in Fig. 1. The 6T cell and SA designs are described by a SPICE netlist.
- BTI parameters: The BTI induced degradation strongly depends on the stress time duration, hence on the workload. The workload sequence is assumed to be replicated until the age time is reached. To define the workloads for our analysis, we assume two extreme workloads for the cell's state: (i) 80% zero's, that is, 80% of the time the cell holds a zero, and (ii) 20% zero's. Similarly, we assume two workloads for the SA: (i) 80% of the instructions are reads, and (ii) 20% of the instructions are reads. Based on this information, we derive four workload sequences for circuit simulation:
  S1: denotes 20% zero's and 80% read instructions for the SA.
  S2: i.e., 20% zero's and 20% read instructions for SA.
  S3: i.e., 80% zero's and 80% read instructions for SA.
  S4: i.e., 80% zero's and 20% read instructions for the SA.
  Using the waveform of the read operation and the workload sequences, we extract duty factors for each transistors individually.
  It is worth noting that in our investigation time-zero variations (i.e., process variations) are also taken into consideration.

Processing: Based on the inputs (i.e., technology, design, BTI parameters and etc.), a perl control script generates several instances of BTI augmented SRAM cell and/or sense amplifier, depending on the simulation case (see Section 3.2). Every generated instance has a distinct number of traps [21] (with their unique timing constants) in each transistor, and are incorporated in a Verilog-A module of cell netlist only, SA netlist only, or both cell and SA netlists. The module responds to every trap individually, and alters the transistors concerned parameters such as V_{th}. After inserting BTI in every transistor of either coupled design or individual designs, a Monte Carlo (MC) simulation is performed at different time steps (100 runs at each time step) where circuit simulator (Spectre) is used to investigate the BTI impact.

Output: Finally, statistical post-analysis of the results are performed for varying supply voltages, temperatures and device drive strengths in MATLAB environment. The raw outputs are measured directly from Spectre and used to determine the *BLS* and *SD* metrics, which are

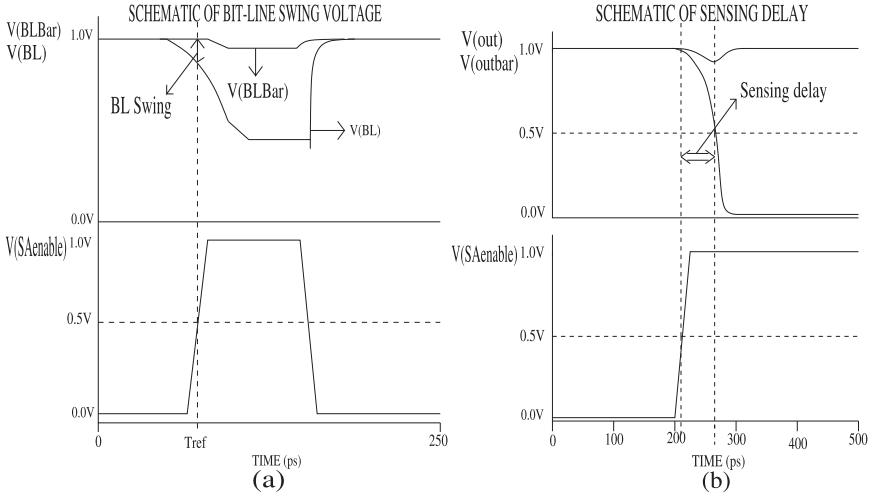

Fig. 3. Metric diagram of (a) *BLS* and (b) *SD*.

described next.

Bit-line swing: The *BLS* specifies the voltage difference between bit-lines *BLBar* and *BL* (see Fig. 3a) at a fixed reference time T_{ref}, i.e., the time where the up transition of the sense amplifier enable signal reaches 50% of the supply voltage as shown in Fig. 3a.

Sensing delay: The *SD* is the time required for the SA to complete its operation; it is the time between the sense enable activation (i.e., when the up transition reaches 50% of the supply voltage) and the falling *out* or *outbar* signal (i.e., when the down transition reaches 50% of V_{dd}) as depicted in Fig. 3b.

3.2. Experiments performed

In this paper, four sets of experiments are performed that are related to the quantification of aging, where each set consists of three cases: (a) only the cell degrades (Cell-Only), (b) only the SA degrades (SA-Only), and (c) both of them degrade (Combined).

1. **BTI impact experiments:** BTI impact on *BLS* and *SD* for four workload sequences (*S1*, *S2*, *S3* and *S4*) for 32-nm technology node at nominal supply voltage ($V_{dd} = 0.9V$) and nominal temperature ($T = 298K$) are investigated.
2. **Supply voltage dependent experiments:** BTI impact on the *BLS* and *SD* for varying supply voltages (i.e., from $-10\%V_{dd}$ to $+10\%$ of V_{dd}) and two workload sequences *S2* and *S3* for 32-nm technology node at nominal temperature are investigated. Note that these two sequences present the best and the worst case stresses.
3. **Temperature dependent experiments:** BTI impact on *BLS* and *SD* for three temperatures (i.e., 233*K*, 298*K* and 348*K*) and two workload sequences *S2* and *S3* for 32-nm technology node at nominal supply voltage are explored.
4. **Technology dependent experiments:** BTI impact on *BLS* and *SD* for three technology nodes (i.e., 45-, 32- and 22-nm) and two workload sequences *S2* and *S3* at nominal supply voltages (i.e., V_{dd} = 1.0 V for 45-nm, 0.9 V for 32-nm, and 0.8 V for 22-nm) and temperature are explored.

4. Experimental results

This section, presents the analysis results of the experiments mentioned in the previous section.

4.1. BTI impact experiments

Table 1 shows the results for the three cases for both time-zero (no aging) and a stress period of 10^8s. Note that the workload is irrelevant for time-zero. The first column presents the simulated case. 'Cell-Only' denotes the case when only the cell is impacted by BTI, 'SA-Only' when only the SA is impacted, and 'Combined' when both the cell and SA degrade due to BTI. Note that in case of 'Cell-Only', both the mean, μ and standard deviation, 3σ of *BLS* and the *SD* are affected, while in the case of *SA-Only*, both the μ and 3σ of the *SD* are impacted (i.e., the μ and 3σ of *SD* may increase due to slow *BLS* development or slow SA) while the *BLS* should not be affected. The table reveals the following for the different cases. For the case 'Cell-Only', the μ BLS is marginally dependent on the workload, resulting in almost no impact on the μ SD while the BLS 3σ increment also impact on the SD's 3σ. This can be explained by the fact that the pull-down transistors of the cell used for this design are very strong (see Fig. 1). We will assume the baseline of SD for μ and 3σ to be equal to 60.80 *ps* and 0.69 *ps*, respectively.

Table 1
BTI impact.

Degradation component	Aging (s)	Workload	Bit-line swing μ (mV)	Bit-line swing 3σ (mV)	Sensing delay μ (ps)	Sensing delay 3σ (ps)
Cell-Only	0	–	108.9	4.2	60.80	0.69
	10^8	20% zero	107.0	6.9	61.09	1.11
	10^8	80% zero	106.3	7.3	61.20	1.18
SA-Only	0	–	110.8	0.7	61.05	1.47
	10^8	20% read instr.	111.1	0.9	61.83	2.88
	10^8	80% read instr.	111.6	1.3	65.71	4.36
Combined	0	–	109.0	4.2	61.24	1.44
	10^8	S1	107.8	6.9	66.08	4.24
	10^8	S2	107.4	6.9	62.18	3.12
	10^8	S3	107.1	7.3	66.21	4.25
	10^8	S4	106.7	7.4	62.29	3.12

For the case 'SA-Only', the cell is not suffering from BTI; hence, it is not affected and is about 111 mV and 0.9 ps for the μ and 3σ of the BLS, respectively. The SD, however, is affected and increases for more stressy workloads. The μ SD at 80% read instructions is ~6% higher than at 20% reads for which the SD is just 1.7% more than the baseline.

For the case 'Combined', although the μ of BLS is reduced as compared with the a-fresh cell (see SA-Only case), the dependency of BLS on the workload is marginal due to the chosen design as already mentioned. However, as can be predicted, the results show clear dependency of the μ of SD on the workload; the SD μ is higher for sequences *S1* and *S3* which both have 80% read instructions for the SA. At 80% read instructions (*S1* and *S3*), the μ SD is also ~6% higher than at 20% read instructions (*S2* and *S4*); in the latter case the μ SD is about ~2.5% more than the baseline. Note that the *relative* increase due to workload is the same as for 'SA-Only' case.

Fig. 4 shows how BLS and SD evolve over time for a duration of 3 years degradation (i.e., 10^8s) for the case 'Combined'; each point in the graph corresponds to the average of 100 Monte Carlo simulations. The figure clearly confirms the conclusions extracted from Table 1, and that (although in terms of absolute number of our case study, the difference are not so big), *the slowest SD* is obtained when *both* the degradation of the cell and the SA are considered. Note that the SD tends to grow very fast when the operational lifetime gets closer to 3 years (10^8s).

4.2. Supply voltage dependency

Table 2 shows the result of Supply Voltage Dependent Experiments for both time-zero (i.e., no aging) and a stress period of 10^8s. The table reveals the following.

For the case 'Cell-Only', similar to the first experiment, the μ and 3σ of the BLS seems to be marginally dependent on the workload. However, a change in the supply voltage clearly influences both the μ of

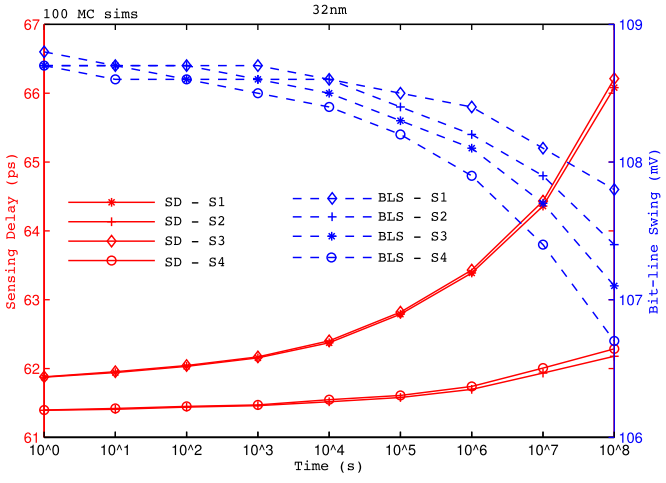

Fig. 4. BTI impact for the four workload sequences.

Table 2
Voltage degradation dependency.

Degradation component	Workload	Aging (s)	Vdd(*V*)	Bit-line swing μ (mV)	Bit-line swing 3σ (mV)	Sensing delay μ (ps)	Sensing delay 3σ (ps)
Cell-Only	20% zero	0	−10%	77.9	2.7	74.35	0.81
		10^8	−10%	76.7	4.0	74.64	1.02
		0	Nom.	108.9	4.2	60.80	0.69
		10^8	Nom.	107.0	6.9	61.09	1.11
		0	+10%	140.0	6.3	52.12	0.81
		10^8	+10%	136.8	7.9	52.53	1.01
	80% zero	10^8	−10%	76.2	4.5	74.74	1.16
		10^8	Nom.	106.3	7.3	61.20	1.18
		10^8	+10%	135.5	8.0	52.67	1.03
SA-Only	20% read instr.	0	−10%	78.9	0.4	74.74	2.16
		10^8	−10%	79.0	0.6	75.82	3.66
		0	Nom.	110.8	0.7	61.05	1.47
		10^8	Nom.	111.1	0.9	61.83	2.88
		0	+10%	143.4	1.14	52.40	1.50
		10^8	+10%	143.7	1.5	53.18	2.50
	80% read instr.	10^8	−10%	79.3	0.9	80.41	6.28
		10^8	Nom.	111.6	1.3	65.71	4.36
		10^8	+10%	144.4	1.8	58.00	4.84
Combined	S2	0	−10%	78.0	2.79	74.90	2.07
		10^8	−10%	76.9	4.2	75.89	3.70
		0	Nom.	109.0	4.2	61.24	1.44
		10^8	Nom.	107.4	6.9	62.18	3.12
		0	+10%	140.2	6.3	52.79	1.47
		10^8	+10%	137.5	7.6	53.92	2.37
	S3	10^8	−10%	76.7	4.7	80.94	5.52
		10^8	Nom.	107.1	7.3	66.21	4.25
		10^8	+10%	136.8	8.3	58.92	4.63

the BLS and the SD and marginally, the 3σ of BLS and SD. Moreover, the impact can be higher when time-zero is considered. Increasing the supply voltage accelerates the development of the swing on the bit lines; hence increasing both the μ and 3σ of the BLS. This in turn reduces both the μ and 3σ of the *SD*. On the other hand, reducing the supply voltages reduces the μ BLS, which in turn increases the *SD* μ. A variation of +10% in supply voltage causes an increase of about 26% in the μ BLS and a reduction of about 14% in SD μ, while a variation of −10 % in supply voltage causes a decrease of almost the same percentage in the BLS μ (27%) and an increase of more than 22% in SD μ.

For the case 'SA-Only', although the cell is not suffering from BTI, the supply voltage clearly impacts both the μ and 3σ of the BLS. It follows the same trend as for Cell-Only case. On the other hand, the μ SD is both supply voltage and workload dependent while SD 3σ does not maintain the same trend particularly for stressy supply voltage and workload. A higher voltage improves (reduces) the μ SD, while a lower voltage worsens (increases) the μ SD while the same trend is not followed for the SD 3σ. A +10% variation in V_{dd} causes a reduction of about 13% in μ SD, and −10 % variation in V_{dd} causes an increase of about 22.4% in μ SD. In addition, although the development of voltage swing is accelerated at higher supply voltage, the impact of the workload dependency seems to be slightly higher at higher supply voltage. For example, at −10 % V_{dd} and 10^8s the mean SD increases from 75.82 ps (for 20% read instructions) to 80.41 ps (for 80% read instructions); an increase of 6% while the 3σ SD increases with 71.6%. However, this is about 9% at +10% V_{dd} for the μ SD. Moreover, this is slightly higher by 1.7% at +10% V_{dd} and at time-zero. Note that the impact of supply voltage variation is much dominant than the impact of BTI; this is due to the sizing of the cell's pull-down transistors (see Section Discussion).

For the 'Combined' case, the results show similar trends as for 'SA-Only' case. Even in terms of absolute numbers, the impact of V_{dd} variations and workloads on μ SD are very close (max 1.5% increase) to the results found for 'SA-Only'. Although the slowest SD is obtained in this case, the additional contribution of interaction between degrading cell and degradation SA to the SD as compared with 'SA-Only' is very marginal and does not exceed 1.5%.

Fig. 5 shows how BLS and SD supply voltage dependency evolve over time for a duration of 3 years degradation for the case ' Combined' using *S3* (worst case stress). The figure shows the impact on the BLS becomes visible when the operational life becomes close to 3 years, which clearly start then impacting the μ SD.

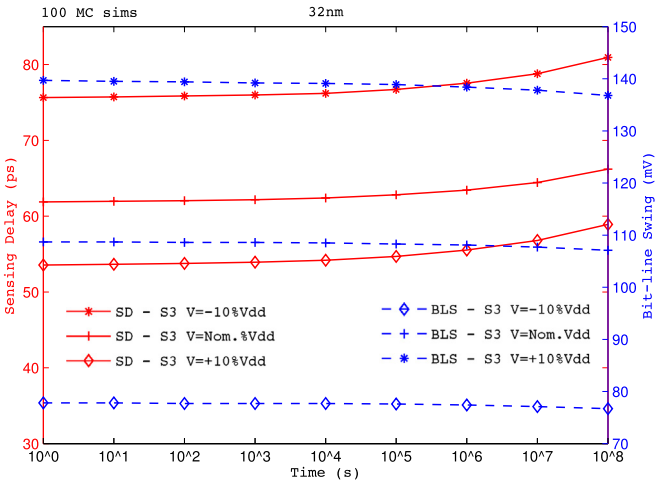

Fig. 5. Supply voltage dependency of SD and BLS for S3 sequence.

4.3. Temperature dependency

Table 3 shows the results of the Temperature Experiments for both time-zero and a stress period of 10^8s. The table reveals the following.

For the case 'Cell-Only', similar to the first two experiments, at 10^8s the μ and 3σ of BLS seem to be marginally dependent on the workload. However, the temperature strongly influences both the μ and 3σ of BLS and SD. The higher the temperature, the lower the BLS and the higher the SD. Increasing the temperature from 298 K to 348 K reduces the μ and 3σ of BLS with about 33% and 13%, respectively. The increase in temperature also increases the μ and 3σ of *SD* with about 41% and 25%, respectively. Moreover, the reduction in μ and 3σ for BLS will be

Table 3
Temperature degradation dependency.

Degradation component	Workload	Aging (s)	Temp. *(K)*	Bit-line swing μ (mV)	Bit-line swing 3σ (mV)	Sensing delay μ (ps)	Sensing delay 3σ (ps)
Cell-Only	20% zero	0	233	176.2	4.8	38.14	0.60
		10^8	233	175.4	6.1	38.23	0.78
		0	298	108.9	4.2	60.80	0.69
		10^8	298	107.0	6.9	61.09	1.11
		0	348	76.2	3.3	85.42	0.69
		10^8	348	72.2	6.1	86.27	1.39
	80% zero	10^8	233	175.2	6.7	38.25	0.85
		10^8	298	106.3	7.3	61.20	1.18
		10^8	348	70.7	6.6	86.62	1.51
SA-Only	20% read instr.	0	233	177.9	1.2	38.19	0.63
		10^8	233	177.9	0.9	38.36	0.79
		0	298	110.8	0.7	61.05	1.47
		10^8	298	111.1	0.9	61.83	2.88
		0	348	77.8	0.5	86.17	3.33
		10^8	348	78.6	1.3	90.10	9.02
	80% read instr.	10^8	233	178.0	1.1	38.63	0.94
		10^8	298	111.6	1.3	65.71	4.36
		10^8	348	79.6	1.9	143.94	113.50
Combined	S2	0	233	176.3	4.8	38.37	0.93
		10^8	233	175.5	6.3	38.59	1.24
		0	298	109.0	4.2	61.24	1.44
		10^8	298	107.4	6.9	62.18	3.12
		0	348	76.4	3.3	86.21	3.00
		10^8	348	73.1	6.5	90.46	8.84
	S3	10^8	233	175.3	6.9	38.87	1.39
		10^8	298	107.1	7.3	66.21	4.25
		10^8	348	72.6	6.8	151.77	117.05

slightly higher at time-zero while there is a significant increase in *SD* (up to 126% for both μ and 3σ).

For the case 'SA-Only', the temperature clearly impacts both μ and 3σ of the BLS although the cell is not suffering from BTI; hence, the temperature impacts both μ and 3σ of the BLS irrespective of BTI. This impact strengthens the degradation of both μ and 3σ of the *SD* due to the BTI. The *SD* is strongly temperature dependent and the situation becomes worst for stressy workloads. At 20% read instructions, the μ SD increases from 61.83*ps* at 298 K to 90.10*ps* at 348 K; an increase of 45% while the increase for the SD 3σ is too significant (up to 213%!). However, the *SD* μ is 119% and the 3σ is much higher for 80% read instructions! Moreover, at time-zero the impact can be slightly higher for the *SD* μ and much higher for the SD 3σ.

For the 'Combined' case, the results show similar trends as to 'SA-Only' case. Even in terms of absolute numbers, the impact of temperature variations and workloads on both μ and 3σ of the *SD* are close to the results found for 'SA-Only'. Although the slowest μ and 3σ of the SD are obtained in this case, the additional contribution of interaction between degrading cell and degrading SA to the μ *SD* as compared with 'SA-Only' is marginal except for the *S3* at 348 K where this is 5.4%. In addition, the impact can be higher while taking time-zero into account.

Fig. 6 shows how BLS and SD evolve over time for a duration of 3 years degradation for workload *S3* in Combined case. The figure clearly confirms the conclusions extracted from Table 3, and that the degradation of the read paths starts to grow exponentially at high temperatures after a stress time of 10^5s.

4.4. Technology dependency

Table 4 shows the results of Technology Dependent Experiment for both time-zero and a stress period of 10^8s. The table also shows BL-swing in columns 5 and 6. The table reveals the following.

For the case 'Cell-Only', similar to the first experiment, the μ and 3σ of the BLS seem to be marginally dependent on the workload, irrespective of the technology nodes considered. However, as the technology node scales down, the development of swing reduces, irrespective of the workload considered. For example, after an operation of 10^8s and 80% zero, the μ of BL-swing is 1.71% reduction for 45-nm, while

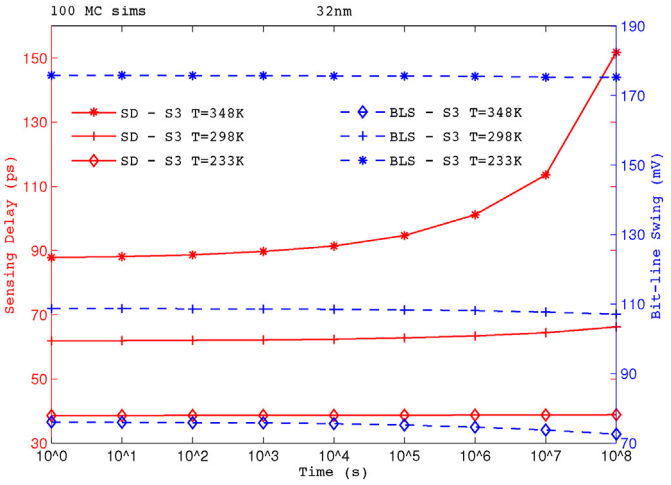

Fig. 6. Temperature degradation dependency of SD and BLS for S3 sequence.

2.45% for 32-nm, and 3.64% for 22-nm technology node.

In addition, the 3σ of the BL-swing increases significantly, irrespective of the workloads and technology nodes considered. For example, at 10^8s and 80% zero, 3σ of BL-swing is 30% for 45-nm while 73.81% for 32-nm, and 85.25% for 22-nm. Moreover, the μ of the sensing delay marginally increases in absolute value, while the 3σ of sensing delay relative increment is significant, irrespective of the workloads and technology nodes considered.

For the case 'SA-Only', despite the fact that the cell is not suffering from BTI, the μ and 3σ of BLS increases as well, irrespective of the technology node. On the other hand, as technology node reduces, the μ and 3σ of the sensing delay significantly increases as well. For example, after an operation of 10^8s and for 20% zero, the μ and 3σ of SD is 0.88% and 69.23% for 45-nm, while 1.28% and 95.92%, and 1.94% and 84.42%, for 32-, and 22-nm, respectively. In addition, for 80% zero, the μ and 3σ of SD are 6.74× and 2.73× for 45-nm, while 5.56× and 2.05×, and 5.75× and 2.65×, for 32-, and 22-nm, respectively.

For the case 'Combined', despite the fact that μ of BLS reduces while

Table 4
Technology degradation dependency.

Tech. nodes	Degradation component	Workload	Aging (s)	BL-swing μ (mV)	BL-swing 3σ (mV)	Sensing delay μ (ps)	Sensing delay 3σ (ps)
45-nm	Cell-Only	–	0	134.9	3.0	66.64	0.62
		20% zero	10^8	133.2	3.8	66.96	0.79
		80% zero	10^8	132.6	3.9	67.06	0.78
	SA-Only	–	0	136.8	1.1	66.80	1.04
		20% read	10^8	137.1	1.3	67.39	1.76
		80% read	10^8	137.6	1.5	70.76	2.75
	Combined	–	0	135.2	3.0	67.13	1.33
		S2	10^8	133.8	3.7	67.95	1.89
		S3	10^8	133.7	4.1	71.44	2.80
32-nm	Cell-Only	–	0	108.9	4.2	60.80	0.69
		20% zero	10^8	107.0	6.9	61.09	1.11
		80% zero	10^8	106.3	7.3	61.20	1.18
	SA-Only	–	0	110.8	0.7	61.05	1.47
		20% read	10^8	111.1	0.9	61.83	2.88
		80% read	10^8	111.6	1.3	65.71	4.36
	Combined	–	0	109.0	4.2	61.24	1.44
		S2	10^8	107.4	6.9	62.18	3.12
		S3	10^8	107.1	7.3	66.21	4.25
22-nm	Cell-Only	–	0	102.5	6.1	57.66	0.98
		20% zero	10^8	99.8	10.3	58.08	1.66
		80% zero	10^8	98.9	11.3	58.22	1.85
	SA-Only	–	0	104.6	1.2	58.20	2.76
		20% read	10^8	104.9	1.9	59.33	5.09
		80% read	10^8	105.4	2.8	64.69	8.93
	Combined	–	0	102.7	6.2	58.47	2.70
		S2	10^8	100.5	10.2	59.81	5.08
		S3	10^8	100.1	11.4	65.66	9.08

the 3σ of BLS slightly increases as compared with aged cell (see Cell-Only), the BLS dependency on workload is marginal, irrespective of the considered technology nodes. Nevertheless, the results show a marginal μ dependency of SD on *S2* workload, while a significant μ dependency of SD on *S3* workload, irrespective of the technology nodes considered.

In addition, the results show a significant 3σ dependency of SD on workloads, irrespective of the technology nodes considered. Note that there is marginal relative μ SD increase as compared to 'SA-Only' case while considering various technology nodes. However, the 3σ SD follows the same trend as compared to 'SA-Only' case while considering various technology nodes.

Figs. 7 and 8 depict the relative BTI impact on the SD and the BLS for different technology nodes while considering both worst-case (*S3*) and best-case (*S2*) workloads at nominal supply voltage and temperature. The figures reveal the following:

- The relative sensing delay degradation is more sensitive to technology scaling than BLS. This is also the case for the absolute numbers as the Table 4 shows.
- The impact of workload is more severe on the SD (up to 5×), than the BLS (not more than 1.1×).

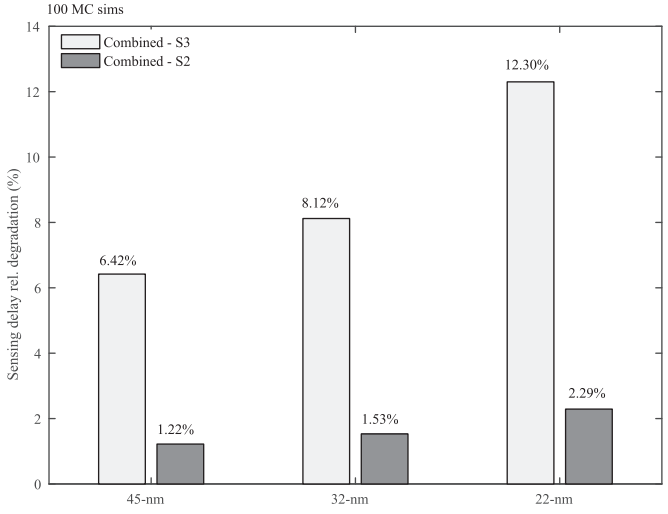

Fig. 7. Technology nodes dependency of SD for both S3 & S2 sequences.

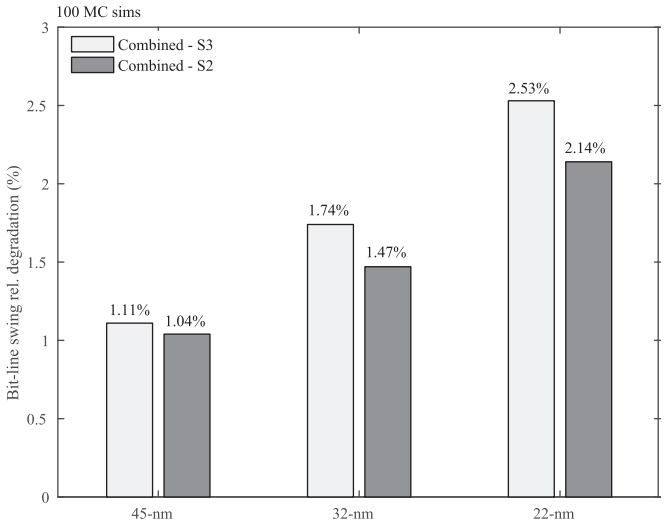

Fig. 8. Technology nodes dependency of BLS for both S3 & S2 sequences.

5. Mitigation schemes

In the previous section, we observed that *BLS* and *SD* may heavily be impacted by BTI. In this section, we investigate two mitigation techniques, i.e., increasing the cell's and the SA's drive strengths. This drive strengths only applies to the pull down transistors for both cell and SA (i.e., *Nom.DS* denoting normal sized transistors, 125%DS denoting 125% larger transistors, and 150%DS denoting 150% larger transistors). Note that the pull up transistors are not affected that much due to bit line and SA pre-charge circuits. We analyze the impact of these drive strengths for workloads *S2* and *S3* which have been defined in Section 3

Table 5
Cell and SA strength degradation.

Component	Workload	Aging (s)	Device-strength *(DS)*	Bit-line swing μ (mV)	Bit-line swing 3σ (mV)	Sensing delay μ (ps)	Sensing delay 3σ (ps)	Energy μ (fJ)	Energy 3σ (fJ)
Cell-Only	*S2*	0	Nom.	108.9	4.2	61.25	1.59	23.57	0.48
		10^8	Nom.	107.3	6.9	62.22	3.15	23.51	0.81
		0	125%	118.0	4.8	60.06	1.5	23.68	0.42
		10^8	125%	116.7	6.0	61.02	2.37	23.64	0.63
		0	150%	124.8	5.1	58.95	1.65	23.69	0.48
		10^8	150%	123.5	6.9	59.88	2.82	23.65	0.75
	S3	0	Nom.	108.9	4.2	61.27	1.62	23.58	0.48
		10^8	Nom.	107.0	7.2	66.27	4.26	24.36	0.93
		10^8	125%	116.5	6.9	64.68	4.11	24.40	0.93
		10^8	150%	123.2	7.8	63.52	4.32	24.42	1.02
SA-Only	*S2*	0	125%	108.8	4.2	56.86	1.38	22.84	0.42
		10^8	125%	107.2	6.9	57.86	2.40	22.80	0.69
		0	150%	108.7	4.2	54.06	1.29	22.32	0.39
		10^8	150%	107.1	6.9	54.97	2.07	22.28	0.54
	S3	10^8	125%	106.9	7.2	61.82	4.14	23.68	1.02
		10^8	150%	106.8	7.2	58.73	3.54	23.15	0.90
Combined	*S2*	0	125%	117.9	4.8	55.88	1.47	22.98	0.42
		10^8	125%	116.6	6.0	56.74	2.31	22.94	0.69
		0	150%	124.5	5.1	52.11	1.26	22.46	0.39
		10^8	150%	123.2	6.9	52.83	2.04	22.39	0.60
	S3	10^8	125%	116.4	6.9	60.16	3.78	23.68	0.90
		10^8	150%	123.0	7.8	56.23	3.06	23.17	0.78

at nominal supply voltage and temperature conditions. Note that the cell strength influences the BLS and thus indirectly the *SD*. It is worth noting that increasing the device size could lead to an increase in the bit-line length and therefore, also an increase in the delay. Hence, the impact of sizing on the overall latency of the array should be also explored.

Table 5 shows the individual impact of the drive strength of the Cell, the SA and their combined impact for both time-zero and a stress period of 10^8s. In the table, 'Cell-Only' *denotes* the case where only the cell's pull-down transistors drive strength are sized up (i.e., *Nom.*DS, 125%DS and 150%DS). Similarly, 'SA-Only' presents the case where only the drive strength of the pull-down transistors of the SA are sized up. In the 'Combined' case, the pull down transistors of both the cell and SA are simultaneously re-sized. The second column specifies the applied workload, both the cell and SA are stressed using either workload *S2* or *S3*. This workload is applied whether or not a component is re-sized or not. The third column presents the aging (lifetime) while the fourth column specifies the device strength (DS) of the pull down transistors, and the last 6 columns show the results; the evaluated metrics are *BLS*, *SD*, and Energy (E), respectively. The BLS and SD are defined in Section 3, while the energy is defined as the dynamic energy consumption for a single read operation. Next, the three cases will be described.

Cell-Only: For the case 'Cell-Only', the μ BLS significantly increases when the transistors are re-sized while the 3σ remains the same. For example, from 107 mV to 123 mV when a 150% bigger size is used. This 15% μ BLS increment is more or less workload independent. However, the μ BLS increment leads to a much smaller *SD* (both μ and 3σ) improvement. For example, for *S2* this improvement is only $\frac{62.22-59.88}{62.22}\times 100 = 3.7\%$, while $\frac{66.27-63.52}{66.27}\times 100 = 4.1\%$ for workload *S3* for the μ *SD*. Moreover, the 3σ *SD* follows the same trend as the μ *SD*. The energy consumption does not alter much with resizing. Although the operation is faster, the peak power consumption increases while there is a marginal reduction in leakage power.

SA-Only: In contrast, 'SA-Only' has the opposite effect and there is no impact on the *BLS*. However, a higher reduction for both μ and 3σ of the *SD* is observed as compared to the 'Cell-Only'. This delay depends strongly on the applied workload. Furthermore, the device drive strength marginally impacts the energy consumption. For example, at 10^8s increasing the device drive strength from 0% to 150%, has no impact on the μ BLS (small differences are due to Monte Carlo simulations) up to 0.2% while no impact for the 3σ BLS; and marginally reduces the energy consumption up to 5.0%, while μ *SD* significantly reduces with up to 11.4% for the worst-case (*S3*) workload.

Combined: For the 'Combined' case, the results show that both μ and 3σ of the BLS is following the same trend as the 'Cell-Only' and the μ SD only slightly improves with respect to the case 'SA-Only'. For example, the impact difference for a 150% device drive strength (DS) on BLS between 'Cell-Only' and 'Combined' is 0.3 mV, this difference can be attributed to Monte Carlo variations. With respect to the μ *SD*, in the case 'SA-Only' a 150% drive strength is able to achieve a reduction of 11.4%, while this is 15.2% for the combined case. Moreover, at time-zero, there is a slight difference. In addition, the energy consumption is similar as well.

Fig. 9 shows the impact of different device drive strength on both *BLS* and *SD* for the 'Combined' case, for workload *S3*. The figure shows that the BLS marginally reduces over time (i.e., up to 1.47% for Nom.DS, 0.94% for 125%DS and 0.97% for 150%DS) while the SD significantly increases (i.e., up to 7.01% for Nom.DS, 6.82% for 125% DS, and 6.73% for 150%DS) over the operational life time. The relative

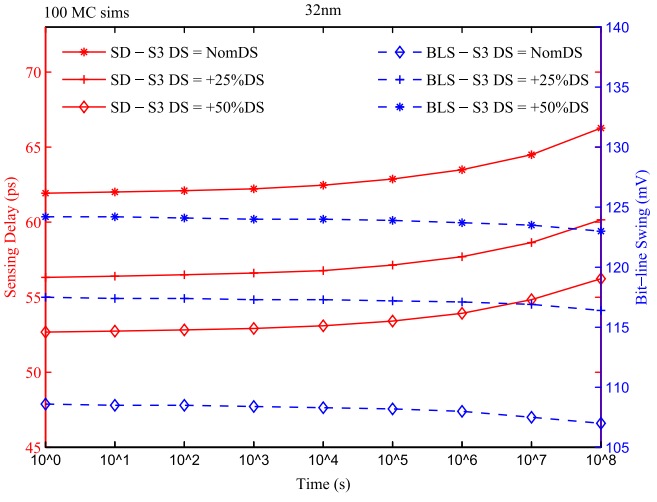

Fig. 9. Cell and SA strength degradation dependency of SD and BLS for S3 sequence.

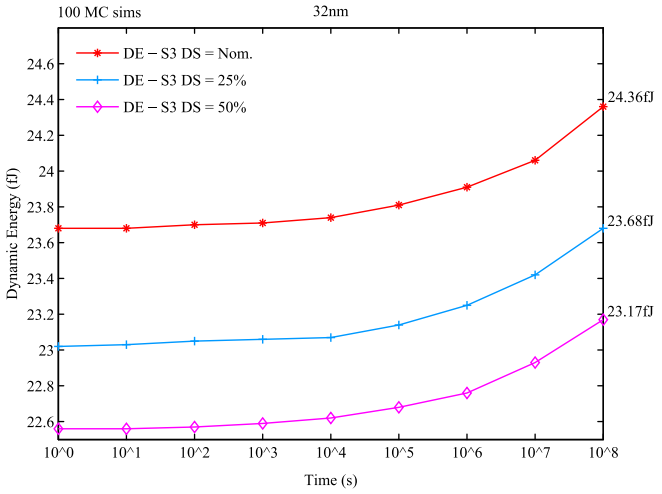

Fig. 10. Cell and SA strength degradation dependency of Dynamic Energy for S3 sequence.

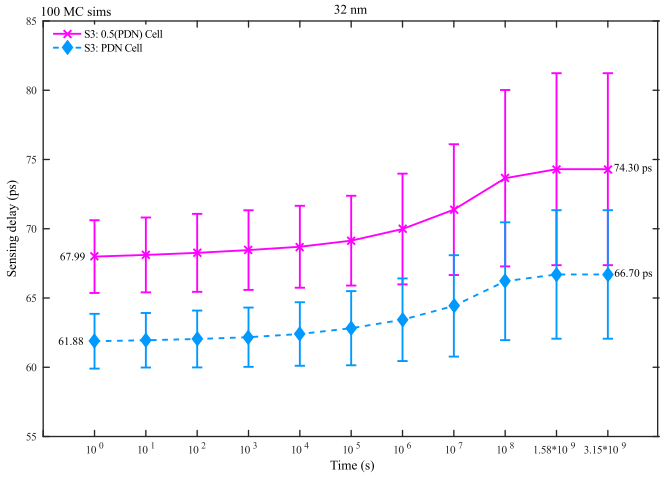

Fig. 11. Variation in SD for S3 sequence for two PDN ratios.

differences between the different drive strengths are marginal.

Fig. 10 shows the impact of the device drive strengths on the energy consumption for the 'Combined' case; the energy reduces as the drive strength increases, irrespective of the operational life time. However, the decrease does not exceed 5.0%. For example, at 10^8s and for *DS = Nom*, the energy consumption is 24.36 fJ, while this is 23.17 fJ for *DS = 150%*. In addition, the figure shows for a given drive strength that the aging causes the energy to slightly increase up to 3.0%, irrespective of the drive strength.

Overall, the most effective mitigation technique would be to re-size the SA Only, especially, when the area is also considered. Increasing the cell sizes affects the whole memory matrix, while increasing the 'SA-Only' has a much lower area impact.

6. Discussion

The memory cell and SA robustness are vital for the overall design of memory systems. Below some interesting observations are made.

The obtained results clearly show that for the considered SRAM design the cell has a low impact and that the SA is the major component responsible for the read path timing degradation, even under different voltages, temperatures and technology nodes. Therefore, this information can be used by the designers to optimize the design margins of the cell. One possible explanation of the marginal contribution of the cell degradation to the SD is the cell's strong pull down transistors. Therefore, we investigate the impact of a small cell where we assume W/L of the pull-down transistors to be 2.4 instead of 4.8 (see Fig. 1). The simulation is performed for 10 years using *S3* workload (Combined case), and the results both for the initial design and the smaller cell design (0.5PDN) are shown in Fig. 11. Although the trends of the SD increase for the two simulations seem similar, there are three interesting points to make. First, the relative increase of SD is 7% for the initial design, while this is 9% for the smaller one. Hence, the stronger the pull-down transistors of the cell, the smaller the contribution of the cell to the SD. Second, as the figure shows, the size of the pull-down transistors have also an impact on the SD spread; the stronger the devices, the smaller the spread (i.e., $+/-3\ \sigma$ represented by the boundaries of the vertical lines in Fig. 11). Third, the SD increases relatively faster after 10^4s, but then tends to saturate after 3 years (10^8s); the relative increase from 3 years to 10 years is no more than 0.7% for initial design and 0.9% for smaller version. Clearly the size of the cell's pull-down devices can be used also to minimize the degradation of the read path in SRAMS; and obviously this should be done while considering the SNM of the cell to ensure the stability of the cell as well.

Clearly, reducing the pull-down network (PDN) ratio (e.g., *pull-down transistors*) will only slightly increase the SD (2.0% difference). Hence, the memory cell area can be optimized as long as the SD is within acceptable limit. However, it is crucial to ensure the cell stability for the smaller cell. Therefore, we investigate for both the nominal and the smaller cell three metrics: *HSNM* (hold static noise margin), *RSNM* (read static noise margin), and *WTP* (write trip point) while considering two workloads (i.e., worst case (*WC*) and best case (*BC*)) for 3 years lifetime as shown in Table 6. The *HSNM* is the voltage V_n that flips the cell when it is injected at its internal node; it is swept from $-V_{dd}$ to V_{dd} while the word lines are disconnected from the bit lines. The *RSNM* is the V_n that flips the cell while the word lines are connected to the bit lines and V_n is swept from $-V_{dd}$ to V_{dd}. The *WTP* is the bit line voltage at which the cell flips while the word lines are connected to the bit lines; this voltage can be found by sweeping one of the bit lines potential from $-V_{dd}$ to V_{dd} [7, 28]. Table 6 shows that for both cells *HSNM* marginally reduces after 3 years (does not exceed 3.9%), and that the relative difference is not more than 1.40%, irrespective of the workload and cell size considered. However, the results show that the *RSNM* reduces quite significantly for both cells; this is up to 9.4% and 5.3% for the *WC* and *BC* workloads respectively, irrespective of the cell size. The difference between both cells is marginal. The table finally shows that the *WTP* increases marginally, irrespective of the workload and cell size considered, and that the relative difference between the two cells does not exceed 1.44%. It is worth noting that for the performed experiments, halving the cell size *does not impact the cell stability much as compared to the normal cell size.*

Our next observation is with respect to the impact of supply voltage. Higher voltage increases the bit line swing after an operation of 10^8s and *reduces* the SD. Hence, it can be used to compensate for the degradation of read path especially when the targeted application poses a

Table 6
Cell stability analysis.

	Time (s)	*Nominal cell size*		*Halve PDN ratio*	
		WC	*BC*	*WC*	*BC*
HSNM (mV)	0	312.8	312.8	309.2	309.2
	10^8	300.6	308.3	298.9	304.0
	Rel. %	−3.90	−1.44	−3.33	−1.68
RSNM (mV)	0	168.3	168.3	167.1	167.1
	10^8	152.5	160.0	153.2	158.2
	Rel. %	−9.39	−4.93	−8.32	−5.33
WTP (mV)	0	269.7	269.7	272.6	272.6
	10^8	271.2	277.9	275.1	279.5
	Rel. %	0.56	3.04	0.92	2.53

worst stress on the read path. Obviously, this comes at additional power consumption.

Furthermore, we observed that a higher temperature does not only reduce the BLS (which may impact the functionality) but also significantly increases the SD. Hence, using appropriate cooling is crucial for lifetime extension and degradation retardation.

Moreover, we observed that the degradation is more significant for SD and S3 workload at a lower technology node (*22-nm*); this leads to read failures even at nominal supply voltage. Hence, this implies that there must be a tradeoff between performance and reliability.

Finally, we observed that resizing the cell only marginally mitigates the read path degradation. In contrast, resizing the SA is much more effective. Therefore, more research should focus on effective mitigation schemes for SA, such as input switching in [14].

7. Conclusion

This paper investigated an accurate technique to estimate and mitigate the impact of Bias Temperature Instability (BTI) on the read path of a memory design while considering various degrading components i.e., *Cell only*, *SA only*, and *Combined* (i.e., cell and SA), and for different workloads, supply voltages, temperatures and technology nodes. Hence, the proposed methodology for the entire read path degradation analysis is an interesting case study as it allows for a better understanding of the overall degradation and hence for better design margin optimization. To ensure correct operational lifetime, designers must be aware about how the different parts of the memory degrade, how their interactions contribute to the degradation, and how all of these determine the overall degradation.

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