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A Switched-Capacitor DC-DC Converter Powering an LC Oscillator to Achieve 85% System Peak Power Efficiency and −65 dBc Spurious Tones

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***Abstract*— In this paper, we propose a new scheme to directly power a 4.9–5.6 GHz LC oscillator from a recursive switched-capacitor DC-DC converter. A finite-state machine is integrated to automatically adjust the conversion ratio and switching frequency of the converter such that its DC output voltage is within ±5% of the desired 1V across input voltage range 1.3–2.2 V and <2 mA load current conditions. A gate-driver circuit is embedded in each switch of the converter to guarantee constant on-resistance across PVT variations without sacrificing device reliability. Furthermore, a spur reduction block (SRB) is embedded in the oscillator to suppress the ripple induced spurs by stabilizing its tail current. Both the converter and the oscillator are implemented in 40-nm CMOS technology. The measured peak power efficiency of the converter is 87%, while its spot noise is <1.5 nV/$\sqrt{\text{Hz}}$, which does not degrade the phase noise of the oscillator. The SRB suppresses the spur to < −65 dBc under the 30 mV_{pp} ripple of the converter.**

***Index Terms*— Switched-capacitor DC-DC converter, LDO replacement, gate-driver circuit, LC oscillator, spur reduction block, phase noise, voltage controlled oscillator (VCO).**

I. Introduction

THE Internet-of-Things (IoT) is constantly spanning new applications [1]. IoT devices are mostly powered from energy stored in supercapacitors or batteries. However, their output voltage fluctuates due to the availability of energy sources and the environment in which they are placed. Consequently, a DC-DC buck converter cascaded with a linear low drop-out (LDO) regulator is customarily used to generate a 'clean' and stable nominal supply voltage of ∼1 V V_{DD} to supply nanoscale CMOS circuits and systems, as shown in Fig. 1 (a) [2]–[5]. Note that the intermediate DC-DC converter is invariably required, otherwise the large voltage drop across the LDO would severely degrade the system efficiency when the LDO is directly connected to the storage element.

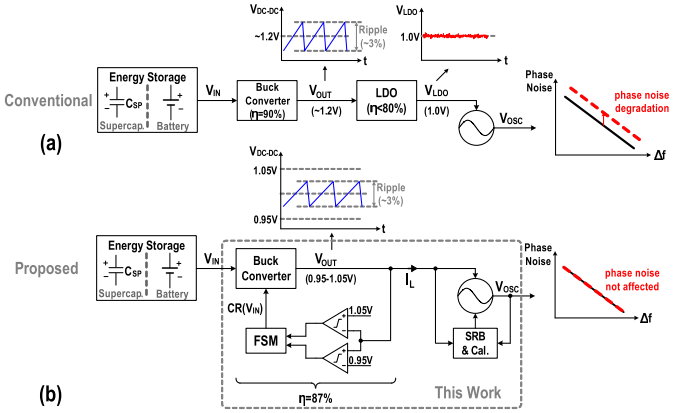

Fig. 1. System diagram of: (a) conventional cascade of a buck converter with an LDO to power up an oscillator, and (b) proposed solution, which avoids the use of the LDO.

Full system integration favors switched-capacitor (SC) buck converters over the traditional inductor-based structures [6]. However, SC converters operate at much higher switching frequencies, thus forcing to increase the LDO's bandwidth and its quiescent current [7]. On the other hand, the equivalent input noise of the LDO's error amplifier and its feedback resistors, directly appears at the output and it can only be filtered at frequencies above the output pole [8]. To minimize the LDO noise, the quiescent current of its error amplifier should increase. Moreover, its feedback resistors should be reduced while keeping their ratio constant, which, in turn, increases the current flowing through them. Hence, there exists a trade-off between the LDO's noise and current efficiency. Considering a so-called cap-less LDO (i.e. no external capacitor at the LDO output), a larger value of the power supply rejection (PSR) forces the output non-dominant pole to be

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further away from the dominant one to ensure the LDO's stability [9]. Hence, the size of the LDO pass transistor must be reduced accordingly, thus increasing the drop-out voltage, leading to the decrease of power efficiency. Therefore, another trade-off exists between the LDO's PSR and power efficiency. The aforementioned trade-offs are even more critical in RF oscillators where the LDO output noise and ripple can easily pollute the oscillator spectral purity.

Since the LDOs are noisy, bulky and inefficient [8], [10]–[12], it would appear beneficial for the IoT circuitry to be connected directly to the buck converter. However, the LDO elimination would impose several challenges on the design of the DC-DC converter and the LC oscillator. First, in face of a wide range of input voltage ($V_{\rm IN}$) and load current (I_L) variations, the converter needs to provide a relatively accurate and constant DC voltage (1 V$\pm$5%) for the oscillator. Second, the converter's noise should be low enough in order not to degrade the inherent phase noise performance of the oscillator. Third, due to the lack of LDO isolation, the converter's ripple is up-converted and appears at the oscillator's output spectrum, degrading its spectral purity. Hence, new techniques should be adapted in the oscillator biasing circuit to reduce its supply pushing factor.

Fig. 1 (b) shows the block diagram of the proposed solution, in which the use of the LDO is avoided, and the DC-DC converter directly powers up the LC oscillator but without degrading its spectral purity. To keep the output voltage of the converter ($V_{\rm OUT}$) relatively constant against $V_{\rm IN}$ or I_L variations, a finite state machine (FSM)-based conversion ratio (CR) and switch frequency ($f_{\rm SW}$) modulation is introduced, which also allows having a predictable spectrum of the converter output voltage. To have an almost constant spot noise at $V_{\rm OUT}$, a new gate-driver circuit is embedded in all converter's switches to guarantee minimum switch on-resistance across the process variations and the entire input voltage range. Finally, to mitigate the effects of ripples generated by the DC-DC converter, a spur reduction block (SRB) is embedded into the oscillator biasing network to suppress its supply sensitivity.

The paper is organized as follows: Section II derives the requirements on the conversion ratio and introduces a recursive switched-capacitor (RSC) topology along with an analysis of its output resistance and losses and a FSM-based digital control. A novel gate-driver circuit to drive the switches is proposed in Section III. In Section IV, the noise level required by $V_{\rm OUT}$ is derived such that it will not affect the inherent spectral purity of the oscillator. Based on the converter ripple, the required supply pushing of the oscillator is derived in Section V, and a spur reduction block based on our previous published LC oscillator [13] is presented. Section VI presents the measurement results as well as a comparison with the state of the art.

II. DC-DC Converter Design

In this section, the required conversion ratio (CR) range and resolution are derived. A converter topology that meets the CR requirement is then presented along with its output resistance analysis. To continuously adjust the CR, a digital FSM-based control is introduced. Finally, the losses of the resulting converter topology are analyzed, to determine the optimal switch sizes.

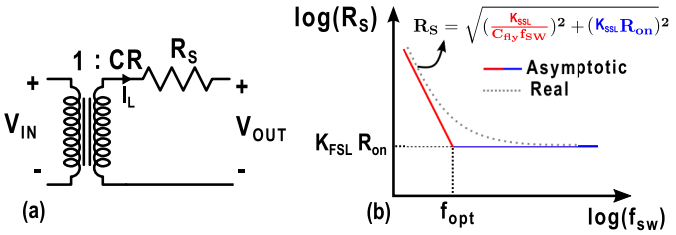


Fig. 2. (a) Equivalent model of an SC DC-DC converter; and (b) its equivalent output resistance versus switching frequency.

A. Requirements on Conversion Ratio Range and Resolution

Fig. 2 (a) shows the equivalent model of an SC DC-DC converter. Its output voltage can be written as

$$V_{\rm OUT} = V_{\rm IN} \cdot {\rm CR} - R_S \cdot I_L, \tag{1}$$

where R_S is the equivalent output resistance of the converter and I_L is the load current. During the operation, the CR and/or R_S must be adaptively adjusted for $V_{\rm IN}$ and I_L variations to keep the output voltage within the $\pm$5% of the oscillator nominal supply voltage (i.e., $V_{\rm OUT}$ = 1V). R_S can be modulated through the switching frequency ($f_{\rm SW}$) or the converter capacitance ($C_{\rm fly}$). However, the former requires to modulate f_{SW} by several orders of magnitude [14]–[17], making it difficult for the oscillator to keep the spur level low enough over the entire $f_{\rm SW}$ range. The latter involves a significant reduction of $C_{\rm fly}$ [18], [19], resulting in larger ripples, further worsening the oscillator spurs. Consequently, in this design, we *mainly* modulate the conversion ratio to simplify the converter control but still to obtain a predictable f_{SW}, facilitating its direct connection to the oscillator.

With the aid of Eq. (1), and considering the targeted V_{OUT} accuracy (i.e., $\pm$5%), and V_{IN} and I_L ranges, one can easily calculate the lowest and the highest CR by

$$\begin{cases} {\rm CR}_{\rm min} = \dfrac{0.95 V_{\rm OUT} + R_S I_{L,\rm min}}{V_{\rm IN,max}} \\ {\rm CR}_{\rm max} = \dfrac{1.05 V_{\rm OUT} + R_S I_{L,\rm max}}{V_{\rm IN,min}}. \end{cases} \tag{2}$$

On the other hand, at a constant input voltage, the difference between the output voltage corresponding to two consecutive CRs should be finer than the targeted V_{OUT} accuracy. Consequently,

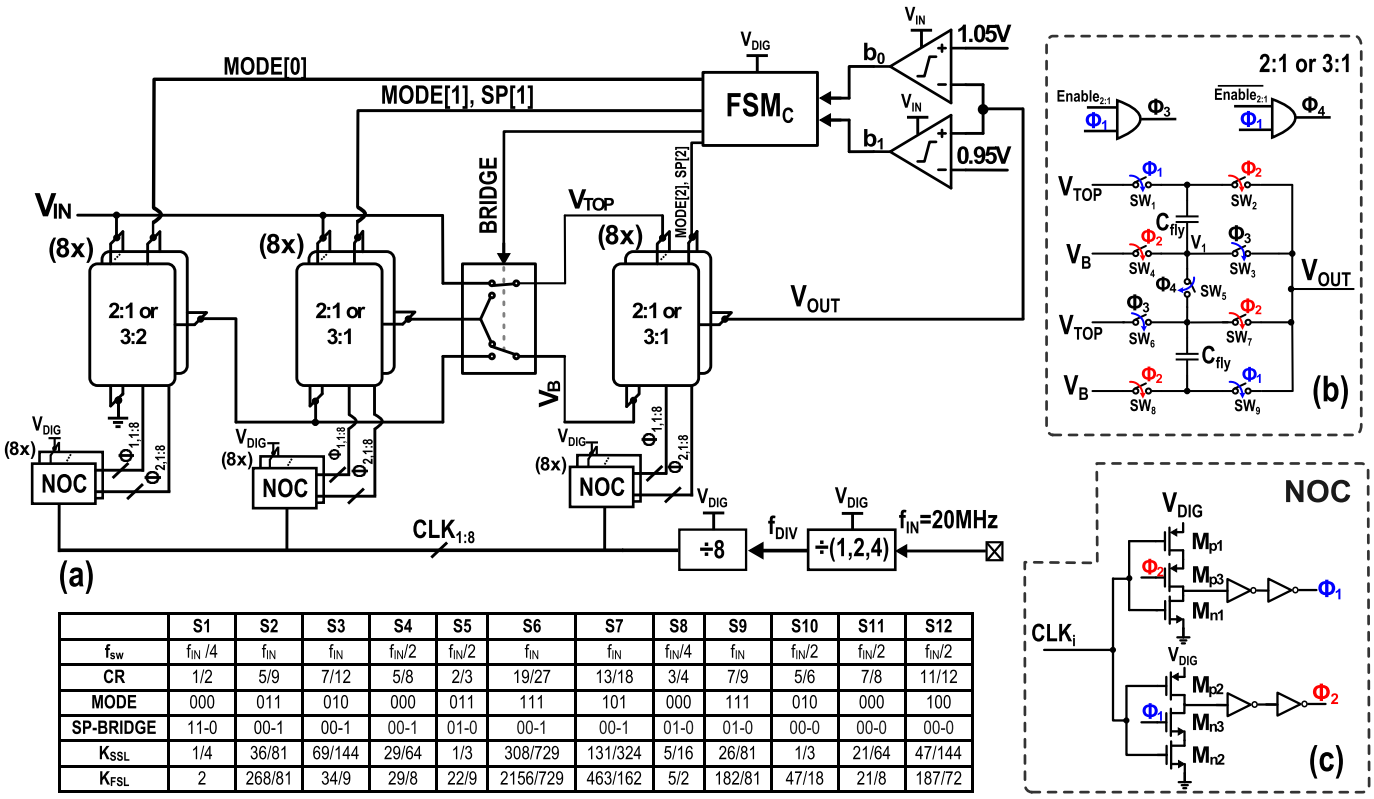
$$V_{OUT,i+1} - V_{OUT,i} < 0.1 V_{OUT}. \tag{3}$$

Considering the worst case scenario ($V_{IN} = V_{IN,max}, I_L = I_{L,min}$), Eq. (3) can be written as

$$V_{IN,max}({\rm CR}_{,{\rm i}+1} - {\rm CR}_i) - (R_{S_{i+1}} - R_{S_i}) I_{L,min} < 0.1 V_{OUT}. \tag{4}$$

Assuming a constant R_S, the required CR resolution can be estimated by

$${\rm CR}_{res} = ({\rm CR}_{i+1} - {\rm CR}_i) < \frac{0.1 V_{OUT}}{V_{IN,max}}. \tag{5}$$



	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
f_{sw}	f_{IN} /4	f_{IN}	f_{IN}	f_{IN}/2	f_{IN}/2	f_{IN}	f_{IN}	f_{IN}/4	f_{IN}	f_{IN}/2	f_{IN}/2	f_{IN}/2
CR	1/2	5/9	7/12	5/8	2/3	19/27	13/18	3/4	7/9	5/6	7/8	11/12
MODE	000	011	010	000	011	111	101	000	111	010	000	100
SP-BRIDGE	11-0	00-1	00-1	00-1	01-0	00-1	00-1	01-0	01-0	00-0	00-0	00-0
K_{SSL}	1/4	36/81	69/144	29/64	1/3	308/729	131/324	5/16	26/81	1/3	21/64	47/144
K_{FSL}	2	268/81	34/9	29/8	22/9	2156/729	463/162	5/2	182/81	47/18	21/8	187/72

Fig. 3. (a) Detailed block diagram of the three-stage recursive switched capacitor (RSC) DC-DC converter with a table showing the control signals for all the converter states; (b) detailed representation of a 2:1 or 3:1 stage and (c) the non-overlapping clock (NOC) generator.

Eq. (5) indicates that the CR resolution should be improved if a larger input voltage or a finer V_{OUT} accuracy is targeted. This increases the total number of CRs, which, in turn, adversely impacts on the complexity of the converter and its power efficiency.

With R_S of 50 Ω, 1.3 V $< V_{IN} <$ 2.2 V, and 0.5 mA $< I_L <$ 2 mA, the resulting CR varies from 0.5 to 0.9 with a resolution of 0.045. Considering the side effects of the converter ripple, the number of CRs has been increased from 9 to 12.

B. Topology Definition

Several SC topologies have already been published in literature that could meet the CR range and resolution requirements discussed above. In particular, a Successive Approximation Register (SAR) SC converter presented in [20] offers a resolution of $V_{IN}/2^N$ (where N is the number of stages), but it suffers from a limited power density as a flying capacitance of 2.24 nF is required to deliver a current $<$ 0.3 mA. An asymmetric shunt SC converter was presented in [21] that increases the number of CRs even further but at a cost of increasing the losses in the slow switching limit (SSL) region. A recursive switched-capacitor (RSC), introduced in [14], offers the same resolution as the SAR but with a lower SSL loss for the same number of stages. However, to achieve our required resolution, it would require *five* 2:1 stages, thus degrading the converter's output impedance and efficiency.

To cover the required CRs, while minimizing the SSL losses and avoiding cascading many RSC stages as in [14], we propose a 3-stage RSC topology but with two CR options (2:1, 3:2 or 3:1) per each stage. The implemented three-stage RSC converter is shown in Fig. 3. Since CR_{min} is about 0.5, the first stage does not need the 3:1 configuration and its output should always be connected to the bottom voltage of the second stage, thereby allowing for a higher CR. The second and third stages operates only in the 2:1 and 3:1 modes with one set of bridge switches placed between them. This allows connecting the output of the second stage to either the top or the bottom voltage of the third stage.

Each stage of the converter is divided into eight smaller interleaved units. This allows to avoid the need for an output capacitor and to reduce the switching losses of the converter [22]. Moreover, each unit embeds the non-overlapping clock (NOC) circuit. The clock $f_{IN} = 20$ MHz is provided externally, while the frequency division (of 1, 2 or 4) to generate f_{DIV} is implemented internally by means of a flip-flop-based frequency divider. Then, the eight interleaved clock phases ($CLK_{1:8}$) are generated by further dividing f_{DIV} [23]. The NOC embedded in each unit generates the two non-overlapped phases (Φ_1 and Φ_2).

C. Charge Flow and Impedance Analysis

To always guarantee $V_{OUT} = 1\,\text{V} \pm 5\%$, while $V_{IN} \in \{1.3 - 2.2\}$ V, the stages of the RSC converter are rearranged in a series/parallel configuration. This has an impact on the charge flow of each stage, and therefore, the output impedance of the converter.

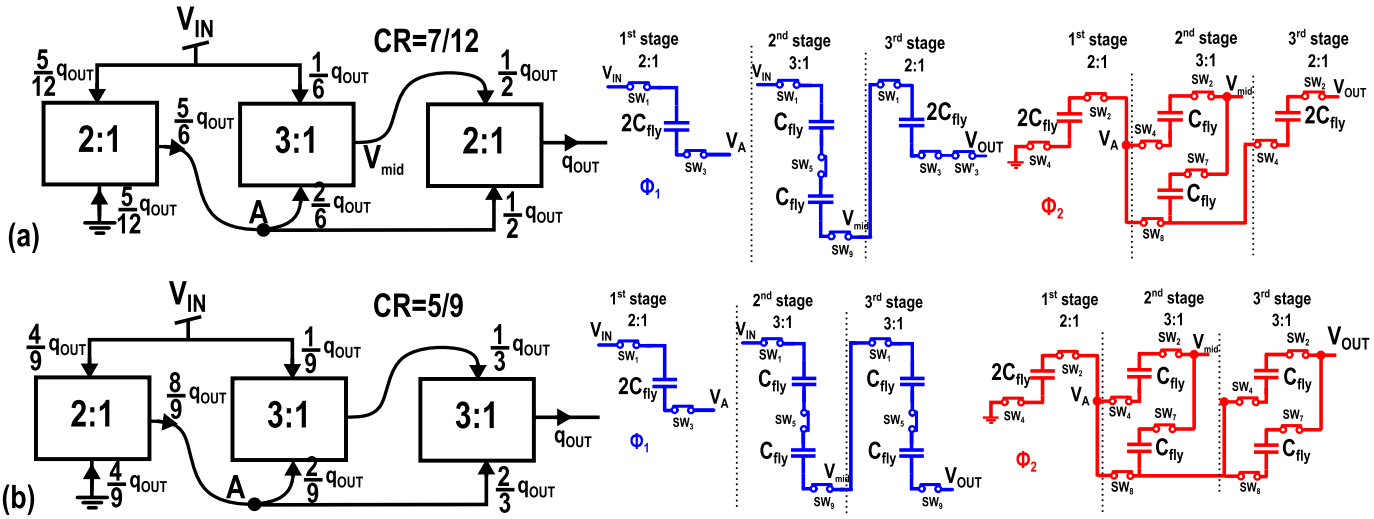


Fig. 4. Charge flow through the inter-stage connections for a conversion ratio of: (a) 7/12, and (b) 5/9, along with the their equivalent circuits for 1 of the 8 units during Φ_1 and Φ_2.

Figs. 4(a) and (b) illustrate two configurations which realize CRs of 7/12 and 5/9, along with their equivalent circuits for 1 of the 8 units. Please notice that node V_A during Φ_1 (V_{mid} during Φ_2) is not floating as it is connected to the other four units operating in the opposite phase.

In Fig. 4(a), the last stage loads half of the output charge q_{OUT} from the second stage. Given that the second stage has a CR of 3:1 ($V_{mid} = \frac{V_{IN}+2V_A}{3}$), the charge taken from the node A ($\frac{2}{6}q_{OUT}$) is twice that from V_{IN} ($\frac{1}{6}q_{OUT}$). Applying KCL at node A, the charge delivered by the first stage is found to be $\frac{5}{6}q_{OUT}$, and it is equally divided between its top and bottom voltages ($V_A = \frac{V_{IN}}{2}$). Fig. 4(b) shows a similar example of charge flow for CR = 5/9.

In the conventional RSC topology with only 2:1 stages, irrespective of the converter configuration, the output current of each stage is a binary-weighted fraction of the load current (i.e., $I_L/2^{N-i}$), thus the switches and capacitors are sized based on the current flowing through them. However, in our topology, the charge flow of each stage depends on the particular configuration, as shown in the two previous examples. Hence, in our design, all the stages are sized identically.

The equivalent output impedance of the converter, R_S, can be modeled by the well-known equation reported below [24]:

$$R_S = \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\left(\frac{K_{SSL}}{C_{fly} f_{SW}}\right)^2 + \left(K_{FSL} R_{on}\right)^2}. \tag{6}$$

R_{SSL} and R_{FSL} are the resistances in the slow and fast switching limit (SSL, and FSL), respectively. K_{SSL} and K_{FSL} are topology-dependent coefficients valid respectively in the SSL and FSL regions [24]. Fig. 2(b) shows a sketch of Eq(6) versus the switching frequency. In the SSL region, the charge-sharing mechanism dominates the losses, whereas, in the FSL region, the finite on-resistance of the switches is the main source of inefficiency.

To compute R_{SSL} and R_{FSL}, one can use the charge multiplier vectors $\mathbf{a_c}$ and $\mathbf{a_s}$ which can be directly computed from the charge flow analysis and represent the charge flowing through each capacitor and each switch, respectively [6], [14], [21], [24]. Assuming that all the switches have the same R_{on}, the resistances in the slow and fast switching limits can be written as

$$R_{SSL} = \sum_{i=1}^{N} \frac{\mathbf{a_{c,i}^2}}{f_{SW} C_i}, \tag{7}$$

and

$$R_{FSL} = \sum_{i=1}^{N} \sum_{j=1}^{switches} 2\mathbf{a_{s,i,j}^2} R_{on}, \tag{8}$$

where the summation over i accounts for the number of stages N, while the summation over j accounts for the number of switches in each stage. C_i is the flying capacitance of i^{th} stage. In the example shown in Fig. 4(a), the charge multiplier vectors are

$$\mathbf{a_c} = \left[\frac{5}{12}\ \frac{1}{6}\ \frac{1}{6}\ \frac{1}{2}\right]$$
$$\mathbf{a_{s,i}} = \left[\frac{5}{12}\ \frac{1}{6}\ \frac{1}{2}\right]^T, \tag{9}$$

while for the example shown in Fig. 4(b) the charge multiplier vectors are

$$\mathbf{a_c} = \left[\frac{4}{9}\ \frac{1}{9}\ \frac{1}{9}\ \frac{1}{3}\ \frac{1}{3}\right]$$
$$\mathbf{a_{s,i}} = \left[\frac{4}{9}\ \frac{1}{9}\ \frac{1}{3}\right]^T. \tag{10}$$

When a stage is used in the 3:1 or 3:2 configuration, two flying capacitors and seven switches are operated, leading to two identical elements in the vector $\mathbf{a_c}$.

With the aid of the charge multiplier vectors and Eqs. (7)–(8), the output resistance of the proposed converter versus CR is calculated at $f_{SW} = 5$ MHz and depicted in Fig. 5. As can be gathered from the red line, R_S greatly varies with the particular configuration used, dramatically affecting the converter efficiency. Moreover, even with a constant load current, moving towards a higher CR might lead to a lower output voltage due to the R_S increase. It is therefore

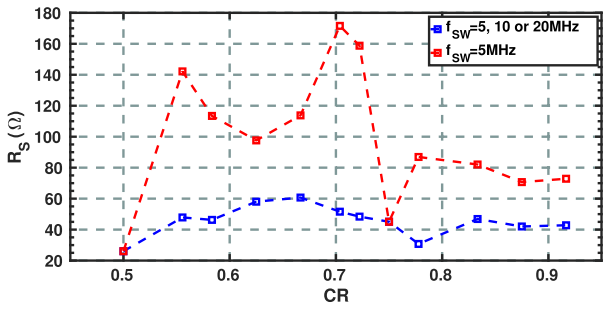


Fig. 5. Calculated output resistance of the converter with fixed (red) and adaptive (blue) switching frequency.

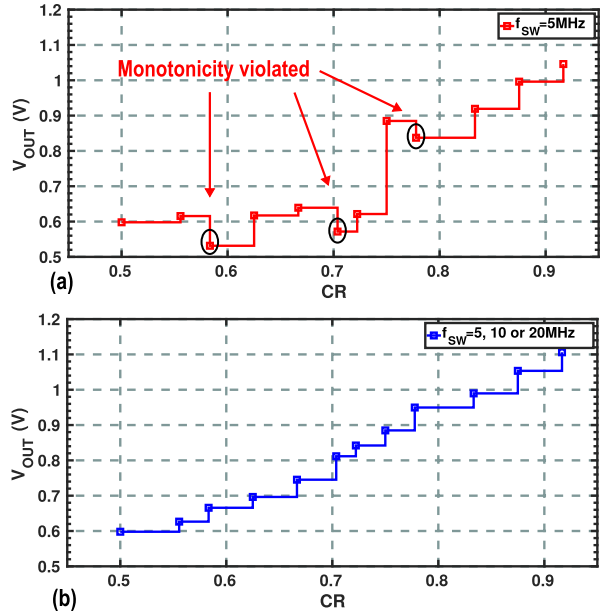


Fig. 6. Output voltage of the converter versus CR with (a) fixed and (b) adaptive switching frequency, when $V_{IN} = V_{IN}^{min}, I_L = I_L^{max}$.

necessary to guarantee the monotonicity of the output voltage as a function of CR. This condition can be modeled by the following equation

$$V_{OUT,i+1} - V_{OUT,i} > 0, \quad \forall i \in \{CRs\}. \tag{11}$$

Considering the worst-case scenario for the monotonicity ($V_{IN} = V_{IN,min}, I_L = I_{L,max}$), Eq. (11), can be rewritten as

$$V_{IN,min}(\mathrm{CR}_{i+1} - \mathrm{CR}_i) - (R_{S_{i+1}} - R_{S_i}) I_{L,max} > 0. \tag{12}$$

Fig. 6 (a) plots V_{OUT} for different CRs with $V_{IN} = V_{IN,min}$ and $f_{SW} = 5$ MHz. V_{OUT} should always increase when moving from one CR to the next higher one. However, for CR of $\frac{7}{12}$, $\frac{19}{27}$ and $\frac{7}{9}$, V_{OUT} decreases, proving that in those two configurations the monotonicity condition is violated.

On the other hand, large R_S variations can also violate the resolution requirement imposed by Eq. (4). To better investigate the resolution requirement, a parameter Δ is introduced and defined as the voltage difference of the output voltages corresponding to two consecutive CRs normalized to the resolution. Hence, Δ can be written as

$$\Delta = \frac{V_{OUT,i+1} - V_{OUT,i}}{0.1 V_{OUT}}. \tag{13}$$

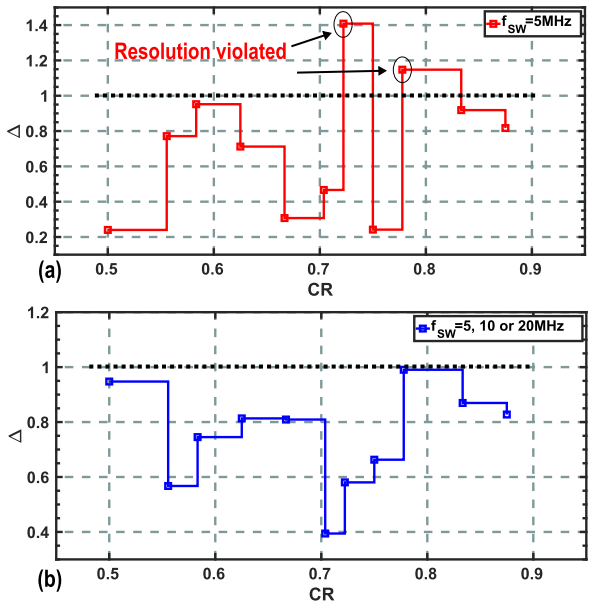


Fig. 7. Calculated resolution of the converter in the worst-case scenario ($V_{IN} = V_{IN}^{max}, I_L = I_L^{min}$) for (a) fixed, and (b) adaptive switching frequency.

Fig. 7 (a) plots the parameter Δ versus CRs for a fixed $f_{SW} = 5$ MHz. As can be seen, at CR $= \frac{13}{18}$ and $\frac{7}{9}$, $\Delta > 1$, thereby violating the resolution requirement.

To overcome the above mentioned problems, the switching frequency in the configurations with a higher R_S can be modulated by a factor of 2× or 4×, resulting in the resolution and monotonicity conditions being always met (see Figs. 7(b) and 6(b)). Moreover, Fig. 5 shows that by adapting f_{SW} to the particular configuration, the output resistance of the RSC converter can be kept fairly constant, thereby maximizing the power efficiency.

Finally, as a general design guide, Eqs. (4) and (12) can be combined into Eq. (14), which provides a compact expression for the two main requirements of SC converters, namely resolution and monotonicity.

$$\begin{cases} V_{IN,max}(\mathrm{CR}_{i+1} - \mathrm{CR}_i) - (R_{S_{i+1}} - R_{S_i}) \\ \quad I_{L,min} < 0.1 V_{OUT} \\ V_{IN,min}(\mathrm{CR}_{i+1} - \mathrm{CR}_i) - (R_{S_{i+1}} - R_{S_i}) \\ \quad I_{L,max} > 0. \end{cases} \tag{14}$$

D. FSM-Based Digital Control

During the operation, V_{OUT} is compared with two reference levels, 0.95 V and 1.05 V, at a rate of 1 MHz. Two bits ($b_{0,1}$) are generated to indicate whether V_{OUT} is within the range, higher or lower. The converter's FSM (FSM_C) then decides to keep the same state or move to the next higher/lower one. Each state has a unique set of control signals (MODE, SP, BRIDGE), which determines f_{SW}, the series or parallel connection of stages, and the CR of each stage. The table in Fig. 3(b) reports all the converter's states and their control signals.

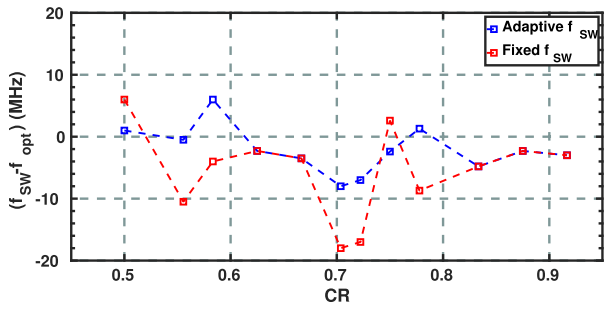


Fig. 8. Difference between the frequency at which the converter is operated and the optimum one in case of fixed and adaptive switching frequencies.

E. Steady-State Loss Analysis

SC DC-DC converters suffer from several losses that impact their power efficiency. The two main sources of such losses are due to the dynamic operation of the switches (switching losses) and due to the output resistance of the converter (conduction losses). Those two contributions can be modeled with the following equation:

$$P_{LOSS} = nC_g V_{sw}^2 f_{SW} + R_S I_L^2, \tag{15}$$

where n is the number of switches operating at f_{SW} with a clock voltage swing of V_{sw}, and C_g is the equivalent gate capacitance of each switch. To maximize the power efficiency, it is required that the converter operates at the boundary between the fast and slow switching limits. Hence, the contribution of the two resistances in the two regions should be the same (i.e., $R_{SSL} = R_{FSL}$), with the optimal f_{SW} being equal to

$$f_{SW} = f_{opt} = \frac{\sum_{i=1}^{N} \frac{a_{c,i}^2}{C_i}}{R_{FSL}} = \frac{\rho}{R_{FSL}}. \tag{16}$$

Fig. 8(a) shows the difference between the frequency at which the converter is operated and f_{opt}. By modulating the switching frequency by only a factor of 2× or 4×, the DC-DC converter can be operated relatively close to its optimal f_{SW}.

By substituting Eq. (16) into Eq. (15), the power loss can be written as

$$P_{LOSS} = \frac{n \cdot C_g \cdot V_{sw}^2 \cdot \rho}{K_{FSL} R_{on}} + \sqrt{2} K_{FSL} R_{on} (I_{L,max})^2. \tag{17}$$

As can be gathered from Eq. (17), the power loss depends on the particular configuration of the converter (n, K_{SSL}, K_{FSL}) and the switch width (C_g, R_{on}). By introducing the capacitance and on-resistance of a unit-width transistor as $\overline{C_g} = \frac{C_g}{W}$ and $\overline{r_{on}} = R_{on} W$, Eq. (17) can be rewritten as

$$P_{LOSS} = \frac{n \cdot \overline{C_g}\ V_{sw}^2\ W^2\ \cdot \rho}{K_{FSL} \overline{r_{on}}} + \sqrt{2}\ \frac{\overline{r_{on}}}{W}\ K_{FSL} \left(I_{L,max}\right)^2. \tag{18}$$

The optimal switch width (W_{opt}) can be found by minimizing Eq. (18) with respect to W, leading to

$$W_{opt} = \left(\frac{\sqrt{2} K_{FSL}^2 \overline{r_{on}^2} \left(I_{L,max}\right)^2}{2n \overline{C_g} \rho V_{SW}^2} \right)^{\frac{1}{3}}. \tag{19}$$

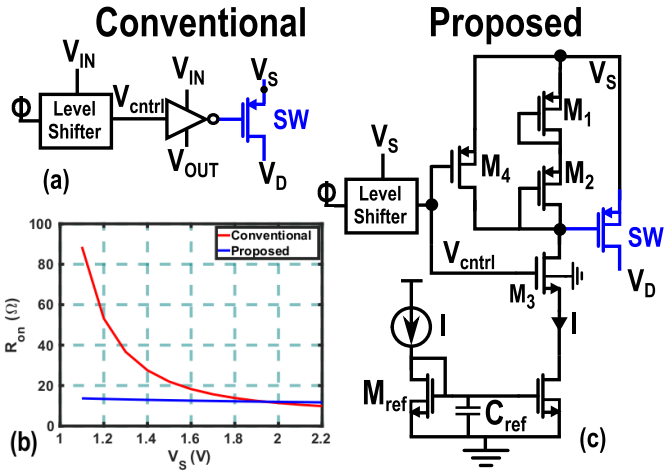


Fig. 9. (a) Schematic of a conventional gate-driver circuit, with (b) the equivalent series resistance versus the supply voltage, and (c) the proposed gate driver circuit, resulting in a constant R_{on}.

Using thin-oxide, minimum channel-length transistors, $\overline{r_{on}}$ and $\overline{C_g}$ equal $1 \cdot 10^3\ \Omega \cdot \mu m$ and $1 \cdot 10^{-15}\ \frac{F}{\mu m}$, respectively. After the circuit optimization, the implemented switch width was chosen to be $W = 130\,\mu$m.

III. Gate-Driver Design

In this section, a new gate-driver circuit is introduced, which offers constant on-resistance across PVT variations without compromising the reliability of the whole converter.

In nanometer CMOS technology, the breakdown voltage of a thin-oxide device is well below the maximum input voltage of the converter. To resolve this issue, prior arts apply different supply rails (e.g., V_S and $V_S/2$ in Fig. 9(a)) as the high and low voltage levels for driving the switch gates. However, as V_{IN} (i.e., V_S) decreases, the gate-source voltage, $|V_{GS}|$, of the switches approaches $|V_{th}|$, leading to an exponential increase in their on-resistance, significantly increasing R_{FSL}, as depicted in Fig. 9(b). This impacts the converter power efficiency, the monotonicity and the resolution conditions. To further investigate it, Fig. 10 plots Δ and V_{OUT} versus CR for different R_{on}. When $R_{on} \geq 40\,\Omega$, changing CR from 0.5 to 0.55 (moving from S1 to S2 in the table of Fig. 3) reduces the output voltage, thereby violating the converter's monotonicity condition. Similarly, the resolution when moving from S4 to S5 is greater than the required output voltage accuracy, thereby violating Eq. (5).

To resolve the aforementioned issues, we propose a gate-driver circuit [25], as shown in Fig. 9(b). When the control voltage V_{cntrl} for the switch SW is high, the bias current I flows through two cascaded diode-connected transistors, $M_{1,2}$, to generate the desired $|V_{GS}|$ (e.g., $\sim 1\,V$) for the switch. $M_{1,2}$ are minimum-width but long-length devices to achieve a higher resistance, minimizing the bias current and avoiding the efficiency degradation. However, when V_{cntrl} goes 0 to turn off the switch, the time constant associated with the discharging process of the gate-to-source capacitance of the switch is high due to this large resistance, slowing down the discharging process. Consequently, M_4 is added to provide a low-impedance path for speeding up the discharging

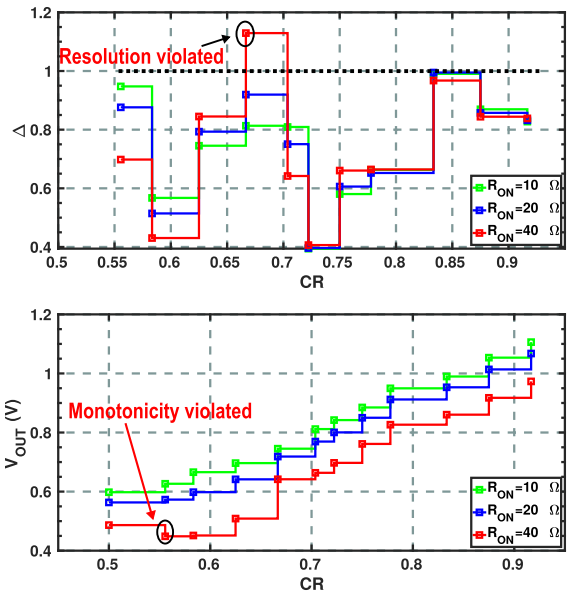


Fig. 10. Resolution and monotonicity conditions versus CR for different values of R_{on}.

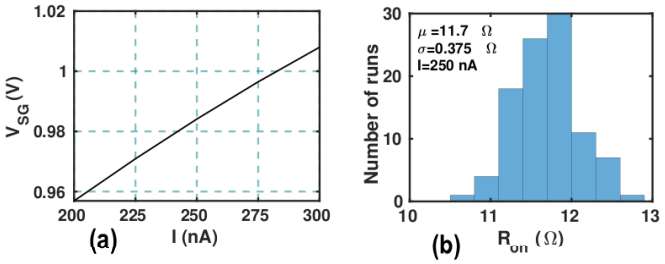


Fig. 11. (a) V_{SG} of the switch SW when a biasing current variation of ±30% is applied; (b) Monte Carlo simulation of its R_{on}.

procedure. $M_{3,4}$ are thick-oxide devices, thus contributing to an increase in the dynamic losses. However, their size is much smaller than that of the switch, leading to a negligible power-efficiency degradation. In the proposed circuit, $M_{1,2}$ and switch SW are of the same type. Hence, their V_{th} changes in the same direction with PVT variations, leading to an almost constant $|V_{GS}|-|V_{th}|$ and ON-resistance of the channel. This has been verified by means of a Monte Carlo simulation with 100 samples, as shown in Fig. 11(b). Moreover, by providing a constant overdrive voltage to all the switches, the switching losses of the converter merely depend on the number of switches being operated.

To properly drive the gates of $M_{3,4}$, a level shifter (LS) is required since the clock signal Φ is in the low-voltage domain. However, the LS only drives $M_{3,4}$, which are much smaller than the main switch SW. In the worst-case scenario, the LS output swings from 0 to $V_{IN} = V_{INmax} = 2.2\,\text{V}$, while consuming $\sim 104\,\text{nW}$. There is a total of 240 switches, of which, in the worst-case scenario (State S6), only 168 are operated simultaneously with a 50% duty-cycle, leading to a power overhead of 17.5 μW, which is negligible when compared to the delivered output power. Moreover, the non-overlapping condition after the LS is still guaranteed, as its propagation delay (hundreds of ps) is much smaller than the non-overlapping time (several ns).

A. Practical Design Considerations

The transistor type, its terminals connections, and especially the body-diode direction of the converter's main switches are of relevant interest to the designer. In this design, the body and source terminals of a PMOS switch are connected, as shown in in Fig. 9(c). Therefore, to guarantee that the body-diode is always reverse biased, the potential of the source terminal, V_S, must always be higher than the drain voltage, V_D. However, when either the second or third stage works in the 3:1 mode, the use of a single PMOS switch as SW3 in Fig. 3(b) cannot satisfy this requirement. To resolve that, SW3 comprises here two cascaded PMOS switches whose drain terminals are connected. This ensures that when the stage operates in the 3:1 mode, at least one of the two switches is always off. Moreover, both switches follow Φ_1 during the 2:1 mode.

With the conventional gate-driver circuit (see Fig. 9(a)), the switches in each converter's stage operate in different voltage domains. Therefore, it becomes challenging to guarantee the non-overlapping condition between two clock phases over the entire input voltage range, potentially affecting the functionality and performance of the converter. With the proposed gate-driver circuit, the realization of the non-overlapping clocks is simplified as all switches operate in the same voltage domain and are powered by the stable output voltage of the converter ($V_{OUT} = 1\,\text{V}$). The non-overlapping clock generator circuit is shown in Fig. 3(c). By adding transistors M_{n3} and M_{p3}, each phase of the clock can change state only when the other phase has already altered, thus guaranteeing the non-overlapping condition.

IV. Noise Requirements

In this section, the requirement on the power supply noise is first derived; then the main noise sources of the DC-DC converter are analyzed and discussed.

A. Supply Noise Requirements

The voltage noise on the power supply can significantly degrade the oscillator's spectral purity [26]. In this subsection, the noise requirements of the DC-DC converter are derived such that it will not significantly affect the oscillator performance. The inherent phase noise of LC oscillator can be calculated by [27]:

$$\mathcal{L}(\Delta f) = 10log_{10}\Big(\frac{kT(1+\gamma)}{2Q^2P_{DC}\alpha_I\alpha_V}\big(\frac{f_0}{\Delta f}\big)^2\Big), \qquad (20)$$

where k is the Boltzman' constant, T is the absolute temperature expressed in Kelvin, γ is the excess noise factor of the transistors, Q is the tank quality factor, and P_{DC} is the oscillator power consumption. α_I is the current efficiency, defined as a ratio of the magnitude of the fundamental current harmonic over the oscillator DC current, and α_V is a voltage efficiency, defined as the ratio of the oscillation amplitude over the oscillator power supply. f_0 and Δf are the carrier and offset frequencies with respect to the main tone, respectively.

On the other hand, the phase noise induced by the noise on the power supply can be estimated as

$$\mathcal{L}_{sup}(\Delta f) = 10log_{10}\Big(\frac{K_V^2}{\Delta f^2}V_{n,supply}^2(\Delta f)\Big) \qquad (21)$$

where $V^2_{n,supply}(\Delta f)$ is the power spectral density (PSD) of the supply noise and K_V is the supply pushing factor of the oscillator. To avoid degradation of the inherent PN of the oscillator, it is required that $\mathcal{L}_{sup}(\Delta f) \ll \mathcal{L}(\Delta f)$, leading to

$$V^2_{n,supply} \ll kT(1+\gamma)2Q^2 P_{DC}\alpha_I \alpha_V \left(\frac{f_0}{K_V}\right)^2. \quad (22)$$

Assuming $P_{DC} = 1\,\text{mW}$, $K_V = 40\,\text{MHz/V}$, $\gamma = \frac{2}{3}$, $f_0 = 5\,\text{GHz}$, $\alpha_I = \frac{4}{\pi}$, $\alpha_V = 0.5$, $Q = 10$ for a complementary oscillator, the maximum supply noise should be $< 23\,\text{nV}/\sqrt{\text{Hz}}$. Note that oscillators with better phase noise (i.e., higher Q or P_{DC}) impose even more stringent noise requirements on their supply voltage.[1]

Note that the reported spot noise of LDOs with high current efficiency (i.e., > 90%) is much higher than the supply noise tolerated by the oscillator [11], [12], [28], [29]. To reduce the output noise of the LDO, its quiescent current should be increased, which leads to a severe current efficiency degradation (e.g., 70% in [30]) or an external filtering capacitor must be used [8].

B. Noise Analysis of the DC-DC Converter

The three main noise sources of the proposed converter are the transistors in the current mirror of the gate driver circuit, the two comparators and the on-resistance of the switches of the DC-DC converter.

Transistor M_{ref} in Fig. 9 generates current noise I_n that is mirrored at the source terminal of M_3 and modulates the gate-to-source voltage of the main switch, thereby modulating its on-resistance. Its noise contribution can be filtered by the capacitor C_{ref} when

$$Z_{C_{\text{ref}}} \ll \frac{1}{g_{\text{m,ref}}}. \quad (23)$$

Hence, the minimum value of C_{ref} should be

$$C_{ref} \gg \frac{I}{f\pi(V_{GS} - V_{th})}. \quad (24)$$

To filter the noise at frequencies above $f = 10\,\text{kHz}$, $C_{ref} \approx 100\,\text{pF}$ is required, which is negligible when compared to the total on-chip flying capacitance.

The comparators' outputs directly drive the FSM_C. Hence, when the FSM_C does not change state, the gain from the output of the comparators to the converter's output is zero, resulting in a null noise contribution of the comparators.

The SC converter acts as an RC circuit from a noise point of view. Consequently, its integrated output noise is $\propto kT/C_{fly}$, whereas its spot noise is $\propto R_{on}$. By employing the gate driver proposed in the previous section, the noise spectral density of the proposed converter is more predictable and well-behaved against PVT. Fig. 12 shows the simulated output noise in different converter states. At lower frequencies ($f < 10\,\text{kHz}$), the output noise is dominated by the flicker noise component of M_{ref}. As the frequency increases, its noise contribution is filtered by the capacitor C_{ref}, while the total output noise is dominated by the thermal noise of the switches' on-resistance.

[1]For example, with a $Q = 15$, $V_{n,supply} < 15\,\text{nV}/\sqrt{\text{Hz}}$)

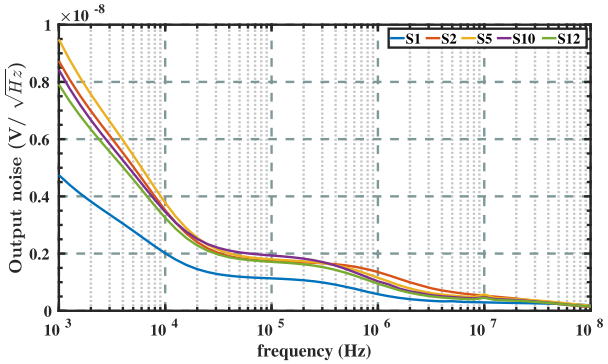


Fig. 12. Output noise of the DC-DC converter when operated in different configurations.

It is worth mentioning that, contrary to the LDO approach, such low noise is achieved without consuming any additional current or using any external components.

V. Ripple Requirements

The voltage ripple on the DC-DC converter's output is up-converted and appears at the oscillator's output spectrum, degrading its spectral purity. In this section, the requirements on the supply sensitivity of the oscillator are firstly derived, followed by discussion on the implementation of the spur reduction block (SRB) in the oscillator.

A. Oscillator's Supply Pushing Factor

A sinusoidal ripple on the supply voltage of the oscillator (with a peak-to-peak amplitude V_m) induces spurious tones around the carrier, whose amplitude (S_{spur}) with respect to the carrier can be calculated by

$$S_{\text{spur}} = 10\ \log_{10}\left(\frac{K_V V_m}{4 f_{SW}}\right)^2 dBc. \quad (25)$$

The peak-to-peak amplitude of the SC DC-DC converter's ripple can be expressed as

$$V_{rip} = \frac{I_L^{max}}{C_{\text{fly}} f_{SW}}. \quad (26)$$

Eq. (25) can be rewritten into Eq. (27) which highlights the maximum K_V that the oscillator should have to meet certain spectral requirements.

$$K_V < \frac{4 f_{SW}^2 C_{\text{fly}}}{I_{L,max}} \cdot 10^{(S_{\text{spur}})/20}. \quad (27)$$

For $S_{\text{spur}} = -65$ dBc, $f_{SW} = 20$ MHz, $C_{fly} = 2.7\,\text{nF}$ and $I_{L,max} = 2$ mA, the maximum supply pushing of the oscillator is $K_V = 2.4$ MHz/V.

Typically, oscillators have a much higher supply pushing factor ($K_V \approx 100\,\text{MHz}/V$ for class-D oscillator [31] and $K_V \approx 18$ MHz/V for class-F oscillator [32]). To solve this issue, we previously presented an LC oscillator which brings the supply pushing factor to as low as $K_V \approx 100$ KHz/V [13]. The next subsection describes the SRB circuit in more detail.

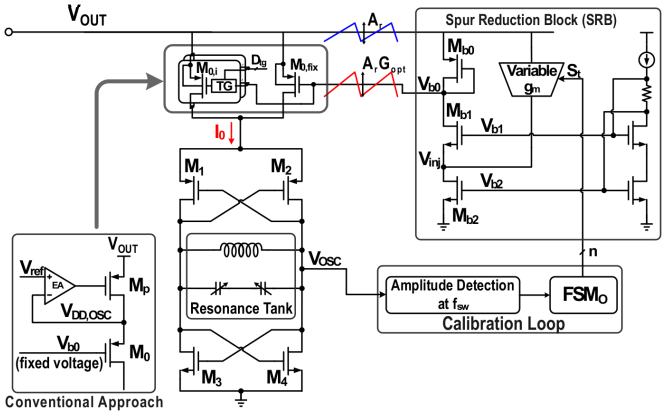


Fig. 13. Detailed implementation of the oscillator with the spur reduction block (SRB) based on [13].

B. Spur Reduction Block

When an LDO is used to stabilize the oscillator supply in the conventional approach, the tail transistor M_0, biased by a fixed voltage, is cascaded with the pass transistor of the LDO, M_p, to adjust the oscillator current, I_0 (see Fig. 13). By removing the LDO, the voltage headroom consumed by M_p is avoided, improving the system efficiency. At the same time, M_0 consists of a bank of unit transistors $M_{0,i}$, each of which could be switched on separately by a transmission gate (TG in Fig.13) to set the desired DC level of I_0. As shown in [13], I_0, and the corresponding oscillation amplitude V_{osc}, should be stabilized to reduce the oscillator's supply pushing, since the variation of the oscillation frequency mainly stems from the variation of the equivalent value of the voltage-dependent parasitic capacitance of the core transistors. To accomplish this, the supply ripple is replicated on the gate terminal of M_0 through the SRB. To account for the finite output resistance of M_0, the gain of the replica is properly tuned by varying the control code of the variable g_m stage. The optimal code is automatically found with the on-chip calibration loop that sweeps the control code using an FSM (FSM_O). For each control code setting, the amplitude detector estimates the variation of the oscillation amplitude at f_{SW}. When this variation reaches its minimum, the code is deemed optimal and fixed by FSM_O. Note that the calibration is only performed in one of the converter states and used during the entire operation.

Considering the SRB's finite bandwidth, a phase shift between the supply ripple and its replica at high ripple frequencies would result in residue variations of I_0, degrading the spur levels. The capacitive load at V_{b0} and the SRB current are optimized based on the highest f_{SW} of the converter (20 MHz). At lower f_{SW}, the oscillator inherently suffers from a lower spur suppression due to a higher tank impedance, requiring tighter I_0 variations. Thus, the SRB gain resolution is designed for the lowest f_{SW} (5 MHz) to guarantee a low enough spur over the f_{SW} range. The SRB is effective as long as M_0 stays in the saturation region. Thanks to the CR adjustment of the converter, the DC level of the oscillator supply only varies by ± 50 mV, which is low enough to keep M_0 safely in saturation. Since the SRB is fully integrated into the oscillator biasing network, only the noise of its extra variable g_m stage degrades the oscillator phase noise (PN) by a negligible amount (i.e., $\sim$0.06 dB). Moreover, the current consumed by the SRB is only 20 μA, which leads to a current efficiency degradation of 98%. A more detailed description of the SRB circuit can be found in [13].

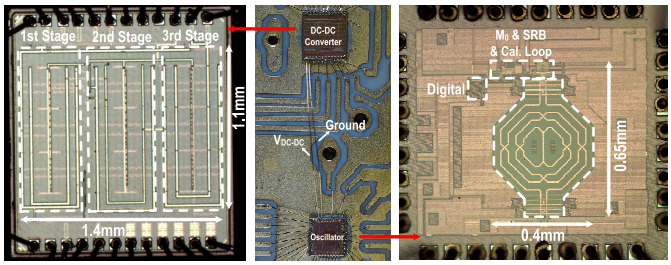


Fig. 14. Die micrographs of the DC-DC converter (left), the oscillator (right), and photo highlighting their direct connection (middle).

VI. Experimental Results

The proposed DC-DC converter and the oscillator are fabricated in the same standard 40-nm CMOS process. Their chip micrographs, as well as a photo highlighting the direct connection of the converter's output to the oscillator supply rail, are shown in Fig. 14. They occupy an active area of 1.54 mm^2 and 0.23 mm^2, respectively. The total on-chip capacitance of the DC-DC converter $C_{\text{fly}} = 2.7$ nF is equally divided among the three stages, as discussed in Section II.B.

A. DC-DC Converter Measurements

Fig. 15 (a) shows the line regulation of the converter for $I_L = 1$ mA along with the state of the FSM_C. Figures 15 (b) and (c) show that as V_{IN} decreases (or increases), both CR and f_{SW} change accordingly to keep V_{OUT} within the desired range.

Fig. 16 (a) shows that the parameter Δ, as defined in Section II.C, in the worst-case scenario ($V_{IN} = V_{INmax} = 2.2$ V and $I_L = I_{Lmin} = 0.5$ mA) is always lower than 1, proving that the first condition imposed by Eq. (14) is met. Fig. 16 (b) illustrates the output voltage of the converter (orange line) and the signal (blue line) that changes the state of FSM_C. As CR rises, V_{OUT} increases monotonically, proving that, in the worst-case scenario for the monotonicity ($V_{IN} = V_{INmin} = 1.3$ V and $I_L = I_{Lmax} = 2$ mA), the second condition imposed by Eq. (14) is also met.

Fig. 17 (a) shows the converter's power efficiency versus V_{IN} for different load currents. The power efficiency of an ideal LDO is added as a comparison. The converter's efficiency stays >80% across the entire 1.3–2.2 V input voltage range for $I_L = 1.5$ mA. Fig. 17 (b) shows that inaccuracy of the biasing current of the gate-driver circuit, $I = 300$ nA $\pm$30%, leads to a negligible degradation of its power efficiency, proving that the static current consumed by the gate driver circuit has negligible effects on the power efficiency, as explained in Section III. For $V_{IN} > 2$ V, the power efficiency is the highest, since the converter operates at the lowest CR = 1/2, in which it exhibits the lowest output resistance due to the lowest number of operating switches, as discussed in Section II.C.

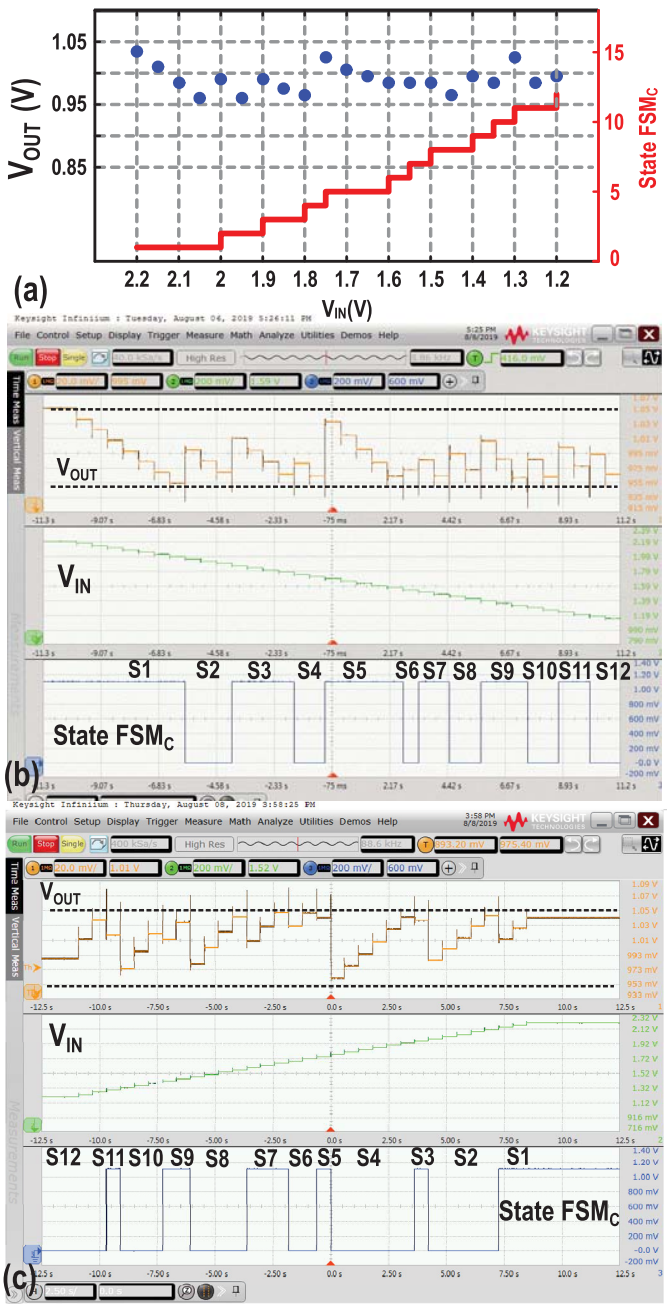


Fig. 15. (a) Measured output voltage of the DC-DC converter versus V_{IN} for $I_L = 1\,\text{mA}$; (b) transient waveform of V_{OUT} for descending and (c) ascending V_{IN} values along with the signal, that triggers the change in the FSM.

Fig. 18 shows that the converter can recover back to the desired range right after two FSM_C clock cycles (i.e., $2\,\mu\,\text{s}$) while facing a 0–2 mA current step with a 10 ns rise time.

The measurement of the output noise of the DC-DC converter is limited by the noise floor of the spectrum analyzer. Hence, an LNA with a gain of 35 dB is placed after the DC-DC converter. The resulting spectrum is shown in Fig. 19 (a) (blue curve) for the FSM_C in State S2. When the LNA is used, the amplitude of the peaks is amplified by 35 dB, whereas the noise is amplified by only 10 dB, proving that the measurement is no longer limited by the noise floor of the spectrum analyzer. At around 6 MHz, the measured noise integrated over the

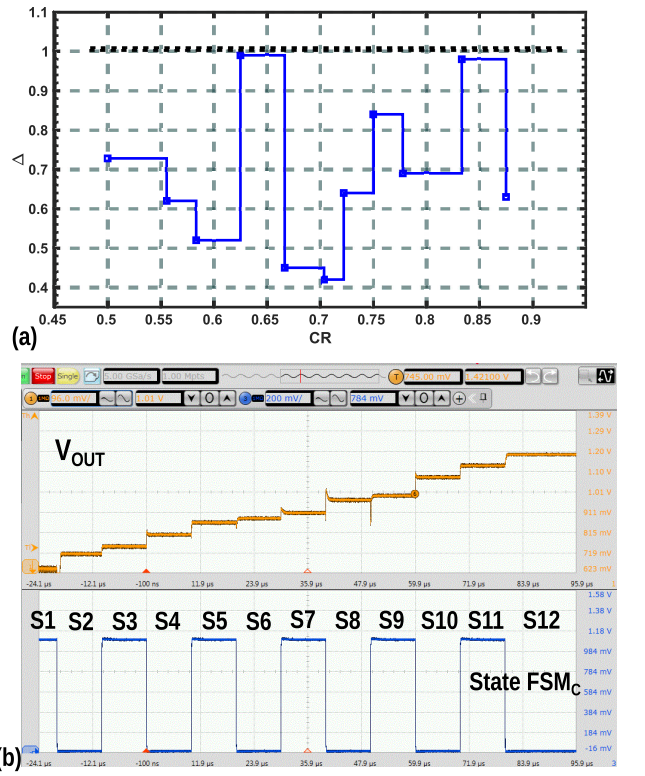


Fig. 16. Measurement results of (a) the resolution of the converter for $V_{IN} = V_{INmax} = 2.2\,\text{V}$ and $I_L = I_{Lmin} = 0.5\,\text{mA}$; (b) the monotonicity of the converter for $V_{IN} = V_{INmin} = 1.3\,\text{V}$ and $I_L = I_{Lmax} = 2\,\text{mA}$.

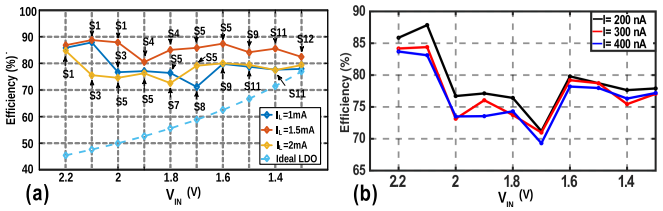


Fig. 17. Measured power efficiency versus V_{IN} for different values of (a) load current, and (b) biasing current of the gate driver circuit.

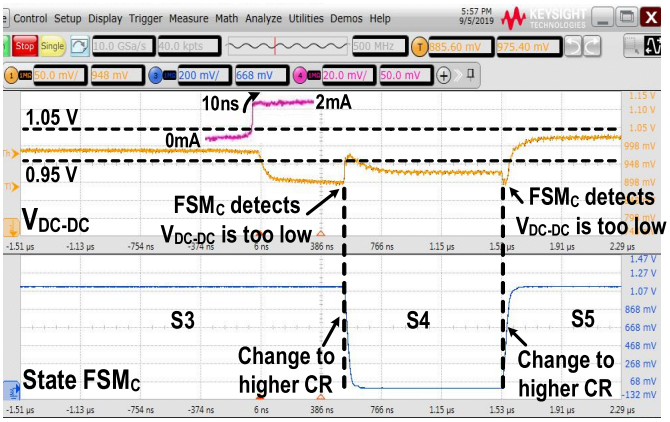


Fig. 18. Response of the converter (orange line) to a current step from $0 - 2\,\text{mA}$ (purple line) along with the signal that triggers the change in the FSM_C (blue line).

resolution bandwidth of the spectrum analyzer (100 kHz) is $\approx -81\,\text{dBm}$. As a result, the spot noise at around 6 MHz is $-81\,\text{dBm} - 35\,\text{dB} + 10\log_{10}(100\,\text{kHz}) = -166\,\text{dBm/Hz} \approx 1.12\,\text{nV}/\sqrt{\text{Hz}}$. Furthermore, the output spot noise level at

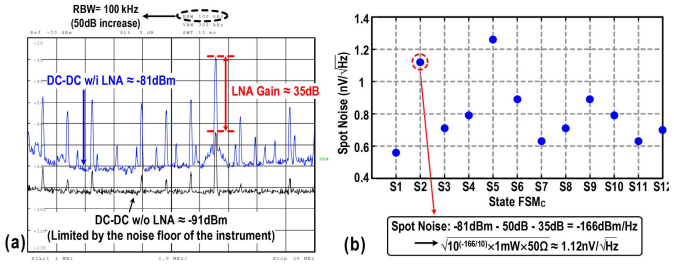


Fig. 19. (a) Spectrum of the output voltage of the DC-DC converter with (blue line) and without (black line) the use of an LNA; (b) spot noise of the converter across different FSM_C state.

TABLE I

COMPARISON WITH DC-DC ARCHITECTURES

	This work	[20] JSSC16	[14] JSSC14	[39] JSSC17	[21] TPE19	[38] JSSC19
Topology	3b Multiratio	7b SAR	4b binary	2-/3- Phase SC Conv.	Asymmetrical Shunt	Algebraic Series/Parallel
CMOS tech	40 nm	180 nm	250 nm	130 nm	250nm	65nm
V_{IN} (V)	1.3-2.2	3.4-4.3	2.5	1.6-3.3	3.3	0.25-1
V_{OUT}(V)	1	>0.45	0.1-2.2	0.5-3.0	0.4-2.8	1
I_{OUT}(mA)	<2	<0.3	<2	<250	<10	<20.1
η_{MAX} (%)	87	72	85	91	87	80
f_{SW} (MHz) (Range)	5,10,20 (X4)	0.08-2.7 (X34)	0.2-9 (X45)	<10 (>X1)	NA	NA
#CR	12 (Theory,22)	117 (Theory,127)	15	6	187	7
C_{fly}(F)	2.7n	2.24n	3n	2x(1μ)	10n	3n
C_{OUT}(F)	0	NA	0	1μ	0	0
Power density (mW/mm²)	1.3	0.27	0.95	-	1.01	22.7

~ 6 MHz is also measured over different converter states and shown in Fig. 19(b). The noise is always $< 1.5\,\text{nV}/\sqrt{\text{Hz}}$ which is well below the supply noise requirement of the oscillator ($V_n < 23\,\text{nV}/\sqrt{\text{Hz}}$), as discussed in Section IV.

Table I provides a comparison with other DC-DC converters targeting a high number of conversion ratios. Fig. 20 reports the peak power efficiency of state-of-the-art DC-DC converters versus the ratio of maximum-to-minimum switching frequency ($R_f = \frac{f_{SW,max}}{f_{SW,min}}$) required for the voltage regulation. R_f should normally be limited to relax the design complexity of the SRB and to avoid lowering the power efficiency, as discussed in Section V.B. At the same time, the number of CRs should be large enough to provide a *fairly* constant output voltage in the face of input voltage and load current variations. As can be gathered from Fig. 20, our work achieves one of the highest peak efficiencies with 12 CRs and an R_f as low as 4. References [15], [34]–[37] achieve higher power efficiency, but with a very limited number of CRs (e.g., 1–3). [39] implements 6 different CRs by using two off-chip flying capacitors of 1 μF each, making the whole converter bulky. R_f of [15], [37] and [40] is also much larger than in our work, leading to a more complex system design.

B. System-Level Measurements

Fig. 21(a) shows the phase noise of the oscillator when powered from a noise-free supply and from the DC-DC converter in different FSM_C states for the oscillator frequency

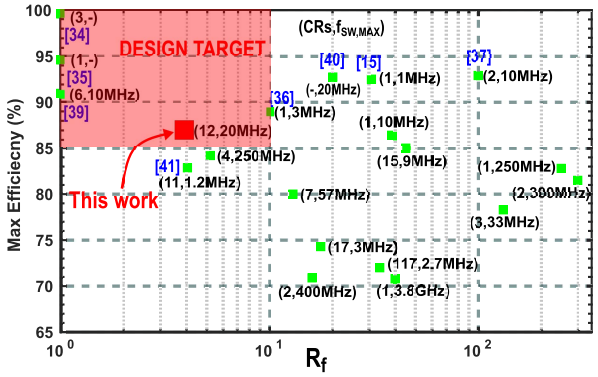


Fig. 20. Peak power efficiency of state-of-the-art DC-DC converters versus the ratio of maximum-to-minimum switching frequency ($R_f = \frac{f_{SW,max}}{f_{SW,min}}$). The number of implemented CRs, and $f_{SW,max}$ are reported in the parenthesis.

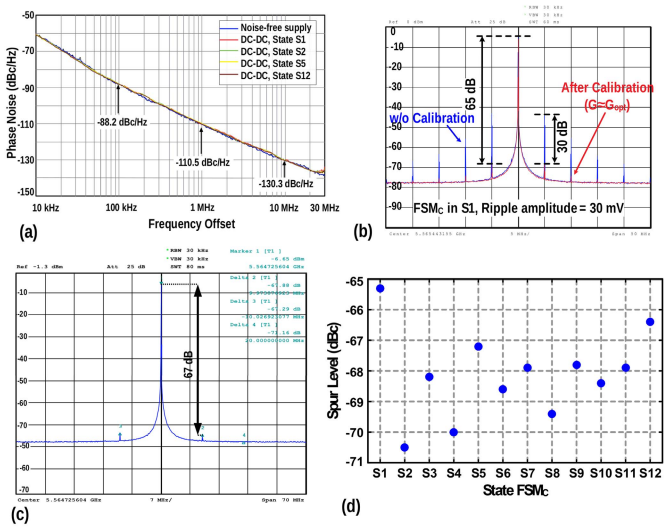


Fig. 21. (a) Measured oscillator PN performance at $f = 5.5$ GHz and (b) its spectrum before and after calibration of the SRB with FSM_C in State S1 and (c) State S5; (d) spur level across different converter states when the oscillator is calibrated only at State S1.

of 5.5 GHz. The inherent PN of the oscillator is not degraded, proving that the condition imposed by Eq. (22) is met and the supply does not limit the oscillator performance. Fig. 21(b) shows the spectrum of the oscillator before and after calibration when powered from the DC-DC converter with a ripple amplitude of ~ 30 mVpp. The spur level is reduced by 30 dB and reaches -65 dBc after the calibration, which is 15 dB lower than the IoT requirements. A similar measurement is also performed while the oscillator is powered by the DC-DC converter in state S5, and the spectrum is depicted in Fig. 21(c). Fig. 21(d) shows the spurious level of the oscillator across all the states of the FSM_C when the SRB of the oscillator is only calibrated in State S1. The spur level always stays below -65 dBc.

Table II summarizes the performance of the whole system and compares it with prior art. Our work is more suitable for a full system integration by avoiding external components and demonstrates the highest system peak power efficiency thanks to the removal of the LDO voltage headroom. Since the SRB is always engaged, the equivalent PSR of our approach is

TABLE II
COMPARISON WITH SYSTEMS POWERING UP LC OSCILLATORS

		This work	[2]	[7]	[8]	[30]
System Architecture		DC-DC+ OSC	DC-DC+ LDO+OSC**	DC-DC+ LDO††	LDO+ OSC	LDO+ OSC
CMOS tech		40 nm	55 nm	65 nm	250 nm	65 nm
V_{IN} (V)		1.3-2.2	1.6-3.3#	2.4-2.6	-	-
V_{IN-LDO} (V)		X	1.4	1.05	2-2.5	0.6
$V_{OUT-LDO}$ (V)		1.0	1.2	1	1.5-2	0.4
$V_{LDO,DROP}$ (mV)		0	200	50	500	200
η_{DC-DC} (%)		87	92	80.3	-	-
η_{LDO}(%)		X	<85.7	<94.9	<79	<60
η_{SRB}(%)		98	X	X	X	X
η_{TOTAL}(%)		85	<79	<76.2	<79	<60
#ext. comp		0	2	0	1	0
Osc. supply noise ($nV/\sqrt{Hz}$)		1.26 (S5) @10MHz	-	14.1# @10MHz	32 @100KHz	22.4*** @10MHz
C_{LDO}(F)		X	-	41p	50n	390p
Quiescent Current (μA)		20	-	10	120	500
PSR (dB)	@5MHz	48.9*	20	12.8†	35	31†
	@10MHz	43*	20	12.8†	-	26†

*PSR of the SRB **Oscillator is part of the whole transceiver †Simulated value

#Extracted from the measurement result ††Can be used to power up an oscillator

***Calculated from phase noise with K_{SUP}=50 MHz/V X=Not needed

calculated in this table from the difference (in dB) between the spur level measured at the optimum setting and the calculated one based on the simulated K_V of the oscillator without the SRB. Compared to the systems with LDOs, our fully passive SC converter exhibits $>10\times$ lower supply noise and our SRB shows >15 dB higher power supply rejection, preserving the oscillator's spectral purity for IoT applications.

VII. CONCLUSION

This paper presents an LC oscillator directly powered by a recursive switched-capacitor (RSC) DC-DC converter without using any LDOs or external components. By automatically adjusting the conversion ratio (CR), the DC variations of the converter output are kept within ±5% of the desired voltage. A gate-driver circuit is proposed to guarantee a constant low R_{on} of the converter's switches, thereby meeting the resolution and monotonicity requirements while avoiding efficiency degradation. The converter output noise is $<1.5\,\text{nV}/\sqrt{\text{Hz}}$, and does not degrade the oscillator phase noise, while the spur reduction block (SRB) embedded in the oscillator suppresses the ripple-induced spurs to < -65 dBc, satisfying the requirement of IoT applications.

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