A 24GHz Radar Receiver in CMOS

Proefschrift

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Summary

This thesis investigates the system design and circuit implementation of a 24GHz-band short-range radar receiver in CMOS technology. The propagation and penetration properties of EM wave offer the possibility of non-contact based remote sensing and through-the-wall imaging of distance stationary or moving objects. The feasibility of realizing these concepts in hardware with a small form factor could accelerate commercialization and initiate new product opportunities. Minimizing the receiver power consumption to the 15mW range enables 4 hours of continuous operation from a 1.2 gram button sized lithium battery. CMOS technology has the potential for realization of both the RF transceiver and baseband processor in a single chip.

An understanding of the functional requirements is a prerequisite for system optimization. The 15mW power budget necessitates the continuous nature of FMCW radar configuration, which obviates the requirement for a power-hungry transmitting amplifier. FMCW radar in short-range applications benefits from the phase noise correlation between transmitted and received waveforms, which may be exploited to lower the power consumption of the LO generation circuits. A choice for the heterodyne receiver architecture mitigates erroneous detection due to second-order intermodulation distortions caused by interfering radar transmitters nearby, accuracy degradation due to frequency pulling of the ultra-wideband VCO, and signal quality degradation due to flicker noise generated by CMOS transistors. The power dissipation and hardware overhead of a heterodyne receiver are relaxed by proper frequency planning and elimination of the image-reject filter due to frequency chirping property of the FMCW signal.

A frequency downconverter for the radar receiver is realized by integrating a LNA, a Gilbert-type mixer, and a VCO running at the carrier frequency. A varactorless frequency tuning scheme is proposed for the VCO which breaks through the conventional trade-offs seen in continuous and wideband mm-wave frequency generation between capacitance tuning ratio, quality factor, and operating frequency in CMOS design. Inductive frequency tuning is enabled by a transformer resonant tank which exploits the gyration (90°) across the input/output terminal voltages of a transconductor. The parallel resonant frequency is controlled by sweeping the sign and magnitude of the transconductance. The VCO is frequency-agile, and is continuously tunable by altering the DC bias current of the transconductance cell. Adaptability between frequency tuning and power consumption is possible. Two VCO test circuits are reported in this thesis. (1) A proof of concept in 0.13μm RF-CMOS consumes 43mW from a 1.2V supply. The frequency coverage is from 23.2GHz to 29.4GHz (23.6% tunable range) and the phase noise is –92.6dBc/Hz at 1MHz frequency offset. (2) A miniaturized prototype is implemented in 90nm CMOS for the radar receiver. It consumes 5.7mW from a 1.0V supply. Its maximum frequency

range is from 18.6GHz to 21.2GHz (13.1% tunable range) and phase noise is –82.0dBc/Hz at 1MHz frequency offset.

Operation of a CMOS LNA in the moderate inversion region and at a frequency approaching the transistor's operational limit deteriorates its power gain and noise figure. A two-step LNA optimization algorithm is proposed in this thesis which addresses both the device and circuit levels. Transistor dimensions and biasing are set for optimal power gain, noise figure, linearity, bandwidth, and matching network loss. Partitioning the limited power budget across multiple gain stages maximizes the overall power gain. Optimizing the transistor's interaction with bilateral power flows in a multi-stage amplifier is facilitated by Smith chart based visualization and a computer-aided design methodology. The advantages of this methodology are demonstrated by design examples.

Current-feedback by a 3-port transformer in a cascode LNA is proposed in this thesis in order to increase the power gain and lower the noise figure performance under low-power conditions. The feedback modifies the relationship between the input referred voltage and current noise sources of a common-gate MOS transistor, and thereby fulfills the internal interface impedance conditions in the cascode LNA for optimal power gain and noise figure matching. A two-stage, single-ended, current-feedback cascode LNA prototype is realized in 90nm CMOS. Physical implementation with multiple magnetic components, signal integrity associated with current return path, and circuit simulations employing an S-parameter model are addressed and emphasized in the LNA development. Consuming just 3mW from a 1V supply, the LNA achieves 14.5dB peak power gain, a –3dB gain bandwidth of 5.0GHz. The noise figure varies from 4.9dB to 5.6dB across a 22GHz and 26GHz RF bandwidth, and the IIP_3 is –6.0dBm.

The frequency downconverter is realized by integrating the inductive-tuned VCO and current-feedback LNA with a differential Gilbert-type mixer. Isolation of the LNA single-ended current return path from the rest of the receiver is maintained by a 8-port transformer balun preceding the mixer. This receiver RF front-end draws 10.7mW from a 1.0V supply, and delivers 12.6dB peak power gain, –3dB bandwidth of 1.25GHz. The noise figure varies from 10.6dB to 11.5dB across the RF bandwidth, and the IIP_3 of the downconverter is –12.1dBm.

Samenvatting

Dit proefschrift onderzoekt het systeemontwerp en de circuitimplementatie van een 24GHz-band radarontvanger voor korte afstand detectie in CMOS technologie. Door gebruik te maken van de propagatie- en penetratie eigenschappen van EM golven is het namelijk mogelijk om stilstaande of bewegende objecten (zelfs achter een muur) op afstand te detecteren of te visualiseren. De mogelijkheid om deze radar systemen te kunnen realiseren in zeer compacte afmetingen, kan hun commercialisatie versnellen en nieuwe product mogelijkheden introduceren. Door het stroomverbruik te minimaliseren tot 15mW, kan een ontvanger 4 uur lang continue operationeel zijn met slechts een 1,2 gram lithium knoopcel batterij als energiebron. Het gebruik van CMOS technologie maakt het mogelijk om zowel de RF zendontvanger als basisbandprocessor in een enkele chip te implementeren.

Om zo'n radar systeem te optimaliseren, is het essentieel om de functionele eisen te begrijpen. Om bijvoorbeeld het energieverbruik tot 15mW te beperken kan gebruik worden gemaakt van het continue karakter van het FMCW radar concept. Hiermee kan de eis voor een energie verslindende hoogvermogen zendversterker worden ondervangen. Verder heeft een FMCW radar voor de korte afstand ook het voordeel dat men gebruik kan maken van de faseruiscorrelatie tussen de zend- en ontvangstgolf; hierdoor kunnen de eisen en dus ook het energieverbruik van de LO signaal generatie worden verlaagd. De keuze voor een heterodyne ontvanger architectuur vermindert ook detectiefouten die t.g.v. tweede-orde intermodulatie effecten veroorzaakt kunnen worden door interfererende radarzenders in de omgeving. Ook frequentie "pulling" van de zeer breedbandige oscillator kan beter worden tegengegaan waardoor de nauwkeurigheid verbeterd. Verder wordt in een heterodyne systeem de invloed van flikkerruis van de CMOS transistors beperkt wat de signaalkwaliteit ten goede komt. Het iets hogere energieverbruik en de compliciteit van een heterodyne ontvanger kunnen worden ondervangen door een optimale frequentieplanning en de eliminatie van het "image-reject" filter, dit is mogelijk door gebruik te maken van de frequentie "chirp" eigenschappen van het FMCW signaal.

De frequentieomzetting in de radarontvanger is gerealiseerd door het integreren van de LNA, een Gilbert-mixer en een VCO die opereert op de werkfrequentie. Een varactor-vrije frequentieverstemming is toegepast in de VCO om de traditionele compromissen tussen verstembaarheid, kwaliteitsfactor en werkfrequentie te ondervangen in CMOS gebaseerde ontwerpen. De toegepaste "inductieve" frequentieverstemming wordt mogelijk door gebruik te maken van een resonerende transformator tank die de 90° fasedraaiing tussen de ingang/uitgang spanning van de "transconductor-cell" aansluitingen benut. In deze configuratie kan de resonantiefrequentie worden geregeld d.m.v. het teken en de grootte van de transconductantie. M.b.v. deze configuratie kan de VCO continue worden veranderd door het aanpassen van de DC-stroom van de "transconductor-cell". Aanpassingen in frequentie verstemmingsbereik en stroomverbruik zijn mogelijk. Twee VCO testcircuits

worden beschreven in dit proefschrift, namelijk: (1) Een demonstratie circuit t.b.v. het aantonen van het concept in 0,13µm RF-CMOS, welke 43mW verbruikt van een 1,2V voeding. Het frequentiebereik van dit circuit is 23,2GHz tot 29,4GHz (23,6% relatieve bandbreedte) met een faseruis van –92,6dBc/Hz bij 1MHz frequentie-offset. (2) Een geminiaturiseerd prototype van de radarontvanger geïmplementeerd in 90nm CMOS. Dit circuit verbruikt 5,7mW van een 1,0V voeding. Het maximale frequentiebereik is 18,6GHz tot 21,2GHz (13,1% relatieve bandbreedte) met een faseruis van –82,0dBc/Hz bij 1MHz frequentie-offset.

Het gebruik van een CMOS LNA in het inversiegebied, in combinatie met een werkfrequentie die de limiet van de transistor benadert, verslechtert de haalbare vermogensversterking en ruis. Een twee-stap LNA optimalisatie-algoritme is voorgesteld in dit proefschrift waarin rekening wordt gehouden met zowel de transistors als de feitelijke circuitimplementatie. In deze aanpak worden transistor afmetingen en stoom ingesteld voor een optimale vermogensversterking, ruisgetal, lineariteit en bandbreedte, terwijl de benodigde matchingnetwerken worden beperkt voor hun verliezen. Het verdelen van het beperkte vermogensbudget over meerdere versterkingstrappen helpt om de totale vermogensversterking te verhogen. Het optimaliseren van de interactie van de transistor met de bilaterale energiestromen in een meertrapsversterker wordt vergemakkelijkt door een Smith chart gebaseerd visualisatie en computer-aided ontwerpmethode. De voordelen van deze techniek worden aangetoond door ontwerpvoorbeelden.

Stroomterugkoppeling d.m.v. een 3-poort transformator in een cascode LNA is in dit proefschrift geïntroduceerd om de vermogensversterking te verhogen en het ruisgetal te verbeteren onder klein-signaal condities. Deze terugkoppeling wijzigt de interne relatie tussen de ingangsspanning en -stroom ruisbronnen van een "common-gate" MOS transistor. Hiermee kan aan de impedantie condities in de cascode LNA worden voldaan voor optimale vermogen en ruis matching. Een twee-traps stroomgekoppeld cascode LNA prototype is gerealiseerd in 90nm CMOS. De fysieke implementatie van de LNA met meerdere magnetische componenten, de bijbehorende signaalintegriteit ten aanzien van het stroomretourpad en circuit simulaties welke gebruik maken van een S-parameter modellen worden belicht en bediscussieerd. Met een energieverbruik van slechts 3mW in combinatie met 1V voeding behaalt deze LNA 14,5dB vermogensversterking bij een –3dB bandbreedte van 5,0GHz. Het ruisgetal varieert van 4,9dB tot 5,6dB over de 22GHz tot 26GHz RF-band en de bijbehorende IIP3 is –6,0dBm.

De frequentieomzetting is gerealiseerd door integratie van de verstelbare-inductie VCO en stroom-teruggekoppelde LNA in combinatie met een differentiële Gilbert-cel mixer. De isolatie van de (single-ended) LNA retourstroom met de rest van de ontvanger wordt gehandhaafd door het plaatsen van een 8-poort transformator balun voor de mixer. Deze RF ontvanger verbruikt 10,7mW uit een 1,0V voeding, en levert 12,6dB vermogensversterking bij een –3dB bandbreedte van

1,25GHz. Het ruisgetal varieert van 10,6dB tot 11,5dB over de RF bandbreedte, met een IIP3 van –12,1dBm.

Chapter 1

Introduction

The discovery of electromagnetic waves and their properties in the late 19th century led to the development of radio detection and ranging (RADAR) technology. The first radar-like apparatus was demonstrated in the Rotterdam harbour of the Netherlands in 1904 [1.1]. It was designed to detect the presence of distant objects on ships for collision avoidance using a spark-gap transmitter, however, it was incapable of providing range information. The first radar for aircraft detection was made practical in Britain in 1935 [1.2] after the invention of the cavity magnetron source [1.3]. Global development of military radar systems evolved rapidly during the Second World War [1.4]. These high-power, pulse-type radars were used to track aircraft and ballistic missiles. Commercialization of the radar technique happened in the post-war era, where it found widespread application in air traffic control [1.5], marine navigation [1.6], weather forecasting [1.7], geological research [1.8], and ground vehicle speed monitoring [1.9]. Advances in integrated circuit and semiconductor device technologies are now enabling the development of low-cost radar products for the automotive [1.10], industrial [1.11] and consumer electronics [1.12] markets. CMOS technologies feature superior mixed-signal integration capability [1.13] and low implementation cost in high volume production due to the planar manufacturing processes [1.14]. This has stimulated miniaturization of commercial radar devices into a small form factor suitable for use in an automobile or for handheld applications using silicon IC technology, and the opportunity to reduce the bill of materials (BoM) cost of the radar products simultaneously through the use of silicon CMOS.

Radar detects remote object by transmitting an electromagnetic (EM) wave towards the target and sensing the reflected waveform, or the “echo” signal. Figure 1.1 illustrates the radar operation with transmitted and received frequency spectra. The time of flight is calculated by recognizing the delay time and frequency difference between the transmitted and echo signals, and the range and relative velocity of distant objects can be detected subsequently.

The purpose of this thesis is to investigate the feasibility of implementing a 24GHz-band short-range radar (SRR) receiver in CMOS technology for the automotive, industrial and consumer electronics market with power consumption in the 15mW range. This enables 4 hours of continuous operation from a button sized lithium battery with a weight of 1.2 grams and energy capacity of 60mAh [1.15].

Factors that determine detection accuracy include the transmit frequency

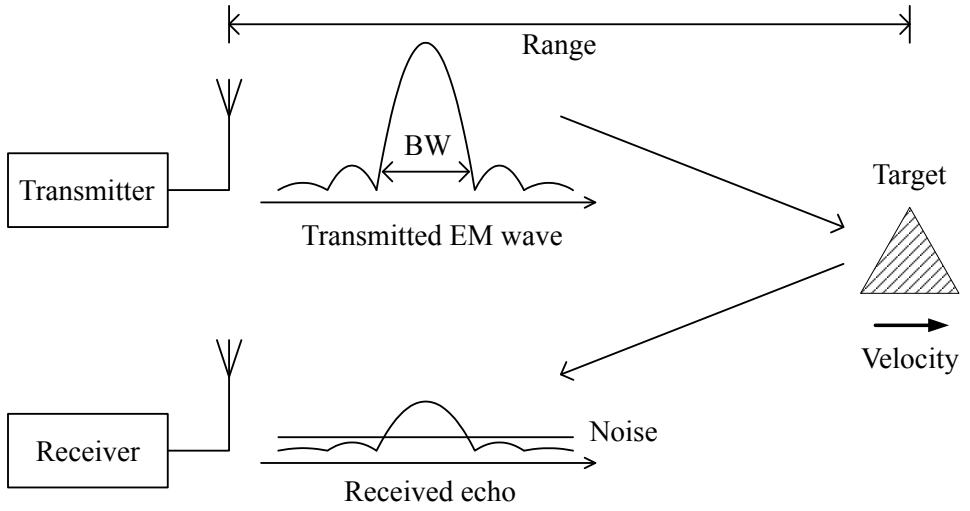

Figure 1.1 Radar operation with transmitted and received frequency spectra

bandwidth and receiver sensitivity. The minimum resolvable range, or range resolution (ΔR) in radar terminology, is inversely proportional to the bandwidth of the transmitted wave (BW) [1.16]. It is expressed as

$$\Delta R = \frac{c}{(2 \cdot BW)}, \tag{1.1}$$

where c is the speed of light. From Eqt. (1.1), the occupied bandwidth requirement on the transmitter and receiver is as wide as 3GHz for a SRR resolution of 5cm.

Selection of the radar frequency band is a trade-off between the fractional bandwidth occupied by the Tx signal and the limits of the technology used. Most commercial usage of the radio spectrum at present is concentrated at frequencies below 10GHz [1.17]. For example, the global system for mobile communication (GSM) occupies frequency bands at 850MHz, 900MHz, 1.8GHz, and 1.9GHz [1.18], and the IEEE-802.11 wireless LAN protocols operate in the 2.4GHz and 5GHz bands [1.19]. Operating in a higher frequency range avoids overcrowding the valuable bands used for mobile and wireless data communications, and relaxes the circuit requirements [1.20] by minimizing the fractional bandwidth as defined by [1.21]

$$\text{fractional bandwidth} = \frac{\text{3dB bandwidth}}{\text{center frequency}}. \tag{1.2}$$

On the other hand, the upper frequency range is limited by the availability of suitable electronic technology for hardware implementation, because performance from active and passive devices always declines with increasing frequency. The 5GHz spectrum at the 24GHz band available from North America and Europe for SRR applications is a good compromise between these factors [1.22].

The choice of this center frequency also favours a smaller antenna because the physical dimensions of an antenna are inversely proportional to the operating

frequency. The wideband circular disc monopole antenna in [1.23] realizes >10dB return loss from 2.5GHz to 55GHz with a disc diameter about one-quarter of the signal wavelength of the first resonant frequency at 3GHz. For the 24GHz SRR, the antenna dimension is further reduced because the lower-end of the frequency range is much greater, at around 22.5GHz.

Regulatory authorities across North America [1.24] and Europe [1.25] allocate certain frequency bands for radar sensing and regulate the maximum radiated power level. The transmitted power experiences two times the free space path loss as it travels from the antenna to the target and back again, as illustrated in Figure 1.1. From Friis' equation [1.26], this loss is given by

$$\text{radar path loss} = \frac{\text{received power}}{\text{transmitted power}} = \frac{1}{(4\pi)^3} \cdot \frac{c^2}{f^2 R^4} \cdot (\sigma \cdot G_r \cdot G_t), \qquad (1.3)$$

where c is the speed of light, f is the signal frequency, R is the target range, σ is the radar cross section of the target, and G_r and G_t are the receiver and transmitter antenna gains, respectively. Assuming that $\sigma = 1\text{m}^2$ and $G_r = G_t = 10\text{dB}$, the radar path loss equals 91dB for a 10m range at 24GHz.

The received echo is accompanied by the thermal noise due to the receiving antenna radiation resistance [1.26]. This noise power has a constant power spectral density over frequency as depicted in Figure 1.1, and its integrated power (P_n) across the signal bandwidth (BW) is given by

$$P_n = k \cdot T \cdot BW, \qquad (1.4)$$

where k and T are Boltzmann's constant and absolute temperature, respectively. P_n equals –79.0dBm for the 3GHz occupied bandwidth at 300K (room temperature). With 0dBm transmit power, the signal-to-noise ratio (SNR) of the echo signal at the receiver input is as low as $(0\text{dBm} - 91\text{dB}) - (-79\text{dBm}) = -12\text{dB}$.

Figure 1.2 illustrates the proposed block diagram for the SRR receiver. The echo signal is first picked up by a receiver antenna and is passed through a band

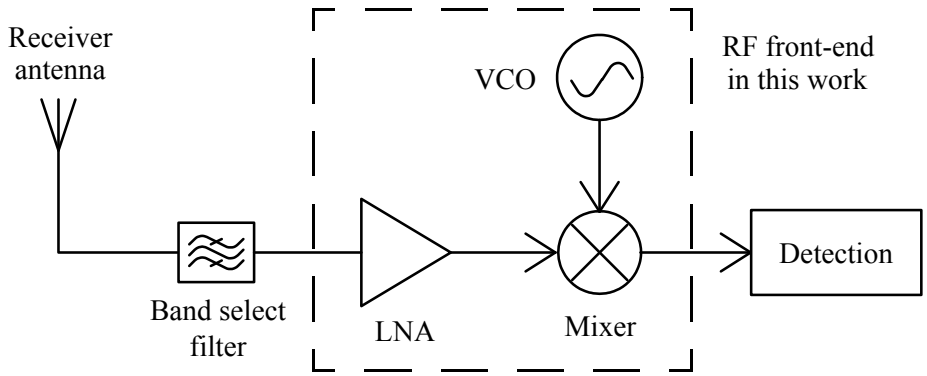

Figure 1.2 Block diagram of a SRR receiver

select filter. Its power level is then scaled up by a low-noise amplifier (LNA) and is subsequently frequency downconverted by the mixer and voltage-controlled oscillator (VCO) prior to a detection circuit block at IF. The designs reported in this thesis cover the implementation and optimization of the wideband signal generation, low-noise amplification and subsequent frequency downconversion, which are integrated into a low-power radar receiver RF front-end.

The LNA is necessary at the receiver to scale up the tiny echo power while adding as little noise as possible in order to maintain the fidelity of the target information. The detection circuit could be implemented in the digital domain [1.27]. The downconversion mixer together with the wideband VCO translates the frequency of the received echo power to an IF prior to digitization by an analog-to-digital converter (ADC). This relaxes the sampling bandwidth requirement on the ADC [1.28].

The designs proposed in this thesis exploit the high frequency capability of advanced nanometer-scaled CMOS technology together with the utilization of on-chip magnetic components to lower power consumption and realize wideband performance specifications. The processing yield and system integration capability of CMOS technology has the potential for realization of both the RF transceiver and baseband processor in a single chip. The LNA gain and noise performance are optimized at low-power dissipation by power gain and noise matching among cascaded amplifying stages. A wideband VCO implemented without any extra-cost technology options is realized by a transconductance frequency tuning scheme that does not use a varactor. Adaptive performance tuning is possible by trading-off power consumption and the frequency tuning range. The mixer is implemented with the Gilbert double-balanced mixer configuration, and an integrated balun couples the differential mixer input to the single-ended LNA output. The measured silicon prototype verifies that these components satisfy the SRR receiver specifications proposed in the system study of this thesis.

1.1 Motivation

The propagation and penetration properties of EM waves offer the possibility of non-contact based remote sensing [1.29] and through-the-wall imaging [1.30] of stationary or moving objects at a distance. The feasibility of realizing these concepts in hardware with a small form factor could accelerate their commercialization with widespread acceptance.

1.1.1 Advantages of Radio Ranging

Alternative technologies exist for the remote detection of objects, including passive-type video-based imaging, and infrared [1.31] or ultrasonic sensing [1.32]. Passive sensors are inherently safe and pose no risk in industrial applications because there is no signal emission in the detection process. They are not subject to government

regulations regarding interference, coexistence or compliance. Ultrasonic sensors are similar to radar in that distance to a target is calculated from interpretation of an echo signal, but at a lower transmitted frequency (e.g., around 18kHz) [1.32]. The signal processing requirements are thus much less demanding with lower BoM cost and power consumption. However, various performance aspects make radio ranging superior to other techniques.

The penetration of millimeter wavelength radio waves [1.33] compared to visible light or ultrasonic waves enables the radar to be mounted behind the vehicle body in automotive applications, or inside the case for most non-metallic handheld products. This is an important factor that promotes the widespread acceptance and market value of a radar sensor for consumers by offering a stylistic advantage in product appearance. This penetration property also gives radar immunity to inclement weather conditions such as rain, fog, high humidity, and heavy dust [1.34].

Signal attenuation due to atmospheric absorption is also the lowest for microwave propagation compared to non-radio frequency bands. During fog condition with visibility of about 1km, [1.35] compares the attenuation of visible light and a 94GHz carrier and they are measured 16dB/km and 2dB/km, respectively. At sea level, lowering the carrier frequency from 94GHz to 24GHz further reduces the atmospheric absorption by about 0.25dB/km [1.36]. Radar sensors therefore have excellent performance for the maximum detectable range among different sensing techniques. Compared to a video-based imaging sensor, their functionality is also not influenced by the time of day or night, or by poor lighting in an indoor environment.

Radar range resolution is inversely proportional to the signal bandwidth [1.16], and millimeter range resolution can be easily achieved by an ultra-wide transmit bandwidth (UWB). The Doppler shift [1.37] introduced by the velocity of both fast and slow moving targets are more resolvable in radar sensing because EM waves travels with the speed of light rather than at the speed of sound.

1.1.2 Potential Markets

The cost reduction of radar implementation could initiate emerging opportunities in different markets. One potential mass-market application is automotive collision avoidance radar, which is intended to increase road traffic safety and lower the number of road accidents. Studies estimate that 95% of road accidents result from human errors [1.38], and that most collisions could be prevented if an additional 2.3 seconds of reaction time were available to the driver [1.39]. One vision for the future is to develop an array of technologies to warn the driver prior before a possible collision, and exercise pre-crash preparations such as airbag launch, pre-tensioning seat belts, etc., if a collision is unavoidable. Short-range radar in an automotive application favors a hybrid array of radar units installed around the vehicle for different functions [1.38]. Potential applications include rear and front collision warning, to pre-crash airbag launch, parking aids, and blind spot detection [1.40]. These

sensors could reduce the number of fatalities, injuries, damage to property, and economic losses to the society. The European Union permits the use of 24-GHz band sensors for the automotive SRR until January 1st 2022 [1.41]. Nevertheless, the technologies developed in this thesis are applicable to other frequency bands as well.

Radar sensors currently available in the industrial sector offer a broad range of measurement capabilities [1.42], but in a bulky form factor with an approximate weight of 6.1kg and starting at a cost of US$3,381 (quoted in April 2015) per unit [1.43]. Industrial automation could be developed further with the penetration of low-cost microwave radar. Non-contact measurements of the existence, distance or velocity of solid or liquid materials is beneficial to the optimization of the cost of production and increased throughput, robustness and quality. This is applicable to either food or pharmaceutical plants in controlled conditions, or chemical or construction sites with high temperature, high pressure, or extremely dusty environments.

Tools exist that estimate the range of objects with known dimensions using video-based cameras, but their accuracy is poor [1.44]. Radar distance measurement of a stationary target demands less signal processing power for the calculation algorithms with simple hardware while maintaining accuracy. This opens-up an opportunity for handheld wireless ranging for length measurements (e.g., an electronic tape measure) or something similar if the RF circuitry for the radar could also be implemented at minimal cost. Embedding radar devices in smartphones or wearable electronic watches or glasses may make the “X-ray glasses” advertised widely in 20th century comic books a potential reality.

1.1.3 Advantages of CMOS Implementation

The continuous scaling of CMOS transistor feature sizes according to Moore's law has strengthened digital computing power and increased data throughput. The technological advantages of digital signal processing are further solidified by the advancement of automated CAD tools for logic synthesis, place-and-route, and functional verification. With the ever decreasing power consumption of digital processors, the advantage of using digitally assisted analog techniques [1.45] to enhance performance of analog and RF circuitry becomes attractive because of its potential for reconfigurability [1.46], scalability across technology nodes, and shortened design time with automated CAD tools.

A 24GHz SRR transceiver can benefit from the evolution of digital computation capability. For example, carrier leakage in the RF transmitter can be suppressed by applying digital compensation algorithms, similar to the off-chip FPGA platform implemented in [1.47]. Linearization of the transmitted modulated carrier by dithering the VCO tuning port via a digital-to-analog converter is demonstrated in [1.48]. Automatic gain control in the RF receiver can be accomplished by adapt-

ing the bias current via digital switches [1.49], with the analog gain steps being compensated in the digital baseband [1.50]. Correction of the analog impairments in the digital backend after the A/D conversion is also possible, such as improvements to the amplitude and phase errors of a radar receiver's IF quadrature signal path [1.51], or the linearity of a pipelined ADC [1.52].

The projection of an increase in silicon wafer diameters from the current state-of-the-art of 300mm to the 450mm, which is expected for mass production in 2017 [1.53] will continuously lower the cost per unit silicon die area for a given technology node.

1.2 Design Challenges

The quality and accuracy of a radar sensor does not only depend on the electrical performance of each building block, but also on the interaction of almost everything involved within the transceiver link [1.54]. This covers the fields of communication theory, wireless standardization, microwave and analog/RF circuit design, and digital signal processing. This thesis investigates the system and circuit design of a low-power, low-cost 24GHz UWB SRR radio receiver, and the challenges of designing and implementing the analog/RF front-end in CMOS technology. Implementation-level considerations are emphasized with respect to passive components integration, performance, and power dissipation. The outcomes of this study could enable other new opportunities radar systems.

1.2.1 Radar Hardware Implementation

Radar used to be an expensive technology with applications limited to air defense, air traffic control or weather forecasting due to the hardware implementation cost. The RF transceiver in a radar usually consists of discrete microwave components such as waveguides, power dividers, isolators, circulators, directional and hybrid couplers, etc. [1.55]. Signal generation, amplification, and frequency translation are feasible with planar monolithic microwave integrated circuit (MMIC) implemented in compound semiconductor technologies [1.56]. Production yield and reliability problems for these circuits limit them to only small-scale integration [1.57], and precision analog and low-power digital are not feasible in these MMICs. Furthermore, monolithic integration of digital switches, power control, voltage regulators, etc., is not possible. The state-of-the-art maximum wafer diameter available in the industry is 150 mm [1.58] which is one-half to one-third the current silicon wafer size used in CMOS production. The computational demands at baseband frequency for either time-gating for pulse-type radar or fast Fourier transform (FFT) signal processor for continuous-type radar could only be satisfied with the employment of a hybrid implementation approach with different semiconductor technologies for the RF and baseband circuitries. Additional regulations and licensing requirements exist for radar applications which govern the frequency band and power emission levels [1.24,1.25]. These factors contribute to the high cost of the radar equipment

realization in the past.

Consumers favor low-cost, low-power products, but also sophisticated functionality. They also demand high performance. The widespread acceptance of radio ranging in the automotive, industrial and consumer electronics markets can be gained only after economical devices become available satisfying the required performance for a particular application. System-on-chip (SoC) integration of the RF radar front-end with data converter, power management, and digital baseband processor in low-cost CMOS technology could offer a possible solution for high-volume applications.

1.2.2 Disadvantages of CMOS Implementation

The performance of CMOS transistors can be quantified by the maximum available gain (MAG). It is plotted in Figure 1.3 together with the forward transmission coefficient ($|S_{21}|$) for an NMOS transistor in 90nm technology having a 1μm finger width, for varying drain current density at a fixed 0.6V drain-source voltage. Both of these gain parameters increase with the bias current in the saturation region but there is a significant gap between the MAG and $|S_{21}|$. This difference arises from the need for passive matching networks which transform the 50Ω source/load resistances to a higher impedance level. These networks resonate out the transistor's parasitic capacitance to realize higher gain. For a constant gain-bandwidth product available from the transistor, adding a narrowband matching network with high quality factor (Q) reduces the circuit bandwidth. This bandwidth narrowing is accentuated in a cascade of independent narrowband amplifier stages.

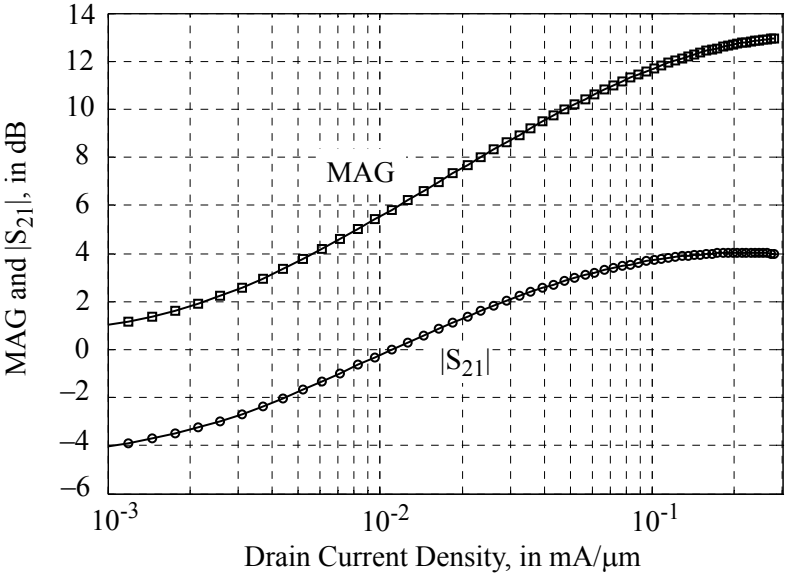

Figure 1.3 Simulated maximum available gain and forward transmission coefficient of an NMOS transistor at 24GHz

The overall RF bandwidth and gain flatness are sensitive to temperature drift and parameter variations of the matching networks. Therefore, careful and precise modelling of the passive networks becomes essential to prevent the measured data deviating from the simulated predictions.

1.2.3 Low-Voltage, Low-Power Implementation

Lowering the circuit supply voltage has the benefit of minimizing the power dissipation for a given bias current. This could maximize battery lifetime, or allow the usage of a coin cell battery with minimal size and weight. This is a critical factor for the realization of portable devices, and in particular integrating the SRR into wearable consumer electronics products such as watches or glasses.

The low-voltage requirement excludes the optimum operation of certain high performance circuit topologies for signal amplification and signal generation, such as the cascode amplifier or Colpitts oscillator. The 90nm CMOS technology utilized in this work concurrently set the nominal operating supply at 1.0V [1.59]. Minimizing the bias current in active devices without compromising performance is another important design objective to be satisfied.

CMOS transistor noise figure and gain parameters are proportional to the drain bias current density. Biasing a transistor at low current constrains the performance available from a single amplifier stage. The cascade of multiple gain stages is therefore usually necessary in order to fulfill system requirements. With each amplifier loaded by a single LC resonant tank, the number of on-chip coils grows with the number of stages. Hence, the layout floorplan with multiple passive components that consumes minimal chip area becomes a critical part of the design process.

The finite reverse isolation of an amplifier without the voltage headroom for a cascode stage must also be addressed in the optimization routine. The selections of amplifier input and output resonant networks for impedance and gain matching are dependent on each other, and the co-design of both active and passive components becomes critical in the optimization process.

1.2.4 Millimeter-Wave Wideband Frequency Generation

VCOs have typically used a voltage-controlled capacitor (i.e., varactor) to electrically control the resonant frequency of an LC tank, thereby allowing electronic tuning of the oscillation frequency. In contrast to operation below 10GHz, where inductor Q dominates losses in the on-chip tank, a varactor implemented in production VLSI technologies (silicon CMOS or SiGe BiCMOS) tends to dominate resonant tank losses at millimeter-wave (mm-wave) frequencies (i.e., above 12.5GHz on a silicon chip). Since the equivalent tank loss is proportional to the inductance to capacitance (L/C) ratio, only a relatively small capacitance can be used if high spectral purity is required from the VCO. In addition, there is a trade-off between the varactor Q and capacitance tunability as its bias voltage varies from maximum to

minimum (i.e., C_{max}/C_{min}). The C_{max}/C_{min} ratio is typically less than three at mm-wave frequencies. Also, parasitic capacitances of the transistors and the tank inductor limit the portion of the total tank capacitance that can be tuned electrically. These three factors: limited total capacitance, available capacitance ratio, and circuit parasitics, restrict the tuning range of a conventional LC VCO to less than 10% at approximately 20GHz [1.60,1.61] and less than 5% at 60GHz [1.62-1.64].

VCOs with 25% tuning range have been implemented using supply and tuning voltage magnitudes at, or above 3V in SiGe BiCMOS (–5.6V and 4.5V in [1.65], –5.5V and 3.0V in [1.66]) when a collector-base junction is used as a varactor diode [1.65], or in technologies featuring processing options for the varactor devices [1.66]. Also, VCOs implemented in silicon-on-insulator (SOI) CMOS technologies, where the parasitic capacitance for both active and passive devices is lower than in bulk CMOS, have demonstrated tunability over a wide frequency range [1.67-1.69]. However, non-standard and/or dual supply voltages increase system and component costs. Extra-cost processing options for the varactor, or implementation in SOI-CMOS adds to the BoM of an integrated circuit, and are not a favorable choice for a low-cost radar implementation.

As to be explained in Chapter 3 of this thesis, a wideband, frequency-agile, and continuously-tunable VCO is an essential element of frequency-chirping continuous-type radar with low power consumption. The techniques of multi-band VCO by switchable capacitor arrays [1.70] or a multi-mode resonant tank [1.71] in order to achieve high frequency tuning range are inapplicable to the low-power radar implementation because of their discrete and discontinuous frequency tuning curves across the radar bandwidth.

1.2.5 On-Chip Magnetic Components

In CMOS technology, magnetic components such as inductors and transformers are implemented by the interconnection of planar coils separated from the substrate by oxide layers. The quality factor of these components is limited by the substrate loss due to electric coupling to the semiconducting silicon substrate and the ohmic losses from metal strips and via interconnections [1.72]. Newer CMOS technology nodes come with an increased number of metal layers in order to cope with the routing congestion in modern ULSI system [1.73]. This increases the oxide thickness underneath the magnetic components and lowers the substrate loss due to electric coupling. On the other hand, the metal thickness scales down together with the active device minimum feature size to favour digital circuit performance by increasing the logic gates layout density and lowering power dissipation caused by the dynamic switching of current. This increases the ohmic loss and the degradation is further magnified by the finite skin depth at the mm-wave frequencies. Stacking multiple metal layers [1.74] lowers the ohmic loss at the cost of higher substrate coupling between metal layers in the stack close to the silicon substrate. Iterative EM simulations are unavoidable when optimizing the coil dimensions for a desired inductance

value and operating frequency range.

The use of multiple magnetic coils is necessary for the implementation of matching networks, a multi-stage LNA, mixer, and LO generation circuits targeting low power dissipation at mm-wave frequencies. EM coupling between these coils must be captured in simulation to prevent shifting of the resonant frequency in an individual LC tank, or potential stability problems caused by parasitic positive feedback loops. Traditional lumped RLC or S-parameter models for individual coils are inadequate to characterize a complex multiple-coil structure, and a new modelling and simulation strategy is necessary for accurate prediction of performance.

1.3 Thesis Organization

This thesis is organized as follows. Chapter 2 lays out the theoretical framework for the design and optimization of a CMOS wireless receiver. It presents the analog impairments in receiver design with physical parameters such as noise, non-linear distortion, and phase noise, as well as definitions and comparisons of different gain parameters in a design of cascaded stages.

The principle of operation for FMCW radar is presented in Chapter 3, along with radar receiver design and link budget considerations. A proposed architecture for a prototype 24GHz-band SRR receiver, as well as a design example with emphasis on the demonstration of a SRR in CMOS technology is also described.

Chapter 4 presents a review of different frequency tuning techniques in CMOS technology, and proposes a new continuous-tuned differential VCO that does not require an on-chip varactor for frequency tuning. The operation principle and adaptability between frequency tuning and power consumption are discussed along with simulation and measurement data for two silicon prototypes.

Chapter 5 discusses the fundamental aspects of LNA design and optimization, and presents a new and efficient Smith chart based bilateral methodology for the design and optimization of a low-voltage, low-power CMOS LNA. Design examples are given to demonstrate the advantages of the proposed optimization algorithm on cascade of (non-cascode) stages with finite reverse isolation.

Chapter 6 continues with a 24GHz LNA prototype operating from a 1.0V supply which consumes 3mW. It conquers the supply voltage limitation and non-optimal power gain and noise matching among the amplifier stages of a cascode amplifier by biasing the transistors in moderate inversion region and applying transformer feedback in the common-gate gain block, respectively. The single-ended-to-balanced interfacing between the LNA and mixer, and design of the downconversion mixer are also detailed. Design and layout techniques for the circuits considering operation at mm-wave frequencies are immediately followed by simulation and measurement data of a frequency downconverter, which implements the front-end of a 24GHz SRR receiver.

This thesis is concluded in Chapter 7 with a brief summary, a list of research contributions, and suggestions for future work.

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Chapter 2

Background Information

This chapter lays out the theoretical framework for the radar receiver architecture, wide-band VCO and LNA developments in this thesis. Quantitative descriptions of the analog impairments in receiver design by noise and non-linear distortion for a single-stage amplifier are first presented. These are followed by definitions and comparisons of gain parameters, and a review of the design equations for cascaded stages. Finally, the concept of phase noise, and its detrimental effect on the down-converted receive signal quality are examined.

2.1 Analog Impairments in a Receiver

Electrical implementation of a practical radar suffers from imperfections which deteriorate the detection accuracy. In this section, the concepts of noise and non-linear distortion, and their implications for the received signal quality are described.

2.1.1 Noise

Noise limits the sensitivity of a radio receiver. The most common form of noise is thermal noise, which is a consequence of the Brownian (random) motion of electrons [2.1]. Conductor metals, resistors, the (inverted) channel and gate contacts to a MOS transistor, and the antenna radiation resistance are all sources of thermal noise. This noise is proportional to absolute temperature and the bandwidth of interested, and has a flat power spectral density (PSD), that is, it is independent of frequency. The power available from the noisy element is

$$P_{\text{available}} = k \cdot T \cdot BW \quad , \tag{2.1}$$

where k is Boltzmann's constant, T is absolute temperature, and BW is the measured bandwidth.

The second type of noise arises from the random fluctuation of electron flow [2.2]. This includes the shot noise observable in a bipolar transistor when an electron travels through the potential barrier across a PN junction, and flicker noise, where electron flow is disturbed by the trapping and releasing of charge. The MOS transistor is a surface-controlled device where current flows immediately below the gate oxide. Interface states and defects in the oxide introduce plenty of opportunities for charge trapping, and therefore MOS transistors suffer more from flicker noise than bipolars. The PSD of flicker noise is given as [2.3]

$$PSD = \frac{K_f}{Area \times f} \quad , \tag{2.2}$$

where K_f is a device-specific flicker noise constant, *Area* is the surface area covered by the interface states (the channel area for a MOS transistor), and *f* is the spot frequency of interest. Because the PSD of flicker noise is inversely proportional to frequency, it is also called 1/f noise.

With each circuit element contributing noise to a circuit block, the noise power affecting a radio receiver may be represented by equivalent voltage and current noise sources at its input [2.4]. These equivalent noise sources represent all of the noise generated in the receiver, and the circuit is then considered as noiseless.

Figure 2.1 illustrates examples of a resistor and a MOS transistor. The resistor noise can be represented as a voltage source in series [see Figure 2.1(a)] or as a current noise source in parallel [see Figure 2.1(b)]. Their mean-square powers are

$$\overline{v_{in,R}^2} = 4kT \cdot R \cdot BW \tag{2.3}$$

and

$$\overline{i_{in,R}^2} = 4kT \cdot \frac{1}{R} \cdot BW\,, \tag{2.4}$$

respectively. Eqts. (2.3) and (2.4) are Thévenin and Norton equivalents, respectively, of the thermal noise power.

The equivalent voltage and current noise powers at the input of the common-source NMOS transistor amplifier are given by [2.4]

$$\overline{v_{in,MOS}^2} = \left(4kT \cdot \frac{\gamma}{g_m} + \frac{K_f}{C_{ox} WL \cdot f}\right) \cdot BW \tag{2.5}$$

and

$$\overline{i_{in,MOS}^2} = \left(\frac{4\pi/3 C_{ox} WL \cdot f}{g_m}\right)^2 \left(4kT\gamma \cdot g_m + K_f \frac{I_D^a}{f}\right) \cdot BW\,, \tag{2.6}$$

where g_m, K_f, C_{ox}, W, L, I_D, γ, and a are: transconductance, flicker noise constant,

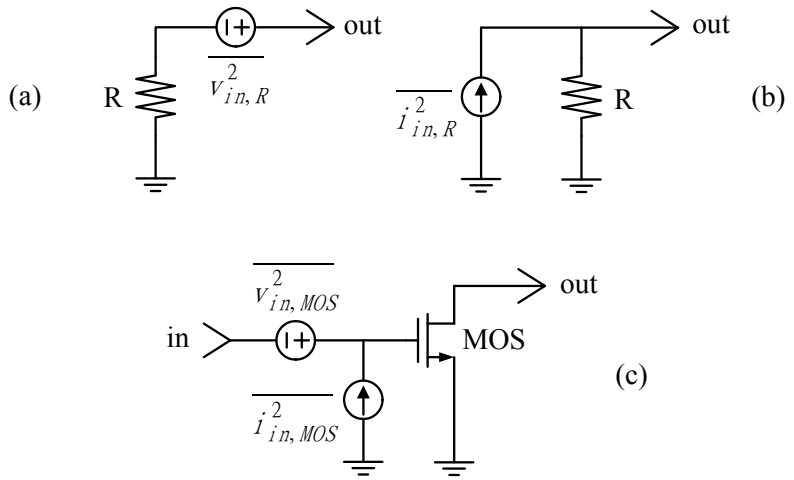

Figure 2.1 Equivalent input noise sources for a resistor [in (a) and (b)] and MOS transistor (c)

gate oxide capacitance per unit area, gate width, gate length, drain bias current, thermal noise coefficient, and constant $0.5 < a < 2$, respectively. The coefficient γ equals 2/3 for long-channel devices, and increases to a value between 2 and 3 for submicron MOS transistors [2.5]. The contribution from the MOS transistor drain current thermal noise $4kT\gamma \cdot g_m$ appears in both Eqts. (2.5) and (2.6). Therefore, these input-referred noise sources are correlated.

While the input-referred voltage and current sources generate noise power, radio receiver performance is parameterized by ratios such as signal-to-noise ratio (SNR), noise factor (F), and noise figure (NF) [2.6]. The SNR is a ratio of the signal and noise powers taken within the same bandwidth, such as the band-select filter in the front-end module, or the channel-select filter in the IF circuitry.

The received signal being processed by the radio receiver is subsequently demodulated to retrieve the desired information. Processes such as amplification, frequency translation, digitization, or digital signal processing always degrade SNR. Noise factor and noise figure are defined as

$$F = SNR_{in} / SNR_{out} \tag{2.7}$$

and

$$NF = 10 \cdot \log_{10} F . \tag{2.8}$$

The noise factor is a relative measure because it depends not only on how noisy the circuit element itself is, but also the impedance of the input source. Consider the equivalent input-referred noise model of the common-source MOS amplifier in Figure 2.1(c), with the input port connected to a source impedance (Z_{source}). If Z_{source} is zero, the noise current source at the input makes no contribution to the total output noise power. A similar observation can be made for Z_{source} approaching infinity and the input noise voltage source. An optimum source impedance (Z_{opt}) which lies between these two extremes (i.e. $0 \le Z_{opt} < \infty$) exists where the noise factor is minimized (i.e., F_{min}) [2.2].

Effects of the input-referred noise sources and source impedance on the noise factor of a two-port amplifier was analyzed in [2.7]. The noise factor is

$$F = F_{min} + \frac{4 r_n \left| \Gamma_{source} - \Gamma_{opt} \right|^2}{(1 - \left| \Gamma_{source} \right|^2) \cdot \left| 1 + \Gamma_{opt} \right|^2} , \tag{2.9}$$

where r_n is the normalized equivalent resistance of the input-referred voltage noise source, and Γ_i is the reflection coefficient of impedance Z_i. F_{min} and Γ_{opt} are functions of the input-referred voltage and current noises, and their correlation. On the complex plane of Γ_{source}, contours of different constant noise factor values are visualized as a family of circles. This is known as the noise circles of the amplifier.

The simulated noise circles of a $40 \times 1\mu m / 90nm$ NMOS common-source amplifier is illustrated in Figure 2.2. The transistor is biased at a current density of 25μA per micron of gate width by a constant drain-source voltage of 0.6V. At

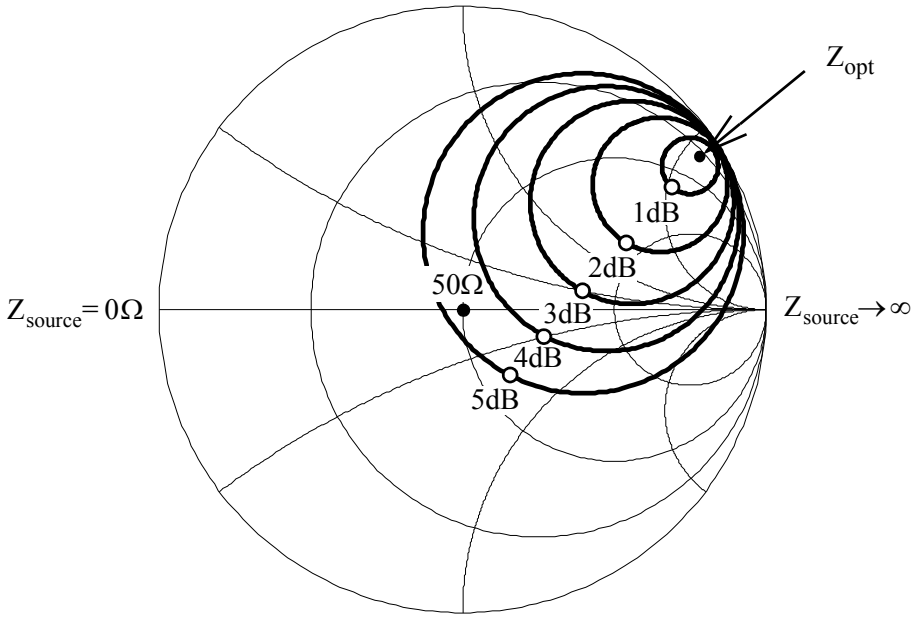

Figure 2.2 Noise figure circles plotted in the Γ_{source} plane for a 40×1μm/90nm NMOS common-source amplifier at 24GHz

24GHz, the optimum source impedance Z_{opt} is $25.5+j170\Omega$, and the minimum noise figure is 0.612dB. On the other hand, the simulated noise figure for a 50Ω source impedance is 4.67dB, which can be observed from the origin of the Γ_{source} plane in Figure 2.2 being bounded by the 4dB and 5dB noise figure circles.

Transformation of the actual source impedance to Z_{opt} minimizes the amplifier noise figure for a given power dissipation. However, the gain, bandwidth, and input return loss of the amplifier are not optimized simultaneously, in general. The degradation of noise figure by any change in the source impedance selection is visualized easily from the Smith chart. This simplifies the process of making design trade-offs involved in the optimization of a multi-stage, power-constrained LNA.

2.1.2 Non-Linear Distortion

Design of linear amplifiers using active devices is based on the assumption of a small-signal model [2.8]. For example, a MOS transistor is biased at a certain quiescent value and linear model is derived. Practical active devices have non-linear transfers, and therefore this assumption of linearity for the transistor is invalid when the input signal grows too large or is accompanied by strong interference. For example, assume that the transfer characteristic of a system can be approximated by

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t), \tag{2.10}$$

where *y(t)* is the output and *x(t)* is the input signal.

With a single sinusoid $x(t) = A_0 \cos \omega t$ applied to the input, the output is

$$y(t) = \left(a_1 A_0 + \frac{3 a_3 A_0^3}{4}\right) \cos \omega t + \frac{a_2 A_0^2}{2} \cos 2\omega t + \frac{a_3 A_0^3}{4} \cos 3\omega t + \ldots \quad , \quad (2.11)$$

which reveals that second, third, and higher harmonics of the input frequency are generated at the outputs. These tones are harmonic distortion generated by the transistor. Amplification of the input signal is characterized by the fundamental term $a_1 A_0 + 3 a_3 A_0^3 / 4$ in Eqt. (2.11). The input –1dB compression point is defined as the input signal magnitude at which the output power drops by 1dB from the ideal linear transfer value (i.e., compression). It is given by [2.9]

$$A_{0,-1\,dB} = \sqrt{0.145 \cdot \left| a_1 / a_3 \right|} \quad . \quad (2.12)$$

A weak desired signal along with a large interferer lowers the gain available from the radio receiver by driving it into gain compression. The reduction in the output signal magnitude is significant compared to the drop of the total output noise level, and the system SNR is degraded.

With two sinusoidal interference tones $x(t) = A_0 \cos \omega_1 t + A_0 \cos \omega_2 t$ injected into the input, the non-linear distortion components at the system output relevant to RF receiver design are dominated by the quadratic and cubic terms specified in Eqt. (2.11). They are

$$\begin{aligned} y(t) = {} & (3/4) \cdot a_3 A_0^3 \cdot [\cos(2\omega_1 - \omega_2) t + \cos(2\omega_2 - \omega_1) t] \\ & + a_2 A_0^2 \cos(\omega_1 - \omega_2) t + \ldots \quad . \end{aligned} \quad (2.13)$$

The first two components in Eqt. (2.13) appear in the vicinity of interferer frequencies at ω_1 and ω_2. They are proportional to the third-order non-linearity (a_3) and are commonly known as third-order intermodulation (IM_3) distortion. The input third-order intercept point is an extrapolation of the input signal level to the point where the output IM_3 equals the linear gain component at the fundamental frequency. It is given by [2.9]

$$A_{0,IP3} = \sqrt{(4/3) \cdot \left| a_1 / a_3 \right|} \quad . \quad (2.14)$$

The last term in Eqt. (2.13) is a low-frequency beat signal at the difference between the two interferer frequencies. It is the second-order intermodulation (IM_2) distortion since it is originated from the second-order non-linearity (a_2) component. The input signal level at which the output signal levels at ω_1 (or ω_2) and $\omega_1 - \omega_2$ equal each other (from an extrapolation) is defined as the input second-order intercept point. It is given by [2.9]

$$A_{0,IP2} = \sqrt{\left| a_1 / a_2 \right|} \quad . \quad (2.15)$$

The implications of IM_2 and IM_3 in a receiver system are illustrated in Figure 2.3. Two interferers with the frequency difference $\Delta\omega = \omega_1 - \omega_2$ are separated

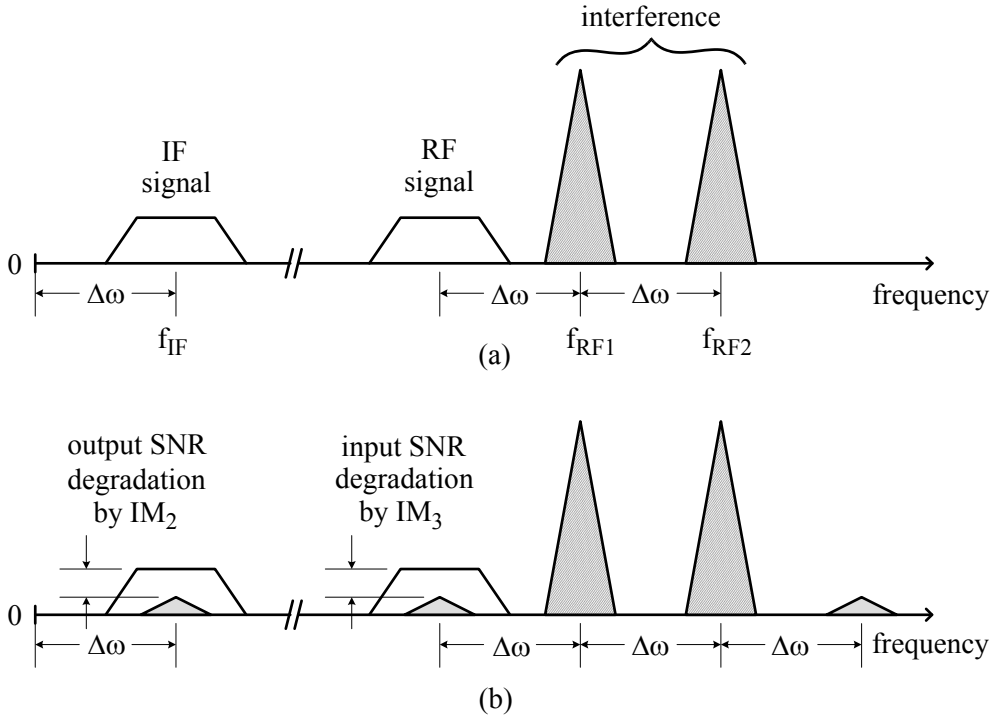

Figure 2.3 Receiver frequency diagram with two-tone interference, showing signal-to-noise ratio deterioration due to second and third-order intermodulations

from the desired RF signal by Δω. For the linear system in Figure 2.3(a), the RF signal is downconverted to the IF by a given LO signal (not shown in Figure 2.3) and the interference does not add distortion. For the non-linear system in Figure 2.3(b), the IM_3 product overlaps the desired RF signal band exactly, and increases the apparent "noise" level in the input SNR budget. Similarly, the low-frequency IM_2 product overlaps the IF signal band and degrades the output SNR. By locating the IF at a higher frequency and selecting the LO frequency appropriately, the degradation by IM_2 can be easily mitigated by high-pass filtering. For low-IF and direct-conversion receivers, IM_2 from the LNA is easily removed by AC coupling to the mixer. Therefore, IM_2 from the mixer dominates the second-order non-linear distortion.

Radio receiver non-linear distortions are seldom validated by measuring the transfer characteristic coefficients of the device-under-test (DUT) as described by Eqt. (2.10). The narrow bandwidth in typical RF circuit could attenuate any harmonic distortion components appeared in Eqt. (2.11) which fall outside the circuit passband. As a result, the measured non-linear coefficients (a_2 and a_3) appears smaller than their inherent values in the DUT. Furthermore, applying harmonic terminations in a narrowband circuit help reducing the distortion generated by the DUT [2.10]. Instead, spectral analysis at the output for a multi-tone input signal

with an increasing sweep of input power is used for characterization. Nevertheless, Eqts. (2.12), (2.14) and (2.15) reveal the importance of quiescent point selection for maximizing the a_1/a_3 and a_1/a_2 ratios in the transfer characteristic of Eqt. (2.10).

2.2 Gain Parameters

Obtaining an open or short circuit becomes more difficult with increasing frequency. The impedance of a high impedance node decreases with increasing frequency due to the parasitic capacitance from circuit elements. Similarly, the low output impedance of a voltage buffer increases with increasing frequency because of the limited gain-bandwidth product available from a feedback loop [2.11]. Therefore, in the mm-wave frequency band, voltage (current) magnitude at the circuit node (branch) of interest have to be specified with the associated impedance value.

The power strength (P_o) associated with a voltage (V_o) or current (I_o) magnitude is quantified by the relationships

$$P_o = V_o^2/R \tag{2.16}$$

or

$$P_o = I_o^2 \cdot R, \tag{2.17}$$

respectively, where R is the resistive component of the circuit node or branch impedances of interest. In the lower frequency range, a short or open circuit are realizable from the output impedance of a voltage or current amplifiers, respectively. From Eqts. (2.16) and (2.17), their associated power strength are infinite. Therefore, power strength is not a precious resource for signal in the lower frequency range.

On the other hand, amplifiers in the mm-wave band have finite input and output impedances, and therefore signal power strength at the amplifier input and output ports are limited. The bilateral power flow in a CMOS transistor could introduce stability problem for voltage amplifier in the mm-wave frequency range (to be explained in this Section). Furthermore, noise is represented in power unit and signal quality in RF circuits is parameterized by signal-to-noise power ratio. Therefore, circuit parameters quantified by power unit could benefit mm-wave amplifiers optimization with respect to gain, stability, and noise figure performance.

For a two-port gain stage as shown in Figure 2.4, there are four gain parameters relating terminal voltages v_{in} and v_{out}, and terminal currents i_{in} and i_{out} [2.12], namely: voltage, current, transconductance, and transresistance gains.

A CMOS transistor is a voltage-controlled current source, where the gate-source voltage modulates the current flow from drain-source. The voltage gain is

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{i_{out} \cdot Z_{total}}{v_{in}} = -G_m \cdot Z_{total}, \tag{2.18}$$

where G_m is the transconductance, and (in general) Z_{total} is a parallel combination of: the amplifier stage output impedance Z_{out}, the succeeding stage input impedance Z_{in2}, and the load impedance Z_{load}.

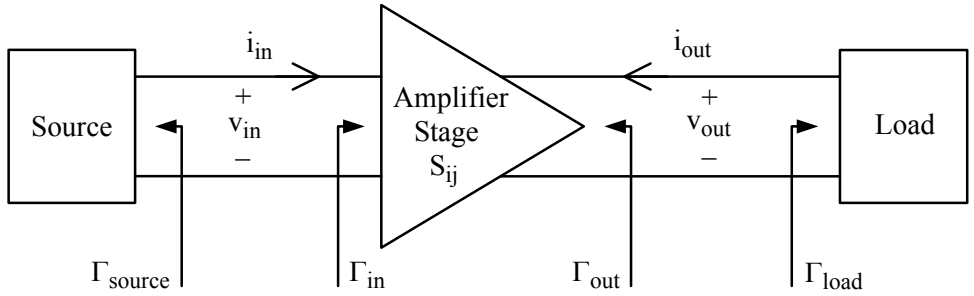

Figure 2.4 Block diagram of a two-port gain stage

A typical (lower frequency) LNA schematic is illustrated in Figure 2.5 which employs an inductor for Z_{load} in order to form a parallel resonant network with the capacitive components Z_{out} and Z_{in2} [2.13]. Assuming the inductor is modelled by a resistor R_s and inductor L_s in series, and the total shunt capacitance at the output of the first stage is C_{out}, the impedance seen at the resonant frequency is $L_s/(R_s \cdot C_{out})$. With diminishing transistor gain due to a low power budget, minimizing the capacitance value is necessary to preserve the highest possible output voltage amplitude and hence the voltage gain. This confines the dimensioning of the down-conversion mixer input devices (2nd stage) which immediately follow and capacitively load the LNA (1st stage) in a typical RF receiver.

A buffering circuit with high input, but low output impedance [2.14] could be employed between the LNA and mixer to relax the capacitive loading. However, the RF performance of a power consuming active buffer becomes poor as the operating frequency approaches the limit for a given technology, and is therefore inappropriate for low-power CMOS circuits.

With the parasitic capacitance bridging the drain and gate nodes of a FET, the input and output terminals of an amplifier are no longer isolated from each other. Figure 2.6 illustrates the simulated reverse isolation which is quantified by the $|S_{12}|$

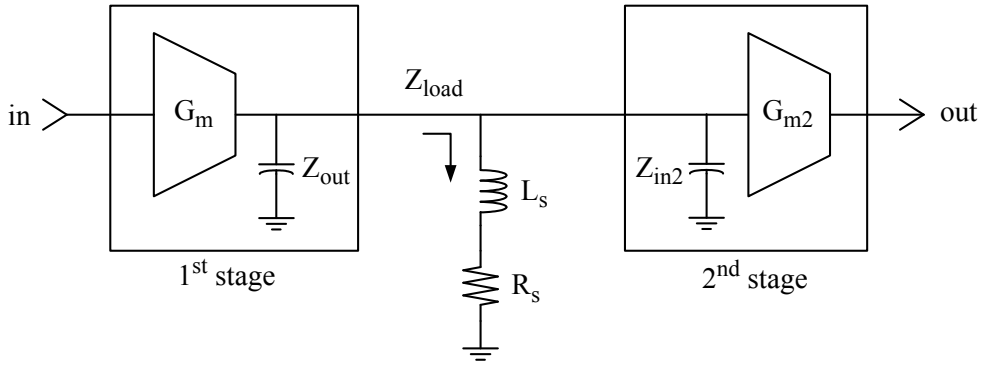

Figure 2.5 A two-stage LNA schematic with parallel resonant network

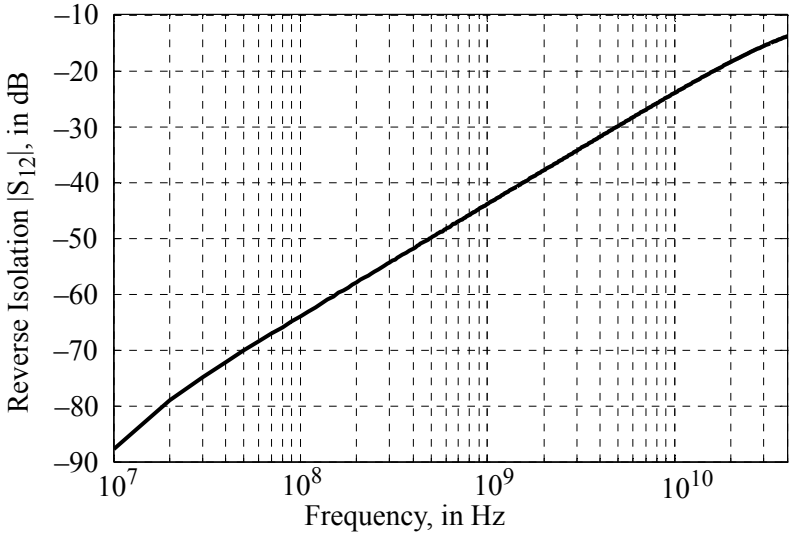

Figure 2.6 Simulated reverse isolation of a 40×1μm/90nm NMOS common-source amplifier biased at 46.8μA/μm and 0.6V drain-source voltage

of a 40×1μm/90nm NMOS common source transistor biased at 46.8μA/μm and 0.6V drain-source. With increasing operating frequency, the isolation is reduced by 26.8dB, from 43.9dB at 1GHz to 17.1dB at 24GHz. This implies that a parasitic feedback loop exists from the output toward the input. The amplifier is therefore vulnerable to oscillation if the source or load terminations are not properly controlled. With the two-port configuration shown in Figure 2.4, the effects from the finite reverse isolation can be summarized as [2.15]

$$\left|\Gamma_{in}\right| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_{load}}{1 - S_{22}\Gamma_{load}} \right| \tag{2.19}$$

and

$$\left|\Gamma_{out}\right| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_{source}}{1 - S_{11}\Gamma_{source}} \right|, \tag{2.20}$$

where the amplifier stage is represented by its S-parameters S_{ij}, and the input, output, source, and load reflection coefficients are Γ_{in}, Γ_{out}, Γ_{source}, and Γ_{load}, respectively. Eqts. (2.19) and (2.20) reveal that the input impedance depends on Γ_{load}, and simultaneously the output impedance depends on Γ_{source}. When feedback between the output and input is positive, a passive Γ_{load} transforms into a negative resistance at Γ_{in} and oscillation of the amplifier becomes possible. A similar observation can be made for Γ_{source} transformed into a negative resistance at Γ_{out}.

The boundaries of the stability regions for the Γ_{load} and Γ_{source} values was analyzed in [2.15]. They appear as a pair of circles on the impedance plane and are known as the load and source stability circles. The simulated stability circles of a 40×1μm/90nm NMOS amplifier at 24GHz are shown in Figure 2.7, with the source

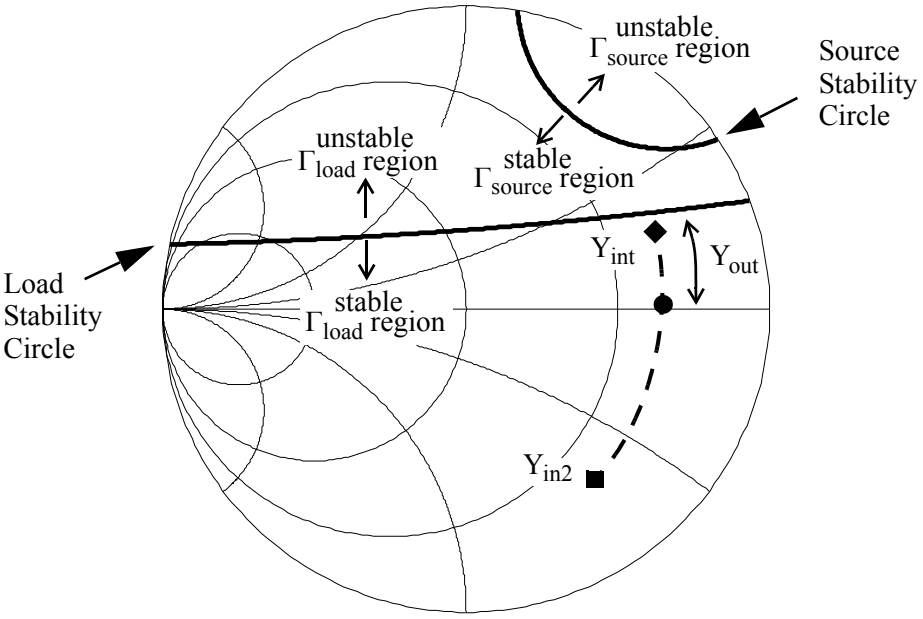

Figure 2.7 Simulated load and source stability circles of a 40×1μm/90nm NMOS common-source amplifier at 24GHz biased at 46.8μA/μm and 0.6V drain-source

and load admittance planes overlapping on the Smith chart are highlighted as stable and unstable impedance regions. Because of the relatively high feed-through via the gate-drain capacitance in CMOS transistor, the unstable region for Γ_{load} occupies the majority of the inductive region in the admittance plane.

A parallel LC resonant tank example to maximize the voltage gain of a voltage amplifier is also illustrated in Figure 2.7 as a dashed line with a fixed conductance. The schematic is similar to the two-stage LNA shown in Figure 2.5. The admittance of the succeeding stage $Y_{in2} = 1/Z_{in2}$ is transformed to Y_{int} by the parallel inductor L_s, and it is subsequently transformed on the x-axis with zero susceptance by absorbing the capacitive $Y_{out} = 1/Z_{out}$ of the amplifier output terminal. Notice that the susceptance of Y_{int} and Y_{out} have to be the same magnitude in order to realize a parallel resonant circuit at the operating frequency. Because Y_{out} is a parasitic parameter, a stable voltage amplifier is never possible with a parallel resonant load for voltage gain if the magnitude of Y_{out} falls into the unstable load impedance region above the x-axis in Figure 2.7. In addition, the magnitude of Y_{out} is proportional to the operating frequency, which makes the stability of a voltage amplifier in CMOS technology difficult to maintain in the mm-wave range.

While transmission line effects necessitates conjugate impedance matching at the input of a RF receiver for maximum power transfer when interfacing with the

off-chip environment, on-chip interconnections (shorter than $\lambda/10$ [2.16], where λ is the wavelength of the highest-frequency signal, *e.g.*, 6.33mm at 24GHz with silicon dioxide dielectric) between building blocks or transistors in an integrated circuit do not behave like transmission lines. Instead, [2.15] shows a diligent selection of the source and load impedances to an amplifier can maximize the amplifier power gain. For a fixed operating frequency, contours of different constant operating power gain values (G_p) are visualized as a family of circles on the complex plane of Γ_{load}. This is known as the operating power gain circles of the amplifier. G_p is the ratio of the power delivered to the load P_{load}, to the power input to the amplifier, P_{in} (i.e., $G_p = P_{load}/P_{in}$). It can be maximized by selecting an appropriate load impedance on the complex plane of Γ_{load}. It is also the parameter to quantify the signal or noise power amplification along the signal path.

A 40×1μm/90nm NMOS common-source amplifier is simulated at 24GHz, and the operating power gain circles are shown in Figure 2.8. As seen on the gain contours in Figure 2.8, there is great flexibility when choosing the load impedance for the same operating power gain, whereas for the voltage gain only a single inductance value is possible that resonates with the total capacitance value at the operation frequency. By properly defining the gain parameter, noise figure, stability, and power gain of an amplifier may be optimized simultaneously using the noise circles, stability circles, and power gain circle for the analysis.

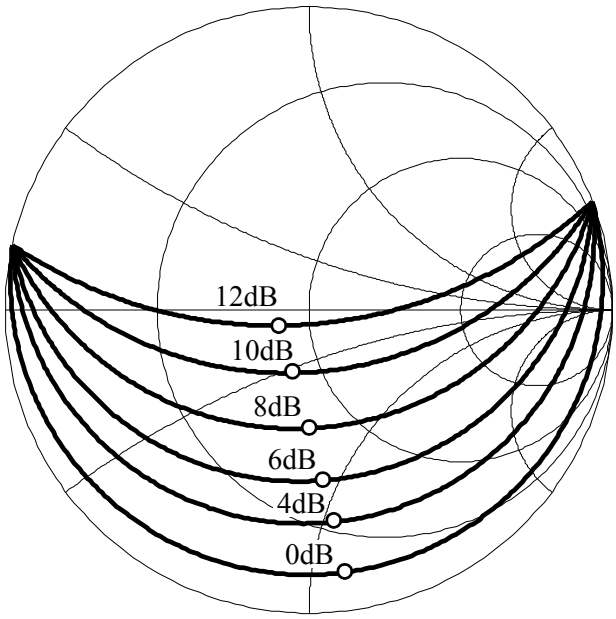

Figure 2.8 Simulated operating power gain circles of a 40×1μm/90nm NMOS common-source amplifier at 24GHz biased at 46.8μA/μm and 0.6V drain-source

Recall from Eqt. (2.7) that the noise factor is a signal-to-noise power ratio, which could be further elaborated with the operating power gain as

$$F = \frac{P_{in}}{N_{in}} \Big/ \frac{P_{in}}{(N_{in} + N_{amp,out}/G_p)}, \tag{2.21}$$

where N_{in} is the noise power accompanying the input signal, and $N_{amp,out}$ is the total output noise originating from the amplifier. The amplifier noise factor is lowered by maximizing the operating power gain. Substituting G_p in Eqt. (2.21) with either voltage (A_v) or current gain (A_i) only take account of the total voltage or current noise power at the amplifier output, respectively. Therefore, G_p has a higher priority than A_v or A_i for amplifier gain optimization.

The use of appropriate gain parameters must be observed for calculating the overall noise factor and linearity of cascade stages. For a two-stage network, the total noise factor is described by the Friis' equation as [2.17]

$$F_{total} = F_1 + \frac{F_2 - 1}{G_{A1}}, \tag{2.22}$$

where F_1 and F_2 are the noise factors of the first and second stages, respectively, and G_{A1} is the available power gain of the first stage (The available power gain is the ratio of the power available from the amplifier output to the power available from the source [2.15]). Maximizing the available power gain for the preceding stage is beneficial to the cascade system noise factor optimization by suppressing the noise contributions from subsequent stages.

There is no precise description for the linearity of cascade stages, because an exact formula must take the phase relationship between all the non-linear distortion products of subsequent stages into account [2.18]. However, an worst-case estimation can be made by assuming all distorted components sum coherently. Expressed as a power, the total input third-order intercept point of a cascade is

$$\frac{1}{G_{IP3,total}} \approx \frac{1}{G_{IP3,1}} + \frac{G_{p1}}{G_{IP3,2}}, \tag{2.23}$$

where $G_{IP3,1}$ and $G_{IP3,2}$ are the input third-order intercept points of the first and second stages, respectively, and G_{p1} is the operating power gain of the first stage. Because the signal and distortion are amplified along the chain, higher linearity is demanded from later stages in the radio receiver. The same observation applies by expressing Eqt. (2.23) in terms of the square of voltage quantities [2.9].

2.3 Phase Noise

Signal from the receiving antenna is not suitable for immediate digitization because the high RF carrier frequency limits the resolution attainable from an analog-to-digital converter (ADC) [2.19]. The poor SNR from multi-gigahertz ADC [2.20] dete-

riorates the receiver demodulation accuracy and the overall system noise figure. The signal is therefore frequency down-converted by a mixer and local oscillator (LO) before A/D conversion and demodulation. Noise from the LO limits the receiver selectivity.

An oscillator is created using a positive feedback loop where instability of the circuit sustains a periodic waveform [2.21]. Ideally, the output is a pure sinusoidal of a precise frequency. In practice, noise from circuit elements affects the phase shift around the feedback loop and modulates the output waveform in a random manner. The LO signal could be expressed in the time domain as

$$V_{LO} = A(t) \cdot \cos(\omega_o(t) \cdot t + \phi(t)), \tag{2.24}$$

where $A(t)$, $\omega_o(t)$, and $\phi(t)$ are the instantaneous amplitude, angular frequency, and phase, respectively. Amplitude fluctuation $A(t)$ describes the LO amplitude noise, which is normally attenuated by limiting (e.g., from the supply voltage), or with a dedicated amplitude control feedback loop. Frequency fluctuation $\omega_o(t)$ could be the result of time or temperature drifting of the transistor gain, LC tank resonant frequency, or parasitic component values. It is usually eliminated when the LO source is embedded in a phase-lock loop which is locked to a stable frequency reference. The dominant noise source is then $\phi(t)$, which is the phase noise.

A number of theories attempt to explain the origin of phase noise, including linear feedback analysis with noise shaping [2.22], and the impulse sensitivity function with cyclo-stationary noise sources [2.23]. They all agree with the observation made by Leeson and presented without formal proof in 1966 [2.24], namely that the single-sideband phase noise, or the single-side-band power spectral density of $\phi(t)$ for an LC oscillator, may be expressed as

$$S_{\phi}(\omega_m) = \left(\frac{F_{LO} \cdot kT}{P_{LO}} + \frac{\alpha}{\omega_m}\right) \cdot \left[1 + \left(\frac{\omega_o}{2Q\,\omega_m}\right)^2\right], \tag{2.25}$$

where F_{LO}, P_{LO}, α, ω_o, ω_m, and Q, are: the effective noise factor, oscillation signal power, flicker noise constant, oscillation frequency, frequency offset between the measured phase noise frequency and the oscillation frequency, and the loaded quality factor of the LC tank, respectively. Variables k and T are as previously defined in this chapter. Thermal noise and 1/f noise are up-converted to the oscillation frequency which contribute the $1/\omega_m^2$ and $1/\omega_m^3$ dependencies, respectively [2.25].

In the frequency domain, phase noise manifests itself as the excessive skirts around the single carrier power as shown in Figure 2.9(a). It is measured by quantifying the noise power within a 1Hz bandwidth with respect to the carrier power in units of dBc/Hz. Overlaying the single-side-band PSD with the axis in logarithmic scale in Figure 2.9(b) reveals the –30dB/dec and –20dB/dec regions which correspond to the α/ω_m and $F_{LO} \cdot kT/P_{LO}$ terms in Eqt. (2.25), respectively.

Jitter is the equivalent of phase noise when expressed in the time domain. It measures the time varying period of the oscillation waveform, which is randomly

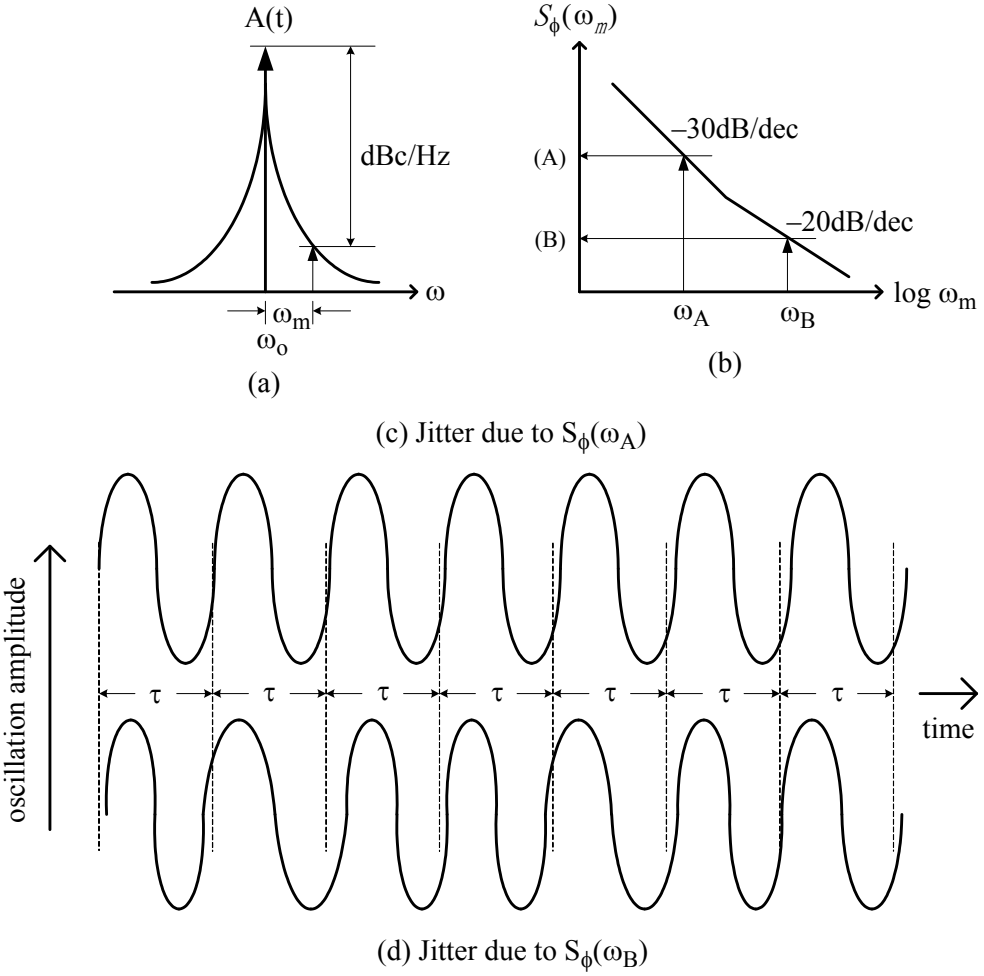

Figure 2.9 Frequency and time-domain representations of phase noise

modulated by noise. This is equivalent to measuring the magnitude of the random variation of the oscillation period from the ideal value of $\tau = 2\pi/\omega_o$. The magnitude of the jitter depends on the noise magnitude, and the rate of change of the jitter depends on the frequency offset (ω_m) of the noise component. This is illustrated in Figure 2.9(c) and (d) by the phase noise at points (A) and (B), respectively. Low frequency noise at point (A) gives a slowly varying jitter whereas high frequency noise at point (B) produces time jitter at a more rapid rate. Considering only the thermal noise source, jitter $\sigma^2(t)$ is related to phase noise by [2.26]

$$\sigma^2(t) = \frac{8}{\omega_o^2}\int_0^\infty S_\phi(f)\sin^2(\pi f t)\,df, \tag{2.26}$$

where ω_o is the nominal oscillation frequency and $S_\phi(f)$ is the phase noise PSD.

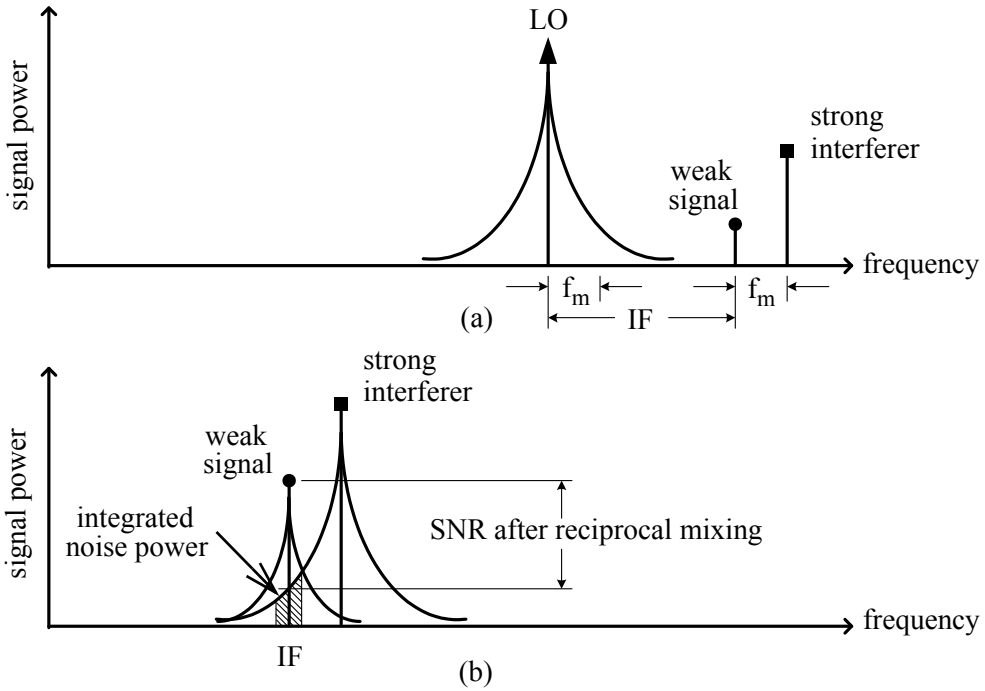

Figure 2.10 Signal-to-noise ratio deterioration due to reciprocal mixing with the x-axis represents RF in (a) and IF in (b)

Receiver selectivity of frequency-modulation based radar is limited by phase noise from the LO signal [2.27]. The mechanism that affects the received signal-to-noise ratio is similar to the reciprocal mixing seen in typical RF receiver. Figure 2.10 shows a (desired) weak but noiseless signal with infinite SNR accompanied by a strong interferer separated by f_m. Both of them are being frequency down-converted by a noisy LO, and this produces overlapping spectra of phase noise power at the intermediate frequency. The integrated phase noise power across the signal bandwidth of the interferer at a frequency offset of f_m overwhelms the desired signal quality. Because the radar received echo is a replicate of the transmitted signal, noise feedthrough from Tx to Rx is equivalent to an echo corresponding to a target at zero range.

2.4 Summary

Different design techniques and the theoretical background for the optimization of a mm-wave frequency radio receiver in CMOS technology were presented in this chapter. The degradation caused by noise, distortion, and oscillator phase noise on the received signal quality were reviewed. Even though impedance matching for maximum power transfer is irrelevant in an integrated circuit implementation, applying microwave circuit design techniques in an on-chip environment offer sig-

nificant advantages over the classical RFIC design approach. Simultaneous optimization of noise figure, stability, gain, linearity, and power dissipation is simplified by proper selection of the DC bias point together with the manipulation of certain performance metrics viewed on the complex impedance plane. This technique will be demonstrated by design examples presented in Chapters 5 and 6 that illustrate the merits of visualizing performance trade-offs between design parameters in the input and output impedance planes. The phase noise power dependency on the LC resonant tank quality factor and power consumption was also described, and its effect on the received signal quality with respective to the relative offset from the LO carrier frequency was explained.

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Chapter 3

Short-Range Radar System Implementation

The low cost and low power requirements of a short-range radar (SRR) for the automotive, industrial and consumer electronics markets require proper selection of the signal modulation and receiver topology. This chapter presents the system level implementation of an frequency-modulated continuous-wave (FMCW) 24GHz-band SRR sensor and addresses the definition of the link budget and the receiver architecture. Specifications for the receiver building blocks with a view towards implementation in CMOS are also derived.

The operating principle of FMCW radars is first presented. It is shown that FMCW is suitable for short-range applications on the basis of hardware implementation, power consumption, and isolation requirements. This is followed by radar link budget calculation which covers the transmitter emission limit, received signal-to-noise ratio, third-order non-linearity, and phase noise specifications. The direct-conversion receiver is then considered for the SRR application. The heterodyne receiver is also examined, and it is shown that the image problem is mitigated by the distinctive frequency profile of an FMCW signal. Finally, a design example that details the selection of parameters for the circuit blocks which optimize the SRR system performance is presented.

3.1 Radar Configurations

Radar requires modulation applied to the waveform radiated by the transmitter, and signal processing of the received echo. Range and velocity parameters are evaluated by observing the time delay and frequency shift introduced to the transmitted carrier by a target before reception.

3.1.1 FMCW Radar

An FMCW radar block diagram is shown in Figure 3.1. Frequency modulation (FM) is performed on a continuous-wave carrier before transmission. The most popular scheme is linear FM by a triangular wave [3.1].

The transmitted waveform via the PA is a continuous sinusoid, where the frequency ramps up between f_1 and f_2 during the first time interval [T_1, as shown in the frequency profiles in Figure 3.2(a)], and ramps down by the same magnitude

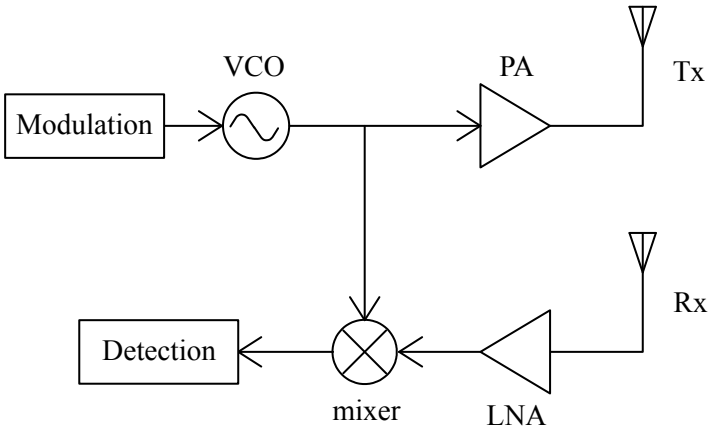

Figure 3.1 FMCW radar block diagram

during the second time interval (T_2). Usually $T_1 = T_2$ and their sum is the modulation period (T_m). The difference between f_1 and f_2 (i.e., the sweep frequency range) defines the bandwidth (BW) of the transmitted signal. For a stationary object positioned at range R, the echo arrives at the receiver LNA with a time delay of $t_{flight} = 2R/c$, where c is the speed of light. The received frequency profile is also shown in Figure 3.2(a). By extracting the instantaneous frequency difference, between the transmitted and received signals at the mixer IF output [Δf shown in Figure 3.2(b)], range information for the target is obtained from simple trigonometric relation as

$$\frac{\Delta f}{BW} = \frac{t_{\text{flight}}}{T_m/2}, \tag{3.1}$$

and therefore

$$R = \frac{T_m \cdot c}{4 \cdot BW} \cdot \Delta f. \tag{3.2}$$

The value of Δf must be determined during the time for detection (T_{det} shown in Figure 3.2), where the IF remains stable with time. Otherwise, this information is lost and is not recoverable. For typical case, $T_{det} = T_m/2$. Assuming that one period of Δf is available within $T_m/2$, the minimum value of Δf is

$$\Delta f_{\min} = \frac{1}{T_m/2} = \frac{2}{T_m}. \tag{3.3}$$

Combining Eqts. (3.2) and (3.3), the range resolution is

$$\Delta R = \frac{c}{2 \cdot BW}. \tag{3.4}$$

FMCW radar completes a full range detection in one modulation period of T_m. Multiple targets are resolved by distinguishing discrete frequency tones in the IF spectrum. The lower bound on T_m is determined by the radar maximum detect-

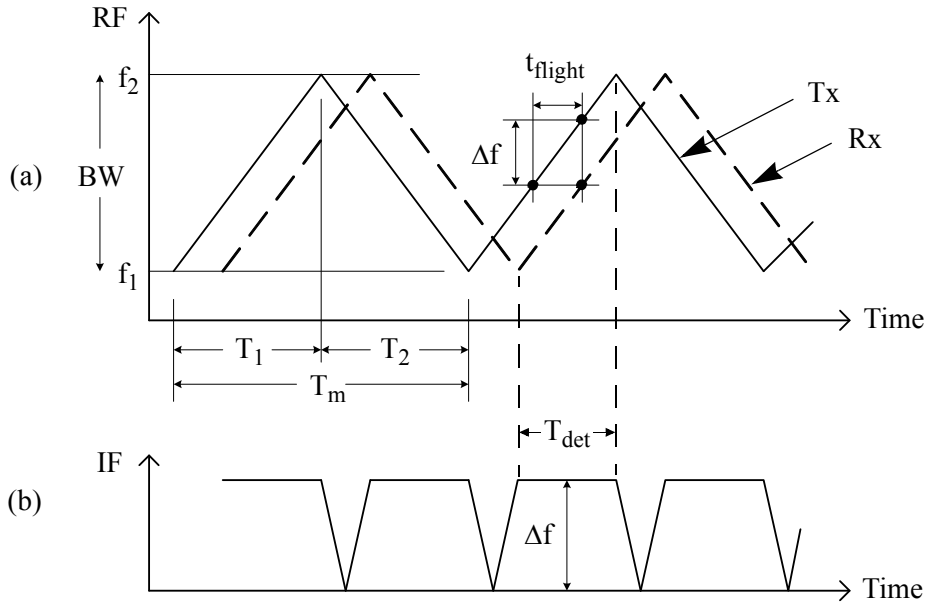

Figure 3.2 FMCW radar transmitted frequency profile in (a), and received frequency profile in (b) on the same time axis for a stationary target

able range where the echo time delay reaches the maximum value and equals to half of the modulation period [i.e., $T_m/2 = t_{flight(max)}$]. Therefore,

$$R_{max} = c \cdot T_m / 4 . \tag{3.5}$$

Doppler shift ($f_{Doppler}$) is introduced to the echo by the relative velocity between the target and radar sensor (Δv_{target}) [3.2]. It is given by

$$f_{Doppler} = \pm \frac{2 \cdot \Delta v_{target} \cdot f_{carrier}}{c} , \tag{3.6}$$

where c is the speed of light, and $f_{carrier}$ is the instantaneous transmitted frequency. The Doppler shift can be used to determine the velocity of a target. The FMCW radar frequency profiles of an approaching target with velocity v_{target} are shown in Figure 3.3. The Doppler shift is proportional to the carrier frequency, which varies during the sweep time T_m because the VCO modulates the carrier frequency as a function of time. In order to simplify the analysis, the assumption is made that the variation of Doppler shift within each period T_m is much less than the frequency difference between Tx and Rx caused by the target range information. This could be expressed by comparing Eqts. (3.6) and (3.1) as

$$\frac{2 v_{target}}{c} (f_2 - f_1) \ll \frac{t_{flight}}{T_m/2} \cdot BW \tag{3.7}$$

or

$$v_{target} \ll (2R) / T_m . \tag{3.8}$$

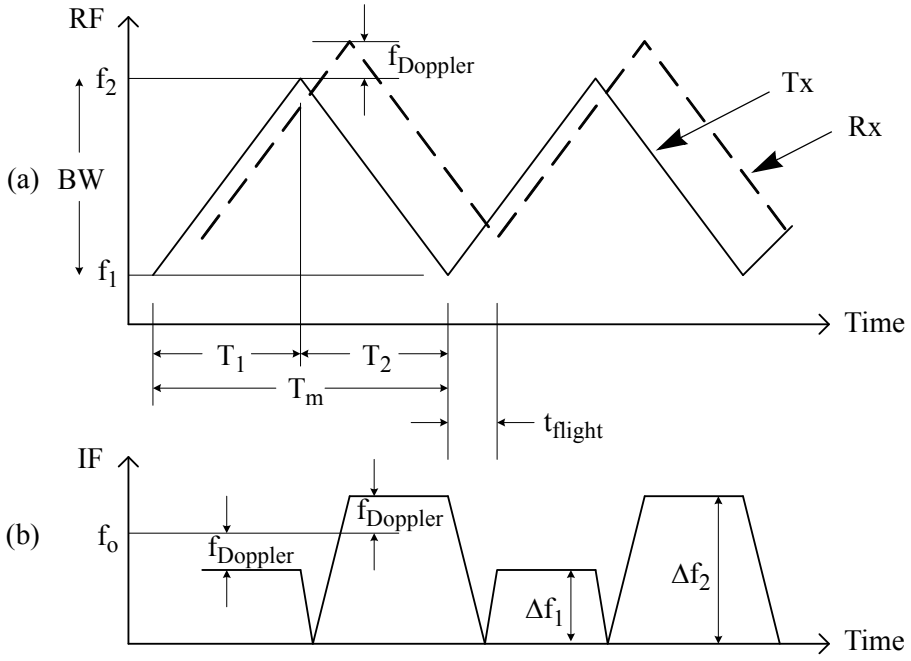

Figure 3.3 FMCW radar transmitted waveform in (a), and received frequency profile in (b) on the same time axis for an approaching target

For example, if the radar specification requires a maximum range and relative velocity of 10m and 30km/hr, respectively, Eqt. (3.8) holds as long as $T_m \ll 2.4$s. The average of f_1 and f_2 is therefore taken for the Doppler frequency calculation as

$$f_o = (f_1 + f_2)/2. \tag{3.9}$$

Therefore, for a positive Doppler shift, the IF values are no longer the same during time intervals T_1 and T_2, which are noted as Δf_1 and Δf_2 in Figure 3.3(b), respectively. The Doppler shift in Eqt. (3.6) modifies the IF output from a stationary target in Eqt. (3.1). This results in

$$\Delta f_1 = \Delta f - \frac{2V_{\text{target}}}{c} \cdot f_o \tag{3.10}$$

and

$$\Delta f_2 = \Delta f + \frac{2V_{\text{target}}}{c} \cdot f_o. \tag{3.11}$$

The target range is calculated by summing Eqts. (3.10) and (3.11), and then applying Eqt. (3.2) as

$$R = \frac{T_m \cdot c}{4 \cdot BW} \cdot \left(\frac{\Delta f_1 + \Delta f_2}{2}\right). \tag{3.12}$$

The target velocity is given by resolving the Doppler shift in Eqt. (3.6) with the difference between Eqts. (3.10) and (3.11) as

$$v_{\text{target}} = \frac{c}{2} \cdot \frac{\text{Doppler shift}}{f_o} \approx \frac{c}{4} \cdot \left(\frac{\Delta f_2 - \Delta f_1}{f_o} \right). \tag{3.13}$$

From Eqts. (3.3) and (3.13), the velocity resolution is

$$\Delta v_{\text{target}} = \frac{c}{T_m} \cdot \frac{1}{f_o}. \tag{3.14}$$

3.1.2 Requirements for Short-Range Application

Measurement distance up to 10m, minimum range of 0.5m, and resolution of 5cm are assumed for the SRR application.

The continuous nature of FMCW radar transmission favours its implementation in nanometer CMOS technology. As will be explained in Section 3.4, a simple buffer with the function of isolating the VCO from the external circuits could obviate the requirement for the PA shown in Figure 3.1 at a low transmitted power level. Even in simultaneous operation, the Rx is difficult to saturate or compress as long as there is adequate isolation between the Tx and Rx antennas.

For an FMCW radar, linearity of the transmitted triangular frequency profile is a prerequisite to ensure accuracy of the range and velocity measurements given in Eqts. (3.12) and (3.13), respectively [3.3]. Direct digital frequency synthesizer [3.4], fractional-N PLL [3.5], or all-digital PLL [3.6] are suitable candidates for LO generation that are well described in the literature. Bandwidths of 512MHz and 250MHz were measured from two SiGe VCOs at 19GHz [3.4] and 24.5GHz [3.5], respectively. Their frequency tuning ranges are less than 3%. On the other hand, a CMOS wideband digitally-controlled oscillator realized an 11.7% tuning range at 60GHz (while the frequency tuning range from a demonstrated FMCW signal is only 1.97%) [3.6]. From Eqt. (3.4), the range resolution of 5cm requires a 3GHz bandwidth at 24GHz with 12.5% tuning range. With the necessary design margin to accommodate process, voltage, and temperature variations, the feasibility of a VCO generating a continuous, wideband spectrum from a low supply voltage still poses a challenge in CMOS technology.

3.2 Link Budget

Restrictions limiting radar performance are multidimensional. Government rulings regulate the carrier frequency, transmission bandwidth and power level. Physical environment and electronic devices introduce path loss, noise, non-linearity, and phase noise that degrade the signal-to-noise ratio. This section covers the radar standards applicable in the United States and Europe, and provides the link budget equations which transform the SRR system requirements into receiver electrical specifications in order to streamline the optimization process.

3.2.1 Emission Limits

Standardization regulates the frequency usage and maximum radiated power level for radar ranging services. An automotive SRR centered at 24GHz is governed by the Federal Communications Commission (FCC) in the US [3.7], and the European Telecommunications Standards Institute (ETSI) across the European countries [3.8]. An ultra-wideband (UWB) signal shall be confined between 22GHz and 29GHz, and between 22GHz and 26.65GHz for the FCC and ETSI provisions, respectively. The permitted radiation level is quantified by the maximum average rms power density. It is defined as the effective isotropic radiated power (EIRP) including antenna gain, and is measured in a 1MHz resolution bandwidth. It can be expressed as

$$P_{\mathrm{EIRP}}(dBm) = P_t(dBm) + G_t(dB), \tag{3.15}$$

where P_t is the transmitter EIRP and G_t is the transmitter antenna gain. A lossless isotropic antenna gives $G_t = 0$dB, and therefore $P_{EIRP} = P_t$.

The FCC limits emissions to a maximum of –41.3dBm in the band designated for automotive radar from 22GHz to 29GHz. The emission limit is lowered to –61.3dBm beyond the 22GHz–31GHz frequency band. The ETSI power density regulation is similar, at –41.3dBm between 22.65GHz and 25.65GHz. The power limit is reduced progressively to –61.3dBm at 22GHz and 26.65GHz. The radiated power must be less than –61.3dBm for the (out-of-band) frequency range between 10GHz and 40GHz. A radar product designed for the consumer electronics markets can reach 50% of the potential customers worldwide [3.9] by satisfying these two regulatory standards for radiated emissions.

3.2.2 Signal-to-Noise Ratio

Radar power transmission can be calculated using Friis' formula [3.10]. The radiated power density available at the target is

$$p_{\mathrm{target\_power\_density}} = \frac{P_t \cdot G_t}{4\pi R^2}, \tag{3.16}$$

where P_t is the transmitter EIRP, G_t is the transmitter antenna gain, and R is the target range. The received signal comes from power reflected by a target, rather than an independent transmitting antenna. Therefore, the radar cross-section (RCS) is used to determine the power at the receiver. The RCS of the target is defined as [3.11]

$$\mathrm{RCS} = \sigma = 4\pi R^2 \frac{p_{\mathrm{receive\_power\_density}}}{p_{\mathrm{target\_power\_density}}}, \tag{3.17}$$

where $p_{\mathrm{receive\_power\_density}}$ is the echo signal power density at the receiver antenna. The relationship between RCS and the target's physical geometry can be determined by solving Maxwell's equations for the scattered field [3.11]. There is no simple equation describing the RCS for most target shapes. A sphere of radius r has an RCS of πr^2. In general, the RCS increases with the target's physical dimensions.

The received power is

$$P_r = p_{\text{receive\_power\_density}} \cdot A_e , \tag{3.18}$$

where A_e is the effective area of the receiver antenna [3.10], and

$$A_e = \frac{\lambda^2 G_r}{4\pi} , \tag{3.19}$$

where λ is the carrier wavelength and G_r is the receiver antenna gain. The received power is found by combining expressions from Eqts. (3.16) to (3.19) to obtain

$$P_r = \frac{1}{(4\pi)^3} \cdot \frac{\sigma\lambda^2}{R^4} \cdot G_r \cdot (P_t \cdot G_t) . \tag{3.20}$$

The last term of Eqt. (3.20) $P_t \cdot G_t$, emphasizes the EIRP limit in Eqt. (3.15).

With only thermal noise taken into account across the echo signal bandwidth, the receiver input SNR is

$$SNR_{\text{in}} = \frac{1}{(4\pi)^3} \cdot \frac{\sigma\lambda^2}{R^4} \cdot G_r \cdot (P_t \cdot G_t) \cdot \frac{1}{kT \cdot BW} , \tag{3.21}$$

where k is Boltzmann's constant, T is absolute temperature, and BW is the signal bandwidth. Substituting Eqt. (3.21) into the noise factor equation (i.e., Eqt. (2.7)) gives the output SNR

$$SNR_{\text{out}} = \frac{1}{(4\pi)^3} \cdot \frac{\sigma\lambda^2}{R^4} \cdot G_r \cdot (P_t \cdot G_t) \cdot \frac{1}{kT \cdot BW} \cdot \frac{1}{F} , \tag{3.22}$$

where F is the receiver noise factor.

Although an UWB signal is used for target ranging at RF, the IF bandwidth in an FMCW radar is given by the instantaneous frequency difference between the Tx and Rx signals. Its value is usually much smaller than the RF bandwidth. Band limiting with a filter at the IF therefore improves the signal-to-noise ratio [3.12], and the resultant SNR is

$$SNR_{\text{out\_IF}} = \frac{1}{(4\pi)^3} \cdot \frac{\sigma\lambda^2}{R^4} \cdot G_r \cdot (P_t \cdot G_t) \cdot \frac{1}{kT \cdot \Delta IF_{\max}} \cdot \frac{1}{F} , \tag{3.23}$$

where $\Delta IF_{\max}$ is the maximum IF bandwidth. For an FMCW radar, $\Delta IF_{\max}$ is the sum of the IF which corresponds to the target range, and the absolute value of the Doppler shift (i.e., the highest value between Eqts. (3.10) and (3.11)).

For a target that changes its position slowly compared to the radar modulation period (see Figure 3.2), the echo from consecutive periods can be integrated coherently (i.e., by applying averaging), while the noise power between the same periods is uncorrelated. Coherent integration therefore introduces processing gain and an increase in the output SNR [3.11]. For N consecutive correlated samples,

$$SNR_{\text{out\_IF\_integrated}} = SNR_{\text{out\_IF}} \cdot N. \tag{3.24}$$

Radar accuracy is quantified by the probability of detection (P_D) and the probability of false alarm (P_{fa}), which are functions of the received signal SNR prior to the decision process. This SNR is minimum for a target positioned at the maximum range. System simulations predict that an SNR of 10.95dB is required for P_D and P_{fa} equal to 0.9 and 10^{-3}, respectively [3.13].

3.2.3 Third-Order Non-Linearity

With the majority of frequency spectrum between 22GHz and 31GHz allocated for radio astronomy, radio location, satellite broadcasting, and satellite mobile communication [3.14], the existence of a strong in-band blocker that would demand high linearity from the SRR is unlikely. The main source of interference for automotive applications is other radar sensors, where it is anticipated that there will be an average of four SRRs per car. A case study in 2009 showed about 453 cars per km^2 in an urban area [3.15]. A worst case scenario will be assumed, where a potential target at maximum range (weakest signal) is accompanied by two equal power interfering radar transmitters positioned at minimum range (strongest interference), and that a third-order intermodulation tone is generated which lies exactly on the target's echo frequency. The magnitude of this IM_3 component at the receiver input is

$$IM_3(dBm) = 3 \cdot P_{\text{interference}}(dBm) - 2 \cdot IIP_3(dBm), \tag{3.25}$$

where $P_{\text{interference}}$ is the power level at the receiver predicted by Eqt. (3.20) for minimum range interference and IIP_3 is the input third-order intercept point of the receiver. Expressing Eqt. (3.25) in linear units gives

$$IM_3 = \frac{P_{\text{interference}}^3}{IIP_3^2}. \tag{3.26}$$

By allocating the distortion to be M times the thermal noise power given by Eqt. (3.23) (where M is a real number), the degradation in the Rx SNR budget is $10 \cdot \log(1+M)$dB. Under the foregoing assumptions, the required IIP_3 is

$$\begin{aligned} IM_3 = \frac{P_{\text{interference}}^3}{IIP_3^2} &= kT \cdot \Delta IF_{\max} \cdot F \cdot M \\ IIP_3 &= \sqrt{\frac{P_{\text{interference}}^3}{kT \cdot \Delta IF_{\max} \cdot F \cdot M}}, \end{aligned} \tag{3.27}$$

where k is Boltzmann's constant, T is absolute temperature, ΔIF_{max} is the maximum IF bandwidth and F is the receiver noise factor.

An FMCW radar uses periodic frequency sweep for range detection. Therefore, the probability that two nearby radars generate a constant in-band IM_3 tone which overlap exactly with the received echo frequency is extremely low. Meeting the specification stated in Eqt. (3.27) is only necessary in the worst-case situation.

Averaging over successive 'chirps' (i.e., modulation cycles) also reduces the degradation from any IM_3 components that appear momentarily in the IF spectrum.

3.2.4 Phase Noise

Target range and velocity information are contained in the IF signal measured in Eqts. (3.12) and (3.13) via frequency mixing of the instantaneous transmitted LO and the received echo. LO phase noise degrades signal fidelity and immediately contributes an additional noise component that affects the SNR calculated in Eqt. (3.23). In a scenario where two closely spaced stationary targets are detected, their IF values depend on their corresponding range from the radar transmitter, and are given by re-arranging Eqt. (3.2) to

$$IF_x = \frac{4 \cdot BW}{T_m \cdot c} \cdot R_x, \tag{3.28}$$

for x = 1 or 2. Variables R_x and IF_x are the range and IF values, respectively. Figure 3.4(a) illustrates how phase noise power from two IF signals affect each other's fidelity.

While phase noise for an oscillator may be described by Leeson's equation as explained in Section 2.3, the effect of phase noise on FMCW radar system performance is mitigated by the correlation between transmitted and received carrier waveforms generated by the same oscillator. This effect was analyzed in [3.16 and 3.17], and a noise reduction factor was derived to correct the phase noise spectrum predicted from Leeson's model. The resulting phase noise equation for an FMCW radar is

$$S_{\phi,\,\mathrm{FMCW}}(\omega_m) = S_{\phi}(\omega_m) \cdot 4\sin^2\left(\frac{R \cdot \omega_m}{2 \cdot c}\right), \tag{3.29}$$

where $S_{\phi,\mathrm{FMCW}}(\omega_m)$ and $S_{\phi}(\omega_m)$ are the single-sideband phase noise PSDs of the FMCW radar echo and local oscillator signals, respectively, ω_m is the offset fre-

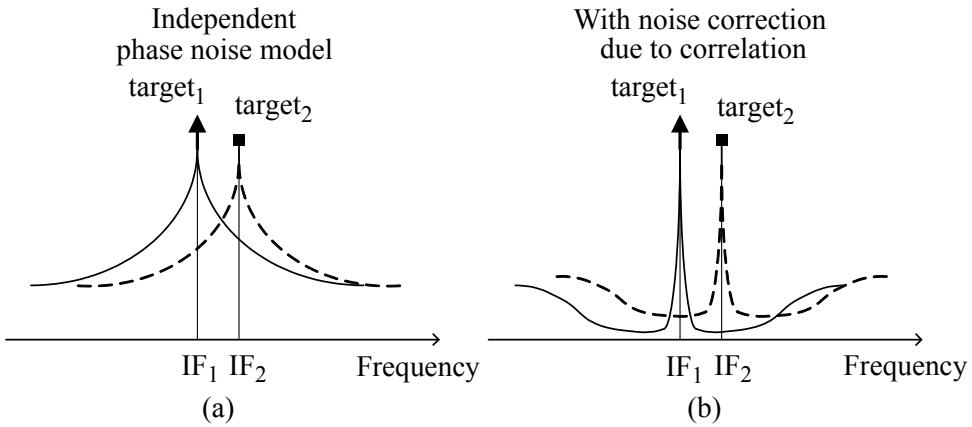

Figure 3.4 FMCW phase noise (a) independent noise model, and (b) with noise correction due to correlation between LO waveforms

quency, R is the range, and c is the speed of light.

The reduction of phase noise power with respect to the target range (R) and offset frequency (ω_m) [as indicated in Eqt. (3.29)] could be interpreted by the jitter analysis introduced in Figure 2.9. The instantaneous transmitted signal is effectively a time delayed version of the received signal, where the delay time is proportional to the target range. A shorter range gives less time for jitter accumulation [3.18]. Therefore, the correlation between signals is stronger and the phase noise is reduced significantly. For example, Eqt. (3.28) indicates that a closer target gives a lower IF value (i.e., $R_1 < R_2$ gives $IF_1 < IF_2$). Therefore, the phase noise reduction at IF_1 is larger than at IF_2, as shown in Figure 3.4(b). For the extreme case of a zero range target, the effect of phase noise on the IF signal diminishes to zero. FMCW radars benefit the most from correlation between the transmitted and received signal when the maximum detection range is limited.

From another perspective, the rate of change of jitter increases with increasing frequency offset (as explained in Section 2.3) when the target range is kept constant. Phase noise close to the carrier varies at a slower rate, and therefore shows greater correlation than phase noise at larger offset frequency. As shown in Figure 3.4(b), there is a null in the phase noise PSD at zero offset frequency.

Given the SRR range specification, the IF planning should exploit the relaxed requirement on phase noise. A lower IF favors phase noise reduction due to greater correlation, which lowers the power consumption necessary for the LO generation.

SNR degradation due to phase noise should also be taken into account in additional to the thermal noise and IM distortion penalties of Eqts. (3.23) and (3.27), respectively. Refer to the scenario illustrated in Figure 3.4(b), where phase noise power from IF_2 degrades the signal quality at IF_1. The phase noise power is found by integrating the phase noise equation [i.e., Eqt. (3.29)] from the IF detection refresh rate (period of one-half the FMCW modulation period T_m) to the maximum IF bandwidth. It is expressed as

$$N_{\text{phase\_noise}} = \int_{4\pi/T_m}^{\Delta IF_{\max}} S_\phi(\omega_m) \cdot 4\sin^2\left(\frac{R\cdot\omega_m}{2\cdot c}\right) d\omega_m. \tag{3.30}$$

While a minimum range target has the strongest echo signal (which gives the highest amount of phase noise power), it also benefits the most from phase noise correlation. The worst-case situation occurs when two targets are positioned at the minimum and maximum ranges, and when the echoes are down-converted to IF_1 and IF_2, respectively. Signal at IF_1 has a higher Rx power but more phase noise reduction, while signal at IF_2 has a lower Rx power but less phase noise reduction. The degradation in SNR seen by each IF signal due to the phase noise of the other depends on the frequency planning of the IF range in the radar system design. The

required VCO phase noise specification is given by $S_\phi(\omega_m)$ in Eqt. (3.30), with ω_m being the difference in IF between the two targets.

3.3 SRR Receiver Architectures

The fundamental problem of radar reception comes from the retrieval of the desired information with adequate fidelity, while confronting the potential disruptions caused by interference, noise, intermodulation distortion, and phase noise. An understanding of the application environment assists the selection and optimization of the receiver architecture.

3.3.1 Homodyne Receiver

The homodyne receiver shown in Figure 3.5 has a simple structure [3.19]. By aligning the LO frequency with the RF carrier, signal is directly downconverted to an IF around zero Hertz via a mixer after being amplified by a LNA. A low-pass filter rejects out-of-band interference prior to detection at IF.

Problems exist in a homodyne receiver that limit its usage in an FMCW SRR. Because of finite port-to-port isolation, LO leakage towards the RF input of the LNA or mixer produces a DC component at the mixer IF output. Apart from corrupting the IF signal, this DC voltage could saturate the circuit connected to the IF output because of high gain in the IF amplifier. High-pass filtering of this DC voltage is difficult because of the low IF used in a short-range FMCW application, and also the desire to use a low IF in order to take advantage of LO phase noise cancellation as explained in Section 3.2.4.

Distortion arising from second-order non-linearity (as explained in Section 2.1.2) can cause severe problems in an FMCW automotive radar. Erroneous detection can occur because the origin of the different RF signals cannot be distinguished due to masking by second-order distortion [3.20]. Two, or multiple vehicles could travel with the same relative position for a lengthy amount of time with respect to

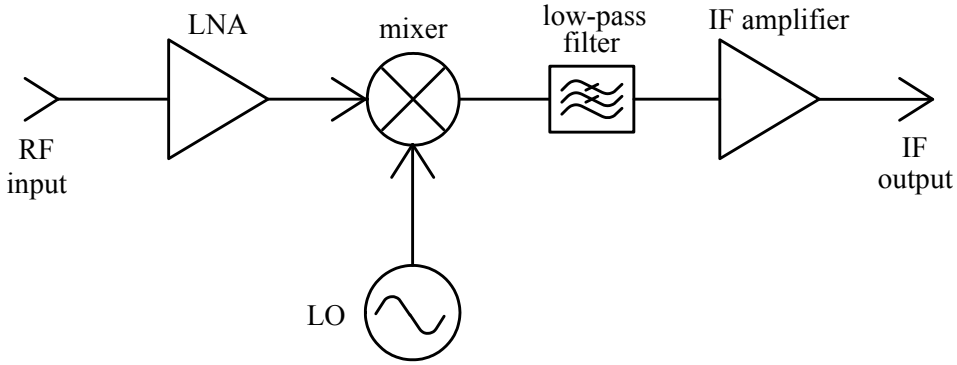

Figure 3.5 Block diagram of a homodyne receiver

the FMCW modulation period. In contrast with the third-order intermodulation described in Section 3.2.3, this undesired IF signal component remains for successive modulation periods and cannot be eliminated by signal averaging.

The second-order non-linearity in an FMCW radar receiver also demodulates any amplitude variation on the received signal to the IF output [3.21]. For example, suppose that there is a pulsed Doppler radar [3.22] nearby transmitting a pulse-modulated carrier with a pulse repetition interval of $1/\Delta IF_{pulsed}$ towards the radar receiver. False alarm will occur indicating a target with an IF at ΔIF_{pulsed}.

An FMCW SRR favors a low IF in order to relax VCO phase noise and power consumption requirements. Also 1/f noise generated by CMOS transistors must be minimized by utilizing very large area devices in the mixer and IF circuit blocks. The cost of doing so is increased power consumption when maintaining the same bias current density for the active devices.

VCO pulling [3.23] via the transmitter power amplifier is a potential problem in a homodyne receiver because the Tx and LO carriers share the same frequency. This is exacerbated by the UWB nature of the FMCW SRR, which requires a wide and continuous tuning range VCO with high sensitivity. The frequency modulation linearity and accuracy are degraded, which adversely increases uncertainty in the radar range and velocity measurement [3.3].

3.3.2 Heterodyne Receiver

The problems designing a homodyne receiver stem from positioning the LO exactly at the carrier frequency. The receiver suffers from imperfections such as flicker (1/f) noise, DC offset, and second-order non-linearity at baseband, as well as limitations on the generation of the LO and its performance at high frequency. The heterodyne receiver shown in Figure 3.6 mitigates these problems by employing two-step down-conversion [3.24], in which LO_1 is offset in frequency from the RF carrier by the first intermediate frequency (IF_1), and conversion by LO_2 subsequently brings this signal to the final IF output.

The DC offset voltage, flicker noise, and second-order intermodulation distortions originating from the first down-conversion stage can be efficiently removed

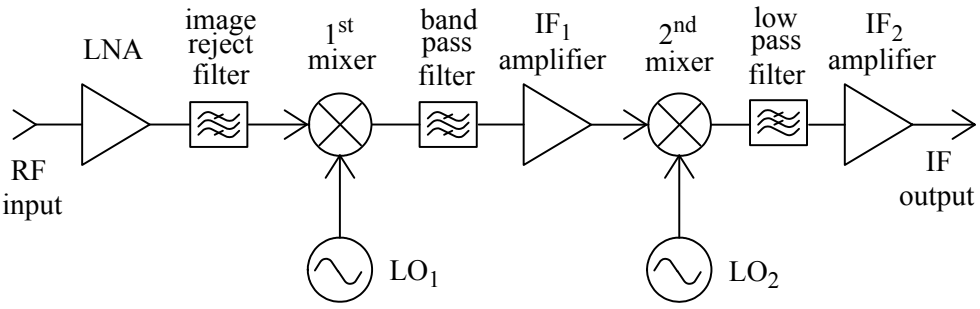

Figure 3.6 Block diagram of a heterodyne receiver

from the IF_1 signal as long as these impairments lie well below the first IF band. Any residual impairments will also be up-converted around the LO_2 frequency in the second mixer, and have no impact on the final IF output.

The second down-conversion by LO_2 is similar to a stand-alone homodyne receiver, but operates at a lower frequency (i.e., $\omega_{LO2} < \omega_{LO1} < \omega_{RF}$). Therefore, matching of differential circuits and port-to-port isolation are better maintained given a certain DC current budget. Subsequently, the DC offset and second-order non-linearity from the 2nd mixer is less severe than the 1st mixer [3.25]. A lower LO_2 frequency also favors the use of larger transistor sizing or a passive-type switching mixer [3.26] that lowers the flicker noise degradation from the 2nd mixer to the final IF output.

The IF_1 amplifier provides additional freedom for the gain distribution across different frequencies, and relaxes the power gain requirements from the LNA and IF_2 amplifier. Compared to the LNA, this amplifier can also be better optimized for transistor size, flicker noise, and power consumption because it operates at IF_1 rather than at the RF.

The extra hardware necessary for the LO_2 source in Figure 3.6 could be simply derived from LO_1 via a frequency divider with little additional cost, so that frequencies LO_1 and LO_2 are related by

$$\omega_{LO2} = \omega_{LO1} / K, \tag{3.31}$$

where K is the division ratio. The radar transmitter performs single-sideband frequency mixing with these LOs [3.27] for the Tx carrier generation, which is given by

$$\begin{aligned} \omega_{TX} &= \omega_{LO1} + \omega_{LO2} \\ &= \frac{K+1}{K}\,\omega_{LO1} \quad . \end{aligned} \tag{3.32}$$

The generation of a linear FMCW carrier from LO_1 is possible by phase locking LO_1 to a lower frequency reference within a PLL [3.4,3.5], in which cascade of divider stages are already present [with division factor K in Eqt. (3.31)]. A lower VCO frequency at LO_1 also favors optimization of the trade-offs between phase noise, power consumption, and tuning range in a CMOS implementation by providing a wider design space for these trade-offs.

The image of the first frequency down-conversion is a problem that must be resolved in a heterodyne receiver [3.24]. Consider the multiplication of a signal frequency (ω_s) by the first LO (ω_{LO1}). This could be represented by

$$\cos(\omega_s t) \cdot \cos(\omega_{LO1} t) = \frac{\cos(\omega_s + \omega_{LO1})t}{2} + \frac{\cos(\omega_s - \omega_{LO1})t}{2}. \tag{3.33}$$

The first term in the frequency summation above is filtered out by a bandpass filter,

and the second term is the first intermediate frequency (IF_1). Note that signal spectra ω_s located one IF_1 above or below ω_{LO1} are mixed down to the same frequency. The bands offset above and below the LO frequency by the intermediate frequency (IF_1 in this case) are the (desired) RF signal band and the image band. Power in the image band must therefore be attenuated prior to downconversion by the first mixer in order to prevent interference with the RF signal because both signals share the same IF (i.e., IF_1). This is accomplished by the image-reject filter shown in Figure 3.6.

A lower value for IF_1 favors the performance of the IF_1 amplifier and 2nd mixer but demands a higher quality factor from the image-reject filter. This is because the signal and image frequencies are drawn closer to one another. High-Q passive filtering is not compatible with silicon technology. It also requires external components, and introduces insertion loss [3.28]. This loss must be compensated for by a higher LNA gain and power consumption.

It is necessary to determine the image frequency in an FMCW radar receiver application in which the RF and LO frequencies vary with time. With a heterodyne topology, the frequency of LO_1 is a scaled-down version of the Tx carrier as given by Eqt. (3.32). The overall frequency profiles at RF are illustrated in Figure 3.7(a). The IF_1 trajectory with time shown in Figure 3.7(b) will converge to the same result as in Figure 3.2 after the down-conversion to the second IF. Without the image-reject filter, interference at the image frequency is indistinguishable from the echo from a potential target. This, however, will not deteriorate the false alarm rate for radar detection in a practical situation as explained in the following paragraph.

An FMCW radar makes a valid detection only if the IF, which is the instantaneous frequency difference between the Tx and Rx waveforms, remain stable during one modulation period of T_m. As observed in Figure 3.7(a), this condition can only be satisfied by a triangular shaped frequency profile for the Rx. The image frequency band for the first down-conversion is at $\omega_{LO1} - \omega_{IF1} = 2\omega_{LO1} - \omega_{RX}$, and has a trapezoidal shaped profile. Because the possibility of having an interfering source with a frequency profile that closely follows the image band as in Figure 3.7(a) is very small (i.e., close to zero), image rejection is not a significant problem for a heterodyne receiver.

However, occasional interference in the image band could disturb the FMCW radar detection process. Attenuation of signal power in the image band is still necessary. This is achieved by proper selection of the first LO frequency, as well as taking advantage of the finite receiver antenna directivity, and limited bandwidth of the LNA RF power gain and input return loss. In addition, undesired tones down-converted to IF may be removed by signal averaging, as long as these tones are not synchronous with the triangular Rx carrier and do not have the necessary trapezoidal frequency profile described previously.

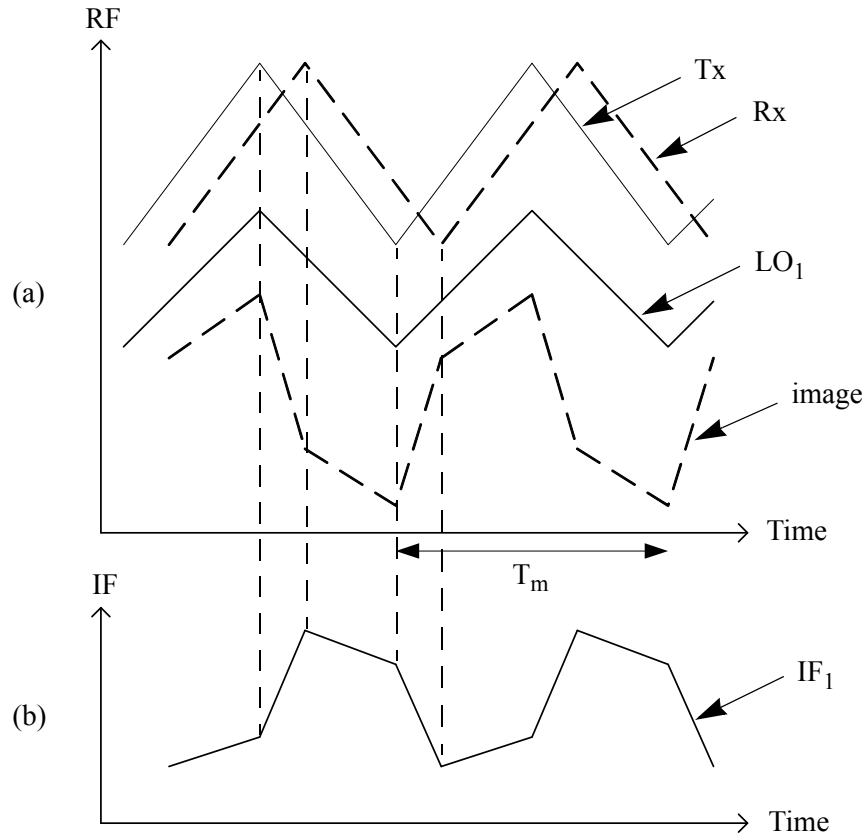

Figure 3.7 FMCW radar (a) RF and (b) IF profiles on the same time axis for a heterodyne receiver

3.4 Design Example

A design example is presented in this section which illustrates the optimization of system performance based upon circuit building block parameters.

3.4.1 Functional Requirements

SRR applications for consumer electronics products are expected to be limited to range measurement of static or slowly moving objects. Radar sensing for industrial automation imposes additional requirements, such as operating under high temperature and high pressure conditions [3.29]. For automotive collision avoidance radar, short-range detection at distances between 0.5m and 10m around a vehicle with multiple radar units provides adequate safety distance against stationary objects such as trees or road lamps, slow moving objects such as pedestrians or bicycles, and nearby vehicles with low relative velocity. A range resolution of 5cm is necessary for rear and forward parking aids. The maximum relative velocity requirement is assumed to be 8.33m/s (30km/hr) and with a resolution of 0.5m/s. This is suffi-

cient to track cyclists and vehicles at the rear and in adjacent lanes for blind spot detection. These SRR functional requirements could be satisfied by an FMCW radar operating in the 24GHz band.

3.4.2 FMCW Radar System Parameters

The radar parameters could be determined from the equations derived in Section 3.1.1. A 5cm range resolution requires 3.00GHz of spectrum spanning from 22.5GHz to 25.5GHz as predicted by Eqt. (3.4). A velocity resolution of 0.5m/s takes 25.0ms for the modulation period from Eqt. (3.14). The specified maximum detectable velocity of 8.33m/s satisfies the assumption made in Eqt. (3.8) that the velocity must be much lower than 800m/s. The frequencies detectable at IF which correspond to a target located at minimum and maximum range are 801Hz and 16.0kHz, respectively, as derived from Eqt. (3.2). Relative velocity is obtained by resolving the Doppler shift at the IF. For a maximum speed of 8.33m/s, the absolute frequency shift in each half of the modulation period is 1.33kHz, as given in Eqts. (3.10) and (3.11). The SRR functional requirements and FMCW radar system parameters are summarized in Table 3.1.

3.4.3 Transceiver Specifications

With the –41.3dBm/MHz radiation limit for both FCC and ETSI standards, the transmitted signal power is –6.53dBm over the 3GHz bandwidth. Assuming that the azimuth and elevation beamwidth are both +/– 90° wide, which gives an antenna gain of $-10\cdot\log_{10}(180/360)^2 = 3.0$dB, the average power required from the PA is –3.53dBm, as derived in Eqt. (3.15).

Assuming the same receiver antenna gain as the transmitter, and for a typical radar cross section of 1m^2 (e.g., 56.5cm radius sphere), the received power in dBm is

$$P_r(dBm) = -64.5(dBm) - 40\cdot\log R\,(dB)\,, \tag{3.34}$$

where R is the target range as given by Eqt. (3.20). This power varies from

Table 3.1 SRR functional requirements and FMCW radar system parameters

Detection range	0.5 – 10 m
Range resolution	5 cm
Relative velocity	0 – 8.33 m/s
Velocity resolution	0.5 m/s
Frequency range	22.5 – 25.5 GHz
Modulation period	25.0 ms
Frequency detectable IF	0.801 – 16 kHz
Doppler shift	0 – 1330 Hz

–104.5dBm to –52.5dBm for ranges of 10m and 0.5m, respectively. Assuming a 20dB safety margin in the receiver at the maximum power level, the receiver input –1dB compression point should be higher than –32.5dBm.

The receiver must amplify the received signal to a voltage range which maximizes the ADC SNR performance. For a 1V supply, a signal swing of 0.632V peak-to-peak across a 10kΩ impedance is equivalent to –23dBm. Therefore, the required receiver power gain is between 81.5dB and 29.5dB. The worst-case signal-to-noise ratio comes at the minimum received power in Eqt. (3.23). At room temperature, the minimum receiver output SNR is related to the noise figure (NF) by

$$SNR_{\text{out\_IF(min)}}(dB) = -104.5(dBm) - (-127)(dBm) - NF(dB) . \qquad (3.35)$$

The first and second terms in Eqt. (3.35) correspond to the signal and noise powers, respectively. A 30kHz margin at the IF is allocated on top of the maximum frequency specified in Table 3.1 to account for the finite out-of-band noise attenuation from the IF filter. The receiver NF should be less than 11.55dB in order to meet the required SNR of 10.95dB. Averaging N consecutive samples improves the SNR by $10 \cdot \log N(\text{dB})$, as indicated in Eqt. (3.24). The receiver noise figure required is relaxed by the same amount.

The third-order non-linearity is specified by Eqt. (3.27). Given the worst-case situation, where two interfering (in-band) transmitters are separated by 1m from the radar receiver and have line-of-sight propagation paths, the interference power level is –64.5dBm. The IIP_3 required is –34.4dBm for 0.5dB SNR degradation due to third-order intermodulation corresponding to $M = 0.122$ in Eqt. (3.27).

Reduction of the phase noise power depends on the target range and the offset frequency relative to the corresponding IF, as presented in Eqt. (3.29). With potential targets positioned at 0.5m and 10m range, their phase noise reduction factors are –111dB and –85.1dB, respectively, given the frequency difference at IF of 15.2kHz. Because the nearest target returns an echo power which is 52dB stronger than the distant one, while its phase noise reduction is only 25.9dB better, it is clear that the furthest target suffers most from SNR degradation due to phase noise from the nearest target.

For a modulation period of 25ms, the integration limits given in Eqt. (3.30) are from 503Hz to 16kHz. With the wideband VCO embedded into a PLL, this frequency range should lie within the PLL loop bandwidth. The phase noise in this band is then dominated by the reference oscillator and the frequency division ratio, and is much better than the value obtainable from a free-running oscillator [3.30]. However, the worst-case situation is assumed in the calculation in order to have a pessimistic estimate for the phase noise specification. By taking the uppermost interference signal power of –52.5dBm, the lower-bound phase noise reduction factor of 111dB, and a flat phase noise PSD of –20dBc/Hz up to an frequency offset of 15.2kHz, the total phase noise power integrated from 503Hz to 16kHz is –142dBm.

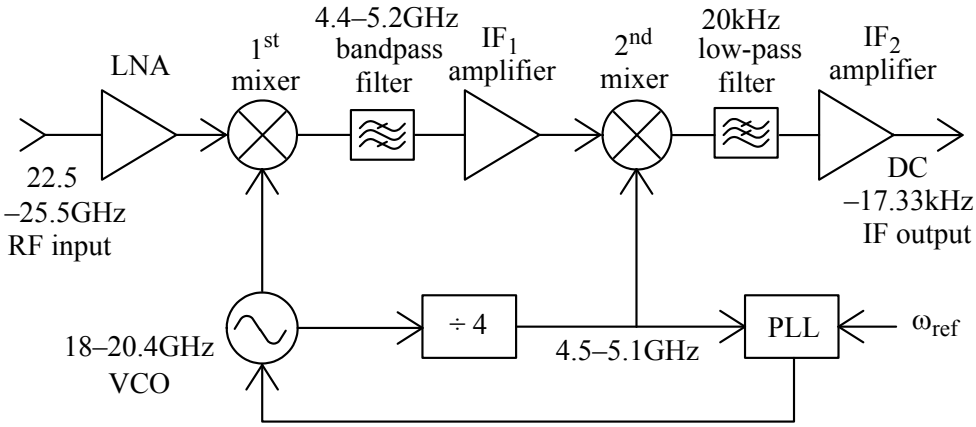

Figure 3.8 Proposed heterodyne FMCW SRR receiver

On the other hand, the thermal noise power in the SNR calculation of Eqt. (3.23) is about –116dBm. Assuming a phase noise slope of –20dB/dec, applying a free-running VCO with phase noise of –60dBc/Hz at 1.52MHz frequency offset on the FMCW receiver will have negligible effect on the received signal SNR.

The proposed heterodyne SRR receiver is shown in Figure 3.8. Frequency planning is chosen with the first down-conversion centered at 4.8GHz. This has an advantage of simplifying the LO generation where a single LO tuned from 18GHz to 20.4GHz is combined with a divide-by-four circuit, which is part of the PLL with reference frequency ω_{ref}. The phase noise influence from the divided-LO is insignificant because its noise level is 12dB lower than the main VCO phase noise. The image lies 9.6GHz away from the RF signal. Assuming that the interference from the image band has the same power level as the desired sign, 20dB of image attenuation from the LNA in addition to finite antenna bandwidth and the use of a directional antenna could obviate the need for image-reject filtering. The 4.4GHz to 5.2GHz bandpass filter at IF_1 could be embedded into a tuned circuit loading the 1st mixer or the first IF amplifier. It attenuates the undesirable output from the first down-conversion mixer, including DC offset, VCO leakage, and up-converted mixing products, which are separated from the average value of IF_1 by 4.8GHz, 14.4GHz, and 38.4GHz, respectively. The second mixer translates the signal spectrum to the final IF and a low-pass filter limits the noise bandwidth prior to demodulation to determine the target range and velocity information. A summary of the transceiver specifications is given in Table 3.2.

3.4.4 Building Block Specifications

The proposed radar receiver shown in Figure 3.8 is a cascade of seven stages, namely: the LNA, 1st mixer, bandpass filter, first IF amplifier, 2nd mixer, low-pass filter, and second IF amplifier. The overall receiver gain is the sum of each individ-

Table 3.2 Proposed transceiver electrical specifications

Tx power	–3.53 dBm
Antenna gain	3.0 dB
Maximum Rx power	–52.5 dBm
Minimum Rx power	–104.5 dBm
Rx power gain	29.5 – 81.5 dB
Image rejection	20 dB
Noise figure (w/o co-integration)	11.55 dB
Input –1dB compression point	–32.5 dBm
Input third-order intercept point	–34.4 dBm
VCO frequency tuning range	18.0 – 20.4 GHz
VCO phase noise	–56.6 dBc/Hz@1MHz
RF	22.5 – 25.5 GHz
IF_1	4.4 – 5.2 GHz
IF_2	0 – 17.33 kHz

ual block gains in decibels. The noise figure of cascaded stages is described by Friis' equation [as given in Eqt. (2.22)], which gives

$$F = F_1 + \frac{F_2 - 1}{G_{a1}} + \frac{F_3 - 1}{G_{a1}G_{a2}} + \ldots + \frac{F_7 - 1}{G_{a1}G_{a2}G_{a3}G_{a4}G_{a5}G_{a6}}, \tag{3.36}$$

where F_m and G_{am} are the noise factor and available power gain of the m^{th} stage, respectively. With reference to Eqt. (2.23), the cascaded input third-order intercept point is determined from

$$\frac{1}{A_{\text{IIP3}}} \approx \frac{1}{A_{1,\text{IIP3}}} + \frac{G_{p1}}{A_{2,\text{IIP3}}} + \frac{G_{p1}G_{p2}}{A_{3,\text{IIP3}}} + \ldots + \frac{G_{p1}G_{p2}G_{p3}G_{p4}G_{p5}G_{p6}}{A_{7,\text{IIP3}}}, \tag{3.37}$$

where $A_{m,\text{IIP3}}$ and G_{pm} are the input third-order intercept point and operating power gain of the m^{th} stage, respectively.

Manipulation of Eqts. (3.36) and (3.37) across 7 stages to reach an optimum result is not obvious. A design tool from Avago Technologies [3.31] is therefore utilized to partition the receiver specifications into building block electrical specifications. The interdependence among the parameters of each block towards the overall receiver chain become visible. More importantly, the noise figure and input intercept point along the cascade chain are listed, which allows any system bottlenecks to be identified immediately.

The proposed radar receiver building block specifications are summarized in Figures 3.9 and 3.10 at the extreme gain settings. An assumption in the design

Stage Data	Units	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7
Stage Name:		LNA	1st Mixer	BPF	1st IF Amp	2nd Mixer	LPF	2nd IF Amp
Noise Figure	dB	5	20	3	10	15	30	30
Gain	dB	15	0	-3	30	0	-3	42.5
Input IP3	dBm	-10	-3	20	-10	20	20	10
Stage Analysis:		0	0	0	0	0	0	0
d NF/d NF	dB/dB	0.48	0.48	0.01	0.10	0.00	0.01	0.02
d IP3/d IP3	dBm/dBm	0.01	0.04	0.00	0.11	0.11	0.11	0.56

System Analysis:

Gain =	81.50	dB	Input IP3 =	-31.28	dBm
Noise Figure =	8.50	dB	Output IP3 =	50.22	dBm

Figure 3.9 Receiver specification partitioning for 81.5dB gain

tool is that the available and operating power gain are identical. Variable gain range is provided by the IF_1 and IF_2 amplifiers, which are tunable by 10dB and 42dB, respectively. The noise figures of these amplifiers are assumed to be constant versus gain tuning, but linearity (i.e., IIP_3) improves with a lower gain setting. In the high gain mode of 81.5dB, the overall noise figure is dominated by both the LNA and first mixer noise figures with the same sensitivity of 0.48dB/dB. On the other hand, linearity is limited primarily by the IF_2 amplifier, and secondarily by the IF_1 amplifier, second mixer and low-pass filter. This verifies the optimization process because the noise and linearity are limited by the preceding and following stages according to Eqts. (3.36) and (3.37), respectively.

In the low gain setting, the LNA and first mixer still dominate the overall noise figure, but it is less sensitive at 0.39dB/dB. Because of 10dB gain reduction from the IF_1 amplifier, the appearance of the low-pass filter and IF_2 amplifier noise figure is now becoming visible with sensitivity of 0.08dB/dB and 0.16dB/dB,

Stage Data	Units	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7
Stage Name:		LNA	1st Mixer	BPF	1st IF Amp	2nd Mixer	LPF	2nd IF Amp
Noise Figure	dB	5	20	3	10	15	30	30
Gain	dB	15	0	-3	20	0	-3	0.5
Input IP3	dBm	-10	-3	20	10	20	20	25
Stage Analysis:		0	0	0	0	0	0	0
d NF/d NF	dB/dB	0.39	0.39	0.01	0.08	0.00	0.08	0.16
d IP3/d IP3	dBm/dBm	0.08	0.55	0.00	0.01	0.13	0.13	0.02

System Analysis:

Gain =	29.50	dB	Input IP3 =	-20.38	dBm
Noise Figure =	9.44	dB	Output IP3 =	9.12	dBm

Figure 3.10 Receiver specification partitioning for 29.5dB gain

Table 3.3 SRR receiver building block electrical specifications

Block name	Gain (dB)	NF (dB)	IIP_3 (dBm)	P_{DC} (mW)
LNA	15	5	–10	3
First mixer	0	20	–3	2
BPF	–3	3	20	0
IF_1 amplifier	from 20 to 30	10	from 10 to –10	1
Second mixer	0	15	20	0
LPF	–3	30	20	0.5
IF_2 amplifier	from 0.5 to 42.5	30	from 25 to 10	0.5
VCO				5
PLL				3

respectively. The 0.94dB degradation in noise figure still meets the transceiver electrical specifications of 11.55dB with enough margin. The 10dB gain drop from the IF_1 amplifier reduces the IF_2 amplifier contribution to the system non-linearity as stated in Eqt. (3.37). Although the first mixer now becomes the major source of non-linearity, the overall IIP_3 improves by 10.9dB by benefiting from lower amplification in the cascade stages.

Table 3.3 summarizes the building block electrical specifications of the SRR receiver for a total power dissipation of 15mW. Two-thirds of the power budget is allocated to the front-end circuits (LNA + 1st mixer + VCO) which are running at the carrier frequency. The bandpass filter is implemented by the RLC parallel resonant tuned load of the 1st mixer. Given the noise, linearity requirements and a non-50Ω input interface impedance, circuit realizations with sub-mW power consumption exist in CMOS technology for both of the first IF [3.32] and second IF amplifiers [3.33], where the maximum IF_1 and IF_2 are 5.2GHz and 17.33kHz, respectively. The 2nd mixer favors a passive implementation because of flicker noise and power dissipation considerations [3.34]. The large LO drive necessary for this mixer in order to lower the noise figure and non-linearity distortion could be realized at low power consumption by absorbing the mixer MOSFET gate capacitance into the frequency divider LC resonant tank centered at 4.8GHz. The low-pass filter could be implemented as an op-amp based higher-order active RC structure [3.35] with a cut-off frequency of 18kHz. The VCO could be embedded into a PLL by reusing the 18GHz divide-by-8 injection-locked frequency divider in [3.36], and the 2GHz PLL in [3.37]. These circuits were demonstrated in a 0.18μm CMOS technology and their combined supply current is 2.17mA. Therefore, 3mW is reserved for the PLL circuitries (excluding VCO) in Table 3.3.

3.5 Summary

This chapter presented the system design aspects for a low-cost and low-power SRR in CMOS technology. The emphasis was on the selection of the radar configuration and receiver architecture. Link budget considerations defined the potential design challenges of the overall system and building blocks together with their specification requirements.

An FMCW radar is well suited to the SRR application with a continuous Tx and Rx operation. Keeping the IF in the lower frequency range takes advantage of VCO phase noise reduction and relaxes the processing bandwidth requirements from the decision circuitry.

A heterodyne receiver is no more expensive than its homodyne counterpart, because image rejection is not necessary for the FMCW SRR application. It offsets the VCO pulling problem with a two-step frequency down-conversion, and is free from the severe second-order non-linearity problems seen in FMCW radar. The VCO phase noise and tuning range requirements are also relaxed by operating at a lower frequency. The third-order non-linearity in the receiver is not seen as an performance limiting parameter because of the signal averaging across successive scanning periods.

The remaining design challenges for realizing the SRR receiver are power consumption and wideband capability for the LNA, the first down-conversion mixer, and the VCO. Their design and optimization are tackled in Chapters 4, 5, and 6 of this thesis.

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Chapter 4

Voltage-Controlled Oscillator

A varactor-based voltage-controlled oscillator (VCO) suffers from narrow frequency tuning range due to the trade-off between capacitance tuning ratio and quality factor (Q), and the decreasing capacitance Q with the operating frequency. In order to break through this design bottleneck, a dedicated transformer resonant tank in which the inductive component is a tunable parameter is proposed in this chapter. This enables varactorless tuning on the VCO frequency. Two testchips are implemented: a 23.2GHz to 29.4GHz VCO in 0.13μm CMOS as a proof of concept [4.1,4.2], and a 18.6GHz to 21.2GHz VCO in 90nm CMOS to be embedded in the low-power, short-range radar receiver.

The motivations of varactorless frequency tuning scheme are first presented. This is followed by the analysis of the frequency range limitations of continuous-tuned and frequency band-switched VCOs using varactors and switched-capacitor arrays, respectively. The proposed transconductor-tuned VCO, which uses an on-chip transformer and transconductance cell to realize continuous wideband frequency tuning, is then described. Finally, experimental results for the two prototype VCOs demonstrating wideband and adaptive tunability performance are presented.

4.1 Motivations

VCOs have typically used a voltage-controlled capacitor (i.e., varactor) to electrically control the resonant frequency of an LC tank, thereby allowing electronic tuning of the oscillation frequency. In contrast to operation below 10GHz, where inductor Q dominates losses in the on-chip tank, losses in a varactor implemented in production VLSI technologies (silicon CMOS or SiGe BiCMOS) tend to dominate resonant tank losses at millimeter-wave (mm-wave) frequencies (i.e., above 12.5GHz on a silicon chip). Since the equivalent tank impedance is proportional to the inductance-to-capacitance (L/C) ratio, only a relatively small capacitance can be used if high spectral purity is required from the VCO. In addition, there is a trade-off between the varactor Q and capacitance as its bias voltage varies from maximum to minimum (i.e., C_{max}/C_{min}). The C_{max}/C_{min} ratio is typically less than three at mm-wave frequencies. Also, parasitic capacitances of the transistors and the tank inductor limit the portion of the total tank capacitance that can be elec-

trically tuned. These three factors: limited total capacitance, available capacitance ratio and circuit parasitics, restrict the tuning range of a conventional LC VCO to less than 10% at approximately 20GHz [4.3,4.4] and less than 5% at 60GHz [4.5-4.7].

VCOs with 25% tuning range have been implemented using supply and tuning voltages at, or above 3V in SiGe BiCMOS (–5.6V and 4.5V in [4.8], and –5.5V and 3.0V in [4.9]) where a collector-base junction is used as a varactor diode [4.8], or in technologies featuring processing options for the varactor devices [4.9]. Also, VCOs implemented in silicon-on-insulator (SOI) CMOS technologies, where the parasitic capacitance for both active and passive devices is lower than in bulk CMOS, have demonstrated tunability over a wider frequency range [4.10-4.12]. However, either non-standard or dual-supply voltages increase system and component costs. Processing options for the varactor or implementation in SOI CMOS adds to the cost of the IC. Hence, a low-cost VCO intended for high volume short-range radar sensor applications should utilize only the components available in bulk CMOS technology.

The VCO electrical specifications for the SRR application are summarized in Table 4.1, which were derived from the system analysis presented in Chapter 3.

4.2 Varactor-Tuned VCOs

A generic varactor-tuned VCO capable of mm-wave frequency generation is shown in Figure 4.1. The frequency tuning network is a parallel LC resonant tank consisting of an integrated inductor (L_{load}) and associated capacitances. A differentially driven symmetric inductor is typically used to maximize Q factor and minimize chip area [4.13]. The total tank capacitance (C_{load}) consists of the continuous-tuned varactor C_v (e.g., an accumulation-mode MOS varactor for higher Q [4.14]), a band-switched capacitor array (C_m in series with switch S_w with parasitic C_{sw}), and a lumped parasitic C_{par}. The negative resistance synthesized by cross-coupled NMOS differential pair M_1 and M_2 cancels losses of the tank elements in order to sustain oscillation. A differential-pair amplifier M_3 and M_4 buffers the VCO output to drive subsequent stages, such as a frequency divider in a phase-locked loop and a mixer in a radio transceiver. Active devices M_1–M_4 make contributions to C_{par}. Parasitic capacitances limit the maximum oscillation frequency and tunability of the VCO, and therefore should be minimized.

Table 4.1 VCO electrical specifications

Frequency	Tuning range	Phase noise	P_{DC}
18.0–20.4GHz	12.5%	–56.6dBc/Hz@1MHz	5mW

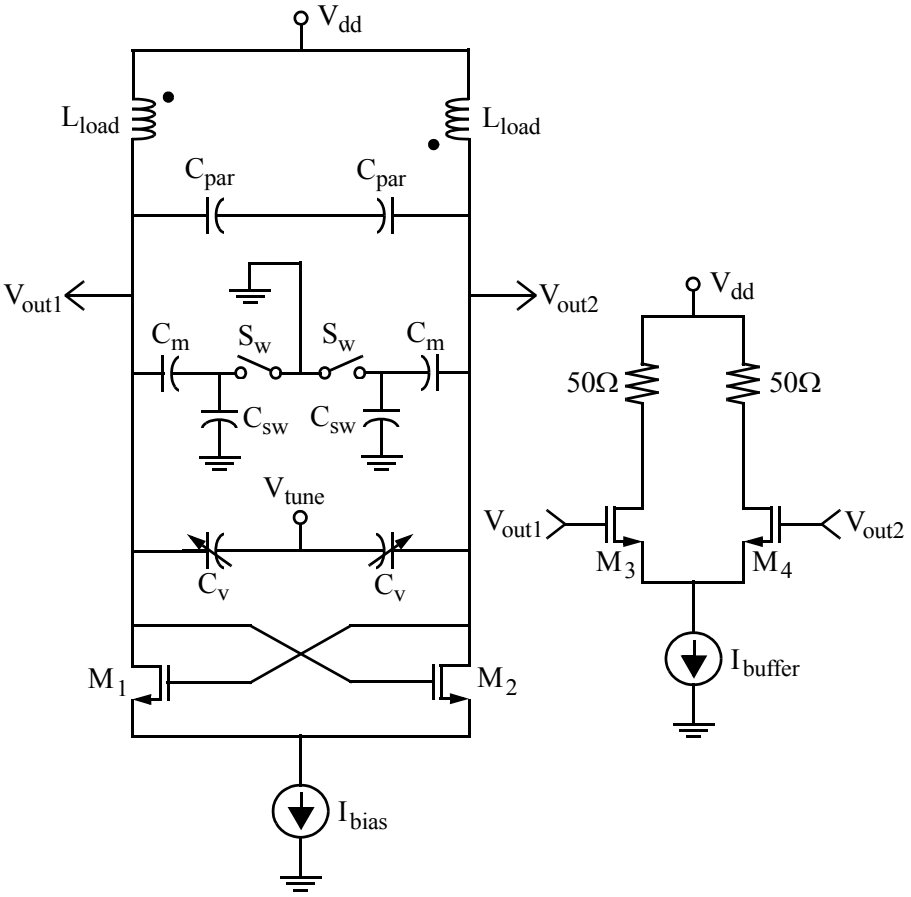

Figure 4.1 Generic varactor-tuned VCO

For the LC tank formed by inductor L_{load} and the total capacitance seen across the tank C_{load}, the equivalent tank impedance at the parallel resonant frequency is given by

$$R_{tank} = \sqrt{\frac{L_{load}}{C_{load}}} \cdot \frac{Q_L Q_C}{Q_L + Q_C}, \tag{4.1}$$

where Q_L and Q_C are the load inductor and load capacitor Q factors, respectively.

The tank losses represented by R_{tank} are compensated for by the negative resistance cell of the oscillator, which must have a transconductance

$$g_m > \frac{1}{R_{tank}} = \sqrt{\frac{C_{load}}{L_{load}}} \cdot \frac{Q_L + Q_C}{Q_L Q_C}. \tag{4.2}$$

In a VCO designed for low power consumption (which implies low transconductance), the quality factors of L_{load} and C_{load} (Q_L and Q_C, respectively)

and the tank inductance-to-capacitance ratio (L_{load}/C_{load}) in Eqt. (4.2) are maximized [4.15,4.16]. However, for a given tuning range, the L_{load}/C_{load} ratio is constrained by the maximum size of the tank tuning capacitor. In addition, transistor and other component parasitics (e.g., loading from the output buffer) increase C_{load} and limit the L_{load}/C_{load} ratio. As a quantitative example, a VCO with a tank inductance of 0.15nH requires a total tank capacitance of 250fF for oscillation at 26GHz. For a 0.13μm CMOS technology, the parasitics across the tank are summarized in Table 4.2.

After accounting for the cross-coupled NMOS differential pair (122fF), the gate capacitance of a common-source output buffer (40fF) and estimated wiring and inductor parasitics of 40fF, there is only 48fF remaining for the varactor capacitance. The ratio of parasitic to varactor capacitance is 4.3 in this example, as the total parasitic is much larger than the varactor capacitance. Thus, one can see that circuit parasitics impose a fundamental limit on the usable range of conventional VCOs implemented in bulk CMOS.

The Q factors of the varactor and capacitive parasitics are inversely proportional to frequency and are affected by interconnect resistance, the resistance of diffused junctions, and losses in the semiconductor bulk. For example, the capacitance and corresponding Q factor for an accumulation-mode varactor with $20\times 2\mu m$ finger width in a 0.13μm CMOS technology from simulations are shown in Figure 4.2. The series resistance and capacitance are extracted from the real and imaginary parts of the simulated Y-parameters, respectively. As the length of each varactor finger is varied from 0.24μm to 0.5μm, it can be seen that the C_{max}/C_{min} ratio increases from 3.7 to 4.9 with increasing gate length. For longer fingers (e.g., 0.5μm), the C_{max}/C_{min} ratio decreases with frequency because the larger channel resistance narrows the bandwidth of the device.

The varactor C_{max}/C_{min} ratio for each case shown in Figure 4.2 assumes a varactor bias voltage ranging from –1V to 1.2V. However, the bias across the varactor is typically bounded by the power supply voltage (i.e., between 0V and V_{dd}) as

Table 4.2 Capacitive loading for a 26GHz NMOS VCO in 0.13μm CMOS

Circuit Function	Capacitive Loading
Cross-coupled NMOS pair synthesizing –130Ω (30μm wide transistor biased at 10mA)	122fF
NMOS output buffer parasitic (30μm wide transistor)	40fF
Wiring and inductor parasitics	40fF
Varactor	48fF
Total tank capacitance	250fF

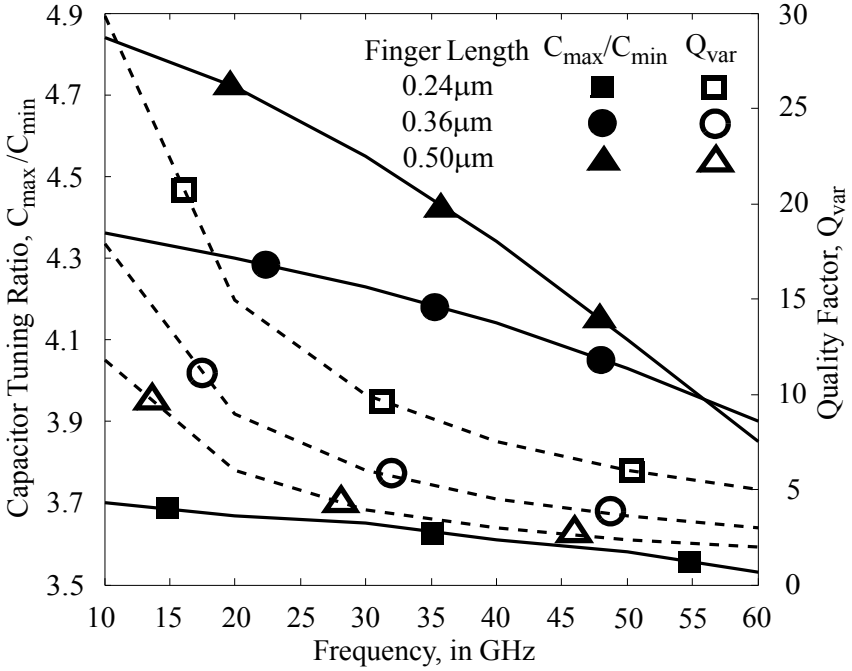

Figure 4.2 C_{max}/C_{min} ratio and the minimum Q factor of a $20\times2\mu m$ accumulation mode varactor versus frequency

for the varactor-tuned VCO of Figure 4.1. Otherwise, a second supply voltage is required. In such cases, the capacitor tuning ratio C_{max}/C_{min} from the previous example is limited to about 1.4 for the three finger lengths considered. In practice, the capacitor tuning ratio is larger than this because the large-signal output causes the varactor bias voltage and its instantaneous capacitance to vary every oscillation cycle [4.17,4.18]. The effective capacitance is a time average of the instantaneous capacitance, and in this example the effective C_{max}/C_{min} ratio lies between 1.4 and the values presented in Figure 4.2.

The Q factor of the varactor (Q_{var}) decreases with increasing finger length and frequency, as seen in Figure 4.2 (i.e., from 30 at 10GHz to 5 at 60GHz for a gate length of 0.24μm). Active devices connected to the VCO tank also lower its Q and (typically) add parasitic capacitance on the order of tens of femtofarads, thereby limiting the maximum frequency of oscillation and the tuning range of the VCO.

Band-switched capacitor arrays (e.g., capacitor C_m and switch S_w in Figure 4.1) are often used to increase or decrease the tank capacitance and widen the tuning range of the VCO [4.19,4.20]. Digital control of the switches in the capacitor array permits coarse tuning of the VCO frequency, thereby constraining the frequency range controlled by the varactor capacitance. This lowers the tuning sensitivity of the VCO and relaxes the trade-off between tuning range and VCO phase noise. Simulations predict that the Q factor of a 50fF MIM band-switching capacitor decreases

from 27 at 10GHz, to 9.3 at 30GHz, and to 5 at 60GHz for a switch transistor width of $40\times(1\mu m/0.12\mu m)$. The Q factor would be reduced further for a smaller transistor width. The capacitance ratio for this band-switching capacitor being turned on and off is only 2.1. Thus, the switched MIM capacitor has limitations in capacitive tuning ratio and Q factor that are similar to a varactor in bulk CMOS.

The predicted VCO oscillation frequency is

$$\omega_o = 1/(\sqrt{L_{load}\cdot(C_v + C_{par})}), \tag{4.3}$$

where C_{par} is the sum of parasitic capacitances, and varactor capacitance (C_v) is constrained by the relationships $C_{min} \le C_v \le C_{max}$. Given the limited C_{max}/C_{min} ratio and the C_{par} added by transistors and (possibly) band-switching capacitors, a poor frequency tuning range is expected at mm-wave frequencies. By substituting C_v in Eqt. (4.3) for either C_{min} or C_{max}, the VCO tuning range is given by

$$\begin{aligned}\text{Tuning Range (\%)} &= 200\cdot\frac{\omega_{o,max}-\omega_{o,min}}{\omega_{o,max}+\omega_{o,min}} \\ &= 200\cdot\frac{(\sqrt{C_{min}+C_{par}})^{-1}-(\sqrt{C_{max}+C_{par}})^{-1}}{(\sqrt{C_{min}+C_{par}})^{-1}+(\sqrt{C_{max}+C_{par}})^{-1}},\end{aligned} \tag{4.4}$$

where $\omega_{o,max}$ and $\omega_{o,min}$ are the maximum (i.e., $C_v = C_{min}$) and minimum (i.e., $C_v = C_{max}$) oscillation frequencies, respectively. Figure 4.3 plots this tuning range

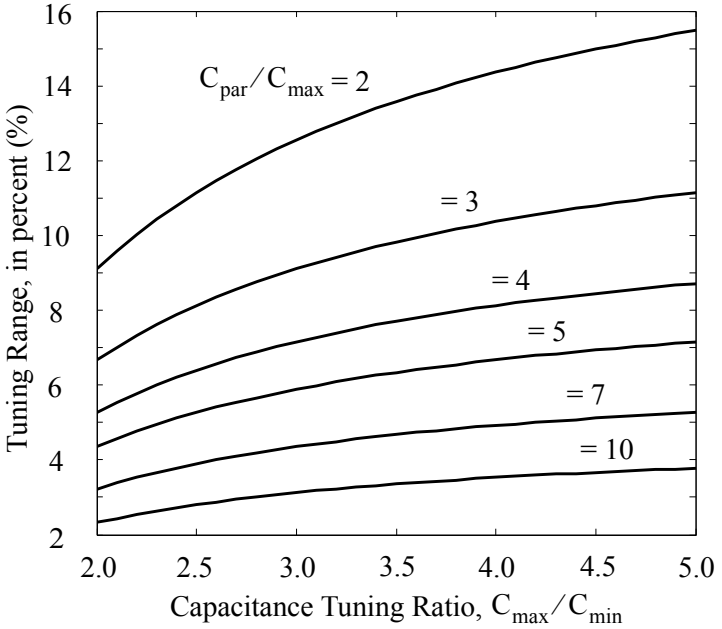

Figure 4.3 Frequency tuning range versus capacitance tuning ratio (C_{max}/C_{min}) and parasitic to maximum varactor capacitance (C_{par}/C_{max})

versus C_{max}/C_{min} against an increase of C_{par}/C_{max} from 2 to 10. As noted previously, the varactor C_{max}/C_{min} is defined by the supply voltage and must be traded off against the Q factor, resulting in a phase noise versus tuning range trade-off. In addition, low-Q components require more gain to overcome tank losses, leading to an increase in power consumption and C_{par}/C_{max} ratio at higher operating frequencies. For a C_{max}/C_{min} of 3, the tuning range decreases from 12.6% to 4.3% for C_{par}/C_{max} ratios of 2 and 7, respectively.

4.3 Transconductor-Tuned VCO

The varactorless LC tank exploits the voltage and current relationships of a transconductor cell within a dedicated transformer resonant tank. A generic transconductor-tuned LC tank is shown in Figure 4.4. By representing the transformer with an equivalent T-model consists of L_1, L_2, and L_3 [4.21], the tank can be visualized as a simple LC circuit in which inductor L_1 is in series with L_2 and the capacitor is C_{tank}, where C_{tank} represents all of the parasitic capacitance appearing across the tank. A tuning network tapping at the mid-point of the inductor coil consists of inductor L_3 in series with a parallel combination of R_L, C_L, and transconductor G_m. This G_m has a terminal voltage V_{g2} and is controlled by the voltage V_{g1}. With the impedance Z_g at the G_m output terminal, it can be shown that

$$Z_g = (1/G_m) \cdot (V_{g2}/V_{g1}). \tag{4.5}$$

For the resonant tank shown in Figure 4.4, the relationship between V_{g1} and V_{g2} can be obtained by applying Kirchhoff's law around the two voltage loops con-

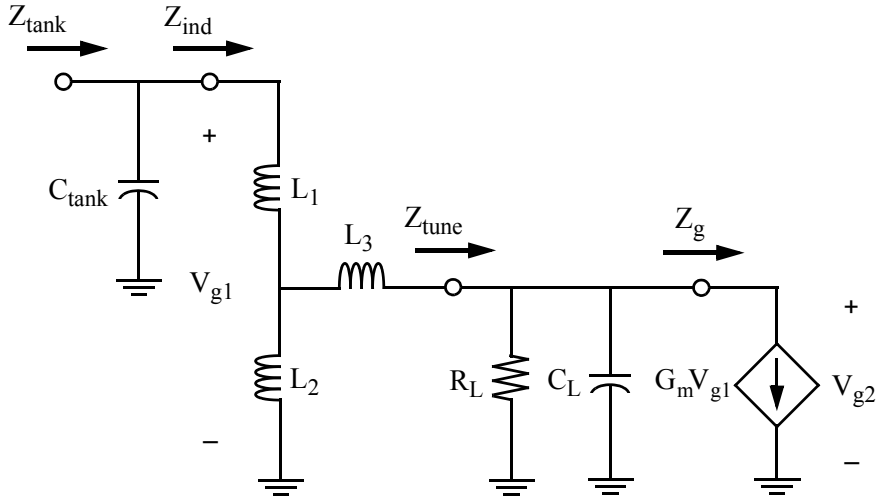

Figure 4.4 Generic transconductor-tuned resonant tank

sist of V_{g1}, L_1, L_2; and L_2, L_3, Z_{tune}. It is given by

$$\frac{V_{g2}(s)}{V_{g1}(s)} = \frac{1-\left(1+\frac{L_1}{L_2}+\frac{L_1}{L_3}\right)sL_3G_m}{\left(1+\frac{L_1}{L_2}\right)+\left(1+\frac{L_1}{L_2}+\frac{L_1}{L_3}\right)sL_3\left(\frac{1+sR_LC_L}{R_L}\right)}. \tag{4.6}$$

In sinusoidal steady state and with $G_m = 0$, the series tank consisting of inductor L_3 and capacitor C_L tapping at the mid-point of L_1 and L_2 causes V_{g2}/V_{g1} to have a phase shift of 90° at a frequency of

$$\omega_{90^\circ} = \frac{1}{\sqrt{L_3C_L}} \cdot \sqrt{\frac{1+L_1/L_2}{1+L_1/L_2+L_1/L_3}}. \tag{4.7}$$

The quality factor of the second-order transfer function in the denominator of Eqt. (4.6) governs the slope of the phase shift of V_{g2}/V_{g1} at the resonant frequency. It is given by

$$Q_{\text{series}} = \omega_{90^\circ} \cdot R_LC_L = R_L \cdot \sqrt{\frac{C_L}{L_3}} \cdot \sqrt{\frac{1+L_1/L_2}{1+L_1/L_2+L_1/L_3}}. \tag{4.8}$$

The resistor R_L in parallel with C_L lowers the quality factor of the series tank, and widens the band over which voltages V_{g1} and V_{g2} have approximately 90° difference in phase. Simulations show a resistor placed in series with L_3 could result in similar behavior. For the inductance values of L_1, L_2, and L_3 of 120pH each with a Q of 15 at 26GHz, capacitor C_L of 170fF, and transconductance of zero siemens, the magnitude and phase response of V_{g2}/V_{g1} is shown in Figure 4.5 for different R_L values. As shown in Figure 4.5, a small value of R_L gives a phase response closest to 90° across the widest bandwidth. It also has a flatter magnitude response compared with larger R_L values.

The numerator of Eqt. (4.6) gives a zero in the characteristic of V_{g2}/V_{g1} at

$$\omega_{\text{zero}} = \frac{1}{L_3G_m} \cdot \frac{1}{1+L_1/L_2+L_1/L_3}, \tag{4.9}$$

which is inversely proportional to G_m. With a transconductance of zero siemens, ω_{zero} locates at infinite frequency and has no effect on the characteristics shown in Figure 4.5. Depending upon whether G_m is positive or negative, ω_{zero} moves from the right-hand-side to the left-hand-side of the s-plane [4.22], and subsequently contributes a negative or positive phase shift to the phase response of Eqt. (4.6), respectively. The frequency in which V_{g2}/V_{g1} maintains approximately 90° difference in phase is altered by the location of ω_{zero}. Therefore, G_m continuously controls the magnitude and phase of impedance Z_g in Eqt. (4.5).

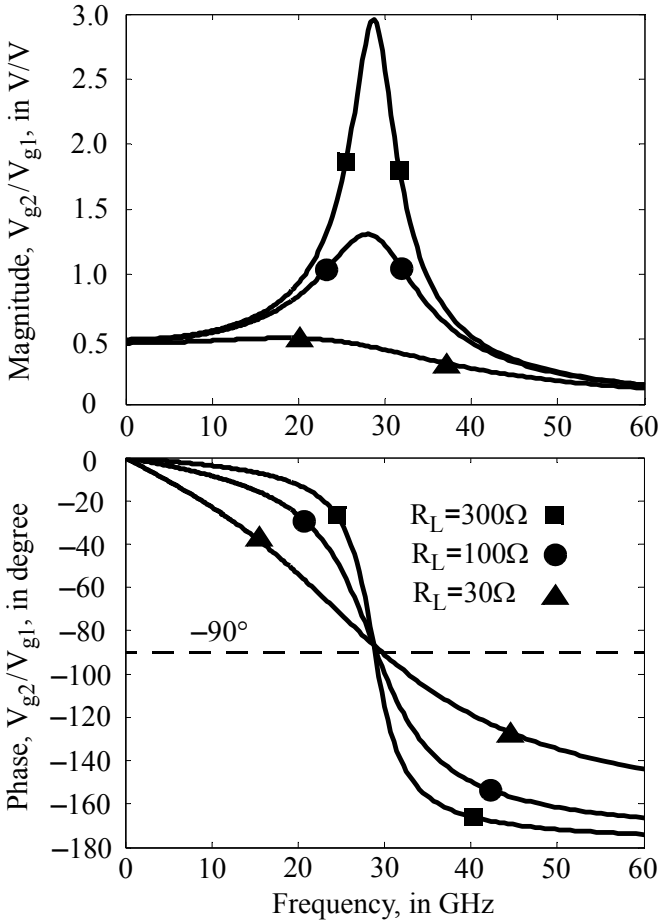

Figure 4.5 Magnitude and phase responses of V_{g2}/V_{g1} for different R_L values

By evaluating Z_{tune} as a parallel combination of Z_g, C_L, and R_L, and substituting Eqt. (4.6) into Eqt. (4.5), it can be found that

$$Z_{\text{tune}} = \frac{R_L\left[1 - sL_3G_m\left(1 + \frac{L_1}{L_2} + \frac{L_1}{L_3}\right)\right]}{sR_LC_L + G_mR_L\left(1 + \frac{L_1}{L_2}\right) + 1}. \tag{4.10}$$

With $G_m = 0$, Eqt. (4.10) is simplified as the impedance of a simple parallel RC circuit. By substituting s with $j\omega$ in Eqt. (4.10) (i.e., sinusoidal steady state), and assuming $|G_mR_L(1 + L_1/L_2)| \ll 1$, the imaginary part of Z_{tune} is calculated as

$$\text{Im}(Z_{\text{tune}}) = -\frac{R_L^2C_L + G_mL_3R_L(1 + L_1/L_2 + L_1/L_3)}{\omega R_L^2C_L^2 + 1/\omega}. \tag{4.11}$$

It is obvious that Z_{tune} is a capacitive impedance, and its value is tunable by the value of G_m. Because Z_{tune} is in series with L_3 which taps in the mid-point of inductors L_1 and L_2, the overall inductive impedance (Z_{ind}) of the LC tank and the parallel resonant frequency of the tank impedance (Z_{tank}) becomes tunable with G_m.

The trade-off between frequency tuning range and tank quality factor (Q_{tank}) is best visualized from simulation of the tank in Figure 4.4 with practical component values. The nominal resonant frequency is designed to be 26GHz. Using the same L_1, L_2, L_3, and C_L component values as in Figure 4.5 (capacitor C_L is selected after an optimization by taking account of the inductance values), and assuming a parasitic capacitance C_{tank} of 200fF and the transconductance (G_m) ranges from –20mS to +20mS, Figure 4.6 presents the simulated frequency tuning range and minimum Q_{tank} across the tuning range for different R_L values. As shown in Figure 4.6, a small R_L gives a small tuning range but a high Q_{tank}. This is because R_L is in series with L_3 (as shown in Figure 4.4), and a small R_L increases the Q of L_3, giving a higher Q_{tank}. However, a small R_L also shunts the output of the transconductance cell to ground. This diminishes the effect of the transconductor and narrows the frequency tuning range. It is important to observe that, for R_L equal to zero, the tank becomes untunable, and Q_{tank} is the same as the Q of L_1 to L_3. Also, a large R_L cannot maintain the 90° phase shift across a wide frequency band. With R_L of 200Ω (as in the previous example), the resonant peak at 26GHz flattens out and Z_{tank} shows two resonant frequencies: one below 26GHz and one above 26GHz. This makes the tank circuit unsuitable for VCO applications.

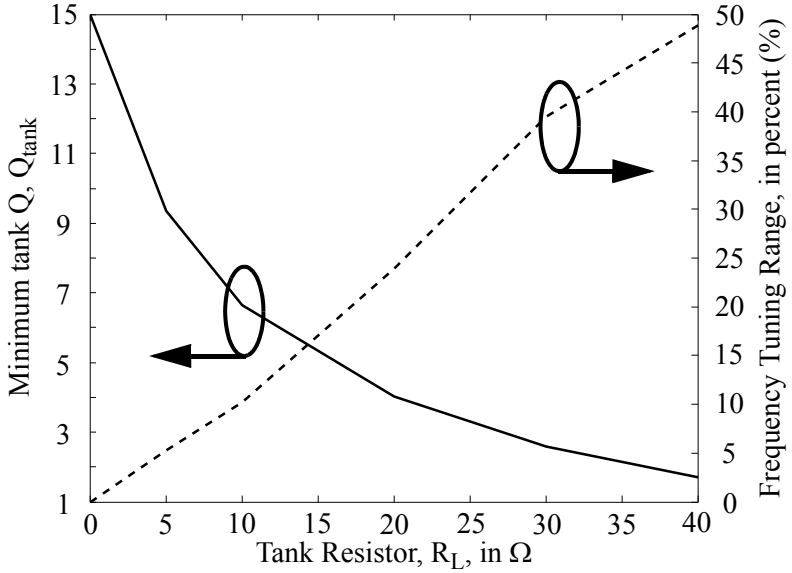

Figure 4.6 Simulated frequency tuning range and tank Q versus different R_L values for a resonant frequency at 26GHz

The large-signal and nonlinear operations of an oscillator introduce noise shaping on the circuit device noises into phase noise [4.23], with the noise power density described by the Leeson's formula in Section 2.3. For the generic varactor-tuned VCO illustrated in Figure 4.1, the dominant noise source is the drain current thermal noise power from transistor M_1 and M_2 ($\overline{i_{M1,2}^2}$). Additional current noise sources presented in the transconductor-tuned resonant tank include noise from resistor R_L and transconductor G_m as illustrated in Figure 4.7. The total amount of current noise power injected at node X is

$$\begin{aligned} \overline{i_X^2} &= \overline{i_{RL}^2} + \overline{i_{Gm}^2} + (\overline{i_{M1,2}^2} \cdot |Z_{\text{tank}}|^2) \cdot G_m^2 \\ &= \overline{i_{RL}^2} + \overline{i_{Gm}^2} + (G_m / G_{m1,2})^2 \cdot \overline{i_{M1,2}^2} \quad , \end{aligned} \tag{4.12}$$

where $G_{m1,2}$ is the transconductance of M_1–M_2. Assumption of $|Z_{\text{tank}}| = 1/G_{m1,2}$ is valid because unity loop gain is required to maintain the oscillation as expressed in Eqt. (4.2). Component parameters used in the designed VCO give $G_m \approx G_{m1,2}$ and $\overline{i_{M1,2}^2} \gg \overline{i_{RL}^2}$. Therefore $\overline{i_X^2}$ is about two times larger than $\overline{i_{M1,2}^2}$.

At the resonant frequency, impedance at node X ($|Z_X|$) is lower than that at the input port of the transformer tank ($|Z_{\text{tank}}|$). With the same component values used in Figure 4.6 and setting $R_L = 30\Omega$, simulation predicts the impedance ratio between $|Z_{\text{tank}}|$ and $|Z_X|$ is about 6.64 at 26GHz. The influence of $\overline{i_X^2}$ on the VCO phase noise power density is scaled down by the same factor. Therefore, $\overline{i_X^2}$ raises the current noise power injected into the transconductor-tuned VCO by a factor approximately equal to $2 / 6.64 = +30\%$.

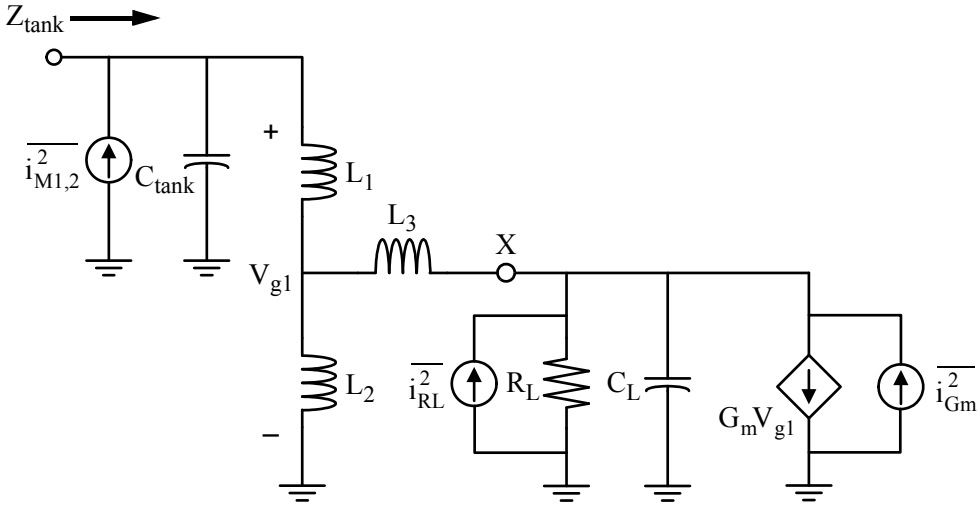

Figure 4.7 Noise sources presents in a transconductor-tuned resonant tank

4.4 First Testchip: 23.2-to-29.4GHz VCO

A 26.3GHz VCO with tuning range between 23.2GHz and 29.4GHz, and power consumption of 36.5mW is first demonstrated in a 0.13µm CMOS technology as a proof of concept of the transconductor-tuned resonant tank [4.1,4.2].

4.4.1 Circuit Design

A simplified schematic of a fully symmetric VCO is shown in Figure 4.8. Inductors L_1, L_2, and L_3 (from Figure 4.4) are a T-model equivalent for the on-chip transformer T_L used in the tank. Thus, the three independent inductor coils are implemented as a single transformer, requiring less chip area and reducing unintended signal coupling between on-chip coils.

The negative resistance cell is implemented using the cross-coupled NMOS differential pair M_1 and M_2. Resistor R_L is set at 30Ω which gives a simulated minimum Q_{tank} of 2.7 (at 26GHz) across the tuning range with the tuning transconduc-

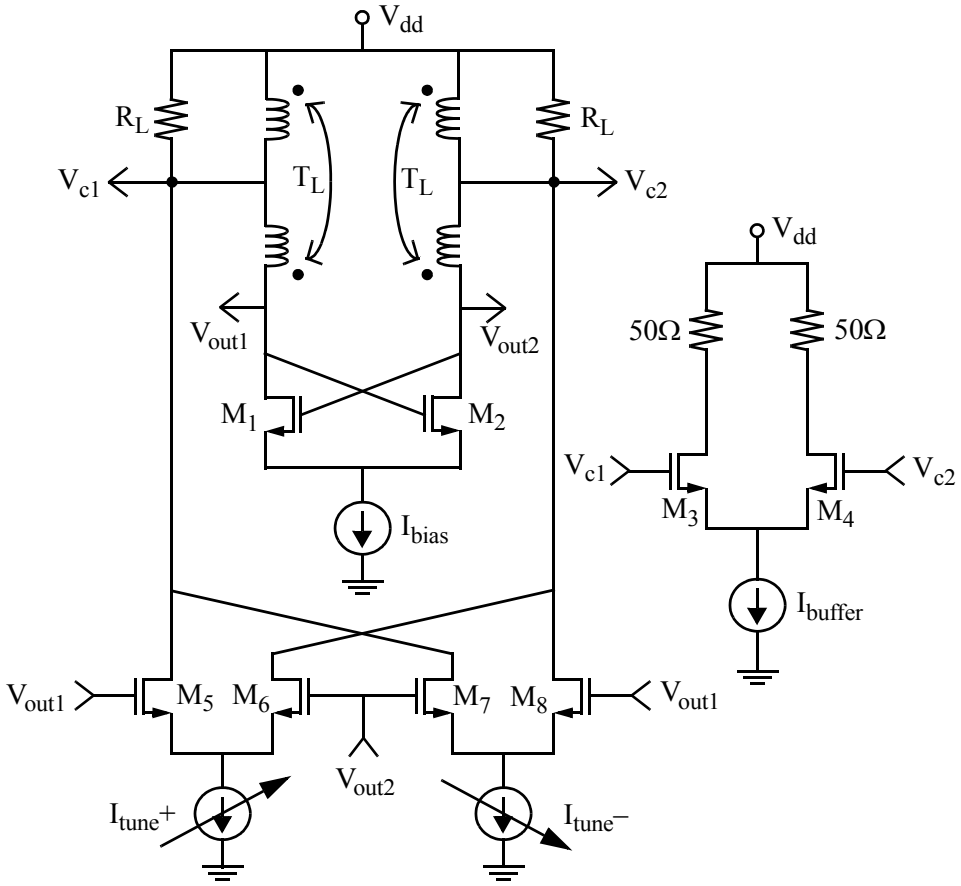

Figure 4.8 Simplified schematic of transconductor-tuned VCO

tor and output buffer included in the simulation. For a resistor sheet resistance on the order of a few hundred ohms per square, this resistor value would have an impractically small aspect ratio of less than 0.1 if implemented as a single element. Thus, R_L is implemented on-chip using multiple resistors in parallel with an aspect ratio of 2.5 for each resistor in order to minimize the effect of processing variations.

Capacitor C_L (from Figure 4.4) is the gate capacitance of M_3 and M_4, which are also a part of the open-drain RF output buffer. The total gate width of each transistor is 72μm, operating at a drain bias current of 2mA. The RF output power of the VCO can be increased by choosing a larger drain bias current. The buffer transistor parasitic capacitances do not affect the tuning range in this design, unlike a varactor-tuned VCO.

The implementation of each transformer T_L and the corresponding lumped-equivalent circuit model derived from full-wave electromagnetic simulation are shown in Figure 4.9. The transformer is implemented using 4μm thick aluminum top metal with an outside dimension of 120μm per side. The metal width and space are 8μm and 5μm, respectively. The two-turn winding gives similar self-inductance values for the primary (P_1) and secondary (P_2). The windings run parallel for posi-

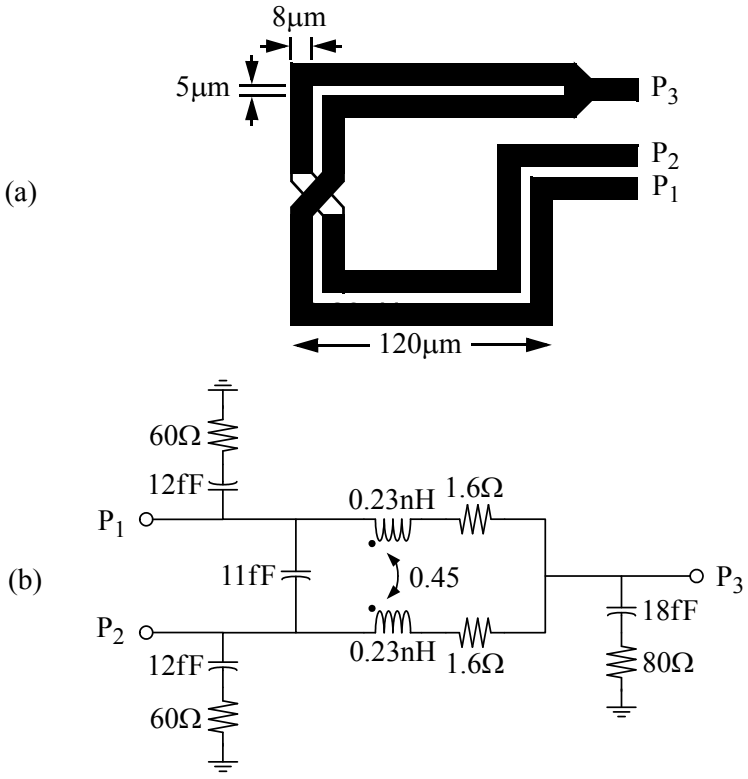

Figure 4.9 Transformer layout and circuit model (a) Physical layout (b) Lumped element circuit model

tive mutual coupling, while port P_3 is the common connection driven by the transconductance cell. The transformer is modeled by two independent inductive branches [see Figure 4.9(b)] with a magnetic coupling (k) factor of 0.45 and mutual capacitive coupling of 11fF. The Q factor of each inductive branch is 18 at 26GHz.

Differential frequency tuning rejects common-mode noise seen by the tuning nodes due to power supply noise and substrate coupling effects, thereby reducing phase noise. The differential transconductor (transistors M_5–M_8 in Figure 4.8) is tunable for both positive and negative values of G_m using current sources $I_{tune}+$ and $I_{tune}–$. With $I_{tune}+$ set equal to $I_{tune}–$, signal currents from M_5–M_6 and M_7–M_8 cancel, resulting in an effective G_m of zero. With $I_{tune}+ = 0$, M_5–M_6 are turned off, and G_m reaches its maximum positive value. Similarly G_m reaches its maximum negative value when M_7–M_8 are turned off (i.e., $I_{tune}– = 0$). The gate capacitances of M_5–M_8 contribute parasitic capacitance to the tank (lumped into C_{tank} shown in Figure 4.4). These capacitances could be minimized if follower buffers were added between the tank output (V_{out1} or V_{out2}) and the gates of M_5–M_8, further increasing the available frequency tuning range.

Since the resonant tank is current controlled, the voltage-to-current converter shown in Figure 4.10 is added for voltage tuning. A differential-pair M_1 and M_2, which are low-threshold devices, is degenerated by 80Ω resistor R_{deg} to linearize the voltage-to-current transfer characteristic. The tuning currents are mirrored to the transconductors shown in Figure 4.8 by PMOS and NMOS current mirrors. The circuit shown in Figure 4.10 limits the single-ended input tuning voltage from 0V to 1.5V (equivalent to ±1.5V differential). However, the transconductor-tuned VCO is

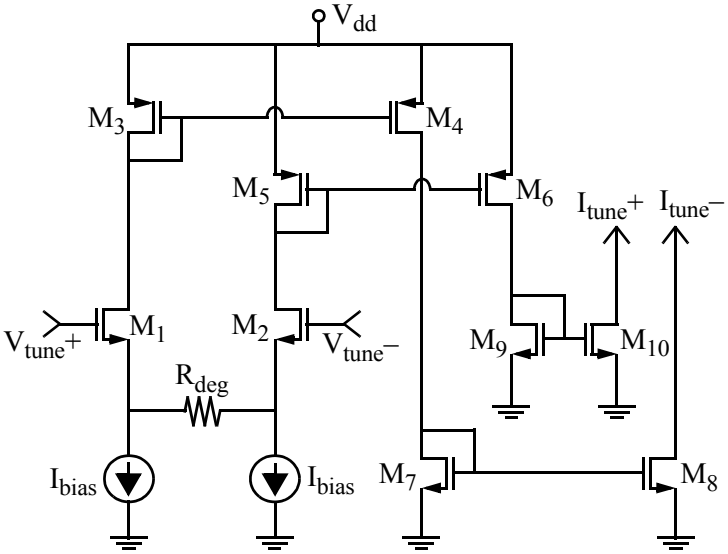

Figure 4.10 Linearized V-to-I converter for differential frequency tuning

a current-controlled oscillator and does not require a tuning voltage beyond the supply or ground potentials, unlike the varactor-tuned VCO described in Section 4.2.

The final tank design is centered at 26GHz, and the simulated tank impedance Z_{tank} as a function of tuning voltage is shown in Figure 4.11. As the differential tuning voltage varies by ±1.6V, the resonant frequency (as defined by the zero-degree phase shift point for Z_{tank}) changes from 23GHz to 31GHz. The magnitude and phase responses resemble those of a parallel LC tank around the resonant frequency. For V_{tune} at 0V, the tank Q is minimum. The magnitude of Z_{tank} is 44dB with a Q factor of 2.7, and the phase response has its lowest slope at the zero-degree phase shift point. Therefore, the phase noise of a VCO is expected to be the poorest at the mid-point of its frequency tuning curve.

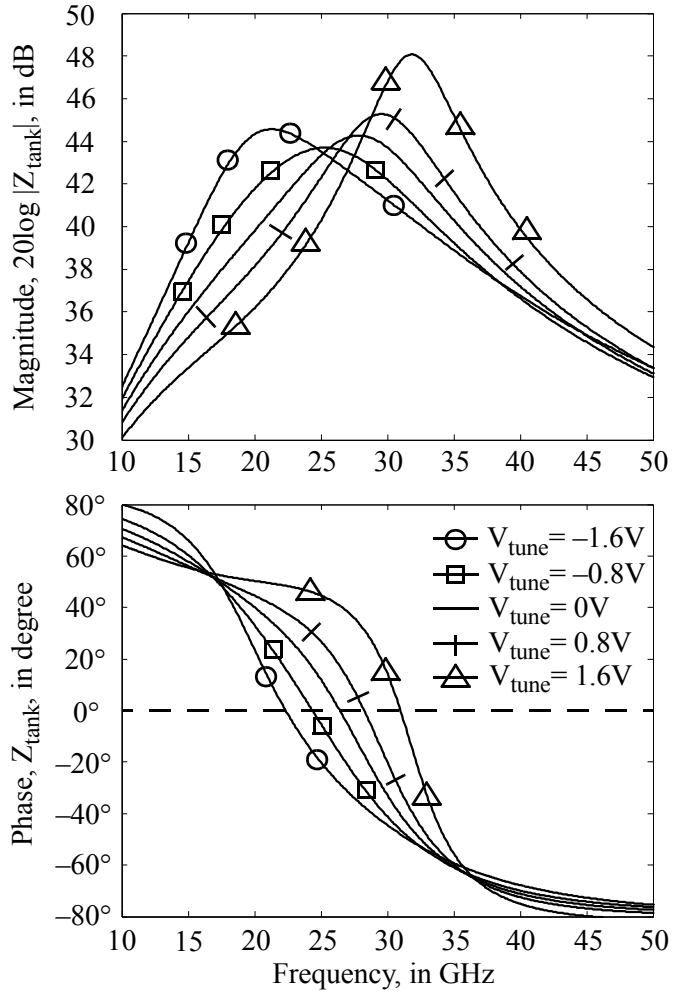

Figure 4.11 Tank impedance versus frequency with ±1.6V tuning voltage for pre-layout simulation.

4.4.2 Experimental Results

The VCO test circuit is implemented in IBM's 0.13μm mixed-signal CMOS technology on a 1–2Ω-cm substrate. The $1 \times 1.4\text{mm}^2$ (including bondpads) testchip is shown in the micrograph of Figure 4.12. The VCO core occupies an area of $0.3 \times 0.4\text{mm}^2$. The differential-mode tuning curve (single-ended output) from wafer probe measurements are shown in Figure 4.13. The tuning is continuous and monotonic from 23.2GHz to 29.4GHz with a 23.6% tuning range. By comparison, the common-mode tuning range is 3.3% from 26.6GHz to 27.5GHz. This highlights the effectiveness of the differential design. The common-mode tuning curve is most sensitive at the common-mode tuning voltage of 0.2V, where the NMOS differential pair in the voltage-to-current converter (as shown in Figure 4.10) cuts off and bias current source I_{bias} enters the linear region. The common-mode tuning range could be further minimized if an improved voltage-to-current converter were used. The average output power delivered to a 50Ω load is approximately –11dBm across the entire tuning range with 3dB loss from interconnect cables and an external bias-tee for the open-drain output buffer at 26GHz. The VCO gain, measured as the absolute slope of the tuning curve, is between 2.0GHz/V and 4.3GHz/V for frequencies ranging from 23.5GHz to 29GHz.

The measured wideband output spectrum at 26GHz (see Figure 4.14) shows a single output tone over the span from 22GHz to 30GHz. Phase noise was measured using a Rohde & Schwarz FSUP-26 signal analyzer [4.24]. This instrument

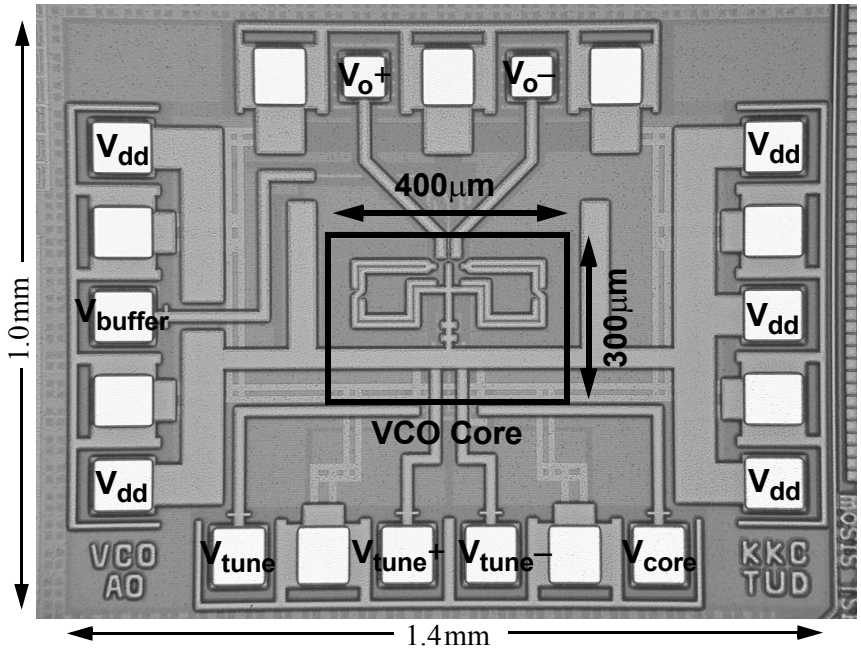

Figure 4.12 Transconductor-tuned VCO chip micrograph

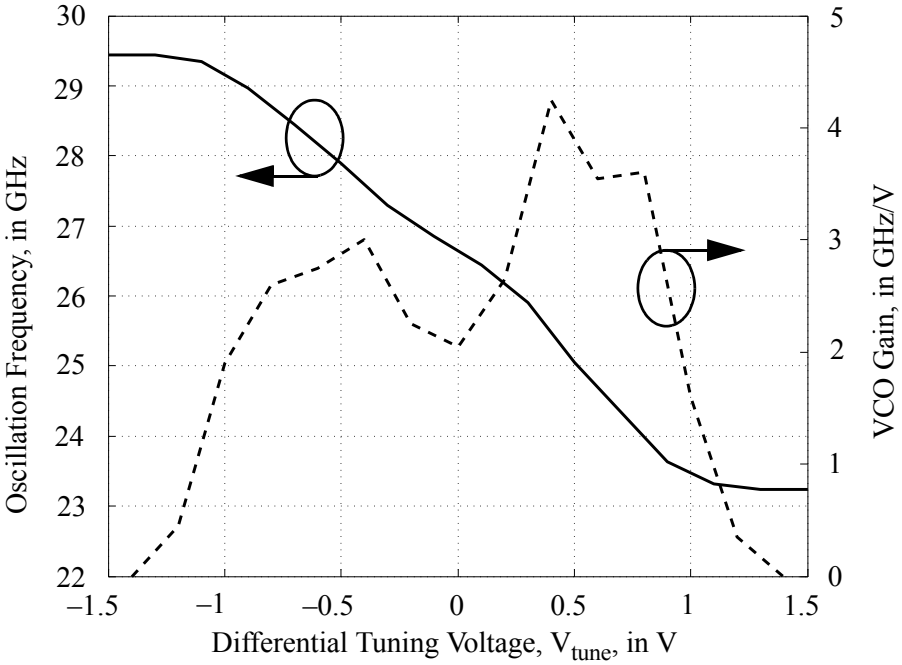

Figure 4.13 Measured output frequency and VCO gain versus differential tuning voltage

uses a phase-locked loop to synchronize an internal reference source to the device-under-test (DUT) frequency, and a phase detector measures the noise level at different offset frequencies. Outside the loop bandwidth, phase noise is caused solely by the DUT. The phase noise plot at an oscillation frequency of 26GHz is shown in Figure 4.15. The phase noise is –92.6dBc/Hz and –106.1dBc/Hz at 1MHz and 3MHz frequency offsets, respectively. The phase noise slope is –30dB/dec up to 10MHz, which is believed to be caused by flicker noise from the deep sub-micron CMOS devices. Figure 4.16 presents the measured phase noise at 1MHz frequency offset versus the frequency tuning range from 23GHz to 26GHz, which is limited by the upper bandwidth of the test instrument. The phase noise performance improves at differential tuning voltages between 1.1V and 1.5V, because the tuning curve sensitivity decreases in this region (as shown in Figure 4.13).

The maximum modulation bandwidth of the VCO is measured by applying a –40dBm differential sinusoidal signal at frequency ω_m to the tuning nodes. The VCO is thus narrowband frequency modulated with the output having two sidebands offset from the carrier by ω_m. The measured modulation bandwidth of 90MHz is defined by the –3dB frequency of the sideband magnitudes. This makes the VCO suitable for a wide range of frequency modulation schemes in radar and communications.

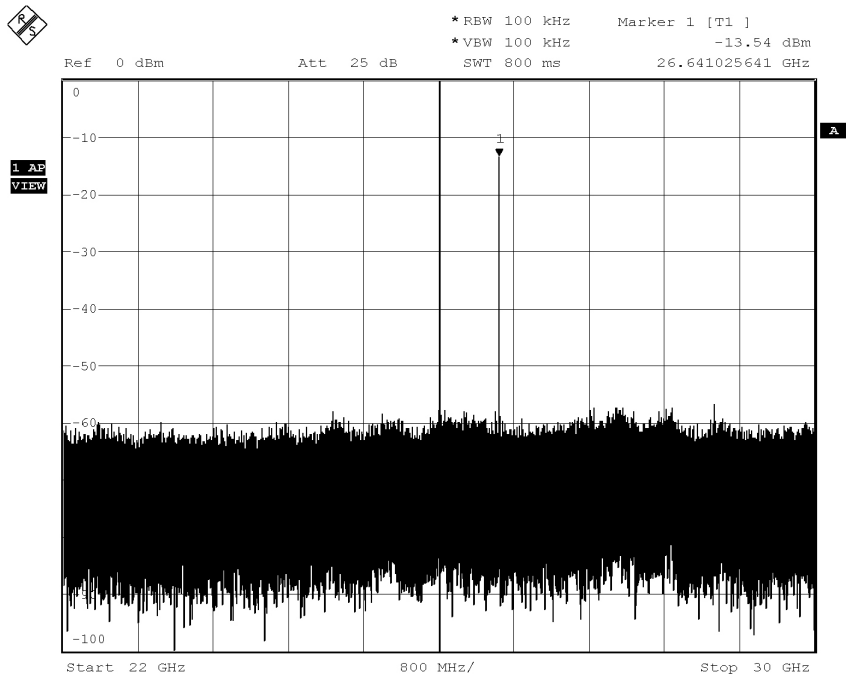

Figure 4.14 Measured wide-span output spectrum at 26.6GHz

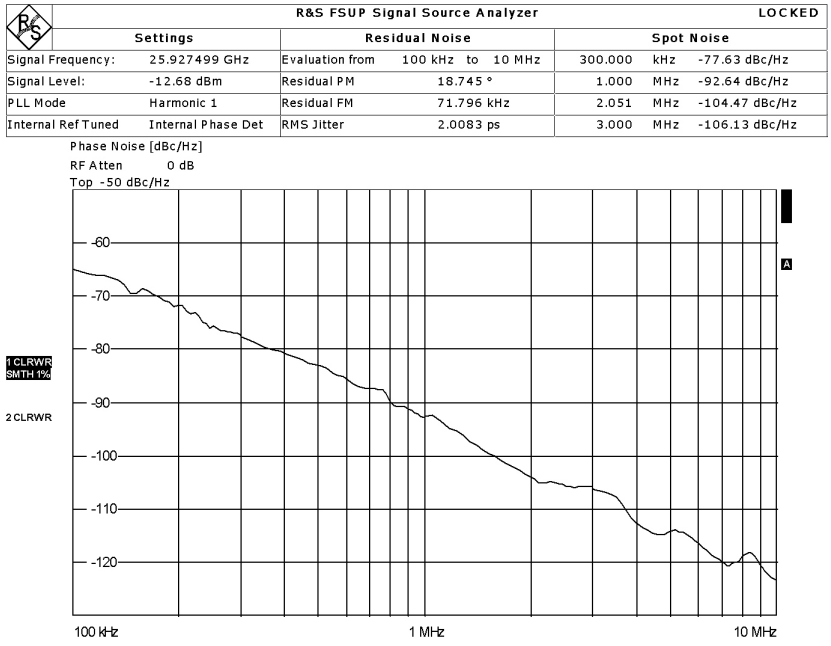

Figure 4.15 Measured phase noise plot at 26GHz

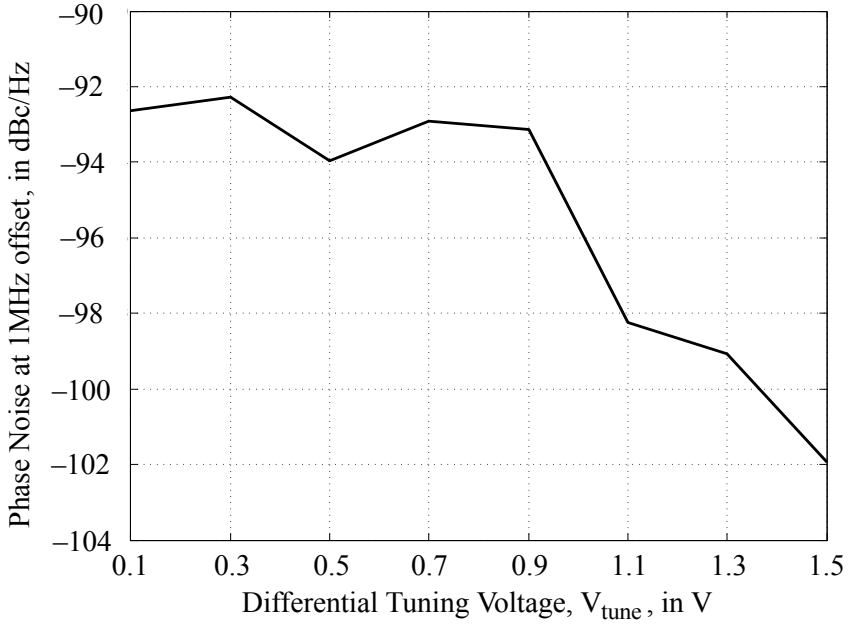

Figure 4.16 Measured phase noise at 1MHz frequency offset versus differential tuning voltage

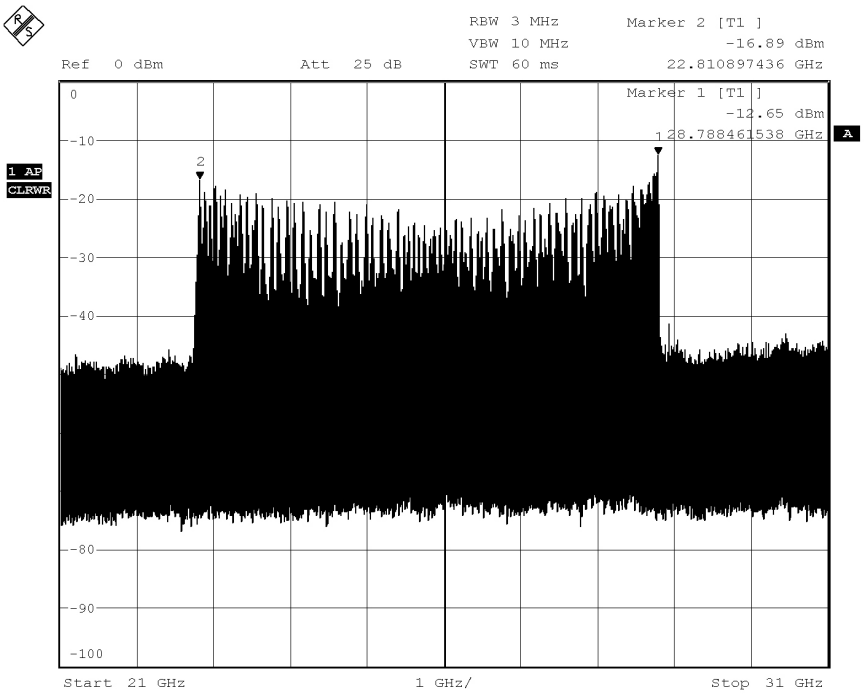

Figure 4.17 Measured output spectrum of the transconductor-tuned VCO for a wideband frequency modulation (ramp input)

To benchmark the wideband capability of the VCO, it is directly modulated by a 100kHz, $0.5V_{pp}$ differential ramp signal. This type of frequency modulation is commonly used in radar applications (e.g., frequency chirping) to enhance range resolution and increases the receiver's resilience to multipath interference [4.25]. The output spectrum shown in Figure 4.17 has 6GHz of bandwidth. This wideband output spectrum is limited by the continuous tuning range of the VCO, and this performance cannot be matched by a narrowband, varactor-tuned, or band-switched VCO.

Total power consumption of the VCO is 43mW (including 6.5mW from the 50Ω output buffer) from a single 1.2V supply.

4.5 Second Testchip: 18.6-to-21.2GHz VCO

The transconductor-tuned VCO is ported to a 90nm CMOS technology intended for the integration with a low-power FMCW short-range radar, in which it acts as the transmitter and receiver LO sources. Design modifications are made in order to minimize the occupied silicon area. It measured with a tuning range from 18.6GHz to 21.2GHz, while only dissipating 5.7mW.

4.5.1 Circuit Design

The radar receiver to be described in Chapter 6 exercises multiple passive inductive components for lowering the power consumption while maximizing the gain and noise performance. In order to minimize the parasitic electromagnetic coupling between the receiver coils and the VCO transformer, and simultaneously relax the floorplanning of the combined receiver and LO circuitry, the two individual transformers shown in Figure 4.9 are merged into a single 5-port differential transformer illustrated in Figure 4.18. Either the transformer in Figure 4.9 or Figure 4.18 could derive to the same equivalent T-model given in Figure 4.4.

The physical layout of the transformer is shown in Figure 4.18(b). The symmetrical primary differential inductor L_1 and L_2, is driven by port P_1 and P_2, respectively. It is implemented using a 4μm thick aluminium top metal with an outside dimension of 137μm×130μm. It is positively coupled to the symmetrical secondary differential inductor L_3 and L_4 by adopting an overlay configuration with maximum magnetic coupling. L_3 and L_4 has a smaller outside dimension of 117μm×130μm and is implemented with a 3μm thick second-top copper layer. The center-tap of the primary and secondary coils are shorted together at port P_5, which acts as a virtual ground for differential excitation. The metal width and space are maintained at 6μm and 4μm, respectively.

An equivalent circuit model similar to the one depicted in Figure 4.9(b) can be obtained for the differential transformer. However, an S-parameter model derived from full-wave electromagnetic simulation accurately captures the multiple cou-

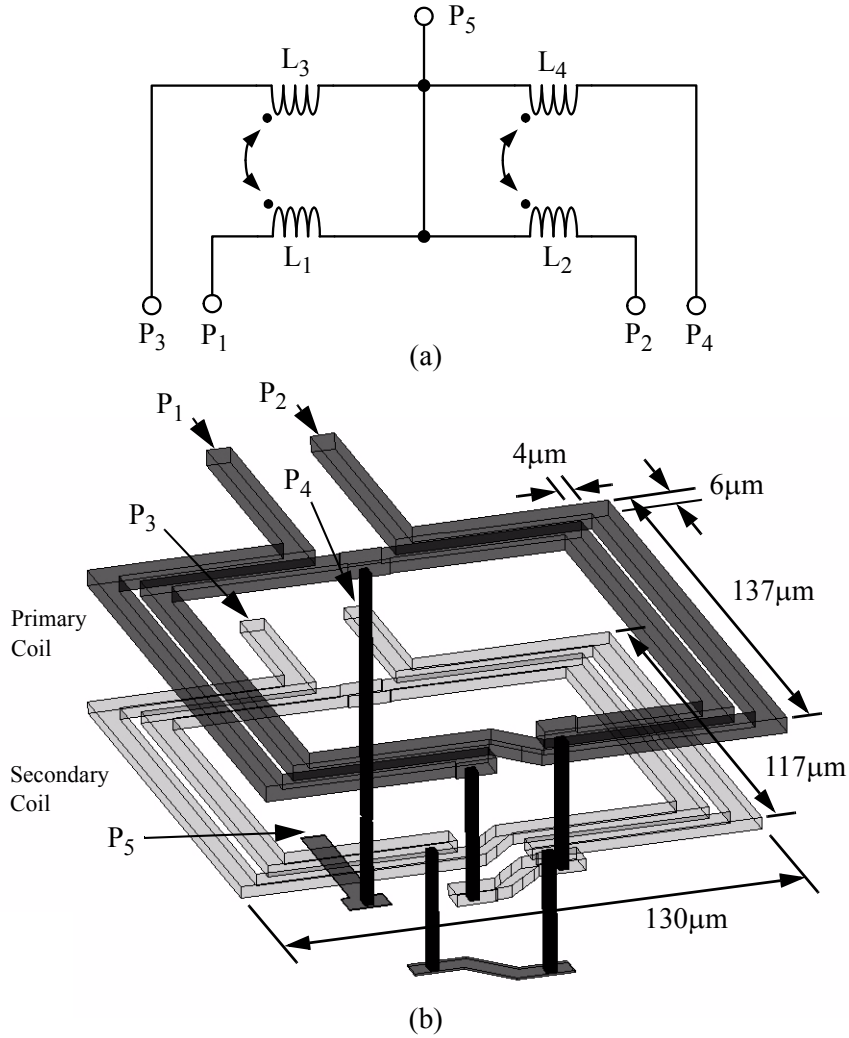

Figure 4.18 5-port differential transformer (a) schematic, and (b) physical layout

pling mechanisms within the 5-port transformer. Additionally, common mode parasitic impedance contributed by bias routing wires, together with supply and ground return paths are properly handled by the S-parameter model. This gives a significant advantage on the modeling accuracy when embedding the VCO into a completed receiver circuit, where the length of the interconnections becomes relatively long compared to the signal wavelength.

The 5-port transformer component values shown in Figure 4.18(a) can be extracted from the S-parameter model. The self-inductance from the primary (L_1+L_2) and secondary (L_3+L_4) coils are predicted at 840pH and 740pH, respectively. Their Q factors at 20GHz are 15.2 and 16.6, respectively. The magnetic coupling factor is about 0.69.

By scaling the transconductance with different DC bias current on transistor M_5–M_8 in Figure 4.8, the frequency range covered by the VCO becomes an adaptable parameter. The current sources $I_{tune}+$ and $I_{tune}–$ in Figure 4.8 are expected to be replaced by two current-mode digital-to-analog converters (DAC) in a complete implementation. Therefore, the differential voltage-to-current converter shown in Figure 4.10 is substituted by two independent current mirrors in the second testchip as illustrated in Figure 4.19. Transistor M_2 and M_3 resemble the output current sources of a DAC [4.26], and R_{deg} in series with the input gate-drain connected transistor linearizes the voltage-to-current relationship with

$$I_{\text{tune}} = \frac{V_{\text{tune}} - V_{gs}}{R_{deg}}, \tag{4.13}$$

where V_{gs} is the gate-source voltage of M_1 or M_4. C_{filter} forms a low-pass filter with R_{deg} at the input terminal in order to reduce the sensitivity to off-chip interferences.

4.5.2 Experimental Results

The second VCO testchip is implemented in IBM's 90nm mixed-signal CMOS technology on a 1–2Ω-cm substrate. It is embedded into a radar receiver circuit and its micrograph is shown in Figure 4.20. The VCO core occupies an area of $170\times220\mu m^2$. Its output buffer (M_3 and M_4 in Figure 4.8) shares the same routing path to the IF port of the receiver mixer (locates on the left-hand-side of the VCO) for probing the oscillation signals at V_o+ and $V_o–$. The design of this VCO is almost identical to the first testchip except for implementation of the differential transformer and frequency tuning current mirror. Therefore, characterization is focused on the frequency tuning range and its adaptivity with bias current settings.

The differential-mode tuning curves for three power dissipation settings are

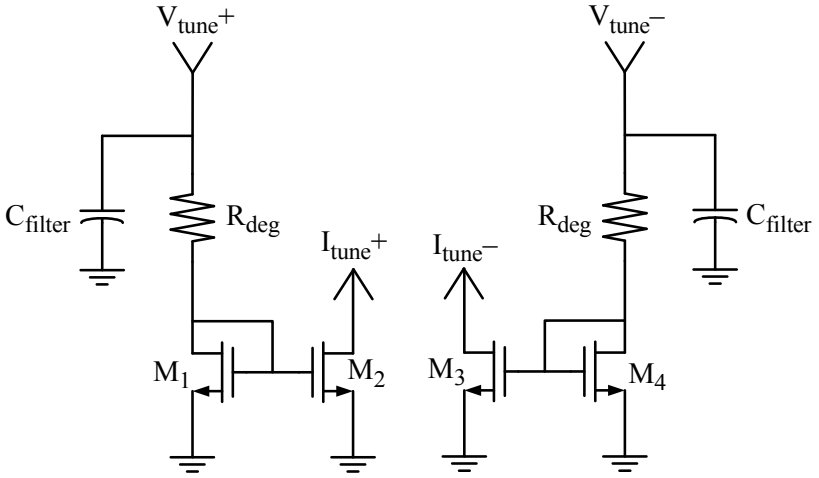

Figure 4.19 Linearized current mirror for differential frequency tuning

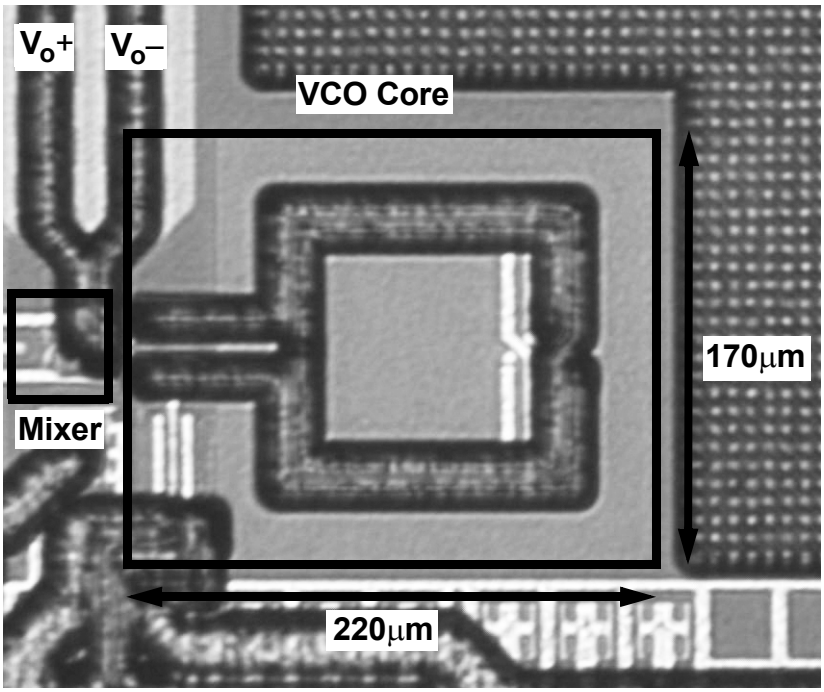

Figure 4.20 Differential transconductor-tuned VCO chip micrograph

shown in Figure 4.21. A wider frequency tuning range could be obtained by increasing the bias current in the transconductance cells (i.e., transistors M_5–M_8 in Figure 4.8). Because differential tuning could be digitally-controlled by a pair of current-DACs, the voltage limitation on the frequency tuning nodes is relaxed. For comparison purpose, the tuning voltage (V_{tune}) on the x-axis is normalized to unity. The 0.2V differential-mode input offset voltage on the x-axis in Figure 4.21 is caused by the transconductor parasitic capacitance, which increases with the bias current [4.14]. For example, the oscillation frequency at V_{tune}= 0V drops from 19.66GHz to 19.57GHz by raising the bias current by 1.29mA. Nevertheless, this offset voltage does not pose problems because the VCO is current tuned.

Table 4.3 summarizes the VCO adaptivity parameters. The tuning range approximately increases by 3% for every 0.65mW increment in the power consumption. While P_{DC} of 5.67mW is limited by the maximum current density on the resistor R_{deg} shown in Figure 4.19, an increase of P_{DC} of 1.3mW (to 6.97mW) is expected to scale up the VCO frequency coverage to 18.0GHz–21.8GHz. This satisfies the VCO frequency specification of 18.0GHz–20.4GHz as specified in Table 4.1. Otherwise, an adjustment of the VCO center frequency from 19.9GHz to 19.2GHz is necessary in order to meet the required frequency coverage.

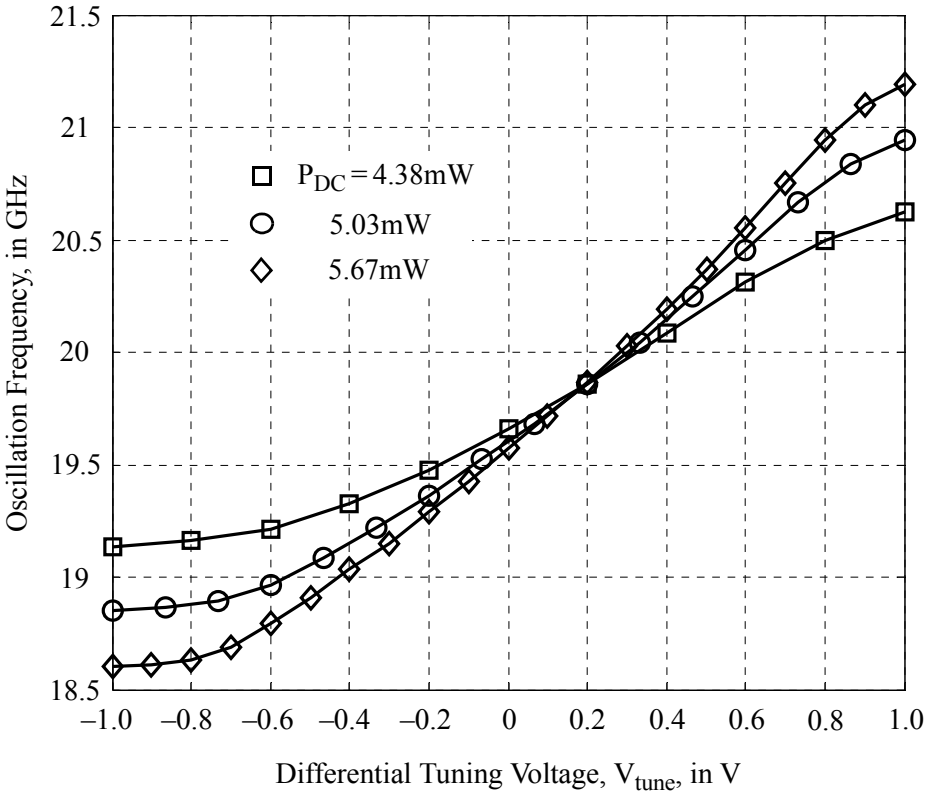

Figure 4.21 Measured output frequency versus differential tuning voltage

At a 1.0V supply and 5.67mW power consumption, the measured phase noise for a 20GHz oscillation frequency is –82dBc/Hz at 1MHz frequency offset. The 2.2mA current budget assigned to the negative resistance cell restricts VCO operation in the current-limited regime [4.27], and constrains its oscillation amplitude and phase noise performance. Burning more DC current drives the VCO into the voltage-limited regime in which phase noise power density could be lowered. However, this is unnecessary for the FMCW SRR application because of the relaxed VCO specification as illustrated in Table 4.1.

Table 4.3 Measured VCO adaptivity parameters

Frequency range	Tuning range	Center Frequency	P_{DC}
19.1–20.6GHz	7.56%	19.9GHz	4.38mW
18.9–20.9GHz	10.1%	19.9GHz	5.03mW
18.6–21.2GHz	13.1%	19.9GHz	5.67mW

4.6 Discussions

Table 4.4 summarizes the measured performance and lists many mm-wave frequency VCOs published in the literature for comparison. To compare VCOs at different oscillation frequency, the normalized phase noise ($PN_{normalized}$) defined by

$$PN_{\text{normalized}} = 10\log\left[\left(\frac{\omega_o}{\Delta\omega}\right)^2 \frac{1}{L\{\Delta\omega\}}\right] \tag{4.14}$$

is used, where ω_o is the oscillation frequency, $\Delta\omega$ is the frequency offset, and $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$.

For bulk CMOS technology designs reported in the literature, the first VCO testchip achieves the widest frequency tuning range. Above 25GHz center frequency, the $PN_{normalized}$ is competitive with designs in all technologies, with the exception of [4.5] and [4.7] in which the tuning range is only 2.2%. Compared with SiGe technology VCOs from [4.8,4.9,4.32], this VCO achieves >10% tuning range without using a dual supply for the tuning voltage. $PN_{normalized}$ is competitive with designs from [4.8,4.30], but is inferior to those of [4.9,4.29,4.32] whose power consumptions are above 130mW or are operating from a 4V supply [4.31]. Compared with SOI technology, this VCO has the widest tuning range and the performance is competitive with [4.10]. $PN_{normalized}$ is worse than that of [4.11,4.12] which could be accounted for by the high-Q passive components available in the SOI technologies used.

The second VCO testchip shows inferior $PN_{normalized}$ compared to all VCOs in CMOS technology. However, it has the widest continuous frequency tuning range with the lowest power consumption. Nevertheless, its phase noise performance satisfy the requirement shown in Table 4.1. Although [4.28] has the lowest power consumption among the VCOs listed in Table 4.4, its frequency coverage is divided into four different bands which is not suitable for FMCW radar application. Compared to both SiGe and SOI technologies, the second testchip has the widest tuning range for less than 10mW power dissipation and less than 1.5V supply voltage, except the SOI VCO in [4.11] which needs a maximum tuning voltage at 3V.

Table 4.5 compares other published inductively-tuned VCOs with wide frequency tuning range. A varactor-array and current-tuning of a transformer resonant tank in [4.35] achieves a 4.1GHz frequency range centered at 4.8GHz. Its relatively low oscillation frequency could tolerate a 0.8μm channel length from an accumulation-mode varactor, which favours the varactor capacitive tuning ratio as explained in Section 4.2. The capacitive and inductive schemes independently contribute about 2.2GHz and 2.0GHz to the overall frequency range, respectively. Quadrupling the center frequency to 20GHz (as in the second VCO testchip) further lowers the varactor tunability and the frequency range for inductive tuning.

Table 4.4 Comparison of millimeter-wave frequency VCOs

Center Frequency (GHz)	Tuning Range (%)	Tuning Voltage Range (V)	Supply Voltage (V)	Phase Noise (dBc/Hz)	Normalized Phase Noise (dB)	Power Consumption (mW)	Reference Number	Technology
26.3	23.6	0 to 1.5	1.2	–92.6@1MHz	–181.0	43	First Testchip	0.13μm CMOS
19.9	13.1	0 to 1	1	–82.0@1MHz	–168.0	5.7	Second Testchip	90nm CMOS
10.9	8.8	0 to 1.2	1.2	–96.7@1MHz	–177.4	70	[4.3]	90nm CMOS
16.2	16.5	0 to 1.8	1.0	–110.0@1MHz	–194.2	5	[4.28]	0.18μm CMOS
17.0	8.6	0.64 to 1.4	1.4	–108.0@1MHz	–192.6	10.5	[4.4]	0.25μm CMOS
20.4	25.0	–5.6 to 0.5	4.5	–105.5@2MHz	–185.7	13.5	[4.8]	0.25μm SiGe
21.3	5.0	0.5 to 4.0	3.2	–113.0@1MHz	–199.6	130	[4.29]	0.25μm SiGe
26.1	5.0	–4.25 to –1.25	1.9	–93.0@1MHz	–181.3	27	[4.30]	0.25μm SiGe
36.4	6.6	0 to 4.0	4.0	–105.0@2MHz	–190.2	84	[4.31]	0.25μm SiGe
40.0	15.0	0 to 2.7	1.5	–97.0@4MHz	–177.0	11.3	[4.10]	0.13μm SOI
40.3	12.5	–1 to 1.5	3.0	–99.0@1MHz	–191.1	363	[4.32]	0.18μm SiGe
41.5	26.3	–2.8 to 3.0	–5.5	–107.0@1MHz	–199.4	280	[4.9]	0.35μm SiGe

43.0	4.2	0 to 1.0	1.0	–90.0@1MHz	–182.7	14	[4.33]	0.13μm CMOS
44.0	9.8	0.1 to 0.9	1.5	–101.0@1MHz	–193.9	7.5	[4.12]	0.13μm SOI
50.0	2.2	0 to 2.6	1.3	–99.0@1MHz	–193.0	13	[4.5]	0.25μm CMOS
51.0	2.7	0 to 1.6	1.0	–85.1@1MHz	–179.3	9.3	[4.6]	0.12μm CMOS
57.0	2.1	0 to 1.2	1.2	–113.6@10MHz	–188.7	20.4	[4.7]	0.13μm CMOS
59.0	9.8	0 to 1.5	1.5	–89.0@1MHz	–184.4	9.8	[4.34]	0.13μm CMOS
60.0	12.5	1.0 to 3.0	1.2	–94.0@1MHz	–189.6	9.6	[4.11]	90nm SOI

Table 4.5 Comparison of inductively-tuned VCOs

Center Frequency (GHz)	Tuning Range (%)	Tuning Voltage Range (V)	Supply Voltage (V)	Phase Noise (dBc/Hz)	Normalized Phase Noise (dB)	Power Consumption (mW)	Reference Number	Technology
4.8	67	0 to 1.2	1.2	–114.1@1MHz	–184.2	7.2 to 24	[4.35]	65nm CMOS
11.3	45.3	0 to 1.8	1.8	–86.8@1MHz	–167.6	14.4 to 32.4	[4.37]	0.13μm SiGe
56.8	14	–0.3 to 1.2	0.4 to 0.9	–72.5@10MHz	–147.5	8.7	[4.38]	90nm CMOS
59.6	25.8	0.5 to 1.5	1.0	–98.5@10MHz	–166.7	5.4	[4.39]	65nm CMOS
61.0	14.2	0 to 1.2	1.0	–108.3@10MHz	–176.2	6.0	[4.39]	65nm CMOS
73.4	44.2	0 to 1.8	1.2	–111.8@10MHz	–188.9	8.4 to 10.8	[4.40]	65nm CMOS

The linear relationship between bias current and diffusion capacitance in a bipolar transistor [4.36] enables efficient frequency-band switching by stepping the bias current in the VCO negative resistance cell, where a 5.1GHz tuning range over six discrete frequency bands is reported in [4.37]. The frequency range realized by sweeping the tuning current in the transformer tank continuously, however, is only 9.8% at 11.3GHz.

Applying a variable resistance to the transformer secondary coil alters the inductance seen from its primary coil, but with high resistive loss and hence poor Q. A 14% continuous tuning range at 56.8GHz is obtained in [4.38] but its normalized phase noise is the poorest compared to all VCOs listed in Table 4.4 and Table 4.5. Substituting the variable resistance with switches shunting the metal strips in the secondary coil realizes inductive-bank switching on the VCO frequency, while continuous tuning is still provided by a traditional varactor. Discrete frequency bands of 9.2GHz and 6.2GHz are measured for the two testchips in [4.39], but their continuous frequency ranges are only 3.0GHz (5.0%) and 2.0GHz (3.3%), respectively. Another 73.4GHz inductive-bank switching VCO in [4.40] increases the discrete frequency bands to 32.6GHz but having a non-overlapping frequency gap between 76GHz and 77.5GHz. Its continuous frequency range is still limited to 2.5GHz (2.8%) at 89GHz.

4.7 Summary

A varactorless frequency tuning scheme is proposed in order to break through the design bottleneck on a continuous and wideband mm-wave frequency generation in CMOS technology: about the trade-off between capacitance tuning ratio and quality factor, and the decreasing capacitance Q with the operating frequency. A dedicated transformer resonant tank exploits the 90° terminal voltages of a transconductor, and control its parallel resonant frequency by sweeping the sign and magnitude of the transconductance. The VCO is frequency-agile, and is continuously tunable by altering the DC bias current from the transconductance cell. It does not require any control voltage exceed the supply or ground potentials. Adaptivity between frequency tuning and power consumption is possible by upper limiting the transconductance bias current. A proof of concept is implemented by two single-ended transformers. It has a frequency coverage from 23.2GHz to 29.4GHz with a 23.6% tuning range. The same design is miniaturized for the low-power short-range radar receiver by applying a 5-port differential transformer. It is tunable from 18.6GHz to 21.2GHz with 5.7mW power dissipation. The integration of this VCO into the radar receiver circuit is covered in Chapter 6 of this thesis.

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Chapter 5

LNA Design and Optimization

Operation of a CMOS LNA on a limited current budget results in transistors biased at a low drain current density, and subsequently suffers from low RF power gain and high noise figure. The situation is exacerbated in the mm-wave frequency range, which approaches the transistor's operational limits. This chapter presents an algorithm for LNA design and optimization with emphasis on low-voltage and low-power operation. At the device level, the individual transistor is dimensioned in order to satisfy power gain, noise figure, linearity, and bandwidth requirements. At the circuit level, the interaction between transistors is co-ordinated in order to optimize the interface impedance for power gain and noise figure in cascaded stages. Employing this algorithm, a low-power LNA preserving power gain and noise figure performance with transistors biased in the moderate inversion region becomes possible.

Single transistor common-source and common-gate amplifiers are first examined for their gain, noise, and linearity characteristics. This is followed by considerations of bandwidth and passive device losses from an on-chip matching network, which reduces the external component count and simplifies the printed circuit board design. This information guides device sizing and topology selection in a multi-stage amplifier. The advantages of applying current budget partitioning and supply voltage scaling to a multi-stage amplifier over the use of a simple single-stage amplifier, is explored as a trade-off between power consumption and design complexity. The optimal impedance matching conditions for cascaded amplifier stages are then revisited based on the cascade power gain and noise figure equations. Two feedback principles facilitating the optimal matched conditions are then discussed. An efficient Smith chart based methodology is followed which simplifies the optimization of inter-stage matching networks by manipulating the two aforementioned feedback schemes simultaneously [5.1]. Finally, three examples are given to demonstrate the advantages of the proposed algorithm.

5.1 Introduction

The LNA electrical specifications summarized in Table 5.1 are derived from the short-range radar system analysis presented in Chapter 3. It dissipates 3mW of the 15mW power budget for the complete radio receiver, and delivers 15dB gain, with

Table 5.1 LNA target electrical specifications

Gain (dB)	NF (dB)	IIP_3 (dBm)	P_{DC} (mW)
15	5	–10	3

5dB noise figure, and –10dBm IIP_3. Biasing a MOS transistor at low current reduces its transconductance and power gain. For frequencies where the transistor's output impedance is dominated by parasitic capacitance, the maximum available power gain decreases at –20dB/decade in frequency from a calculation based on the small-signal model [5.2]. For 3mW of DC power, simulation with an RF MOSFET model [5.3] (including wiring parasitic resistances and capacitances up to the 1st metal layer) predict that the unity maximum power gain frequency (i.e., f_{max}) of a 90nm NMOS transistor is approximately 200GHz. The ratio of f_{max} to the operating frequency at 24GHz is limited to 8.3. The low transconductance due to the constrained current budget also translates to a higher equivalent input voltage and current noise sources [5.4], and subsequently a higher minimum noise figure. The noise figure deteriorates at higher frequencies because of the transistor's decreasing power gain. Additionally, resistive losses contributed by an on-chip matching network further increase the LNA noise figure. Although the linearity of MOS transistors improves with a larger gate-source overdrive voltage (and therefore a higher DC power dissipation), there is an optimum point at which peak values of the –1dB compression and third-order intercept points can be observed at a lower bias current [5.5]. This will be demonstrated in Section 5.2.3, where the same IIP_3 of 0dBV can be delivered by an NMOS transistor biased at a drain current density of either 34.6μA/μm or 180μA/μm. While amplifier IIP_3 depends on the impedances loading and driving the transistor, the selected quiescent point remains valid when optimizing IIP_3 [5.6]. Therefore, the optimization priorities for a low-power, mm-wave LNA are the power gain and noise figure specifications, and secondarily, on meeting the linearity requirement.

The LNA optimization algorithm developed in this chapter can be summarized by the following design steps:

1) In order to quantify the performance limit from a given technology, characterize the parameters of different basic amplifier topologies in terms of
   i) power gain,
   ii) noise figure,
   iii) linearity,
   iv) bandwidth,
   v) noise figure dependency on matching network loss.
2) Given the information generated in Step (1), analyze whether a single-stage or cascade is necessary to satisfy the LNA specifications within the power budget, and determine the appropriate transistor sizing.
3) If a cascade amplifier is necessary, determine

i) the advantage of current and voltage partitioning on the overall power dissipation budget.
ii) the best topology for each amplifier stage.
iii) the interaction between stages on the overall amplifier performance.
iv) the implementation and optimization algorithm to satisfy the interfacing requirements for each amplifier stage.

Scalable and experimentally verified RF compact models [5.3] provide the means of extracting these parameters for all of the simulations covered in this chapter.

5.2 Optimization at the Device Level

The three basic amplifier configurations for a single CMOS transistor are the common-source, common-gate, and common-drain. Consider a 90nm NMOS transistor with multi-finger gate of $50 \times 2\mu m$ width, and minimum channel length of 90nm biased at $15\mu A/\mu m$. The simulated maximum power gain and minimum noise figure at 24GHz are summarized in Table 5.2. The common-source outperforms other configurations in terms of gain and noise figure, and the common-gate gives a better gain but worse noise performance than the common-drain.

Although the common-drain delivers considerable RF performance, it does not behave well as an RF amplifier. The input-to-output DC voltage relationship being fixed by the gate-source voltage which hinders the DC bias flexibility when cascading with other circuit blocks in a low-voltage design. Also, the parasitic gate-source capacitance of the MOS transistor introduces a significant coupling path for signal feedthrough. As a result, the common-drain amplifier suffers from poor reverse-isolation, which is an important parameter for an RF amplifier. This coupling path also introduces impedance transformation between the input and output terminals. For example, inductive [5.7] or capacitive [5.8] output loads are transformed to a positive or negative resistance at the amplifier's input, respectively. This adversely affects gain and stability optimizations of a multi-stage amplifier and the design complexity. Therefore, only the common-source and common-gate amplifiers are considered in the LNA optimization procedures.

5.2.1 Device Sizing for Power Gain

Conventional LNA optimization of device dimensions suffers from two weaknesses. The power gain of a transistor is usually quantified and compared by the parameter f_{MAX} for the transistor when configured as a common-source amplifier,

Table 5.2 RF performance of three single-transistor NMOS amplifiers with dimension $50 \times 2\mu m$ by 90nm, biased at $15\mu A/\mu m$, and at 24GHz

	common-source	common-gate	common-drain
MAG (dB)	6.616	5.828	4.034
NF_{min} (dB)	0.9519	1.962	1.160

and the gate width and length are then varied under different bias current density [5.9]. For a MOS transistor, the gate-drain capacitor couples the input and output terminals in a common-source amplifier, but acts as a grounded capacitance in a common-gate amplifier. Therefore, this method ignores the transistor parasitics behave differently in different amplifier topologies.

For an 100μm wide NMOS transistor, Figure 5.1 shows the simulated power gain against frequency for a bias current of 1.5mA for different finger widths (i.e., a constant drain current density of 15μA/μm). At frequencies below 40GHz, the transistor is potentially unstable and the maximum stable gain (MSG) is given by $|s_{21}/s_{12}|$. Unstable operation of the transistor is due to the parasitic feedback via the gate-drain parasitic capacitance, and the source and load impedances defined in the power gain equations [5.10]. With decreasing power gain at higher frequencies, the transistor becomes unconditionally stable in the maximum available gain (MAG) regime. The inflection point in Figure 5.1 divides MAG and MSG regimes. Sheet resistance of the gate material and gate contact resistance contribute to the transistor's gate resistance, which damps and stabilizes the parasitic feedback loop. A multi-finger transistor layout reduces the sheet resistance, but is ultimately limited by the contact resistance. Therefore, the two widest unconditionally stable regimes correspond to the widest ($W_f = 10\mu m$) and narrowest ($W_f = 0.5\mu m$) finger widths as shown in Figure 5.1.

Optimization of active device sizing using f_{MAX} as a quantifier could lead to misleading results because the simulated f_{MAX} across different finger widths varies between 58.2GHz and 145.1GHz, but the MSG values are roughly the same at 24GHz (i.e., around 6.7dB). Extrapolation of the power gain beginning from the

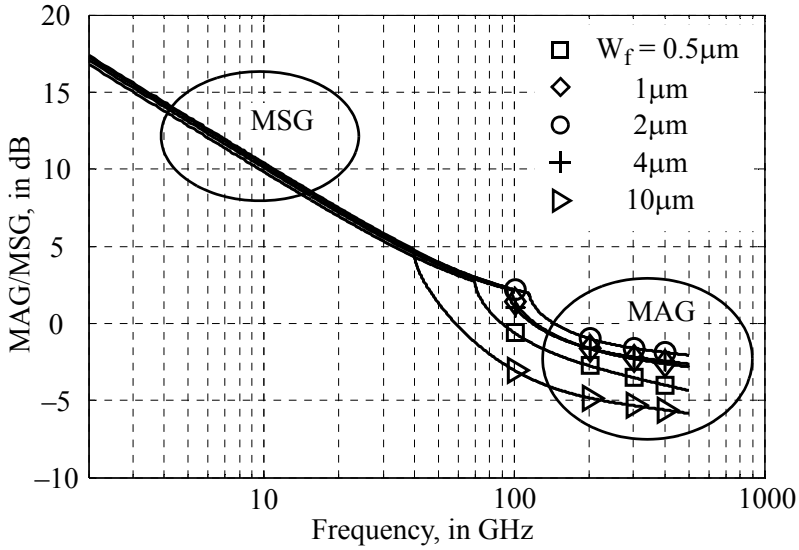

Figure 5.1 Simulated power gain of an 100μm/90nm NMOS transistor versus frequency for different finger widths when biased at 1.5mA

lower frequency regions where the extrapolated f_{MAX} would give approximately the same value is still not sensible when attempting to optimize the transistor finger width when the operating frequency is in the MAG region. For example, at 60GHz the power gain for $W_f = 10\mu m$ is 3dB lower than for other finger widths, as shown in Figure 5.1, while the extrapolation from 24GHz indicates that W_f from 0.5μm to 10μm share the same f_{MAX} of ≈109GHz.

In order to avoid these unnecessary inaccuracies and give better insight for the target application, a better method is to evaluate the transistor's power gain exactly at the desired operating frequency, and ensure the power gain specification satisfies the electrical requirement.

For a common-source configuration, five different finger widths (W_f) from 0.5μm to 10μm are compared in Figure 5.2 for the power gain and forward transmission coefficients versus drain current density. The total transistor width and drain-source voltage are fixed at 100μm and 0.5V, respectively, and their selections will be explained in Sections 5.2.4 and 5.3.1. Both power gain and $|S_{21}|$ increase with the drain current density. Their variations over the finger widths are partly due to differences in gate resistance, and partly due to the fact that the effective gate width (W_{eff}) is shorter for a smaller finger width, because $W_{eff} = W_f - \delta W$, where δW is a constant for a given gate-to-bulk bias voltage [5.11]. Compared to $|S_{21}|$, the power gain shows less variation across different finger widths because the changes

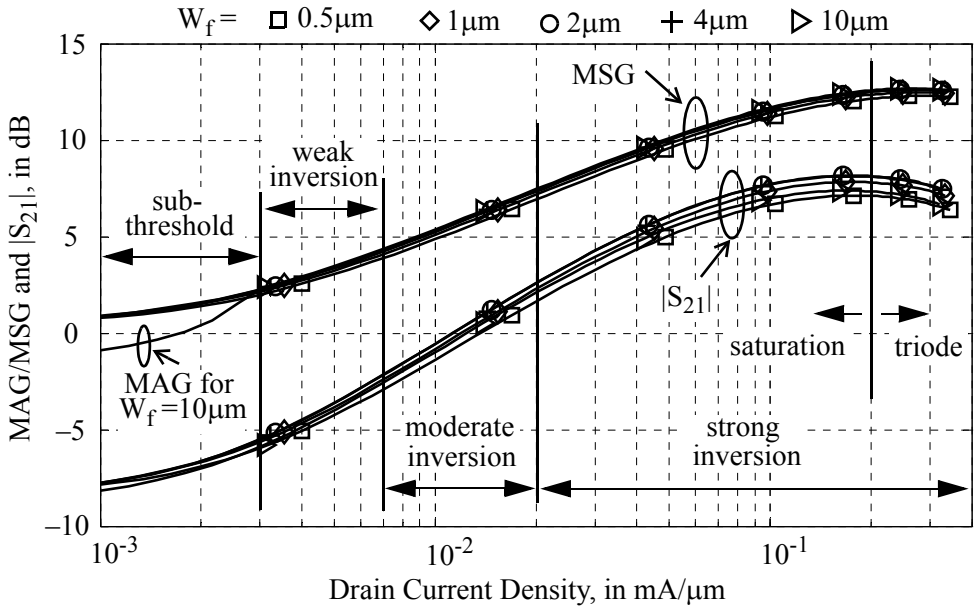

Figure 5.2 Simulated power gain and forward transmission coefficient of an NMOS common-source amplifier with 90nm channel length versus drain current density for different finger widths at 24GHz

in the transistor's input and output impedances are adapted by the matching networks. The optimal finger width for the common-source configuration from these simulations is 2μm from power gain considerations.

Three operating regions for the MOS transistor are observed in Figure 5.2. In the sub-threshold region (current density $<3\times10^{-3}$mA/μm), the power gain and $|S_{21}|$ are bounded by signal feedthrough via the gate-drain parasitic capacitance. The moderate inversion region is located at drain current density between 7×10^{-3}mA/μm and 2×10^{-2}mA/μm. Power gain and $|S_{21}|$ in the strong inversion region (current densities $>2\times10^{-2}$mA/μm) are limited when the transistor eventually falls into the triode region (current densities above 0.2mA/μm) with the gate-source overdrive voltage is equal to, or greater than the drain-source voltage.

The same power gain characterization can be applied to a common-gate configuration. With the same transistor dimensions, but maintaining the gate and drain DC bias voltages at the 1.0V supply, the simulated power gain and forward transmission coefficients are plotted in Figure 5.3. The grounded gate-drain capacitance in the common-gate configuration gives 7.34dB better isolation than a common-source amplifier, with an $|S_{12}|$ of –18.97dB. This advantage of higher reverse isolation is seen by the continuous decrease of $|S_{21}|$ in the sub-threshold region because of less signal feedthrough compared to the common-source amplifier simulation results as shown in Figure 5.2. This amplifier is unconditionally stable under

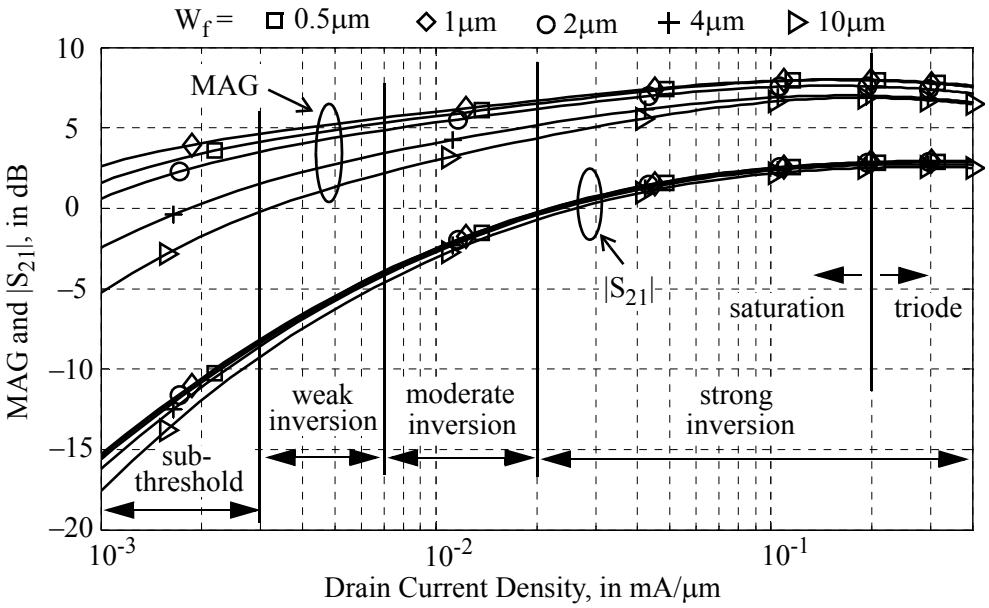

Figure 5.3 Simulated power gain and forward transmission coefficient of an NMOS common-gate amplifier with 90nm channel length versus drain current density for different finger widths at 24GHz

the range of parameters given in Figure 5.3, and therefore the power gain equals MAG. In the strong inversion region, the power gain is lower than the common-source amplifier. However, they give comparable results in the moderate inversion region.

The variation of MAG across W_f is contributed by the variation in gate resistance because it introduces negative feedback in a common-gate amplifier. For NMOS transistors having W_f of 0.5μm and 10μm, their simulated gate resistances are 2.779Ω and 11.43Ω, respectively, at the same drain current density of 10^{-2}mA/μm. Adding 8.7Ω of extrinsic gate resistance to the 0.5μm W_f transistor lowers its power gain from 5.73dB to 3.52dB, which is 0.53dB below the 2.98dB gain of the 10μm W_f transistor. This verifies that gate resistance is the cause of gain reduction observed for the different finger widths. The finger width for optimum power gain in the common-gate configuration is 1μm.

5.2.2 Device Sizing for Noise Figure

The effects of gate resistance on the noise performance of MOS transistors have been investigated extensively [5.12,5.13]. The target for optimization is to choose the transistor dimensions that minimize the noise figure within the power consumption budget. Figure 5.4 shows the simulated minimum noise figure of a 100μm wide common-source NMOS transistor versus finger width and drain current density, at a fixed drain-source voltage of 0.5V. A local minimum (NF_{min}) appears at the drain

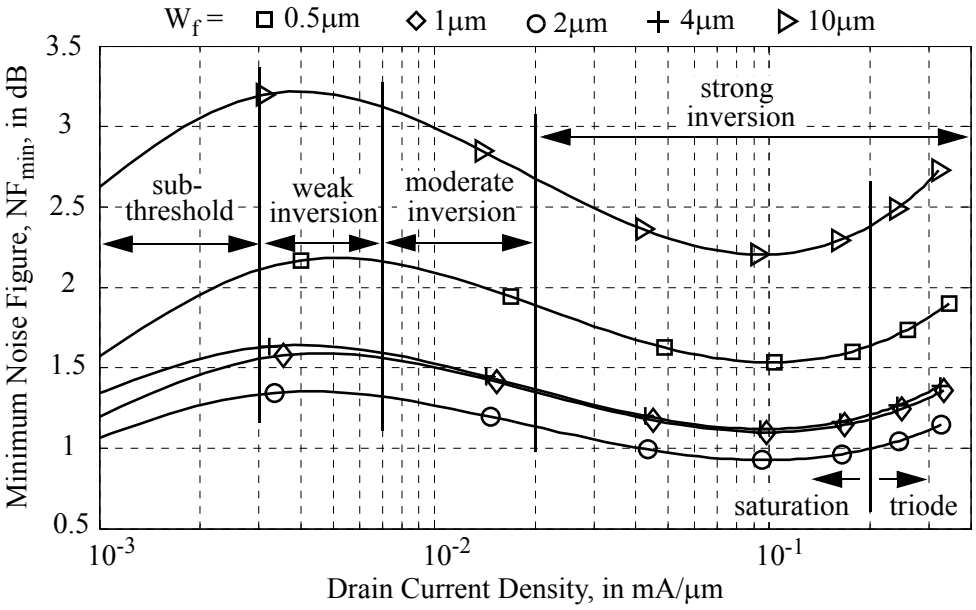

Figure 5.4 Simulated minimum noise figure of a common-source amplifier with 90nm channel length versus drain current density for different finger widths at 24GHz

current density of 10^{-1}mA/μm which corresponds to the transistor in the strong inversion and saturation regions. Increasing the drain current density (above 0.2mA/μm) by a higher gate-source voltage drives the transistor into the triode region, where NF_{min} increases because there is a higher thermal noise power but the transistor power gain remains flat (see Figure 5.2). Reduction of the current density also increases NF_{min} until the transistor is driven into the sub-threshold region (current density $<3\times10^{-3}$mA/μm) where the transistor thermal noise decreases, but the signal feedthrough to the output via the gate-drain capacitance stays constant.

The common-gate configuration shows similar noise performance as seen in Figure 5.5, except that NF_{min} increases continually in the sub-threshold region because there is no parasitic signal path between the amplifier input and output terminals. For the parameter ranges shown, the common-gate always shows inferior noise performance compared to the common-source configuration. This is because the channel thermal noise shunts to the amplifier input directly without any transconductance gain [5.14]. Nonetheless, the difference in NF_{min} is only about 0.30dB and 0.61dB in the strong and moderate inversion regions, respectively. In these regions, both configurations show that the increase in NF_{min} is much slower than the decrease in power gain at reduced drain current densities. For a decade drop from 10^{-1}mA/μm to 10^{-2}mA/μm, the common-source and common-gate configurations give NF_{min} increases of 0.34dB and 0.65dB, respectively, while power gain decreases by 5.94dB and 1.52dB, respectively. Therefore, maximizing the power

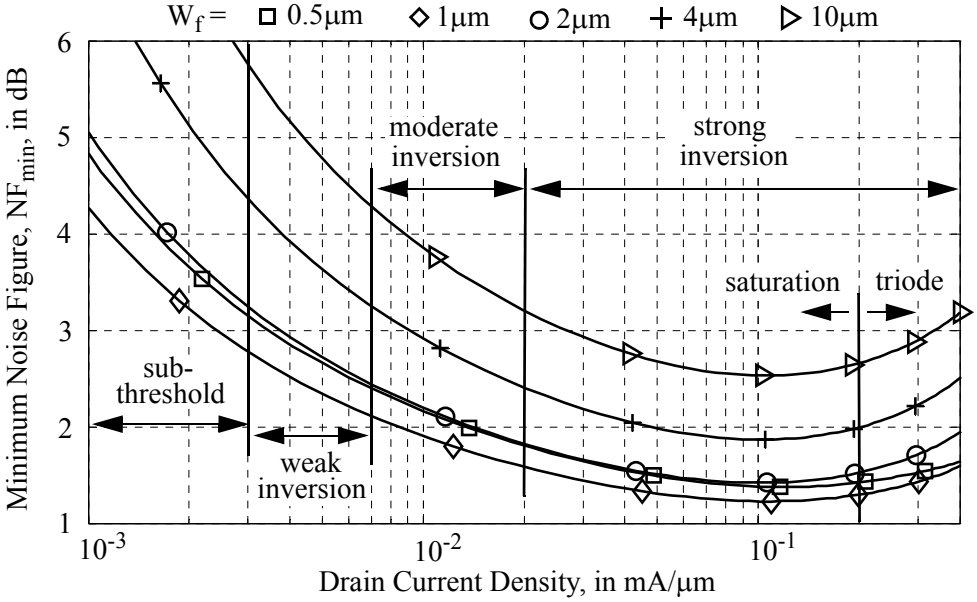

Figure 5.5 Simulated minimum noise figure of a common-gate amplifier with 90nm channel length versus drain current density for different finger widths at 24GHz

gain is more difficult than minimizing the noise figure for a low-power LNA design.

The optimum finger width for minimum noise figure aligns with the results for maximum power gain: 2μm and 1μm for common-source and common-gate configurations, respectively. Simulations show the optimum finger width is insensitive to different types of feedback applied to the common-source or common-gate amplifiers. The required source and load impedances in order to realize maximum power gain or NF_{min} are also insensitive to the transistor's finger width.

5.2.3 Device Sizing for Linearity

There is an optimum bias current density for maximum linearity [5.5]. For a given quiescent point, the transistor transconductance transfer curve can be expressed as a series $a_1x(t) + a_2x^2(t) + a_3x^3(t) + \ldots$, where x(t) is the input signal, and coefficients a_i are given by their corresponding i^{th}-order derivative of the I_{DS}-V_{GS} curve. This is illustrated in Figure 5.6(a) for the simulated fundamental (a_1), second (a_2), and third-order (a_3) coefficients of a 50×2μm/90nm common-source NMOS amplifier versus the drain current density and with a fixed 0.5V drain-source voltage. The linear gain coefficient a_1 is the transconductance of the transistor, which increases with increasing bias current. The derivative of a_1 is the second-order coefficient a_2, which reaches a peak value at a drain current density of 43.8μA/μm. Similarly, a_3 is the derivative of a_2 and it's value becomes zero at this current density (i.e., 43.8μA/μm). Because the coefficients a_i are measured at DC, the above observations are also valid for the common-gate topology.

The input second and third-order intercept points of the same 50×2μm/90nm common-source NMOS amplifier are simulated with time varying inputs at 24GHz, and the results are shown in Figure 5.6(b) in order to verify their relationship with the coefficients a_i. The IIP_2 and IIP_3 of the common-source amplifier are proportional to $\sqrt{a_1/a_2}$ and $\sqrt{a_1/a_3}$, respectively, according to Eqts. (2.14) and (2.15). Below the drain current density of 43.8μA/μm, both a_1 and a_2 increase with the bias current and therefore IIP_2 is fairly constant. Beyond that point, IIP_2 increases rapidly because a_2 is decreasing in value. The IIP_3 reaches a local peak of 9.67dBV at 43.8μA/μm, which coincides with the same biasing current density for a zero value of a_3 as shown in Figure 5.6(a). The above simulations are performed by AC shorting the transistor's input and output terminals to ground in order to characterize the nonlinearity caused by the DC I_{DS}-V_{GS} relationship. Applying second harmonic terminations at the input and output of the transistor reduce the odd-order intermodulation distortions, but the DC point for optimal IIP_3 remains valid [5.6].

The transistor simulated in Figure 5.6 reaches an optimum IIP_3 value when biased at a current density of 43.8μA/μm. However, this could also result in an

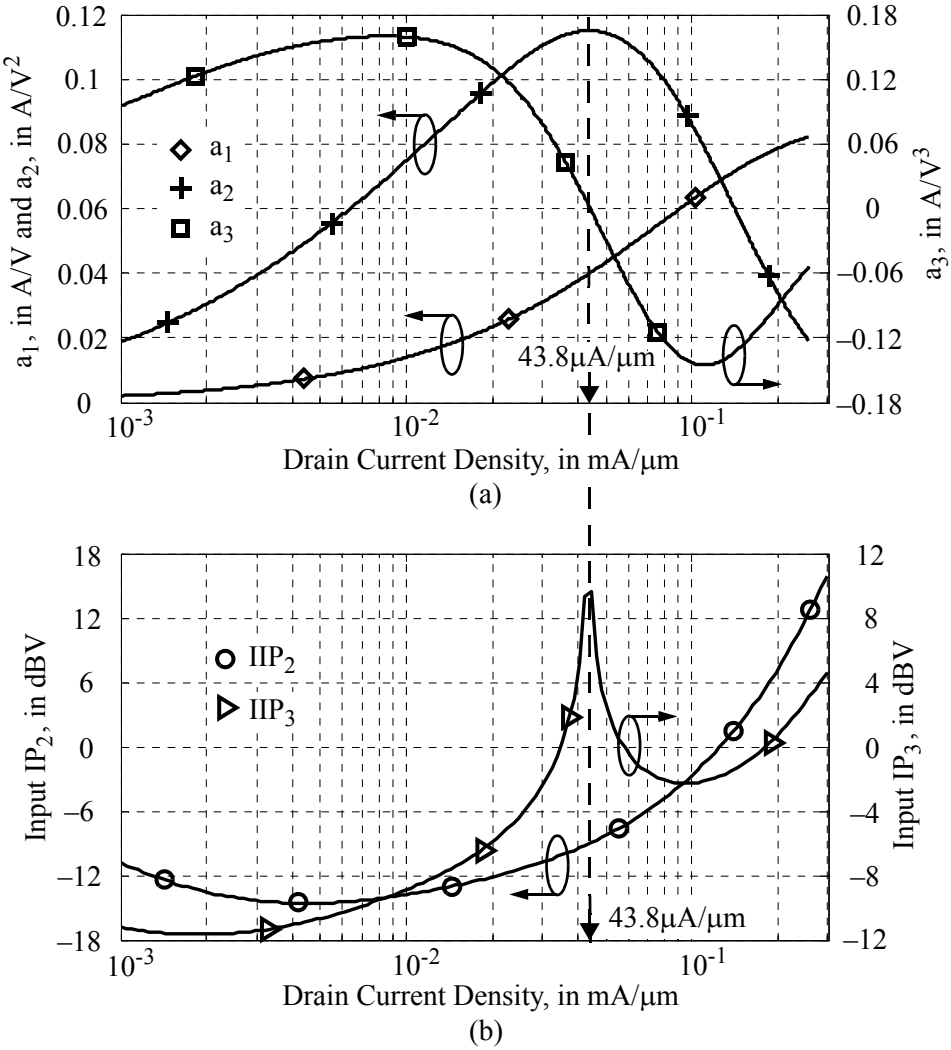

Figure 5.6 Simulated characteristics of a 50×2μm/90nm NMOS amplifier (a) transconductance series coefficients a_1, a_2 and a_3, (b) input IP_2 and IP_3 at 24GHz

overdesign on the linearity specification which wastes DC power. Table 5.1 specifies –10dBm IIP_3 for the LNA, which is equivalent to –20dBV for a source and load impedances of 50Ω. Selecting a transistor with 0dBV IIP_3 gives 20dB design margin from this LNA requirement. Given the data shown in Figure 5.6(b), a current density of either 34.6μA/μm, 58.2μA/μm, or 180μA/μm all deliver the same 0dBV IIP_3 required from the transistor. Therefore, a careful selection of transistor gate width can optimize the transistor DC bias point for linearity performance with the lowest current budget.

The even-order distortion products appear as a common-mode signal in differential operation [5.15]. Instead of boosting the current density for a higher IIP_2, maintaining the symmetry of a differential circuit results in cancellation of common-mode distortion products and therefore a high IIP_2 performance. AC coupling between the LNA and mixer attenuates the low-frequency, even-order distortions generated by the LNA. Therefore IIP_2 is usually a problem for mixer design but not for the LNA. A single-ended LNA implementation (with strong a_2 coefficient) could therefore save half of the bias current with little degradation in the receiver IIP_2.

5.2.4 Device Sizing for Bandwidth

For a given DC bias current, a reduction of transistor width increases the drain current density and hence improves the power gain and noise figure performance as explained in Sections 5.2.1 and 5.2.2. However, a smaller transistor width results in a lower input capacitance and a higher output resistance, giving high impedance levels at both the amplifier input and output terminals. This is detrimental to the bandwidth of both the input and output matching networks. The transistor's gate width optimization is therefore partly determined by the bandwidth requirement.

A series RLC resonant tank gives a –3dB bandwidth of $\omega_o^2 RC$ at the resonant frequency (ω_o) [5.16]. Therefore, the input bandwidth of different amplifier topologies can be compared relatively using the RC time constant (τ_{RC}) of the amplifier's input impedance as a quantifier.

For a 50×2μm/90nm NMOS transistor biased at 15μA/μm, the common-source amplifier with the drain terminal AC grounded has an input impedance of 9.41 – j60.0Ω at 24GHz. This is equivalent to a τ_{RC} of 1.04ps. The bandwidth of a common-source amplifier can be improved by using a longer finger width, which increases the gate resistance and therefore the RC time constant, but at the cost of a higher NF_{min} as illustrated in Figure 5.4.

Source degeneration with an inductor is seen as a positive resistance in series with the gate terminal [5.7], and this increases the input RC time constant. Applying the same 50×2μm/90nm NMOS transistor with a 200pH (Q=15) to the source, the simulated input impedance is 36.7 – j56.7Ω and τ_{RC} is 4.29ps. This simple arrangement gives a four times larger τ_{RC} compared to the simple common-source amplifier.

A common-gate amplifier offers advantages in wideband performance because the resistance seen at the source terminal is $1/g_m$. For low-power design, this input resistance is much higher than the parasitic gate resistance. The same 50×2μm/90nm NMOS transistor is simulated by tying the gate and drain DC bias at 1.0V. The simulated input impedance and τ_{RC} being 40.4 – j20.8Ω and 13.5ps,

respectively. The τ_{RC} from common-gate is 13 and 3 times larger than that from the common-source amplifier with or without source degeneration, respectively. As a result, a common-gate amplifier can use a narrower width transistor with smaller capacitance while maintaining a similar bandwidth to a common-gate amplifier. A narrower width transistor with a fixed current budget increases the drain current density, and therefore improves the power gain, noise figure and linearity characteristics. However, this also requires a larger gate-source overdrive voltage for a given bias current, and demands higher supply voltage headroom in order to accommodate the DC biasing requirements.

5.2.5 Device Sizing for Passive Matching Network Loss

The forward transmission coefficients ($|S_{21}|$) shown in Figures 5.2 and 5.3 illustrate the active gain of the MOS transistor for a 50Ω source and load in the common-source and common-gate topologies. MOS transistors have low active gain, and the separation between the MAG/MSG and $|S_{21}|$ in these curves is due to the change in gain from the addition of input and output matching networks [5.10]. Passive matching components, such as on-chip inductors in standard CMOS technology, suffer from a relatively low Q-factor (e.g., ranging from 3 to 20) due to the conductive silicon substrate and thin interconnect metal layers. Therefore, the noise performance of CMOS mm-wave amplifier is likely to be worse than the NF_{min} of the intrinsic device.

However, the overall noise figure is usually dominated by the first stage amplifier. For example, Friis' formula [Eqt. (2.22)] predicts that a 10dB power gain from the first stage reduces the contributions of the following stages to the overall noise factor by 90%. Furthermore, it is usually only the input of an RF receiver that must be conjugate matched to a 50Ω source (e.g., an antenna). Therefore, only the input matching loss of the LNA is taken into account in the optimization process.

Although the optimization procedure described in this section is applicable to different amplifier topologies, only the common-source NMOS amplifier is presented here as an example. Consider an ideal noiseless amplifier where the equivalent input voltage and current noise sources are represented by $\overline{v_{in,MOS}^2}$ and $\overline{i_{in,MOS}^2}$, respectively. Two types of matching network are considered for transforming the transistor input impedance to a specified input impedance. They are shown in Figure 5.7(a) for a series inductor L_s, and in Figure 5.7(b) for a parallel inductor L_p. Their resistive losses are modeled by R_s and R_p with

$$R_s = \omega \cdot L_S / Q \tag{5.1}$$

and

$$R_p = \omega \cdot L_p \cdot Q. \tag{5.2}$$

A high quality factor (Q) implies a small R_s and a large R_p. Their noise powers are represented by the equivalent voltage and current source mean square pow-

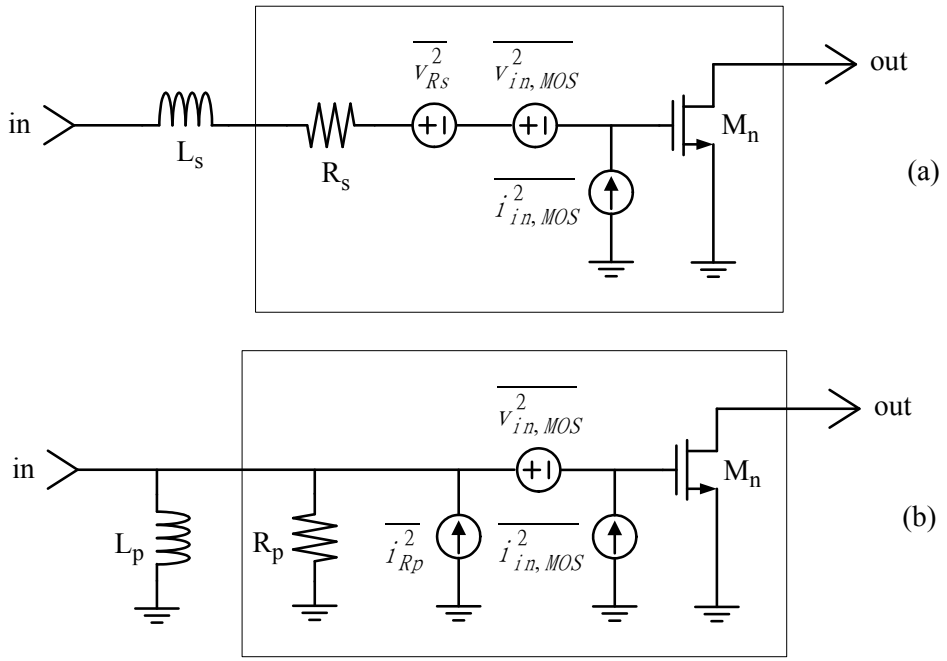

Figure 5.7 Equivalent input noise sources including contribution from (a) series and (b) parallel input matching networks

ers of $\overline{v_{Rs}^2}$ and $\overline{i_{Rp}^2}$, as given by Eqts. (2.3) and (2.4), respectively. Noise produced by the matching network or active device are uncorrelated.

In order to simplify the analysis, the flicker noise component is ignored. Eqts. (2.5) and (2.6) can be simplified as

$$\overline{v_{in,MOS}^2} = 4kT \cdot \frac{\gamma}{g_m} \cdot BW \tag{5.3}$$

and $$\overline{i_{in,MOS}^2} = \left(\frac{4\pi}{3} C_{ox} WL \cdot f\right)^2 \cdot \overline{v_{in,MOS}^2} = (C_{gs} \cdot \omega)^2 \cdot \overline{v_{in,MOS}^2}, \tag{5.4}$$

with the parameters as defined in Section 2.1.1. For a single NMOS transistor, the equivalent input voltage and current noise sources are fully correlated to one another by the scaling factor ($C_{gs} \cdot \omega$), which is proportional to the operating frequency and transistor dimensions. A smaller area device shows a larger amount of voltage noise than current noise. This factor becomes unity for a C_{gs} of 6.63pF at 24GHz, which equivalent to a transistor width of 6mm in the 90nm CMOS technology. Therefore, voltage noise is usually the dominant input noise source for typical device dimensions.

Considering only the drain current (thermal) noise, the noise powers of Eqts. (5.3) and (5.4) are fully correlated. Therefore, the correlation admittances [5.17]

between $\overline{v_{in,MOS}^2}$ and $\overline{i_{in,MOS}^2}$ are

$$G_c = \sqrt{\frac{\overline{i_{in,MOS}^2}}{\overline{v_{in,MOS}^2}}} \tag{5.5}$$

and

$$G_u = 0. \tag{5.6}$$

Substituting Eqts. (5.5) and (5.6) into the minimum noise figure equation in [5.17], the noise factor becomes

$$F_{min} = 1 + \frac{\sqrt{\overline{v_{in,MOS}^2} \cdot \overline{i_{in,MOS}^2}}}{4kT \cdot BW}, \tag{5.7}$$

where k is Boltzmann's constant, T is absolute temperature, and BW is bandwidth.

As illustrated in Figure 5.7, the inclusion of passive matching network noise into the minimum noise figure equations is equivalent to lumping $\overline{v_{Rs}^2}$ into $\overline{v_{in,MOS}^2}$, or $\overline{i_{Rp}^2}$ into $\overline{i_{in,MOS}^2}$. This also reduces the correlation between the resultant voltage and current noises. Their impact on the minimum noise figure depends on the relative rms power level of $\overline{v_{in,MOS}}$ and $\overline{i_{in,MOS}}$ in the product term of Eqt. (5.7). This is conceptually illustrated in Figure 5.8 for variation in the product of the voltage and current noise rms powers from 0.1 to 1.0. If the rms voltage noise is much higher value than the rms current noise, as indicated in region A, the overall noise figure is much more tolerant of the additive series resistor voltage noise of $\overline{v_{Rs}^2}$ because a large increase in the voltage noise rms power only gives a small increase in the

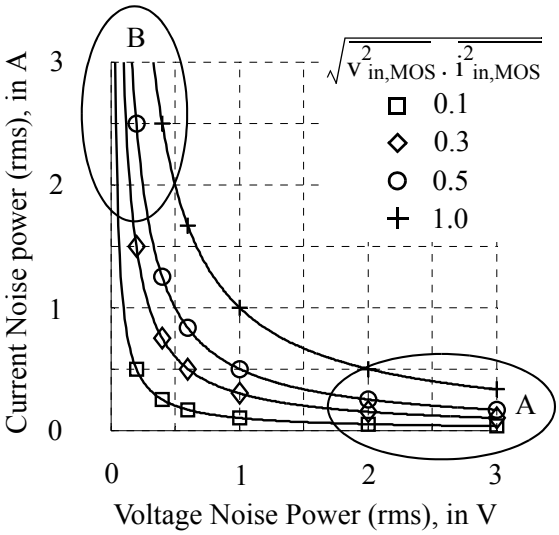

Figure 5.8 Simulated effects of voltage and current noise rms power level on the noise factor in Eqt. (5.7)

noise product of $\sqrt{\overline{v^2_{in,MOS}}} \cdot \overline{i^2_{in,MOS}}$. A similar observation can be made for the current noise $\overline{i^2_{Rp}}$ contributed by a parallel resistor in region B.

The influence of the passive matching network losses on noise figure is quantified by merging the matching network noise, modelled by a resistor, and the NMOS transistor to form a composite device (enclosed by the rectangular boxes as shown in Figure 5.7). For the series matching network of Figure 5.7(a), minimum noise figure was simulated for varying R_s resistance values from 1Ω to 100Ω. For a fixed finger width of 2μm (i.e., optimized width from Sections 5.2.1 and 5.2.2), simulations of six gate widths ranging from 10μm to 200μm (i.e., increasing number of fingers) illustrate the influence of transistor sizing on the NF_{min} tolerance to the series noise. The results are plotted in Figure 5.9 for a drain current density of 15μA/μm and operating frequency of 24GHz.

The noise contribution from the series resistance is much less significant for a smaller width transistor, or equivalently, the relatively high input noise voltage of a smaller transistor can accommodate larger values of series gate resistance (R_s) and inductance (L_s). This result aligns with the observation in the region A of Figure 5.8 where $\sqrt{\overline{v^2_{in,MOS}}} \gg \sqrt{\overline{i^2_{in,MOS}}}$ for a smaller device size.

The simulation results for gate widths of 30μm and 150μm are compared with only consider the effect of inductor Q on the amplifier NF_{min}. If the inductor that is parallel resonant to the 150μm wide transistor has inductance L_{150} and equiv-

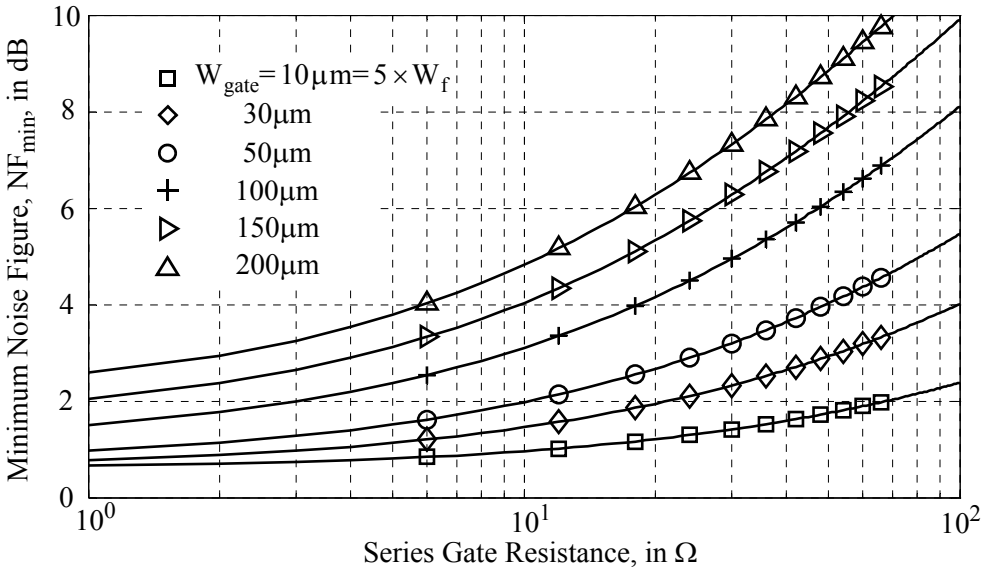

Figure 5.9 Simulated minimum noise figure of a common-source amplifier with 90nm channel length versus series gate resistance for different gate widths at 24GHz (W_f=2μm)

alent series resistance R_{150}, smaller transistor (having one-fifth of the capacitance) requires an inductance of $L_{30} = L_{150} \times 5$ (with series resistance R_{30}) in order to maintain the same resonant frequency. For an expected NF_{min} of 4dB, the maximum tolerable series gate resistance for the 30μm and 150μm transistors are 100Ω and 10Ω, respectively, as shown in Figure 5.9.

For the first situation where inductor Q is independent of inductance value, an assumption of $R_{150} = 10\Omega$ easily derives $R_{30} = R_{150} \times 5 = 50\Omega$. In other words, the smaller transistor has a margin of 50Ω for the gate resistance which is unused. Therefore, a smaller transistor can potentially give a lower NF_{min} at the given resonant frequency.

Now consider the case where inductor Q depends on the inductance value. With $R_{150} = 10\Omega$, $R_{30} = 100\Omega$ and $L_{30} = L_{150} \times 5$,

$$Q_{150} = (\omega \cdot L_{150}) / R_{150} = (\omega \cdot L_{150}) / 10 \tag{5.8}$$

and

$$Q_{30} = (\omega \cdot L_{30}) / R_{30} = (\omega \cdot L_{150}) / 20 . \tag{5.9}$$

In other words, the smaller transistor gives a lower NF_{min} as long as $Q_{30} > Q_{150} / 2$. Without considering the occupied silicon area and practical range of inductance values (e.g., due to self-resonant frequency), a smaller device size is usually favorable for minimizing NF_{min} with a series matching network.

The same 150μm wide transistor is simulated with the parallel matching network and the results are shown in Figure 5.10. The parallel gate resistance varies

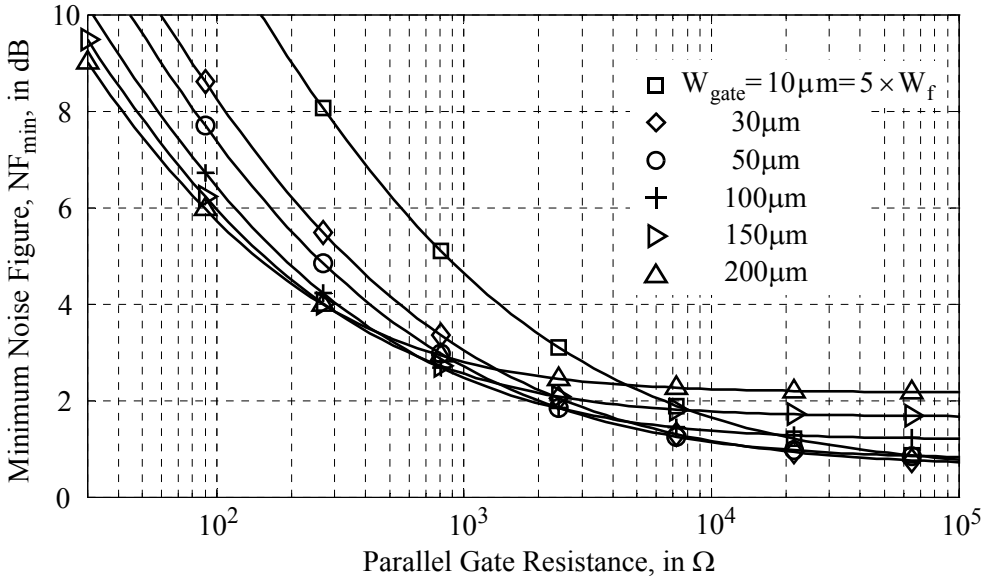

Figure 5.10 Simulated minimum noise figure of a common-source amplifier with 90nm channel length versus parallel gate resistance for different gate widths at 24GHz (W_f=2μm)

from 300Ω to 100kΩ. In this case, a larger resistance corresponds to a higher Q, and therefore a lower current noise power due to the parallel resistor. For a NF_{min} of 4dB, the parallel gate resistance has much less effect on the noise of the larger transistor, or equivalently, a larger device can accommodate a higher input current noise. Although the maximum gate width of 200μm illustrated in Figure 5.10 is much smaller than the 6mm width derived in Eqt. (5.4), the current noise dependency in region B of Figure 5.8 where $\sqrt{\overline{v^2_{in,MOS}}} \ll \sqrt{\overline{i^2_{in,MOS}}}$ for a larger device size is still observable in Figure 5.10.

5.3 Optimization at the Circuit Level

Given the power consumption of the LNA specified in Table 5.1, distribution of the current and voltage budget across a cascade of stages shows advantages over a single-stage amplifier for power gain. However, applying a lower bias current to each stage deteriorates the minimum noise figure achievable. Optimization of the interface between gain stages is necessary in order to preserve the power gain and noise figure.

5.3.1 Current and Voltage Budget Partitioning

The advantage of partitioning the current budget is illustrated by analyzing the power gain data shown in Figures 5.2 and 5.3. Consider the common-source configuration, where a drain current density of 0.01mA/μm is taken as a reference unit and about 5dB of MSG is achieved for an optimized transistor gate width. Doubling or quadrupling the drain current density for a single-stage amplifier boosts the power gain by 2.09dB or 4.13dB, respectively. However, maintaining an amplifier at the reference current and cascading two or four stages gives a potential increase in the power gain of 5.36dB or 16.1dB, respectively. Similar observations are made for the common-gate, where cascading two or four stages increases the power gain by 5.98dB or 17.9dB, respectively, compared to the 0.70dB or 1.34dB improvement available from a single-stage amplifier for a two or four times increase in the drain bias current, respectively.

A much higher power gain seems possible by fixing the unit current reference to an even lower value and using a higher number of cascade stages. However, the number of inter-stage passive matching networks also grows with the number of stages. These matching networks occupy a large silicon area and complicate the floor planning of bulky passive components in order to minimize their parasitic couplings. Furthermore, NF_{min} and IIP_3 are degraded at lower drain current densities, and there are increased contributions from multiple of stages. Meeting the overall noise figure and linearity specifications also sets an upper limit on current budget and its partitioning in a cascade amplifier design.

Subdividing the supply voltage headroom between multiple amplifier blocks (in DC cascode) takes the advantage of current sharing at the cost of a lower

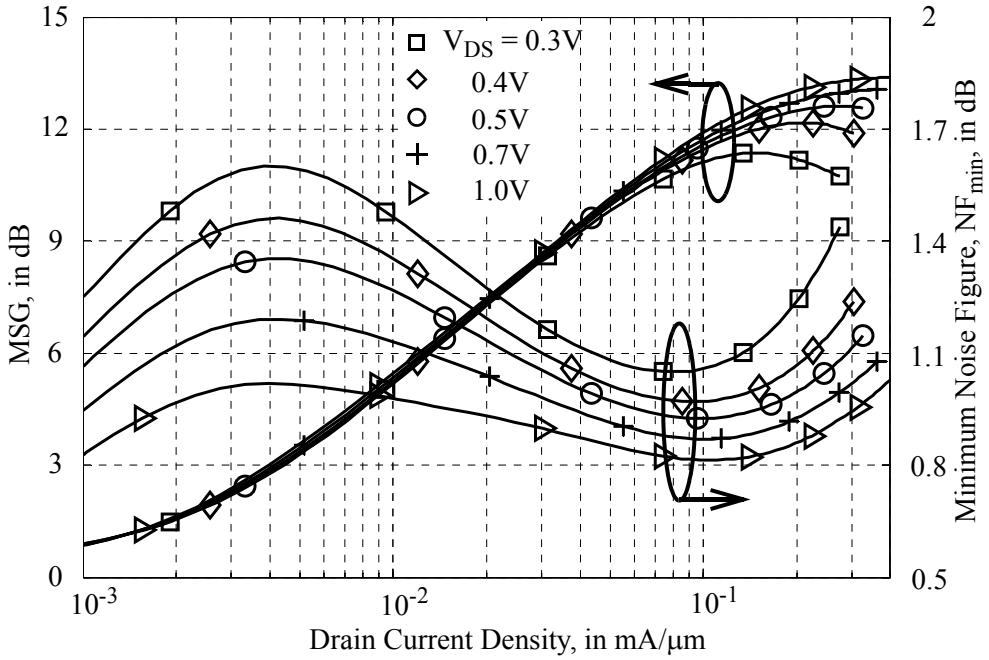

Figure 5.11 Simulated MSG and NF_{min} of a common-source amplifier versus drain current density for different V_{DS} at 24GHz

drain-source voltage across each MOS transistor, which may push it out of the saturation and into the linear region. For the common-source configuration, the degradation in MSG and NF_{min} are simulated for different drain-source voltage versus the drain current density. The results are shown in Figure 5.11 for a 50×2μm/90nm NMOS transistor operating at 24GHz. Significant influence of V_{DS} on the power gain is observable only at current densities higher than 0.1mA/μm, where the transistor operates in the strong inversion region with a high gate-source overdrive voltage. It requires a higher V_{DS} to maintain the saturated condition. The noise figure performance favors a higher V_{DS}, but the degradation is less than 0.3dB for drain current density ranging from 0.02mA/μm to 0.1mA/μm, and V_{DS} ranging from 0.3V to 1.0V.

The influence of V_{DS} on the common-gate configuration is simulated for the same transistor but with the gate terminal tied to 1.0V. The results shown in Figure 5.12 reveals a high dependence of the power gain on V_{DS}. This is because the inverted channel of the MOS transistor makes a direct connection between the drain and source terminals. Lowering the drain-source voltage pushes the transistor closer towards the triode region, which immediately causes the power gain to drop across the drain current density range. From Figure 5.12, the noise figure performance also favors a higher drain-source voltage.

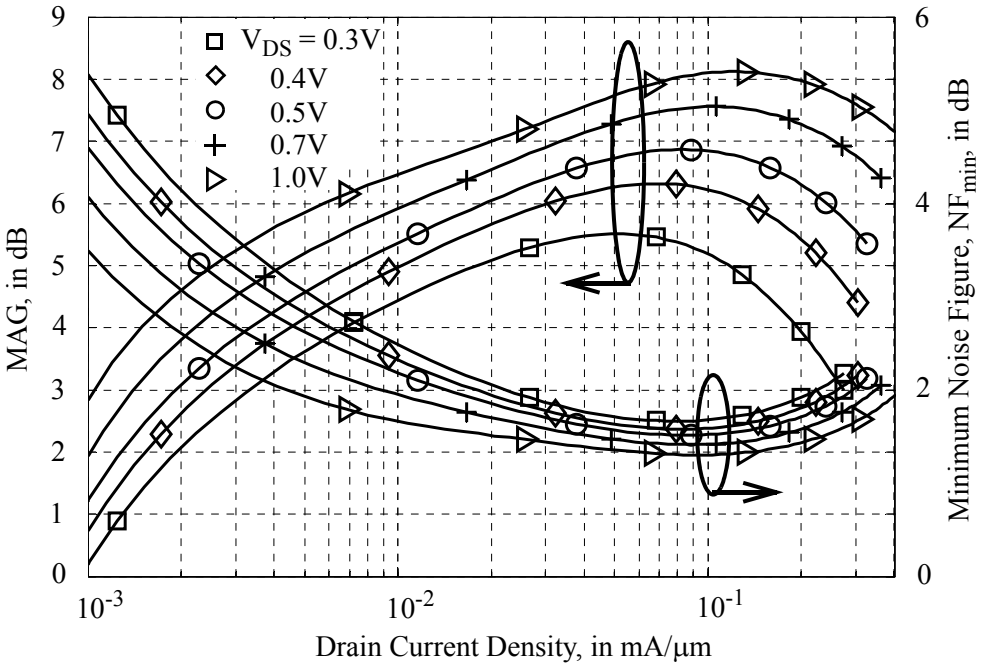

Figure 5.12 Simulated MAG and NF_{min} of a common-gate amplifier versus drain current density for different V_{DS} at 24GHz

5.3.2 Impedance Matching Conditions for Cascaded Stages

Optimization procedure for composite amplifier structures, such as cascode [5.9] or multicascode [5.18], typically require sweeps of the individual transistors dimensions in order to maximize the MAG/MSG parameters. By considering a cascode amplifier, this procedure hinders the convergence to an optimal result because the possibility of impedance matching between the common-source and common-gate stages is ignored. In fact, a careful selection of interface impedance is critical to the power gain and noise figure optimization.

Because of the short interconnection between amplifier cells on an integrated circuit, conjugate matching to minimize power reflections is not necessary. Instead, the background information explained in Sections 2.1.1 and 2.2 form the basis for optimizing the inter-stage impedance matching conditions. This can be divided into consideration of the internal requirements and external influences, as summarized by the system block diagrams shown in Figure 5.13.

The difference between the noise figure and NF_{min} for an amplifier depends on how closely the source impedance (Z_{source}) approaches the optimum source impedance (Z_{opt}) for minimum noise figure. Z_{opt} is independent of Z_{load} as long as the equivalent input noise sources of the amplifier block shown in Figure 5.13 are independent of Z_{load}. The MAG of the each amplifier stage has to be maximized in

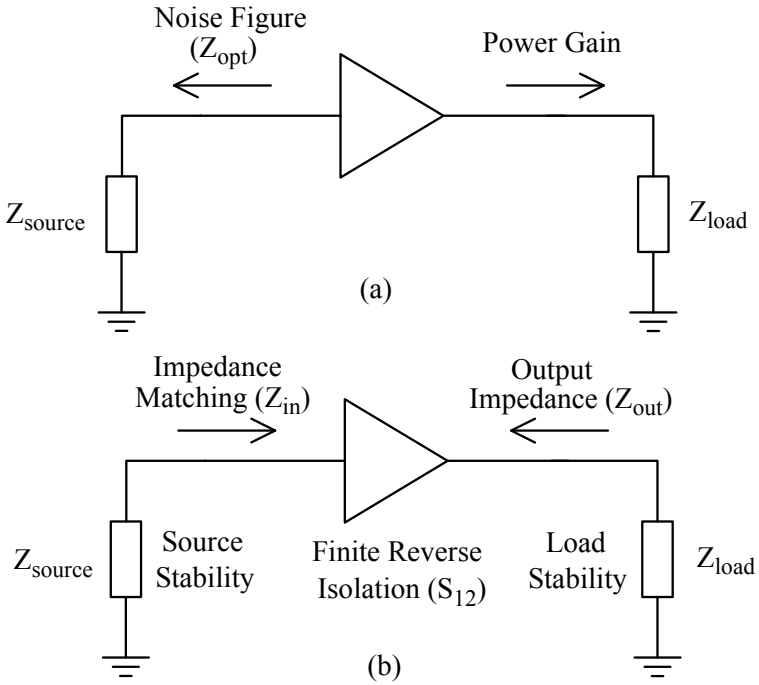

Figure 5.13 Matching conditions for (a) requirements and (b) mismatch effects from source and load impedances

order to minimize the cascade noise figure as given by Eqt. (3.36). The amplifier operating power gain is maximized by appropriate selection of the load impedance (Z_{load}) on a power gain circle for a particular gain value. These terminal impedance requirements on the amplifier performance optimization are summarized in Figure 5.13(a).

The S-parameters of the amplifier have a direct influence on the source and load impedance selection. This is summarized in Figure 5.13(b). These impedance values have to remain within the source and load stability circle boundaries. If the amplifier belongs to the first stage of the cascade, conjugate matching is necessary at the input (i.e., Z_{source} match to Z_{in}). Otherwise, Z_{in} of the succeeding stage has to be matched to maximize power gain from the preceding stage [i.e., Z_{load} in Figure 5.13(a)]. For an amplifier having finite isolation (S_{12}), Z_{in} is influenced by the load impedance (Z_{load}) which must be taken into account for the power gain optimization. Similarly the output impedance (Z_{out}) is influenced by Z_{source} and it is also a determining factor for the noise figure performance of the succeeding stage.

5.3.3 Feedback Based Impedance Matching

For most amplifier topologies, the optimum source (Z_{opt}) and input (Z_{in}) impedances are not conjugate, but share a fixed relationship. Meeting the condition in Fig-

ure 5.13(a) for minimum noise figure cannot satisfy the input impedance requirements in Figure 5.13(b) for either maximum power transfer from the antenna, or delivering maximum operating power gain for the preceding stage.

Two feedback schemes are considered for the common-source configuration which decouple the relationship between Z_{opt} and Z_{in} in order to realize simultaneous noise and power matching. The inductive (L_s) source degeneration [5.7] of a transistor with transconductance g_m and gate-source capacitance C_{gs} shown in Figure 5.14(a) gives good bandwidth performance as described in Section 5.2.4. By ignoring the transistor's gate-drain capacitance and using a hybrid-π small-signal model for the transistor, its input impedance is given by

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + g_m \frac{L_s}{C_{gs}} . \tag{5.10}$$

The shunt-series feedback by L_s modifies Z_{in} by introducing a resistive term $g_m L_s / C_{gs}$. It has a similar, but much smaller effect on Z_{opt} [5.19], which can be accurately captured with the aid of computer simulations. Degeneration also lowers the power gain. Therefore, the smallest possible value of L_s should be used that satisfies the simultaneous matching conditions.

The gate-drain capacitance C_{gd} shown in Figure 5.14(b) is parasitic to the CMOS transistor. It introduces bilateral power flows between the input and output terminals [5.19]. Due to the shunt-shunt feedback by C_{gd}, the load impedance Z_{load} modifies Z_{in} but has minimal effect on Z_{opt}. This provides an additional degree of freedom when decoupling Z_{opt} and Z_{in}. Placing additional capacitance in parallel to C_{gd} as a design parameter [5.20] would degrade the transistor power gain and reverse isolation performance. Therefore, optimization for impedance matching is only taken around the intrinsic gate-drain parasitic capacitance (i.e., no capacitance

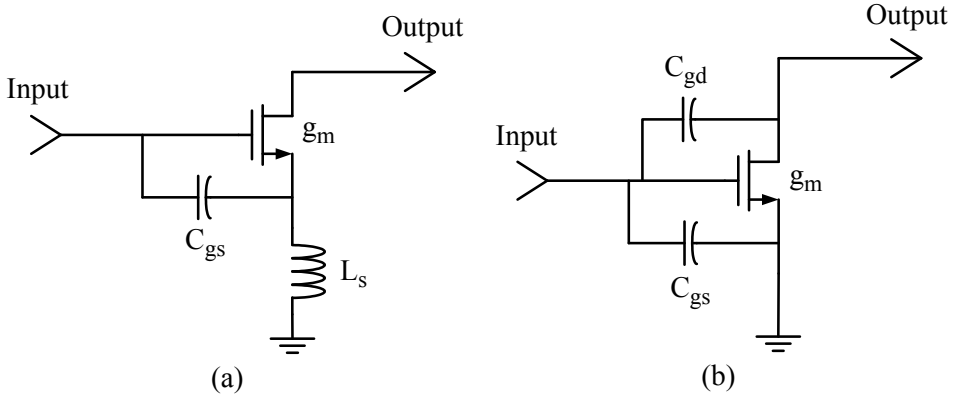

Figure 5.14 Feedback schemes applied to common-source amplifier. (a) Inductive source degeneration by L_s. (b) Shunt capacitor C_{gd}.

is added). By using a small-signal transistor model, the input admittance is given by

$$Y_{in} = sC_{gs} + sC_{gd} + \frac{sC_{gd} \cdot (g_m - sC_{gd})}{\frac{1}{Z_{load}} + sC_{gd}}, \tag{5.11}$$

where a conductance term is introduced in parallel with the two capacitive components. Because C_{gd} is small (but non-negligible), the influence on Z_{in} from Z_{load} in Figure 5.14(b) is much less than the influence on Z_{in} from L_s in Figure 5.14(a). By applying both feedback schemes to a common-source amplifier, simultaneous noise and power matching is achieved with minimum degradation on the power gain.

5.3.4 Smith Chart Based Bilateral Optimization Methodology

Unilateral stages permit independent design of the input and output matching networks. This eases the LNA optimization process. On the other hand, simultaneous noise and power matching by feedback schemes, such as applying inductive source degeneration together with a shunt capacitive feedback to a common-source amplifier (as described in Section 5.3.3) is an example of bilateral design. It must take the reverse signal flow in an amplifier stage into account for the design of matching networks and the choice of the source degeneration inductance. With the advancement of CAD tools, an efficient Smith chart based design methodology that is based solely on S-parameters simulations was presented in [5.1]. It elucidates a procedure for manipulating the bilateral LNA optimization.

After following the guidelines derived in Section 5.2 for selecting optimal gate and finger widths, drain bias voltage and current density, the amplifier noise and power gain circles are computed as described in Sections 2.1.1 and 2.2. Input impedance values are then simulated for load impedances ranging from the inductive to capacitive regions. When plotted on the Smith chart, the load and input impedance for a simultaneous noise and power match are obvious. The operating power gain for the amplifier is found by mapping the selected load impedance to the power gain circles. The optimization goal is to realize a matched input and output with maximum power gain and minimum noise figure. Linearity is maintained by the optimal biasing outlined in Section 5.2.3, and will be verified after selection of the inter-stage matching networks.

The optimization begins without the source degeneration inductance. If simultaneous matching cannot be met or the resultant power gain is too low, the inductance value is increased progressively in order to minimize any power gain reduction. The optimization procedure is then repeated. Source and load stability margins are monitored at each step.

An example is illustrated in Figure 5.15 for a $50 \times 2\mu m/90nm$ NMOS transistor without degeneration inductance, and biased at 1.5mA and 0.5V drain-source voltage at 24GHz. The optimum source impedance (Z_{opt}) for minimum noise figure is approximately $12.41 + j73.95\Omega$ with a NF_{min} of 1.19dB. Shown in the lower-right

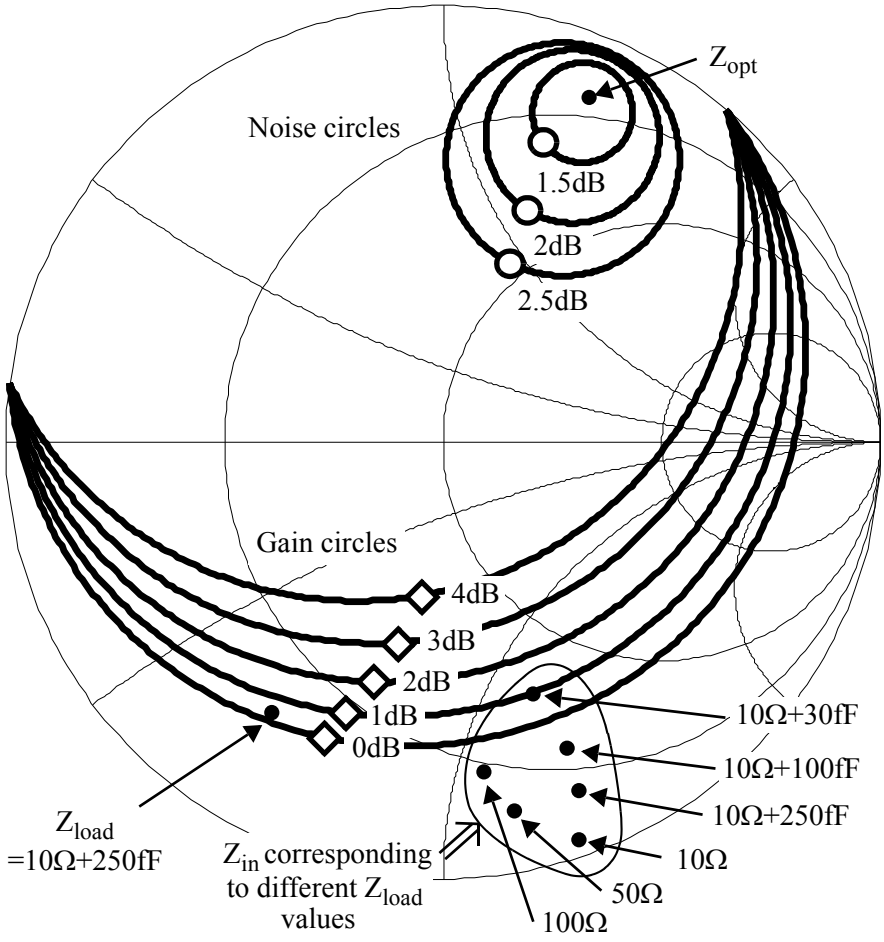

Figure 5.15 Simulated input impedance as a function of load impedance for a common-source amplifier without degeneration at 24GHz

region of the Smith chart are the input impedances (Z_{in}) of the amplifier corresponding to different load impedances (Z_{load}). With a Z_{load} of $10 - j26.5\Omega$ (i.e., $10\Omega + 250\text{fF}$), Z_{in} is conjugate matched to Z_{opt}, and simultaneous noise and power matching is possible without inductive degeneration. However, this Z_{load} impedance (plotted in the lower-left region) lies on the power gain circle of 0.42dB. Thus, the operating power gain available for the matched LNA is only 0.42dB out of the simulated 6.49dB MSG available from the transistor. This power gain value is too low to be useful as a amplifier.

The design flow is repeated with the addition of a source degeneration inductance. This allows one to realize simultaneous noise and power matching at the cost of gain degradation. For a progressive increase in the source degeneration inductance, the noise and power matched conditions are monitored along with the

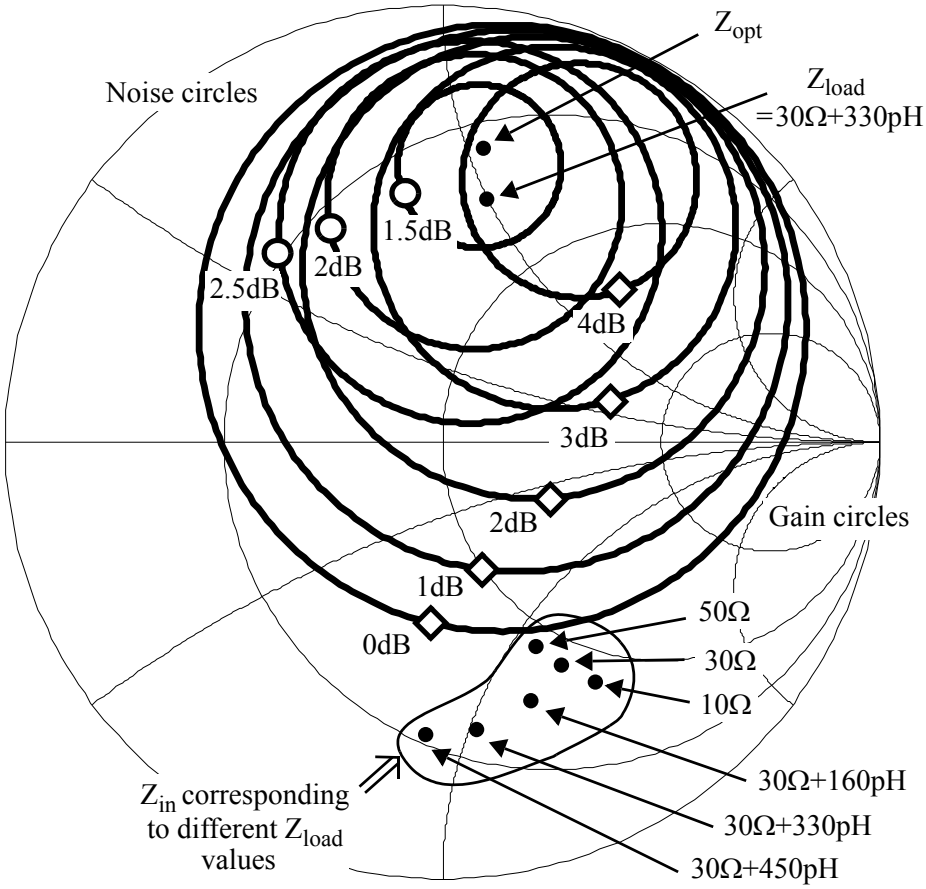

Figure 5.16 Simulated input impedance as a function of load impedance for a common-source amplifier with 240pH degeneration at 24GHz

available power gain from the amplifier. Figure 5.16 illustrates another example for a L_s of 240pH. The degenerated transistor is unconditionally stable with a MAG of 4.88dB. There is a power gain drop of 1.6dB compared to the simple common-source amplifier. The Z_{opt} is simulated to be 21.00 + j52.51Ω with a minor increase in NF_{min} to 1.27dB. The matched condition at the input is realized for Z_{load} of 30 + j49.8Ω (i.e., 30Ω + 330pH), and the power gain is 4.19dB. This is a drop of 0.69dB from the MAG limit. This result demonstrates that a matched LNA design is realizable in the technology at 1.5mA bias current and within the 0.75mW power budget.

The preceding optimization procedure assumes ideal matching components. Losses from the matching network can be estimated and modeled as a lumped resistor in series (or in parallel) to the NMOS transistor depending on the input matching network design as described in Section 5.2.5. The design is iterated as described

previously, until a simultaneous noise and power match matched condition is attained with maximum power gain.

The second stage of the cascade amplifier is optimized using a similar procedure with the exception that Z_{opt2} of the second stage is matched to Z_{out1} of the first stage as shown in Figure 5.13(a). Z_{in2} of the second stage is also matched to the required Z_{load1} of the first stage as given in Figure 5.13(b). These matching requirements are again facilitated by the two feedback schemes introduced in Section 5.3.3, together with an explicit inter-stage impedance transformation network similar to the one described in [5.1].

5.4 Design Examples

Three 24GHz LNAs are designed and compared in order to demonstrate the advantage of the proposed optimization algorithm. The design parameters and simulated performance of these amplifiers are summarized in Table 5.3.

A common-source NMOS amplifier is proposed to highlight the limitation of a single-stage amplifier for low-power operation. With a 1V supply and a 3mW power budget, the transistor's drain current is set at 3mA. The gate width is chosen at 100μm from bandwidth considerations, and a finger width of 2μm is selected in order to optimize power gain and noise figure. Therefore, the drain bias current density is 30μA/μm. From Figure 5.11, the transistor has only a MSG of 8.7dB. A lower supply of 0.5V increases the current density to 60μA/μm and subsequently the MSG to 10.5dB. A source degeneration inductance (L_s) of 100pH improves the

Table 5.3 Comparison of single-stage, cascode, and 4-stage cascade amplifiers

Parameter	Single-stage	Cascode	4-stage cascade
Transistor width	2μm × 50	C-S: 2μm × 50 C-G: 1μm × 100	2μm × 50 per stage
Drain current density	60μA/μm	30μA/μm	15μA/μm
Supply voltage	0.5V	1.0V	0.5V
Total drain current	6mA	3mA	6mA
L_s	100pH	100pH	240pH per stage
Z_{in}	31.5 – j41.8 Ω	29.8 – j55.0 Ω	32.2 – j47.9 Ω
Z_{opt}	18.3 + j59.9 Ω	30.7 + j57.2 Ω	24.0 + j50.8 Ω
Z_{load}	50Ω	50Ω	50Ω
Power gain	9.27dB (MSG)	11.8dB (MAG)	16.5dB (MAG)
NF_{min}	0.906dB	2.77dB	1.93dB
IIP_3	–0.065dBV	–2.18dBV	–11.63dBV

bandwidth performance and facilitates simultaneous noise and impedance matching at the LNA input. The amplifier is conditionally stable at 24GHz and delivers a power gain of 9.27dB and NF_{min} of 0.906dB. The Z_{in} and Z_{opt} are not exact conjugates. However, accurate noise matching at the LNA input is not necessary because NF_{min} is much lower than the 5dB NF specification, so backing off the source impedance from Z_{opt} is possible. From Figure 5.11, IIP_3 of the intrinsic transistor is –0.569dBV at a current density of 60μA/μm. The degeneration inductor provides some linearization and therefore the LNA IIP_3 improves to –0.065dBV. From the data shown in Figure 5.11, a single-stage amplifier can never meet the 15dB power gain requirement.

A higher power gain is possible from the cascode topology. This amplifier is designed by re-using the common-source amplifier with an additional cascode transistor. The supply voltage is increased to 1V but the total drain current is lowered by half to 3mA. The cascode transistor's gate width cannot be shorter than 100μm in order to leave about 0.5V voltage headroom for the bottom common-source transistor, and it's finger width is 1μm from the optimization results of Section 5.2.1 and Section 5.2.2. This amplifier is unconditionally stable and has a power gain improvement of 2.53dB compared to the single-stage amplifier. However, NF_{min} and IIP_3 are degraded by 1.86dB and 2.12dB, respectively. In this design, Z_{in} and Z_{opt} closely match each other.

A 4-stage cascade amplifier is designed by following the Smith chart based bilateral optimization methodology illustrated in Section 5.3.4. The example in Figure 5.16 is extended by another three cascaded stages. Each amplifier stage is identical with the optimized gate and finger width. Except for the first stage, the input matching network of each stage consists of a 25pH series inductance connected to the gate, and then shunted by a 250pH inductance to the supply rail. Simulations predict that this amplifier is unconditionally stable. Conjugate matching between Z_{opt} and Z_{in} behaves better than that of the single-stage amplifier because mismatch between the real and imaginary parts of Z_{opt} and Z_{in} are reduced by 38% and 24%, respectively.

Although the transistors in this 4-stage cascade amplifier have the lowest drain current density compared to those in the other two LNAs, only this amplifier can exceed the 15dB power gain specification by delivering a 16.5dB MAG. It's power gain is 7.2dB and 4.7dB higher than that from the single-stage and cascode amplifiers, respectively. However, the low bias current density of the 4-stage amplifier at 15μA/μm also implies the worst noise figure (NF_{min} = 1.2dB from Figure 5.4) and linearity (IIP_3 = –7.40dBV from Figure 5.6) performance from the intrinsic transistor. Contributions of noise and intermodulation products in the four cascade stages, which are predicted by Eqts. (3.36) and (3.37), respectively, further exacerbate the noise figure and linearity of the LNA. Therefore, the difference

observed between the intrinsic transistor and the 4-stage LNA parameters on NF_{min} (degraded from 1.20dB to 1.93dB) and IIP_3 (degraded from –7.40dBV to –11.63dBV) are within expectations. These performance numbers are better than the LNA specifications.

These examples demonstrate the advantage of the proposed LNA optimization algorithm on maximizing power gain with low power consumption while preserving noise figure performance.

5.5 Summary

The chapter presented a two-step optimization procedure of a low-power mm-wave LNA focusing on the device and circuit levels. Device dimensions, terminal bias voltages and drain current density are optimized for the common-source and common-gate amplifier configurations with respect to power gain, noise figure, linearity, operating bandwidth, and passive device losses. Optimization of a single transistor in each configuration requires different dimensions. Amplifier noise figure immunity to the magnitude and type of resistive loss from passive impedance matching network (series or parallel resistance were considered) also depends of the transistor sizing. Partitioning the limited power budget across multiple of gain stages was shown to maximize the overall power gain achievable. Noise figure from a cascade of stages is minimized by meeting the inter-stage impedance matching conditions with the aid of two feedback schemes. Iterative optimization procedures for bilateral amplifier stages are facilitated by Smith chart based visualization and a computer-aided design methodology. The advantages of the proposed design procedure was illustrated using three examples and by comparing the performance outcomes. In Chapter 6, this design algorithm is applied to the optimization of a cascode low-noise amplifier and the radar receiving frequency down-converter.

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Chapter 6

LNA and 24GHz Frequency Downconverter

A cascode LNA bears the advantage of immediate DC and AC coupling between common-source and common-gate stages in a series (stacked) configuration. However, it suffers from suboptimal power gain and noise figure performance due to suboptimal interface impedances, as described in Chapter 5. This chapter examines this limitation and methods to overcome it, by applying current feedback around the common-gate amplifier. The feedback amplifier is shown to simultaneously satisfy the power gain and noise matching conditions required by the common-source amplifier. A 24GHz frequency downconverter is implemented by cascading this LNA with a mixer that is driven by the wideband VCO described in Chapter 4.

Three types of cascode amplifiers are examined from the perspective of inter-stage impedance matching in the first sections of this chapter. A current feedback technique using a 3-port transformer is then applied to the common-gate transistor. Circuit analysis of the proposed feedback scheme and a Smith chart based optimization procedure are then presented, together with performance comparisons for the three cascode amplifiers. This is followed by the design and implementation of a low-power LNA for the radar receiver. A Gilbert-type down-conversion mixer is then described with emphasis on the single-ended to differential interfacing towards the LNA. Finally, simulation and experimental results of the frequency downconverter testchips are detailed.

6.1 Low Noise Amplifier

The section explores the limitations of the cascode LNA and proposes a new cascode topology suitable for low-noise amplification at low power dissipation.

6.1.1 Limitations of Cascode LNAs

For the three amplifier topologies presented as design examples in Section 5.4, the cascade, 4-stage common-source LNA is the only candidate which satisfies the power gain specification. However, this LNA requires a 0.5V supply from the 1.0V (nominal) supply voltage of thin-oxide FETs in a 90nm CMOS technology [6.1]. This wastes 50% of the battery power unnecessarily via a linear voltage regulator whose efficiency is approximately equal to the output-to-input voltage ratio.

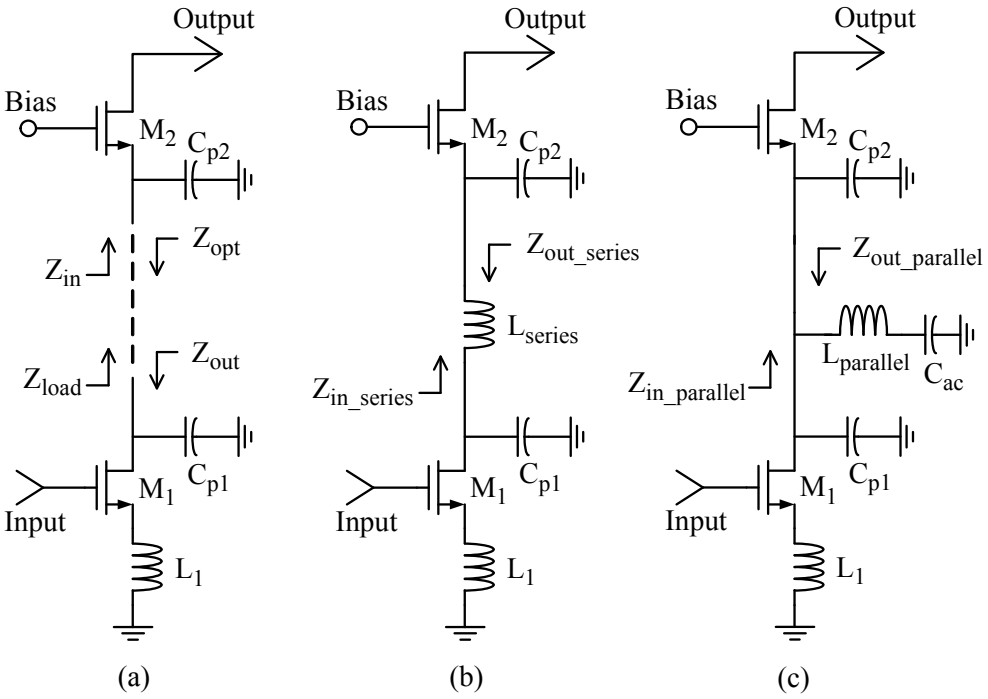

Figure 6.1 Cascode LNA (a), with (b) series or (c) parallel matching coils

On the other hand, the cascode LNA in Section 5.4 operates with the nominal supply voltage. Its schematic is shown in Figure 6.1(a), where the 1.0V supply is divided across 2 transistors by stacking the bottom (M_1) and cascode (M_2) transistors, with the added advantage of supply current sharing. The inferiority of the cascode LNA is quantified by comparing its power gain and noise figure to those calculated by the cascade-stage design equations described in Section 3.4.4. Table 6.1 summarizes the cascode LNA parameters of Section 5.4 together with those from amplifiers M_1 and M_2 individually. The power gain and minimum noise figure from the cascode are 37% and 38% poorer than the calculated decibel values, respectively.

Table 6.1 Comparison of single-stage cascode and cascade-stage LNAs at 24GHz and 3mA

	Power gain (dB)	NF_{min} (dBm)
Cascode	11.8	2.77
Common-source (M_1)	8.40	1.03
Common-gate (M_2)	7.82	1.13
Cascade-stage equations	16.2	1.73

The interface impedance matching within a cascode LNA can be visualized on a Smith chart, as shown in Figure 6.2. By considering the cascode as two independent amplifiers, and following the design guidelines outlined in Section 5.3.2, Z_{in} and Z_{out} should match Z_{load} (for operating power gain from M_1) and Z_{opt} (for noise figure of M_2), respectively. The circuit parameters in Figure 6.1 are identical to the cascode amplifier illustrated in Section 5.4, but the power budget is limited to 1.5mA from a 1.0V supply. Simulations at 24GHz predict that Z_{in} lies on the 1.2dB gain circle (out of 4.64dB MAG) and Z_{out} lies on the 6.8dB noise circle (out of 1.26dB NF_{min}). Therefore, gain and noise performance from a cascode LNA is worse than the cascade stages.

Different techniques aimed at eliminating the common-node parasitic capacitance [C_{p1} and C_{p2} shown in Figure 6.1(a)] have been used to improve the cascode LNA performance. In [6.2], a series inductor is inserted between M_1 and M_2 as illustrated in Figure 6.1(b), where L_{series} forms a lumped-element transmission line with C_{p1} and C_{p2}. Similarly, [6.3] uses a parallel inductor $L_{parallel}$ to resonate out this parasitic capacitance as shown in Figure 6.1(c). Both of these techniques can be interpreted as introducing an impedance transformation network between M_1 and M_2. The value of L_{series} and $L_{parallel}$ for this study are obtained by following the design procedures described in [6.2] and [6.3], and the transformed input and output impedances are plotted on the Smith chart shown in Figure 6.2. Series and parallel matching improve the common-source amplifier's power gain by 1.5dB and 2.0dB,

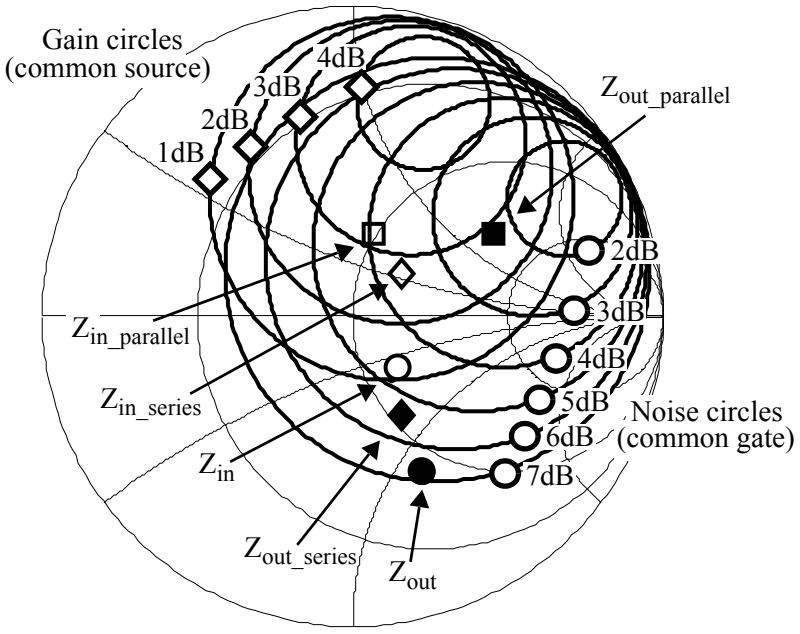

Figure 6.2 Visualization of interface impedance matching on a Smith chart

respectively, and the common-gate amplifier's noise figure by 1.4dB and 4.5dB, respectively. However, satisfying both the power gain (i.e., $Z_{load}= Z_{in}$) and noise matching conditions (i.e., $Z_{out}= Z_{opt}$) with a single impedance transformation network is impossible because Z_{in} and Z_{opt} of the common-gate stage are dependent on each other.

6.1.2 Current Feedback with a 3-Port Transformer

Applying current feedback to a common-gate amplifier modifies its transfer function. The input referred current noise becomes adjustable while the input referred voltage noise remains unchanged. This decouples the amplifier input impedance (Z_{in}) and optimum source impedance (Z_{opt}). Therefore, simultaneous gain and noise matching towards a common-source amplifier becomes possible.

A simplified schematic of the proposed current-feedback cascode LNA is illustrated in Figure 6.3. The RF input signal is applied to the gate of M_1, and the output is at the drain of M_2 via series inductor L_{drain}. This current sensing inductor is magnetically coupled (k) to L_{source} with the aim of modifying the input current of the common-gate transistor M_2. L_{drain} and L_{source} form a 3-port, because the two terminals of L_{drain} and one terminal of L_{source} lie in the AC signal path, while L_{source} has one terminal AC grounded via C_{ac}. For circuit optimization, one-half of the parasitic capacitance at the common node between M_1 and M_2 (i.e., C_{p1}) is assigned to the output capacitance of M_1, and the other half (i.e., C_{p2}) is assigned to the input capacitance of M_2. The common-source amplifier is optimized by the bilateral methodology outlined in Section 5.3.4. However, the common-gate amplifier relies on the feedback path to achieve simultaneous matching by optimizing the

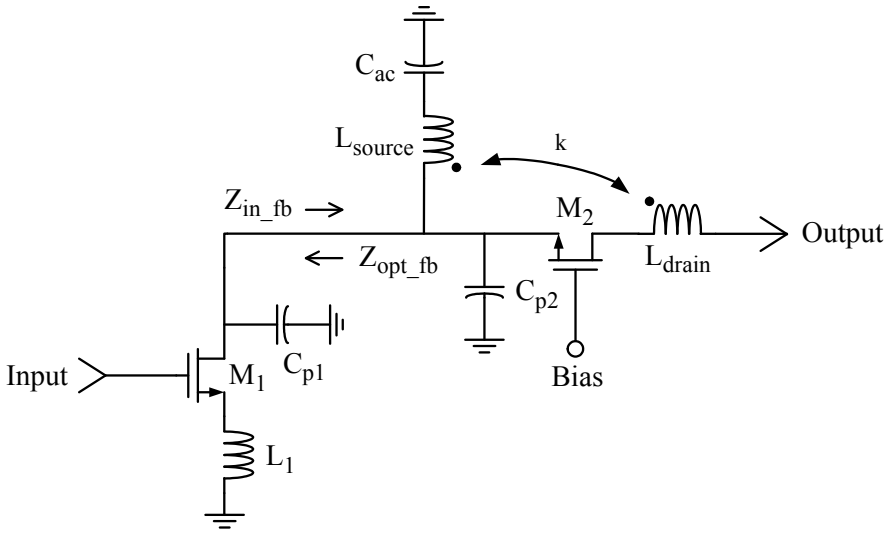

Figure 6.3 Current-feedback cascode LNA using transformer

values of Z_{in_fb} and Z_{opt_fb}.

Current feedback applied to the common-gate amplifier is analyzed from the small-signal equivalent circuit shown in Figure 6.4. For noise analysis, thermal noise on the drain current ($\overline{i_{D2}^2}$) and induced gate noise of M_2 ($\overline{i_{G2}^2}$) [6.4] are considered. Magnetic coupling between L_{drain} and L_{source} is modelled by current-controlled voltage sources with mutual inductance (M). Blocking capacitor C_{ac} is idealized by an AC short circuit in Figure 6.4. Parasitics of L_{drain} and L_{source}, and gate-drain capacitance of M_2 are ignored in order to simplified the analysis. M_2 is in the saturation region and therefore its output resistance is also neglected. At DC, $i_1 = 0$ and the current-feedback cascode resembles the simple cascode in Figure 6.1(a), because the feedback loop is an open circuit.

The amplifier output is solely in the current domain because it is in series with a current source. Therefore, only the transconductance and current gains are of interest. It is clear that the transconductance gain is equal to g_m. Summing the currents at the positive terminal of input source v_x, and observing that $v_{gs} = -v_x$ and $i_{out} = -i_2 = g_m \cdot v_{gs}$ gives

$$\text{current gain} = \frac{i_{out}}{i_x} = -\frac{s \cdot g_m L_{source}}{1 + s \cdot g_m (L_{source} - M) + s^2 \cdot L_{source} C_{gs}} = -\frac{s \cdot g_m L_{source}}{1 + \dfrac{2\zeta}{1/\sqrt{L_{source} C_{gs}}} \cdot s + \left(\dfrac{s}{1/\sqrt{L_{source} C_{gs}}}\right)^2}, \tag{6.1}$$

where $\zeta = (g_m/2) \cdot (1/\sqrt{C_{gs}}) \cdot (\sqrt{L_{source}} - k\sqrt{L_{drain}})$. The current gain of a com-

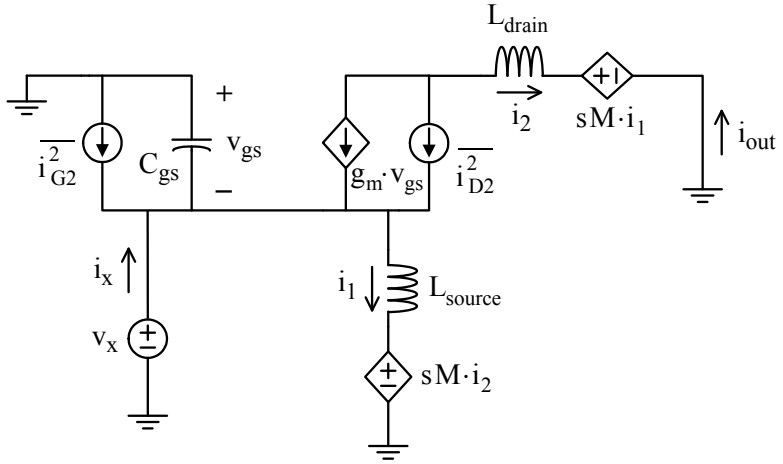

Figure 6.4 Small-signal equivalent circuit of the common-gate amplifier with feedback

mon-gate amplifier without feedback is $-1/(1+sC_{gs}/g_m)$, which shows a first-order roll off with frequency [6.5]. The proposed current feedback reshapes the transfer function gain into a second-order bandpass characteristic. The location of the complex poles in Eqt. (6.1) depends only on L_{source} and C_{gs}, and the damping factor (ζ) depends on L_{source} and L_{drain}.

The input impedance Z_{in_fb} is the ratio between v_x and i_x. Substituting $i_{out} = -g_m v_x$ into Eqt. (6.1) gives

$$Z_{in\_fb} = \frac{V_X}{I_X} = \frac{s \cdot L_{source}}{1 + s \cdot g_m (L_{source} - M) + s^2 \cdot L_{source} C_{gs}} . \tag{6.2}$$

For $s = j\omega$ (i.e., sinusoidal steady state) and re-arranging terms in Eqt. (6.2), the input admittance is

$$Y_{in\_fb} = \frac{1}{Z_{in\_fb}} = g_m \left(1 - k \sqrt{\frac{L_{drain}}{L_{source}}} \right) - j \frac{1 - \omega^2 L_{source} C_{gs}}{\omega L_{source}} . \tag{6.3}$$

For a given operating frequency and transistor dimensions defining C_{gs}, the input susceptance depends only on L_{source}, while the input conductance decreases with increasing L_{drain}/L_{source} ratio.

The optimum source admittance Y_{opt_fb} for minimum noise figure depends on the equivalent input voltage noise ($\overline{v^2_{x\_noise}}$) and current noise ($\overline{i^2_{x\_noise}}$) powers, and their correlation [6.4]. The drain current thermal noise in Figure 6.4 is transferred to the input by the amplifier's transconductance and current gain. On the other hand, the induced gate noise shunts the input directly. Therefore,

$$\overline{V^2_{x\_noise}} = \frac{1}{g_m^2} \cdot \overline{I^2_{D2}} \tag{6.4}$$

and

$$\overline{I^2_{x\_noise}} = \frac{\overline{I^2_{D2}}}{(\text{current gain})^2} + \overline{I^2_{G2}} . \tag{6.5}$$

Correlation between $\overline{i^2_{D2}}$ and $\overline{i^2_{G2}}$ is ignored in this analysis because its magnitude is less than 0.5 even for short-channel MOS transistor [6.6]. Therefore, the first term in Eqt. (6.5) is fully correlated to Eqt. (6.4), but the second term is assumed to be uncorrelated. From [6.7], the real part of Y_{opt_fb} is

$$\text{Real}\{Y_{opt\_fb}\} = \sqrt{\overline{I^2_{G2}} / \overline{V^2_{x\_noise}}} = g_m \cdot \sqrt{\overline{I^2_{G2}} / \overline{I^2_{D2}}} . \tag{6.6}$$

From [6.7] and Eqt. (6.1) with $s = j\omega$, the imaginary part of Y_{opt_fb} is

$$\text{Imag}\{Y_{opt\_fb}\} = -\text{Imag}\left\{ \frac{\overline{V^*_{x\_noise}} \cdot \overline{I_{x\_noise}}}{\overline{V^2_{x\_noise}}} \right\} = \frac{1 - \omega^2 L_{source} C_{gs}}{\omega L_{source}} . \tag{6.7}$$

The optimum source admittance has a conductance that is fixed by the transistor transconductance and ratio of noise powers [as expressed in Eqt. (6.6)]. On the other hand, susceptances Y_{opt_fb} and Y_{in_fb} are equal in magnitude, but oppositve in phase as $\text{Imag}\{Y_{opt\_fb}\} = -\text{Imag}\{Y_{in\_fb}\}$ [referring to Eqts. (6.3) and (6.7)].

The common-gate amplifier Z_{in} and Z_{opt} may be tuned by varying the transistor area, and the self and mutual inductance values of the transformer. Figure 6.5 plots the simulated input and optimum source admittances of the common-gate stage of the feedback cascode LNA shown in Figure 6.3. The amplifier parameters are identical to those specified for the LNA in Figure 6.1(a). The transformer coupling factor k is fixed at 0.6, and the self inductance has a Q of 15 at 24GHz. Parasitics C_{p1} and C_{p2} are set equal to 10fF, and C_{ac} of 30pF gives a –j0.22Ω impedance to ground in series with L_{source} at the operating frequency.

Although based on the simplified equivalent circuit model illustrated in Figure 6.4, Eqts. (6.3), (6.6), and (6.7) closely resemble the relationship between Y_{opt_fb} and Y_{in_fb} predicted from transistor-level simulations. As L_{source} and L_{drain} vary from 230pH to 430pH, and from 40pH to 640pH, respectively, Y_{opt_fb} remains on the same constant conductance circle at 4mS, with susceptances that are independent of L_{drain} but decrease from 19mS to 9mS with increasing L_{source}. Similarly, the

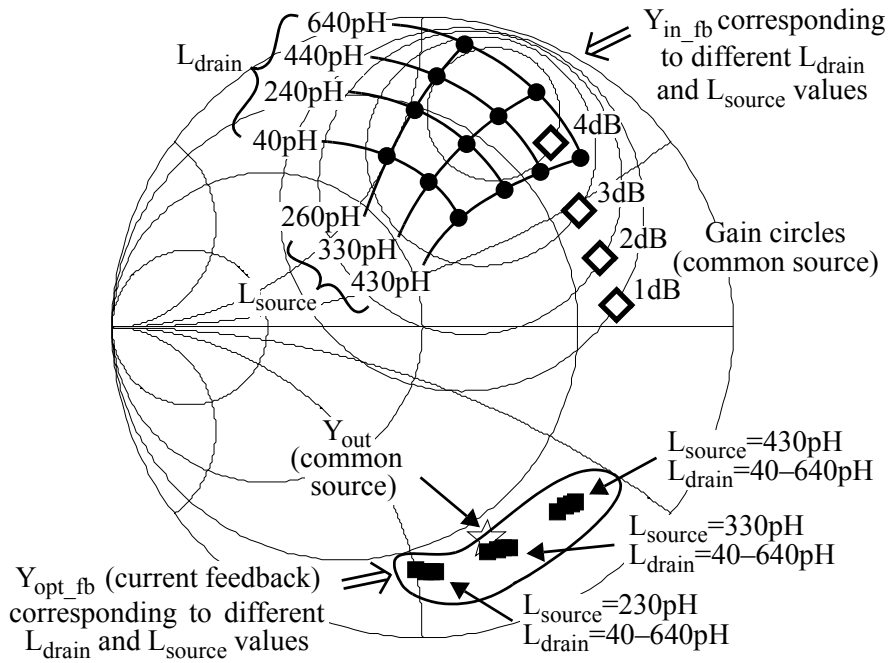

Figure 6.5 Input and optimum source admittances of a current-feedback, common-gate amplifier at 24GHz superimposed on the power gain circles and output admittance of a common-source amplifier

susceptance of Y_{in_fb} lies approximately on the same constant susceptances circle for each value of L_{source}. It has the same magnitude but opposite sign compared to the susceptance of the corresponding Y_{opt_fb}. It is also clear that the conductance of Y_{in_fb} decreases with the L_{drain}/L_{source} ratio.

The power gain circles and output admittance (Y_{out}, represented by the star-shaped symbol) of the common-source stage in Figure 6.1(a) are also shown in Figure 6.5. The design target is to match Y_{opt_fb} to Y_{out} for minimum cascade noise figure, and select Y_{in_fb} to maximize the operating power gain.

6.1.3 Simulated Performance Comparison

The simulated performance of the proposed current feedback LNA in a 90nm CMOS technology [6.8] is compared to the three cascode LNAs from Figure 6.1. Using the optimization algorithm outlined in Chapter 5, the common-source (M_1) and the common-gate (M_2) transistors have gate widths of $50\times 2\mu$ and $30\times 1\mu$, respectively. For a given current budget, a narrower M_2 favors the gain and noise performance with little degradation in the bandwidth (see Section 5.2). For a 1.0V supply and 1.5mA bias current, the drain-source voltage across M_1 is about 0.4V. An inductive Q of 15 at 24GHz and $C_{p1}=C_{p2}=10fF$ are assumed.

The degeneration inductance (L_1) is 240pH from the optimization study results of Section 5.4. Maximizing the cascode unity-gain current frequency [6.2] gives $L_{series}=265.5pH$ in Figure 6.1(b), and resonating the cascode common node at the operating frequency [6.3] requires $L_{parallel}=482.0pH$ in Figure 6.1(c). For the current-feedback LNA of Figure 6.3, the simulation results in Figure 6.5 immediately highlight optimum selections of $L_{drain}=450pH$ and $L_{source}=300pH$. Additionally, the current gain of the common-gate stage in Eqt. (6.1) is optimized by selecting the transistor size and inductance values appropriately.

Figure 6.6 compares the power gain and minimum noise figure of the LNAs from 22GHz to 26GHz. Current feedback enhances the power gain from the simple cascode LNA by 8.1dB across this frequency range. Series and parallel matching gives less improvement, at about 3.6dB and 0.7dB, respectively. The 8.1dB gain increment is partly contributed by the optimized power gain from the common-source stage (Y_{in_fb} positioned at the maximum power gain circle in Figure 6.5), and partly due to the re-shaping of the current gain transfer function in Eqt. (6.1).

Given the four LNAs have the same input and output impedances, their maximum available power gain increases in direct proportion (in dB) to the active gain [6.9], which is characterized by its forward transmission coefficient (see Section 1.2.2). Figure 6.7 shows the simulated $|S_{21}|$ for the simple and current-feedback cascode LNAs. Current feedback increases $|S_{21}|$ by 6.2dB at 24GHz, and the power

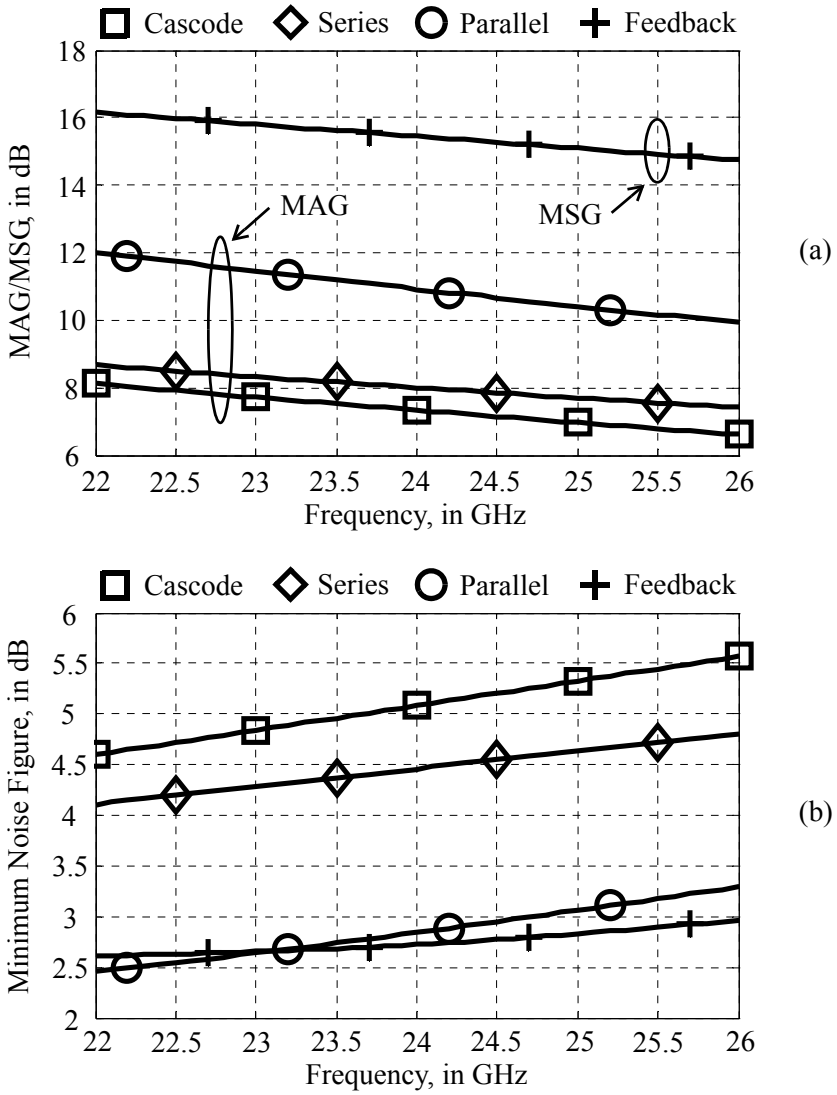

Figure 6.6 Simulated power gain and minimum noise figure versus frequency of cascode LNA, with series or parallel matching coils, and with current feedback

gain in Figure 6.6(a). While $|S_{21}|$ from the simple cascode gives a constant negative slope at –0.26dB/GHz, it increases at rates of 0.69dB/GHz and 0.42dB/GHz at 22GHz and 26GHz, respectively, for the current-feedback cascode.

Current feedback increases the active gain of the common-gate amplifier shown in Figure 6.3. Solving for the amplifier's ABCD parameters [6.10] gives

$$A = 0, \quad B = -\frac{1}{\text{transconductance gain}}, \quad C = 0, \quad \text{and} \quad D = -\frac{1}{\text{current gain}}. \tag{6.8}$$

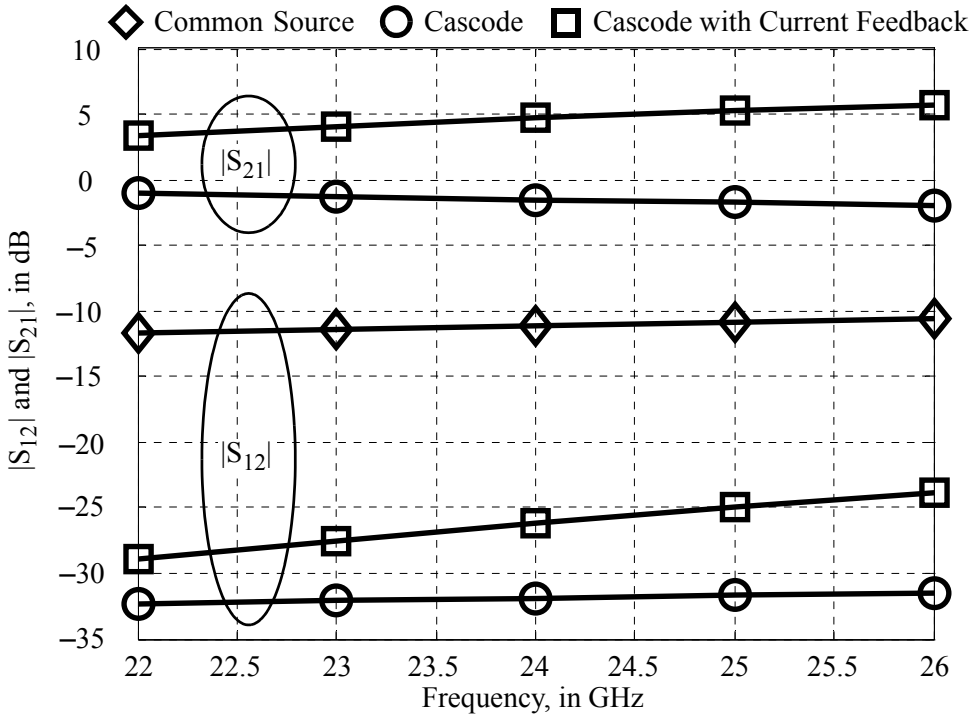

Figure 6.7 Simulated $|S_{12}|$ and $|S_{21}|$ versus frequency

Substituting Eqt. (6.1) into Eqt. (6.8), and subsequently converting the ABCD to S-parameters [6.11] gives

$$|S_{21}| = \left| \frac{s \cdot 2 g_m L_{source}}{1 + s \cdot [L_{source}/Z_o + g_m (L_{source} - M)] + s^2 \cdot L_{source} C_{gs}} \right|. \qquad (6.9)$$

Similar to the current gain in Eqt. (6.1), the $|S_{21}|$ is shaped by the same second-order transfer function except with a different damping factor. Therefore, the active gain of the current-feedback cascode is expected to follow the bandpass response specified by Eqt. (6.9).

The inductor in either the series or parallel matched cascode LNA also resonates with the transistor's gate-source capacitance (C_{gs}) to improve the transistor's current gain and active gain. Simulations predict that $|S_{21}|$ are improved by 1.26dB and 1.28dB for the series and parallel matched cascodes, respectively.

Matching of the optimum source impedance for the succeeding stage to the output impedance of the preceding stage lowers the cascade noise figure. This is evident in Figure 6.6(b), where the current-feedback cascode gives the lowest NF_{min} of 2.72dB at 24GHz. It coincides with the matched impedance values displayed on the Smith chart in Figure 6.5. The parallel-matched cascode gives the second lowest NF_{min} of 2.84dB, because $Z_{out\_parallel}$ lies on the 2.4dB noise circle

shown in Figure 6.2, but not at the optimum Z_{opt} of 1.26dB. Series matching only improves the NF_{min} of the simple cascode by 0.64dB (from 5.10dB to 4.46dB).

Applying current feedback to the common-gate transistor in Figure 6.3 creates a reverse signal path from the drain to the source via the mutual inductance. The impedance at the cascode's common node is also increased by inductance L_{source}. This exacerbates the reverse signal flow via the gate-drain capacitance of the common-source transistor. These issues are quantified by the reverse transmission coefficients ($|S_{12}|$) shown in Figure 6.7. For the cascode amplifier, current feedback degrades $|S_{12}|$ by 3.3dB and 7.7dB at 22GHz and 26GHz, respectively. Simulation predicts a worst-case $|S_{12}|$ of –18.4dB at 72GHz. Nevertheless, reverse isolation of the current-feedback cascode (two-stage amplifier) still outperforms the single-stage common-source amplifier. Their differences in $|S_{12}|$ are 17.3dB and 13.2dB at 22GHz and 26GHz, respectively, with a minimum spread of 12.6dB at 72GHz.

The sensitivity of the amplifier power gain and noise figure to the bias current is shown in Figure 6.8. It also foresees the feasibility of trading off battery life for RF performance of the LNA. For the four LNAs optimized at 1.5mA, simulations predict that both power gain and noise figure improve with increasing bias current until 4.2mA, where the gate-source voltage of the common-gate transistor is 737mV. This leaves 263mV across the drain-source terminals of the common-source transistor. The above observations comply with the voltage scaling simulation data given in Figure 5.11, where degradation of MSG is noticeable for the NMOS transistor at a drain current density of 4.2×10^{-2}mA/μm and V_{DS} of 0.3V.

The amplifier parameters plotted on the Smith chart of Figure 6.9 permits visualization of the amplifier optimization. The stability circles drawn on Figure 6.9 reveal that the current-feedback cascode LNA is conditionally stable. The source impedance selection involves trade-offs between noise figure (matching to Z_{opt}), input return loss (matching to the conjugate of S_{11}), stability (distance from the source stability circle), and input bandwidth (matching between LNA input and source impedances, which vary with frequency). Similar considerations apply to the load impedance on gain (lies on a specific gain circle), load stability (distance to load stability circle), and output bandwidth (load impedance across frequency). Resistive losses from input and output matching networks have to be included when quantifying the LNA wideband stability, which is covered in the next section about LNA implementation.

Transforming S_{11} to 50Ω with an L-type matching network [6.12] requires an inductance of 470pH. Assuming a Q of 15 at 24GHz for this coil, the corresponding series equivalent resistance is 4.72Ω. The noise produced by this resistance increases the amplifier's simulated minimum noise figure from 2.72dB to 3.62dB, and it should be included in the characterization shown in Figure 6.9. On the other

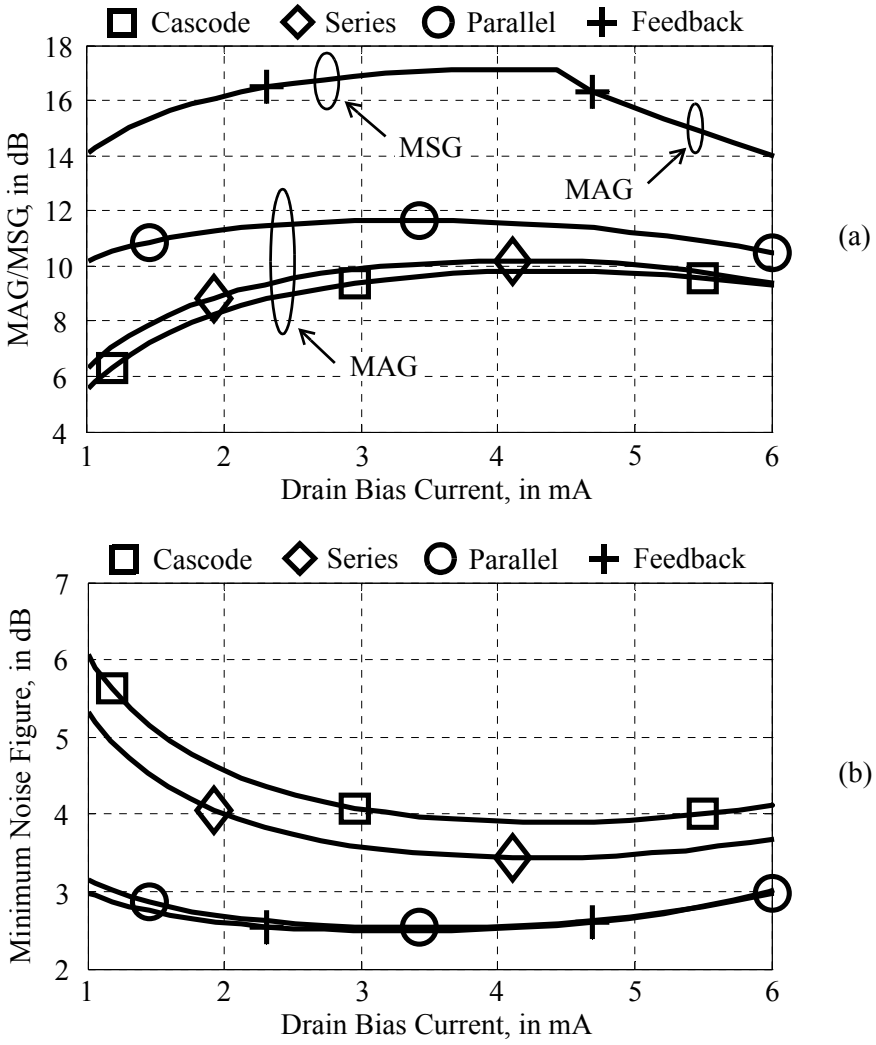

Figure 6.8 Simulated power gain and minimum noise figure versus bias current of the cascode LNA, with series or parallel matching coils, and with current feedback

hand, this loss together with the loss from the output loading stabilize the amplifier. For example, increasing the series resistance to 7Ω makes the amplifier unconditionally stable between 1GHz and 100GHz.

Parameters S_{22} and Z_{opt} are widely separated in Figure 6.9, and therefore matching S_{22} to the succeeding stage's Z_{opt} seems difficult (with assumption that the succeeding stage is a common-source amplifier). For example, S_{22} of the simple cascode and current-feedback cascode LNAs are $0.922\angle{-15.7°}$ and $0.915\angle{-22.7°}$, respectively, while the Z_{opt} in Figure 6.9 is $0.686\angle{85.4°}$. However, it is not necessary to match the input of the succeeding stage to 50Ω, and simulations predict that

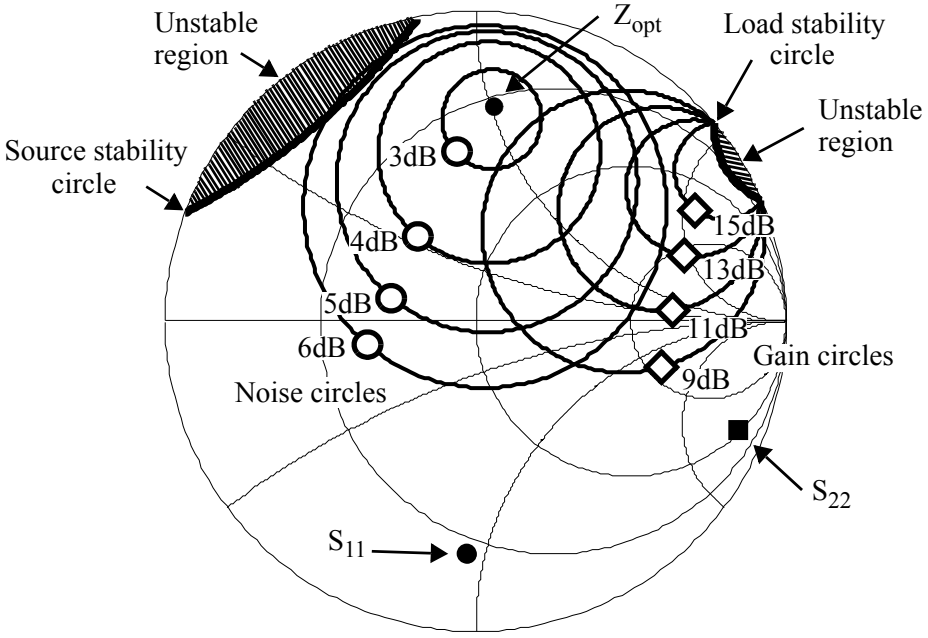

Figure 6.9 Characteristics of the current-feedback cascode LNA at 24GHz illustrated on a Smith chart

Z_{opt} may be adjusted by varying degeneration inductance L_1 in Figure 6.1. Moreover, the noise from the succeeding stage has less effect overall given the 15.4dB power gain from the cascode LNA. For example, the 3.62dB LNA noise figure only degrades to 4.0dB and 5.0dB for succeeding stage noise figures of 8.50dB and 14.6dB, respectively. Therefore mismatch between S_{22} and Z_{opt} of the succeeding stage is tolerable.

6.1.4 LNA Design and Implementation

The LNA is required to deliver 15dB power gain, 5dB noise figure, and –10dBm IIP_3 from a 3mW power budget, as summarized in Table 5.1. Although simulations in Figure 6.8 reveal that the current-feedback cascode topology provides 16.9dB MSG at 3mW, the available power gain is lower because of power losses along the signal path.

Figure 6.10 shows the simplified schematic of the proposed LNA. The first stage consists of transistors M_1–M_2, degeneration inductor L_{1s}, and current feedback transformer L_{2p}–L_{2s}, together with decoupling capacitor C_{ac1}. Potential sources of loss include: the input transmission line with characteristic impedance Z_o, and finite Q factor from input and output matching networks with L_{1p} and L_{3p}. Assuming an inductor Q of 15 at 24GHz and 1.5mA bias current, the first stage is designed for 15.4dB of power gain (see Figure 6.6), which drops to 9.79dB with the

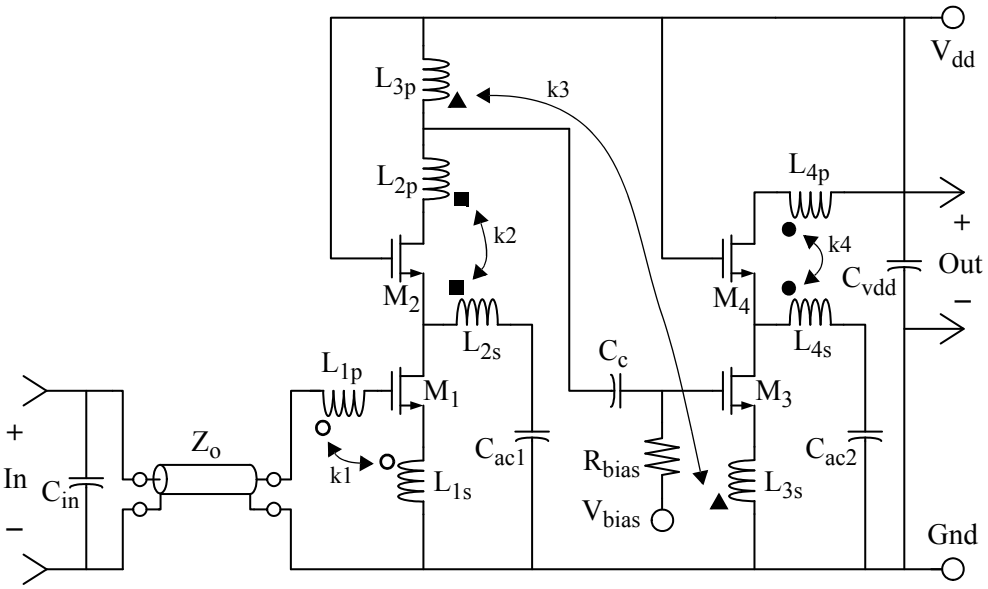

Figure 6.10 Simplified schematic of a 2-stage, current-feedback cascode LNA

estimated input and output resistive losses. The minimum noise figure also increases from 2.73dB to 3.63dB. The power gain is expected to drop by another 1.5dB after accounting for RC parasitics from transistors M_1–M_2, and dissipation of the input transmission line. The cascode LNA shown in Figure 6.1(a) experiences a (similar) power gain degradation from 7.33dB to 2.17dB when the matching losses are applied.

An increase in the bias current to 3mA only boosts the power gain by 1.6dB (see Figure 6.8). Therefore, one-half of the current budget is allocated to the second stage, which consists of M_3–M_4, L_{3s}, L_{4p}–L_{4s}, and C_{ac2} in Figure 6.10. M_4 is identical to M_2, but the gate width of M_3 is about two-thirds that of M_1. A narrower gate width is desirable because of the higher drain current density, which results in higher power gain and lower minimum noise figure (see Section 5.2). The higher gate impedance from M_3 is acceptable because the second stage input is not matched to 50Ω. For this single-ended implementation, the two stages are AC coupled by a 1.3pF MIM capacitor (C_c) which provides DC blocking. Its low Q of 0.85 at 24GHz [6.1] introduces a 6.2Ω equivalent series resistance which, combined with R_{bias}, degrades the second stage power gain from 17.3dB to 13.7dB. It also increases the minimum noise figure from 2.06dB to 4.28dB. Note that the power loss from the output matching network is not taken into account because it belongs to the mixer input stage implementation. There is an additional 1.0dB drop in the second stage gain due to the transistors' RC parasitics.

Counting transformers L_{2p}–L_{2s} and L_{4p}–L_{4s} as two coils and including the output loading, the schematic shown in Figure 6.10 employs seven separate coils.

Physical implementation of this circuit not only consumes significant silicon area, but also imposes difficulties in minimizing parasitic coupling between coils and accessing the input and output connections to the circuit. Therefore, inductors L_{1p} and L_{1s}, and L_{3p} and L_{3s} are grouped together as two independent transformers, and their magnetic couplings are embedded in the optimization. This reduces the total number of coils from seven to five. Input signal is fed towards the LNA from a ground-signal-ground RF pad (300μm width) via a microstrip-type transmission line with line width tapered from 25μm to 7μm. This transmission line also deliberately separates the input current return path (In–) from the local ground plane (Gnd). This transmission line and capacitance from the RF pad (C_{in}) are embedded as part of the 50Ω input matching network. Capacitor C_{vdd} (26.6pF) decouples the local supply current return path via a 0.25Ω impedance at 24GHz.

Figure 6.11 shows the floorplan of the LNA layout. The supply voltage and ground reference are centralized among the magnetic coils, which are orthogonally positioned. Transformer L_{3p}–L_{3s} lies at 135° to the horizontal, between L_{2p}–L_{2s} and L_{4p}–L_{4s}. The transmission line is adjacent to L_{1p}–L_{1s} in the lower-left corner. All components within the LNA (including the transformers) have their return currents decoupled by capacitor C_{vdd}. Therefore, the parasitic inductances from external supply wires have less influence on the LNA operation. At 24GHz, simulations predict that a pair of 1μH inductors in series with the V_{dd} and ground wires change the LNA power gain by only 0.11dB, NF_{min} by 0.021dB, and $|S_{11}|$ by 0.21dB. The ver-

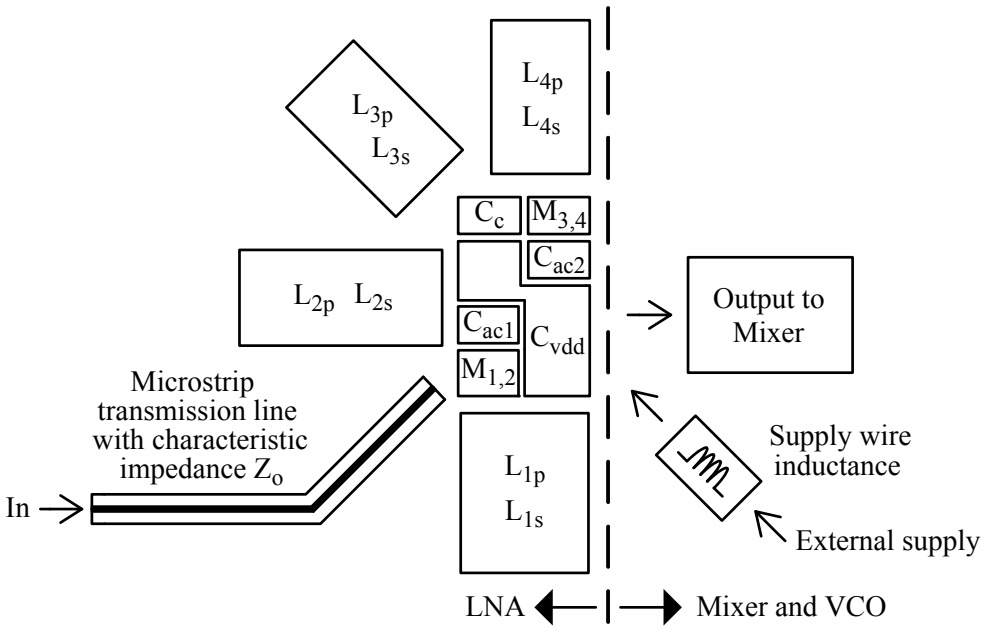

Figure 6.11 Floorplan of the magnetic coils, input transmission line, and decoupling capacitors in the LNA layout

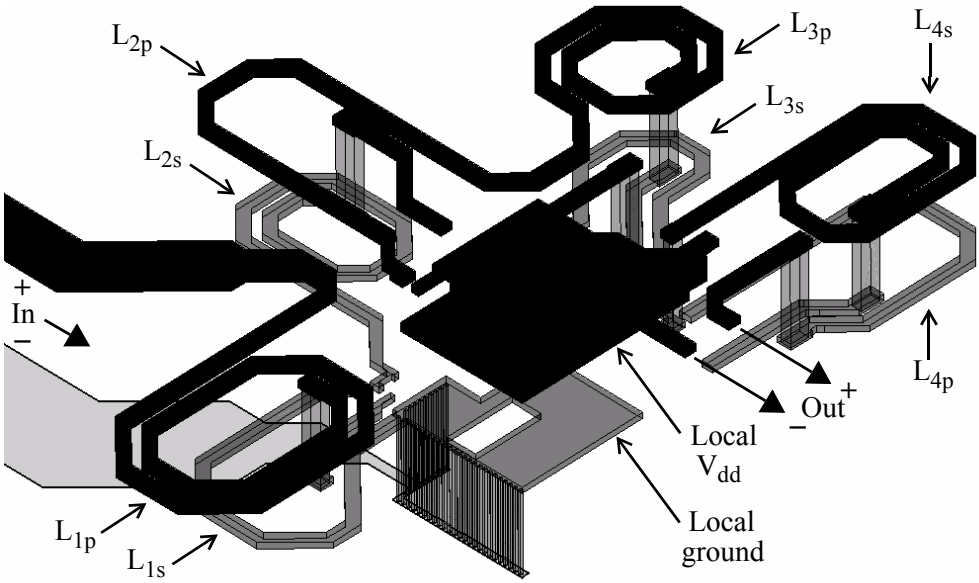

Figure 6.12 Three-dimensional visualization of the implementation of the magnetic devices for the LNA

tical dashed line in Figure 6.11 highlights the boundary between the LNA and other parts of the receiver chain illustrated in Figure 3.8 (RF mixer, VCO, IF amplifier, etc.).

Figure 6.12 shows an isometric view of the LNA's magnetic components. The two top-most metal layers (4μm and 3μm thickness) implement all of the coils, local supply and ground plane. Only the transmission line's return path lies on a lower metal, which is 0.5μm thick.

Electromagnetic simulation is used to determine a single S-parameter based model of the multi-port structure shown in Figure 6.12. This modelling approach incorporates both the parasitic coupling among adjacent magnetic components (e.g., between L_{2s}–L_{2p} and L_{3p}–L_{3s}) and the local supply and ground plane inductance (about 70pH/100μm) into the transistor-level circuit simulations. The transistors, resistors, and capacitors are represented by lumped-element model equivalents with their post-layout extracted RC parasitic elements. The same methodology is applied to the simulations of the RF mixer and VCO.

The LNA power transfer characteristics from simulations are shown in Figure 6.13 and Figure 6.14. For 3mW power dissipation, the power gain (MAG) and forward transmission coefficient ($|S_{21}|$) at 24GHz are 17.5dB and 9.70dB, respectively. The mismatch gain from the LNA output is accountable for the 7.8dB gain difference. Similar to the first stage, resistive loss lowers this gain by another 2.8dB. The gain roll-off is contributed by the resonant load formed by inductor L_{3p} and the second stage input impedance.

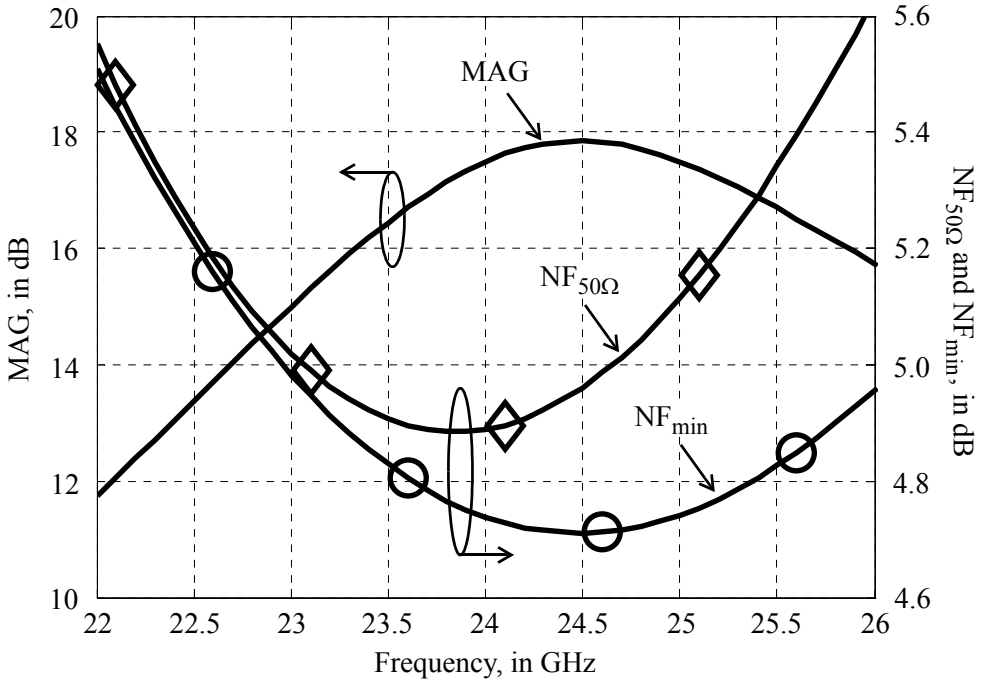

Figure 6.13 Simulated LNA power gain, noise figure, and minimum noise figure versus frequency

The noise figure of 4.89dB is higher than NF_{min} by 0.15dB at 24GHz. The gap between $NF_{50\Omega}$ and NF_{min} becomes larger with increasing frequency because the LNA optimum source impedance shifts away from 50Ω. On the other hand, the input reflection coefficient ($|S_{11}|$) remains well below –10dB across 22GHz to 26GHz. The simulated reverse isolation ($|S_{12}|$) is about twice to that of the single stage shown in Figure 6.7.

There are two necessary and sufficient criteria [6.9] to verify the broadband unconditional stability of the LNA. They are

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/(2|S_{12}S_{21}|) > 1 \tag{6.10}$$

and

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 . \tag{6.11}$$

On the other hand, the load and source stability circles introduced in Chapter 2 reveal the sensitivity of an amplifier's stability to source and load impedance values at a certain frequency. The input and inter-stage matching losses stabilize the LNA, and therefore Figure 6.15 shows that the LNA is unconditionally stable between 15GHz and 28GHz, and with a minimum *K* of 3.39 at 24GHz.

Applying two –50dBm tones at 23.9GHz and 24.1GHz to the LNA input generates third-order intermodulation tones which are 90.5dB lower than the fundamental components. Therefore, the simulated IIP_3 is –4.73dBm.

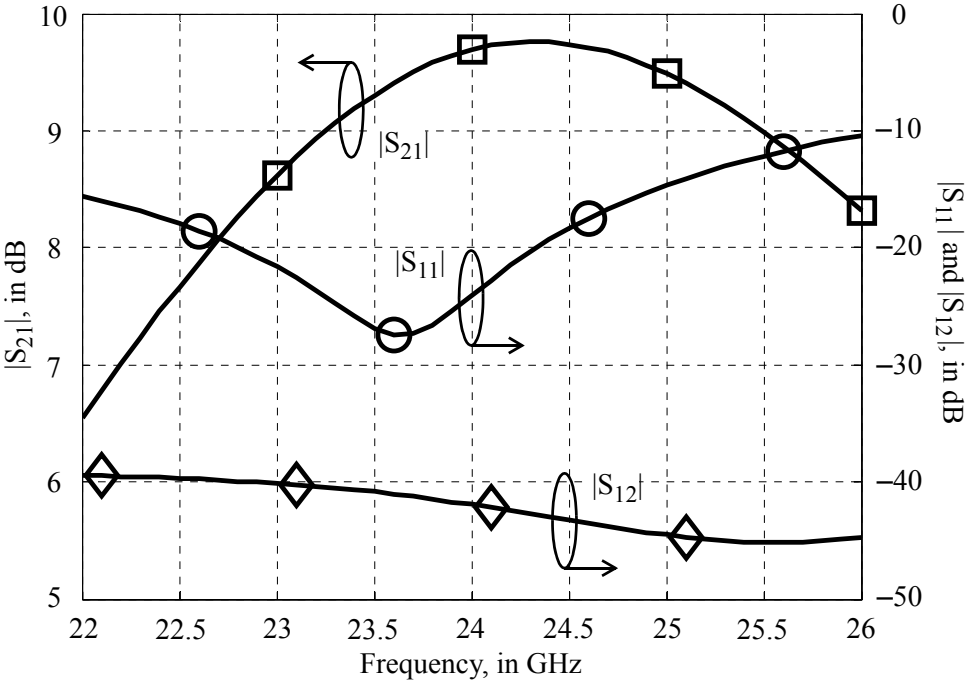

Figure 6.14 Simulated LNA S-parameters

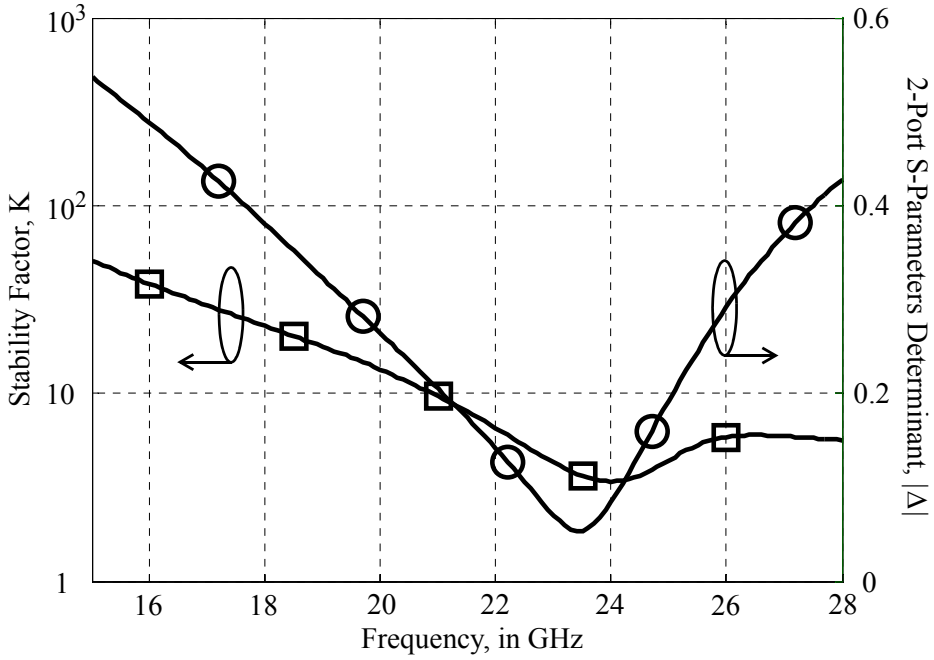

Figure 6.15 Simulated LNA stability factors versus frequency showing unconditional stability (i.e., K>1 and $|\Delta|<1$)

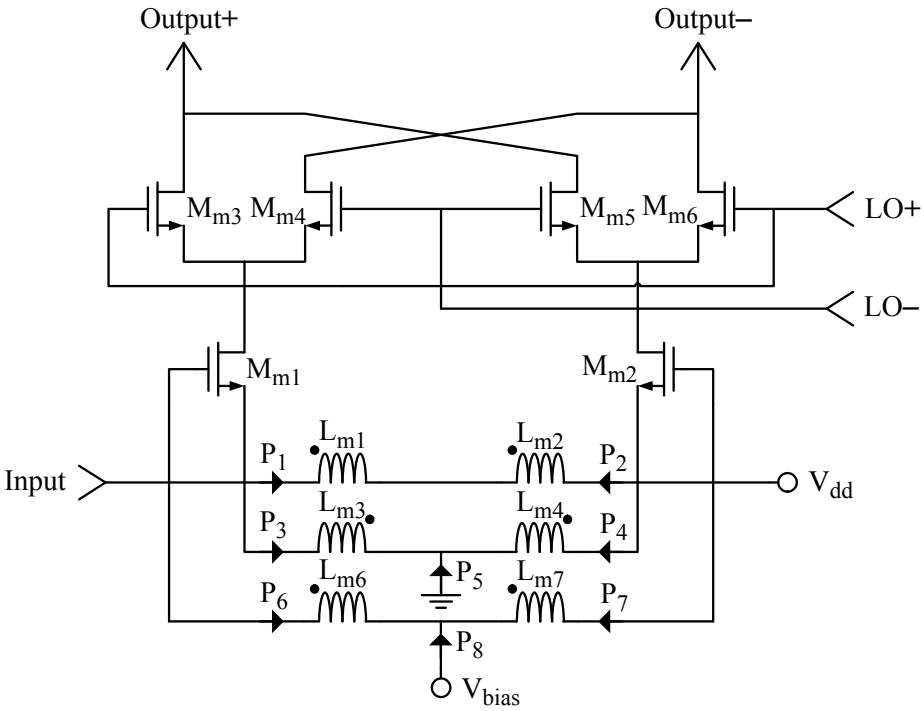

Figure 6.16 Simplified schematic of the frequency mixer

6.2 Frequency Downconverter

The frequency downconverter integrates three RF building blocks of the FMCW SRR receiver, as shown in Figure 3.8. The amplified echoes from the LNA are downconverted to an IF band centered around 4.8GHz by a mixer whose LO-port is driven by the wideband VCO presented in Chapter 4. This section describes the realization of the mixer.

6.2.1 Mixer Design and Implementation

The mixer is expected to deliver 0dB power gain, 20dB noise figure, and –3dBm IIP_3 at 2mW power dissipation from a 1.0V supply. The RF and IF bandwidth range from 22.5GHz to 25.5GHz, and 4.4GHz to 5.2GHz, respectively. These design targets have been derived in Chapter 3, and are summarized again in Table 6.2. Figure 6.16 shows the simplified schematic of the proposed Gilbert-type mixer where M_{m1} and M_{m2} are the transconductance stage, and M_{m3}–M_{m6} realize the cross-coupled switching quad.

Table 6.2 Mixer electrical specifications

Gain (dB)	NF (dB)	IIP_3 (dBm)	P_{DC} (mW)
0	20	–3	2

The relaxed mixer specifications due to the short-range functional requirement from the radar receiver permit aggressive reduction of the power consumption. Therefore, the VCO output is directly applied to gates of the switching quad without any buffering. The lack of a sharp signal transition from this sinusoidal LO waveform (about $0.5V_{pk}$ differential) degrades mixer gain and noise figure because imperfect switching from M_{m3}–M_{m6} attenuates the signal current at the IF output [6.13]. Simultaneous conduction among M_{m3}–M_{m6} also introduces additional thermal noise from these transistors, together with noise amplification from the LO path. The non-buffered mixer connection to the LO-port also presents capacitive loading towards the VCO resonant tank. This imposes an upper limit on selection of the gate width for M_{m3}–M_{m6}. Nevertheless, the proposed mixer adequately satisfies the design targets shown in Table 6.2.

An 8-port transformer excites the mixer input transconductors differentially from the single-ended LNA output. Transformer feedback between gate and source terminals of transistors M_{m1} and M_{m2} by inductors L_{m3}–L_{m4} and L_{m5}–L_{m6} is similar to the one employed in [6.14], with the exception that the input signal is now magnetically coupled to the mixer via L_{m1}–L_{m2}. The transistor's gate and source bias voltages are applied via center-taps at ports P_8 and P_5, respectively. Parasitic inductance and resistance in these ports appears as a common-mode impedance that does not alter the signal quality. It is important that signal current via port P_2 returns to the LNA's local ground plane (terminal Out– in Figure 6.12) to preserve signal

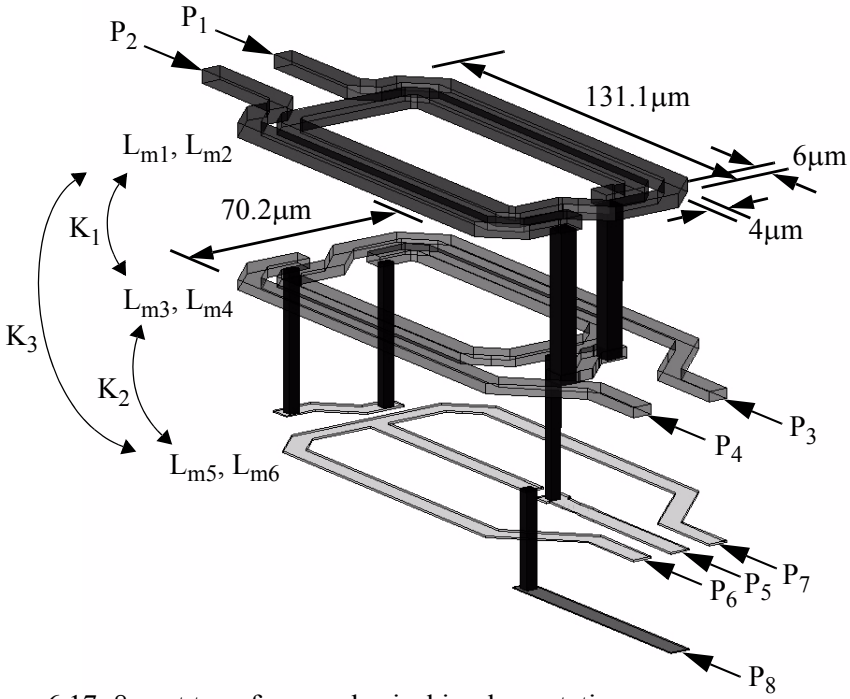

Figure 6.17 8-port transformer physical implementation

integrity. The transformer parameters are selected to optimize the signal transfer from the LNA to the transconductance stage, and provide the impedance seen by the LNA output terminal required to maximize the LNA power gain.

Figure 6.17 shows the implementation of the 8-port transformer. An overlay structure is chosen to minimize the occupied chip area, and to maximize the magnetic coupling factor. The transformer dimension is $70\mu m \times 113\mu m$. EM simulations predict that the differential inductances of L_{m1}–L_{m2}, L_{m3}–L_{m4}, and L_{m5}–L_{m6} are 530pH, 506pH, and 221pH, respectively. Coils lying on adjacent metal layers show stronger magnetic coupling ($K_1 = 0.68$ and $K_2 = 0.60$) than those on an alternate metal layer ($K_3 = 0.43$). The quality factors for the coils range from 8.8 to 12.4 at 24GHz. An independent testchip (without the LNA) adapts the transformer sizing in order to achieve 50Ω matching at the mixer input port.

6.2.2 Simulation Results

The transformer is quantified by parameters such as the signal attenuation between input and output, and amplitude and phase mismatches at the differential output. With reference to the notation given in Figure 6.16, the input signal is

$$\text{input signal} = V_{P1} - V_{P2}, \tag{6.12}$$

and the output signal is

$$\text{output signal} = (V_{P6} - V_{P3}) - (V_{P7} - V_{P4}). \tag{6.13}$$

Figure 6.18 shows that the attenuation increases with frequency, and it is –1.08dB and –1.30dB at 22GHz and 26GHz, respectively. Mismatch between ($V_{P6} - V_{P3}$)

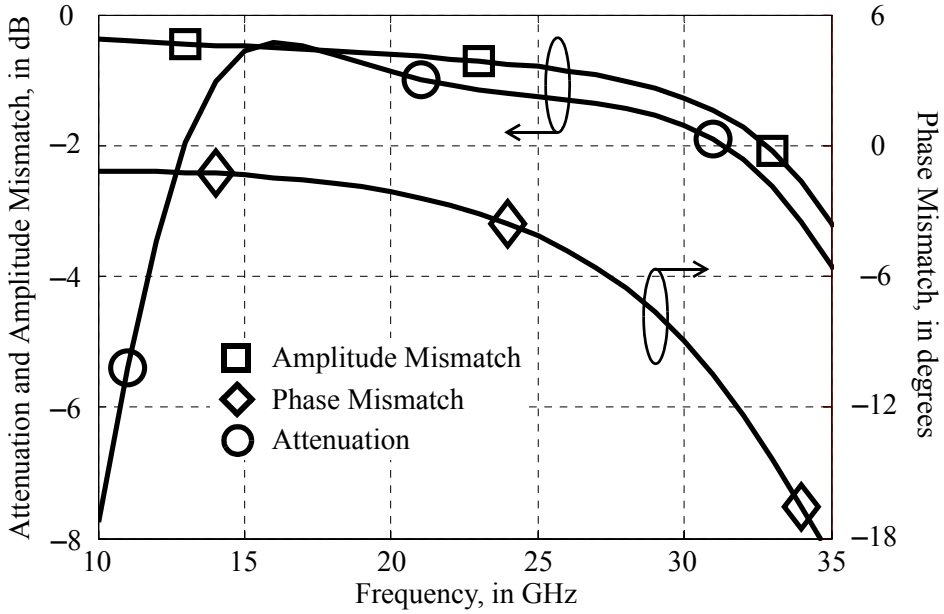

Figure 6.18 Simulated attenuation, amplitude and phase mismatches of the integrated balun of Figure 6.17 versus RF

and ($V_{P7} - V_{P4}$) increases the downconverted noise and interference around even harmonics of the LO to the differential output, and subsequently degrades the received signal quality. The mixer LO-to-RF isolation and even-order intermodulation distortion also deteriorate because of this mismatch. Below 26GHz, the simulated amplitude and phase mismatches are less than 0.86dB and 4.80°, respectively.

The mixer is characterized with a 100Ω load (differential) because its open drain output terminals (Output+ and Output–) are connected to the 50Ω characteristic impedance from the measurement setup. On the other hand, the mixer is loaded by a tuned circuit (which acts as a bandpass filter) within the radar receiver as illustrated in Figure 3.8. Therefore, the mixer is simulated against two different setups: a pair of 50Ω loads, and a pair of tuned loads. The measurement data with a 100Ω load is then adjusted by the difference of these two sets of simulations in order to estimate the measured mixer performance with a tuned load.

Mixer gain is usually expressed in the voltage domain because impedance matching is not required at IF. The measured power gain can be converted to voltage gain by

$$\text{power gain (dB)} = \text{voltage gain (dB)} - 10\log\frac{Re(Z_{out})}{Re(Z_{in})}, \qquad (6.14)$$

where Z_{out} and Z_{in} are the output and input impedances, respectively, and *Re(Z)* is the real part of *Z*.

Fixing the LO at 19.2GHz while sweeping the RF from 22GHz to 24GHz, the simulated mixer voltage and power gains with the two types of load are plotted against the input frequency in Figure 6.19. A RLC parallel resonant tuned load centered at 4.8GHz with a Q of 7.80 is assumed. Its 9.53dB voltage gain peaks at 24GHz and the gain variation across the 800MHz IF bandwidth is 1.98dB. On the other hand, power gain at 24GHz is 10.8dB lower but has a flatter response against RF, because of the difference in impedance levels between input and output. The power gain variation across the same IF bandwidth is 0.59dB.

With a 50Ω load, the mixer voltage gain is –9.78dB at 24GHz. This gain decreases with increasing frequency because of the RC roll-off from mixer's output pole. The power gain is 1.90dB lower because the Z_{out} in Eqt. (6.14) is 100Ω in parallel with the mixer output, while its Z_{in} is matched to 50Ω for this mixer. The 10.4dB power gain difference between the 50Ω and RLC loads (ΔA_p) at 24GHz indicates that the mixer power gain can be optimized by a proper selection of the load impedance.

Given the same setup used to simulate the mixer gain, Figure 6.20 shows the mixer noise figure (referred to 50Ω) simulated across the input frequency range. For a Gilbert-type mixer, flicker noise from transistors in switching quad M_{m3}–M_{m6} is sampled at twice the LO frequency with a gain that is inversely proportional to the slope of the LO waveform during switching [6.15]. This low-frequency noise

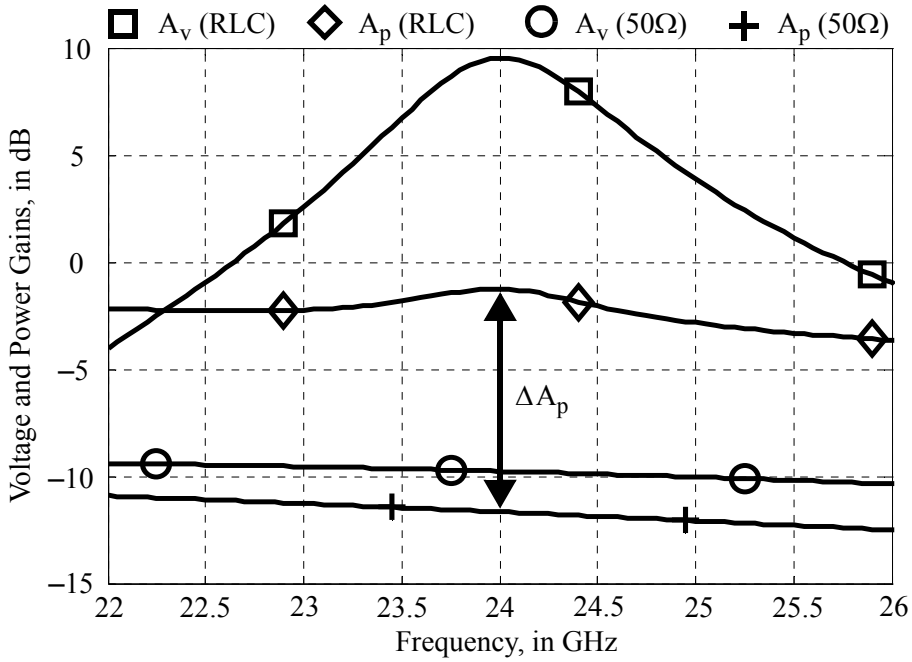

Figure 6.19 Simulated mixer voltage and power gains versus RF

appears at the mixer output without frequency translation. The application of a tuned load at IF filters out this noise and reduces the noise figure. On the other hand, applying 50Ω at the mixer output integrates low-frequency noise with a first-order lowpass transfer function and harms the output signal-to-noise ratio. Therefore, the simulated noise figure from a tuned load is about 3.9dB lower than that from a 50Ω load across 22GHz to 26GHz.

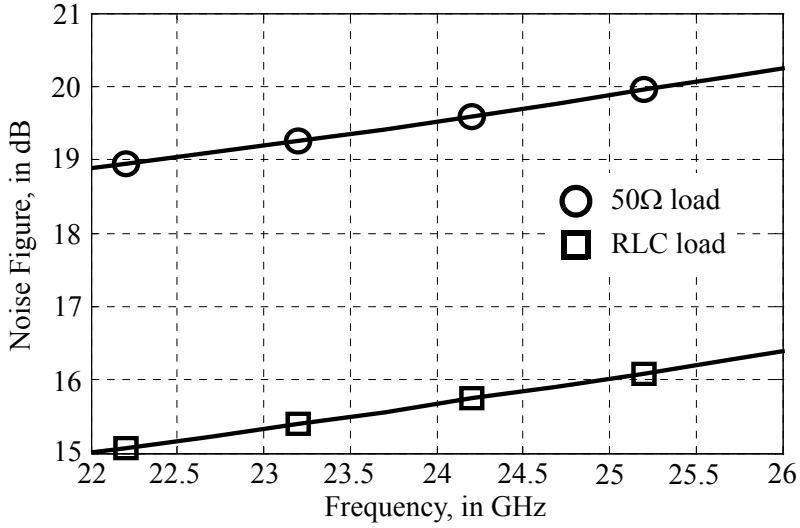

Figure 6.20 Simulated mixer noise figure versus RF

Applying two 23.9GHz and 24.1GHz sinusoids at the mixer input and measuring their third-order intermodulation products reveals that the input IIP_3 are 0.053dBm and 0.45dBm for the mixer having RLC and 50Ω loads, respectively.

6.3 Experimental Results

Three test circuits are implemented in IBM's 90nm RF-CMOS technology. The micrograph of frequency downconverter testchip is shown in Figure 6.21. It integrates the LNA, mixer and VCO. The core circuit occupies an area of $0.51 \times 0.95 \text{mm}^2$, which includes six transformers, supply and bias MIM decoupling capacitors, LNA input transmission line, and RF probe pads. The upper part of the die, which occupies the IF transmission lines and probe pads in the testchip, is allocated for the mixer LC resonant tank. Similarly, the area occupied by the decoupling capacitors at the bottom is reserved for the VCO divider and PLL circuitry shown in Figure 3.8.

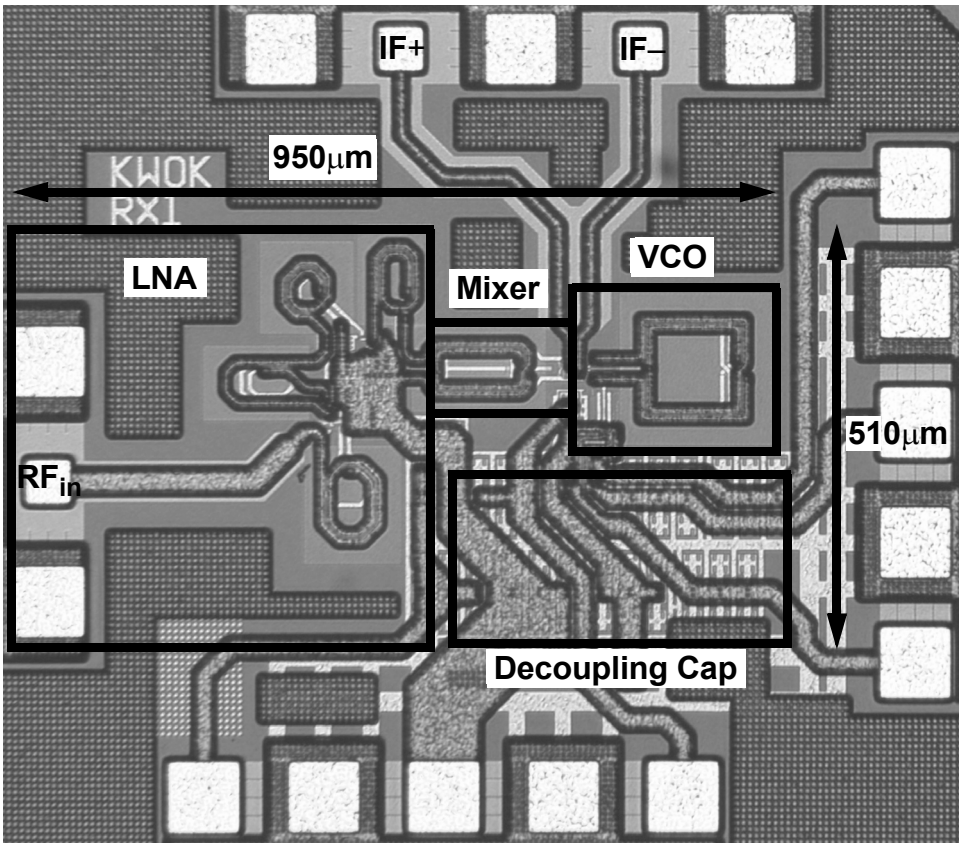

Figure 6.21 Micrograph of frequency downconverter testchip with LNA, mixer and VCO

The second test circuit is intended for mixer and VCO characterization. It is similar to the first testchip but with the LNA removed. The IF transmission lines and probe pads are shared among the mixer and VCO buffer output, and the mixer's 8-port input transformer is designed for a 50Ω input impedance. The third test circuit is dedicated for noise figure measurement. It is identical to the first testchip, but the VCO is removed and substituted by a connection to an external LO source. This ensures that the measured noise figure is not contaminated by the VCO phase noise and time drifting of the carrier frequency.

Figure 6.22 shows the measurement setup for power gain characterization. The RF input signal is brought to the IF band by the frequency downconverter. DC bias current for individual building blocks and the VCO center frequency are independently governed by adjusting the DC power sources. Signal at IF is measured single-ended with 50Ω terminations, and power gain is calculated by the input and output signal strength difference. Power losses along the RF and IF signal paths (outside the IC) are independently measured and compensated for each data point. Their average values are about 6dB and 3dB, respectively, in the corresponding frequency ranges of interest. The optional LO path applies to the noise figure measurement. A differential LO signal is derived by a power splitter and a pair of variable phase shifters. Single-point calibration is carried out on the two phase shift values by targeting minimum LO-to-IF leakage at 18.5GHz as measured on the spectrum analyzer. This algorithm is based on the fact that LO feedthrough grows exponentially with LO phase and amplitude mismatches [6.16], and that the (measured) insertion loss of the phase shifter is roughly independent of the phase shift setting.

A sample of the measured IF spectrum for the first test circuit is shown in

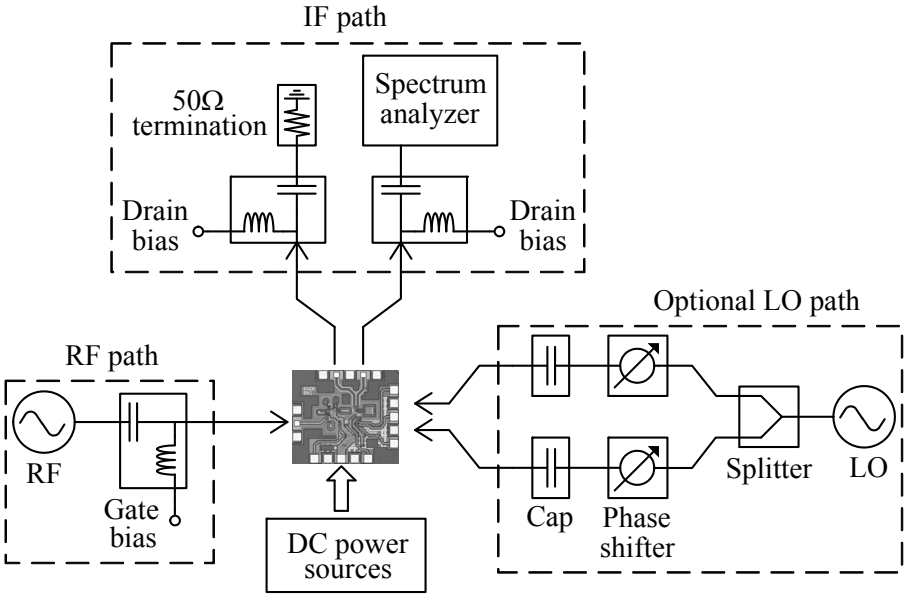

Figure 6.22 Measurement setup for power gain characterization

Figure 6.23 for a –20dBm single-tone RF input at 24GHz and an internal LO at 19.15GHz. Multiple frequency tones are observed in the measured spectrum. The RF-to-IF leakage and components downconverted by even-order LO harmonics (i.e. $2LO-RF$ and $2LO-2RF$) are common-mode signals at the mixer output. They will be rejected by differential sensing at the IF (except residual components due to circuit mismatch). On the other hand, the LO-to-IF leakage is a differential residue which should be nulled by double-balanced mixing from an ideal Gilbert mixer [6.17]. With increasing RF input power, measurements show that the sixth frequency tone to appear in the IF output spectrum (not shown in Figure 6.23) is the differential IF component $3LO-2RF$ located at 9.45GHz (i.e., the LO's third harmonic downconverts the second-harmonic distortion from the LNA).

The mixer power gain is first characterized by the second test circuit, where the VCO is free running at 19.0GHz. Figure 6.24 shows the simulated (25Ω or 50Ω load) and measured (25Ω load) power gain versus the input frequency at RF from 22GHz to 26GHz. Because the IF path is shared with the VCO output buffer (which has a 50Ω on-chip termination), the measured mixer power gain corresponds to an equivalent load impedance of 25Ω. Measurement data shows similar gain roll-off versus frequency to the simulation, but has a discrepancy ($\Delta_{measurement}$) of about 1dB. This difference should be due to signal loss from the IF transmission lines and

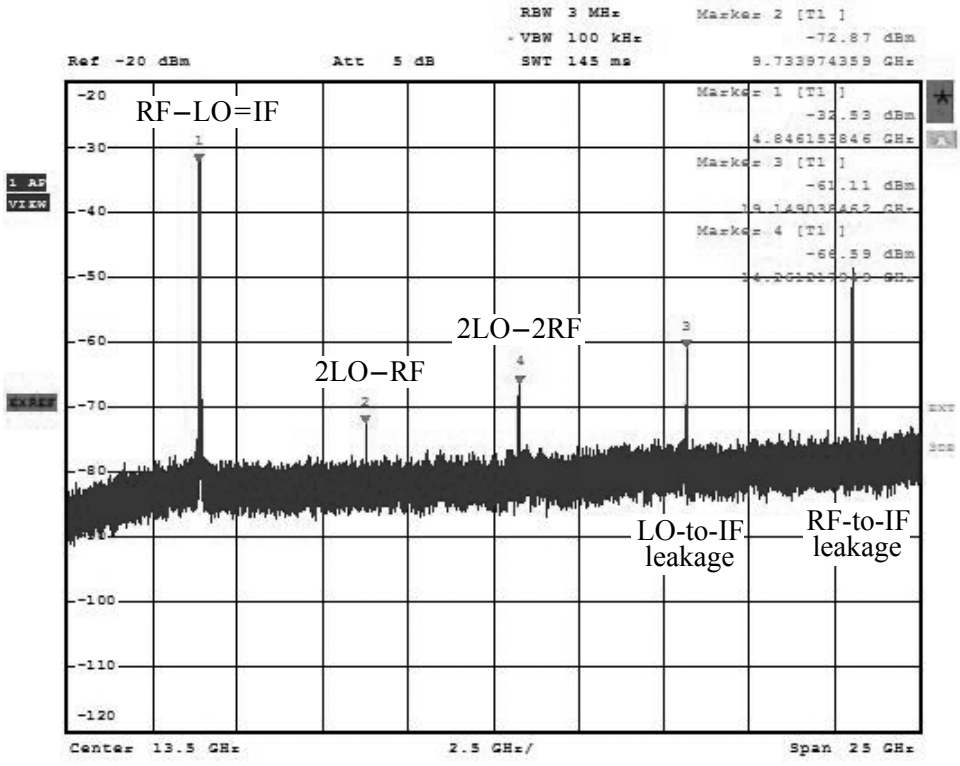

Figure 6.23 Measured frequency spectrum at the single-ended IF output

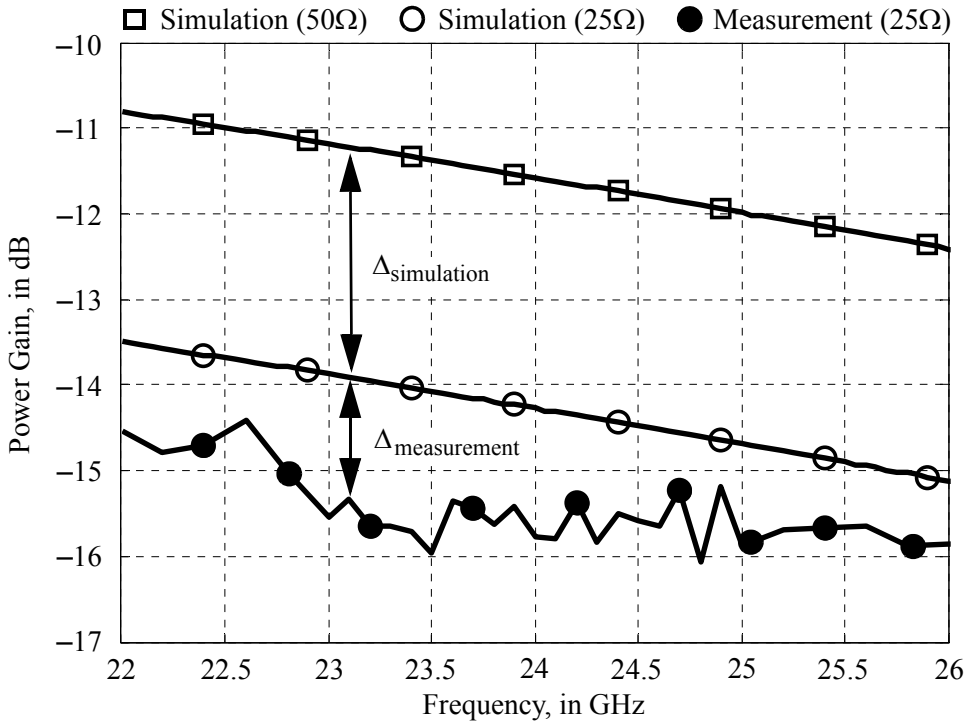

Figure 6.24 Simulated and measured mixer power gains versus RF

additional parasitic capacitance from IF probe pads, because they are not included in the simulations. When drawing 2mA from a 1V supply, measurement shows that the mixer power loss is 15.8dB at 24GHz.

The mixer integrated in the frequency downconverter has an open-drain output. The simulated mixer power gain with 50Ω load is also compiled in Figure 6.24. The measured mixer power gain with 50Ω load is expected to follow the trend of the measurement results with 25Ω load, and to be improved by the difference between their respective simulation data (i.e. $\Delta_{simulation}$). Similarly, the power and voltage gain with a tuned load at IF is predicted to increase by another 10.4dB and 21.2dB, respectively, at 24GHz according to the simulations shown in Figure 6.19.

With the same measurement setup, the first test circuit is characterized for power gain from the frequency downconverter. The VCO is free running at 19.0GHz, and the LNA and mixer draw 3mA and 2mA from a 1V supply, respectively. Figure 6.25 shows the measured power gain with 50Ω load overlaid with the simulated power gain for 50Ω and resonant tuned RLC loads. The measurement data closely resembles predictions from simulation, except that the peak frequency shifts downward from 23.75GHz to 22.60GHz, and the −1dB gain bandwidth decreases from 2.2GHz to 2.1GHz. The measured peak power gain is 2.14dB, which is expected to increase by 10.5dB (RLC simulation in Figure 6.25) when resonant tuning is applied at the mixer IF output.

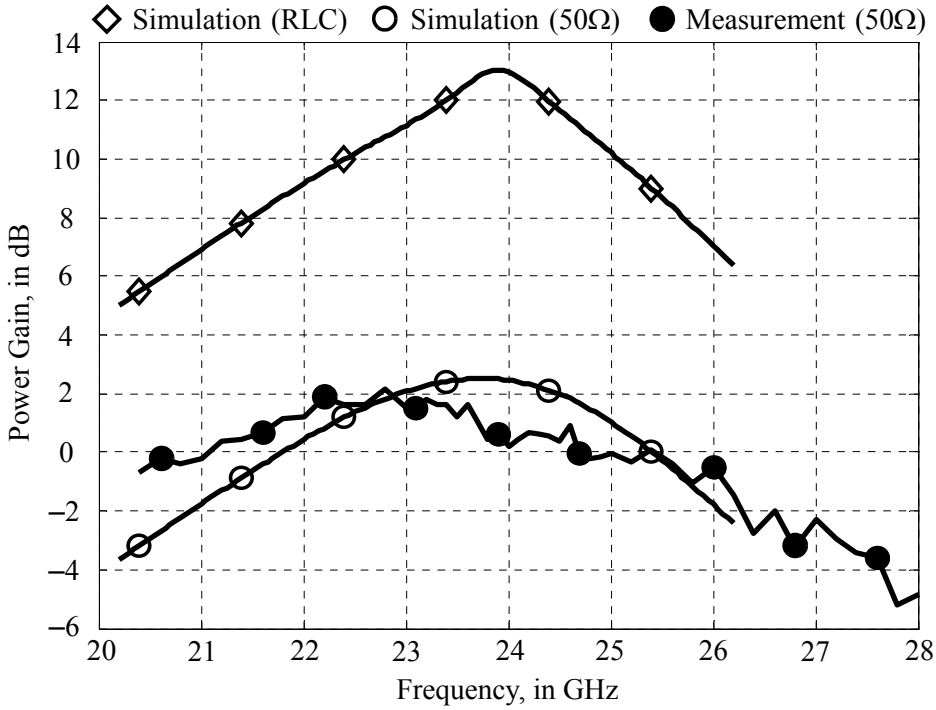

Figure 6.25 Simulated and measured downconverter power gains versus RF

Power gain of the LNA is indirectly measured by subtracting the power gain of the frequency downconverter (first test circuit) and the mixer (second test circuit) under the condition that both test circuits are measured for the same load of 50Ω. The results are illustrated in Figure 6.26. The two stage LNA (shown in Figure 6.10) is measured at two power dissipation settings in order to demonstrate the feasibility of trading off battery life for RF performance. It consumes either 3mW (1.5mW in each stage) or 4.3mW (2.5mW and 1.8mW in the 1st and 2nd stages, respectively). Compared to simulation, the measured LNA peak frequency shifts down from 24.0GHz to 23.2GHz, but with a higher peak gain value of 0.45dB, and an increase of the –3dB gain bandwidth from 4.0GHz to about 5.0GHz. The higher Q factor of the LNA power gain transfer curve in Figure 6.26 compared to the frequency downconverter is due to the effect of the mixer power gain roll-off in Figure 6.24 on the measurement data in Figure 6.25. A LNA power gain of 15dB can be achieved using a higher DC power consumption. For example, 16.5dB gain is obtained at a dissipation at 4.3mW.

The measured input reflection coefficient ($|S_{11}|$) of the frequency downconverter agrees well with the simulated prediction. It is shown in Figure 6.27. Its minimum value is very close to the simulation value of –25dB except for the frequency, which shifts from 23.5GHz to 24.7GHz (+5.1%). This discrepancy could be attributed to imperfections in the passive and active devices models (e.g., accuracy of the

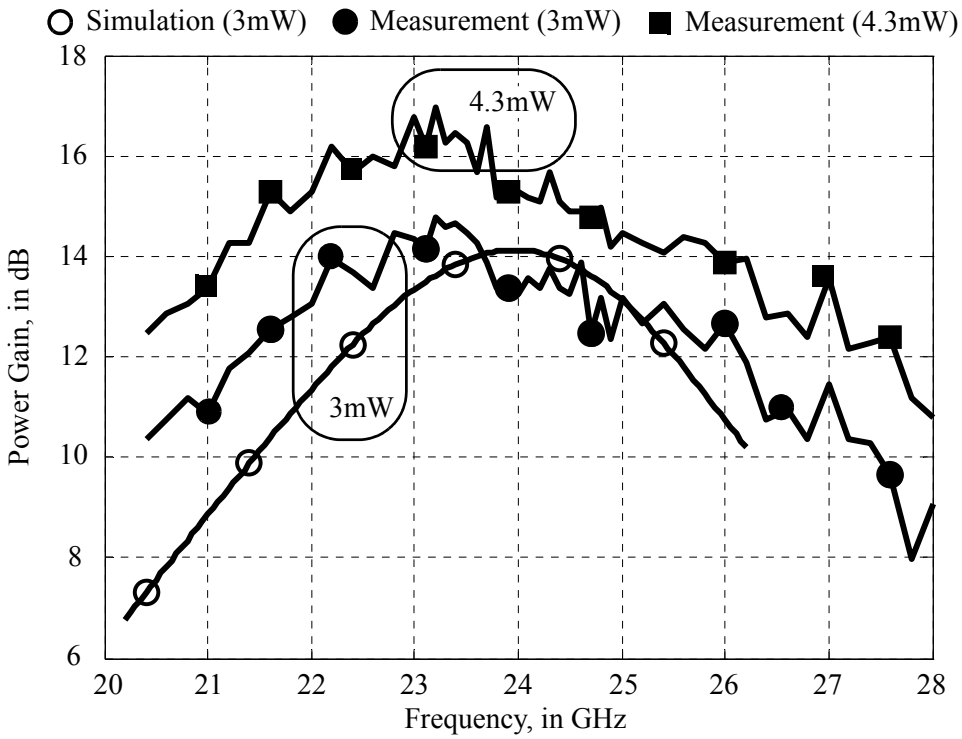

Figure 6.26 Simulated and measured LNA power gains versus RF

parasitic capacitance values). Both the simulated and measured $|S_{11}|$ are better than −10dB across the 20GHz and 26GHz band. The measurement shows a wider frequency span for 50Ω input matching, where the upper frequency range at 26.5GHz is limited by the network analyzer.

Linearity of the frequency downconverter and its building blocks are quantified by the input-referred third-order intercept points (IIP_3) from a two-tone test. The RF source shown in Figure 6.22 is substituted by a power combiner whose input ports are connected to two RF signal generators with equal power levels at frequencies of 23.9GHz and 24.1GHz. As explained in the power gain characterization, the mixer (second test circuit) and frequency downconverter (first test circuit) are measured for IF loads of 25Ω and 50Ω, respectively. Simulation provides the flexibility to compare the influence of the load impedance on mixer linearity, and sorting out the linearity relationship of circuit blocks in a cascade of stages. The IIP_3 for these test circuits with different combinations of load impedance values are tabulated in Table 6.3.

While the measurement data is obtained by driving the mixer with the on-chip VCO free running at 19.0GHz, an ideal sinusoidal source is used in the simulations. This is due to convergence problems for a two-tone simulation with a self-oscillatory circuit when using an S-parameter model for the magnetic components.

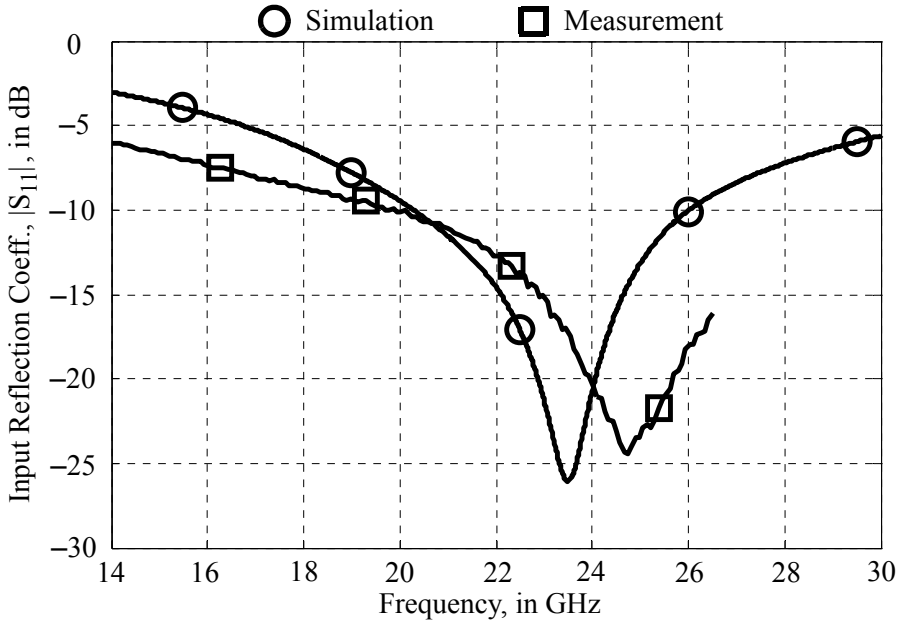

Figure 6.27 Simulated and measured downconverter input reflection coefficients ($|S_{11}|$) versus RF

Simulations show that the load impedance has a marginal impact on the IIP_3. For different load impedances at the mixer (25Ω, 50Ω, or resonant load), variations in the IIP_3 is only 0.40dB. Similarly, a 50Ω or resonant load at the frequency downconverter varies its IIP_3 by 0.58dB. The measured IIP_3 data are expected to follow the trend of these simulations. Therefore, the expected IIP_3 measurement of the mixer test chip having a resonant load should be 1.55dBm, provided that the mixer measured IIP_3 with a 25Ω load is 1.87dBm and a –0.32dB correction factor (0.05dBm−0.37dBm) is used in Table 6.3. This expected IIP_3 measurement is 1.5dB better than the simulation. The expected IIP_3 measurement of the frequency downconverter with a resonant load is derived in a similar manner, giving a value of –12.1dBm, which is 1.5dB better than the simulation.

Deducing the measured IIP_3 of the LNA is not straightforward because the cascade linearity equation of Eqt. (2.23) assumes the worst-case scenario (i.e., all distorted components added coherently). However, the simulated IIP_3 data of the circuit blocks with 50Ω load (highlighted by † in Table 6.3) could be used as a starting point to estimate the cascade-stage linearity relationship. A fictitious LNA power gain (G_{fict}) of 12.4dB is first obtained by applying the IIP_3 parameters to Eqt. (2.23), where

$$G_{\text{fict}}(dB) = 10 \cdot \log\left[\left(\frac{1}{10^{-12.7/10}} - \frac{1}{10^{-4.73/10}}\right) \cdot 10^{0.45/10}\right]. \qquad (6.15)$$

Table 6.3 Simulated and measured input referred third-order intercept points (IIP_3) for circuits under different loading conditions

	Resonant tuned network	Resistive 50Ω	Resistive 25Ω
LNA @3mW	–6.0dBm (expected)	–4.73dBm† (simulation)	
Mixer @2mW (simulation)	0.05dBm	0.45dBm†	0.37dBm
Mixer @2mW (measurement)	1.55dBm‡ (expected)		1.87dBm
Downconverter (simulation)	–13.3dBm	–12.7dBm†	
Downconverter (measurement)	–12.1dBm‡ (expected)	–11.5dBm	

† Simulated IIP_3 data with 50Ω load

‡ Expected IIP_3 data from measurement and correction factor

Assuming that the distorted components in both simulation and measurement maintain the same phase relationship, an expected LNA IIP_3 of –6.0dBm is attained by substituting the fictitious power gain with the expected mixer and frequency downconverter IIP_3 (highlighted by ‡ in Table 6.3) into Eqt. (2.23).

For an LO frequency at 19.2GHz, the simulated image rejection for an IF at 4.8GHz (i.e. the signal and image frequencies located at 24GHz and 14.4GHz, respectively) is about 21.2dB. This image power attenuation is contributed solely by the LNA selectivity.

The LO-to-RF leakage (isolation) and noise figure of the frequency downconverter are characterized by the third test circuit, which uses an external LO. A stable and clean signal generator is necessary for measuring the tiny LO leakage at the RF port, and measuring noise figure without impairments from VCO phase noise. The 13.11dBm LO power applied to the test circuit at 19.0GHz is attenuated to –0.46dBm at the mixer LO port (i.e., 13.57dB attenuation along the LO path). Considering the differential 100Ω on-chip termination and parasitic capacitance at the LO port, this power level corresponds to an LO amplitude of $0.5V_{pk}$ differential. A spectrum analyzer connected to the RF input identified a –67.74dBm tone at the LO frequency. Accounting for the 6.10dB RF path loss at 19.0GHz, the measured LO-to-RF leakage is 61.2dB down.

The noise figure measurement setup is similar to the one shown in Figure 6.22, but with a noise source attached to the RF input. The IF signal path is immediately followed by a second frequency downconversion before measurement with a noise figure meter. This downconversion path consists of a fixed-frequency, cavity-

type bandpass filter at 5.5GHz (with a Q of 6.9), a double-balanced diode mixer, and a 33MHz low-pass filter at baseband frequency. Because the IF is fixed at 5.5GHz, noise figure across the input frequency range is measured by sweeping the LO frequency from 16.5GHz to 20.0GHz in 0.5GHz steps, which correspond to an RF from 22GHz to 25.5GHz. The upper limit is imposed by the maximum frequency range available from the external LO signal generator.

Figure 6.28 shows the simulated and measured noise figures of the frequency downconverter. Following the same interpretation on the mixer simulation results shown in Figure 6.20, employment of a parallel resonant network rather than a 50Ω load at IF lowers the noise figure by 1.85dB to 2.32dB across the RF input range. The ±1dB fluctuation of the measured noise figure is primarily caused by impedance mismatch between the mixer open-drain output transistor and the 50Ω reference impedance. This mismatch introduces erroneous terms in the noise figure calibration. The low power gain (measured from –0.5dB to 2dB, as shown in Figure 6.25) of the frequency downconverter cannot suppress this calibration error [6.18]. The curve-fitted approximation to the measured data is about 1.2dB to 2.4dB higher than the predicted results from simulations. Calculations show that its discrepancy at 24GHz could be contributed by either a 5.4dB or 3.2dB increment in the LNA or mixer noise figures, respectively. This is based on the simulation data at 24GHz, where the LNA maximum available gain and noise figure are 17.5dB and 4.9dB,

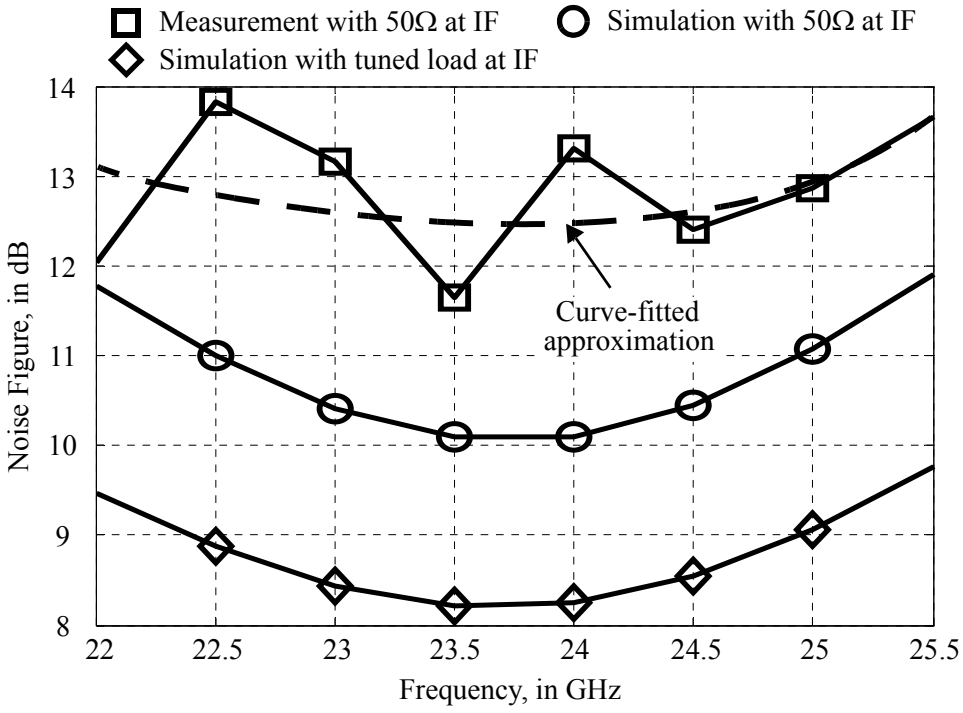

Figure 6.28 Simulated and measured noise figures of the frequency downconverter for a fixed 5.5GHz IF and 50Ω reference impedance versus RF

respectively (shown in Figure 6.13), and the mixer noise figure is 26dB (referred to the LNA output impedance). The measured power gain, input reflection coefficient, and third-order intercept point for the LNA closely match the simulation results. However, the mixer measured power gain is lower than the simulation result by about 1.5dB. Therefore, it is expected that the mixer noise figure increases from 26dB (simulation) to 29.2dB (measurement), rather than the LNA noise figure increases from 4.9dB (simulation) to 10.3dB (measurement).

Tables 6.4 and 6.5 summarize the measured performance of the test circuits, and list other 24GHz-range LNA and frequency downconverters published in the literature for comparison.

All of the LNAs presented in Table 6.4 are different combinations of common-source (CS), common-gate (CG), and cascode topologies, except the design developed in this work and [6.20], where a dual-gate transistor is used. The dual-gate FET is similar to a cascode amplifier, but with common source and drain junctions merged (eliminating some of the capacitance) at the shared node of the CS and CG device. Among these LNAs, the proposed current-feedback cascode topology achieves the lowest power dissipation, while maintaining a power gain higher than 14dB. The LNA in [6.19] saves 0.22mW but for a 5.3dB penalty in gain. Other LNAs either burn more power for less gain [6.24], or demand 4 to 8 times more DC power for a gain improvement from 0.2dB to 5.5dB.

The presented LNA does not have an outstanding noise figure. It is either comparable to [6.20] and [6.22], or only better than [6.23] by 0.4dB to 1.1dB, but for 4 to 6 times less power dissipation. On the other hand, its input matching is the best among all these LNAs, given that [6.21] has only a –3dB gain bandwidth of 2.6GHz, and [6.24] gives the second lowest power gain of 9.9dB.

Linearity performance is similar across these LNAs, except [6.22] (assume $IIP_3 = P_{-1dB} + 10dB = -0.7dBm$) which has the second highest power consumption in the list.

The presented frequency downconverter demands the lowest LO amplitude. However, it also delivers the second lowest gain because the IF amplifier in the receiver chain is excluded from the test circuit. For example, the IF amplifiers in [6.23] (called a mixer output buffer) and [6.25] (called a baseband amplifier) consume 34.5mW and 17.4mW, respectively. A 1.5dB IF amplifier gain in [6.24] results in the frequency downconverter having a power gain as low as 3.2dB, given that its LNA gain is 9.9dB.

The more than tenfold increase in power dissipation observed in [6.23] and [6.25] gives a 3dB to 4dB advantage in noise figure compared to the presented work. Lowering the gap in power budget by 2.7 times in [6.24] reduces the difference in noise figure to only 1.5dB. Similar to the LNAs, the lowest power gain of [6.24] returns a 10dB higher IIP_3 among the four frequency downconverters presented in Table 6.5.

Table 6.4 Comparison of LNAs

Reference	This work	[6.19]	[6.20]	[6.21]	[6.22]	[6.23]	[6.24]	[6.25]
Topology	2-stage current-feedback cascode	2-stage common-source	2-stage dual-gate transistor	2-stage: CS + cascode	2-stage: cascode + CS	3-stage: CG + CS + CS	single-stage differential cascode	2-stage cascode
Center frequency (GHz)	23.2	23.6	23.0	28.5	24.0	21.8	21.0	24.0
Peak power gain (dB)	14.5	9.2	18.9	20	14.7	15	9.9	18
–3dB gain BW (GHz)	5.0	3.7	7.3	2.6	3.5	not reported	> 6	3.0
Noise figure (dB)	4.9 to 5.6	3.7 to 4.5	4.7 to 5.8	2.9 to 4.2	4.3 to 5.8	6	3.8 to 4.3	4.2
IIP_3 (dBm)	–6.0	–2.9	–4.5	–7.5	–10.7 ($P_{-1dB,in}$)	not reported	not reported	not reported
$\|S_{11}\|$ (dB)	–24.5 to –12	–16 to –5	–8 to –7	–22 to –12	–27 to –7.5	–20.5 to –18	–27 to –15	–17 to –5
P_{DC} (mW)	3	2.78	12	16.25	20.2	24	8	21.1
DC Supply (V)	1	1	2	1	1 and 1.5	1.5	1.6	1.2
Technology	90nm CMOS	0.13μm CMOS	65nm CMOS	90nm CMOS	0.13μm CMOS	0.18μm CMOS	0.13μm CMOS	65nm CMOS

Table 6.5 Comparison of frequency downconverters

Reference	This work	[6.23]	[6.24]	[6.25]
Topology	Heterodyne Gilbert mixer	Heterodyne single-balanced mixer	Homodyne sub-harmonic mixer	Homodyne sub-harmonic mixer
Differential LO amplitude (V_{pk})	0.5	0.8	0.9	0.8
Center frequency (GHz)	22.9	21.8	24.0	24.1
Peak power gain (dB)	12.6 (w/o IF amp)	27.5 (w/i IF amp)	3.2 (IF amp: 1.5dB)	31.5 (w/i IF amp)
–3dB gain BW (GHz)	1.25	0.7	0.67	2.5
Noise figure (dB)	10.6 to 11.5	7.7 to 8.1	10	6.7 to 8.8
IIP_3 (dBm)	–12.1	–23 ($P_{-1dB,in}$)	–12.7 ($P_{-1dB,in}$)	–13
P_{DC} (mW)	5	64.5	13.6	55.3
DC Supply (V)	1	1.5	1.6	1.2
Technology	90nm CMOS	0.18μm CMOS	0.13μm CMOS	65nm CMOS

6.4 Summary

Current feedback via a 3-port transformer is proposed in order to reduce the mismatched impedance conditions within a cascode LNA and thereby improve its power gain and noise figure. The common-gate transistor's input and optimum source impedances for power gain and noise figure are matched to the common-source transistor's output impedance by applying current feedback. With the DC power budget as a primary design constraint, this LNA delivers the best possible power gain and noise figure performance out of the limitations imposed by the intrinsic transistors and passive devices losses. Circuit analysis and a Smith-chart based optimization technique are applied to the proposed LNA topology. A proof of concept is implemented by a two-stage, current-feedback cascode LNA which produces 14.5dB and 16.3dB power gains measured at power consumptions of 3mW and 4.3mW, respectively. Physical implementation with multiple magnetic components, signal integrity associated with the current return path, and circuit simulations employing an S-parameter table lookup model are addressed and emphasized in the LNA development. A frequency downconverter is realized by integrating this LNA with a Gilbert-type mixer, and the VCO presented in Chapter 4. The 8-port trans-

former balun preceding the mixer isolates the LNA single-ended current return path from the rest of the radar receiver, and simultaneously provides a load impedance to satisfy the LNA power gain matching requirement. This receiver front-end meets the FMCW SRR electrical requirements derived in Chapter 3 by delivering 12.6dB gain, 11.5dB noise figure, and –12.1dBm IIP_3 while drawing 10.7mW from a 1V supply.

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Chapter 7

Conclusion and Recommendations

This thesis presents the system design of a 24GHz-band short-range radar receiver, and its circuit implementation in a 90nm CMOS technology. This chapter concludes the findings of the work, highlights the contributions, and provides recommendations for future work.

7.1 Findings

Optimization of a multi-stage LNA can be simplified by the manipulation of certain performance metrics viewed on a complex impedance plane. Overlaying the LNA input and output reflection coefficients with its noise figure circles, source/load stability circles, and operating power gain circles visualizes the trade-offs between design parameters. This optimization technique is important in power-constrained mm-wave LNA design because the carrier frequency is approaching the transistor's operational limit.

FMCW radar is well-suited to the implementation in nanometer CMOS technology because of the continuous Tx and Rx operation. A simple buffer with the function of isolating the VCO from the external circuits could obviate the requirement for a PA. Maintaining the IF in the lower frequency range for a short-range application takes advantage of VCO phase noise reduction and relaxes the processing bandwidth requirements from the decision circuitry.

A homodyne receiver in an FMCW radar suffers from exacerbated frequency pulling problem by the transmitter PA, because the ultra-wideband and continuous tuning range from the VCO shows high sensitivity. The second-order intermodulation linearity from a homodyne receiver must also be sufficient to handle erroneous reception of radiation from interfering FMCW radars, and to minimize amplitude demodulation of the transmitted signal from pulsed Doppler radars in the surroundings.

The heterodyne architecture mitigates imperfections from flicker noise, DC offset, second-order non-linear distortions, and VCO pulling. The image-reject filter in a heterodyne FMCW radar receiver is redundant because the interference frequency is either stationary or not coherent with the chirp rate of an FMCW signal. The VCO phase noise and tuning range requirements are also relaxed by operating

at a lower frequency. The third-order non-linearity in the receiver is not seen as a performance bottleneck because of the signal averaging across successive scanning periods.

Varactor quality factor tends to dominate VCO resonant tank losses at mm-wave frequencies in CMOS technology. In addition, there is a trade-off between varactor Q and capacitance tuning ratio, where both of them decrease with increasing frequency. The maximum dimension for the varactor is also constrained in a low-power application. This restricts the tuning range of a conventional LC VCO to less than 10% at approximately 20GHz, and less than 5% at 60GHz. Capacitor bank switching has the advantage of lowering the VCO tuning sensitivity, and therefore relaxes the trade-off between tuning range and VCO phase noise. However, its limitations in capacitive tuning ratio and Q factor are similar to a varactor in bulk CMOS technology.

Biasing a MOS transistor in the moderate inversion region reduces its transconductance and power gain. This also translates to a higher minimum noise figure. Additionally, resistive losses contributed by an on-chip matching network increase the LNA noise figure further. On the other hand, the same IIP_3 at 0dBV can be delivered by the same NMOS transistor in a 90nm CMOS technology when biased at a drain current density of either 34.6μA/μm or 180μA/μm. Applying second-harmonic terminations to the LNA source and load impedances could further improve the IIP_3. Therefore, the priority for a low-power, mm-wave LNA when optimizing the design is primarily on achieving the power gain and noise figure specifications, and secondarily on meeting the linearity performance requirement.

The influence of input matching network resistive losses on the LNA noise figure depends on the relative magnitude of the LNA equivalent input voltage and current noise sources. Noise contribution from a series resistive loss is much less significant if the voltage noise power is much higher than the current noise power. A similar observation applies for a parallel resistive loss if the current noise power is dominant. For a NMOS transistor in 90nm CMOS, a larger amount of voltage rather than current noise is observed at 24GHz for a transistor total gate width narrower than 6 millimeters. Therefore, a series inductor (with loss in series with the MOS gate) is usually applied to a CMOS LNA input matching network for typical transistor dimensions.

Partitioning the limited power budget across multiple LNA gain stages maximizes the overall power gain achievable. For a NMOS common-source amplifier in a 90nm CMOS technology, doubling or quadrupling the drain current density boosts the power gain by 2.09dB or 4.13dB, respectively. However, maintaining the same current density per stage, and cascading two or four stages gives a potential power gain increase of 5.36dB or 16.1dB, respectively. Similar observations are found for the common-gate amplifier. This advantage is limited by the number of inter-stage passive matching networks, because the silicon area occupied grows with the num-

ber of stages. Furthermore, meeting the overall noise figure and linearity specifications is affected, because NF_{min} and IIP_3 in each stage are degraded at a lower drain current densities, and there are increased contributions from multiple of stages. The same principle applies when partitioning the power supply voltage headroom to multiple amplifier blocks (connected in cascode) as long as the MOS transistors remain in the saturation region.

Conventional LNA optimization compares the f_{MAX} parameter by sweeping the transistor(s) dimension and bias current for either a transistor configured as a common-source amplifier, or composite transistor amplifier structures (such as a cascode or multi-cascode). This method ignores the possibility that different amplifier topologies could deliver a distinct optimum in transistor dimensions, and the potential performance improvement from impedance matching between individual transistors.

The short interconnection between amplifier cells in an integrated circuit does not require conjugate matching to minimize power reflection. However, there are matching conditions for minimum noise figure of cascaded stages according to Friis' equation, and for maximum power gain from the methodology of power gain circles. Sometimes an explicit matching network cannot simultaneously satisfy the noise and power matching conditions because the input and optimum source impedances of an amplifier are dependent on each other. For a common-source amplifier, applying feedback overcomes this limitation, such as the series-series feedback by inductive source degeneration or the shunt-shunt feedback by gate-drain capacitance.

7.2 Contributions

A 24GHz-band radar system is designed within the framework of short-range application with a low bill of materials cost and low power consumption. For the receiver architecture, the direct-conversion receiver is less suitable for short-range radar applications because of frequency pulling and second-order intermodulation nonlinearity problems. An FMCW radar is proposed and implemented using a heterodyne receiver. Its advantages are: low transmitted power, phase noise reduction due to time correlation, simplified frequency planning and generation, and mitigation of the image problem. The receiver link budget calculations and building blocks specifications towards implementation in a CMOS technology were also addressed.

The traditional varactor-based VCO fails to generate the multi-gigahertz continuous and wideband FMCW transmitted spectrum with high range resolution. A varactorless frequency tuning scheme is proposed for the VCO which breaks through the conventional trade-offs seen in continuous and wideband mm-wave frequency generation between capacitance tuning ratio, quality factor, and operating frequency in CMOS design. [7.1,7.2]. Two test circuits are reported in this thesis. A proof of concept in 0.13μm CMOS consumes 43mW from a 1.2V supply. The fre-

quency coverage is from 23.2GHz to 29.4GHz (23.6% tunable range) and the phase noise is –92.6dBc/Hz at 1MHz frequency offset. A miniaturized prototype is also implemented in 90nm CMOS for the radar receiver. It consumes 5.7mW from a 1V supply. Its maximum frequency range is from 18.6GHz to 21.2GHz (13.1% tunable range) and phase noise is –82.0dBc/Hz at 1MHz frequency offset. Inductive tuning of the VCO frequency is enabled by introducing a transformer resonant tank which exploits the 90° terminal voltages of a transconductor, and control its parallel resonant frequency by sweeping the sign and magnitude of the transconductance. The VCO is frequency-agile, and is continuously tunable by altering the DC bias current from the transconductance cell. Adaptability between frequency tuning and power consumption is also possible because the VCO frequency is current-controlled.

In order to overcome the weakness of the conventional LNA design methodology due to the strong bilateral power flows via the gate-drain parasitic capacitor of transistors in CMOS technology, a new two-step optimization algorithm for low-power mm-wave LNA is proposed [7.3]. At the device level, the individual transistor is properly dimensioned in order to satisfy power gain, noise figure, linearity, bandwidth requirements, and minimize performance degradations due to matching network losses. This results in different optimal transistor dimensions for each amplifier topology. At the circuit level, current budget partitioning and supply voltage scaling on a multi-stage amplifier maximize the overall power gain achievable. The impedance matching conditions between transistors in the cascade of stages are co-ordinated by manipulation of the input and output reflection coefficients of each transistor with its noise figure circles, source/load stability circles, and operating power gain circles on a complex impedance plane. An efficient Smith chart based visualization and a computer-aided design methodology are also proposed in order to simplify the simultaneous optimization on the overall power gain, noise figure, input return loss, and stability of a CMOS based multi-stage LNA.

A new current-feedback topology employing a 3-port transformer is proposed for the common-gate amplifier in order to de-couple its input and optimum source impedances. This overcomes the suboptimal power gain and noise figure observed in a cascode LNA under low-power condition. A two-stage, current-feedback cascode LNA is implemented in 90nm CMOS as a proof of concept. Consuming 3mW from a 1V supply, the LNA achieves 14.5dB peak power gain, –3dB gain bandwidth of 5.0GHz, noise figure varies from 4.9dB to 5.6dB across the 22GHz to 26GHz RF bandwidth, and an IIP_3 of –6.0dBm. The power gain increases to 16.3dB by increasing the power consumption to 4.3mW. With the DC power budget as a primary design constraint, this LNA delivers the best possible power gain and noise figure out of the limitations imposed by the intrinsic transistors and passive losses. Circuit analysis and a Smith-chart based optimization techniques are applied to the proposed LNA topology. The merits of physical implementation with multiple magnetic components, signal integrity associated with current return path, and circuit simulations employing an S-parameter based model are addressed and emphasized

in the LNA development.

A frequency downconverter was realized by integrating the inductive-tuned VCO and current-feedback LNA with a differential Gilbert-type mixer. This receiver RF front-end draws 10.7mW from a 1V supply, and delivers 12.6dB peak power gain with a –3dB gain bandwidth of 1.25GHz. Noise figure varies from 10.6dB to 11.5dB across the RF bandwidth, and the IIP_3 is –12.1dBm. Isolation of the LNA's single-ended current return path from the rest of the receiver is maintained by an 8-port transformer balun preceding the mixer. This receiver front-end meets the FMCW short-range radar electrical specifications derived from the system design requirements.

7.3 Future Work

This thesis demonstrated that the implementation of a 24GHz-band short-range radar receiver in a 90nm CMOS technology with only 15mW of power dissipation is feasible. Further studies in the area of radar systems are necessary in order to determine potential improvements.

Development of a radar receiver requires integration of other building blocks. This includes the remaining blocks in the IF signal path shown in Figure 3.8, and a phase-locked loop which embeds and modulates the proposed VCO for wide-band FMCW signal generation. A transmitter circuit having –6.53dBm continuous output power and a pair of Tx and Rx antennas to the receiver would complete the radar transceiver. Practical radar evaluation by transmission and reflection of EM wave with physical objects would then be possible. The radar system parameters can also be validated experimentally by measuring the signal-to-noise ratio at the receiver IF output for targets of different sizes, shapes, and ranges.

The radar system design presented in Chapter 3 is solely based on hand calculations assuming ideal radar signal waveforms and link budget equations. System simulation is required to capture the effects of different non-idealities on the radar detection accuracy. This includes the transmitted FMCW signal chirp non-linearity, antenna radiation pattern, multi-path propagation of the transmitted and reflected EM waves, etc.

The frequency tuning ranges reported for the two VCO testchips are measured by sweeping the bias current on the transconductance cell. Because parasitic capacitances of the MOS transistor are voltage dependent, the supply voltage [7.4] or bias current in the negative resistance cell [7.5] offers additional tunability of the VCO oscillation frequency. These two tuning schemes promise the possibility of frequency-band switching for auto-zeroing the VCO center frequency. An amplitude-control loop [7.6] to maintain a constant oscillation amplitude could also be a potential improvement to the proposed VCO.

The variable current sources in the VCO transconductance cell could be

substituted by two current DAC, in which the feasibility of compensation for non-linearity of the VCO frequency chirp in the digital domain could be investigated.

The magnetic devices used in the frequency downconverter are modelled as a multi-port composite structure where a single S-parameter model captures the input-output characteristics. The S-parameter file must be combined with transistors, resistors, and capacitors lumped-element model for transistor-level circuit simulations. This modelling approach has the advantage of incorporating all parasitic couplings between adjacent magnetic components and the local supply and ground plane. However, improvements are needed to increase its efficiency and flexibility.

For most EM simulators (e.g., Momentum from Keysight Technologies [7.7]), meshing is applied to metal layers of the magnetic devices. Maxwell's equations are then solved numerically for each mesh unit. The mesh dimension is a fraction of the signal wavelength at the maximum frequency of interest, and the mesh is uniformly applied to a given metal layer. Because all magnetic devices and the local supply and ground plane in multiple metal layers are merged into a single structure, the finest mesh dimension employed for the RF circuit blocks (e.g., the LNA mesh frequency at $24\text{GHz} \times 5 = 120\text{GHz}$ to include the 5^{th} harmonic) is also applied to the VCO's LC tank (20.4GHz), and the 1^{st} IF bandpass filter (5.2GHz). Electromagnetic simulations are time consuming and require significant computing resources [7.8]. This creates a burden on the S-parameter-based model generation and limits the number of design iterations to optimize the parameters of each inductor in the composite structure.

Although the S-parameter-based model incorporates all parasitic coupling within the composite structure, it gives no insight to highlight the parasitic coupling path or to identify the possibilities for improvements to the magnetic structure.

The simulation methodology presented in Chapter 6 uses the S-parameter-based model for verification rather than optimization. Each transformer is independently modelled and embedded in transistor-level simulations for circuit optimization. All transformers are combined as a single composite structure afterwards for EM simulation. Verifications of the frequency downconverter are then performed to ensure that performance changes due to parasitic EM coupling and local supply and ground plane inductance are within the tolerable limits.

An improved strategy for S-parameter-based model generation and transistor-level co-simulation with lumped-element models is necessary to shorten the EM simulation time and increase the flexibility of magnetic device optimizations.

The application of S-parameter data file into transistor-level simulation is available from different circuit simulators [7.9,7.10]. However, the proposed simulation methodology results in an unusually large number of ports in the composite EM structure. For example, the S-parameter file has 43 ports and 36 ports for the first (LNA+mixer+VCO) and second test circuits (LNA+mixer), respectively.

While most types of simulations perform normally with the S-parameter-based model, convergence difficulties were found for multi-tone simulation with a self-oscillatory circuit, and phase noise simulation of an oscillator. Applying different interpolation methods to the S-parameter file [7.9] results in tiny time steps [order of attoseconds (10^{-18}s)] with spline or linear methods, or an indefinite calculation time for a ROM data file with rational method. The problem does not exist if a simplified EM structure (i.e., only including the VCO LC tank) is used. A possible solution to the convergence difficulty is to convert the S-parameter model into a lumped-element equivalent circuit model similar to the those developed in [7.11 and 7.12].

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List of Abbreviations and Symbols

Abbreviations

ADC	Analog-to-Digital Converter
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BoM	Bill of Materials
BPF	Band-Pass Filter
BW	Bandwidth
CAD	Computer-Aided Design
CD	Common-Drain
CG	Common-Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common-Source
DAC	Digital-to-Analog Converter
DUT	Device-Under-Test
EIRP	Effective Isotropic Radiated Power
EM	Electromagnetic
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FET	Field-Effect Transistor
F	Noise Factor
FFT	Fast Fourier Transform
FM	Frequency Modulation
FMCW	Frequency-Modulated Continuous Wave
F_{min}	Minimum Noise Factor
FPGA	Field-Programmable Gate Array
Gnd	Ground
GSM	Global System for Mobile Communication
IC	Integrated Circuit
IF	Intermediate Frequency
LAN	Local Area Network
LC	Inductor-Capacitor
L/C	Inductance-to-Capacitance
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MAG	Maximum Available Gain
MIM	Metal-Insulator-Metal
mm-Wave	Millimeter-Wave

MMIC	Monolithic Microwave Integrated Circuit
MOS	Metal Oxide Semiconductor
MSG	Maximum Stable Gain
NF	Noise Figure
NF_{min}	Minimum Noise Figure
NMOS	N-Channel Metal Oxide Semiconductor
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PSD	Power Spectral Density
RADAR	Radio Detection and Ranging
RCS	Radar Cross-Section
RF	Radio Frequency
RFIC	Radio-Frequency Integrated Circuit
RLC	Resistor-Inductor-Capacitor
Rx	Receiver
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SNR_{in}, SNR_{out}	Input and Output Signal-to-Noise Ratio
SoC	System-on-Chip
SOI	Silicon-on-Insulator
S-Parameter	Scattering Parameter
SRR	Short-Range Radar
Tx	Transmitter
UWB	Ultra-wide Band
VCO	Voltage-Controlled Oscillator
VLSI	Very-Large-Scale Integration
ULSI	Ultra-Large-Scale Integration

Symbols

1/f	Flicker
a	a Constant
a_i	i^{th}-Order Transfer Characteristic Coefficient
A_e	Receiver Antenna Effective Area
A_i, A_v	Current and Voltage Gains
Area	Surface Area Covered by Interface States
A(t)	Instantaneous Amplitude
c	Speed of Light
C_{ac}	Blocking Capacitance
C_{filter}	Filtering Capacitor
C_{gs}	Gate-Source Capacitance

C_m	Band-Switched Capacitor
C_{max}	Maximum Capacitance
C_{min}	Minimum Capacitance
C_{out}	Output Capacitance
C_{ox}	Gate Oxide Capacitance per Unit Area
C_{par}	Parasitic Capacitance
C_{sw}	Switch Parasitic Capacitance
C_v	Varactor Capacitance
f	Frequency
$f_{carrier}$	Carrier Frequency
$f_{Doppler}$	Doppler Shift
f_{max}	Unity Maximum Available Gain Frequency
F_{LO}	Effective Noise Factor
g_m, G_m	Transconductance
G_A	Available Power Gain
G_{fict}	Fictitious LNA Power Gain
$G_{IP3,i}$	i^{th}-Stage Input-Referred Third-Order Intercept Point
G_p	Operating Power Gain
G_r	Receiver Antenna Gain
G_t	Transmitter Antenna Gain
i_{in}, i_{out}	Input and Output Current
I_D	Drain Bias Currents
IIP_2, IIP_3	Input-Referred Second and Third-Order Intercept Points
IM_2, IM_3	Second and Third-Order Intermodulation Distortions
k	Boltzmann's Constant or Magnetic Coupling Factor
K	Stability Factor
K_f	Device-Specific Flicker Noise Constant
L	Gate Length
$L\{\Delta\omega\}$	Phase Noise Power Spectral Density at $\Delta\omega$
M	Mutual Inductance
$N_{amp,out}$	Total Output Noise Originating from Amplifier
N_i	i^{th} Constant
N_{in}	Noise Power Accompanying an Input Signal
P_{AVA}	Power Available from Amplifier Output
P_{AVS}	Power Available from Source
P_D	Probability of Detection
P_{DC}	DC Power Consumption
P_{fa}	Probability of False Alarm
P_{in}	Power to Amplifier Input
$P_{interference}$	Interference Power
P_{load}	Power to Load
P_{LO}	Oscillation Signal Power
P_n	Integrated Noise Power

P_o	Power Strength
P_t	Transmitter Effective Isotropic Radiated Power
$PN_{normalized}$	Normalized Phase Noise
Q	Quality Factor
Q_{tank}	Tank Quality Factor
R	Target Range
R_{deg}	Degeneration Resistor
R_s	Gate Series Resistor
R_{tank}	Tank Losses
S_{11}, S_{22}	Input and Output Reflection Coefficients
S_{12}, S_{21}	Reverse and Forward Transmission Coefficients
S_w	Switch
$S_\phi(f)$	Phase Noise Power Spectral Density
$S_{\phi,FMCW}(f)$	FMCW Signal Phase Noise Power Spectral Density
t_{flight}	Round-Trip Flight Time
T	Absolute Temperature
T_m	Modulation Period
v_{in}, v_{out}	Input and Output Voltages
V_{DD}	DC Supply Voltage
V_{tune}	Tuning Voltage
W	Gate Width
W_{eff}	Effective Gate Width
W_f	Finger Width
Y_{in2}, Z_{in2}	Succeeding Stage Input Admittance and Impedances
Y_{int}	Intermediate Admittance
Y_{opt}, Z_{opt}	Optimum Source Admittance and Impedances
Y_{out}, Z_{out}	Output Admittance and Impedances
Y_{source}, Z_{source}	Source Admittance and Impedances
Z_{in}	Input Impedance
Z_{ind}	Overall Inductive Impedance
Z_{load}	Load Impedance
Z_o	Characteristic Impedance
Z_{tank}	Tank Impedance
Z_{total}	Parallel Combination of Z_{in2}, Z_{load}, and Z_{out}
α	Flicker Noise Constant
Δ	Determinant of Scattering-Parameter Matrix
ΔIF_{max}	Maximum IF Bandwidth
ΔR	Range Resolution
Δv_{target}	Relative Velocity to Target
$\Delta\omega$	Frequency Offset
$\phi(\tau)$	Instantaneous Phase
η	Matching Network Power Transfer Efficiency
Γ_{in}	Input Reflection Coefficient

Γ_{load}	Load Reflection Coefficient
Γ_{opt}	Optimum Source Reflection Coefficient
Γ_{out}	Output Reflection Coefficient
Γ_{source}	Source Reflection Coefficient
λ	Wavelength
μ	Thermal Noise Coefficient
σ	Target Radar Cross Section
τ	Discrete Time Intervals
ω	Angular Frequency
ω_m	Offset between Phase Noise and Oscillation Frequencies
ω_o	Oscillation Frequency
$\omega_o(\tau)$	Instantaneous Frequency
ω_{ref}	Reference Frequency

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List of Publications

Publications related to this thesis

Journal Papers

K.C. Kwok and J.R. Long, "A 23-to-29GHz transconductor-tuned VCO MMIC in 0.13μm CMOS," *IEEE Journal of Solid-State Circuits (Special Issue on the 2007 ISSCC)*, vol. 42, pp. 2878–2886, Dec. 2007.

Conference Papers

K.C. Kwok, J.R. Long, and J.J. Pekarik, "A 23-to-29GHz differentially tuned varactorless VCO in 0.13μm CMOS," *IEEE International Solid-State Circuits Conference*, 2007, pp. 194–195. (Beatrice winner award for editorial excellence)

K.C. Kwok and J.R. Long, "Bilateral design of mm-wave LNA and receiver front-end in 90nm CMOS," *IEEE International Symposium on Circuits and Systems*, 2008, pp. 181–184.

Workshops

K.C. Kwok and J.R. Long, "Analysis of multi-port transformer in VCO resonator design," *Proceedings of ProRISC 2005, 16th Annual Workshop on Circuits, Systems and Signal Processing*, 2005, pp. 233–236.

K.C. Kwok and J.R. Long, "Millimeter-wave low noise amplifier in 90nm CMOS," *Proceedings of ProRISC 2006, 17th Annual Workshop on Circuits, Systems and Signal Processing*, 2006, pp. 53–56.

K.C. Kwok and J.R. Long, "A 79GHz receiver front-end for automotive radar in 90nm CMOS," *Proceedings of ProRISC 2007, 18th Annual Workshop on Circuits, Systems and Signal Processing*, 2007, pp. 51–54.

K.C. Kwok and J.R. Long, "A 16GHz VCO and quadrature injection-locked divider circuits," *Proceedings of ProRISC 2008, 19th Annual Workshop on Circuits, Systems and Signal Processing*, 2008, pp. 202–205.

Biography

Ka Chun Kwok was born in Hong Kong in 1977. He received the Bachelor of Engineering and Master of Philosophy degrees, both in electrical and electronic engineering, from the Hong Kong University of Science and Technology (HKUST), Hong Kong, in 1999 and 2001, respectively. Since October 2004, he is working towards the doctorate degree at the Electronics Research Laboratory of the Delft University of Technology on the subject of millimeter-wave circuit design in CMOS technology.

In 2001, he worked on analog IC design in Broadcom Corporation, Singapore. Between 2002 and 2003, he was with the Analog Research Laboratory of HKUST where he pursued research on low-voltage RF-VCO in CMOS technology. He is specialized in analog and RFIC design, where he developed RF transceivers in Catena Microelectronics, Delft, from 2009 to 2010, and in NXP Semiconductors, Eindhoven, from 2011 to 2013.

He was the recipient of the 2007 International Solid-State Circuits Conference (ISSCC) Beatrice Winner Award for Editorial Excellence.