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An Aging-Robust 32MHz RC Frequency Reference with 0.4ppm Allan Deviation and ±1550ppm Inaccuracy from −40°C to 125°C after a 1-Point Trim

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RC-based frequency references [1-6] are widely used for clock generation in SoCs since they are compact, low power, and can achieve medium frequency accuracy. Designs based on low-TC poly resistors can achieve inaccuracies of a few 100ppm [1-5], but this is dwarfed by their drift, which can be as large as 5000ppm after accelerated aging [5-6]. Although designs based on via-metal [4] or diffusion [6] resistors exhibit significantly lower drift, in the order of several 100ppm, their larger TCs mean that a 2-point trim is required to achieve inaccuracies of several 100ppm. This paper presents an aging-robust 32MHz RC frequency reference based on diffusion resistors and a BJT-based temperature compensation scheme. After a low-cost 1-point trim, it achieves ±1550ppm inaccuracy from −40°C to 125°C, which increases to ±2350ppm after accelerated aging. Due to the extensive use of dynamic error-correction techniques, it also achieves an Allan deviation floor of 0.4ppm, corresponding to state-of-the-art short-term stability.

Figure 1 (a) shows the operating principle of an RC frequency reference with a BJT-based temperature compensation scheme [6]. It consists of a frequency-locked-loop (FLL), which locks the period of a VCO to the time it takes a reference current (I_{REF}) to charge a MIM capacitor (C_0) to a reference voltage (V_{REF}). Since the TC of C_0 is negligible, the VCO's output frequency (F_{OUT}) can then be stabilized by ensuring that the TC of V_{REF} matches that of I_{REF}. In [6], this is done by using a BJT-based biasing circuit and N-diff resistors to generate PTAT ($I_{PTAT}=\Delta V_{BE}/R$) and CTAT ($I_{CTAT}=V_{BE}/R$) currents, as shown in Fig. 1 (b), which are scaled and combined to generate V_{REF} and I_{REF}. The TCs of I_{REF} and V_{REF} can then be matched by using binary-weighted current mirrors to trim the scaling factors K_{RP}, K_{RC}, K_{CP} and K_{CC}. However, the mismatch of the current mirrors requires 2-point trimming, while their 1/f noise results in a high Allan-deviation floor (18.8ppm).

To address the issues above, a simplified biasing circuit is proposed, as shown in Fig. 1 (c). By simply adding a resistor in parallel with one of the BJTs [7], a reference current I_{REF} (= $\Delta V_{BE}/R_{B1} + V_{BE}/R_{B2}$) with both PTAT and CTAT components can be generated. Its 1st order TC (TC1) is mainly determined by the ratio of the resistors, their TCs and the TCs of V_{BE} and ΔV_{BE}. In a further simplification, V_{REF} is generated by dividing R_{B2} into two segments and injecting a copy of I_{REF} into the lower one. Its TC1 can then be tuned by adjusting the relative size of the segments. Since this TC1 is multiplied by the TC1 of the resistors in the expression for the charging period of C_0, the result is an adjustable 2nd-order TC (TC2) compensation [6]. Compared to the biasing circuit used in [6], the TCs of I_{REF} and V_{REF} are now determined by fewer components (one less opamp and one less resistor), which improves their stability. Furthermore, the proposed biasing circuit only uses fixed current mirror ratios, facilitating the use of dynamic element matching (DEM) to mitigate both mismatch and 1/*f* noise.

The implementation of the proposed FLL, together with its timing diagram, is shown in Fig. 2. The biasing circuit employs two PNPs (Q_1, Q_2) with a fixed emitter area ratio N, which are biased at the same emitter current by PMOS current sources. These are driven by a telescopic OTA (gain≈95dB, gm≈20μS), which forces V_{BE} across R_{B2} (185kΩ), and ΔV_{BE} across R_{B1} (6kΩ), respectively. The resulting I_{REF} is then mirrored by two more PMOS current sources, which charge C_0 (5.3pF) and generate V_{REF} (~0.7V at room temperature). To mitigate their offset and 1/f noise, the OTA is chopped ($F_{CHOP}=F_{OUT}/64$), while the four current sources are dynamically matched, with a cycle frequency ($F_{DEM}=F_{OUT}/256$). This choice of frequencies ensures that the DEM and chopping ripples can both be suppressed by a single switched-capacitor (SC) notch filter sampling at $F_{OUT}/256$.

As in [6], the operation of the FLL is divided into three phases with a period of 1μs ($32/F_{OUT}$). During the discharge phase Φ_{DSCH} (250ns), V_C is reset by shorting C_0 (5.3pF) to ground. During the subsequent charging phase Φ_{CH} (500ns), C_0 is charged by an I_{REF} current source to generate V_C. At the end of this phase, the output of the current source V_X is connected to a resistive dumper, which is sized such that $V_X \sim V_C$ to minimizes the voltage step in V_X. In the next integration phase Φ_{INT}, the difference between V_C and V_R is integrated by a two-stage Gm-C loop filter (gm_1=3.5μS, gm_2=120μS, C_{INT}=3pF). Its output drives the VCO, via a ping-pong SC notch filter, towards the steady-state output frequency of 32MHz. The use of a ping-pong filter [8] reduces the associated loop delay, thus improving the loop's stability and settling behavior. As in [6], the VCO consists of a current-starved ring oscillator controlled by a resistor-degenerated PMOS transistor.

Trimming is applied to obtain a stable and accurate F_{OUT} under batch-to-batch and chip-to-chip variations. As shown in Fig. 3(a), to adjust the nominal F_{OUT}, C_0 is trimmed by a CDAC consisting of a coarse MIM cap array (3-bit, 275fF LSB or ~5%) and a fine MOM cap array (8-bit, 1.45fF LSB or ~250ppm). Since the resulting ripple will also be removed by the SC notch filter, the last 3 LSBs were implemented by pulse-width-modulating a unit MOM cap (~11.6fF) at $F_{OUT}/256$. Fig. 3(b) shows the TC1 compensation. A coarse 4-bit trim (~18ppm/°C LSB) is implemented by selecting the tap on R_{B2} through which I_{REF} is injected. Kelvin connections are used to avoid errors due to the IR drops of the switches. A fine 3-bit trim (~3ppm/°C LSB) is implemented by switching part of the lower segment of R_{B2} to ground. A TC2 trim is achieved by adjusting the emitter area ratio and hence ΔV_{BE}, as shown in Fig. 3(c). To minimize their leakage current, the associated switches were realized with high-V_T devices.

The RC frequency reference was fabricated in a standard 0.18μm CMOS process (Fig. 7). Each ceramic packaged chip contains eight identical frequency references, each of which occupies 0.031mm^2 and consumes 89 μA from a 1.8V supply.

Samples from two batches (56 from batch-1 and 56 from batch-2) were characterized over the automotive temperature range (-40°C to 125°C). After an initial batch calibration to determine the optimum TC1/TC2 trim settings, the batch-1 samples achieve a peak inaccuracy of ±1550ppm after a 1-point trim (Fig. 4(a)). Compared to [6], this design exhibits much less temperature hysteresis (Fig. 4(c)). Since PMOS current sources are known to be stress-sensitive [9], this is ascribed to the use of DEM to stabilize all the current ratios used in this design. After one week of accelerated aging at 150°C [5,6], the average frequency error increased to ±2350ppm (Fig. 4(b)). Using the TC1/TC2 codes inherited from batch-1, the batch-2 samples achieve an inaccuracy of ±2900ppm, mainly due to a TC1 shift. After batch calibration, however, their inaccuracy is nearly identical to that of the batch-1 samples. Fig. 5(a) and Fig. 5(b) show the output period jitter and supply sensitivity of the proposed frequency reference, respectively, and Fig. 5(c) shows the start-up acceleration obtained by disabling the notch filter during the first 16 capacitor cycles (~16μs). Thanks to the use of DEM/chopping on all the amplifiers and current sources, the Allan deviation floor is only ~0.4ppm (Fig. 5 (d)).

The performance of the proposed RC frequency reference is summarized and compared to the state-of-the-art in Fig. 6. It achieves the best 1-point trimmed inaccuracy after accelerated aging. It also exhibits negligible hysteresis, and an Allan deviation floor that is at par with the state-of-the-art [1].

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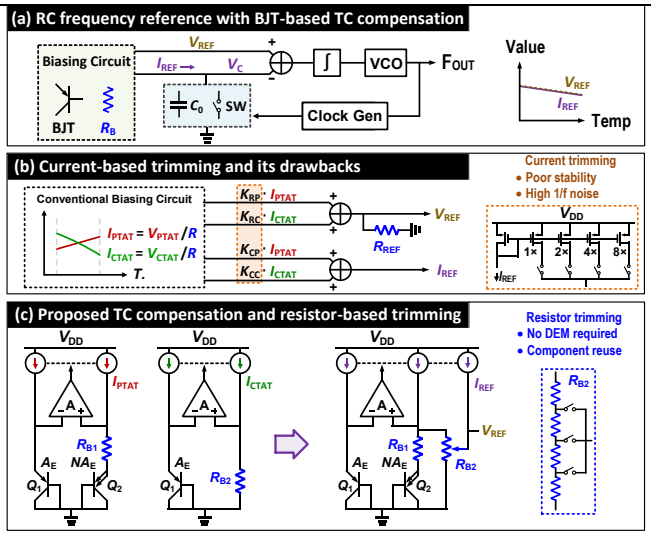


Fig. 1. BJT-compensated RC frequency references: (a) basic structure, (b) current-based TC trimming, (c) the proposed resistor-based TC trimming.

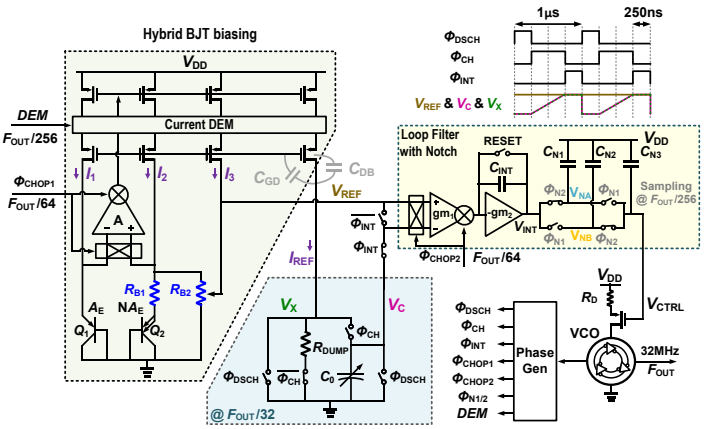


Fig. 2. System block diagram of the proposed frequency reference.

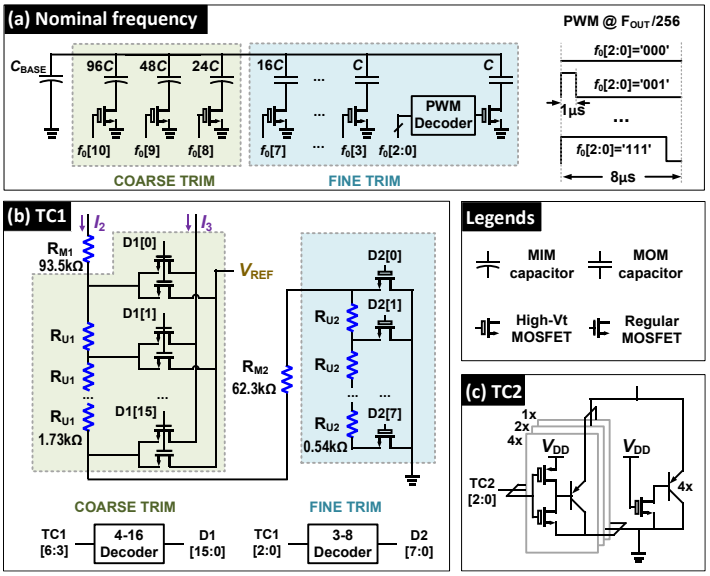


Fig. 3. Trimming circuits for (a) nominal frequency, (b)TC1, (c) TC2.

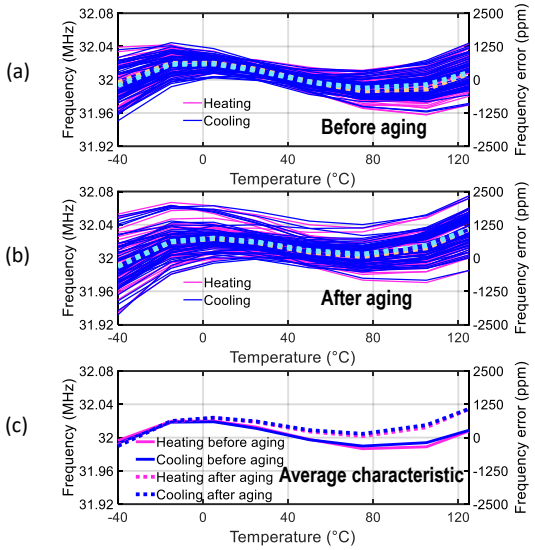


Fig. 4. Frequency error of batch-1 samples: (a) after batch + 1-point calibration, (b) after 168 hours of accelerated aging at 150°C with the same trimming codes. (c) Averaged results.

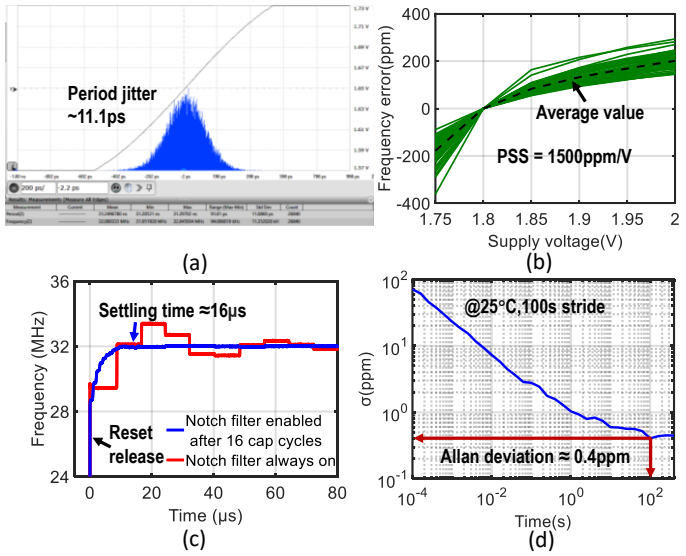


Fig. 5. (a) Measured jitter, (b) power supply sensitivity, (c) start-up response (d) Allan deviation.

	JSSC 2022 [1]	ISSCC 2021 [2]	JSSC 2023 [3]	JSSC 2023 [4]	JSSC 2023 [5]	ISSCC 2024 [6]	This work
Technology	180nm	180nm	65nm	65nm	180nm	180nm	**180nm**
Main resistor	P-Poly	P-Poly	N-Poly	P/N-Poly	P-Poly	N-Diff	**N-Diff**
Compensation device	S-Poly	S-Poly	P+ Diff	VIA Res.	N-Poly	BJT	**BJT**
Area [mm^2]	0.3 [a]	0.14 [a]	0.15	0.22	0.01	0.028	**0.031**
Frequency [Hz]	16M	16M	100M	100M	10M	32M	**32M**
Power [µW]	220	158.4	464	142	85.1	131	**160**
Energy [pJ/cycle]	13.8	9.9	4.64	1.42	8.51	4.1	**5**
Temp. range [°C]	-45~85	-40~85	-40~85	-40~85	-45~125	-40~125	**-40~125**
Trimming points	2+batch	1+batch	2	2	1+batch	2+batch	**1+batch**
Temp. coefficient [ppm/ °C] [b]	1.3	5.2	6.8	12.16	31.5	10.6	**18.8**
Freq. error [ppm]	±90	±400	+450/-400	±760	±2800	±900	**±1550**
Freq. error after aging [ppm]	-	-	-	±1030 [c]	-3200/ -7300 [d]	+1600/ -1400 [d]	**±2350** [d]
Supply range [V]	1.6~2	1.6~2	0.9~1.1	1.1~1.3	1.5~1.8	1.7~2.0	**1.75~2.0**
Supply sensitivity [ppm/V]	1200	2000	1000	1400	9000	3000	**1500**
Jitter [ps]	39.9	10.2	13.3	5.1	41.4	18.7	**11.1**
Allen Deviation Floor [ppm]	0.32	0.35	3	8.1	2.3	18.8	**0.4**
Number of samples	20	18	20	10	112	28	**112** [e]

[a] with high-order polynomial engine [b] box method [c] 500hours @125°C
[d] 168hours @150°C [e] 2 batches, 56 samples per batch

Fig. 6. Performance summary and comparison with state-of-the-art RC-based frequency references.

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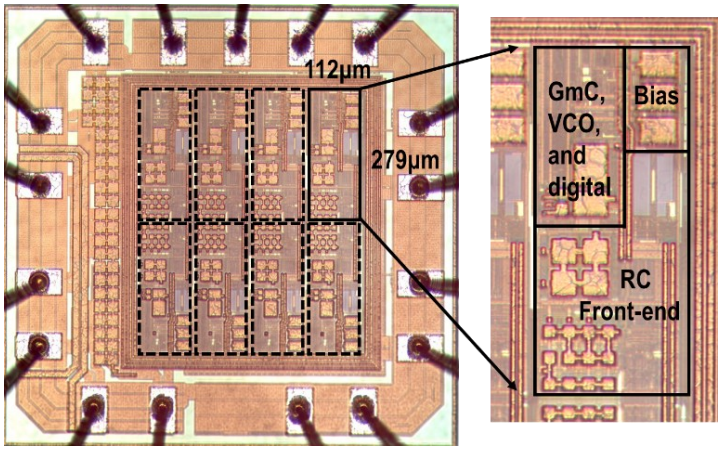


Fig. 7. Chip micrograph with 8 identical FLLs and a zoomed-in view of one FLL.

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