All-Digital I/Q RF-DAC

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Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen

op donderdag 19 juni 2014 om 12.30 uur

door

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Samenstelling promotiecommissie:

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Seyed Morteza Alavi,
All-Digital I/Q RF-DAC,
Ph.D. Thesis Delft University of Technology,
with summary in Dutch.

Keywords: balun, digital power amplifier (DPA), digital predistortion (DPD), digital-to-RF-amplitude converter (DRAC), in-phase/quadrature-phase (I/Q) modulator, MOS switch, RF digital-to-analog converter (RF-DAC), transformer, transmitter (TX).

ISBN 978-94-6259-218-6

Printed in the Netherlands.

To my lovely parents (Mehdi and Noushin)
To my lovely sister (Sara) and her respected family
To my lovely grand parents and my late grand parents
To my lovely uncles, aunts, and my late uncles
To my lovely cousins and their respected families
To all my family members in Iran and around the world
To all my friends in Iran and around the world
To all my teachers in Iran and around the world
And last, but not least, to my lovely wife (Haleh) and her respected family

"Now it is established in the sciences that no knowledge is acquired save through the study of its causes and beginnings, if it has had causes and beginnings; nor completed except by knowledge of its accidents and accompanying essentials."

Avicenna, 980-1037

Contents

Chapter 1

Introduction

Consumer electronic devices such as smartphones, tablets, and laptops, are constantly evaluated against three key criteria: low-cost, high power efficiency, and support of multi-mode/multi-band communication standards such as Wi-Fi including wireless LAN (IEEE 802.11) [1], Bluetooth [2], GNSS[1], second generation (2G) cellular using Global System for Mobile Communications (GSM), third generation (3G) cellular using Wideband Code Division Multiple Access (WCDMA) [3], and fourth generation (4G) cellular using either of WiMAX or 3GPP Long-Term Evolution (LTE) [4,5]. These gadget devices comprise a myriad of integrated circuit (IC) chips to perform an extensive number of distinct functions such as multimedia streaming and gaming as well as supporting the aforementioned communication standards. As an example of contemporary gadget devices, Fig. 1.1 illustrates the mainboard of a smartphone , e.g., the iPhone 5. It consists of an application processor (AP) unit, subscriber identification module (SIM) card slot, NAND flash memory, power management unit, Class-D audio amplifier and, most significantly, a number of radio frequency (RF) transceiver modules that support today's universal communication standards such as GSM, CDMA, Wi-Fi/Bluetooth/FM, GPS, and LTE in combination with its power management unit. Over the past two decades, there have been tremendous efforts to design RF radios that will afford an opportunity to address the low-power, low-cost, and extremely power efficient demands and, yet, they have also employed inventive transceiver architectures.

1.1 The Conventional RF Radio

As depicted in Fig. 1.2(a), a conventional RF transceiver consists of a baseband digital signal processing (DSP) unit, transmitter (TX), and receiver (RX) [6,7]. The transmitter performs

[1]GNSS is the abbreviation of global navigation satellite system. It includes American's GPS, Russian's GLONASS, European Union's Galileo, and China's Beidou navigation system.

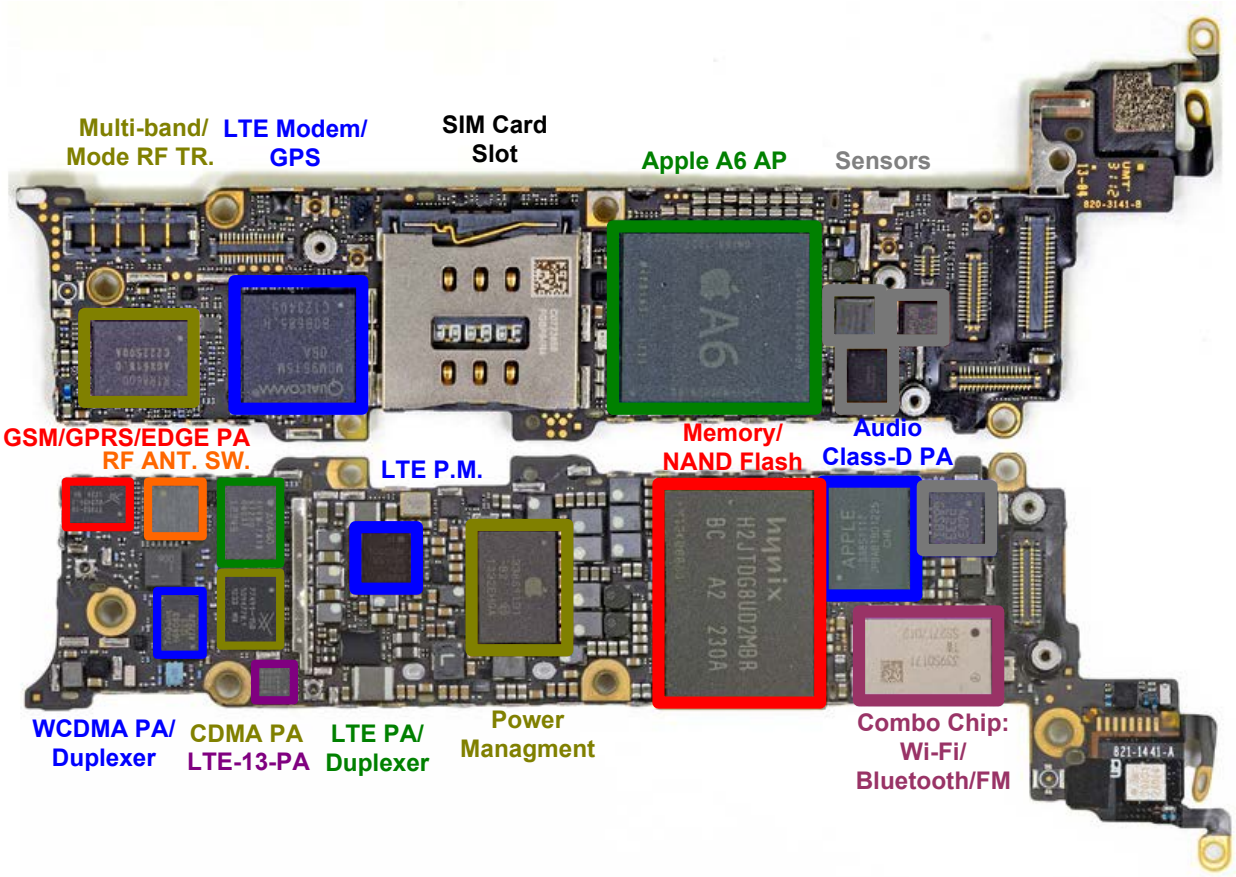

Figure 1.1: The front and rear mainboard of iPhone-5 (Courtesy of Apple Inc.).

in the following manner: The anticipated transmitted information such as voice, video, or digital data like text/images are initially digitally processed, then encoded, and subsequently applied to a digital-to-analog converter (DAC) in order to convert the digital data to their corresponding analog counterparts. Due to the fact that these analog signals comprise unwelcome noise and spectral replicas, the transmitter utilizes low-pass filter (LPF) to reduce those undesirable artifacts. The filtered analog signals are subsequently mixed with an RF local oscillator (LO) utilizing an upconverting mixer and, consequently, upconverted to their designated RF transmit frequency band. Otherwise stated, as illustrated in Fig. 1.2(b), the LO signal translates the low-frequency baseband analog signals with the bandwidth of ω_{BB} into their equivalent high-frequency RF representation. In fact, the LO clock modulates the baseband signal. Thus, the upconverting RF mixer is referred to as an RF modulator. A power amplifier (PA) is succeedingly employed to efficiently boost the RF signal. The subsequent RF amplified signal is then applied to either a duplexer or transmit/receive (TR) switch[2] in order to be delivered to the transmitting antenna.

[2]If the radio uses frequency-division duplexing (FDD), it employs a duplexer. Otherwise, in the time-division duplexing (TDD) communication system, it requires a TR switch.

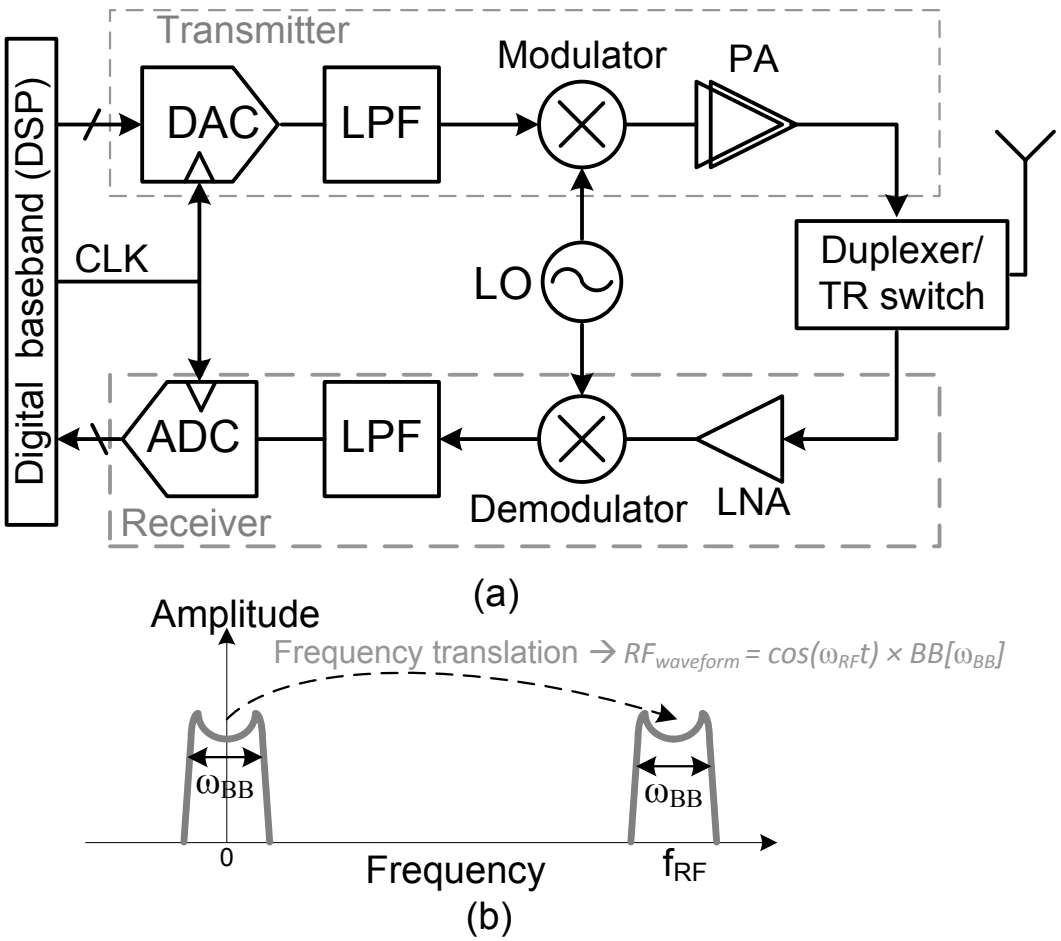

Figure 1.2: (a) A conventional RF transceiver, (b) frequency-domain illustration of modulating the baseband signal.

In the receiver, however, its sensitivity is ameliorated utilizing a low noise amplifier (LNA). The subsequent signal is then down converted to baseband frequency utilizing a down-converter mixer, which is also referred to as a demodulator. By employing a few LPF circuits and then an analog-to-digital converter (ADC), the received signal is digitized for further digital baseband processing operation.

Among transceiver blocks, the RF transmitter is considered to be the most power consuming block of the entire radio, thus being a hindrance for extending the battery lifetime of portable wireless devices. This is due to the fact that it comprises power hungry building blocks such as DAC, the upconverting mixer and, most importantly, the RF PA. For example, in the aforementioned smartphone, as indicated in Fig. 1.1, there are at least 6 different RF-PA modules[3] to support multi-band/ multi mode communication standards.

Consequently, the power amplifiers are the most "power-hungry" building blocks of any portable device due to the high-power RF signal generation that is required by the corre-

[3]1-GSM/GPRS/EDGE; 2-WCDMA; 3-CDMA; 4-LTE; 5-LTE band 13; 6-Wi-Fi/Bluetooth/FM.

Table 1.1: Worldwide Smartphone Sales in 4Q13 (kUnits)

Company	4Q13 Units	4Q13 Market Share (%)	4Q12 Units	4Q12 Market Share (%)
Samsung	83,317.2	29.5	64,496.3	31.1
Apple	50,224.4	17.8	43,457.4	20.9
Huawei	16,057.1	5.7	8,666.4	4.2
Lenovo	12,892.2	4.6	7,904.2	3.8
LG	12,822.9	4.5	8,038.8	3.9
Others	106,937.9	37.9	75,099.3	36.2
Total	282,251.7	100	207,662.4	100

Source: Gartner (February 2014)

sponding communication standard to continuously ensure an impeccable transmitting operation. For example, the corresponding PA in the GSM standard should provide 2 W RF power. Considering a power efficiency as high as 40%, the battery must drain 5 W to generate such RF power which reduces the battery life of the portable device [8–10].

It is worth mentioning that, currently, there are over 6 billion cellular phone users and, in particular, the number of smartphone users is increasing exponentially. Table 1.1 depicts the third quarter of 2012-2013 global smartphone market. As is indicated, smartphone production increases approximately 45% every year. With the progressive number of wireless devices and the relative shortage of bandwidth availability, it will become increasingly difficult to transmit power efficient, undistorted RF signals that do not interfere with other users.

1.2 Motivation

Considering the aforementioned design challenges of the conventional RF transmitter in Section 1.1, intensive research has recently been directed towards the realization of digitally intensive and all-digital RF transmitters that provide high output power with high efficiency while concurrently being highly reconfigurable [11–21]. This was also in response to the incredible advancements of the mainstream Complementary metal-oxide-semiconductor (CMOS) technology in both processing speed and circuit density as well as the relentless coercion to reduce total solution costs through integration of RF, analog, and digital circuitry. Since the digital baseband part of a wireless communication channel has traditionally been implemented in the most advanced CMOS technology available at a given time for mass

production, the need for single-chip CMOS integration has forced immutable changes to the way RF circuits are fundamentally designed. In this low-voltage nanometer-scale CMOS environment, the high-performance RF circuits must exploit the time-domain design paradigm and rely significantly on digital assisted techniques. In other words, contemporary designers are analog thinkers; they tend to cogitate in terms of continuous voltages and currents. On the contrary, digital designers think in terms of discrete-time, discrete-value and, most recently, time-domain operations.

Scientist researchers believe that the development of the concepts behind direct digital or all-digital RF transmitters are in their infancy and innumerable untapped applications and standards are still available. In the current Information Era where more and more data is wirelessly transmitted, it is essential that this information is transmitted in a clear and distortion-free manner while exploiting as little energy as possible. The innovative concept should involve a method and system for digitally generating wideband radio frequency (RF) signals that can be transmitted without the requirement of the current state-of-the-art polar topology which has only been successfully applied to narrowband modulation schemes [14][4]. Otherwise stated, the wireless LAN (WLAN) as well as the currently running wideband modulation standards such as the 3G cellular employing WCDMA and the 4G cellular using 3GPP LTE cannot exploit the current state-of-the-art digital polar RF technology [14] due to the wide bandwidth requirements. Solving the wide bandwidth modulation issues will afford an opportunity to introduce a universal all-digital RF transmitter. It will decrease the cost of production for new and existing IC customers and also will benefit the end users. Concurrently, it will reduce the IC area which signifies increased space for other applications. It will also lower power consumption, thereby resulting in a longer battery lifetime. To summarize, the main advantages of utilizing the new direct digital transmitter architecture are:

1. The circuit integration level will be higher, thus the wireless portable devices can be smaller, lighter, and have nicer designs through smaller form factors. From a technical perspective, employing a direct digital transmitter eliminates the bulky DAC, analog LPFs, and analog mixers;

2. Due to the elimination of several power-hungry analog components, the power efficiency of the RF transmitter will be higher, therefore, it subsequently increases battery life or leads to smaller battery size.

3. The new topology can afford more sophisticated reconfigurability in order to handle various standards and even modulation methods that have yet to be invented.

[4] As will be explained in the following chapters, although recent publications have indicated that polar architecture can manage up to 20 MHz [18–21], the utilized polar structure is still very complicated. Moreover, it could not handle wider band signals such as 802.11n/ac with the modulation bandwidth of 40/160 MHz.

1.3 The Thesis Objectives

Based on the previous explanations in Sections 1.1 and 1.2, the underlying objective of this dissertation is, therefore, to implement an innovative, fully-integrated[5], all-digital RF transmitter which should be power-efficient and, yet, must manage a wideband complex-modulated signal in order to support multi-mode/multi-band communication standards. Moreover, it should generate adequate RF power, minimal out-of-band spectra while the generated far-out noise of the all-digital RF transmitter must be low enough that is does not desensitize the companion receiver circuit blocks. Due to the zero-order-hold operation in the digital-to-RF interface, the direct digital RF transmitter, however, inherently creates spectral replicas at multiples of the baseband upsampling frequency away from the carrier frequency. In contrast, in the conventional analog RF transmitter, the spectral replicas have been eliminated due to utilizing the analog continuous-time filters directly following the DAC (see Fig. 1.2(a)). Moreover, the quantization noise induced by the limited effective baseband code resolution of the digital transmitter, worsens out-of-band spectra. This anomaly also does not exist in the analog counterparts. To gain more insight into these phenomena, the following subsection will be conducive.

1.3.1 System Simulation of WCDMA Baseband Data

As discussed previously, although the direct digital transmitter does not necessitate the bulky analog LPF, it requires another type of filtering based on a discrete-time digital approach. Consider a WCDMA baseband signal in which its data rate varies between 7.5 kb/s to 960 kb/s. Fig. 1.3 illustrates the filtering process whereby the spread spectrum filter is first applied to an in-phase digital baseband (I_{BB}) and a quadrature-phase digital baseband (Q_{BB}) samples at a chip rate of 3.84 MHz. Subsequently, in order to constrain the occupied RF band, the resulting signals get pulse-shaped. The pulse-shaped oversampling rate is usually 16; therefore, the baseband data rate will increase to 61.44 Mb/s. If these samples (I_{PS} and Q_{PS} shown in Fig. 1.3) are applied directly to the mixer of an all-digital transmitter, then the resulting signal will produce spectral images at every 61.44 MHz from the up-converted spectrum which are very difficult to filter out. Therefore, it necessitates interpolation of these signals to higher data rates. Moreover, with the use of upsampling, the quantization noise spreads over a wider operational frequency range which also improves the dynamic range or resolution. With the employment of three cascaded finite impulse response (FIR) filter-based interpolators, each with an upsampling factor of $L = 2$, the resulting signal sampling rate is 535 MHz. Consequently, the images repeat every 535 MHz from the desired spectrum, which are now easier to filter out. It should be mentioned that,

[5]As will be demonstrated in Chapter 4, the first prototype is exploited an on-chip, digitally-controlled oscillator (DCO) while the second chip in Chapter 7 just utilizes an external local oscillator (LO).

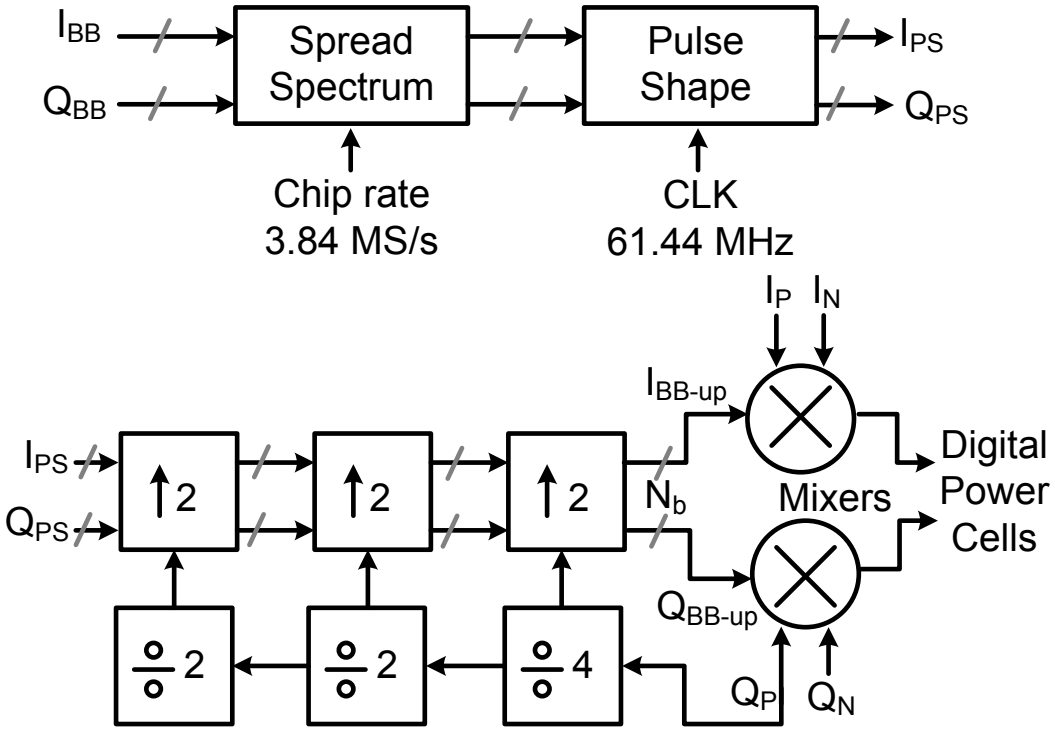

Figure 1.3: Upsampling and interpolation process of WCDMA baseband signals.

as depicted in Fig. 1.3, the FIR clocks are synchronized to the carrier clocks using clock frequency dividers which are a divide-by-4, and consecutive divide-by-2.

The simulation results of Fig. 1.3 are depicted in Fig. 1.4, which also indicates that, by increasing the resolution (N_b) of the all-digital transmitter, the quantization noise is decreased and, thus, the dynamic range of the WCDMA signal improves. Each additional bit corresponds to a 6 dB improvement in the dynamic range. The far-out spectrum of Fig. 1.4 demonstrates the sampling image replica of the original signal which is located 535 MHz away. This reveals that the baseband signals[6] are ultimately upsampled by a factor of 128 (16×8) to spread the quantization noise, thus lowering its spectral density.

In conclusion, an all-digital RF transmitter at the equal RF output power level compared to its analog counterpart, creates more noisy out-of-band spectrum.

1.3.2 Some Important Figures-of-Merit in RF Transmitters

The RF transmitter can be evaluated by employing a number of figures-of-merit and they will be discussed as follows. First, the drain efficiency of the transmitter is defined as:

$$\eta_{drain} = \frac{P_{RFout}}{P_{DC-PA}} = \frac{V_{RFout} \times I_{RFout}}{V_{DC-PA} \times I_{DC-PA}} \tag{1.1}$$

[6]Note that the WCDMA chip rate is 3.84 MS/s.

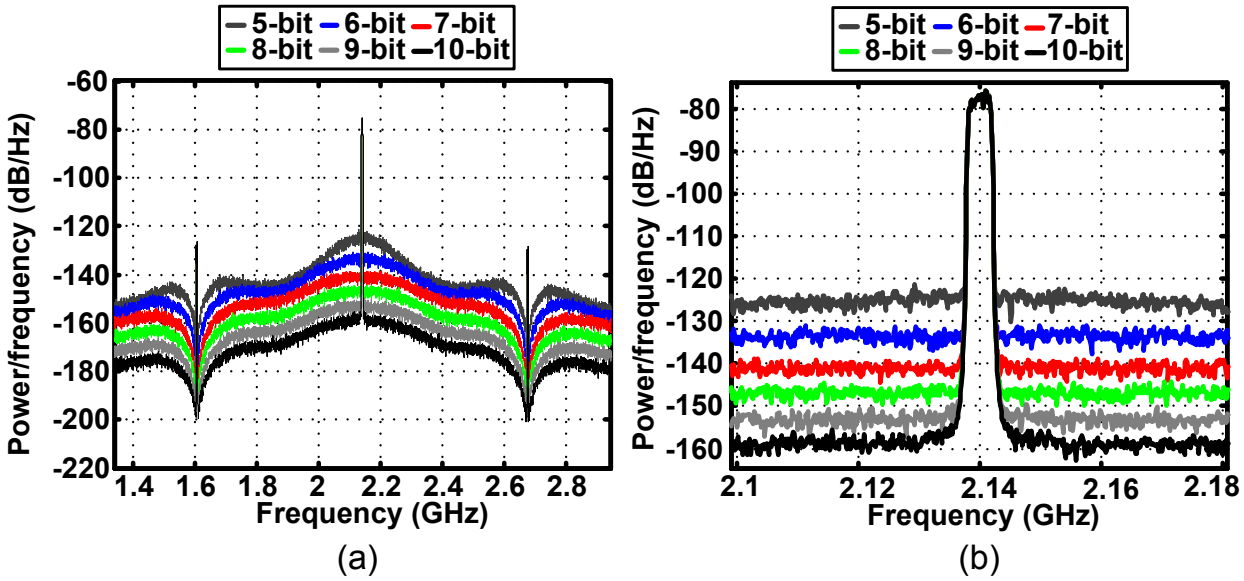

Figure 1.4: Simulated WCDMA RF output spectrum for different resolutions of all-digital transmitter: (a) far-out; (b) close-in range.

where P_{RFout} is the generated RF output power at the 50 Ω load, and P_{DC-PA} is the corresponding direct current (DC) power consumption of the PA. Moreover, V_{RFout} and I_{RFout} are root mean square (RMS) output voltage and current, respectively. Second, the system efficiency of the transmitter is defined as:

$$\eta_{system} = \frac{P_{RFout}}{P_{DC-Total}} = \frac{P_{RFout}}{P_{DC-PA} + P_{DC-Driver}} \tag{1.2}$$

where $P_{DC-Total}$ is the related DC power consumption of the entire RF transmitter which includes the DC power consumption of PA and the upconverting clock driver circuit. The RF transmitter dynamic performance is subsequently divided into in-band performance and out-of-band spectral purity. The error vector magnitude (EVM) is conventionally utilized for the evaluation of the in-band performance and calculates the difference between the symbol sampling points of the measured and reference waveforms. The EVM result is defined as the square root of the ratio of the mean error vector power to the mean reference power and is expressed as a percentage [3]:

$$EVM_{RMS} = \frac{\sqrt{\sum_{i=1}^{N_{pt}} \frac{1}{N_{itr}} \times (IQ_{ideal}(i) - IQ_{real}(i))^2}}{\sqrt{\sum_{i=1}^{N_{pt}} \frac{1}{N_{itr}} \times (IQ_{ideal}(i))^2}} \tag{1.3}$$

where N_{itr} is the number of iterations for each point, and N_{pt} is the number of constellation points. Moreover, $IQ_{ideal}(i)$ and $IQ_{real}(i)$ are "i_{th}" ideal (reference) and real (measured) constellation points, respectively. Additionally, the out-of-band spectral purity can be evaluated as an adjacent channel power ratio (ACPR)[7] and far-out noise performance at the corresponding receiver frequency band of interest. ACPR is utilized to measure the nonlinear distortion in the transmitted signal. Moreover, ACPR in combination with the modulation scheme determines the maximum allowable nonlinearity of the related RF transmitter. ACPR is defined as follows [22, 23]:

$$ACPR_{adj} = \frac{P_{adj}}{P_{main}} \tag{1.4}$$

where P_{adj} is the total adjacent right/left channel and P_{main} is the total RF power within the main transmit channel. Note that, instead of ACPR, the third order intermodulation product (IM_3) can also be employed [22, 24]. Furthermore, as discussed previously, the far-out noise performance of the RF transmitter strongly depends on quantization noise and baseband up-sampling rate. It is noteworthy that the far-out noise at the receiver frequency band of interest[8] must be less than its related thermal noise of -173.83 dBm/Hz[9]. Thus, as will be explained in more detail in Chapter 5, the baseband code resolution as well as the baseband upsampling rate should be suitably selected so as not to deteriorate the out-of-channel spectrum as well as the far-out noise performance.

1.4 Thesis Outline

This dissertation is organized as follows:

In Chapter 2, four types of RF transmitter architectures are briefly described. The analog Cartesian modulators are the most simple and most widely exploited RF transmitters. They have subsequently been replaced by analog polar counterparts to address their poor power efficiency and noise performance. However, in the analog polar RF transmitters, their related amplitude and phase signals must be aligned, or spectral regrowth is inevitable. Utilizing digitally intensive polar RF transmitters mitigates the latter alignment issue. Nonetheless, polar transmitters suffer from an additional issue related to its nonlinear conversion of in-phase and quadrature signals into the amplitude and phase representation. Consequently, the polar RF transmitters are unable to manage the substantial baseband bandwidth of the most stringent communication standards. However, reusing Cartesian modulators based on

[7] Sometimes ACPR is expressed as adjacent channel leakage ratio (ACLR).

[8] This condition is applicable in full-duplex systems.

[9] This noise power level is obtained assuming conjugate matching at the input of the receiver, 50 Ω input load and temperature at $27°C$ [24, 25]. Note that, the noise figure (NF) and signal-to-noise ratio (SNR) of the receiver should also be considered which will be discussed in more detail in Chapter 5.

digitally intensive implementation appears to be a reasonable approach for managing this issue.

In Chapter 3, the novel all-digital I/Q RF modulator is described. This concept suggests that utilizing an upconverting RF clock with a 25% duty cycle ensures the orthogonal summation of I_{path} and Q_{path}. It is clarified that electric summing of I and Q digital unit array switches are the most appropriate I/Q orthogonal summation approach. Moreover, in order to cover all four quadrants of the constellation diagram, differential quadrature upconverting RF clocks should be used.

In Chapter 4, a novel 2×3-bit all-digital I/Q (i.e., Cartesian) RF transmit modulator is implemented. The radio-frequency digital-to-analog converter (RF-DAC) functions according to the concept of orthogonal summing and it is based on a time-division duplexing (TDD) manner of an orthogonal I/Q addition whereby a simple and compact design featuring high-output power, power-efficient and low-EVM is realized.

In Chapter 5, the system design considerations of the proposed high-resolution, wideband all-digital I/Q RF-DAC are discussed.

In Chapter 6, the design procedure of a 12-bit digital power amplifier together with a class-E-based power combining network are discussed.

In Chapter 7, the implemented wideband, 2×13-bit I/Q RF-DAC-based all-digital modulator realized in 65-nm CMOS is presented. The 12-bit DRAC is implemented by employing the segmentation approach which consists of 256 MSB bits and 16 LSB thermometer unit cells. The layout arrangement of the DRAC unit cell proves to be very crucial. The LO leakage and I/Q image rejection technique as well as two DPD memoryless techniques of AM-AM/AM-PM and constellation mapping are introduced which will be employed extensively during the measurement process.

In Chapter 8, the high-resolution wideband 2×13-bit all-digital I/Q transmitter will be measured. First, the chip is tested in continuous-wave mode operation. The RF-DAC chip generates more than 21 dBm RF output power within a frequency range of 1.36 to 2.51 GHz. The peak RF output power, overall system, and drain energy efficiencies of the modulator are 22.8 dBm, 34%, and 42%, respectively. The RF-DAC could be linearized using the DPD lookup table. Its linearity is examined using single-carrier 4/16/64/256/1024-QAM as well as multi-carrier 256-QAM OFDM baseband signals while their related modulation bandwidth is as high as 154 MHz. Moreover, the constellation-mapping DPD is applied to the RF-DAC thereby improving linearity by more than 19 dB.

In Chapter 9, the dissertation is concluded, and sensible suggestions are presented for future developments.

Chapter 2

Analog Versus Digital RF Transmitters

This chapter gives an overview of the various existing types of radio frequency integrated circuit transmitter (RFIC-TX) architectures that are required to determine their advantages and disadvantages in order to develop an innovative approach to devise a fully integrated all-digital RF transmitter. Though this has already been explained in many ways in existing literature [24–26], it is still beneficial to reiterate their distinctions. Section 2.1 discusses analog-intensive Cartesian as well as polar RF transmitters. In Section 2.2, the need for digital-intensive RF transmitters is examined. Section 2.3 explains the new paradigm of RF transmitter design utilizing the nano-scale CMOS process technology. In Section 2.4, an all-digital polar transmitter is explored while Section 2.5 unveils all-digital Cartesian transmitters. Finally, the conclusion of the chapter is drawn in Section 2.6.

2.1 Analog-Intensive RF Transmitters

Beginning around the 1990s, virtually all RFIC-TXs have been analog intensive and based on an architecture similar to that depicted in Fig. 2.1. At the transmitter back-end, the baseband user information symbols become pulse-shaped to obtain two orthogonal components of complex-number digital samples, i.e., in-phase (I) and quadrature-phase (Q) that are constrained to the allocated frequency channel.

They are then converted into an analog continuous-time domain through a DAC with a typical zero-order-hold (ZOH) function. The LPF following the DAC subsequently filters out the switching harmonics. Thus obtained analog baseband signal is then upconverted (frequency translated) into RF through a quadrature modulator. The resulting (typically external) PA increases the RF power level at the antenna to that of what is required by

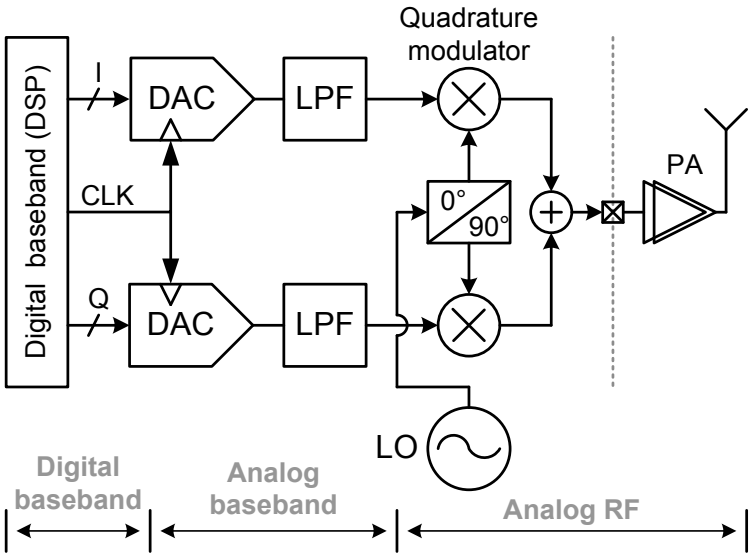

Figure 2.1: Traditional analog-intensive Cartesian (I/Q) RF transmitter.

the wireless standard, which could be as high as 2 W for a GSM handset. The frequency synthesizer-based LO performs the frequency translation. It is typically realized as a charge-pump phase-locked loop (PLL) with $\Sigma\Delta$ dithering of the divider modulus to realize the fractional-N frequency division ratio. The complete architecture and monolithic circuit design techniques of the conventional transmitter exhibited in Fig. 2.1 have been described extensively in an innumerable amount of literature, particularly in the latest editions of text books [24, 25]. These architectures have been successfully employed in integrated CMOS transmitters [27–34] for over a decade (since the late 1990s). Unfortunately, their beneficial lifetime is gradually coming to an end [35] to make room for analog polar and more digitally-intensive architectures. In summary, due to linear summation of I and Q signal paths, this architecture can manage large modulation bandwidth. On the other hand, it comprises power-hungry as well as bulky components which make this transmitter deficient.

An alternative to the I/Q topology of Fig. 2.1 is the polar realization exhibited in Fig. 2.2 in which the two uncorrelated, i.e., orthogonal, components (alternative to the I and Q components) are amplitude ρ and phase θ:

$$\begin{aligned} \rho &= \sqrt{I^2+Q^2} \\ \theta &= \tan^{-1}\left(\frac{Q}{I}\right) \end{aligned} \tag{2.1}$$

The complex-envelope signal is $S = \rho \exp(\mathrm{j}\theta)$. The phase modulation could be performed by a direct or indirect frequency modulation of a PLL. The amplitude modulation could be performed by a low drop-out (LDO) voltage regulator modulating the V_{DD} supply of a high-efficiency switched-mode PA, such as a class-E PA. The analog polar TX architecture is a more recent development that addresses the inherent poor power efficiency and noise issues

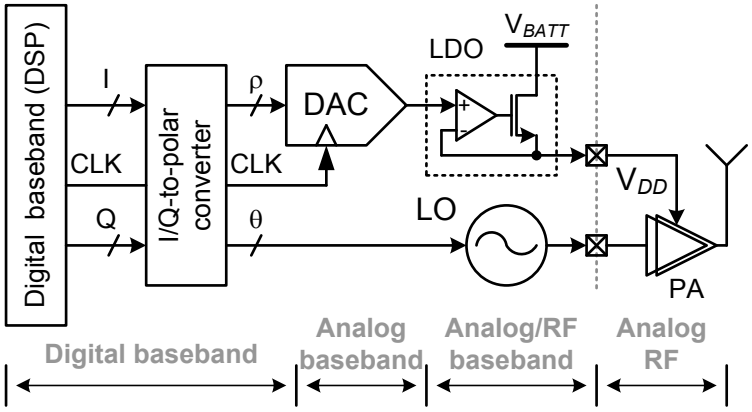

Figure 2.2: Traditional analog-intensive polar RF transmitter.

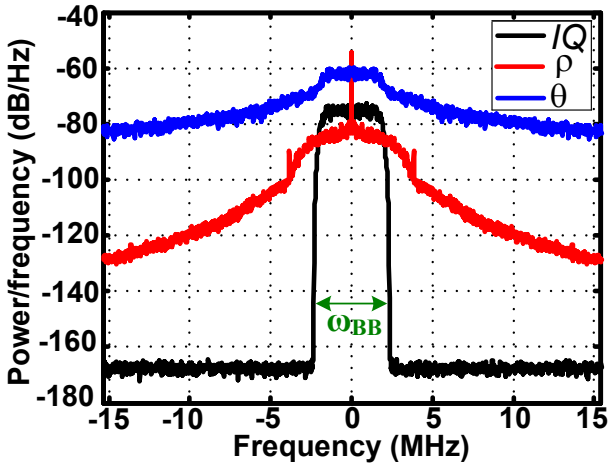

Figure 2.3: Polar modulator bandwidth expansion of the WCDMA signal.

of the I/Q architecture. Notwithstanding these benefits, polar topologies exhibit certain serious disadvantages:

1. Their phase and amplitude paths exploit heterogeneous circuits whose delays must be accurately aligned to avoid spectral distortion at the final recombining stage, yielding spectral re-growth;

2. The required instantaneous bandwidth is significantly larger than in the I/Q approach. Otherwise stated, the composite modulator bandwidth is typically limited due to the bandwidth constrains in the practical DC-to-DC switchers or linear converters.

The latter aspect can be understood by examining the nonlinear operations that the amplitude ρ and phase θ experience during conversion from the I/Q representation (2.1).The resulting signal bandwidth expansion can be observed in Fig. 2.3. This figure compares the baseband bandwidth (ω_{BB}) expansion of an example WCDMA I/Q modulator with its polar

counterpart. Note that the bandwidth expansion is due to the fact that ρ and θ enhance the even ($2\omega_{BB}$, $4\omega_{BB}$, $6\omega_{BB}$, ...) and odd ($3\omega_{BB}$, $5\omega_{BB}$, $7\omega_{BB}$, ...) harmonics of baseband signal, respectively[1].

Over the past several years, such analog-intensive polar transmitters (both small-signal, i.e., at the transceiver IC level, and large signal, i.e., encompassing PA) have been touted for their reconfigurability, implementational, and performance benefits more so than their traditional Cartesian counterparts that are based on an I/Q upconversion mixer. A number of recent publications have demonstrated their superiority with highly-integrated silicon realizations [36–42] but only for the *narrowband* (200 kHz allocated bandwidth) modulation standard, Enhanced Data rates for GSM Evolution (EDGE), of the 2G cellular. The polar architecture migration to *wideband* modulation standards, such as 3G (WCDMA – allocated bandwidth of 5 MHz), 4G (3GPP LTE, WiMAX – allocated bandwidth of up to 20 MHz), and other evolving wideband wireless standards (e.g., 802.11n/ac) continues to be a daunting task and, thus far, there has only been one very recent silicon demonstrator that produces low efficiency and low RF output power (3 dBm) discussed in the open literature [43]. The effort, however, appears to continue with another theoretical proposal of the polar topology for WCDMA [44] and one 90-nm CMOS demonstration of the RF front-end block components of the WCDMA digital polar transmitter [45].

2.2 Digitally-Intensive RF Transmitters

As mentioned above, the digital approach to design RF circuits and architectures is taking over in industry. The primary contributors to this sea-like transformation are the ever-improving cost advantages and processing capabilities of the CMOS technology that have been occurring at regular intervals at the pace according to the so-called Moore's law. Basically, with every CMOS process technology advancement node (i.e., from 90-nm to 65-nm, then to 40-nm, and then to 28-nm, and so on) occurring every 18–24 months, the digital gate density, being a measure of the digital processing capability, doubles (i.e., gate area scaling factor of 0.5×). Simultaneously, the basic gate delay, being a measure of the digital processing speed, improves linearly (i.e., gate delay scaling factor of 0.7×). Likewise, the cost of fabricated silicon per unit area remains approximately the same at its high-volume production maturity stage. Indeed, over the last decade, the cost of silicon charged by IC fabs has remained constant. The main implication of this is that a cost of a given digital function, such as a GSM detector or a digital audio decoder, can be cut in half every 18-24 months when transitioned to an upgraded CMOS technology. At the same time, the circuits consume proportionately less power and are faster [26].

[1]Note that according to eq. (2.1) the envelope signal is an even function (square function) which entails the bandwidth expansion due to even harmonics. On the other hand, the phase signal is an odd function (arctangent function) which causes the bandwidth expansion because of odd harmonics.

Unfortunately, these astonishing benefits of digital scaling are not shared by traditional RF circuits. Additionally, the strict application of the Fig. 2.1 and Fig. 2.2 architectures to the advanced CMOS process node might actually result in a larger silicon area, inadequate RF performance, and higher consumed power. The constant scaling of the CMOS technology has had an unfortunate effect on the linear capabilities of analog transistors. To maintain reliability of scaled-down MOS devices, the V_{DD} supply voltage continues to decrease, while the threshold voltage V_t remains almost constant (to maintain the low level of leakage current). This negatively affects the available voltage margin when the transistors are intended to operate as current sources. Moreover, the implant pockets that were added for the benefit of digital operation have drastically degraded the MOS channel dynamic resistance r_{ds}, thus severely reducing the quality of MOS current sources and the maximum available voltage self-gain

$$A_{v-intrinsic} = g_m \cdot r_{ds} \tag{2.2}$$

where g_m is the transconductance gain of a transistor. Furthermore, due to the thin gate dielectric becoming increasingly thinner, large high-density capacitors realized as MOS switches are becoming unacceptably leaky. This prevents an efficient implementation of low-frequency baseband filters and charge pump PLL loop filters.

2.3 New Paradigm of RF Design in Nanometer-Scale CMOS

An early attempt at designing RF circuits in advanced CMOS has revealed a new paradigm:

> In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals [11].

On a pragmatic level, this indicates that a successful design approach in this environment would exploit this paradigm by emphasizing the following:

1. Fast switching characteristics or high f_T (20 ps and 250 GHz in 40-nm CMOS process, respectively) of MOS transistors: high-speed clocks and/or fine control of timing transitions;
2. High density of digital logic (1 Mgates/mm^2) and also static random access memory (4 Mb/mm^2) results in extremely inexpensive digital functions and assistant software;
3. Ultra-low equivalent power-dissipation capacitance C_{pd} of digital gates leading to both low switching power consumption

$$P_T = f \cdot C_{pd} \cdot V_{DD}^2 \tag{2.3}$$

as well as potentially low coupling power into sensitive analog blocks;

4. Small device geometries and precise device matching made possible by the fine lithography to create high-quality analog and RF data converters;

while avoiding the following:

1. Biasing currents that are commonly exploited in analog designs;
2. Reliance on voltage resolution with continuously decreasing supply voltages and increasing noise and interferer levels;
3. nonstandard devices that are not required for memory and digital circuits, which constitute the majority of the silicon die area.

Despite the early misconceptions that the digitalization of RF would somehow produce more phase noise, spurs, and distortion, the resulting digitally-intensive architecture is inclined to be, overall, more robust by actually producing lower phase noise and spurious degradation of the transmitter chain and a lower noise figure of the receiver chain in face of millions of active logic gates on the same silicon die, as repeatedly substantiated in subsequent publications [13,14,17,19,46–49]. Additionally, the new digital TX architecture would be highly reconfigurable with analog blocks that are controlled by software to guarantee the best achievable performance and parametric yield. An additional benefit would be an effortless migration from one process node to the next without significant modifications.

2.4 All-Digital Polar Transmitter

A transmitter architecture that is amenable to the digital nanoscale CMOS technology is depicted in Fig. 2.4 [13,14]. This digital polar transmitter has found its way into commercial products. Note that, this digital-to-RF architectural transformation is influenced by the ever-improving cost advantages and process capabilities of CMOS technology, and various successful implementations have been brought to fruition, e.g., [14]. The work of Chowdhury *et al.* [19] and, most recently, Lu *et al.* [21,49] proposed wideband polar modulators, which achieve high output power and high efficiency.

The LO in Fig. 2.4 is realized as an all-digital PLL (ADPLL) that produces a phase or frequency modulated digital clock carrier employing the two-point digital modulation scheme. The clock is fed into a digital-to-RF-amplitude converter (DRAC) that produces an RF output of which the envelope is substantially proportional to the amplitude control word (ACW) or ρ. Hence, the architecture is termed as a digital polar TX.

The DRAC is realized as an all-digital RF power generation circuit as illustrated in Fig. 2.5(a) [50]. It is also referred to as a digitally controlled power amplifier (DPA). Note that compared to the traditional power amplifier which amplifies the analog/RF input signal,

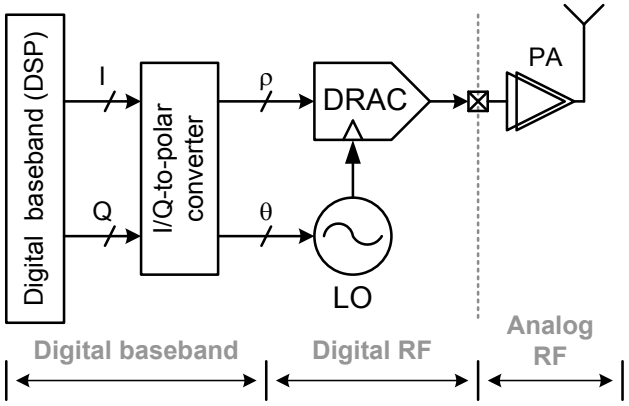

Figure 2.4: All-digital polar transmitter.

in this context, the input signal of the DPA is an internal digital clock, therefore, measuring the *amplification* gain of the DPA seems a bit problematic. The DRAC has proven its exploitation by the amplitude modulation in more advanced modulation schemes, such as the extended data rate (EDR) mode of Bluetooth, EDGE and WCDMA.

The DRAC operates as a near-class-E RF PA and is driven by the square wave output of a digitally-controlled oscillator (DCO) in the ADPLL. The rise-/fall-time of digital signals, including clocks, is typically 40–60 ps in 65 nm low-power CMOS process, which makes the trapezoidal shape almost square for cellular band signals. A large number of core NMOS transistors are employed as on/off switches, each with a certain conductance $1/R$, and are followed by a matching network that interfaces with an antenna or an external PA. The number of active switches, and thus the total conductance $\sum(1/R)$, is digitally controlled and establishes the instantaneous amplitude of the output RF envelope. The RF output power is incited by coherently moving the resonating energy through the LC tank between the load and the switches. The supply V_{DD} replenishes the energy lost to the load and internally. The RF amplitude is contingent upon the relationship between the total switch conductance and the conductance of the matching network.

The class-E PA operation is attempted in order to achieve the maximum output power (all the switches are active), where the highest achievable efficiency is of the utmost importance. Note that there could be different methods of conversions from digital to RF amplitude as well as classes of operation. For example, class-D PA [18, 52] would utilize two switching devices operating complementary and connected to the supply/ground and the matching network. Fine amplitude resolution is achieved through high-speed $\Sigma\Delta$ transistor switch dithering. The timing diagram of Fig. 2.5(a) [50] assumes that the data changes with every RF clock cycle, which is reasonable considering the high-speed dithering. In practice, the integer ACW signals would change every certain number of DCO cycles. Despite the high speed of digital logic operation, the overall power consumption of the transmitter architecture is reasonably low.

As previously indicated, the significant advantage of the polar architecture is its high

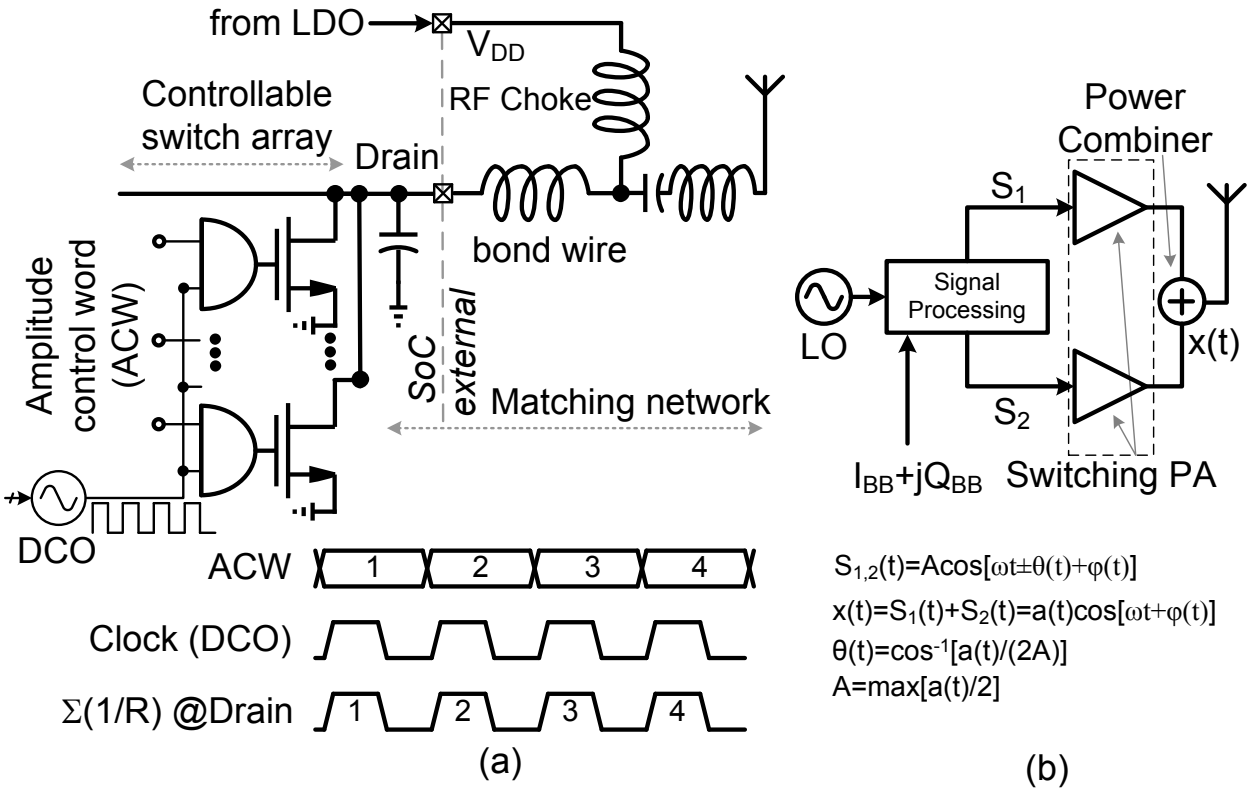

Figure 2.5: (a) DRAC in digital polar TX [50]. (b) Digital outphasing TX [51].

power efficiency. However, due to the nonlinear signal processing, there is a significant bandwidth expansion that makes it unusable for very wideband signals. This has prompted researchers to consider alternative architectures. The outphasing architecture [53], which avoids the amplitude modulation at the component level, is not only highly efficient at maximum RF output power, but also efficiently operates at back-off power levels. Moreover, a few research groups have recently demonstrated various digital implementations [51,54–56]. Depicted in Fig. 2.5(b), the digital transmitter in [51] produces 26 dBm peak RF power while its drain efficiency is 35 %. However, the outphasing architecture still experiences bandwidth expansion issues due to the nonlinear signal transformation which might limit its usefulness for very wideband signals.

2.5 All-Digital I/Q Transmitter

As mentioned in 2.1, due to the bandwidth expansion of ρ and θ, which could be as much as 10× the original I/Q signal bandwidth, it might be problematic to apply the digital polar TX architecture to the wideband modulation, especially the most recent 3GPP LTE cellular and 802.11.n/ac wireless connectivity standards. The required bandwidths would exploit approximately hundreds of MHz. Even though [17] introduced a wideband digital polar PA,

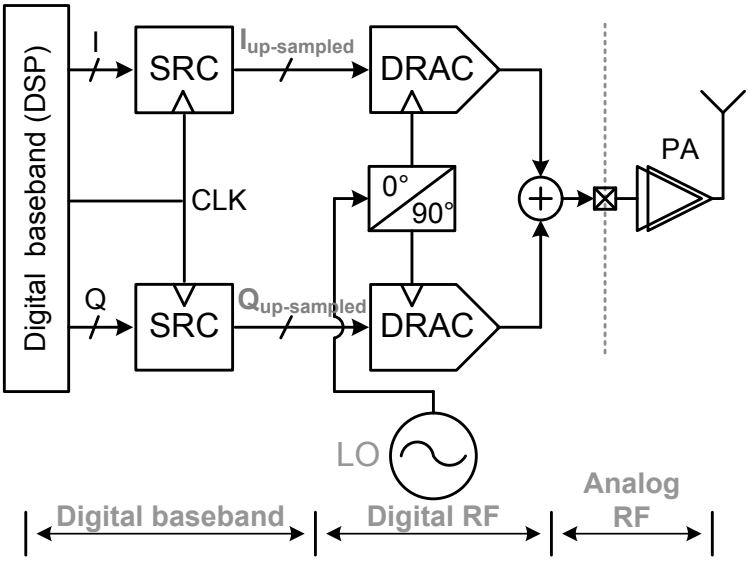

Figure 2.6: Digital I/Q TX.

the efficiency was inadequate. In addition, [19, 48, 49] proposed wideband polar modulators, which achieve high output power and high efficiency. Nonetheless, they require a complicated baseband processing of ρ and θ signals. Consequently, the digitally intensive I/Q architecture has been introduced [16, 57–66] to maintain the digital RF approach while addressing the bandwidth expansion issue of the polar topology. A typical architecture is illustrated in Fig. 2.6. Compared to Fig. 2.1, a new optional circuit,sample-rate converter (SRC), is included to convert the lower-rate baseband I/Q signal (processed at integer multiple of the symbol rate) into a much higher rate that is necessary to spread the quantization noise, thus lowering its spectral density. Note that this optional SRC circuit could also be incorporated in the digital polar TX of Fig. 2.4 as a component of the I/Q-to-polar converter.

The operation of the digital I/Q modulator is as follows. The I and Q digital samples drive their respected DRAC converters that produce two RF signal components in which their amplitudes are ideally proportional to the respective I/Q digital inputs. The two amplitude-modulated RF components are subsequently combined to produce the desired composite RF output. The output is then either directly transmitted to the antenna or through a high-performance power amplifier. Note that, the phase of the subsequent RF signal is implicitly the result of the arctangent function of "DRAC Q RF output voltage" to "DRAC I RF output voltage". This is due to the fact that the phase of the DRAC Q output is 90^o delayed with respect to that of the I output.

This digital I/Q architecture does not appear to compare favorably with the polar topology of Fig. 2.4. The digital I/Q architecture seems increasingly complex with extra circuitry contributing noise and creating signal distortion. The frequency modulation of the LO in Fig. 2.6 could be satisfactorily accomplished through the familiar two-point modulation scheme of the ADPLL. The phase component is thus under the closed-loop feedback, which

reduces the noise and distortion content falling within the ADPLL loop bandwidth. Closing the loop around the I/Q modulator RF output is typically much more difficult. The traditional issues of the timing misalignment in the analog polar architecture is no longer an issue with the digital approach. The digital discrete-time operation is, by construct, clock-cycle accurate while the modern technology can clearly support sampling rates even at the GHz range, as well as ultra-fast settling of the DPA conversion circuits (with the speed governed by f_T). Consequently, the circuits of digital architectures can ensure fine time accuracy which is constant and not subject to processes and environmental changes. The DRAC could be implemented as a digitally-controlled RF-modulated current source [16, 58]. In this manner, the addition of the two DRAC output components could be as uncomplicated as connecting them electrically. For the I/Q signal orthogonality to maintain, these two current sources must be ideal such that one signal path output does not influence the operation of the other. This indicates the need to resort to current source impedance boost techniques, such as cascoding. Unfortunately, stacking of the MOS transistors in a cascode structure as a current source is difficult in the modern low-voltage technologies and further produces an excessive amount of leakage and noise. In order to mitigate the aforementioned issues, consequently, there is a need for a digital TX architecture that is capable of supporting advanced wideband wireless modulation standards but which also avoids the intrinsic bandwidth expansion issues of the polar topology and the severe noise issues of the conventional digital I/Q architectures.

2.6 Conclusion

Four types of RF transmitter architectures are briefly described. The analog I/Q modulators are the most straightforward and widely employed RF transmitters. They are later replaced by analog polar counterparts to address their poor power efficiency and noise performance. On the other hand, in the analog polar RF transmitters, their related amplitude and phase signals must be aligned or spectral regrowth is inevitable. Utilizing digital intensive polar RF transmitters mitigates the latter alignment issue. Nonetheless, polar transmitters suffer from an additional issue that is related to their nonlinear conversion of in-phase and quadrature-phase signals into the amplitude and phase representation. Therefore, the polar RF transmitters are not able to manage very large baseband bandwidth of the most stringent communication standards, therefore, reusing I/Q modulators based on digitally intensive implementation appears to be a reasonable approach to resolve this issue. The digital I/Q RF transmitters, however, suffer again from inadequate power efficiency. Moreover, the combination of in-phase and quadrature-phase paths must be orthogonal to produce an undistorted-upconverted-modulated RF signal. In Chapter 3, a novel digital I/Q modulator that alleviates those extreme issues will be uncovered.

Chapter 3

Idea of All-Digital I/Q Modulator

As discussed in the preceding chapters, for wide modulation bandwidths, due to their direct linear summation of the I and Q signals and thus the avoidance of the bandwidth expansion, Cartesian [16,57–66] modulators are prove to be a better choice than their polar [13,14,17,19, 46–49] or outphasing [51, 54–56] counterparts. Reference [16] proposed a digitally controlled I/Q modulator that utilizes current sources to isolate the orthogonal I and Q paths. The exploitation of the current sources, however, worsens the far-out noise. Additionally, in order to produce the required RF output power, that approach employs an external power amplifier. Later, an I/Q direct digital RF modulator is introduced in [63] in which an FIR-based quantization noise filter is embedded in order to filter the quantization noise in the receiver frequency band. Implemented in 130 nm CMOS, it also employed numerous current sources to isolate the orthogonal paths as well as to establish the proper coefficient value for the FIR filtering operation. However, its drain efficiency, at 15.4 dBm output power, does not exceed 13%. Moreover, the related noise floor is not better than -152 dBc/Hz at 20 MHz offset. To alleviate the foregoing concerns, a novel digital I/Q modulator concept is introduced. Section 3.1 explains the principal concept behind the proposed digital I/Q modulator. Section 3.2 discusses the various types of orthogonal summing in digital intensive or all-digital I/Q transmitters. Finally, Section 3.3 summarizes this chapter.

3.1 Concept of Digital I/Q Transmitter

Fig. 3.1 illustrates the concept of the digital I/Q modulator. The desired I/Q vector (IQ) is constructed by vectorial summing of their composite I and Q digital vectors. Their code resolution (N_b) must be high enough to cover all I/Q points of the corresponding trajectory

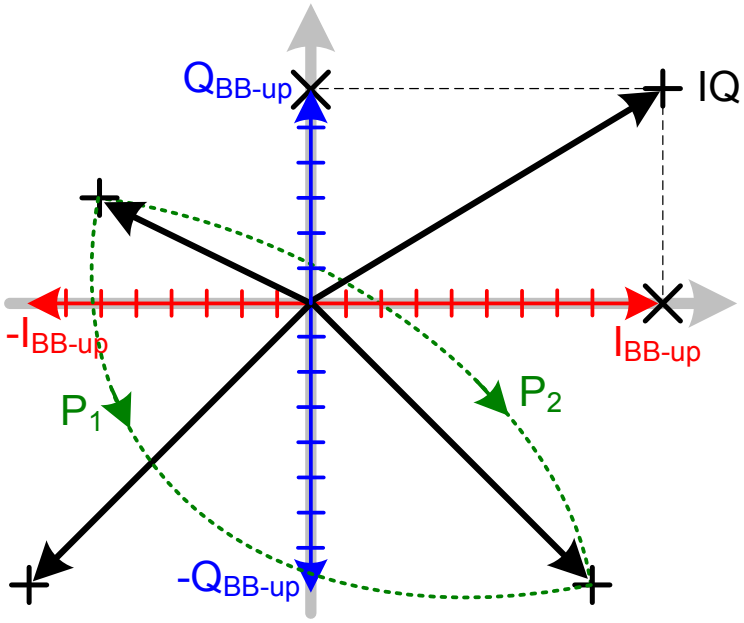

Figure 3.1: Digital I/Q modulation concept; Its related IQ constellation vectors.

connecting the symbols [22].

This indicates that, for supporting only an m-symbol constellation diagram, the resolution of the digital I/Q modulator should be at least[1]

$$N_b \geq \log_2(\sqrt{\frac{m}{4}}) \tag{3.1}$$

In addition, N_b also affects the subsequent quantization noise, which is discussed in more detail in the following chapters. A significant issue related to any transmit modulator is its agility to traverse from one I/Q point to another. As graphically depicted in Fig. 3.1 by P_1 and P_2 paths, traversing along P_2 trajectory instead of P_1 makes the complex baseband modulation faster and, consequently, the modulator must manage a wider bandwidth as well as a higher sampling rate. To do so, based on the idealized block diagram in Fig. 3.2, the I_{BB} and Q_{BB} digital baseband signals are upsampled as interpolated I_{BB} (I_{BB-up}) and interpolated Q_{BB} (Q_{BB-up}). This process ensures that the spectral images will be attenuated and located far away from the carrier and thus can easily be filtered out. The I_{BB-up} and Q_{BB-up} are $2\times N_b$-bit (N_b for in-phase as well as N_b for quadrature component) upsampled digital signals, which should be directly upconverted to their continuous-time reconstructed RF output signal. As a result, these signals are applied to a pair of DRACs, comprising an array of 1-bit unit cell mixers and 1-bit unit cell DPAs.

The DRACs are clocked in tact of differential quadrature upconverting clocks I_P, I_N, Q_P, and Q_N [2]. According to Fig. 3.1, the four quadrants of the constellation diagram must be

[1] Of course, the resolution based on eq. (3.1) is not enough to support corresponding IQ trajectories.

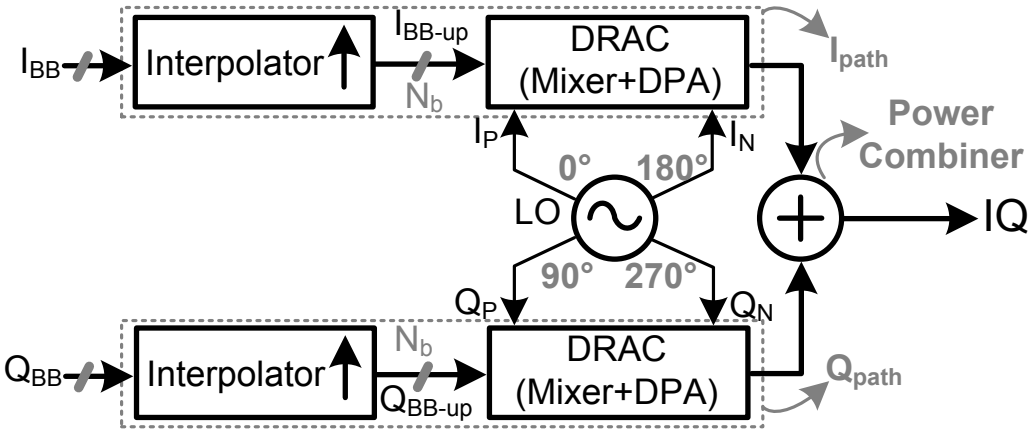

Figure 3.2: Digital I/Q modulation concept; Its related idealized block diagram.

addressed by the modulator. The switching between quadrants can be achieved by swapping between I_P/I_N or/and between Q_P/Q_N according to the sign bits of I_{BB-up} and Q_{BB-up}. The DRAC outputs are connected to a power combiner that facilitates the conversion of the upconverted digital signals into the reconstructed RF output. In fact, the digital I/Q modulator represents an RF digital-to-analog converter (RF-DAC). In this approach, however, the primary challenge is related to the orthogonal summing of the I and Q DRAC outputs in order to reliably reconstruct the modulated RF signal [26, 67–69].

3.2 Orthogonal Summing Operation of RF-DAC

From the digital communications theory, in order to maintain high bandwidth efficiency, the baseband information is generally represented by two orthogonal streams, i.e., I and Q signals, each modulated by the corresponding orthogonal carrier signal (i.e., basis function), and they are subsequently summed. Based on that, the I/Q RF-DAC of Fig. 3.2 has two signal paths, namely, the in-phase path (I_{path}) and the quadrature-phase path (Q_{path}) performing the following operations:

$$I_{path}(t) = (I_P(t) - I_N(t)) \times I_{BB-up}(t) = 2 \times I_P(t) \times I_{BB-up}(t) \tag{3.2}$$

$$Q_{path}(t) = (Q_P(t) - Q_N(t)) \times Q_{BB-up}(t) = 2 \times Q_P(t) \times Q_{BB-up}(t) \tag{3.3}$$

The final modulated IQ signal is generated by vectorial summation of (3.2) and (3.3) and mathematically expressed as:

[2]These clocks comprise four phases separated by 90°

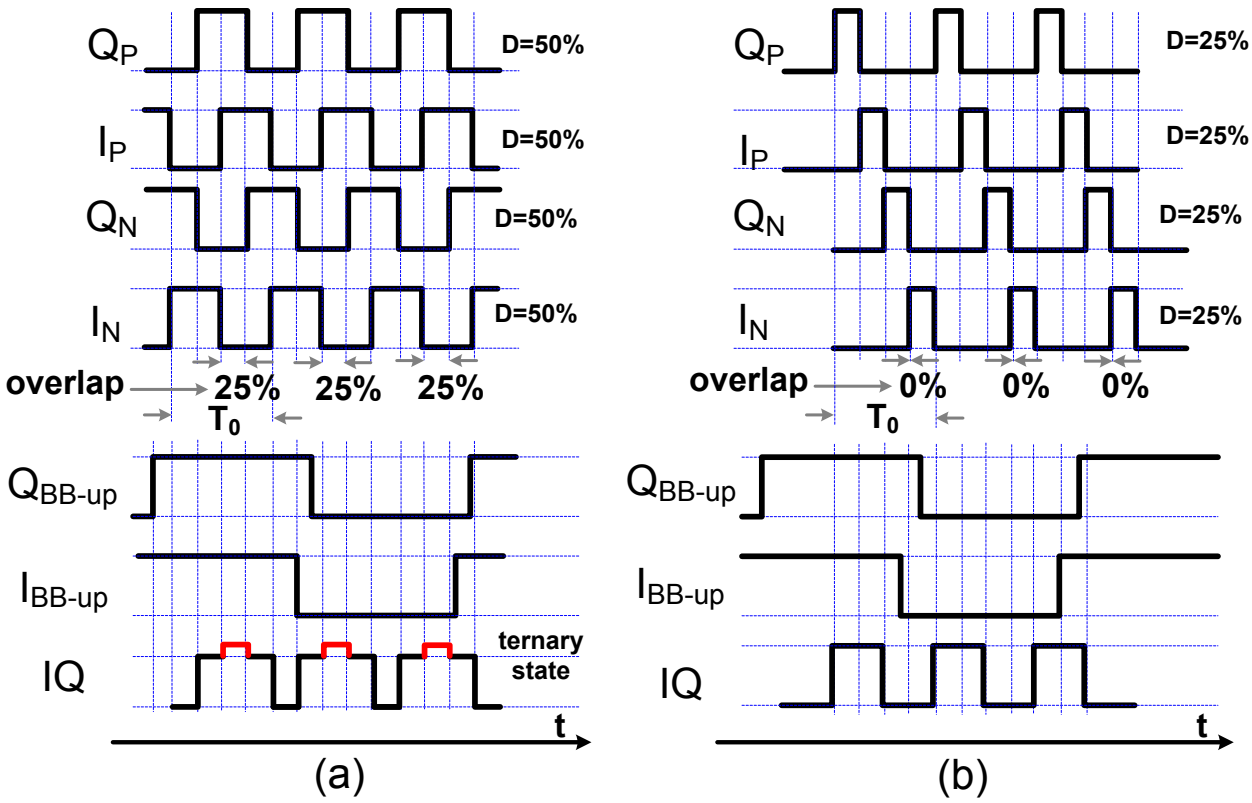

Figure 3.3: Conceptual diagram of I/Q signals: (a) $D = 50\%$; (b) $D = 25\%$.

$$\begin{aligned} IQ(t) &= I_{path}(t) + Q_{path}(t) \\ &= 2 \times \{I_P(t) \times I_{BB-up}(t) + Q_P(t) \times Q_{BB-up}(t)\} \end{aligned} \tag{3.4}$$

The transmitted RF signal is a band-pass filtered version of $IQ(t)$.

$$RF_{out}(t) = \text{filter}\,[IQ(t)] \tag{3.5}$$

Equation (3.4) reveals two aspects of the quadrature modulation: orthogonality and summation. The summing operation must be orthogonal, and there should be no interaction or correlation between I_{path} and Q_{path}, or the EVM, bit error rate (BER) and spectral regrowth will arise. The digital carrier signals are typically rectangular pulses with a 50% duty cycle (D) that toggle between ground and supply. If duty cycle of the upconverted clock is 50% [66], there invariably exists an overlap between I_P/I_N and Q_P/Q_N. Mathematically, their orthogonality can be verified by employing a dot product operation. Fig. 3.3(a) is a conceptual illustration of the carrier signals. Based on mathematical principles, two signals are orthogonal with respect to each other if an integral of their inner product over the interval of one period is zero. The orthogonality of the carrier signals (D=50%) is examined

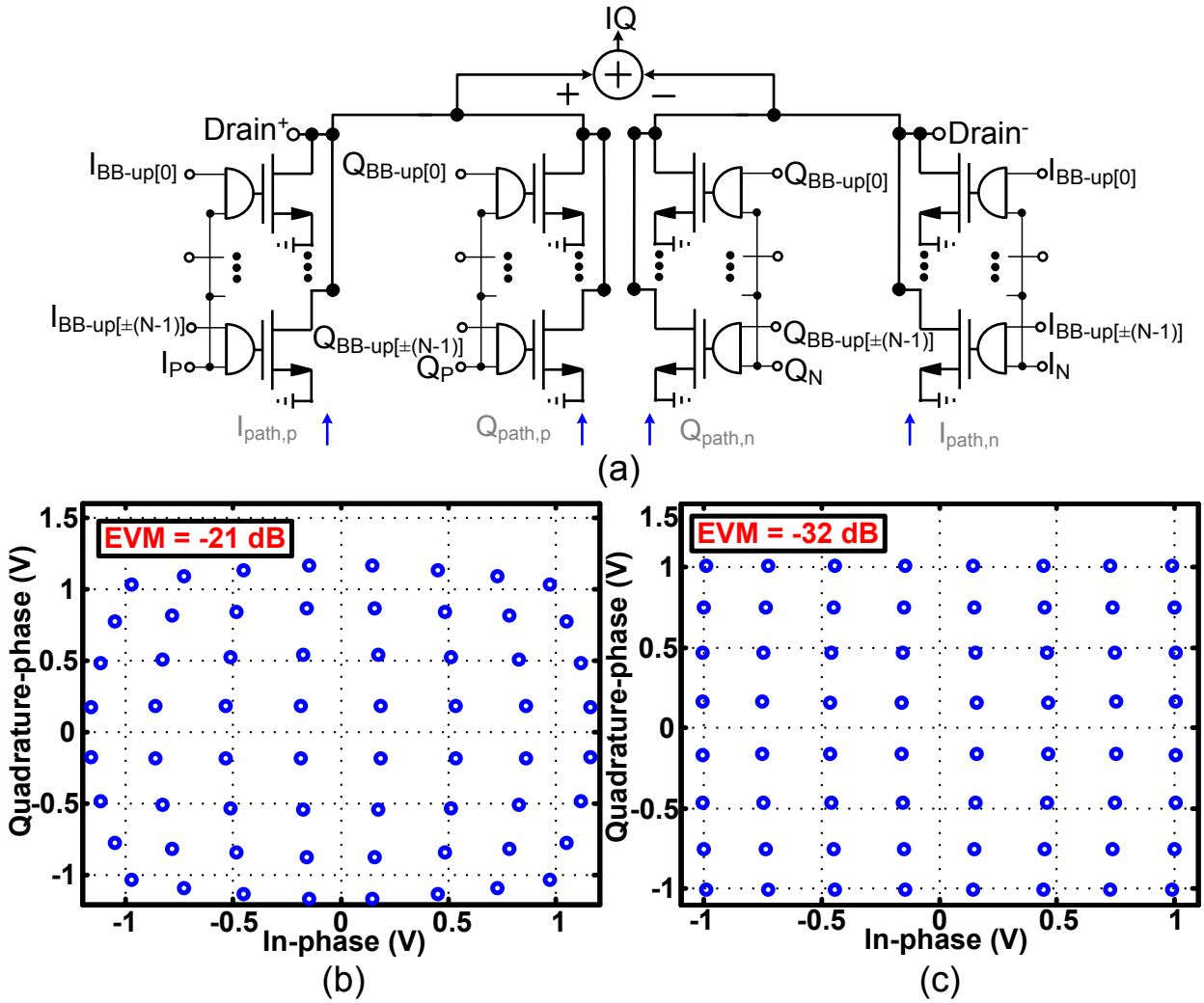

Figure 3.4: (a) Idealized schematic of digital I/Q modulator; Its related SPICE simulated constellation diagrams for (d) D=50%; (c) D=25%.

as follows:

$$\frac{1}{T_0}\int_0^{T_0}[(I_P - I_N)\cdot(Q_P - Q_N)] = 0.25 \tag{3.6}$$

where T_0 is the clock period, and the clocks are assumed of unity amplitude. Based on (3.6) the carrier signals, I_P/I_N and Q_P/Q_N, are not orthogonal. Fig. 3.3(a) intuitively confirms (3.6) and clearly demonstrates that, when I_P and Q_P are both simultaneously one, provided that I_{BB-up} and Q_{BB-up} are also one, then the resulting IQ signal of a practical circuit implementation exhibits a third state. This signifies that the I_{path} and Q_{path} are correlated, and the receiver cannot determine the component to which this unsolicited state belongs. Let's consider an idealized digital I/Q modulator depicted in Fig. 3.4. Employing the D=50% clocks, the foregoing circuit is simulated. According to its SPICE simulated

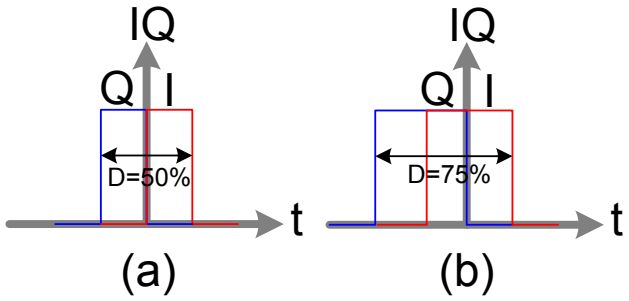

Figure 3.5: Illustration of full power combining of I_{path} and Q_{path} employing upconverting clock for (a) D=25%; (b) D=50%.

Table 3.1: Comparison between 1^{st}, 2^{nd}, and 3^{rd} harmonic components: D=50%; D=75%.

IQ Duty Cycle	**Fundamental (dB)**	**Second (dB)**	**Third (dB)**
50%	-2.34	-327	-11.88
75%	-5.35	-8.36	-14.89

constellation diagram of Fig. 3.4(b), its related EVM at 16 dBm RF output power is -21 dB. Hence, to improve linearity, a sophisticated digital predistortion (DPD) algorithm would be required [66]. In addition, the drain efficiency of its composite DPA is deficient due to the fact that the maximum conduction angle is 75% of the RF clock cycle.

To make the carrier signals orthogonal, their overlapping part should be eliminated. As a result, to perform orthogonal summation, the duty cycle of upconverting clocks is selected at 25% to deter any interaction between the I_{path} and Q_{path}. Based on Fig. 3.3(b), the overlap between I_P/I_N and Q_P/Q_N is now zero and the resultant IQ signal comprises only two states. The orthogonality of the new carrier signals can be expressed as:

$$\frac{1}{T_0}\int_0^{T_0}[(I_P - I_N)\cdot(Q_P - Q_N)] = 0 \tag{3.7}$$

Thus, this also mathematically confirms the orthogonality of the component carriers. The solution could be considered as a TDD in which the linear addition of the time-shifted I and Q paths is accomplished by allocating individual time slots to enter the I/Q information into the system. Employing the aforementioned D=25% upconverting clocks of the digital I/Q modulator of Fig. 3.4(a), the circuit level simulated constellation diagram of Fig. 3.4(c) is achieved. Its corresponding EVM at 16 dBm RF output power is -32 dB. As a result, this system only needs a very simple DPD [70, 71] and, more significantly, the related drain efficiency of its composite DPA is higher due to the 50% maximum conduction angle. Note that, according to Fig. 3.4, the I/Q RF-DAC can cover the entire 4-quadrant constellation diagram.

It should be pointed out that, at the maximum power of operation, since both I_{path}

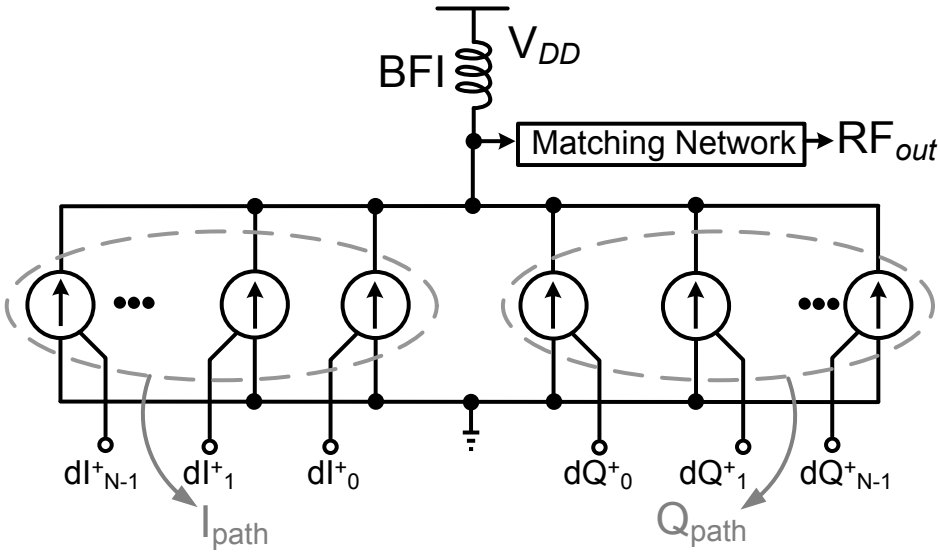

Figure 3.6: Analog current source arrays summing.

and Q_{path} are activated, the subsequent drain voltage waveform is a square-shaped signal with D=50% providing that the duty cycle of their related upconverting clocks is 25% (see Fig. 3.5(a)). In contrast, if the duty cycle of the upconverting clock is chosen at 50%, which is depicted in Fig. 3.5(b), their subsequent IQ signal is a square-shaped waveform with the duty cycle of 75%. Table 3.1 summarizes their corresponding fundamental, second, and third harmonic frequency components. According to it, the fundamental component of the 50% IQ waveform is $\sqrt{2}\times$ higher than with the 75% one. Moreover, the 50% IQ waveform, ideally, creates a zero second harmonic frequency component which facilitates the design of the following transformer balun in the power combiner. On the other hand, the preceding clock generator circuits of the 50% duty cycle differential quadrature signals are less complicated than their 25% counterparts.

As stated earlier in (3.4), an additional aspect of the quadrature modulation is the summation. There would be at least four different ways of adding the orthogonal base function signals.

In the first approach [16, 58], as depicted in Fig. 3.6, the summation is performed by electrically connecting unit-weighted ideal current sources and adding them according to the input data. The controlling signals of the current sources are $dI^+_{0,1,\cdots,N-1}$ and $dQ^+_{0,1,\cdots,N-1}$ and are expressed as:

$$dI^+_{0,1,\ldots,N-1} = I_P \times I_{0,1,\ldots,N-1} \tag{3.8}$$

$$dQ^+_{0,1,\ldots,N-1} = Q_P \times Q_{0,1,\ldots,N-1} \tag{3.9}$$

which indicates the implicit mixer operation. For maintaining the orthogonality of the I/Q

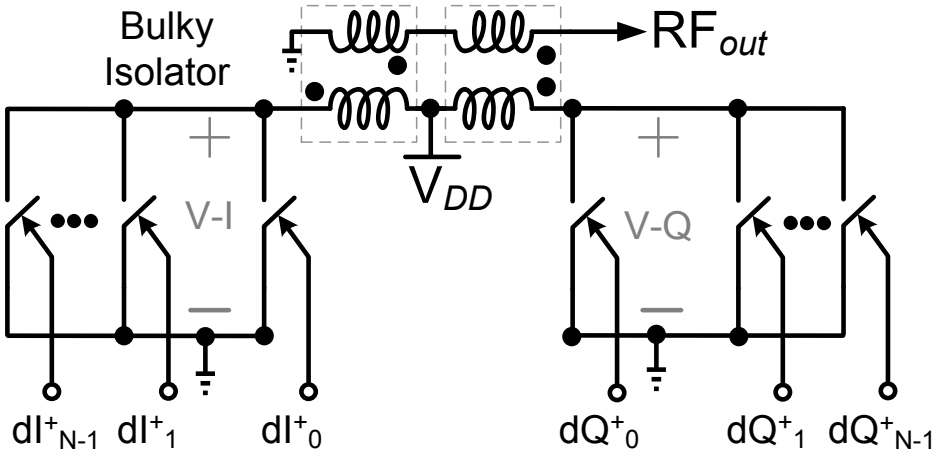

Figure 3.7: Two separate digital switch arrays using transformer summing.

signal, the I_{path} and Q_{path} must be uncorrelated such that one signal path output does not affect the operation of the other. This might require resorting to a current source impedance boost technique, such as cascoding. Unfortunately, stacking of the MOS transistors in a cascode structure is difficult in the modern low-voltage CMOS technologies and further produces an excessive amount of leakage and noise. In summary, numerous disadvantages exist related to this approach. First, this structure comprises MOS current sources which continuously work in the saturation region, therefore, create more noise than when operated in other regions. This structure is primarily implemented employing the Gilbert mixer topology. The thermal output spot noise of a Gilbert cell mixer can be approximated as [60]:

$$\overline{V_{out-n}^2} = 4KT\gamma\frac{G^2}{g_m} + KT\pi\frac{G}{g_m} \tag{3.10}$$

where K=1.38×10^{-23} J/K denotes the Boltzmann constant, T is the absolute temperature, the parameter γ has a value of 2/3 in saturation region for long channel devices, g_m is the device transconductance, and $G \propto g_m R_{out}$ is the voltage gain of the Gilbert mixer (R_{out} is the equivalent mixer output resistance). Since the gain of the mixer is constant due to linearity constrain, in order to reduce the noise, g_m should be increased. Thus, as a second disadvantage, the power efficiency of this approach is minimal, as is apparent in [16, 58]. Third, the linearity of this structure is not promising due to the voltage to current conversion in the Gilbert cell.

The second approach illustrated in Fig. 3.7 might also be realized as a pair of digitally-controlled RF-modulated resistor structures. This approach could benefit from a less complicated circuit, the lack of stacked devices, and the elimination of noisy current sources. Since the MOS switch operates either in the off or in triode state, less noise is introduced. In addition, because of the switched-mode behavior, it has a potential to produce higher power efficiency [50]. Unfortunately, the final I/Q signal summation is difficult to accomplish in

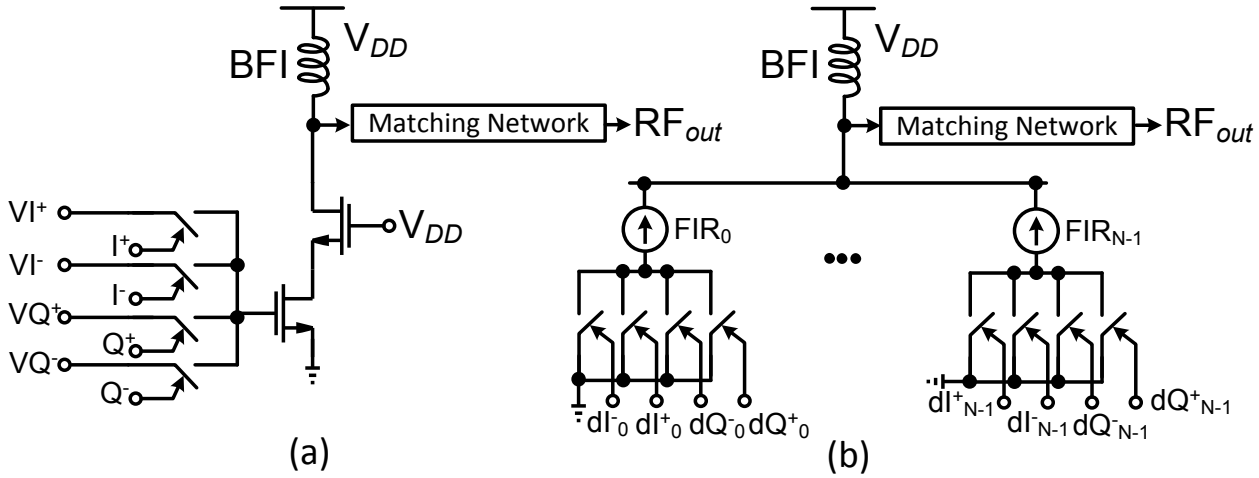

Figure 3.8: (a) Quadrature passive upconverting mixer using 25% duty cycle upconverting clock. (b) Analog current source FIR arrays summing.

this method since the individual I and Q outputs are not currents but, instead, voltages. Due to the fact that the individual voltages of the RF outputs of the matching networks must be included, bulky microwave-type isolator/combiner would be required, otherwise, the RF voltage level of the I_{path} will affect the impedance of the Q_{path}, and vice versa. Hence, the I/Q orthogonality of this structure will not be preserved.

The third approach is based on employing the quadrature passive mixer which utilizes 25% duty cycle upconverting clock which is depicted in Fig. 3.8(a) [60, 61]. Note that, in this approach, the baseband input signals are converted to analog continuous-time waveforms exploiting two separate DACs and their following LPFs (see [60,61]). To boost the subsequent upconverted signals, however, this approach requires stand alone on-chip as well as off-chip power amplifiers. Thus, its power efficiency is deficient. Moreover, this approach is a digitally intensive approach rather than a fully digital approach. In order to transform it into a fully digital structure, the upsampled baseband signals are directly applied to passive mixer arrays [63]. In this approach, the in-phase and quadrature-phase signals are orthogonally summed employing analog current source cells which are depicted in Fig. 3.8(b). Note that the aforementioned current sources also provide the required FIR filter coefficient in order to notch the generated noise of the transmitter at the receiver frequency band. Implemented in a 130 nm CMOS process, this approach requires large voltage headroom due to adopting current sources. Moreover, this structure necessitates an additional power amplifier to increase the transmitted RF power thus its power efficiency is deficient.

In the fourth approach, the total I/Q summation is also performed by the addition of unit-weighted digital switches (Fig. 3.9(a)), each contributing a finite conductance G. The difference between the second and fourth approaches is that, in the former, the I_{path} and Q_{path} are isolated and subsequently summed in the voltage domain while, in the latter, these paths are electrically summed (like in the first approach). As a result, this approach

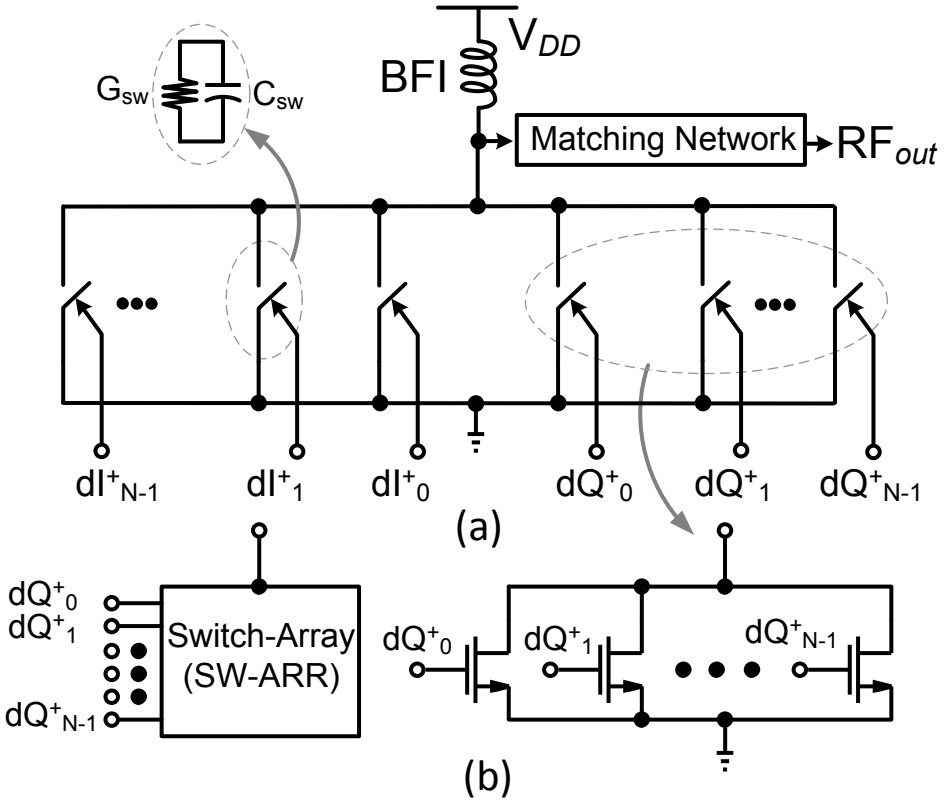

Figure 3.9: Electric summing; (a) digital switch arrays; (b) switch array structure.

selectively exploits the best advantages of the first and second approaches.

Utilizing the Agilent ADS$^{\text{TM}}$ circuit simulator, two simulations ($D = 50\%$, and $D = 25\%$) are performed based on the approach exhibited in Fig. 3.9(a). The corresponding I/Q switch array banks comprise 512 unit-weighted switches. The dimensions of each NMOS switch are W/L = 660 nm/100 nm. The frequency of operation targets the basestation WCDMA band-I at 2.14 GHz. Simulation results confirm that, for the $D = 50\%$ case in Fig. 3.10(a), the orthogonal summation is not feasible. The reason is that, in the overlap region, the drain voltage further decreases and forces both I and Q switch banks to enter deep-triode, which causes a subsequent drop in the drain current. However, for $D = 25\%$ in Fig. 3.10(b), there is no overlap; therefore, the summation possesses potential to be orthogonal. As depicted in Fig. 3.9(a), each digital switch can be modeled as a combination of a parallel conductor (G_{sw}) and drain capacitor (C_{sw}). The off-state resistance of the switch is substantial and can be approximated as a zero conductance. The on-state conductance and resistance of the NMOS switch are:

$$G_{sw-ON} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \tag{3.11}$$

$$R_{sw-ON} = \frac{1}{G_{sw-ON}} \tag{3.12}$$

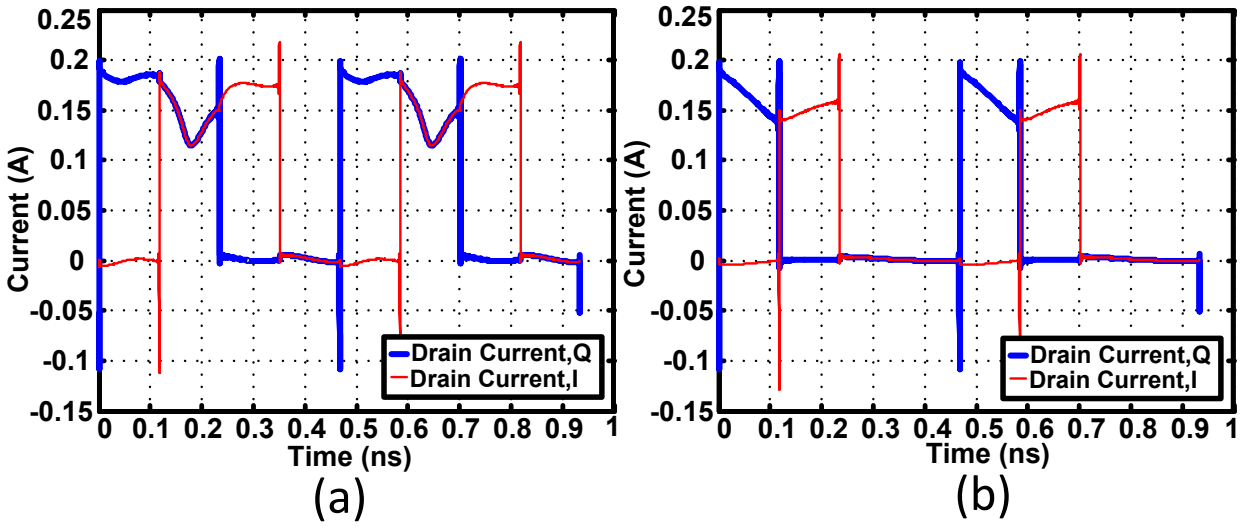

Figure 3.10: Simulated I/Q drain currents (a) $D = 50\%$; (b) $D = 25\%$.

where μ_n, and C_{ox} are electron mobility and gate oxide capacitance per unit area of NMOS transistor, respectively. In addition to the finite conductance (3.11), C_{sw} depends on the width of the switching transistor [72].

$$C_{sw} = W \times E \times C_j + 2 \times (W + E) \times C_{jsw} \tag{3.13}$$

where E is drain length, C_j and C_{jsw} are junction capacitance per unit area, and sidewall capacitance per unit length, respectively. Note that junction capacitance is inversely related to drain voltage.

$$C_j = \frac{C_{jo}}{\left[1 + \frac{V_R}{\Phi_B}\right]^m} \tag{3.14}$$

where V_R is reverse bias voltage to the drain terminal, Φ_B is the junction built-in potential, and m is an exponent power typically in the range of 0.3 and 0.4. As a result, C_j and, consequently, C_{sw} strongly depend on drain DC value. Based on (3.11) and (3.13), due to the fact that that they are proportional to the switch channel width, there exists a trade off between G_{sw-ON} and C_{sw}. The parasitic capacitance impacts the resonant frequency of the power combining network and diminishes its quality factor Q_F. By cumulatively turning the switches on in the sequential manner (see Fig. 3.9), the total conductance of I_{path} and Q_{path} will be increased as:

$$G_{sw-I-N_I} = \sum_{i=0}^{i=N_I-1} G_{sw-I}(i) \tag{3.15}$$

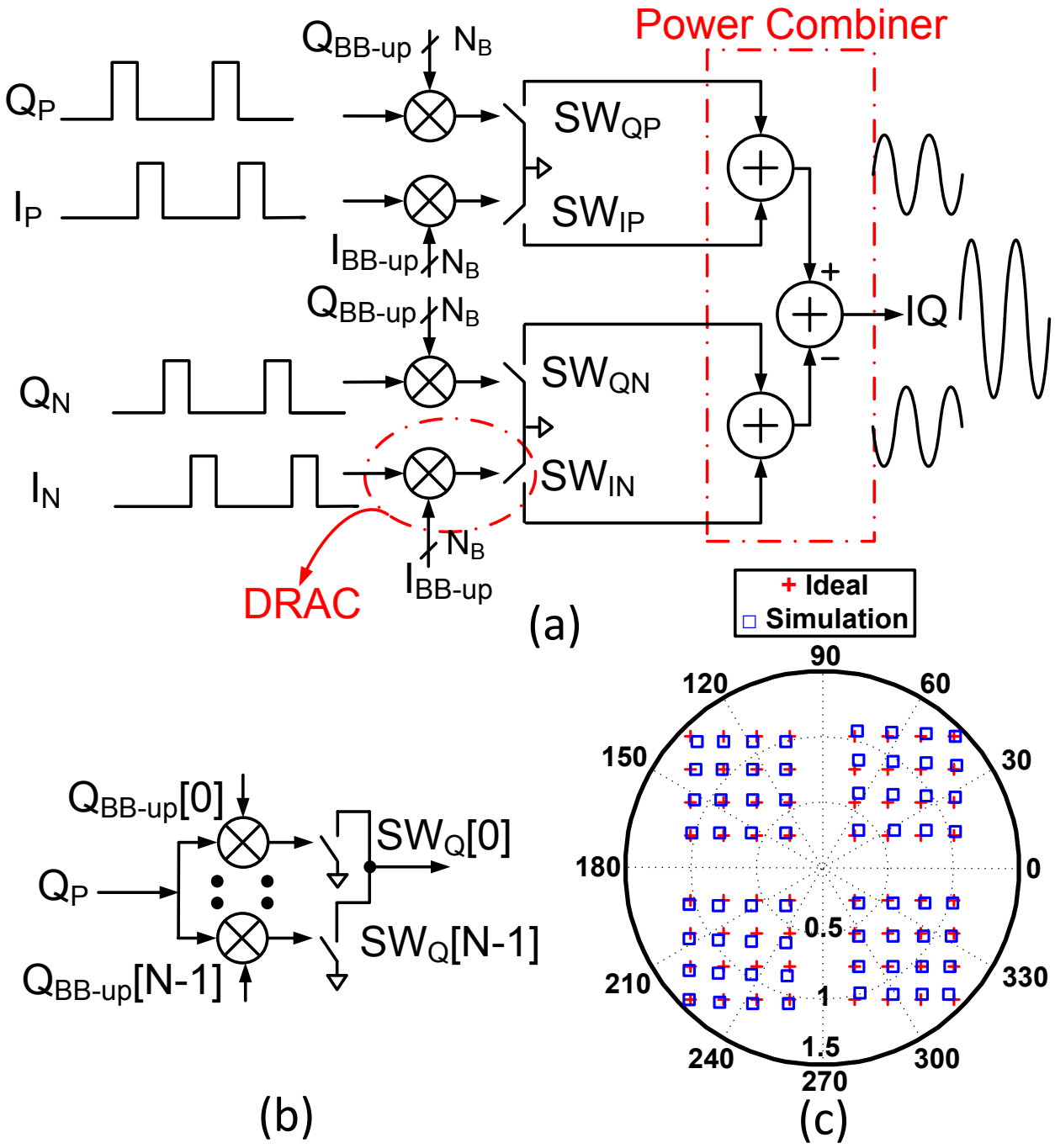

Figure 3.11: Illustration of: (a) an RF-DAC-based orthogonal digital I/Q modulator, (b) DRAC, (c) Spice post-layout simulation result of 64-point I/Q constellation diagram.

$$G_{sw-Q-N_Q} = \sum_{i=0}^{i=N_Q-1} G_{sw-Q}(i) \tag{3.16}$$

where $N_I \leq N$ and $N_Q \leq N$ are the number of ON-state NMOS switches of I_{path} and Q_{path},

respectively. N is the number of NMOS switches in each individual I/Q path. Moreover, the total resistance of each switch array (I or Q) is:

$$R_{on} = \frac{1}{\sum_{i=0}^{i=N-1} G_{sw}(i)} \tag{3.17}$$

Equations (3.15) and (3.16) indicate that, by controlling the state of the digital switches, the conductance (current capability) and, consequently, the output amplitude of the I/Q switch banks can be varied.

$$G_{sw-I-N_I} \propto I_{BB-up} \tag{3.18}$$

$$G_{sw-Q-N_Q} \propto Q_{BB-up} \tag{3.19}$$

Collectively considering (3.4), (3.15), (3.16), (3.18), and (3.19), the modulator can, therefore, cover the I/Q constellation points of a chosen digital communication standards, e.g., WCDMA, Wi-Fi, or WiMAX.

$$IQ \propto I_P \times G_{sw-I-N_I} + \mathrm{j} \times Q_P \times G_{sw-Q-N_Q} \tag{3.20}$$

To cover all four quadrants of the constellation diagram, the modulator requires the complementary (or differential) phases of quadrature I_P and Q_P clocks. According to Fig. 3.11(a), I_P, Q_P, I_N, and Q_N each has a 25% duty cycle and a relative phase difference in multiples of 90°. In fact, by swapping between I_P/I_N or between Q_P/Q_N, the sign bits of the baseband data can be reversed.

$$\begin{aligned} IQ &\propto \pm(I_P - I_N) \times G_{sw-I-N_I} \pm \mathrm{j} \times (Q_P - Q_N) \times G_{sw-Q-N_Q} \\ &\propto \pm 2 \times I_P \times G_{sw-I-N_I} \pm \mathrm{j}2 \times Q_P \times G_{sw-Q-N_Q} \end{aligned} \tag{3.21}$$

Each clock subsequently mixes with the baseband data and finally drives the corresponding switch. The combination of the mixer and switch array thus constitutes the DRAC (Fig. 3.11(b)), which is an individual I or Q modulator within the composite I/Q RF-DAC. A simulation of a 64-point constellation of the proposed approach is demonstrated in Fig. 3.11(c) and indicates as follows:

1. Using the four banks of DRAC, the amplitude and phase of the resultant IQ signal are modulated;

2. By interchanging between the differential clocks, the four quadrants of the constellation diagram can be addressed.

Note that the thermal output spot noise of this structure employing upconverting clock with

D=25% is as follows:

$$\begin{aligned}\overline{V_{IQ,n}^2} &= 2\times(4KTR_{sw-I-N_I}+4KTR_{sw-Q-N_Q})\times(D)\\ &= 2\times(4KTR_{sw-I-N_I}+4KTR_{sw-Q-N_Q})\times(\frac{1}{4})\\ &= 4KTR_{on}\end{aligned} \tag{3.22}$$

As a result, comparing to (3.10), the noise performance of the proposed modulator is superior. The modulator output spot noise with respect to the maximum power of operation is as follows:

$$\begin{aligned}P_{relative-noise-power} &= \frac{\overline{V_{IQ,n}^2}}{V_{out-full}^2}\Rightarrow\\ P_{relative-noise-power}|_{dBc/Hz} &= 10\log\frac{\overline{V_{IQ,n}^2}}{V_{out-full}^2}\end{aligned} \tag{3.23}$$

Considering R_{on}=1 Ω, and $V_{out-full}$=1 V, the relative spot noise power based on (3.23) is -197.81 dBc/Hz. Note that equation (3.23) does not take the noise contribution from the clock signals into consideration. Otherwise stated, the thermal noise of the I/Q switches only minimally affect the eventual noise performance of the modulator. Specifically, this amount of spot noise is sufficient to meet the stringent communication standards at the receiver frequency bands.

3.3 Conclusion

A novel all-digital I/Q RF modulator is described. Employing an upconverting RF clock with a 25% duty cycle ensures the orthogonal summation of I_{path} and Q_{path}, which avoids nonlinear signal distortion. It was clarified that electric summing of I and Q digital unit array switches is the most appropriate I/Q orthogonal summation approach. Moreover, to address all four quadrants of the constellation diagram, the differential quadrature upconverting RF clocks must be utilized. In addition, it was explained that employing switches instead of utilizing current sources leads to superior noise performance of the all-digital I/Q transmitter.

Chapter 4

Orthogonal Summation: A 2×3-bit All-Digital I/Q RF-DAC

Following the orthogonal summing concept of the digital I/Q modulator in Chapter 3, this chapter presents a simple 2×3-bit all-digital I/Q modulator to justify the proposed solution [67] [69]. Note that, as will be explained in Chapter 5, the baseband code resolution of three bits is not an appropriate option for supporting the most stringent communication standards. However, in order to simply substantiate the proposed *orthogonal* I/Q RF modulator, its resolution is selected to be 2×3-bit, which is the most straightforward and feasible I/Q RF modulator. In the conventional analog I/Q approach of Fig. 2.1, the DACs and mixer tend to be of a rather bulky and power hungry. The proposed I/Q approach in Fig. 4.1 employs a pair of DRACs which comprise implicit mixers and switch array banks that directly convert the digital signal input to its RF waveform representation. Hence, the circuit functions as an RF-DAC with a discrete-time complex-valued digital input and a real-valued continuous-time output. Note that, in such an approach, the traditional analog-circuit issues of calibration and timing misalignment no longer pose a problem since the digital discrete-time operation is clock-cycle accurate with modern technology sufficiently supporting sampling rates in the GHz range. This yields ultra-fast settling of the RF-DAC conversion circuit. Consequently, these digital circuits can ensure fine timing accuracy that is constant (to at least within a clock cycle delay) and not subject to processing and environmental changes.

In this specific implementation, the output clock of an on-chip LO, which operates at 4× of the desired carrier frequency, is first down-converted by a divide-by-4 circuit. Inherently, it directly provides the required I and Q clocks with their appropriate phase relationship and duty cycle. The differential in-phase (c_I^+/c_I^-) and quadrature-phase (c_Q^+/c_Q^-) clocks, at

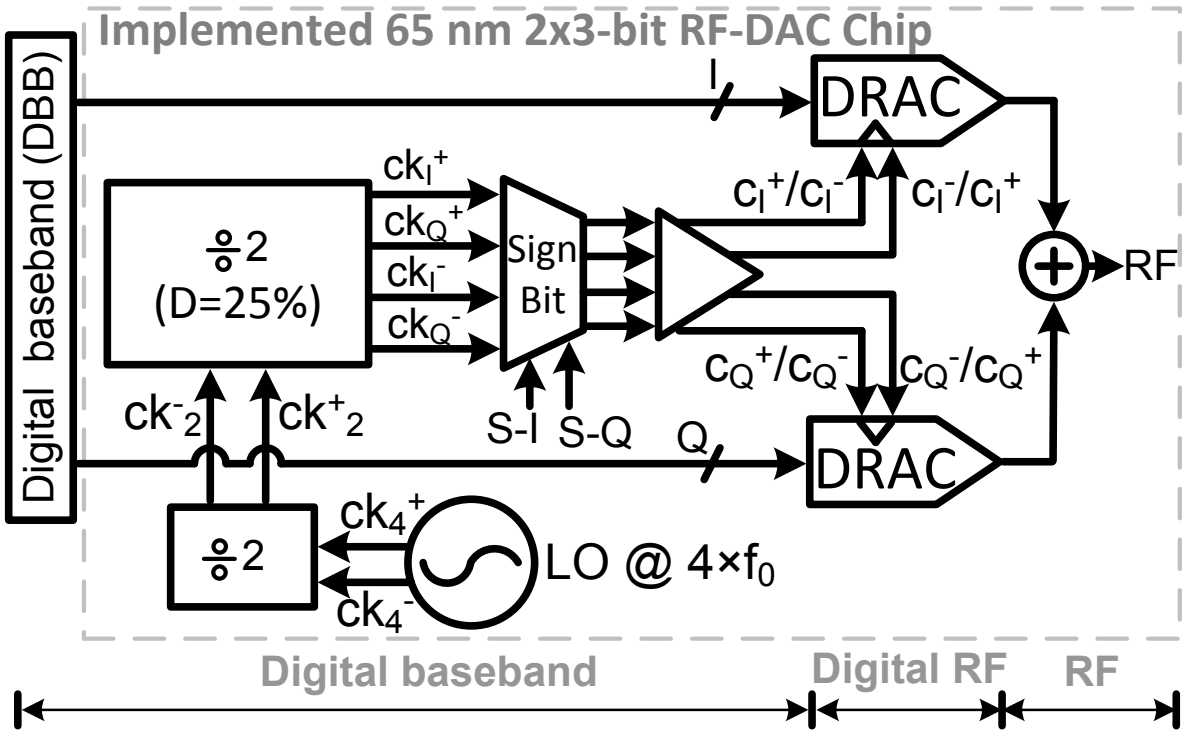

Figure 4.1: Implementational block diagram of the 2×3-bit all-digital I/Q modulator.

fundamental frequency of f_0, are subsequently "multiplied" by the baseband I/Q signals through the implicit mixer and drive the transistor switch arrays. The outputs of the switch arrays are connected to a power combining network that adds and converts the discrete-time pulses into a continuous-time RF output signal. As previously discussed, the proposed approach represents an RF-DAC which, as such, does not require the baseband DAC and explicit mixers of Fig. 2.1. Moreover, the bandwidth of the digital modulator is only limited by the passive output power combiner and the speed of the digital circuitry. The main technical challenge is the orthogonal summing of I/Q pulses in order to reconstruct the modulated RF signal. Section 4.1 thoroughly explains the circuit building blocks of the proposed modulator including a digitally controlled oscillator, divide-by-two circuit, 25% duty cycle generator, sign bit circuit, implicit mixer, and a 2×3-bit I/Q switch array circuit. Section 4.2 addresses the related measurement results. The conclusion of the chapter is drawn in Section 4.3.

4.1 Circuit Building Blocks of Digital I/Q Modulator

In the remainder of this section, the modulator's building blocks will be sequentially unveiled and their circuit design techniques described.

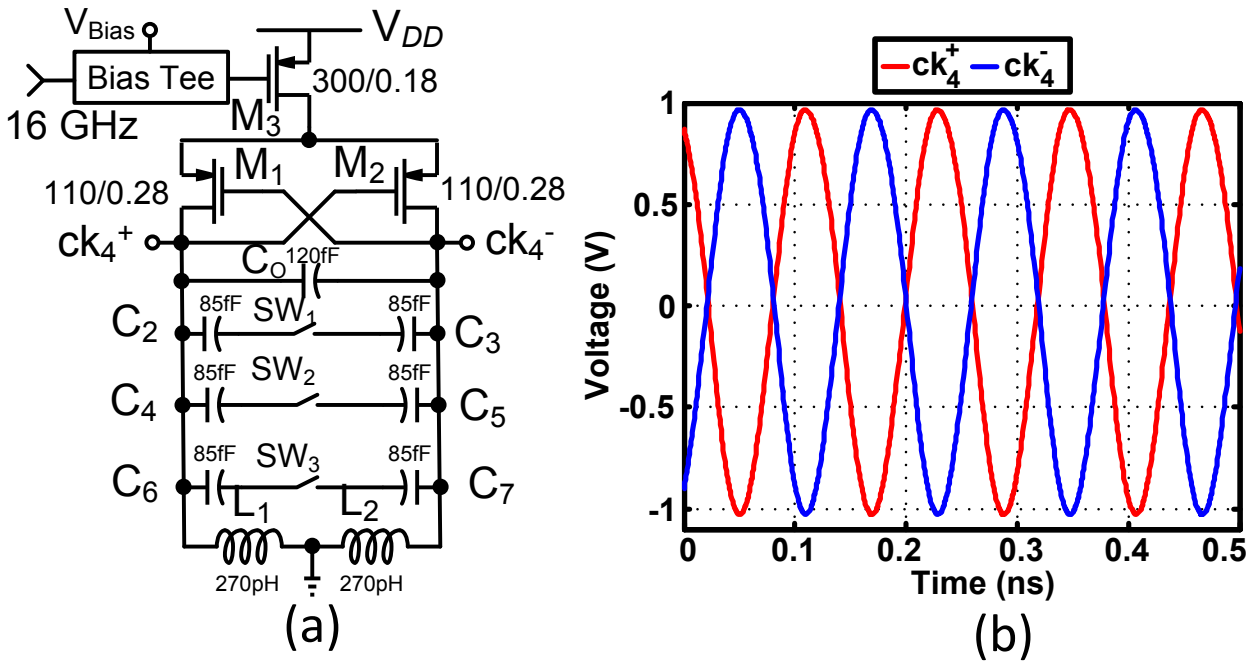

Figure 4.2: DCO (a) circuit schematic; (b) simulation results.

4.1.1 Digitally Controlled Oscillator

An on-chip 8 GHz DCO is included to generate the clock signals for the digital I/Q modulator that targets 3G cellular basestation applications operating at 2 GHz[1]. Following are explanations for the selection of the 8 GHz DCO resonating frequency:

1. The energy of the DCO resonating at 8 GHz will not substantially leak to the 2 GHz output;
2. The injection pulling of the 2 GHz RF output has a sufficiently weak 8 GHz harmonic to disturb the DCO resonant tank;
3. The 8 GHz DCO occupies less area than the 4 GHz or 2 GHz DCO due to its smaller inductor;
4. Frequency-down conversion of the 8 GHz signal automatically yields the proper fundamental I and Q differential clock signals in which their related duty cycle is 25%.

Fig. 4.2(a) demonstrates the DCO core circuit which is a conventional cross-coupled LC-tank DCO with a PMOS current source. Fig. 4.2(b) exhibits the simulation results of the differential output nodes ck_4^+ and ck_4^-. In order to be able to construct the constellation

[1]Courtesy of my group colleague Akshay Visweswaran. The DCO and the first divider have been designed and laid-out by him.

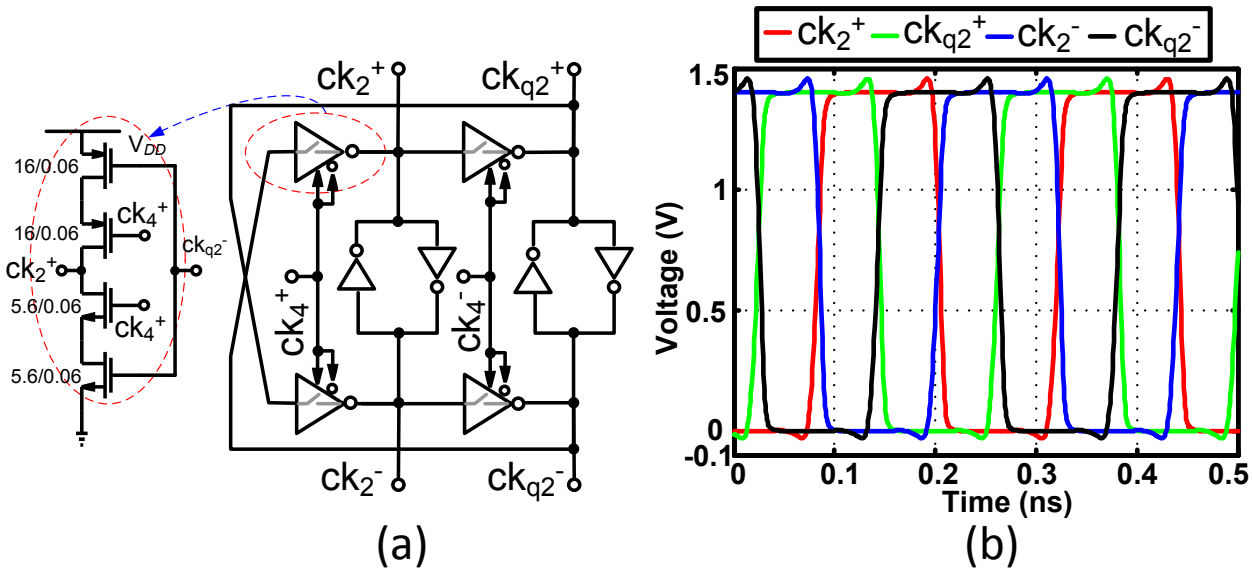

Figure 4.3: first divider: (a) schematic; (b) simulation results.

diagram and calculate the EVM of the modulator as it was illustrated in Fig. 3.11(c), the modulated phase must be measurable. Therefore, the modulator requires a stable phase reference. To achieve that, the DCO is injection-locked to an external 16 GHz oscillator through the tail current source M_3. Since the source nodes of the cross-coupled transistors M_1 and M_2 exhibit 2× the frequency of their drain nodes, this node is forced to lock to the injected signal (16 GHz reference clock) [73]. It should be noted that, for injection-locking of the DCO, the bias voltage node (V_{Bias}), and three-bit switched-capacitor (varactor) bank should be tuned. The varactor elements force the DCO into the vicinity of 8 GHz so that it can be easily injection-locked.

4.1.2 Divide-By-Two Circuit

The differential signals of ck_4^+ and ck_4^- are applied to the first divide-by-two circuit, which is depicted in Fig. 4.3(a). For the frequency down conversion, as demonstrated in Fig. 4.1, the chip employs two divide-by two circuits. The divider comprises four gated inverters, namely C^{2}MOS latches [74] [75], that latch the input clocks. The back-to-back inverters [14] guarantee that the prohibited state will not occur. This divider provides a very low jitter and the speed increases with process scaling. Moreover, the divider output frequency is 4 GHz, and it creates quadrature outputs, which are exhibited in Fig. 4.3(b). For the subsequent stage, only one differential node (i.e., ck_2^+ and ck_2^-) of the divider is required.

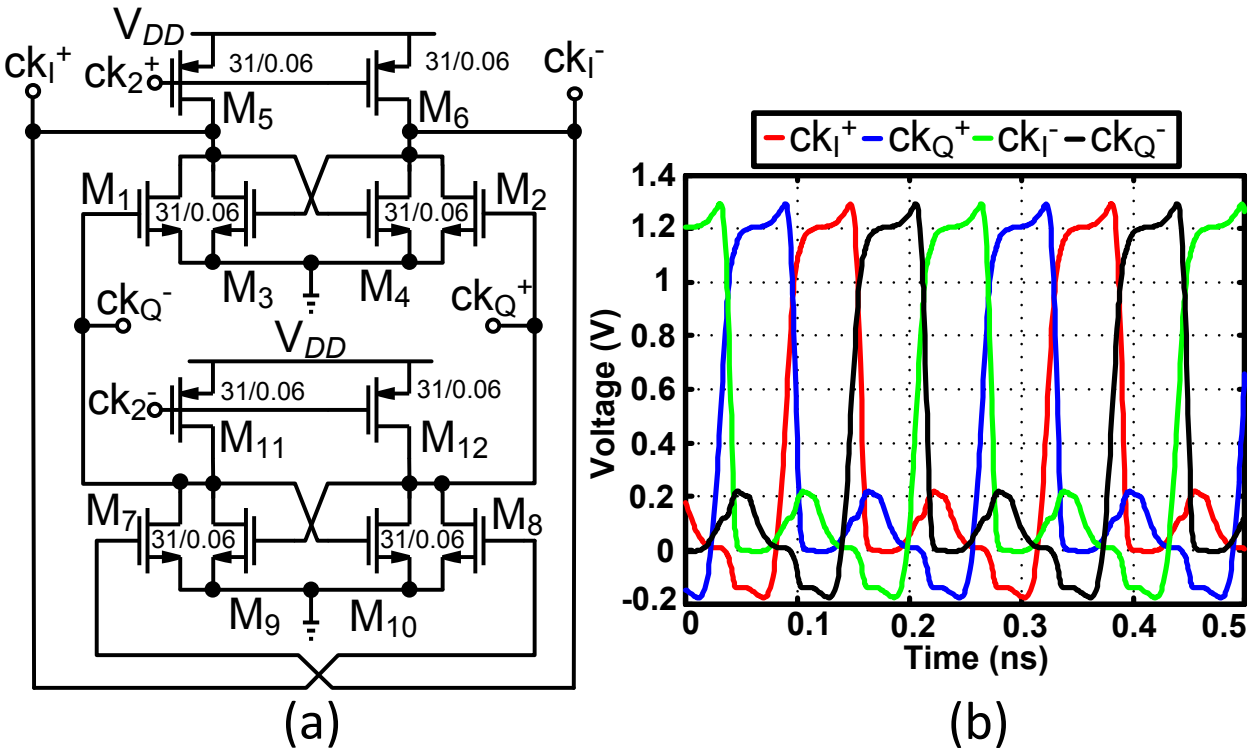

Figure 4.4: Second divider (a) schematic; (b) simulation results.

4.1.3 25% Duty Cycle generator

As a result, the ck_2^+ and ck_2^- nodes drive the second divider which subsequently produces the four clock phases with the targeted duty cycle of 25% at 2 GHz [76] (see Fig. 4.4(a)). The clock nodes (ck_2^+ and ck_2^-) run at 2× the fundamental frequency (4 GHz), while ck_I^+, ck_Q^+, ck_I^-, and ck_Q^- represent the 2 GHz clock signals with a 25% duty cycle. The simulation result of the second divider is illustrated in Fig. 4.4(b). The divide-by-two and 25% duty cycle signal generation are explained as follows. In each input clock cycle (i.e., the differential nodes of ck_2^+ and ck_2^-), two of the PMOS transistors (e.g., M_5 and M_6) are activated, which makes one of the drain nodes high (e.g., ck_I^+) and the other (cross-coupled differential drain node, ck_I^-) low. In this case, the previous state of the nodes ck_I^+, ck_Q^+, ck_I^-, and ck_Q^- are low, high, low, and low, respectively. It should be mentioned that ck_I^- also has a tendency to be high (since M_6 is also active) but, because of the positive feedback from the cross-coupled transistors of M_3 and M_4, it eventually returns to a low level (see in Fig. 4.4(b), the small ripple of each node around the ground). Simultaneously, the other two (e.g. M_{11} and M_{12}) are off thereby generating floating nodes that allow the ck_Q^- to remain low, and ck_Q^+ decreases from a high to a low level because ck_I^+ is now in high level state. Therefore, $ck_I^+, ck_Q^+, ck_I^-, ck_Q^-$ = "1000". This indicates that, in each half cycle of the input clock, the high level output voltage of the circuit rings from one node to another node and, consequently, in two cycles

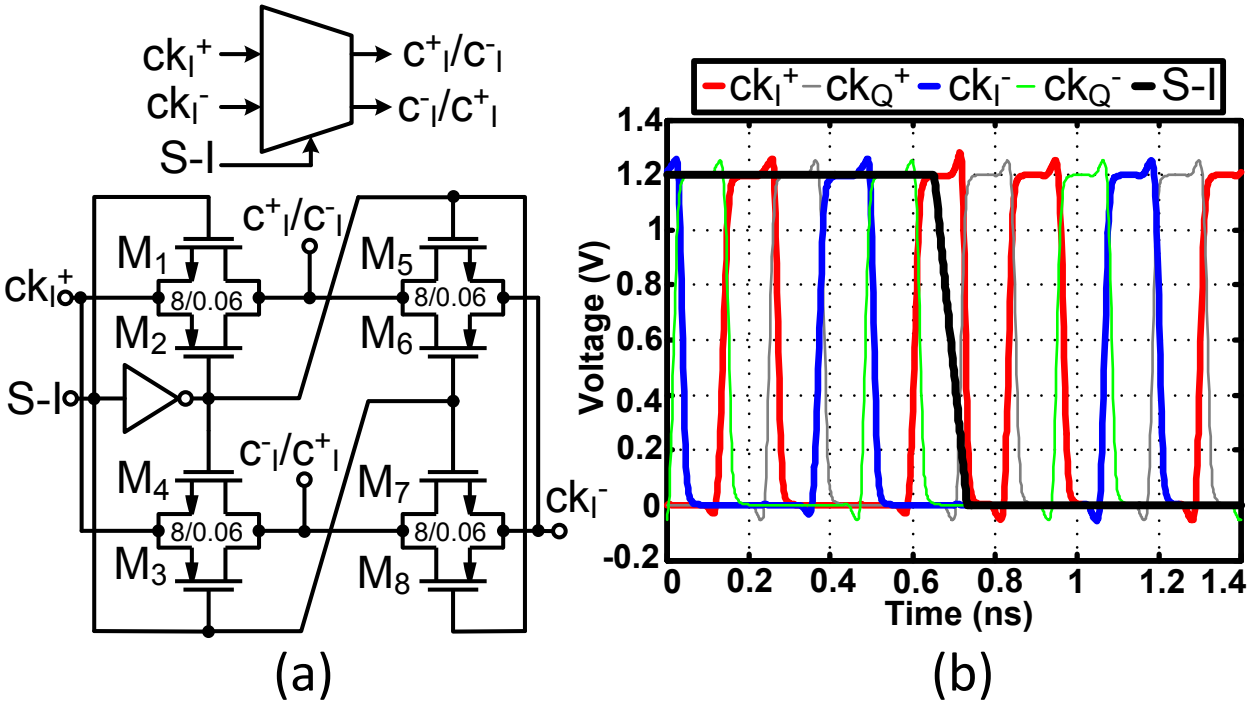

Figure 4.5: Sign bit selector: (c) schematic; (d) simulation results.

of the input clock (divide-by-2), the high level voltage passes through all of the output nodes (i.e. the circuit generates a 25% duty cycle).

4.1.4 Sign Bit Circuit

The slightly distorted, four differential quadrature clock signals of ck_I^+, ck_Q^+, ck_I^-, and ck_Q^- are "cleaned" by the subsequent clock buffer stages and applied to the sign bit circuit. To address the four quadrants of the I/Q constellation diagram, as mentioned in Chapter 3.2, the modulator additionally requires two sign bits. Fig. 4.5(a) demonstrates the sign-bit circuit for the in-phase I clocks, which proves to be a multiplexer. According to the simulation result of the sign bit circuit (see Fig. 4.5(b)), when the sign bit is high, then ck_I^+ and ck_I^- pass directly through the transmission gate switches to the c_I^+ and c_I^- nodes. When the sign bit is low, the inputs ck_I^+ and ck_I^- are swapped through the pass-gate switches to reach the c_I^- and c_I^+ nodes, respectively. The same circuit is employed for the Q clock, thus, in total, the modulator requires two multiplexer circuits.

4.1.5 Implicit Mixer Circuit

The four clock signals transit through clock buffers to arrive at the implicit mixer stages. Fig. 4.6(a) indicates one of the unit cells of the implicit mixer which is realized as a transmission gate based AND gate. The clock signal c, which could be any of the c_I^+, c_Q^+, c_I^-, or c_Q^-

signals of Fig. 3.11, passes through the transmission gate if the baseband data bit I or Q is asserted, and the resulting signal is termed dI or dQ which is an up-converted version of the I or Q, respectively. The pull-down NMOS transistor (M_3) is utilized for suppressing carrier leakage. The M_3 transistor should be appropriately sized in order to shunt the carrier energy at the gate of the switch array transistor in the unit's off-state without excessive loading in the unit's on-state.

4.1.6 2×3-bit I/Q Switch Array Circuits

Fig. 4.6(b) demonstrates the corresponding equivalent transistor switch array of Fig. 3.11, which possesses 2×2 bits of resolution. Considering the sign bits, it is indeed a 2×3-bit modulator. The switch arrays are implemented in a pseudo-differential configuration. The differential design of transistor switch arrays affords several advantages over the single-ended version:

1. It dramatically reduces the second harmonic distortion. As an example, based on simulation results for the single-ended power cells, the second harmonic distortion is approximately -24 dB while, for the differential counterpart, it is better than -60 dB;

2. It doubles the output power. Moreover, due to differential generation of quadrature clocks employing differential DCO and dividers, if they are implemented as single-ended digital power cells, then the I/Q modulator wastes more power. As a result, the system efficiency will be diminished;

3. It is also more tolerable to common-mode noise through the supply and substrate coupling. Furthermore, the supply and ground bond-wire inductance have less impact on the power cells. Consequently, the ripple and instability are substantially reduced. In addition, the supply and ground bond-wire would not affect the power combining network. Most importantly, the differential configuration eases the oscillator's injection pulling and pushing phenomena;

4. It eliminates the requirement of bulky on-chip DC current choke. The reason lies in the fact that the differential drain currents are pulled from the common supply voltage in which they tend to cancel each other. As a result, the inductance of the passive current source does not require to be very high.

The dI and dQ signals drive the gates of the switch array transistors. When the I (or Q) code is kept constant while the Q (or I) code is varying, the conductance of the switches changes and, consequently, the amplitude and phase of the composite RF output also change. In addition, when both the I and Q codes change, the amplitude and phase of the RF output change due to the orthogonality. The size of the transistor switch is W/L=(64× 0.96 μm)/(0.12 μm). The length of the switches are designated as twice the minimum feature

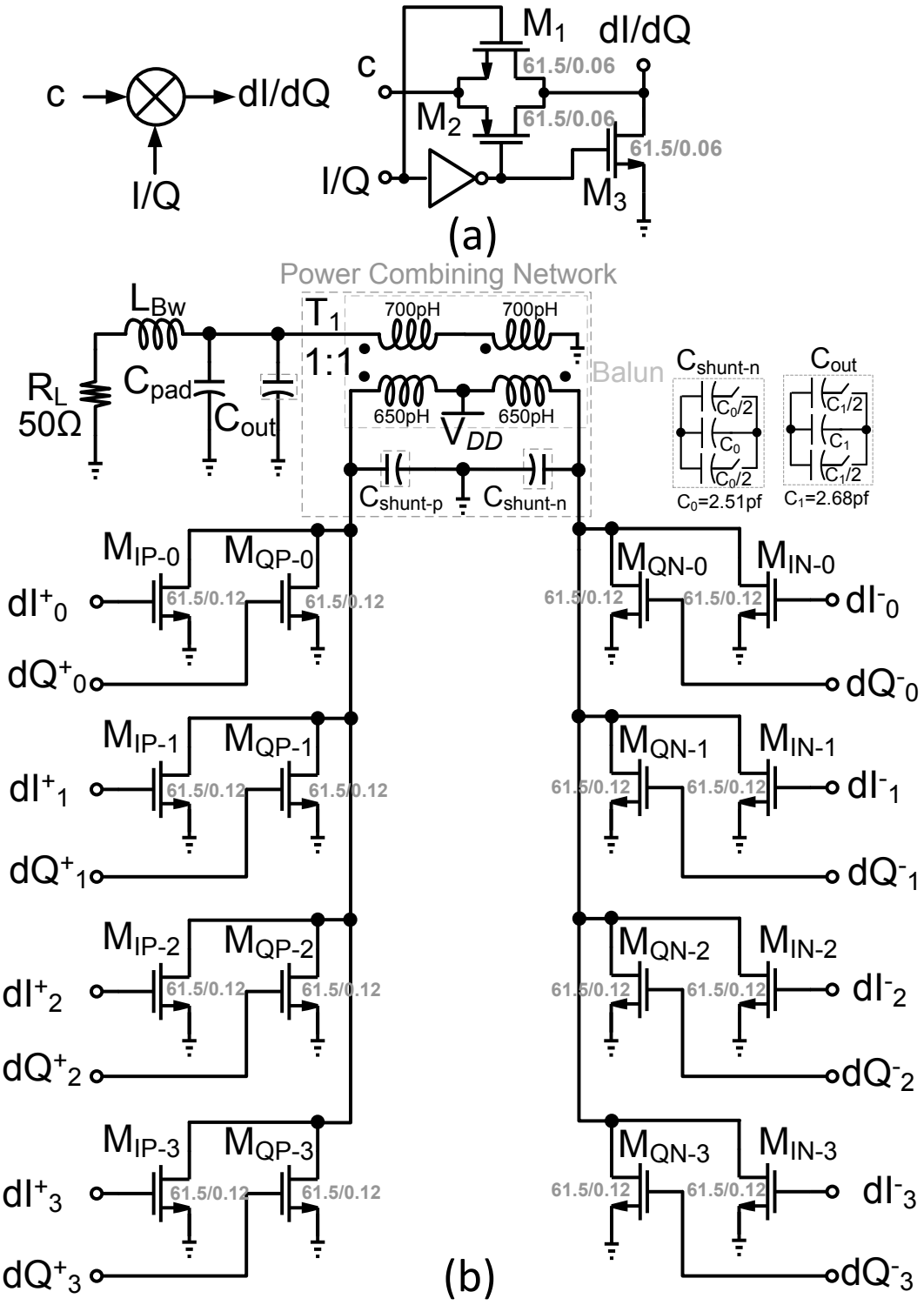

Figure 4.6: Schematic of (a) implicit mixer unit; (b) 2×2-bit switch array banks.

length of the corresponding process technology to ensure good matching. The disadvantages are diminished output power, larger clock buffers, and more occupied area.

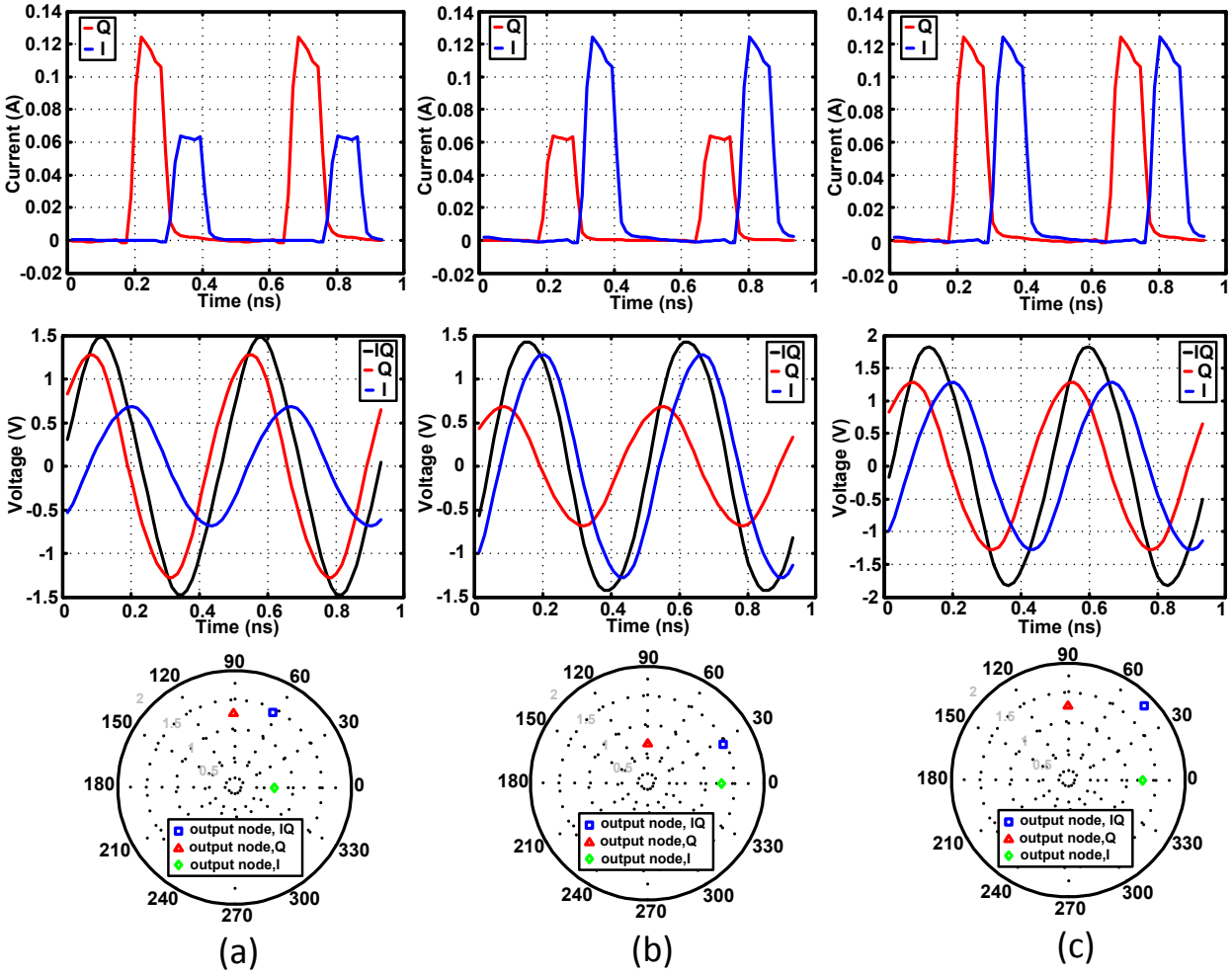

Figure 4.7: Plots of drain current (top row), output voltage (middle row), and related constellation points (bottom row) for the codes of: (a) (Q, I) = (1,0.5); (b) (Q, I) = (0.5,1); (c) (Q, I) = (1,1).

To confirm the correct operation of the modulator, three simulations are performed for three different I/Q codes which include (I,Q) = (1, 0.5), (0.5, 1), and (1, 1), respectively. Fig. 4.7 exhibits simulated drain currents of $M_{IP-0...3}$ and $M_{QP-0...3}$ transistors of Fig. 4.6 with corresponding output voltages and the related constellation points of the RF output. The corresponding phasors of the constellation points are $1.43\angle 63.06°$, $1.46\angle 27.22°$, and $1.81\angle 44.5°$ versus the expected $1.43\angle 63.44°$, $1.43\angle 26.57°$, and $1.81\angle 45°$, thus demonstrating the appropriate basic operation of the digital I/Q modulator. In addition, recall that Fig. 3.11(c) illustrates the post-layout simulation results of the 64-point digital modulator. The highest output power is 14.26 dBm and the related calculated EVM with no digital predistortion is 4.83%, according to (1.3).

The transistor switch arrays are connected at the output to the power combining network, which will be thoroughly explained in Chapter 6. It comprises the balun transformer

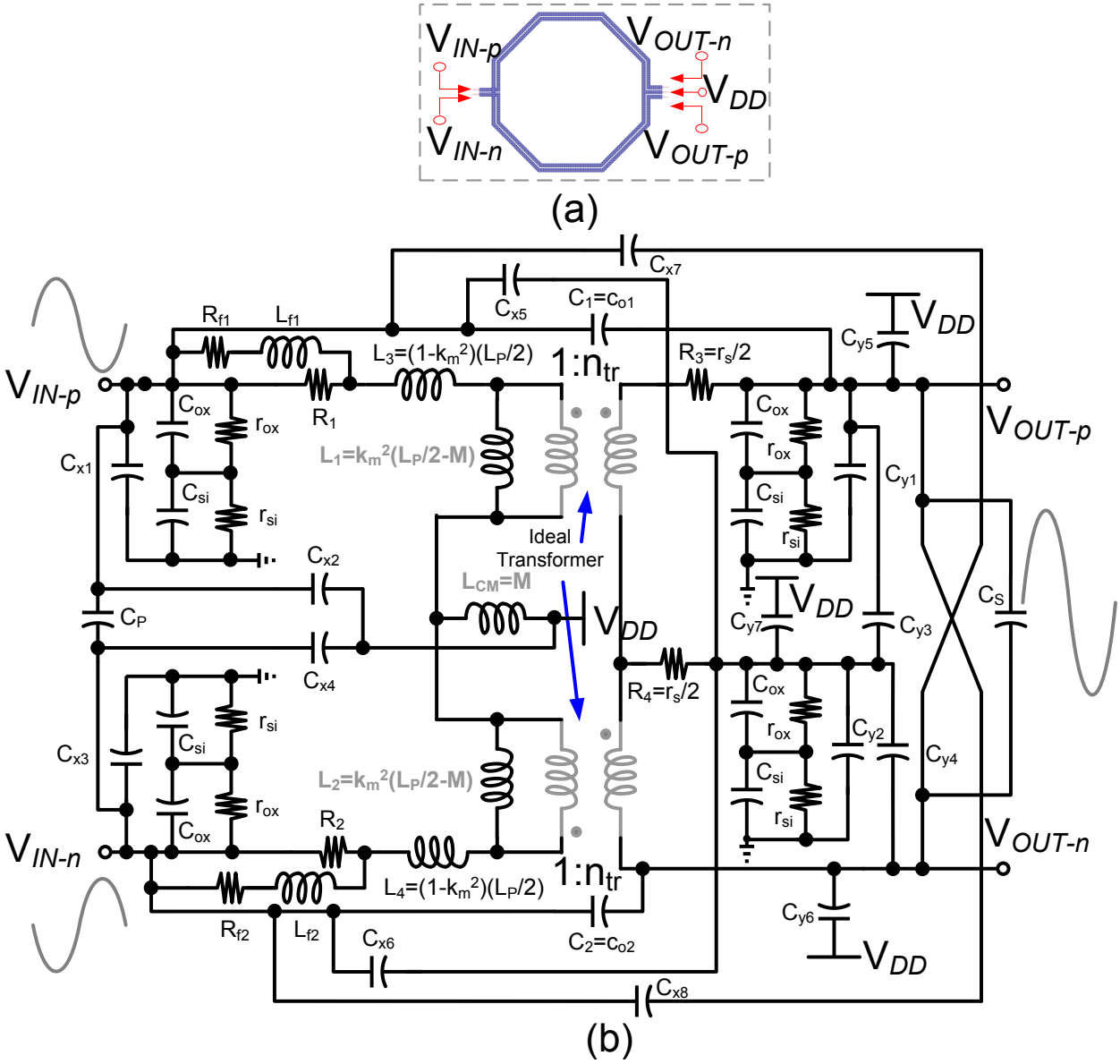

Figure 4.8: (a) Layout of balun; (b) corresponding lumped equivalent circuit.

T_1 with input $C_{shunt-p}$, $C_{shunt-n}$ and output C_{out} tuning capacitors. As will be clarified in Chapter 6, the shunt input and output capacitances of the power combiner are employed to fine-tune the amplitude and the phase relationship of the I/Q signal as well as the output power at 2 GHz. These capacitances consist of a fixed component part (with values of C_0, C_1) and a tuning component part (with values of $C_0/2$, $C_1/2$), which are tuned utilizing NMOS switches. The size of NMOS switches should be carefully selected since it affects the quality factor and, consequently, the insertion loss of the power combining network. The shunt input and output capacitances are realized as fringe interdigitated capacitors which use metal layers one through seven of our selected technology to improve the capacitor density

per unit area.

The layout of the balun transformer T_1 is depicted in Fig. 4.8(a). T_1 is utilized to convert the differential signals to a single-ended output. It impacts the modulator performance and, hence, requires special attention to its layout. The balun transformer uses metal layers 6 and 7 as well as an aluminum layer for decreasing losses due to the series resistance. The transformer traces are $12\,\mu$m wide for maximizing the current handling capability and with $3\,\mu$m gaps between them which imposes by metal density rule of the process technology. The total size of the transformer is $500\times500\,\mu\text{m}^2$ with a 1:1 turns ratio (with center tap). The size is selected to be large enough to address the frequency range of 1 GHz to 3 GHz. The transformer layout has been simulated employing ADS Momentum$^{\text{TM}}$. The resulting S-parameter model has been converted to an equivalent lumped circuit model [77] that is used in the time-domain circuit simulations. However, the equivalent lumped circuit is a modified version of [77], which is exhibited in Fig. 4.8(b). In this modified equivalent lumped model, the mutual inductance between two primary differential legs of the balun is included. Therefore, by using the T-section model for the primary side, the magnetizing inductor is:

$$L_{pm} = k_m^2 \times \left(\frac{L_p}{2} - M\right) \tag{4.1}$$

where M is mutual inductance, L_P is self-inductance of the primary winding [77], and the related coupling factor of the transformer is $k_m = 0.65$. Moreover, in this model, all of the parasitic capacitances between the six ports (two inputs, two outputs, V_{DD}, and ground) of the balun are included. In addition L_{f1}, R_{f1}, and L_{f2}, R_{f2} are parallel to R_1, and R_2, respectively, which could model the metal skin effect or frequency-dependent substrate losses. Fig. 4.9(a) and Fig. 4.9(b) compare the simulation results between the Momentum S-parameter and the equivalent lumped model for the primary and secondary inductance and series loss resistance versus frequency of the balun transformer. According to Fig. 4.9(a)-(b), the equivalent lumped model coincides favorably with the Momentum simulation results. Based on simulation results, the insertion loss of balun is approximately 1.7 dB which causes the drain efficiency of the modulator to drop from almost 33% to about 21%. It should be mentioned that, in Fig. 4.6(b), the R_L is connected to the power combining network via a bond wire inductor(L_{BW}). In addition, the effect of capacitance of the RF pad (C_{pad}) should be considered. The effect of these extra passive components is simulated for 1 to 5 GHz frequency range, and the corresponding load reflection coefficient (Γ_L) is shown in Fig. 4.9(c). Based on simulation results, if $L_{Bw} = 1\,nH$ (which is a typical value for 1-mm-long bond-wire) and $C_{pad} = 376\,fF$, then $Z_L = 53\angle0\,\Omega$, as a result, the corresponding Γ_L, the related voltage standing wave ratio (VSWR), and its return loss (RL) are 0.029, 1.06, and 30.71, respectively. This slight deviation from the ideal $50\,\Omega$ has a very minimal effect on the functionality of the power combining network. Thus, the modulator enjoys the small VSWR, and its performance of the RF power, efficiency, and modulation accuracy will not be diminished. However, as will be discussed in Chapter 6, in the design steps of power

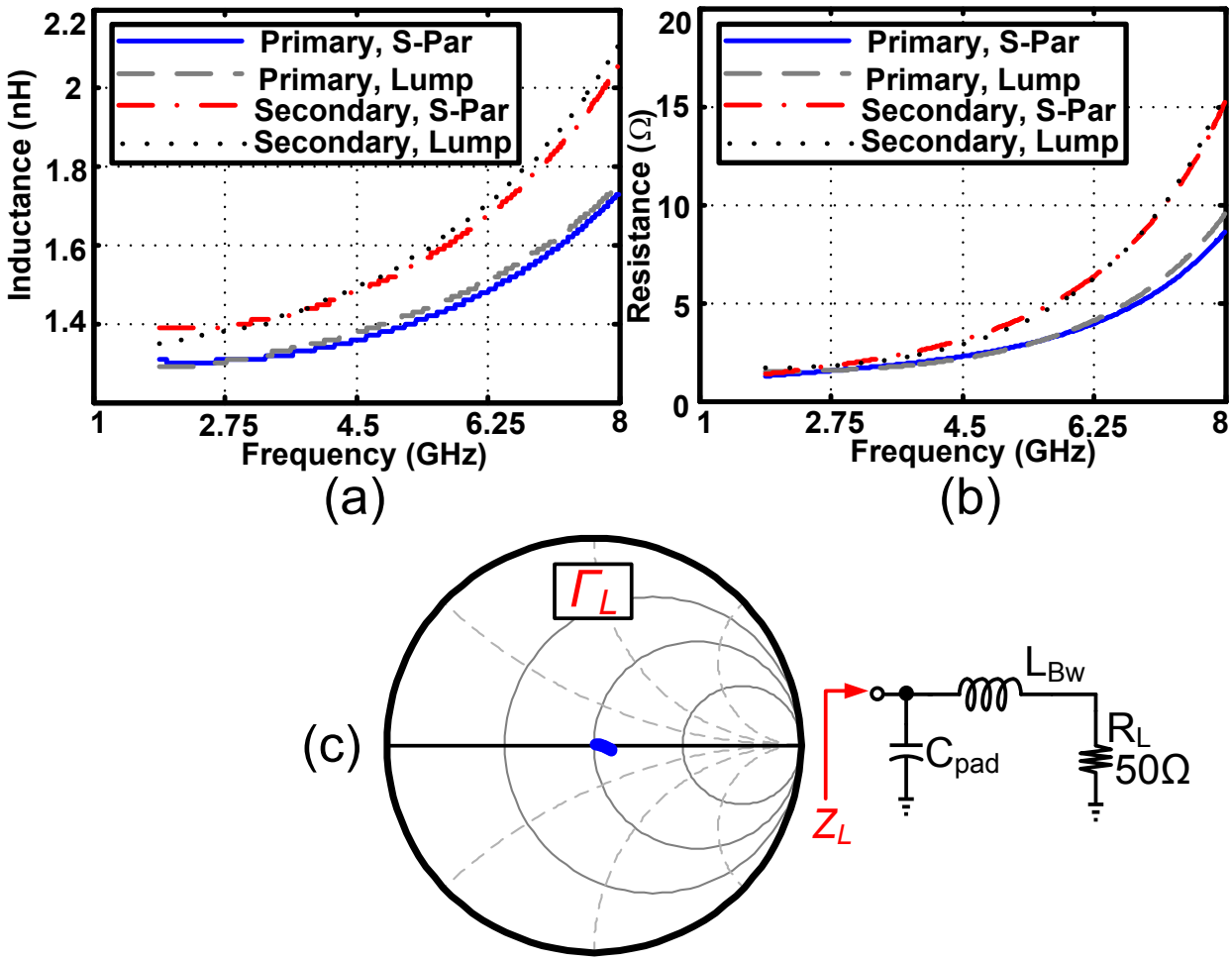

Figure 4.9: (a) Primary and secondary inductance; (b) primary and secondary loss resistance; (c) load reflection coefficient of Z_L in 1 to 5 GHz frequency range.

combining network, C_{pad} is considered as parts of C_{out}.

4.2 Measurement Results

As an experimental validation of the proposed orthogonal I/Q combining concept, a 2×3-bit (including one sign bit) direct-digital I/Q modulator circuit is fabricated in 65 nm CMOS technology. Fig. 4.10(a) exhibits the micrograph of the implemented chip. The total chip area is $1.2\times2\,\text{mm}^2$ with an active part of $0.6\times1.15\,\text{mm}^2$. The chip is mounted on a FR4 PCB board (see Fig. 4.10(b)) and all of the pads, including two RF pads (16 GHz input clock reference and 2 GHz RF output), are wire bonded. The test board is designed such that very short bond-wires could be utilized for all RF signals as well as for supply and ground connections.

The chip height is approximately 600 μm, and it is placed into a designated hole on

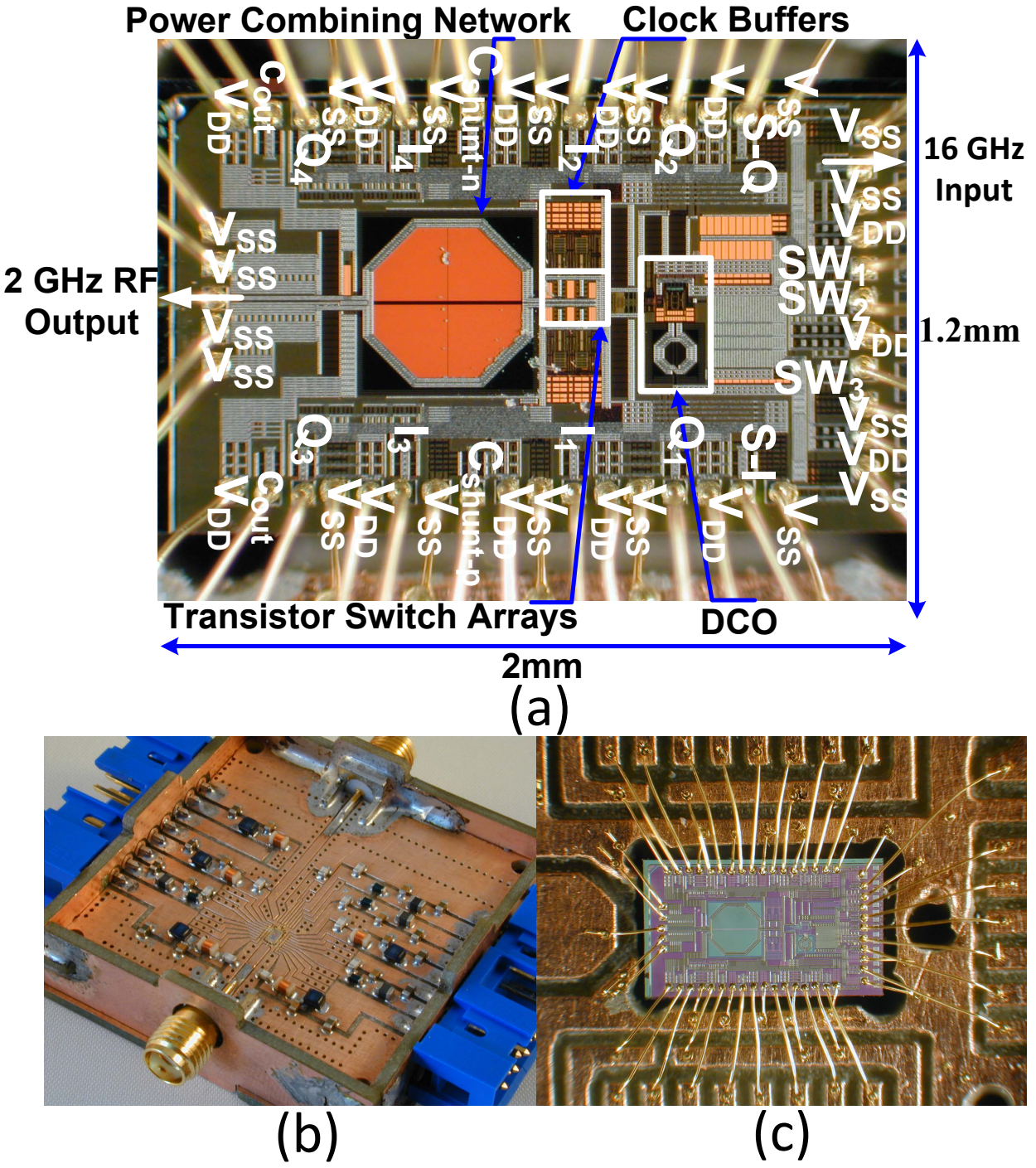

Figure 4.10: (a) Micrograph of the 2×3-bit-bit, 2 GHz all-digital I/Q modulator including 8 GHz DCO; (b) FR4 PCB board; (c) mounted chip.

the FR4 board which results in even shorter bond-wires (see Fig. 4.10(c)). For the correct operation of electrostatic discharge (ESD)[2] protection circuits, digital control bits are surrounded by ground and supply pads. In addition, as depicted in Fig. 4.10(a), SW_1, SW_2,

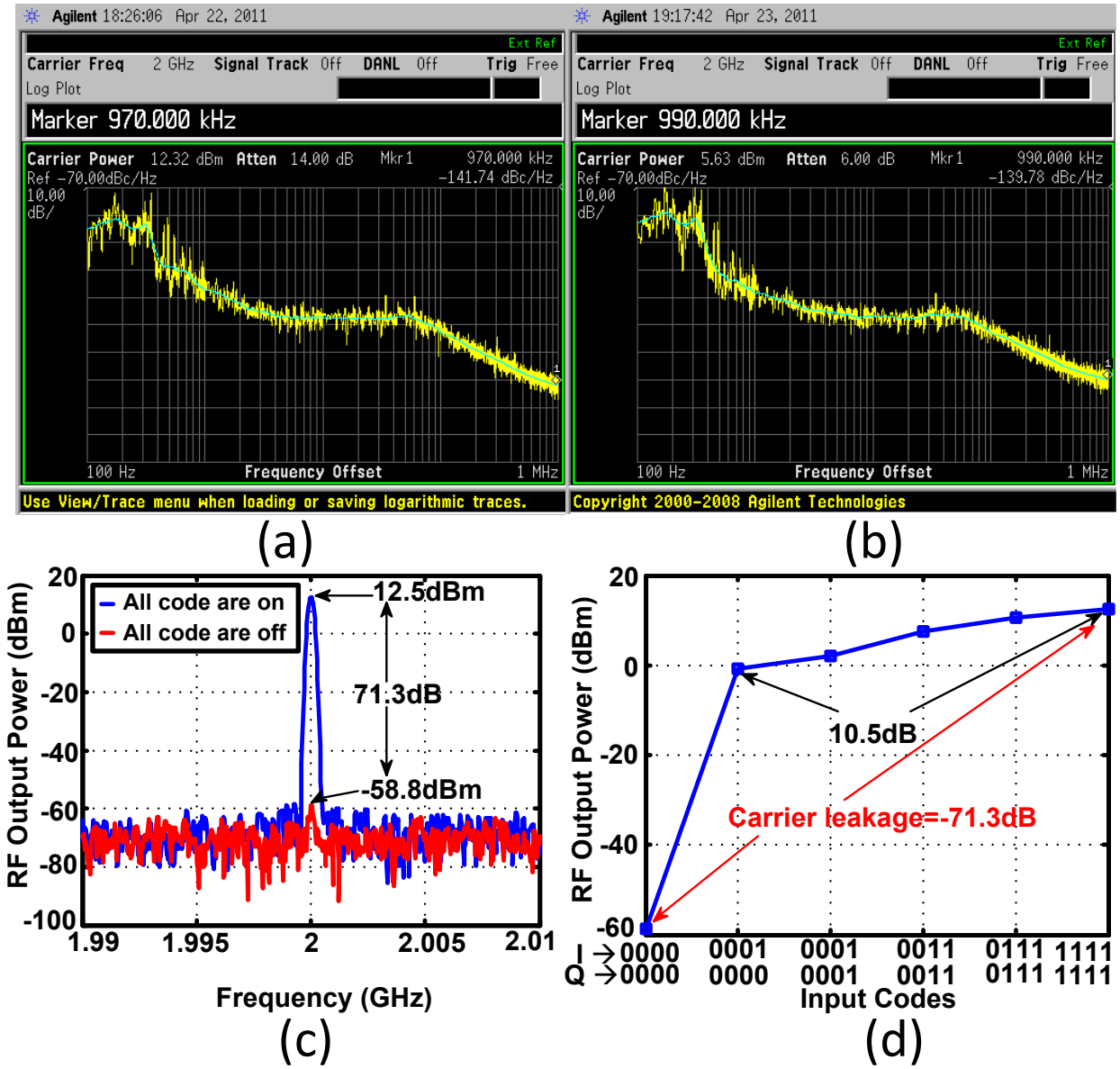

Figure 4.11: Phase noise of injection-locked RF output at 2 GHz; (a) at 12.32 dBm; (b) at 5.63 dBm. Measured (c) output power spectrum; (d) output power versus input codes.

and SW_3 are the digital control frequency bits of the DCO. Also $C_{shunt-p}$, $C_{shunt-n}$ and C_{out} of Fig. 4.6(b) are used for tuning the power combining network. Moreover, the I/Q baseband digital control bits are S-Q, S-I, Q_1, I_1, Q_2, I_2, Q_3, I_3, Q_4, and I_4. During the measurement process, these digital baseband bits are purposely and statically switched on and off in order to address a desired constellation point.

At the start of the measurements, the chip is first injection locked to a 16 GHz ref-

[2]Courtesy of our group's technical supporter, Atef Akhnoukh. The ESD and related circuits have been designed and laid-out by him from scratch.

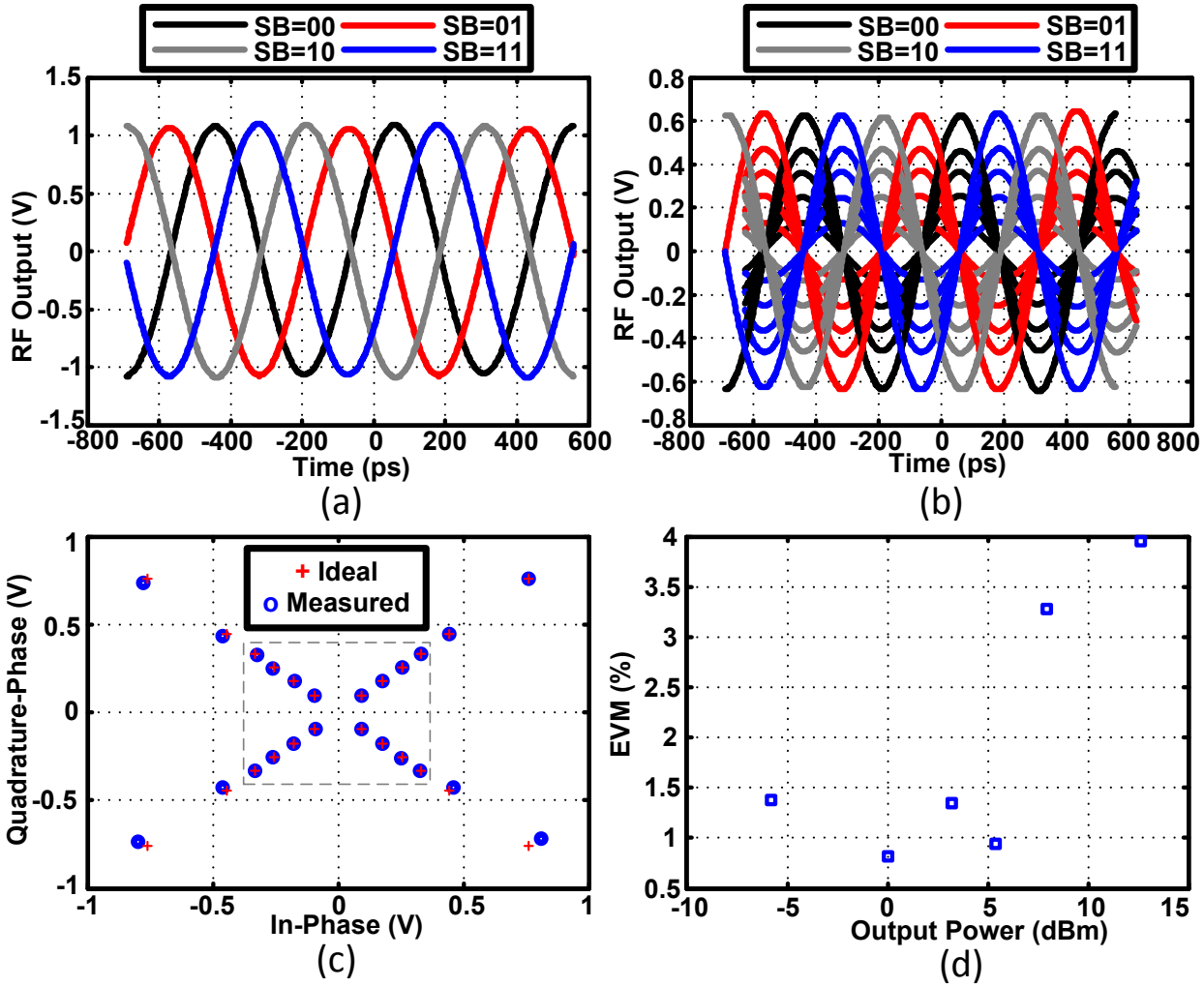

Figure 4.12: Measured time-domain 4-QPSK (a) phase changing; (b) amplitude changing; (c) corresponding constellation points; (d) corresponding EVM.

erence signal source. Fig. 4.11(a)-(b) illustrates the resulting phase noise spectrum of the modulator output while the DCO is injection-locked to 16 GHz reference signal source. The measured phase noise are demonstrated at two different output power levels of 12.32 dBm and 5.63 dBm. For both cases, the measured phase noise at 1 MHz offset is approximately -140 dBc/Hz. The DC drain current of the transistor switch arrays is 60 mA at the maximum measured output power of 12.32 dBm. Note that after de-embedding the 0.3 dB loss of the SMA cable as well as board losses, the output power is actually 12.62 dBm. Consequently, the related drain efficiency is 20% (V_{DD} = 1.4 V), which is considered excellent from the I/Q RF modulator perspective. Fig. 4.11(c) indicates the highest output power and carrier leakage superimposed. The carrier leakage is -71 dBc below the peak output power. In Fig. 4.11(d), the variation of the output power versus the I/Q codes is plotted, which indicates the 10.5 dB dynamic range of the modulator. Note that this value is in accordance with

the modulator resolution of 2 bits when the supply is kept constant. Since the carrier leakage is less than -58 dBm, it affords the opportunity to increase the resolution of the modulator to a higher number of bits in a rather unambiguous manner. In fact, the dynamic range is now exceeding 70 dB (dynamic range = maximum power (12.62) - minimum power (-58)). Therefore, the resolution could be extended to more than 11 bits ($11 \times 6 = 66 \leq 70$). Note that the post layout simulated carrier leakage was approximately -70 dBm. The difference between the simulation and measurement could be a result of coupling between the clock traces, the drain nodes, and the digital/RF ground plane.

The implemented modulator is tested in two different constellation modes, specifically, in quadrature phase-shift keying (QPSK) and 64-point quadrature amplitude modulation (QAM). For both of these measurements, time domain RF output signals are captured and saved. Fast Fourier Transform (FFT) of these signals is subsequently calculated, and the amplitudes and phases are plotted. In the QPSK mode, by statically changing the sign bits, the phase of the RF signal can be adjusted by 90° (see Fig. 4.12(a)). In addition, by increasing the I/Q code from the lowest to the highest, the modulator amplitude is also changed, which is exhibited in Fig. 4.12(b). The corresponding constellation points and the related EVM are shown in Figs. 4.12(c)-(d), which indicate that, for the output power less than 6 dBm the EVM is less than 1.5% in QPSK modes of operation. Note that, to show the functionality of the proposed digital I/Q RF modulator, with this measurement, only six different QPSK points within each quadrant are measured[3].

As a final point, Fig. 4.13 shows the modulator performance in 64-QAM constellation mode. The measured time-domain of three different points in each of the four quadrants (12 points in total) are demonstrated in Figs. 4.13 (a)-(d). These points are (I, Q) = (1,4), (I, Q) = (2,2), and (I, Q) = (4,1), respectively. The corresponding constellation points are depicted in Fig. 4.13(e), which are designated by a white "x" that establishes the correct operation of the modulator. The entire 64-QAM constellation diagram is indicated in Fig. 4.13(e). The maximum output power in this case is 6 dBm while $V_{DD} = 1$ V and the corresponding maximum drain efficiency is 10%. The related EVM is 2.36% or, equivalently, -32.53 dB, without using any pre-distortion, which is a favorable number. It should be mentioned that the constellation diagram will be easily improved in more advanced implementations when exploiting a higher output resolution (see Chapter 7). In this case, the pre-distortion techniques can be implemented in an uncomplicated manner. Fig. 4.13(e) reveals that the first and third quadrants of the constellation diagram exhibit improved behavior over the other two quadrants. This is due to the mismatch between the clock paths of the four transistor switch arrays.

The measurement results of 2×3-bit digital I/Q RF modulator are summarized in Table 4.1. Note that, as will be discussed in Chapter 6, Section 6.2, the peak drain efficiency of the proposed I/Q RF-DAC while operating at full RF power should be more than 40%. Based

[3]For the output power higher than 6 dBm, $V_{DD} = 1.4$ V and for the remaining, $V_{DD} = 1$ V.

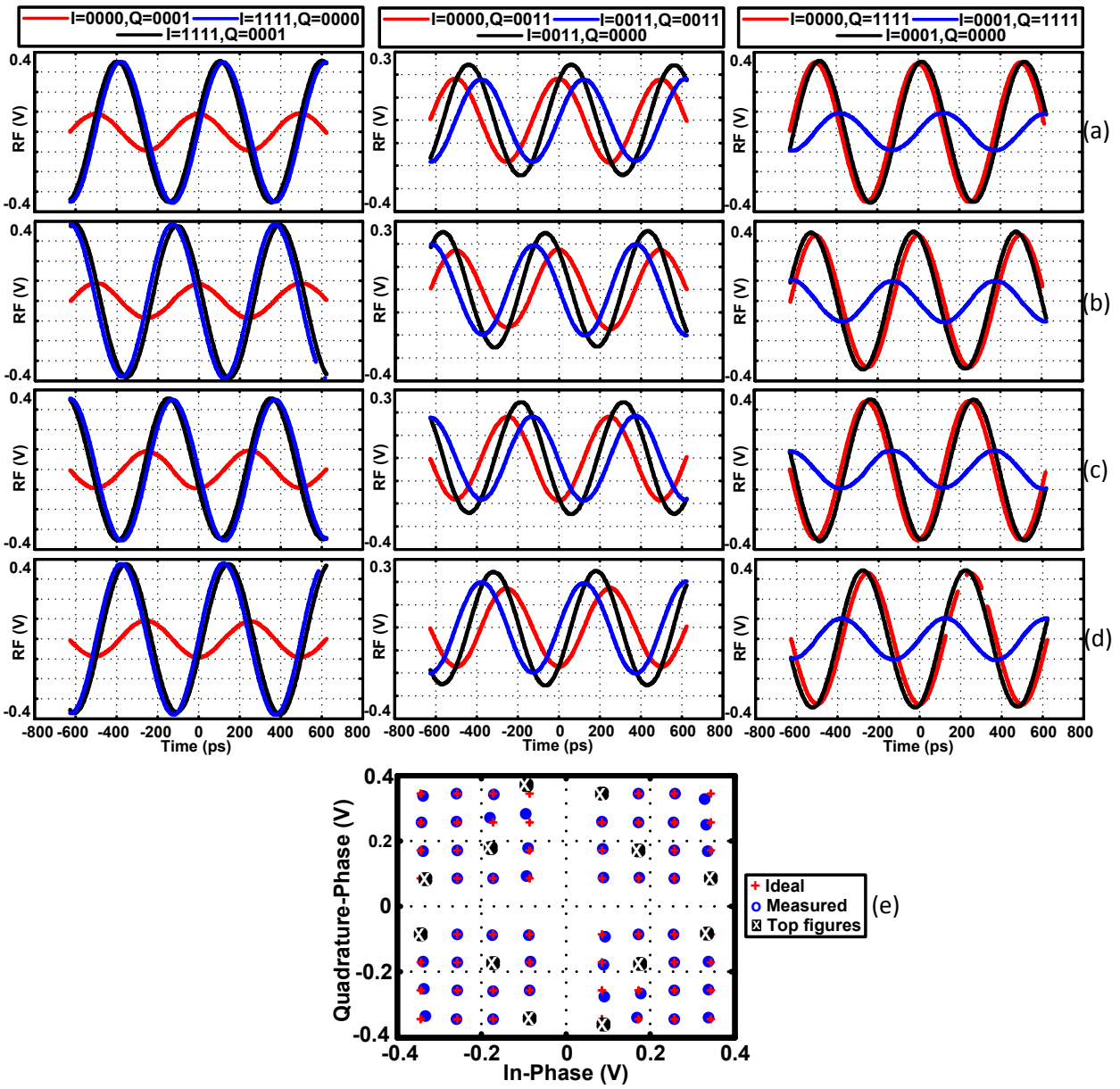

Figure 4.13: Measured time-domain (a) 1^{st}; (b) 2^{nd}; (c) 3^{rd}; (d) 4^{th} quadrant;(e) corresponding measured 64 points I/Q constellation diagram at 2 GHz.

on Table 4.1, however, the drain efficiency of the contemporary I/Q RF-DAC, i.e. [69], at 12.6 dBm RF power is approximately 20%. The foregoing efficiency drop is regarded to the fact that the transistor length of the switch arrays is selected 120 nm which entails more power losses. Moreover, the designated power combining network could not transform the optimum loading condition at the drain nodes of the related switch arrays. In order to improve the efficiency, in the next I/Q RF-DAC test chip, which will be elaborated in more detail in Chapter 7, these oversights are addressed. In addition, employing an ultra thick metal layer, the insertion loss of the balun transformer is reduced. Thus, the achievable

Table 4.1: 2×3-bit digital I/Q RF modulator

	Process (nm)	**Output Power (dBm)**	**Carrier Leakage (dBc)**	**Drain Efficiency (%)**	**EVM (%)**
All-Digital I/Q RF-DAC [69]	65	5.4	-71	10	0.94[1]
		12.6		20	3.95[2]
		5.4		10	2.36[3]

[1] Only 4-point (QPSK) is considered, which is based on Fig. 4.12(c).
[2] Only 4-point (QPSK) is considered, which is based on Fig. 4.12(c).
[3] Only 64-point (64-QAM) is considered, which is based on Fig. 4.13(e).

drain efficiency is increased up to 40%.

4.3 Conclusion

In this chapter, a novel 2×3-bit all-digital I/Q (i.e., Cartesian) RF transmit modulator is implemented which operates as an RF-DAC. The modulator performs based on the concept of orthogonal summing, which is introduced and elaborated in Chapter 3. It is based on a TDD manner of an orthogonal I/Q addition. By employing this method, a very simple and compact design featuring high-output power, power-efficient and low-EVM has been realized. The resolution of the experimental RF-DAC presented in this work is only 3-bit (including one sign bit), but it will be demonstrated in the following chapters that the resolution can be increased to 8–12 bits in an unequivocal manner for utilization in multi-standard wireless applications.

Chapter 5

Towards High-Resolution RF-DAC: The System Design Perspective

The all-digital *orthogonal* I/Q modulator concept of Chapter 4 [67–69] substantiates that the direct orthogonal summation of the in-phase and quadrature digital RF vectors can generate the composite IQ RF vectors. According to Chapter 4, a 2×3-bit static I/Q implementation could achieve a maximum RF output power and drain efficiency of 12.6 dBm and 20%, respectively, while the corresponding RF supply voltage is 1.4 V. Moreover, its related static EVM of "4QPSK" symbols is -28.6 dB at maximum RF power. In addition, the measured static constellation diagram of Fig. 4.13(e) demonstrates certain mismatches between differential quadrature paths of Fig. 3.11(a) due to either mismatches between the 25% duty cycle differential quadrature clocks of I_P, Q_P, I_N, and Q_N or an insufficient symmetrical layout. Furthermore, the differential drain nodes of the switch array structure of Fig. 4.6(b) would not tolerate more than 1.3 V differential voltage swing employing low-power 65-nm CMOS technology and, as a result, their corresponding NMOS transistor switches would definitely break. Note that the maximum RF power using the switch array structure of Fig. 4.6 is 14 dBm. Likewise, the digital I/Q modulator has only been tested at an RF frequency band of 2 GHz. The ultimate universal digital I/Q transmitter would operate in multiple RF bands to support multi-mode/multi-band communication standards.

The above disadvantages of the digital I/Q modulator of Chapter 4 must be addressed. Most importantly, the dynamic performance of the proposed digital I/Q modulator employing the actual wideband complex baseband signals has yet to be examined. Since the effective modulating sample resolution is an utmost important parameter as it directly impacts the achievable dynamic range, linearity, EVM, noise floor and out-of-band spectral emission,

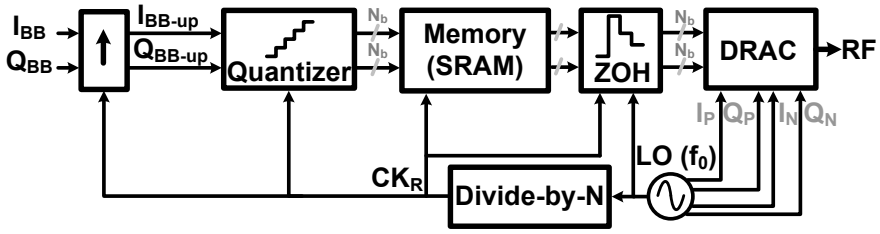

Figure 5.1: System level simulations at f_0=2.4 GHz:the block diagram of the test-bench.

we recently proposed an all-digital I/Q RF-DAC with 2×13-bit resolution that can provide output power beyond 22 dBm [70, 71]. Due to its high efficiency, wide bandwidth, high functionality and fine resolution, while requiring only limited chip area, the proposed solution is a very promising candidate for future multi-mode/multi-band transmitters. As stated in Chapter 1, Section 1.3.2, the dynamic performance of the RF-DAC can be evaluated employing EVM for in-band performance and spectral purity as well as noise floor at RX frequency bands for out-of-band performance. In order to address the aforementioned issues, in this chapter, the system design perspective of the 2×13-bit RF-DAC is elaborated in more detail. The circuit level design considerations as well as digital calibration along with associated digital predistortion techniques, and measurement results will be addressed in the following chapters (Chapters 6, 7, and 8). Section 5.1 systematically explains the proposed high resolution RF-DAC and investigates its system design parameters. The conclusion of the chapter is drawn in Section 5.2.

5.1 System Design Considerations

The dynamic performance of the all-digital I/Q RF-DAC strongly depends on the interpolation rate of the I_{BB-up}/Q_{BB-up} signals and their resolution. Since, in this prototype, the digital signal processing and the I/Q baseband interpolations are performed in MATLAB^{TM} and subsequently uploaded into two on-chip static random access memory (SRAM) via universal asynchronous receiver/transmitter (UART), see also Appendix A.1, the memory length (SRAM capacity) also affects the RF-DAC performance. Fig. 5.1 illustrates the system-level simulation setup structure that reflects the dependency of these parameters on its dynamic performance. First, I_{BB} and Q_{BB} are interpolated in software by a CK_R clock, which is generated by an integer-N division of the RF carrier LO clock. Thus, the CK_R clock and the baseband upsampled signals are synchronized to the LO clock. Next, I_{BB-up} and Q_{BB-up} are quantized and then uploaded into the SRAM memory. Subsequently, the SRAM memory is read out employing a CK_R clock and directly fed to the DRAC block. Since the CK_R is slower than the LO clock, the DRAC performs as a ZOH to balance the speed of baseband upsampled signals with the LO clock. For the sake of signal processing clarity, ZOH is exhibited as a separate block between the memory and the DRAC. Note

that all subsequent simulations based on Fig. 5.1 are performed under an assumption that the DRAC resolution is identical to that of the quantizer; the carrier frequency (f_0) is 2.4 GHz. As a result, three yet-to-be-defined variables in the RF-DAC system of Fig. 5.1 are:

1. CK_R frequency (f_{CKR})
2. DRAC resolution (N_b)
3. memory length (l_{mem})

which should be appropriately selected. The f_{CKR} lower limit is determined by the highest operational bandwidth of I_{BB}/Q_{BB}. At present, the bandwidth of baseband communication signals does not exceed 160 MHz. On the other hand, the f_{CKR} upper limit could be as high as f_0. Note that, in this case, the divide-by-N would be redundant. In reality, running the CK_R at the LO rate would consume an overabundance of power, thus reducing the overall system efficiency. In fact, according to equation (1.2) in Chapter 1, the relationship between the system efficiency and f_{CKR} is as follows:

$$\begin{aligned} \eta_{system} &= \frac{P_{RF-out}}{P_{DC-drain} + P_{DC-4\times} + P_{DC-Buffer} + P_{DC-CKR}} \\ &= \frac{P_{RF-out}}{P_{DC-drain} + P_{DC-4\times} + P_{DC-Buffer} + V_{DD}^2 \times A \times C_{par} \times f_{CKR}} \end{aligned} \tag{5.1}$$

where A is the circuit activity factor and C_{par} is the related total parasitic capacitances of the baseband processing circuit. Moreover, $P_{DC-4\times}$ and $P_{DC-Buffer}$ are the DC power consumption of a clock generation circuit and clock buffer which drive digital switch arrays of the RF-DAC, respectively. As a result, the system efficiency is inversely proportional to f_{CKR}. For example, in this aspect, the power consumption of the SRAM at 300 MHz is 12 mW. The $P_{DC-4\times}$=36 mW and $P_{DC-Buffer}$=84 mW at 2.4 GHz. Moreover, $P_{DC-drain}$=396 mW and the corresponding RF power is 22 dBm. Consequently, η_{system}=30%. If SRAM hypothetically works at 2.4 GHz, then its related power consumption will be 96 mW while $P_{DC-Buffer}$=150 mW. Note that the power consumption of $P_{DC-Buffer}$ is due to the contribution of the CK_R in DRAC structure. Hence, η_{system}=23.3%.

Fig. 5.2 exhibits the simulations for which f_{CKR} is swept from 150 to 600 MHz in increments of 150 MHz while I_{BB}/Q_{BB} are 64-tone/80 MHz signals. The subsequent RF power spectrum is shaped by the Sinc function of the ZOH interpolation:

$$Sinc(f) = \text{sinc}^2\left(\frac{f - f_0}{f_{CKR}}\right) \tag{5.2}$$

The ZOH operation creates spectral replicas at multiples of sampling frequency f_{CKR} away from the f_0 carrier:

$$f_n = f_0 \pm n \times f_{CKR} \tag{5.3}$$

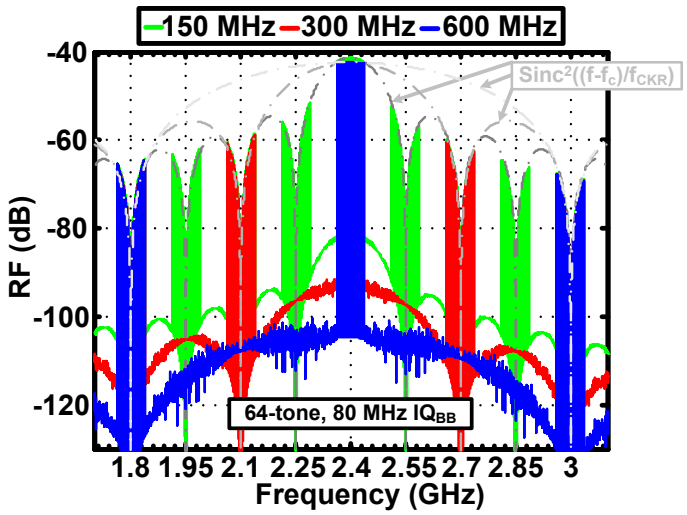

Figure 5.2: System level simulations at f_0=2.4 GHz: Sweeping over upsampling clock frequency f_{CKR} for 64-tone, 80 MHz I_{BB}/Q_{BB} baseband signals.

where $n = 1, 2, ...$ In conclusion, the upsampling and synchronization operations represent a ZOH that performs as a sinc-filter with its corresponding zeros located at f_n. As such, the spectral images are notched by the ZOH operation. Note that doubling f_{CKR} not only reduces the out-of-band emissions but also lowers the spectral replicas by 6 dB. If f_{CKR} is 150 MHz, then it would be impractical to support the 160 MHz baseband signals. On the other hand, 600 MHz clock consumes twice as much power than at 300 MHz. Furthermore, SRAM in a low-power 65 nm CMOS process would not be feasible at 600 MHz. Therefore, f_{CKR} is selected 300 MHz that is generated employing a $\div 8$ divider.

Another simulation is performed by sweeping the bandwidth (two-tone frequency spacing) of I_{BB}/Q_{BB} from 20 MHz to 80 MHz. According to Fig. 5.3(a), the "wider band" signals produce higher out-of-band spectra, while the spectral replicas are larger (6 dB/octave). This is merely the limitation of the present implementation and is entirely due to the limited sample-storing memory relative to the signal period.

Fig. 5.3(b) further illustrates that doubling l_{mem} improves the noise floor, although this would not be a limitation in practical transmitters. Since, in this work, the upsampled baseband signals residing in SRAM are fed to DRAC, this configuration performs as an FFT executor. Consequently, the higher number of FFT points result in the lower out-of-band spectrum. In this work, however, l_{mem} is selected 8-kword (every word is 16 bits) to save the chip area. We should emphasize that the SRAM storage of modulating samples was chosen over a real-time reception of the baseband data in order to emulate the environment of contemporary single-chip radios in which the the RF transceiver is integrated with the digital baseband. This provides the benefit of avoiding contamination of the sensitive RF spectrum from the wideband modulating digital data through bond pads, bond-pad wires, and an ESD ring. Nonetheless, the limitations of utilizing on-chip SRAM in combination

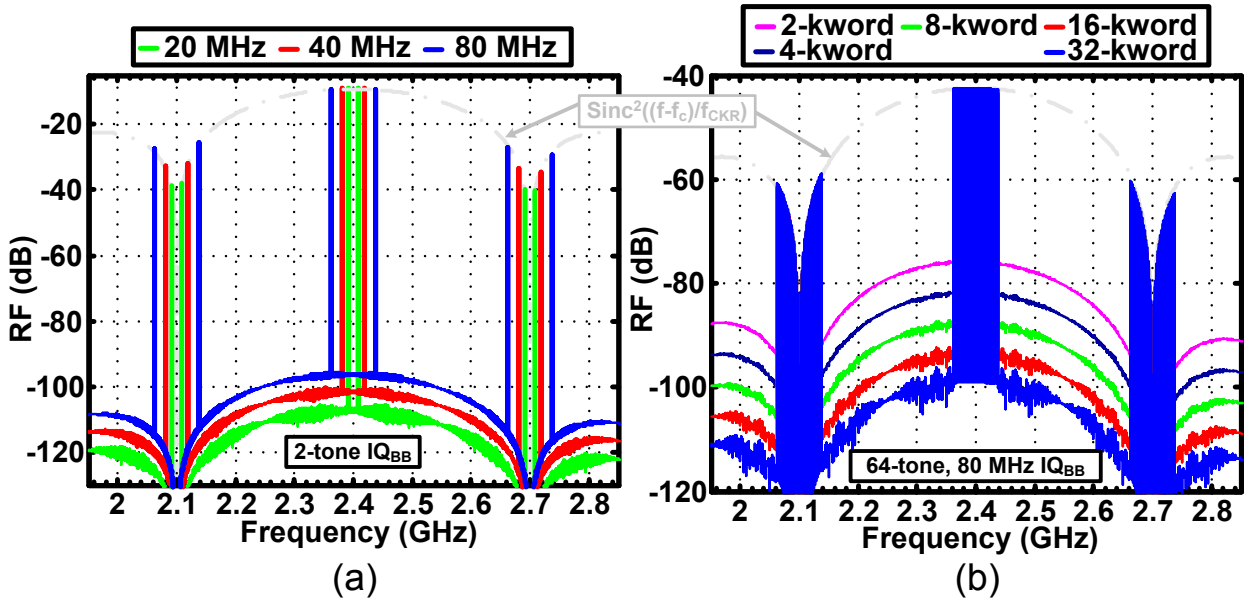

Figure 5.3: System level simulations at f_0=2.4 GHz:(a) signal bandwidth (two-tone frequency spacing); (b) SRAM memory length (l_{mem}=8-kword).

with MATLAB in comparison with an actual situation can be explained as follows:

The SRAMs must be large enough to preserve the necessary baseband data. The memory length, l_{mem}, affects the following dynamic performances of the proposed I/Q RF-DAC:

1. As previously stated, utilizing SRAM with larger memory length improves the out-of-band spectrum. It also affects the far-out noise performance.

2. In order to produce accurate DPD profiles, the SRAM should be at least 16 k-word. This will be explained in Chapter 7, Subsection 7.9.4.

As a result, l_{mem} collectively with the corresponding upsampling clock, CK_R, of the SRAM are two important design parameters. The reason can be attributed to the subsequent resolution bandwidth of RF-DAC depending on l_{mem} as well as the CK_R. Since, in each period of CK_R clock, one data point is fed into the RF-DAC, consequently, the total resolving time of the baseband data as well as its related resolution bandwidth are expressed as follows:

$$T_{resolve} = l_{mem} \times \frac{1}{f_{CKR}} \tag{5.4}$$

$$RBW = \frac{1}{T_{resolve}} \tag{5.5}$$

For example, in this work, since the carrier frequency, f_0, is 2.4 GHz, then the frequency of the upsampling clock, f_{CKR}, is 300 MHz. Also, l_{mem}=8 k-word. Thus, the resolving baseband time and its corresponding resolution bandwidth are 27.3 μs and 36.6 kHz, respectively. Hence, the resolution bandwidth of the measured out-of-band spectrum as well

as the far-out noise performance of the current RF-DAC is limited to 36.6 kHz. Stated differently, to measure the far-out noise performance with the resolution bandwidth of 1 Hz while employing 300 MHz clock, the subsequent memory length should be 300 M-word. In fact, this hypothetic SRAM would occupy a prohibitively immense chip area. Moreover, it consumes exorbitant amount of power and, thus, it is avoided. In conclusion, in order to measure RF-DAC out-of-band spectrum as well as far-out noise performance while its related resolution bandwidth is low enough, the most beneficial manner is to perform the measurement in the real-time test setup.

As discussed earlier, the lower limit of N_b is determined by (3.1). However, it should be much higher than that in order to meet the quantization noise requirements of practical communication standards. Thus, as with any DAC converter, increasing N_b improves the dynamic range of RF-DAC. Note that the dynamic range of the RF-DAC for a single-tone baseband signal can be expressed as the SNR expression of the DAC [78] [79] [80] that is as follows:

$$DR(f)_{ST}|_{f_{CKR}/2} = 1.7609 + 6.0206 \times N_b + 20\log_{10}\left(\text{sinc}\left(\frac{f - f_0}{f_{CKR}}\right)\right) \tag{5.6}$$

in which equation (5.6) indicates the dynamic range of RF-DAC in the Nyquist band from 0 to $f_{CKR}/2$. Note that the final term in equation (5.6), i.e. "sinc function" is a result of the ZOH operation of the RF-DAC. Moreover, the dynamic range of a single-tone baseband signal in 1-Hz bandwidth is as follows:

$$DR(f)_{ST}|_{Hz} = DR(f)_{ST}|_{f_{CKR}/2} + 10\log_{10}\left(\frac{f_{CKR}}{2}\right) \tag{5.7}$$

Equation(5.7) and also Fig. 5.2 indicate that doubling the sampling clock frequency, i.e. f_{CKR}, improves the dynamic range by 3 dB. In addition, for a modulated or multi-tone signal with the peak-to-average power ratio (PAPR), its dynamic range of in 1-Hz bandwidth could be rewritten as

$$DR(f)_{MT}|_{Hz} = DR(f)_{ST}|_{Hz} - 10\log_{10}\left(\frac{PAPR}{2}\right) \tag{5.8}$$

where PAPR is as follows

$$PAPR = \frac{P_{RF-max}}{P_{RF-avg}} \tag{5.9}$$

where P_{RF-max} and P_{RF-avg} are maximum and average RF power, respectively. If the input signal is a single tone, then PAPR=2 and then equation (5.7) and (5.8) will be identical. Note that, in this thesis, only two complex-modulated baseband signals are employed: single-carrier M-QAM and multi-carrier M-QAM orthogonal frequency-division multiplexing (OFDM) signals. Under the assumption of equal probability of occurrence for all levels, the PAPR of a single-carrier 64 and 256-QAM signals are 3.7 and 4.2 dB, respectively [80,81][1].

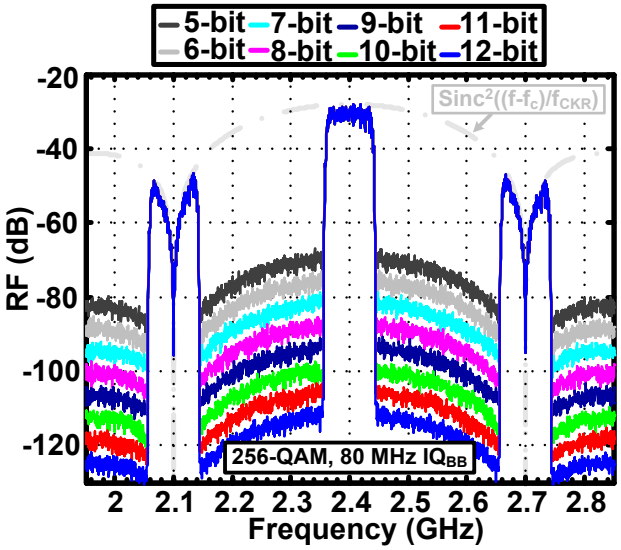

Figure 5.4: System level simulations at f_0=2.4 GHz: DRAC resolution ($N_b = 12$).

Moreover, the PAPR of multi-carrier 64 and 256-QAM OFDM signals are 17.2 and 20.6 dB[2], respectively [24,80,82]. According to equation (5.8), employing the aforementioned complex-modulated baseband signals deteriorates the dynamic range of the RF-DAC. In reality, due to the fact that the maximum achievable power mode of operation is only minimally incorporated, the hard-clipping algorithm could be utilized to decrease the PAPR of the OFDM signal [83]. In this work, however, due to employing SRAM, the complex-modulated baseband signals are windowed (filtered). As a result, as will be demonstrated in Chapter 8, Section 8.3, the PAPR of applied complex-modulated signals will not exceed more than 8.6 dB.

Note that, generally, the dynamic range of modulated/multi-tone signal in B-Hz bandwidth can be expressed as:

$$DR(f)_{MT}|_B = DR(f)_{MT}|_{Hz} - 10\log_{10}(B) \tag{5.10}$$

The RF-DAC resolution of Fig. 5.1 is swept for a single-carrier "256-QAM 80 MHz" signal and the corresponding power spectral density of the RF-DAC system is depicted in Fig. 5.4. Based on Fig. 5.4 and equation(5.6), each extra bit improves the out-of-band spectrum by almost 6 dB. In this work, N_b is selected as 13 bits (the most significant bit (MSB) is the sign bit) to support the most stringent communication standards.

[1]Assuming the equal probability for all QAM constellation points, then its PAPR is equal to $10\log_{10}3 + 10\log_{10}\left(\sqrt{M}-1\right)/\left(\sqrt{M}+1\right)$. Consequently, if $M \to \infty$ then PAPR$\to 10\log_{10}3$=4.77.

[2]The related sub-carriers (N_{sb}) are 52, and 115, respectively and the PAPR is calculated based on $10\log_{10}(N_{sb})$.

As stated previously, the TX noise floor at RX frequency bands is another important out-of-band performance of a digital transmitter. The TX noise floor is almost dominated by the related noise of the I/Q RF modulator. The noise floor specification is dictated by the following items [6, 7, 24, 25, 60, 61, 84]:

1. How much of the TX noise floor can be leaked to RX frequency bands in order not to desensitize the receiver of the corresponding radios? Otherwise stated, the TX noise floor should be smaller (at least 9 dB) than the sensitivity of the receiver. Namely

$$\begin{aligned} N_{TX}|_{B,Hz} &\leq P_{sen}|_{dBm} \\ &\leq (10\log_{10}(KT) + 30_{dB}) + NF + 10\log_{10} B + SNR_{min} \\ &\leq -173.83_{dBm/Hz} + NF + 10\log_{10} B + SNR_{min} \end{aligned} \tag{5.11}$$

   where KT is "available noise power" when the receiver is matched to the antenna and the temperature is 300°K, NF is the noise figure of the receiver, B is the bandwidth of interest, and SNR_{min} is the minimum SNR ratio of the receiver. As a result, the required TX noise floor with respect to the maximum RF output power, which is the negate of the dynamic range (5.8), is as follows:

$$N_{TX}|_{dBc/Hz} = -DR(f)_{MT}|_{Hz} = N_{TX}|_{B,Hz} - (P_{TX,Max} - L_{duplexer}) \tag{5.12}$$

   where $P_{TX,Max}$ is the peak RF output power and $L_{duplexer}$ is the duplexer isolation loss. For example, with a typical number of NF=3 dB and $L_{duplexer}$=45 dB as well as $P_{TX,Max}$=22 dBm, the required TX noise floor must be less than -148 dBc/Hz. If, in the proposed RF-DAC, N_b=12 bit, f_{CKR}=300 MHz, and PAPR=9 dB are selected, then these choices ensure that the TX noise floor will not desensitize the receiver.

2. The spectral emission mask of the corresponding communication standard must be satisfied so as not to corrupt the adjacent as well as alternate frequency channels of operation. For example, WCDMA standard emission mask [24] establishes that, at 12 MHz offset from the center of the transmission channel, the related emitted signal must be less than -63 dBm in a 100-kHz bandwidth which is equal to -135 dBc/Hz considering 22 dBm RF output power.

3. It is common in contemporary mobile devices to incorporate the other applications such as Bluetooth, GNSS, FM, and wireless LAN as well as other cellular standards in combination with the designated cellular system. This is referred to as co-existence of various radios on the same mobile devices. For example, in order to comply with the 3GPP co-existence standards, the TX noise at 40 MHz offset should be less than -79 and -71 dBm in a 100-kHz bandwidth in the GSM RX bands of 900 and 1800 MHz, respectively [24]. Stated differently, the TX noise floor at the foregoing RX frequency

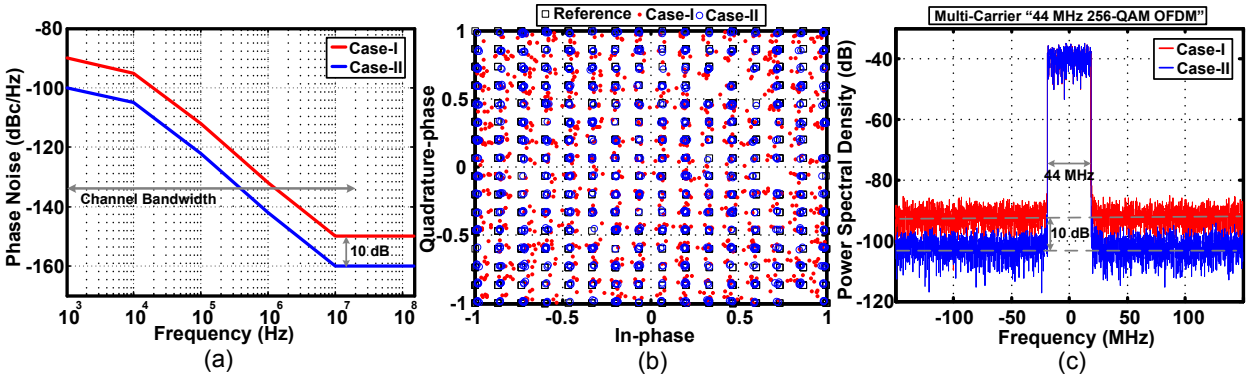

Figure 5.5: (a) Two different phase noise profiles; (b) In-band performance, EVM_{case-I}=-23.5 dB, $\text{EVM}_{case-II}$=-34.5 dB; (c) Out-of-band spectra, case-II is 10 dB better than case-I.

bands should be -162 and -151 dBc/Hz considering maximum RF power of 33 and 30 dBm, respectively.

As stated in Chapter 1, EVM is related to the in-band performance of the transmitter. The modulation accuracy of a transmitter is verified by EVM. Equivalently, at the receiver, the modulation error is validated employing BER. The SNR ratio of the quadrature baseband signals are inversely proportional to EVM [85]:

$$SNR_{M-QAM}|_{dB} \cong -PAPR_{dB} + 20\log_{10}\left(\frac{EVM_{\%}}{100}\right) \Rightarrow SNR_{M-QAM} \approx \frac{1}{EVM^2} \tag{5.13}$$

Moreover, in-phase and quadrature-phase gain and phase mismatches, oscillator phase noise, and in-phase and quadrature-phase DC offset deteriorate the performance of the transmitter EVM. The proposed 2×13-bit RF-DAC guarantees that the SNR is high enough. Furthermore, as illustrated in Fig. 5.1 and will be discussed in Chapter 7, utilizing divide-by-N as well as a master divide-by-4 ensure maintaining the quadrature accuracy of the digital I/Q modulator. In addition, employing an IQ image and leakage calibration techniques entail minimal gain/phase mismatches as well as moderate IQ DC offset. Furthermore, as will be addressed in the following chapters, the RF-DAC requires a DPD algorithm that also improves EVM. As a result of IQ image and leakage calibrations, the EVM is mostly affected by the phase noise of upconverting quadrature clocks. The EVM and phase noise are approximately related to one another as follows [86, 87]:

$$EVM_{dB} \cong PN_{dBc/Hz} + 10\log_{10}(BW_{channel}) + 3.01_{dB}|_{SSB\rightarrow DSB} \tag{5.14}$$

where the right-hand side of eq. (5.14) is, indeed, double-sideband integrated phase noise over the desired channel bandwidth. The effect of phase noise on the in-band performance, i.e., EVM, as well as output-of-band spectra are depicted in Fig. 5.5. The performance of I/Q RF-DAC systematically simulated employing two different phase noise profiles of Fig. 5.5(a)

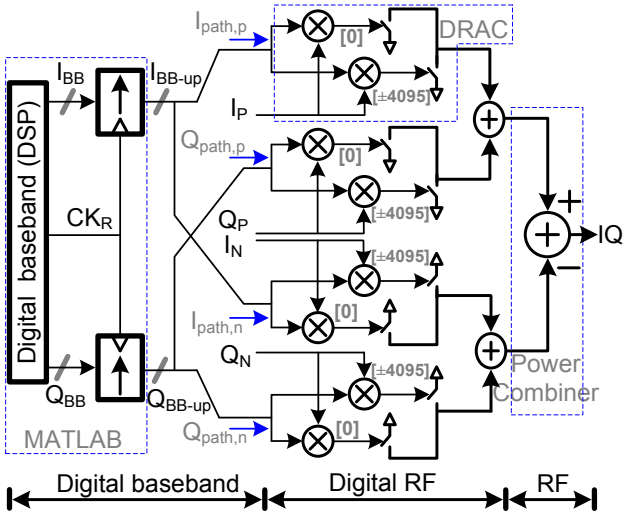

Figure 5.6: The differential orthogonal 2×13-bit all-digital I/Q RF-DAC.

while their I/Q baseband signal is a multi-carrier "44 MHz 256-QAM OFDM". Their related EVMs as well as out-of-band spectra are approximately separated by 10 dB which is, literally, the difference between the related phase noise profiles.

Finally, Fig. 5.6 exhibits the complete block diagram of the differential orthogonal 2×13-bit all-digital I/Q RF-DAC. It comprises four paths: $I_{path,p}$, $Q_{path,p}$, $I_{path,n}$, and $Q_{path,n}$. Each path contains a DRAC comprising unit cell mixers and an array of digital power amplifiers (DPAs). The multitude of DPA outputs are connected to a differential power combing network that promotes transformation of the upconverted digital signals into a "high power" continuous-time RF output in an energy efficient manner. The represented RF-DAC does not require the baseband DACs of a conventional analog I/Q transmitter. Moreover, I/Q calibration can be easily performed at baseband while its bandwidth is only limited by the speed of the digital circuitry and the passive output power combiner.

5.2 Conclusion

The system design considerations of the proposed high-resolution, wideband all-digital I/Q RF-DAC are discussed. It is demonstrated that the upsampling clock frequency (f_{CKR}), DRAC resolution (N_b), and memory length (l_{mem}) are three important parameters that affect the dynamic performances of the proposed RF-DAC. Based on system level simulation results and the limitation in implementing the RF-DAC test-chip, they are designated as f_{CKR}=300 MHz, N_b=12 bit, and l_{mem}=8 k-word. The effect of these parameters on the in-band as well as out-of-band performance of RF-DAC are investigated. It is concluded that exploiting 12 bits of resolution for quadrature baseband signals is sufficient to meet the most stringent communication requirements.

Chapter 6

Differential I/Q DPAs and The Power Combining Network

Within the past decade, tremendous research has been directed towards the design of power efficient on-chip combining networks. For example, Aoki *et al.* proposed a distributed active transformer (DAT) topology which makes it possible for watt-level power generation in CMOS bulk technology for mobile and wireless applications [8–10]. In addition, Gang Liu *et al.*, Haldi *et al.*, and Chowdhury *et al.* proposed transformer-based power combining techniques that enhance the efficiency at power back-off levels [88–90]. Moreover, Hua Wang *et al.* revealed a power amplifier that also employs transformer-based matching network to generate high power as well as to achieve broadband operation [91]. These novel, well-cited papers indicate that it is possible to implement a fully integrated power efficient RF transmitter which generates the desired RF power level without utilizing any external passive components. Though these power amplifiers have successfully generated the desired RF power using transformer-based power combiners, they have not been implemented along with the entire RF transmitter. Most recently, Kousai *et al.* unveiled an analog polar RF transmitter based on a power mixer array structure, which also uses power combining for watt-level power generation [15]. Moreover, Chowdhury *et al.* and Lu *et al.* proposed inverse class-D power combiners for polar RF-DACs [19, 21, 48, 49]. Furthermore, Yoo *et al.* employs a class-D type power combiner for switched-capacitor digital polar transmitter [18]. Similarly, Chao Lu *et al.* also demonstrated an inverse class-D power combiner for an I/Q RF-DAC [66].

Considering the advantages as well as disadvantages of the foregoing power combiners, in this chapter, the design procedures of the proposed differential I/Q class-E based power

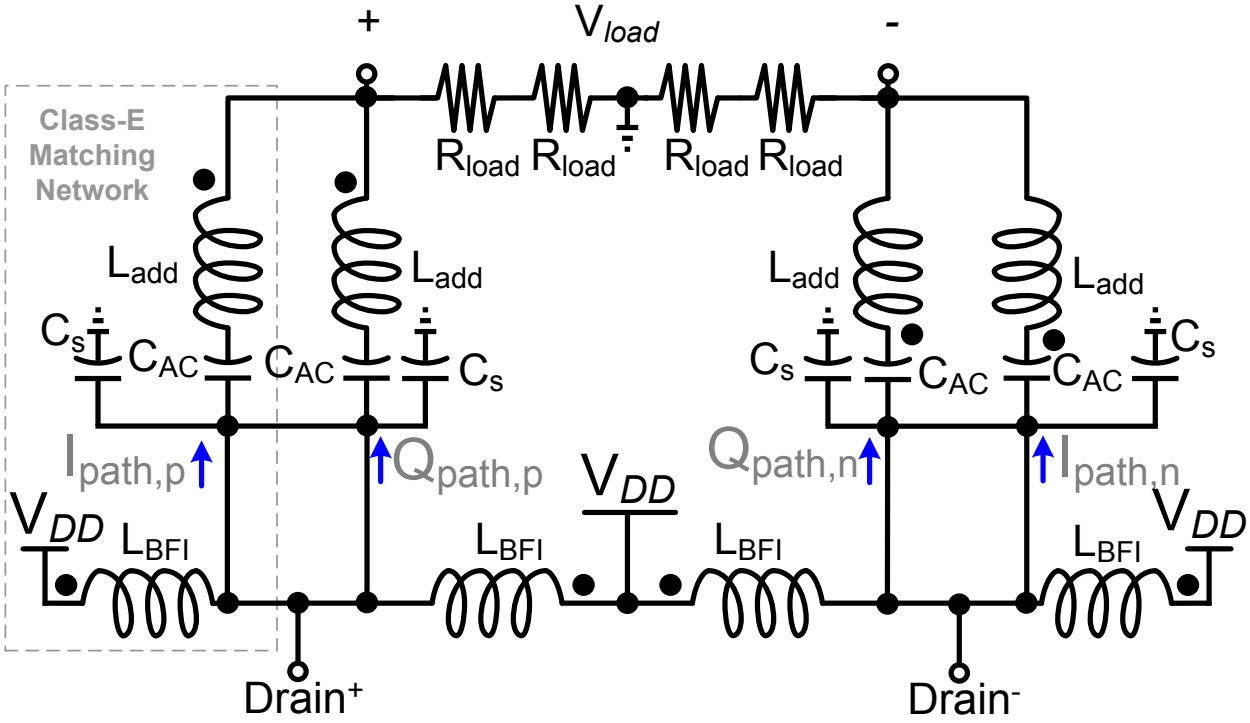

Figure 6.1: Schematic diagram an idealized power combining network.

combining network will be discussed [70, 71]. Section 6.1 introduces two DRAC topologies, namely DRAC based on an AND-Gate mixer (see Fig. 6.2(a)) and DRAC based on a switchable cascode structure (see Fig. 6.2(b)). An idealized power combining network is revealed which can be employed in either of the two DRAC structures. Section 6.2 discusses a differential power combiner which is designed according to the class-E matching configuration at full power. Section 6.3 discusses the related efficiency of the power combining network. Section 6.4 explains the effect of timing constraints of upconverting clock on the RF-DAC performance. Section 6.5 discloses that the RF-DAC operates as a class-B power amplifier at back-off power levels. Section 6.6 explains a procedure to design an efficient transformer which is employed in the power combiner. Finally, in Section 6.7, the chapter is concluded.

6.1 Idealized Power Combiner With Different DRACs

As stated previously in Chapter 3 (Section 3.2), the orthogonality and summation of the I_{path} and Q_{path} in Fig. 3.2 are two important aspects of the quadrature modulation (see equation (3.4)). It was later concluded that by employing 25% quadrature clocks, the vectorial addition of the I_{path} and Q_{path} is simply performed by electrical summing (Fig. 3.9). Nonetheless, the proposed all-digital high resolution I/Q RF-DAC of Fig. 5.6 should generate the desired RF power and, most importantly, must be power efficient. The on-chip differential power

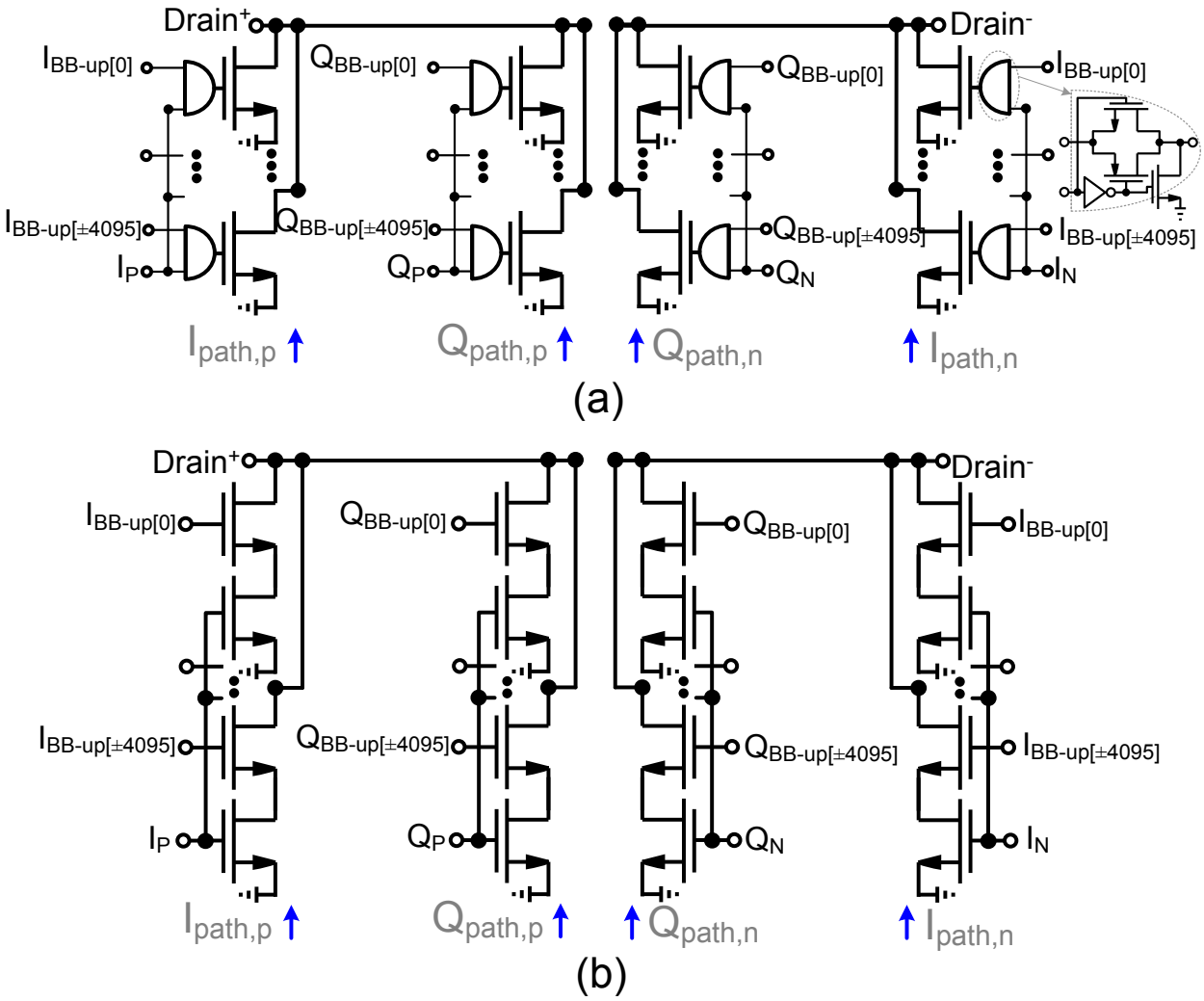

Figure 6.2: Schematic diagram the 2×13-bit differential I/Q power switch array : (a) simple DPA (Chapter 4); (b) switchable cascode DPA structure.

combining network of Fig. 5.6 performs the efficient RF power combination of $I_{path,p}$, $Q_{path,p}$, $I_{path,n}$, and $Q_{path,n}$.

Fig. 6.1 exhibits an idealized power combining network which could be connected to either of the following two DRAC structures:

1. According to Fig. 6.2(a), the DRAC is a pseudo-differential quadrature structure, in which each path comprises unit cell mixers (AND gates), and the composite DPA consists of the parallel combination of 4096 single transistor units. Hence, its resolution is 2×12 bits. This DRAC structure is incorporated into the 2×2-bit digital I/Q modulator of Chapter 4 (see Fig. 4.6) and is referred to as a single-switch DRAC structure;

2. Based on Fig. 6.2(b), the DRAC is a pseudo-differential quadrature structure, in which

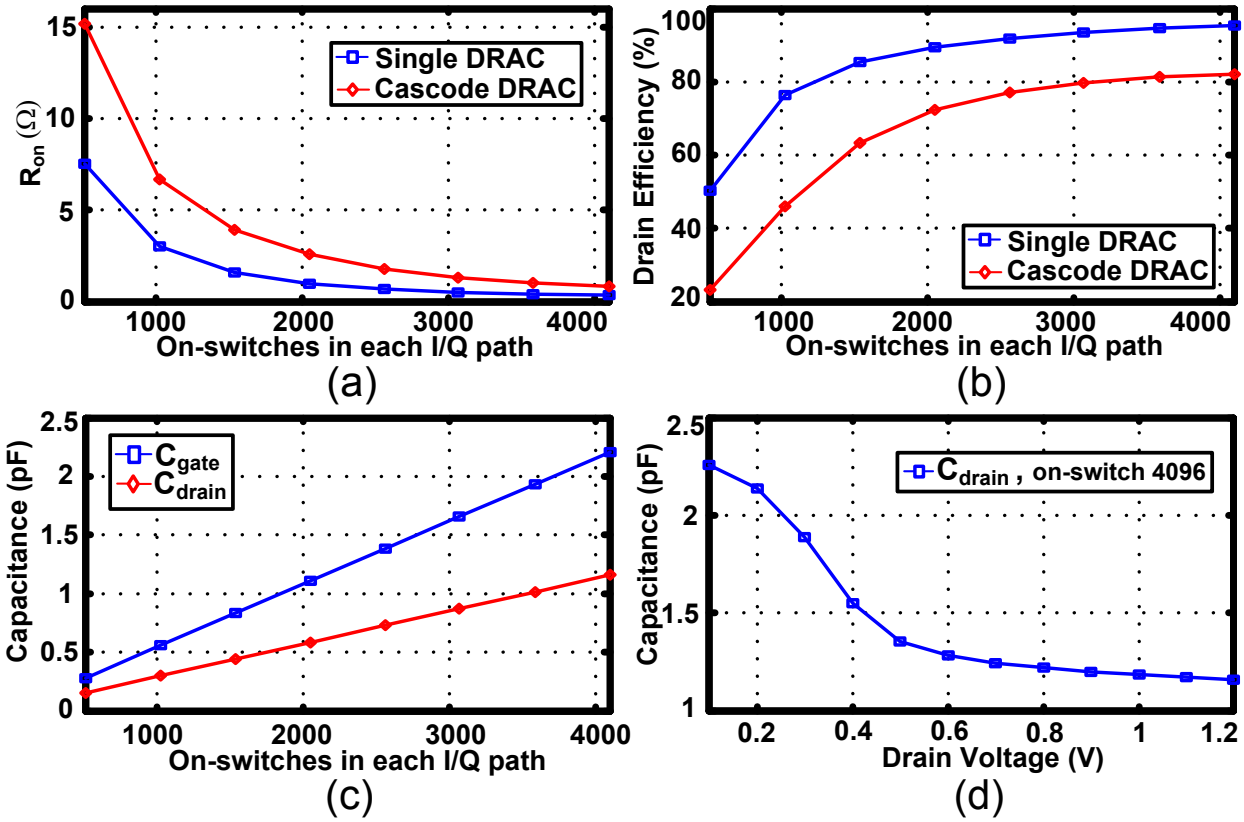

Figure 6.3: Simulations of each I/Q path for (a) R_{on}; (b) drain efficiency; (c) gate/drain capacitance versus on-switches; and (d) drain capacitance versus drain voltage.

each path is composed of unit cell mixers (switchable cascode transistor), and the composite DPA consists of the parallel combination of 4096 switchable cascode transistor units. Thus, its resolution is also 2×12 bits. Note that it is, indeed, a 2×13-bit considering the sign bits. This structure is referred to as switchable cascode DRAC structure.

The peak voltage swing of $Drain^{+}$ and $Drain^{-}$ nodes could be more than 2.4 V which can cause a device breakdown if the switchable cascode DRAC structure is not utilized. Using the switchable cascode as a unit cell, however, increases the on-resistance (R_{on}) of the unit cell switches (see Fig. 6.3(a)) which subsequently incites higher power loss as well as lowered drain efficiency. Note that all simulations of Fig. 6.3 are performed employing matching network of Fig. 6.1 with a single/cascode unit cell switches using a channel length of 60 nm while its gate width is 500 nm. As stated, the DRAC resolution is 12 bits which requires 4096 switch-array unit cells in each orthogonal path of $I_{path,p}$, $Q_{path,p}$, $I_{path,n}$, and $Q_{path,n}$. In this work, the targeted maximum RF output power (P_{max}) exceeds 22 dBm while maintaining V_{DD} at 1.2 V. Therefore, the maximum RF power of each orthogonal path should be 1/4 of P_{max}. According to simulations, using W=500 nm minimum-length

switches in 12-bit RF-DAC configuration ensures that each orthogonal path provides more than 16 dBm.

Fig. 6.3(b) indicates that the drain efficiency of the cascode switch is lower than that of a simple switch due to its higher R_{on}. In this simulation, the power combining network of Fig. 6.1 is lossless, which would result in 100% drain efficiency if R_{on} was, hypothetically, zero. Increasing the number of unit cell on-switches from 512 to 4096 improves the drain efficiency as a result of the lower R_{on} (less overall power loss due to increased turned-on switches). Note that the cascode switch not only mitigates the related breakdown issue, but it is also used as an upconverting unit cell mixer. Controlling each switchable cascode transistor unit based on its related baseband data (i.e., I_{BB-up}/Q_{BB-up}), the equivalent on-resistor of I_{path}/Q_{path} is changed. Therefore, this can modulate the amplitude and phase of the reconstructed RF output signal (see eq. 3.21). Finally, perhaps the most significant advantage of this switchable cascode structure is to effectively isolate the I and Q paths which results in improved EVM and linearity.

In addition to its on-resistance, the cascode MOS switch also has a considerable gate or drain capacitance which is proportional to its channel width that was previously discussed in eq. (3.13 and their capacitance simulation results are depicted in Fig. 6.3(c). Selecting wider cascode switches in order to achieve higher efficiency, unfortunately, exacerbates the power consumption of the preceding RF clock buffers which subsequently reduces the overall system efficiency. As a result, the selected channel width of 500 nm appears to be an effective compromise between the overall system efficiency and maximum RF power[1]. Note that the drain capacitance also depends on the drain voltage (see eq. (3.14). Fig. 6.3(d) illustrates that the drain capacitance at V_{DD}=0.1 V is almost double of that at V_{DD}=1.2 V. Therefore, turning on the switches as well as varying the drain voltage changes the drain capacitance, which eventually results in AM-AM and AM-PM nonlinearities. As a result, the selected power combining network must also manage the drain capacitors.

The power combining network is an important part of the RF-DAC as it determines its output power, efficiency, and quadrature accuracy. Its importance is verified using load-pull simulations and demonstrated in Fig. 6.4(a). Note that, for simplicity, the load-pull simulation is only performed for the $Drain^{+}$ node, and its related drain efficiency, power, and modulation error contours are plotted. The modulation error is defined as a deviation of the modulated RF output signal from its ideal position. Load-pull simulation of Fig. 6.4(a) indicates that the orthogonality is degraded for loads corresponding to high efficiency and power contours. This reveals that employing upconverting clocks with D=25% is a necessary, but not sufficient, condition for the orthogonal operation. Note that the modulation orthogonality can be easily substantiated with the assumption of the linear time-invariant model of the

[1]As indicated in Chapter 5, eq. (5.1), in DPA-based TX, there is no such a concept as an analog/RF input power. The overall system efficiency is determined considering all related DC power losses including peripheral circuits.

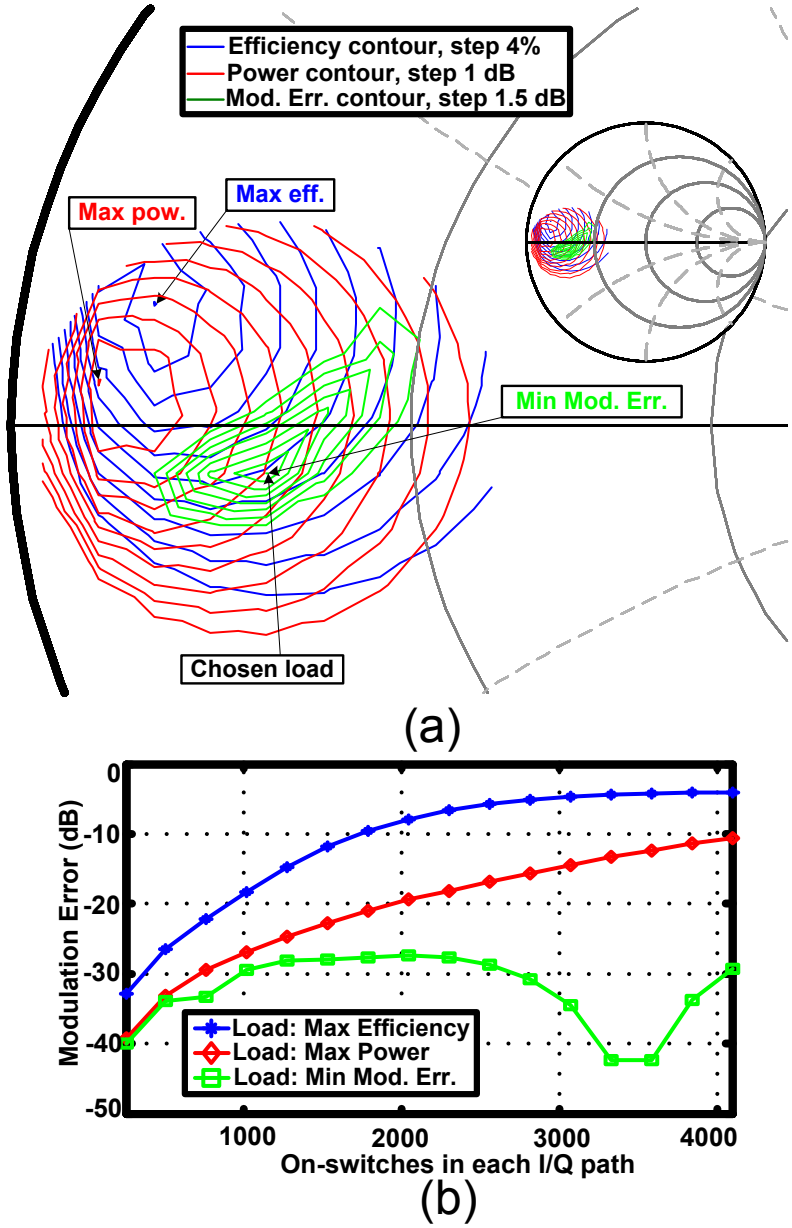

Figure 6.4: (a) Load-pull simulations for $Drain^{+}$ node. (b) Modulation error of different load types (max efficiency, max power, and min modulation error) versus count of on-switches in each orthogonal path.

switched PA (Fig. 3.9) which is valid when the effective transistor impedance (total switch resistance, R_{on}) in (3.17) is much larger than the loading matching network impedance R_{load} in Fig. 6.3(a). Equivalently, the RF output power in that region of operation is much less than its saturation level. Adding an incremental switch conductance will linearly increase the RF output envelope independent from the total instantaneous conductance level. Stated differently, at low RF power, the I and Q paths barely interact with each other. However, at higher RF power, R_{on} is lower and the drain capacitance is higher (lower capacitance

reactance), therefore the I and Q paths begin interacting (loading) with each another.

Note that, according to the simulated load-pull contours, three possible loads could be chosen: load based on the maximum efficiency, maximum power, and minimum modulation error. Fig. 6.4(b) exhibits the simulated modulation error versus the number of turned-on switches for the three mentioned load scenarios. This simulation confirms that the most appropriate choice for the modulation accuracy better than -28 dB is selecting the load based on a minimum modulation error, which is indicated in Fig. 6.4(a). This load provides the best modulation accuracy and reasonable efficiency (better than 50%) as well as generating the desired RF output power. By doing so, I and Q interaction becomes less while the digital predistortion can be simpler. In other words, as will be discussed in Chapter 7, it is possible to use only 2×one-dimensional (1D) DPD instead of two-dimensional (2D) counterpart due to uncorrelated I and Q paths. In conclusion, to maintain $I_{path,p}$, $Q_{path,p}$, $I_{path,n}$, and $Q_{path,n}$ orthogonal at all RF power levels, the circuit elements of power combining network must also be incorporated in all quadrature paths. It should be pointed out that all circuit simulations are performed at 2.4 GHz. This signifies that in order to maintain the orthogonality for other carrier frequencies, the optimum loading condition, which is selected based on the best modulation accuracy, must be adjusted accordingly.

6.2 A Differential I/Q Class-E Based Power Combiner

In order to achieve high efficiency at high RF power, and considering I_P, Q_P, I_N, and Q_N as being digital clock signals of rectangular pulse shape with a duty cycle of 25%, the class-E type matching network [92–95] is adopted because it is well suited for pulse-shaped signals. Furthermore, the class-E matching can absorb the drain capacitance of the cascode switches. Based on Fig. 6.2(b), the drain capacitance of the cascode switches is also considered in the eventual shunt capacitance, C_s in Fig 6.1. It should be mentioned that, due to the electrical summation of I_{path} and Q_{path}, the overall duty cycle at differential nodes of $Drain^+$ and $Drain^-$ in Fig. 6.2(b) is 50% at equal component power levels. In addition, in a class-E matching network, the loading condition for an RF signal with D=50% is completely different than at D=25% [94]. This explains why the efficiency/power contours of Fig. 6.4(a) significantly differ from the modulation error contours.

Based on the above considerations, the design of an orthogonal power combining network is divided into four identical class-E type matching networks, which are clearly depicted in Fig. 6.1. In this idealized power combiner, L_{BFI} provides the required DC current of DRAC; C_{AC} decouples the drain node from the output. There are three yet-to-be-defined components: R_{load}, C_s, and L_{add}, which will be addressed later in this section. The idealized power combiner of Fig. 6.1 is rather impractical. It should be modified such that it does not contain bulky components such as L_{BFI} and C_{AC}. Moreover, the eventual RF output must drive the single-ended load of 50 Ω. As a result, this power combiner should be modified.

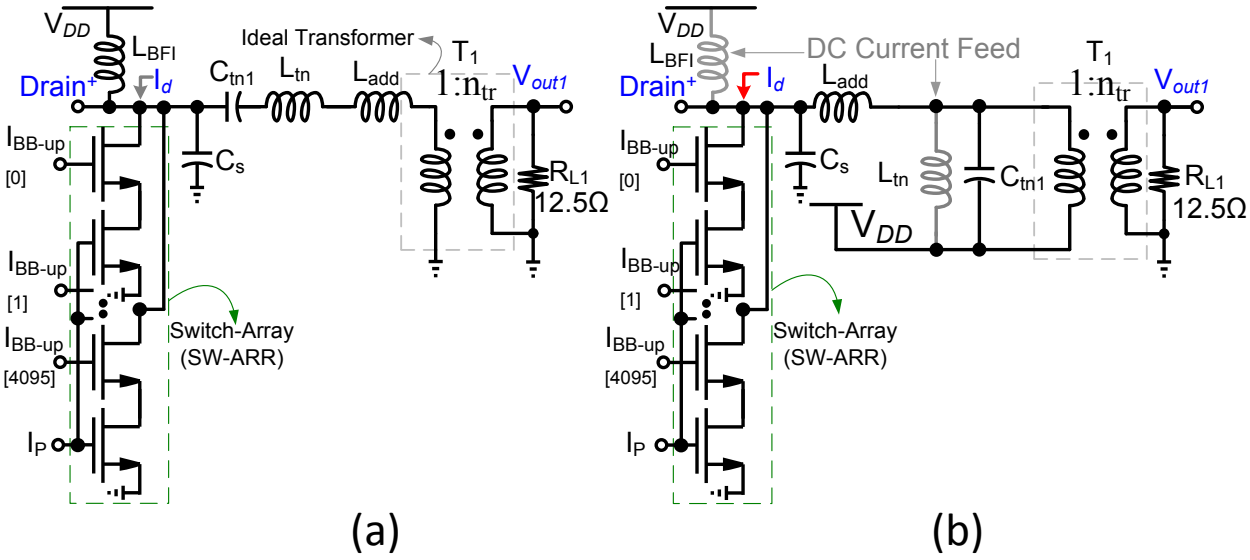

Figure 6.5: Power combining network: (a) first and (b) developing step.

Fig. 6.5(a) demonstrates the conventional class-E network [92] [93] [94] terminated with the transformed load. According to Figs. 6.1 6.2, the RF-DAC comprises four separate sections, and the total RF output power is the summation of the power delivered by each individual section. Therefore, the output load for each section can be viewed as

$$R_{L1} = \frac{1}{4} \times R_L = \frac{50}{4} = 12.5\,\Omega \tag{6.1}$$

However, the Fig. 6.5(a) matching network is not an effective selection for monolithic implementations. The use of two inductors (L_{BFI}, $(L_{add} + L_{tn})$) and one transformer (T_1) substantially increases the occupied area. The series tank filter of L_{tn} and C_{tn1} allows only the fundamental current component to pass. Equivalently, the series filter could be replaced by a parallel tank filter, as shown in Fig. 6.5(b). Although L_{tn} is employed as a component of the fundamental-frequency selective circuitry, it also could be used as the DC current feed, thus eliminating L_{BFI}.

This modification is illustrated in Fig. 6.6(a). Moreover, a practical transformer consists of magnetizing and leakage inductors [77]. Now, L_{BFI}, which is typically large, is fortunately eliminated. In addition, this circuit incorporates only one transformer and does not require the additional inductors. Indeed, L_{tn} and L_{add} are the magnetizing and leakage inductors of the transformer T_1 that is highlighted by the dotted gray box. C_{tn1} moves into the secondary side of the transformer and is now labeled as C_{tn}. Since the turns ratio of the transformer is $n_{tr} \geq 1$, then $C_{tn} \leq C_{tn1}$. Note that the Fig. 6.6(a) schematic depicts only the in-phase (i.e., I) switch array and not the complete quadrature modulator. Therefore, for the complete quadrature configuration, another C_s and L_{add} should be added parallel to the circuit, which is exhibited in Fig. 6.6(b). In contrast to the primary side of the transformer, the summation

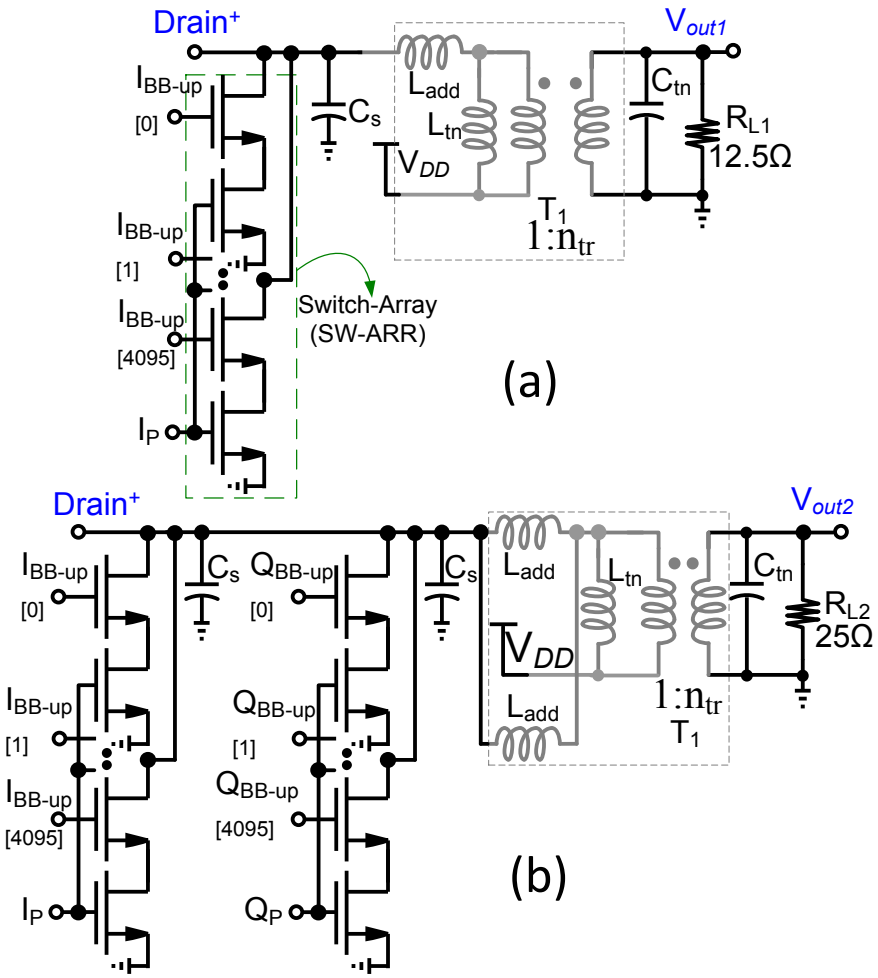

Figure 6.6: Power combining network: (a) modified version; (b) I/Q single-ended.

of I and Q signals in the secondary side is performed in series. Hence, R_{L2} is defined as:

$$R_{L2} = 2 \times R_{L1} = \frac{50}{2} = 25\,\Omega \tag{6.2}$$

As mentioned previously, the targeted power combining network should be differential (see also Section 3.2, Section 5.1 and Fig. 6.7) and should also act as a balanced-unbalanced (balun) converter. Accordingly, the transformer T_1 consists of leakage and magnetizing inductors of L_{leak} and L_{tn}, respectively, as well as an ideal transformer with N_1:N_2 turns ratio [77]. The signal summation on the secondary side of T_1 is performed in the voltage domain and, as a result, $R_L = 2 \times R_{L2} = 50\,\Omega$.

$$R_L = 2 \times R_{L2} = 4 \times R_{L1} = 50\,\Omega \tag{6.3}$$

For designing the power combining network, the values of C_{shunt}, C_s, L_{add}, L_{tn}, C_{tn}, C_{out}, R_{in}, and n_{tr} should be derived. Based on [94], the values of C_s and L_{add} depend on D, f_0,

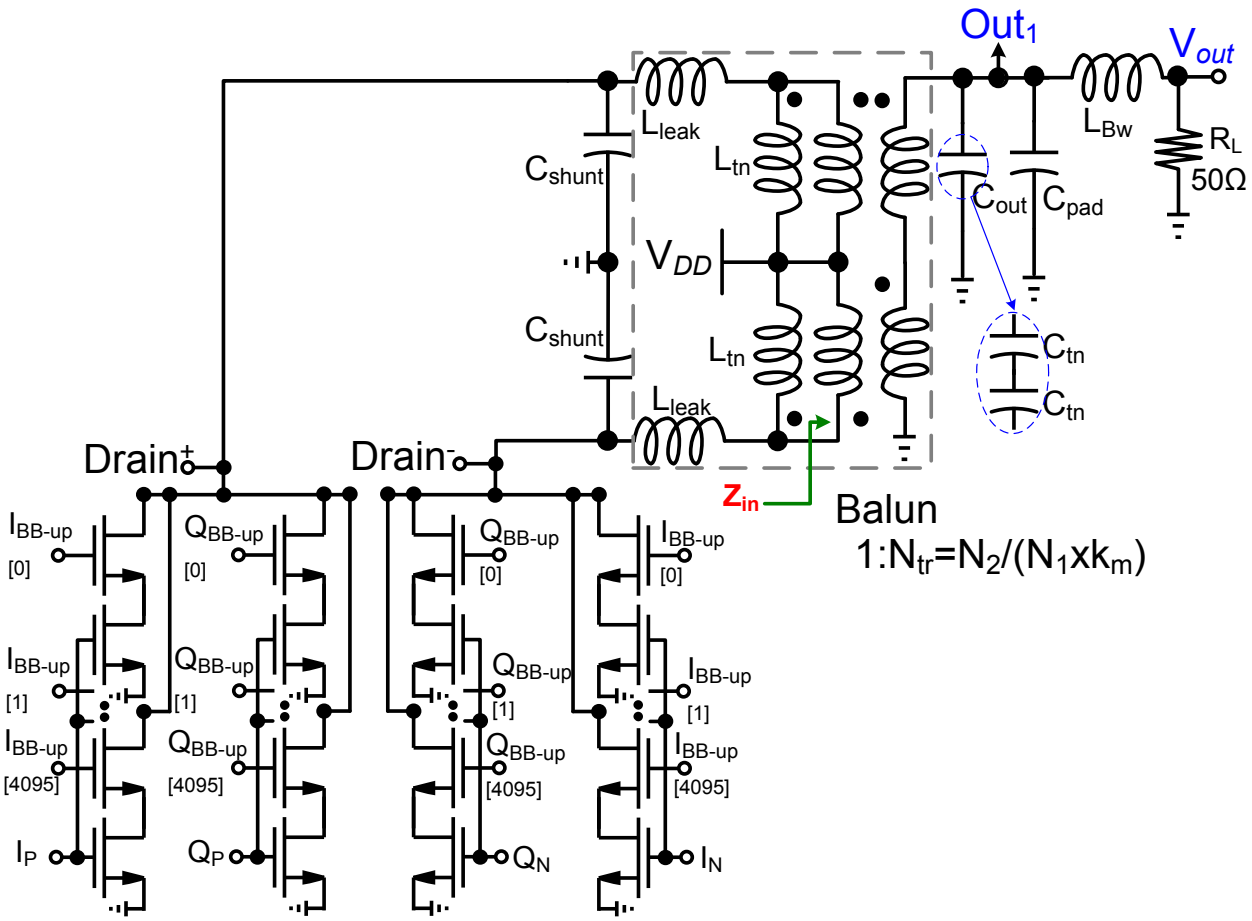

Figure 6.7: Power combining network: final differential I/Q RF-DAC.

R_{L1}, and n_{tr} (transformer turns ratio, i.e., $N_2/{N_1}^2$) and could be expressed as follows:

$$C_s(D, f_0, R_{L1}, n_{tr}) = \frac{f(D = 25\%)}{2\pi f_0 \times (R_{L1}/n_{tr}^2)} = \frac{f(D = 25\%)}{2\pi f_0 \times R_{load}} \tag{6.4}$$

$$L_{add}(D, f_0, R_{L1}, n_{tr}) = \frac{gt(D = 25\%) \times (R_{L1}/n_{tr}^2)}{2\pi f_0} = \frac{gt(D = 25\%) \times R_{load}}{2\pi f_0} \tag{6.5}$$

where $f(D)$ and $gt(D)$ represent two different functions, which depend on the duty cycle and are described in Appendix A [eqs. A.6 and A.8]. Furthermore, based on (A.10) and (A.11) for a 25% duty cycle, C_s and L_{add} are as follows

$$C_s(f_0, R_{load}) \cong \frac{0.21322}{2\pi f_0 \times R_{load}} \tag{6.6}$$

[2]Considering coupling factor, the eventual transformer turn ratio is $n_{tr} = \dfrac{N_2}{N_1 \times k_m}$ (see [77])

$$L_{add}(f_0, R_{load}) \cong \frac{3.5619 \times R_{load}}{2\pi f_0} \tag{6.7}$$

Moreover, R_{load}, which is depicted in Fig. 6.1 is the equivalent input referred resistor of Fig. 6.6(a), and defined as follows:

$$R_{load} = R_{L1} \times (\frac{N_1}{N_2})^2 = \frac{1}{4} \times R_L \times (\frac{N_1}{N_2})^2 = R_L \times (\frac{1}{2n_{tr}})^2 = 12.5 \times (\frac{1}{n_{tr}})^2 \tag{6.8}$$

According to Fig. 6.6(b) L_{tn} and C_{tn} resonate at f_0 and filter out higher-order harmonics. The value of L_{tn} affects the area, transformer coupling factor (k_m), quality factor (Q_F), and, consequently, the output power. The k_m of planar monolithic transformer is usually $0.6 \leq k_m \leq 0.9$. Therefore, e.g., choosing $k_m = 0.71$, the value of L_{tn} (magnetizing inductance) is equal to the leakage inductance of each balun leg [77], which is:

$$L_{tn} = L_{leak} = L_{add}/2 \tag{6.9}$$

C_{tn} resonates with L_{tn} which is:

$$C_{tn} = \frac{1}{(2\pi f_0)^2 \times L_{tn} \times n_{tr}^2} \tag{6.10}$$

C_{Shunt} and C_{out} are the parallel and series combinations of C_s and C_{tn}, respectively, and based on Fig. 6.6(b) and Fig. 6.7, can be expressed as:

$$C_{shunt} = 2 \times C_s \tag{6.11}$$

$$C_{out} = C_{tn}/2 \tag{6.12}$$

Note that, based on the new arrangement of Fig. 6.7, L_{tn} should resonate out with the combination of C_{out} and C_{pad}:

$$C_{out} + C_{pad} = \frac{1}{(2\pi f_0)^2 \times (2L_{tn}) \times n_{tr}^2} \tag{6.13}$$

where C_{pad} is the bond-pad capacitance. L_{BW} is a bond-wire inductor, which only slightly affects the power combining network and has also been examined previously in Section 4.1.6 and was specifically depicted in Fig. 4.9(c). Generally, the desired L_{leak} determines the size and structure of the selected transformer which subsequently determines the value of L_{tn} for a given value of the magnetic coupling factor k_m. To conclude, the balun performs the following:

1. It de-couples the drain DC condition from the load (elimination of C_{AC});
2. It converts the differential signal to a single-ended output;
3. It provides a DC bias path for the DRAC transistor switches (elimination of L_{BFI});
4. It transforms the $50\,\Omega$ load to the desired impedance at the drain nodes of DRAC.

Z_{in}, which is shown in Fig. 6.7, is indeed the single-ended matching network impedance of the modulator:

$$Z_{in} = R_{in} = \frac{R_L}{2 \times (n_{tr})^2} = 2 \times R_{load} \tag{6.14}$$

The output power of Fig. 6.7 expresses as:

$$P_{out} = \frac{(V_{out})^2}{2 \times R_L} = 4 \times P_{path} \tag{6.15}$$

where P_{path} is the power related to each orthogonal path of Figs. (6.1 ,6.2) or Fig. 6.7 and based on [94, eq. 3.29] expressed as

$$P_{path} = \frac{1}{2} \times (\frac{2 \times V_{DD}}{g(D)})^2 \times \frac{1}{R_{load}} = \frac{2}{(g(D))^2} \times \frac{V_{DD}^2}{R_{load}} \tag{6.16}$$

where $g(D)$ is a unitless function and depends only on D, and thus, $g(D = 25\%)\approx 5.8$ (see Appendix A, eqs.(A.4)-(A.9)). According to (A.10) the P_{path} is as follows:

$$P_{path} = \frac{2}{(5.79925)^2} \times \frac{V_{DD}^2}{R_{load}} \cong \frac{1}{16.8157} \times \frac{V_{DD}^2}{R_{load}} \tag{6.17}$$

As a result, the total output power can be expressed as:

$$P_{out} \cong \frac{4}{16.8157} \times \frac{V_{DD}^2}{R_{load}} \cong \frac{1}{4.2039} \times \frac{V_{DD}^2}{R_{load}} \tag{6.18}$$

In addition, according to (6.8)

$$P_{out} \cong \frac{(2n_{tr})^2}{4.2039} \times \frac{V_{DD}^2}{R_L} \cong \frac{(n_{tr})^2}{1.051} \times \frac{V_{DD}^2}{R_L} \tag{6.19}$$

Consequently, n_{tr} can be expressed as the output power:

$$n_{tr} \cong \frac{\sqrt{(1.051 \times R_L \times P_{out})}}{V_{DD}} \tag{6.20}$$

If V_{DD} is kept constant and, since most of the time the off-chip load impedance (R_L) is fixed and equal to $50\,\Omega$, according to (6.19) and (6.20), if n_{tr} increases, then the output power

Table 6.1: Design parameters of I/Q RF-DAC assuming a lossless transformer-based power combiner: $V_{DD} = 1.2\,\mathrm{V}$, $f_0 = 2.4\,GHz$, $L = 60\,nm$

n_{tr}	R_{in} (Ω)	P_{out} (dBm)	I_d (mA)	W (nm)	C_{shunt} (pF)	L_{leak} (pH)	N_{on-sw}
1	25	14.36	52	220	2.26	1500	1024
1.25	16	16.31	80	160	3.53	944	2048
1.5	11.11	18.29	126	120	5.09	656	4096
1.75	8.16	19.22	156	155	6.93	482	4096
2	6.25	20.40	200	210	9.05	369	4096
2.25	4.94	21.42	268	280	11.45	292	4096
2.5	4	22.31	317	345	14.14	236	4096
2.75	3.31	23.16	384	415	17.10	195	4096
3	2.77	23.89	451	485	20.36	164	4096

also increases, and the following statements can be concluded:

1. If the desired output power is considered to be in the range of $14.35 \leq P_{out-dBm} \leq 23.9$ while V_{DD}=1.2 V, then $1 \leq n_{tr} \leq 3$;
2. If the targeted output power should be in the range of $20.75 \leq P_{out-dBm} \leq 30.3$, while V_{DD}=2.5 V, then $1 \leq n_{tr} \leq 3$.

Note that, in the preceding conclusions, the passive components of the power combining network are considered lossless. To validate the equations derived above, the RF-DAC of Fig. 6.7 is simulated in Agilent ADS employing the following fixed design parameters: $V_{DD} = 1.2\,\mathrm{V}$, $f_0 = 2.4\,\mathrm{GHz}$, $L_{NMOS} = 60\,\mathrm{nm}$. All of the passive components are considered lossless. Table 6.1 reveals design components of the power combining network for different n_{tr} values of the transformer turns ratio[3]. As it is expected from (6.19)–(6.20) and substantiated by simulation results, increasing n_{tr} results in higher output power. Moreover, for all cases, the drain efficiency is $\eta_{drain} \approx 45\%$[4]. As will be concluded later, the efficiency drops in comparison to class-E primarily due to an increase of shunt capacitance (6.11), which, subsequently increases the modulator DC current.

[3] C_{shunt} in Table 6.1 is the value of the required shunt capacitor. This capacitor consists of the total drain capacitance of the related unit cell DPAs as well as additional explicit shunt capacitors.

[4] For all cases, their drain voltage swing is the same. Moreover, although employing a wider switch decreases its related R_{on}, yet its related DC current increases, consequently, P_{loss}=V_{on}×I_{DC}≈cte.

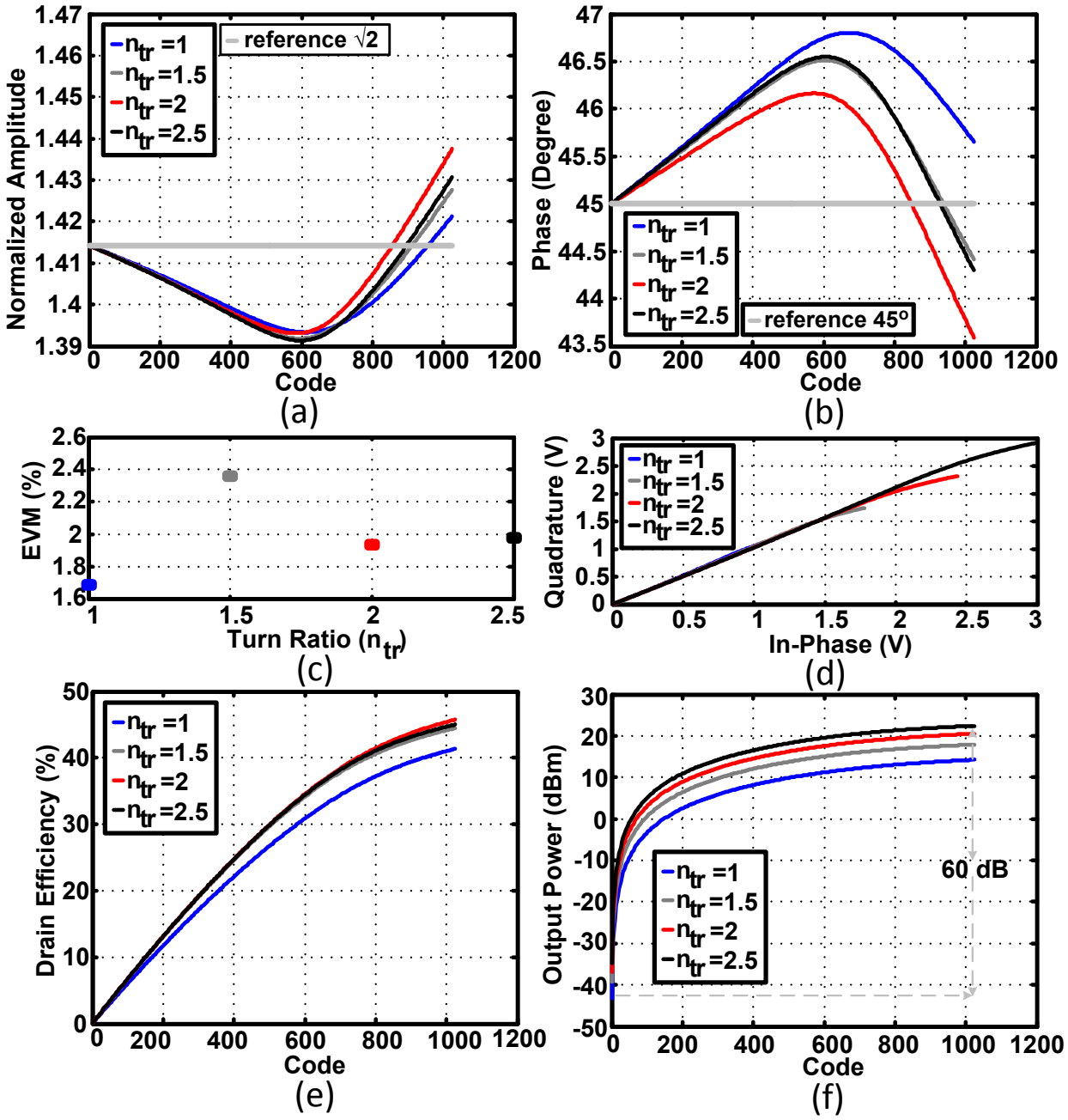

Figure 6.8: Simulation results of power combining network for equal I/Q codes (10 bits of resolution): (a) Normalized amplitude and (b) phase of RF output node; (c) corresponding EVM; (d) 1^{st} quadrant constellation diagram; (e) drain efficiency; (f) output power.

By sequentially and simultaneously increasing the I and Q modulator codes, the summing and orthogonality can be examined in view of the simulation results exhibited in Fig. 6.8. In this context, the I/Q modulator of Fig. 6.7 is simulated again in Agilent ADS using the following fixed design parameters: $V_{DD} = 1.2\,\text{V}$, $f_0 = 2\,\text{GHz}$, $L_{NMOS} = 100\,\text{nm}$. Moreover, for simplicity, the resolution (N_b) is reduced to 10-bit. Note that, in the conventional equation

of quadrature modulator, the resultant IQ signal can be expressed as:

$$IQ = I_{BB} \times \cos(\theta) - Q_{BB} \times \sin(\theta) \tag{6.21}$$

If $I_{BB} = Q_{BB}$, then

$$IQ = \sqrt{2} \times I_{BB} \times \cos\left(\theta + \frac{\pi}{4}\right) \tag{6.22}$$

As a result, the amplitude and phase of the IQ signal are

$$\rho_{IQ} = \sqrt{2} \times I_{BB} \tag{6.23}$$

$$\theta_{IQ} = \frac{\pi}{4} \tag{6.24}$$

Based on (6.23), the output power of Fig. 6.6(b) is:

$$P_{out2} = 2 \times P_{out1} = 2 \times P_{path} \tag{6.25}$$

where P_{out1} is the output power of Fig. 6.5(a)-(b) and Fig. 6.6(a) . Furthermore, (6.25) substantiates that each orthogonal path provides one quarter of P_{out}, which was previously indicated in (6.15). As derived in (6.23) and (6.24), the normalized amplitude and phase of the modulator should be $\sqrt{2}$ and $\pi/4$, respectively. Based on the simulation results, there are small deviations from these target numbers, which are illustrated in Fig. 6.8(a)–(b). As is previously stated and also is seen in Fig. 6.4(b), the reason for these amplitude and phase deviations are related to the fact that changing the G_{sw} would slightly change the phase and amplitude of the drain node and, consequently, the output node. Fig. 6.8(c) exhibits the corresponding EVM calculation based on (1.3). Simulation results reveal that the EVM for all of the simulation conditions is less than 2.5%, which confirms the orthogonal summing and power combining operation. Fig. 6.8(d) shows that the linearity of the modulator is improved when the transformation ratio is increased which entails increasing of the peak output power. The reason is that, for higher output power, R_{in} is lower and, consequently, the drain voltage swing is lower. Fig. 6.8(e) and Fig. 6.8(f) show that the drain efficiency and output power are selected to be maximum when the code is maximum. Moreover, based on Fig. 6.8(e), the dynamic range of the modulator is approximately 60 dB, which could correspond to 10 bits of the RF-DAC resolution.

6.3 Efficiency of I/Q RF-DAC

Based on Table 6.1 and also as was illustrated in Fig. 6.8(e), the maximum drain efficiency of the I/Q RF-DAC is approximately half of the ideal class-E. The efficiency drop is investigated

by considering the effect of the circuit component values on the drain current, voltage, and, subsequently, the resultant DC current and output power. In this context, the drain voltage of Fig. 6.6(a), which is depicted in Fig. 6.9(a), is considered periodic, thus, it can be represented using Fourier series. As a result, the periodic drain voltage could be expressed as:

$$V_{drain}(\theta) = V_{DD} + \sum_{n=1}^{\infty} a_n \cos(n\theta) + b_n \sin(n\theta) \tag{6.26}$$

in which a_n and b_n are in-phase and quadrature components of the periodic drain voltage in units of volts, respectively. In addition, the Fourier representation of a periodic pulse with $D = 25\%$ is:

$$\Pi_{D25}(\theta) = \frac{1}{4} + \left(\frac{2}{\pi}\right) \times \sum_{m=1}^{\infty} \left(\frac{1}{m}\right) \times \sin\left(\frac{m\pi}{4}\right) \times \cos(m\theta) \tag{6.27}$$

therefore, the switch conductance, which is illustrated in Fig. 6.9(b), is expressed as:

$$G(\theta) = G_{sw} \times \Pi_{D25}(\theta) \tag{6.28}$$

where G_{sw} was defined in 3.11. It is worth reiterating that the DRAC switch conducts only 25% of the clock period. According to Ohm's law, the switch (transistor drain) current depends on V_{drain} and G:

$$I_d(\theta) = V_{drain}(\theta) \times G(\theta) \tag{6.29}$$

Applying Kirchoff's voltage and current law as well as equating all cosine and all sine terms, and considering only the first two harmonics of eqs. (6.26)-(6.28), I_{DC}, a_1, and a_2 can approximately be estimated:

$$a_1 \cong \frac{V_{DD}}{\sqrt{2}\pi \times DET_1} \times H\left(\frac{C_s}{G_{sw}}, \frac{R_L}{L_{add}}\right) \tag{6.30}$$

$$a_2 \cong \frac{1}{DET_2} \times K\left(\frac{C_s}{G_{sw}}, \frac{R_L}{L_{add}}\right) \tag{6.31}$$

$$b_1 \cong \frac{V_{DD}}{\sqrt{2}\pi \times DET_1} \times T\left(\frac{C_s}{G_{sw}}, \frac{R_L}{L_{add}}\right) \tag{6.32}$$

$$I_{DC} \cong G_{sw} \times \left(\frac{V_{DD}}{4} + \frac{a_1}{\sqrt{2} \times \pi} + \frac{a_2}{2 \times \pi}\right) \tag{6.33}$$

where, DET_2, DET_1, H, K, and T are defined in Appendix A [eqs. A.12 and A.16]. Note that H, K, and T depend on the following variables:

$$B_{Cs} = 2\pi f_0 C_s \tag{6.34}$$

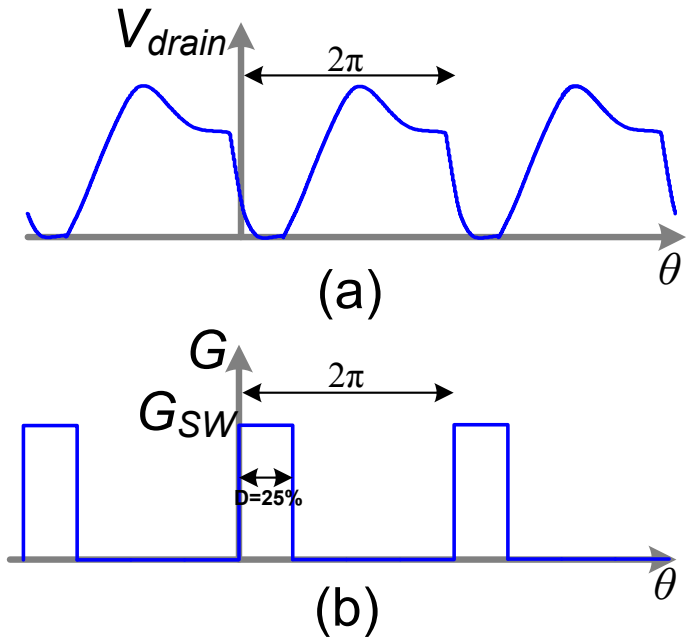

Figure 6.9: Waveforms of (a) the drain voltage, $V_{drain}(\theta)$; (b) switchable conductance, $G(\theta)$.

$$X_{Ladd} = 2\pi f_0 L_{add} \tag{6.35}$$

$$|Z_{RX}|^2 = R_L^2 + X_{Ladd}^2 \tag{6.36}$$

In fact, the phasor representation of drain voltage and output voltage at fundamental frequency of operation (f_0) of Fig. 6.6(a) are:

$$V_{P-drain} = a_1 + \mathrm{j}b_1 \tag{6.37}$$

$$V_{P-out} = V_{P-drain} \times \left(\frac{R_L}{R_L + \mathrm{j}X_{Ladd}} \right) \tag{6.38}$$

Consequently, based on the voltage and current equations of (6.26)-(6.38), the output power, DC power, and drain efficiency are:

$$P_{out1} = \frac{1}{2} \times \Re \left(V_{P-out} \times \mathrm{conj} \left(\frac{V_{P-out}}{R_L} \right) \right) \tag{6.39}$$

$$P_{DC1} = V_{DD} \times I_{DC} \tag{6.40}$$

Table 6.2: Design parameter of class-E in Fig. 6.6(a) for $V_{DD} = 1V$, $f_0 = 2\,GHz$, $R_{on} = 0.4\,\Omega$, $C_{tn} = 10\,pF$, $L_{tn} = 633\,pH$, $n_{tr} = 1$

Type	**Figure**	$\boldsymbol{C_s}$ (pF)	$\boldsymbol{L_{add}}$ (pH)	$\boldsymbol{R_{L1}}$ (Ω)
Case I	Fig. 6.6(a)	16.97	284	1
Case II	Fig. 6.6(b)	33.94	142	2

Table 6.3: Comparison between derived equations and circuit simulation

Type	$\boldsymbol{V_{P-drain}}$ (V)	$\boldsymbol{V_{P-out}}$ (V)	$\boldsymbol{P_{out1}}$ (dBm)	$\boldsymbol{I_{DC}}$ (mA)	$\boldsymbol{\eta_{drain1}}$ (%)
Equations Case I	-1.100-j0.317	-0.163+j0.263	16.805	54	89.061
Simulation Case I	-1.082-j0.431	-0.191+j0.250	16.950	55	89.500
Equations Case II	-0.742+j0.149	-0.340+j0.451	19.019	137	58.065
Simulation Case II	-0.726+j0.210	-0.300+j0.478	19.007	142	56.148

$$\eta_{drain1} = \frac{P_{out1}}{P_{DC1}} \tag{6.41}$$

For validating these equations, two different cases are considered. The first case (case I) is related to the class-E circuit (Fig. 6.6(a)) with $R_{on} = 0.4\,\Omega$. The second case (case II) is the circuit of Fig. 6.6(b) in which the quadrature switch arrays are off. The design parameters of the two cases are tabulated in Table 6.2. Note that for the sake of simplicity, in this context, the R_{L1} is considered $1/2\,\Omega$. As a result, Table 6.3 compares the derived equations and circuit simulation results of these two cases. Table 6.3 reveals certain significant conclusions:

1. There is a positive agreement between the derived equations and circuit simulation results. The moderate differences between them arise because of neglecting the higher harmonics of (6.26);

2. Since $C_{s-caseII} = 2 \times C_{s-case1}$, $L_{add-caseI} = 2 \times L_{add-caseII}$, and $R_{L1-caseII} = 2 \times R_{L1-caseI}$, according to (6.30)-(6.36), these entail an increase of a_1, a_2, I_{DC}, and reduction in quality factor. Consequently, the drain efficiency of the modulator decreases compared to a class-E implementation;

3. The phase and amplitude of the drain node and, consequently, the output node depend

only on the value of G_{sw} when the other passive components are fixed. Therefore, by sequentially turning on the switches, the phase of output would be changed (see eq. 3.21). In other words, turning on and off the switches modulate the RF output signal and can address the desired constellation diagram points;

4. The output power of the second case (P_{out2-2}) is higher than case one (P_{out1}):

$$P_{out2-2} = \alpha_p \times P_{out1} \tag{6.42}$$

where α_p is an incremental factor of power. Simulation results indicate that this value primarily depends on R_{on}, and α_p varies between $1 \leq \alpha_p \leq 2$. As was previously mentioned, the second case is an especial case of Fig. 6.6(b) in which the Q path is completely deactivated (off). Thus if the Q path turns on completely, then the output power will be doubled.

6.4 Effect of Rise/Fall Time and Duty Cycle

As thoroughly explained in this thesis, in order to isolate between the I_{path} and Q_{path}, the differential quadrature upconverting clocks with the duty cycle of 25% are utilized. Thus, due to their shorter pulse width, the related rise/fall time of the upconverting clocks should be fast enough to properly charge and discharge the drain capacitances in a short period of time in order to perform reasonable isolation between I_{path} and Q_{path}. Consequently, the I/Q RF-DAC is implemented in 65 nm CMOS which affords moderate rise/fall time. According to the post layout simulation results of the I/Q RF-DAC, the rise/fall time at the gate of digital power amplifier switches are approximately 45 ps. Employing a 2.4 GHz upconverting clock while its related duty cycle is 25%, the rise/fall time must be less than 104.16 ps in order to avoid non orthogonal operation. To validate the effect of rise/fall times, they are swept from 30 ps to 100 ps. According to the simulation results of Fig. 6.10(a)-(c), the related modulation error of the I/Q RF-DAC will be less than -25 dB as long as the corresponding rise/fall time of the upconverting clocks are less than 80 ps. Moreover, as depicted in Fig. 6.10(a)-(c), the drain efficiency of the RF-DAC along with its corresponding output RF power will be diminished for the slower clock edges. Nonetheless, implementing the proposed RF-DAC in a more advanced nano-scale CMOS process, such as 28 nm, will improve the performance.

Note that, in order to preserve orthogonality as stated throughout the thesis, the duty cycle of the upconverting differential, quadrature clocks is selected at 25%. As explained previously, this selection, based on the fact that the timing overlap of the differential quadrature clocks, must be as minimal as possible. As a result, any duty cycle less than 25% is also acceptable. Nonetheless, there would be three primary disadvantages in not selecting the 25%. First, generating differential quadrature upconverting clocks with a 25% duty cycle is

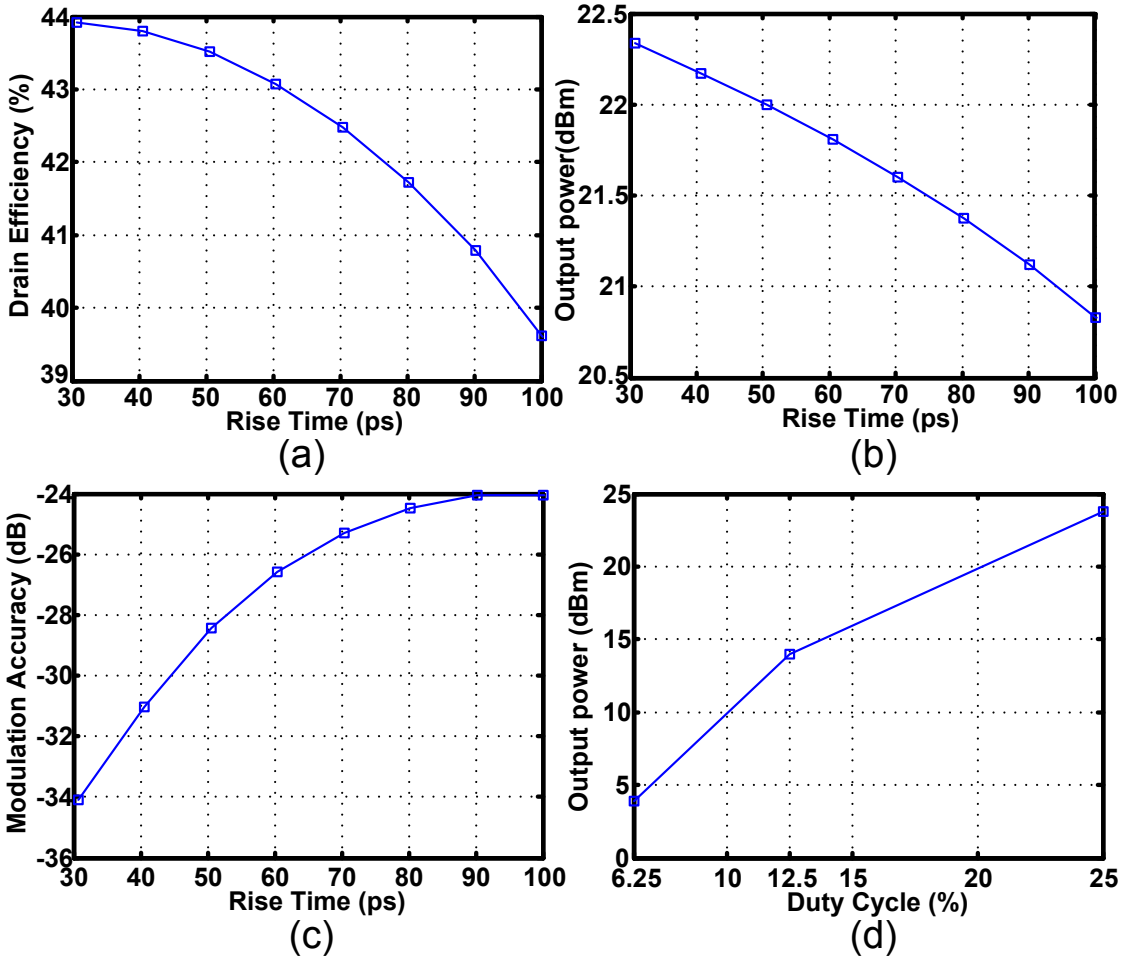

Figure 6.10: Simulation results based on sweeping the rise/fall time of the upconverting clock in order to illustrate their effects on (a) drain efficiency; (b) output power; (c) modulation accuracy. (d) Output power versus the duty cycle of the upconverting quadrature clocks.

less complicated. Second, the corresponding clock generation circuitry consumes less power. Third, as depicted in Fig. 6.10(d), the related RF output power for a 25% duty cycle is much higher due to the fact that the fundamental frequency of the RF current is proportional to the clock pulse width which makes the RF output power proportional to the pulse width of the differential, quadrature upconverting clock. It should be pointed out that the related drain efficiency as well as modulation accuracy of them, i.e., upconverting clocks with $D \leq 25\%$, are more or less identical.

6.5 Efficiency and Noise at Back-Off Levels

Although the power combining network, at full power, has been designed based on a class-E matching network, yet at back-off power, the RF-DAC performs more like a class-B power

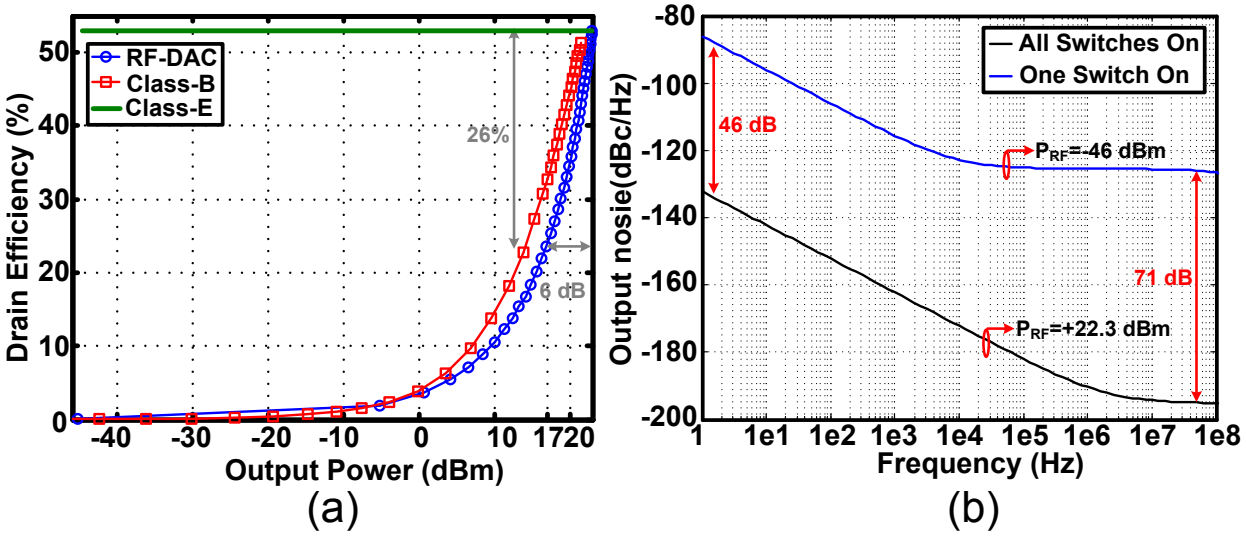

Figure 6.11: (a)Comparison of back-off power profiles between the proposed RF-DAC and a class-AB power amplifier. (b) Noise performance of the RF-DAC at low and full power mode of operation.

amplifier. The reason is related to the fact that, at full power, the entire transistor arrays perform equivalently as a switch due to the low drain-source, on-resistance (R_{on}) of the equivalent switch. According to the simulation result in Fig. 6.3(a), the R_{on} at full power, i.e., the baseband code of 4096, is less than 2 Ω. Otherwise stated, the drain-source voltage of the aforementioned switchable cascode transistors is approximately 0.25 V indicating that the equivalent switch operates in the triode region. On the other hand, at back-off power levels, the number of on-switches decreases which subsequently increases the R_{on} of the equivalent switch. As a result, the drain-source voltage of the equivalent switch increases. This causes the equivalent switch (switchable cascode transistor) to operate in the saturation region. Thus, it performs as a current source rather than a switch which indicates that the RF-DAC operates as a class-B power amplifier. In order to confirm the foregoing discussion, the performance of the RF-DAC efficiency is simulated while the input baseband code is swept from code 1 up to 4096. Simultaneously, a class-B power amplifier, which employs an idealized matching network, is also simulated. The two simulation results are depicted in Fig. 6.11(a). According to that, the RF-DAC at back-off power levels more or less performs the same as a class-B power amplifier. Additionally, it indicates that the drain efficiency diminishes approximately 26% at 6 dB back-off power[5]. Note that, if the RF-DAC were also to operate in class-E mode at the power back-off as illustrated in Fig. 6.11(a), it must maintain its drain efficiency as in the full RF power even at the back-off power levels.

[5]Note that at 6 dB back-off power levels, the power is one-fourth of its saturated RF power. In this context, the drain's fundamental as well as its DC current component is one-half of their maximum value. Nonetheless, its related DC voltage is fixed, i.e., V_{DD}=1.2 V, while its fundamental drain voltage becomes half. Consequently, the efficiency drops to half of its maximum value.

The RF-DAC noise performance is also simulated and depicted in Fig. 6.11(b). Two scenarios are exhibited which are the noise performance of the RF-DAC when the baseband input code is 1 and 4096, respectively. As expected, the RF-DAC noise performance will improve provided it operates at higher power levels in which the number of on-switches are increased. The noise floor is better than -194 dBc/Hz at full power which indicates that the noise of the switches is not a limiting factor in the total noise floor of the RF-DAC. Indeed, as will be presented in Chapter 7, Section 7.4, Fig. 7.4(d), the noise of the clock generator sources are the dominant noise sources. Note that, based on the simulation results of Fig. 6.11(b), at low frequencies, the noise of the switches are almost dominant ($1/f^3$ and $1/f^2$ regions), however, at higher frequencies, the noise sources related to the power combining network overtakes the noise of the switches.

6.6 Design an Efficient Balun For Power Combiner

As stated previously, the power combining network consists of input/output capacitor tuners and the balun. The transformer, however, should be properly designed as it affects efficiency, output power, and modulation accuracy. In the previous sections, the balun role and its impact on the eventual RF output power as well as the modulation accuracy of the proposed I/Q RF-DAC have been thoroughly discussed. Nonetheless, this passive component introduces certain power losses and should be carefully designed.

Fig. 6.12 exhibits six different balun transformers (T_1). The turns ratio (N_2/N_1) of these baluns are 1:2, in which the top row of Fig. 6.12 is a conventional 1:2. According to Table 6.1, for producing $\geq$22 dBm RF output power, the balun must manage high currents from 317 mA up to 451 mA while $n_{tr} \geq 2.25$. To support this substantial current, the balun could employ three parallel traces in the primary winding (see Fig. 6.14) that are inter-digitated with the secondary winding to satisfy electromagnetic rules of the technology [19]- [48]. The bottom row of Fig. 6.12 utilizes the inter-digitated transformer structure with 1:2 turns ratio. Furthermore, according to Fig. 6.12, the size of the outer diameter varies between 300 to 450 μm. The transformers use metal layers 6 and 7 as well as an aluminum layer for decreasing losses due to the series resistance. Note that the thickness of metal 6, 7, as well as the aluminum layer are 0.9, 3.4, and 1.45 μm, respectively. Thus, metal 7 is the thickest layer. The transformer traces are 12 μm wide except in Fig. 6.12(d) that uses 6 μm traces for the primary side. The traces are separated with 3 μm gaps between them in order to satisfy the metal density rule of the process technology. The 2×13-bit I/Q RF-DAC is simulated together with these baluns in the power combining network. The simulations have been performed using the following conditions. f_0=2.4 GHz, V_{DD}=1.2 V, W=500 nm, L=60 nm, and R_L=50 Ω. Note that, according to simulation results based on Table 6.1, for the lossless power combining network, the drain efficiency would be in the range of 45%. Moreover, based on the simulation results of Table 6.3, the drain efficiency for a lossless

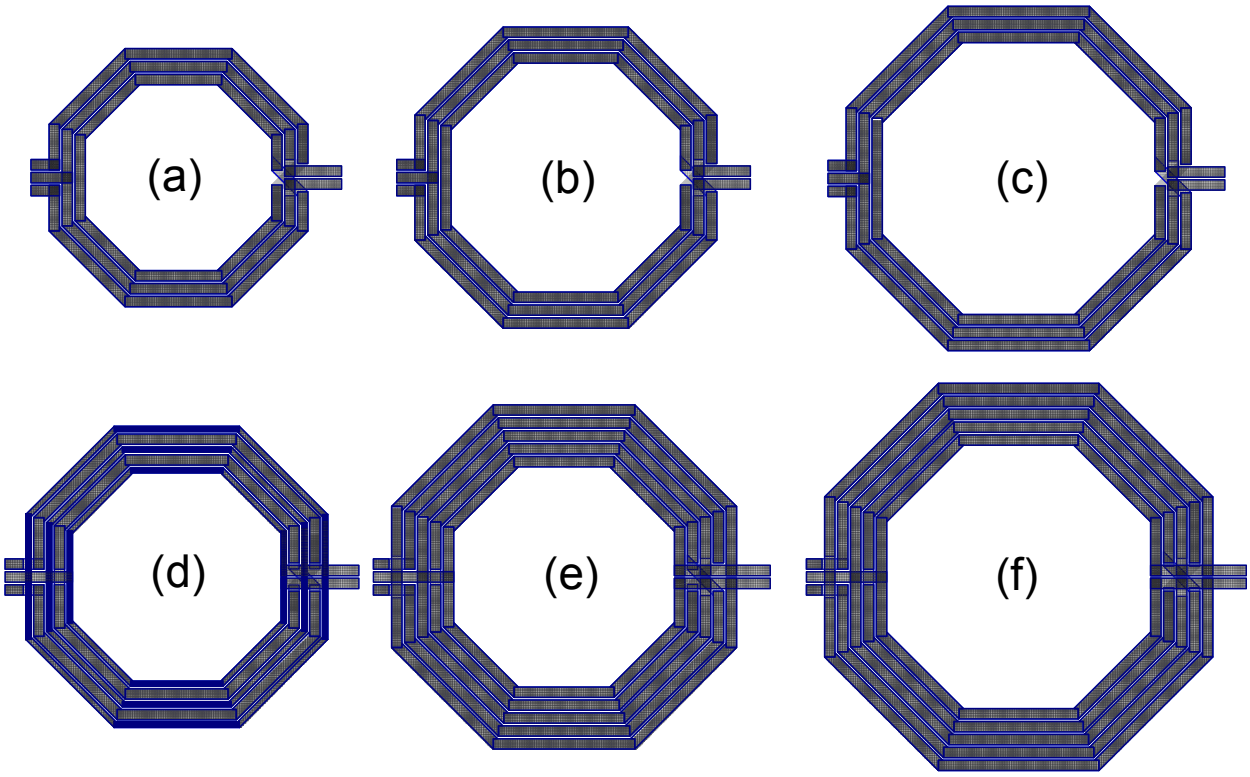

Figure 6.12: Six different baluns (T_1) design example: Conventional 1:2, (a) $300\times300\,\mu m^2$; (b) $350\times350\,\mu m^2$; (c) $400\times400\,\mu m^2$. Inter-digitated 1:2, (d) $350\times350\,\mu m^2$; (e) $400\times400\,\mu m^2$; (f) $450\times450\,\mu m^2$.

power combining network can exceed 55%. The difference between these two results is related to the selected width of their corresponding switches. Consequently, the efficiency of Table 6.1 would increase using wider switches. As stated earlier, selecting unit cell switches with 500 nm width is an effective compromise between the overall system efficiency, output power, and modulation accuracy. Table 6.4 summarizes the simulation results. Note that Q_p, and Q_s are the primary and secondary quality factors of the balun, respectively, and the following statements can be inferred:

1. The conventional balun manifests moderate Q_p, output power, and efficiency. In addition, its insertion loss (P_{loss}) is also not better than 1.1 dB;

2. The corresponding differential primary inductance of conventional transformer, L_p, is higher. Note that L_p of Fig. 6.7 is defined as follows:

$$L_p = 2 \times (L_{leak} + L_{tn}) \tag{6.43}$$

The L_p of conventional transformer is higher than the inter-digitated one due to smaller effective width of the primary winding. Consequently, the current through

Table 6.4: Simulation results of RF-DAC at f_0=2.4 GHz using the baluns of Fig. 6.12

T_1	L_p (nH)	C_{iw} (fF)	k_m	Q_p	Q_s	P_{loss} (dB)	P_{out} (dBm)	EVM (%)	η_{drain} (%)	η (%)
(a)	0.6	23	0.74	7.5	10.5	1.3	21.3	3.9	51	38
(b)	0.76	31	0.77	8.1	10.9	1.1	21.3	4.3	51	39
(c)	0.93	39	0.79	8.3	10.7	1.1	21.3	5.2	51	40
(d)	0.52	52	0.82	10.7	9.6	1	22.1	2.5	53	42
(e)	0.53	64	0.82	15.9	8.4	0.9	22.4	3	53	43
(f)	0.67	76	0.84	16.6	8.5	0.8	22.4	3.5	54	44

the conventional transformer is more constant than through the inter-digitated one[6].

3. The coupling factor (k_m) of an inter-digitated balun is higher than the conventional one. This is due to fact that the primary winding sandwiches between the secondary winding trances. Moreover, since the effective width of primary winding is larger, the power losses are subsequently smaller and Q_p is higher;

4. The inter-winding capacitance of inter-digitated transformer, C_{iw}[7], which is the capacitance between the primary and secondary winding is higher due to five inter-digitated metal traces. These distributed capacitors electrically couple the primary to secondary winding that provide paths between the single-ended output node to the differential primary inputs. As a result, due to lower impedance of the inter-winding capacitance at higher frequencies, the transmission of the even and odd harmonic contents of the differential drain nodes to the output node is easier. Thus, both the even and the odd harmonic contents of the inter-digitated balun are higher than the conventional one. Stated differently, the balanced-to-unbalanced performance of the inter-digitated transformer is inferior than the conventional structure.

As noted previously, the RF-DAC must produce more than 22 dBm RF output power. The width of the digital NMOS switches is selected 500 nm to provide the necessary R_{on} for generating that amount of targeted RF power. Based on the simulation results of Table 6.4, the conventional balun structures of Fig. 6.12 could not transform the optimum impedance to the drain nodes in Fig. 6.7. Therefore, the desired 22 dBm RF output power could not be generated. This also affects the efficiency and modulation accuracy of the RF-DAC. On the

[6]Note that the drain DC power of DPA switches is fed using L_{tn}. This inductance should be large enough to provide only DC path from V_{DD}.

[7]C_{iw} is represented by C_{o1} and C_{o2} in Fig. 4.8.

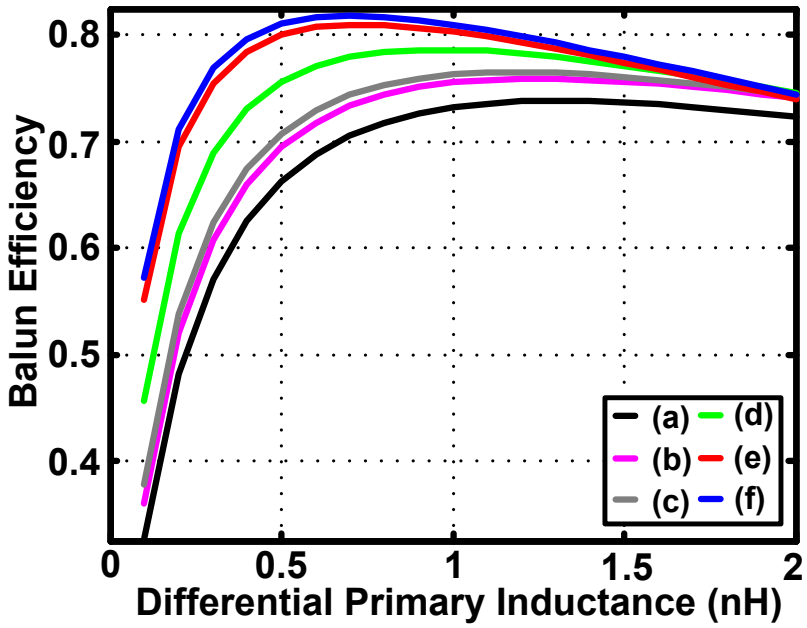

Figure 6.13: The balun efficiency comparison of all transformers of Fig. 6.12.

other hand, the inter-digitated transformer balun can produce the expected output power level due to its higher coupling factor and lower primary inductance. Note that, according to Aoki *et al.* the transformer efficiency can be expressed as follows [8]

$$\eta_{Balun}(X_p) = \frac{R_L/n_{tr}^2}{\left(\frac{X_p/Q_s + R_L/n_{tr}^2}{k_m X_p}\right)\cdot\frac{X_p}{Q_p} + \frac{X_p}{Q_s} + R_L/n_{tr}^2} \tag{6.44}$$

where $X_p = \omega_0 L_p$ while $\omega_0 = 2\pi f_0$. Based on this equation(6.44), to obtain adequate efficiency, the balun must be designed in such a way that its Q_p, Q_s, and k_m are as high as possible. Using the equation(6.44), the balun efficiency of all transformers of Fig. 6.12 is compared in Fig. 6.13 versus L_p. According to Fig. 6.13, the highest efficiency (82%) is obtained employing the inter-digitated transformer "f" in Fig. 6.12. Note that the maximum balun efficiency occurs when L_p=0.7 nH. This is an interesting result since, based on Table 6.3, the L_p of the balun (f) is approximately 0.67 nH. Based on the foregoing explanations, the balun of Fig. 6.14(a) is selected (same as Fig. 6.12(f)), which is the inter-digitated 450×450 μm^2 with 1:2 turns ratio. In summary, the inter-digitated balun structure introduces two primary advantages [19]

1. Due to effective wider primary traces, the DC ohmic series losses are reduced;

2. Due to inter-digitated traces, the AC resistance caused by proximity effect[8] is dramatically decreased.

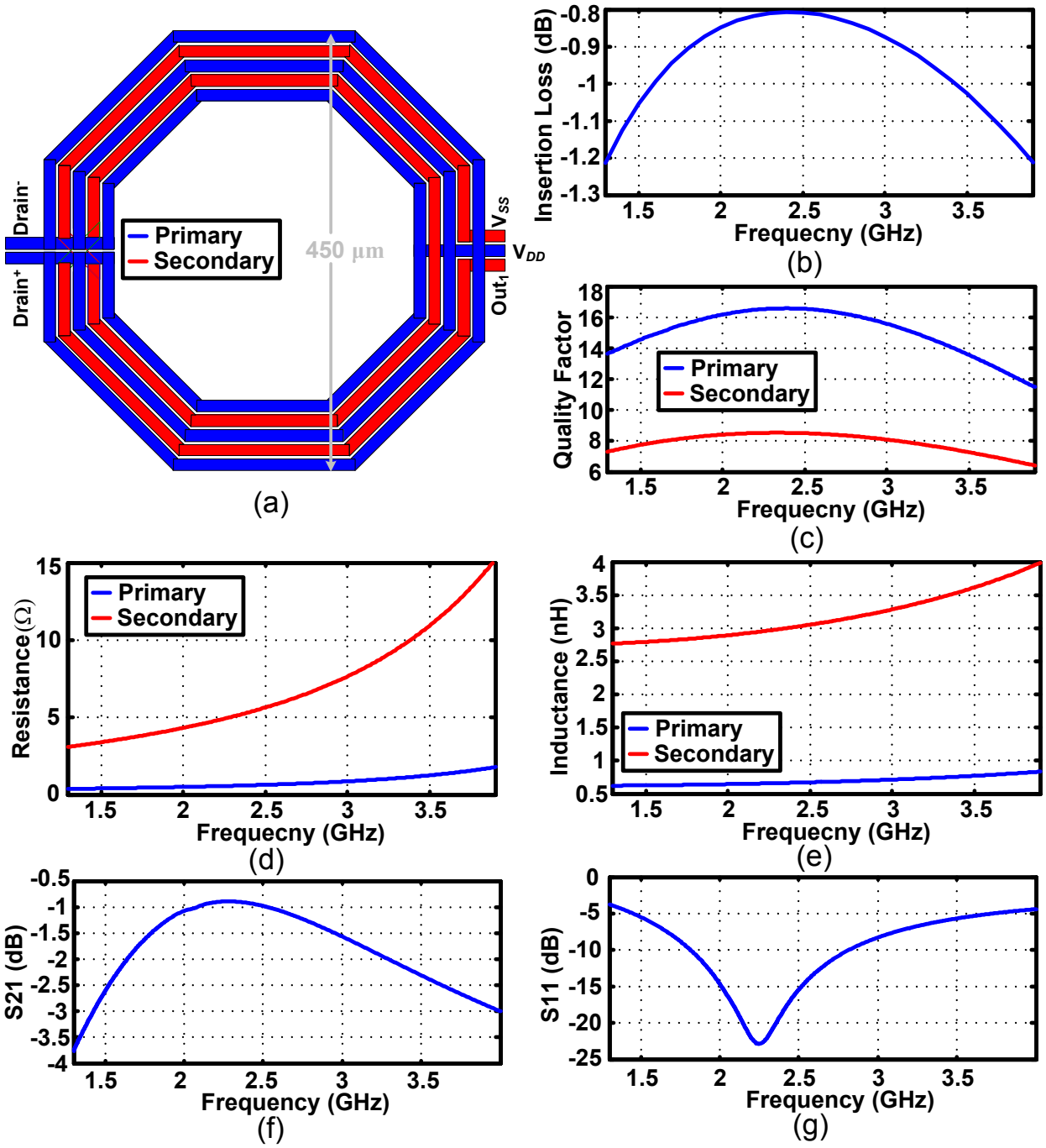

Figure 6.14: (a) Chosen balun; (b) insertion loss; (c) quality factor; (d) loss series resistance; (e) inductance; versus frequency. Loaded (f) S21, and (g) S11 versus frequency.

Fig. 6.14(b)-(e) illustrate the ADS Momentum simulation results of the selected balun structure. According to Fig. 6.14(b), the insertion loss is better than 1 dB in the frequency

[8] At RF frequencies, the opposite currents of two parallel traces tend to be concentrated along adjacent edges (non-uniform current distribution), which causes higher insertion loss [19].

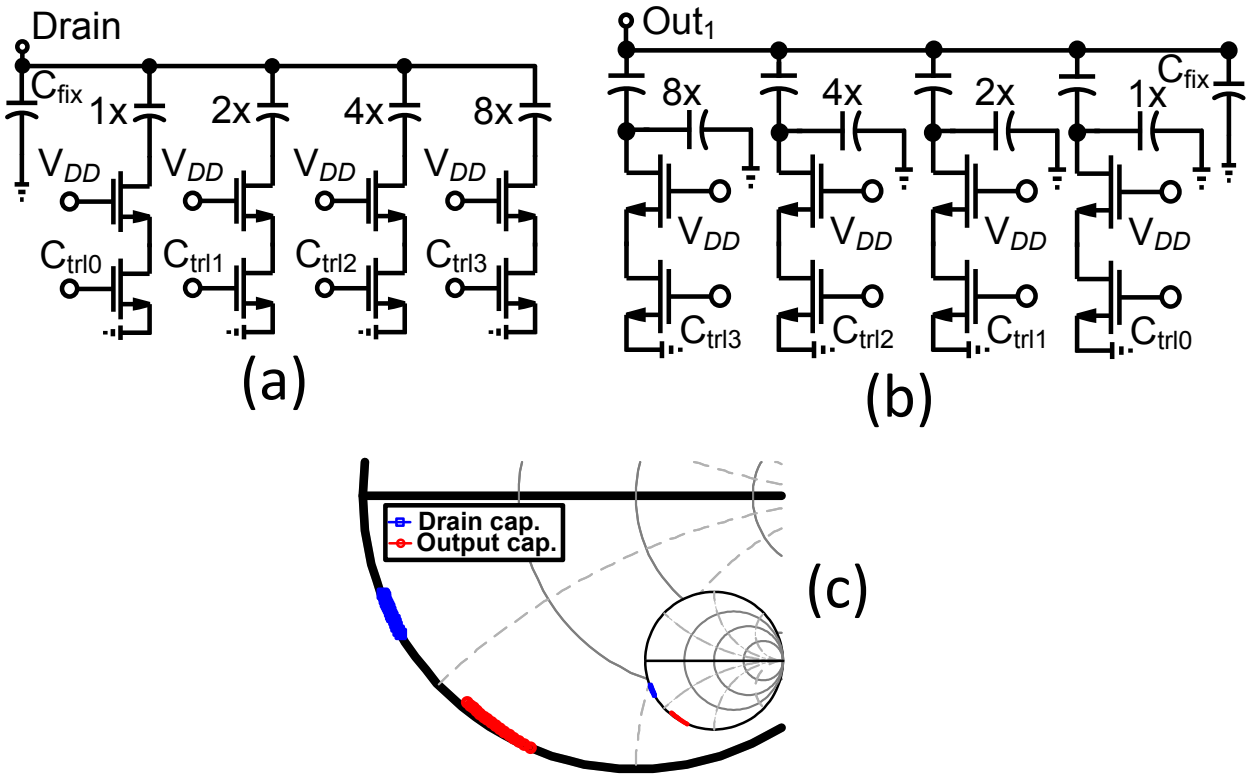

Figure 6.15: (a) The primary input shunt tuning switched-capacitors; (b) the output tuning switched-capacitors; (c) The simulation results of the related load reflection coefficients.

range of 1.6 to 3.4 GHz. Furthermore, the Q_p is higher than 14.5 within the frequency of 1.5 to 3.3 GHz (Fig. 6.14(c)). In addition, the related k_m of up to 6 GHz is 0.84 and the equivalent primary loss resistance is less than 1 Ω while the frequency is less than 3.2 GHz. It is worth mentioning that, based on the simulation results in Table 6.4, drain efficiency is 54%. Moreover, based on equation(6.44), the balun efficiency is 82%. As a result, the eventual efficiency is 0.54×0.82=0.44 which agrees to the simulated total efficiency that is reported in Table 6.4.

Note that, although the power combining network has been designed based on the class-E matching network topology, its operational "carrier" bandwidth (see Figs. 6.14(f)-(g)) is much higher than with the traditional narrowband Class-E PA. The reason lies in the fact that, in this context, the balun transformer is employed instead of an inductor. In general, the transformer's bandwidth is much larger than inductor's due to its tolerance to lower quality factor requirements as well as a larger number of transfer function poles. It should be pointed out that, as stated previously, the subsequent power combining network is not a pure class-E matching network. Based on simulation results of Figs. 6.14(f)-(g), the designed power combiner can manage more than 500 MHz RF bandwidth.

The shunt input and output capacitors of the transformer balun are utilized to fine tune the amplitude and phase relationships of the I/Q modulator for the desired frequency.

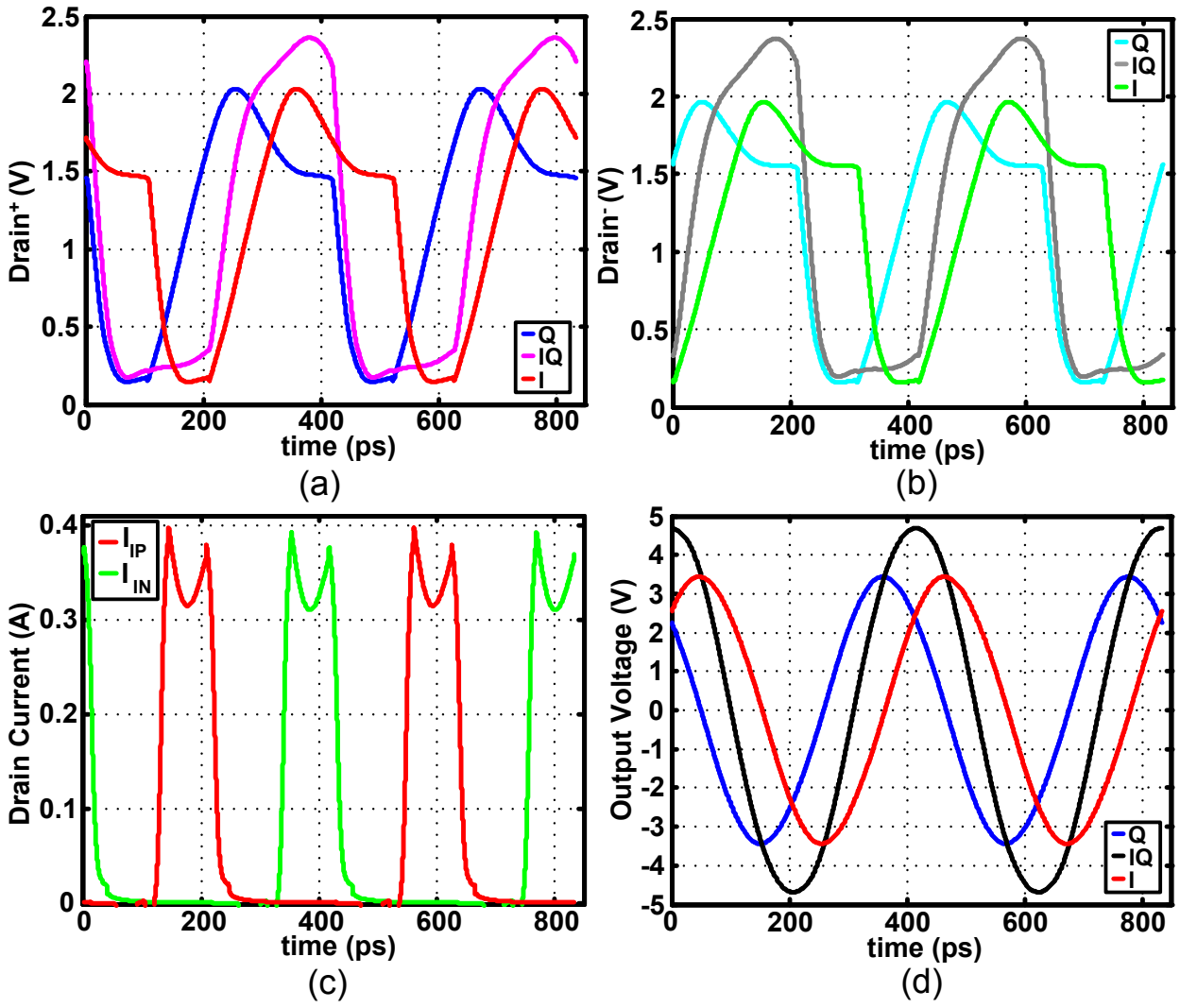

Figure 6.16: I/Q RF-DAC voltage/current waveforms of three simulation results of Fig. 6.7 in which Q path is on, on and off, respectively. Moreover, I path is off, on and on, respectively; (a) $Drain^{+}$; (b) $Drain^{-}$; (c) In-phase drain currents; (d) RF output voltage.

For this purpose, two 4-bit binary-weighted capacitor banks are added at the primary and secondary sides of Fig. 6.7 and are illustrated in Fig. 6.15(a)-(b). Since the entire design is accomplished using 1.2 V standard thin-oxide transistors, the voltage swings at the transformer connections are too high to be managed by a single transistor. Consequently, cascode switches are used. Moreover, the voltage swing at the secondary side can be as high as 4 V. Therefore, series-capacitors are incorporated to reduce the cascode drain node swing to, at most, 2 V (Fig. 6.15(b)) [96]. The load reflection coefficient of primary/secondary capacitor tuners are shown in the Smith chart of Fig. 6.15(c). Based on the simulations, the primary capacitance varies between 4.8 to 7.8 pF while the secondary capacitance changes between 1.9 to 2.7 pF. Note that, although in both input and output capacitor tuners, many lossy

switches are employed, yet their quality factors (≥32) are still significantly higher than the designated balun (see Fig. 6.14(c)).

In addition, the reliability of RF-DAC is evaluated with the assistance of Fig. 6.16(a)-(b). Based on that, the peak drain voltage of nodes $Drain^{+}/Drain^{-}$ is less than 2.4 V, which indicates that the breakdown will not occur[9]. Moreover, according to this simulation, the minimum drain voltage is approximately 0.25 V, which results in an appropriate drain efficiency. Fig. 6.16(c) depicts the simulated 25% drain current of $I_{path,p}$ and $I_{path,n}$. To achieve the highest possible RF power and drain efficiency, as could be seen, the NMOS power switches must carry almost 400 mA while they enter in the triode region. Indeed, these NMOS switches operate in a "voltage limited" regime [97]. Within this region of operation, the drain-source voltage of the switches become minimal which subsequently cause the drop of the drain current. The dimple at the peak of the drain current in Fig. 6.16(c) indicates that the switches operate in a "voltage limited" regime. Note that, in the lower power mode of operation in which the turn-on power switches are fewer, the DPAs operate in a "current limited" regime that the NMOS power switches work at in the saturation region. The eventual peak RF output power of the I/Q RF-DAC exceeds 22.4 dBm while the drain efficiency including power combining network losses (η) is better than 44%. Also, the appropriate modulation accuracy of I/Q RF-DAC could be quickly ascertained from Fig. 6.16(a)-(b),(d). Based on these simulations, the IQ signal is the result of orthogonally summing of I and Q signals (IQ=I$\angle(\pi/4)$).

6.7 Conclusion

In this chapter, the theory and the design procedure of an innovative, differential, orthogonal power combining network, which is employed in the proposed all-digital modulator, is thoroughly explained. It is demonstrated that, in order to maintain an orthogonal operation between the in-phase and quadrature-phase paths, the effect of the power combiner on the in-phase and quadrature-phase paths must be considered, otherwise, the linear summation will not occur. As a result, the EVM and linearity performance will diminish. The power combiner consists of a transformer balun as well as its related programmable primary and secondary shunt capacitors. In order to achieve high efficiency at full power of operation, a class-E type matching network is adopted and subsequently modified in order to obtain a minimum modulation error. A switchable cascode structure is exploited to mitigate a relia-

[9]Note that due to the fact that the DPA unit cell is, indeed, a switchable cascode structure, the peak gate-drain voltage could be as high as 2.2 V provided that one or more cascode switches are off (i.e., the gate of cascode switch is shorted to ground). Based on the study in [98], the gate-drain breakdown voltage in 65-nm CMOS could be as high as 2.1 V. As a result, the breakdown will not occur. This assumption has also been verified in the lab: The RF-DAC test-chip has been measured over long time and no performance degradation has been observed. This indicates that the gate-drain breakdown does not occur.

bility issue as well as to perform a mixer operation. Moreover, utilizing a switchable cascode structure also improves the isolation between quadrature paths. Furthermore, it is explained that the power combiner efficiency is primarily related to the transformer balun efficiency. A procedure is introduced in order to design an efficient, compact balun transformer. Also, it is explained that the RF-DAC operates as a class-B power amplifier at the power back-off levels. As a result, its performance in the power back-off region is lowered.

Chapter 7

A Wideband 2×13-Bit All-Digital I/Q RF-DAC

This chapter comprehensively explains the circuit level design of the 2×13-bit all-digital I/Q RF-DAC [70, 71]. The measurement result of this chip will be subsequently revealed in the following chapter, i.e. Chapter 8. Fig. 7.1 exhibits a block diagram of the implemented 2×13-bit RF-DAC transmitter. In the remainder of this section, its building blocks will be sequentially disclosed and their circuit design techniques described. Section 7.1 discusses the input transformer which converts a 4× single-ended clock into a differential one. Section 7.2 reveals high-speed low-noise divide-by-2 circuits which are employed as dividers throughout the chip. Section 7.3 reveals the high-speed rail-to-rail complementary quadrature sign bit while Section 7.4 introduces the utilized 25% duty cycle generator. The floorplan of the DRAC is proposed in Section 7.5 which requires its related binary-to-thermometer encoder addressed in Section 7.6. The design of MSB and least significant bit (LSB) DRAC unit cell is discussed in Section 7.7 while the philosophy supporting the selected segmentation configuration is revealed in Section 7.8. The digital calibration techniques as well as DPD procedures are addressed in Section 7.9. Finally, Section 7.10 concludes the chapter.

7.1 Clock Input Transformer

An off-chip single-ended clock at $4\times f_0$ frequency is applied to an on-chip transformer to convert it to differential clock signals (ck_4^+/ck_4^-). The transformer size is selected at 150×150 μm^2 with 1:1 turns ratio while the center tap is located at its secondary winding and connected to a common mode voltage of $V_{DD}/2$. The windings are 6 μm wide with 3 μm gaps in-between. Momentum simulation demonstrates that the coupling factor within a frequency range of 7 to 13 GHz is $k_m \approx 0.625$. Note that the simulated k_m is related to the coupling

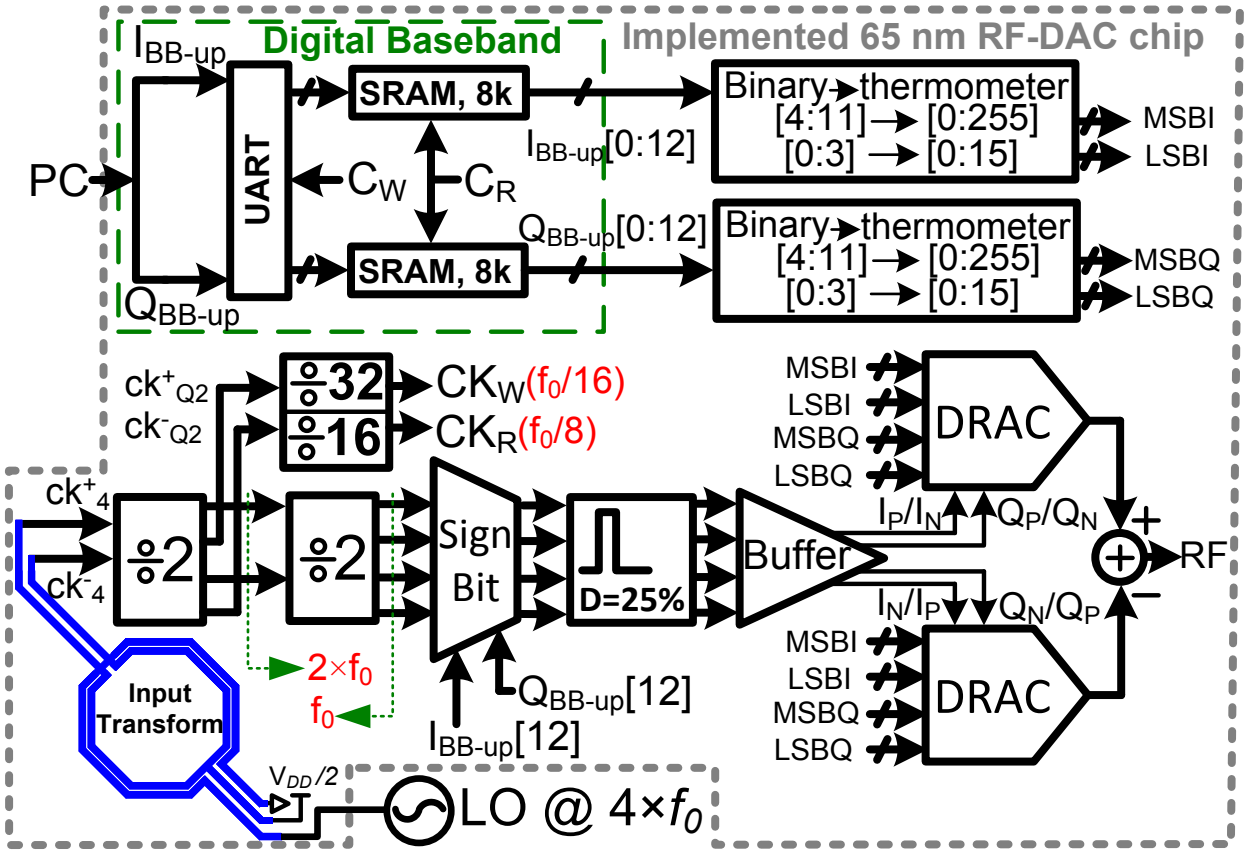

Figure 7.1: Block diagram of the implemented transmitter based on 2×13-bit all-digital I/Q RF-DAC.

between the input and output turns of the transformer. Based on that, the circuit simulations indicate that the transformer converts a $3.84\,\mathrm{V}_{p-p}$ single-ended clock to $2{\times}1.2\,\mathrm{V}_{p-p}$ differential signals that swing around $V_{DD}/2$.

Due to non-identical differential layout traces that introduce differing parasitic capacitance, the differential signals could arrive at the following ÷2 divider misaligned and that might corrupt its operation. Therefore, the phases of ck_4^+/ck_4^- clocks are aligned employing back-to-back inverters.

7.2 High-Speed Rail-to-Rail Differential Dividers

The differential $4 \times f_0$ clock, ck_4^+/ck_4^-, is applied to two cascaded ÷2 dividers to generate the desired carrier LO at f_0 (see Fig. 7.2(a)-(b)). The ÷2 divider is implemented as a flip-flop based frequency divider which consists of four C^{2}MOS latches [74] arranged in a loop (Fig. 7.2(c)). This topology produces four differential quadrature clock signals (ck_{I2}^+, ck_{Q2}^+, ck_{I2}^-, and ck_{Q2}^- in Fig. 7.2(a)) that operate at $2f_0$. The back-to-back inverters of Fig. 7.2(c)

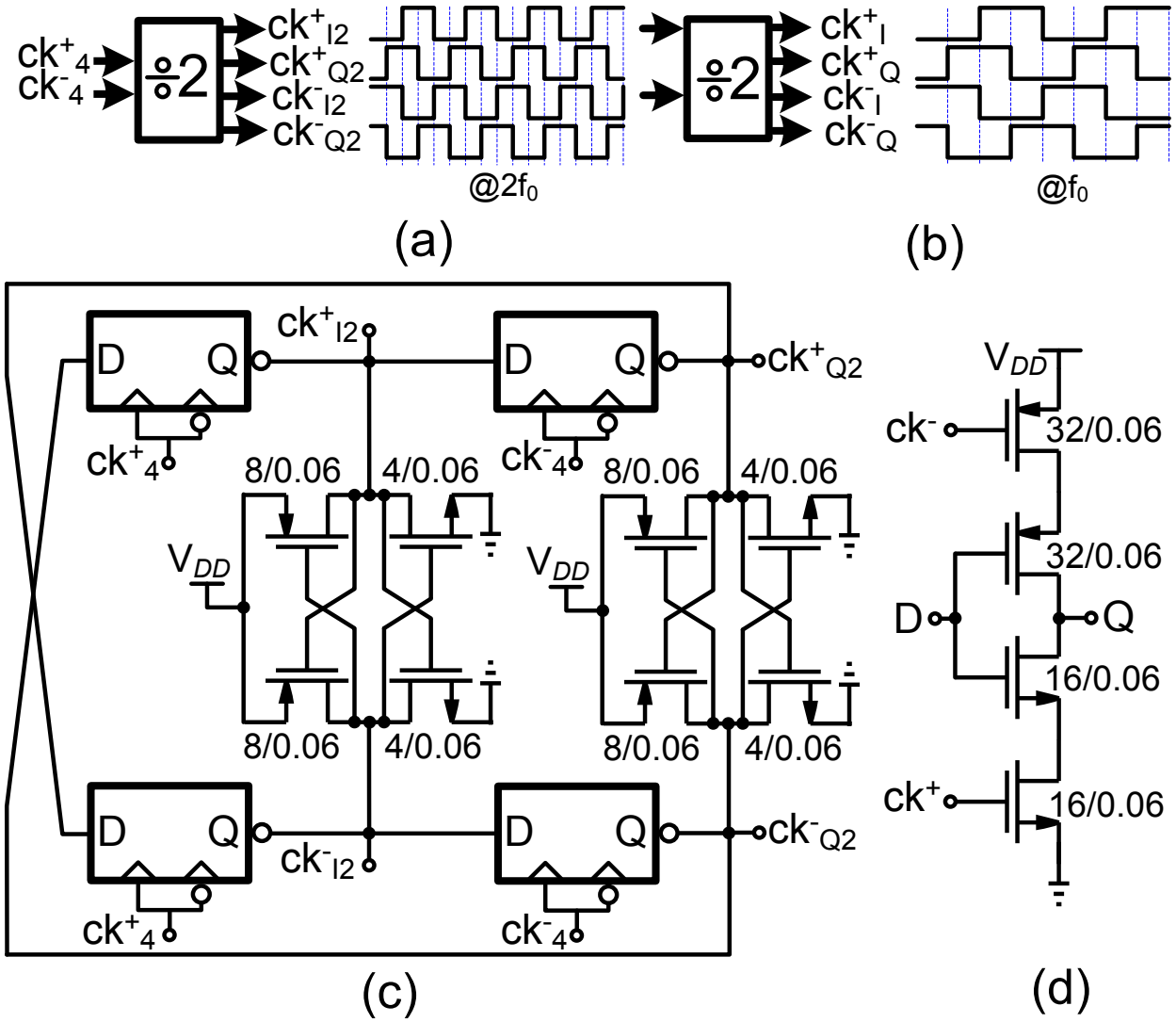

Figure 7.2: Clock ÷2 dividers with corresponding waveforms: (a) first; and (b) second; (c) schematic; (d) C^{2}MOS latch with swapped data/clock inputs.

ensure that no illegal states will occur. They also align the differential clock phases (ck^+_{I2}/ck^-_{I2} and ck^+_{Q2}/ck^-_{Q2}). The input and output nodes of C^{2}MOS latches experience rail-to-rail voltage swing. Consequently, they exhibit a superior noise performance over the low-swing current-mode logic (CML) latches. On the other hand, due to their high current bias and lower voltage swing, the operational frequency of the CML latches can be much higher than that of C^{2}MOS. Since the noise performance and power consumption are crucial design considerations and recognizing that the speed advantages of the CML latches are not always needed, the C^{2}MOS latches are thus adopted in this instance. The $2f_0$ clock signals, however, could be as high as 7 GHz and the divider should be operational for all process, voltage, and temperature (PVT) conditions, which might be difficult to achieve. Dissipating more

current (e.g., by employing wider transistors) could improve the speed of C^{2}MOS latches as the supply voltage is fixed. Hence, their power consumption increases, which would decrease the overall system efficiency of the transmitter.

In this work, however, in lieu of increasing the power, the data and clock inputs of C^{2}MOS are swapped (Fig. 7.2(d)). By doing so, the D-to-Q delay of the latch and, subsequently, the overall loop time period of the divider, decreases. Based on simulation and measurement results, the RF-DAC frequency of operation can be as high as 3.5 GHz at V_{DD} ≤1.3 V. Note that all other ÷2 divider circuits also utilize the same structure. The transistor sizing, however, is adjusted based on its operational frequency. For instance, the width of all transistors in the next ÷2 divider in both the main RF clock path (÷2) as well as the baseband clock path (÷16/32) of Fig. 7.1 are reduced by a factor of two. Furthermore, every other differential output clock of the first divider (ck_{2I}^{+}/ck_{2I}^{-} and ck_{2Q}^{+}/ck_{2Q}^{-}) is applied to the next divide-by-two circuits. By doing so, all C^{2}MOS latches experience identical loading conditions. Thus, their fan-outs are equal.

Note that all clocks in the digital baseband circuitry (CK_W and CK_R) as well as the final RF fundamental clocks, I_P, Q_P, I_N, and Q_N, are synchronized. The amplitude and phase imbalances of the I and Q paths would deteriorate the IQ image and leakage performance of the transmitter, thus they should be calibrated. The baseband and RF phase synchronization makes the IQ calibration much simpler. Furthermore, employing two cascaded ÷2 dividers (i.e., divide-by-4 circuit) will ameliorate the quadrature accuracy of the fundamental clocks since all the phases of the fundamental f_0 clock are derived from the same rising edge of the $4 \times f_0$ master clock even in face of a non-50% duty cycle.

7.3 Complementary Quadrature Sign Bit

As depicted in Fig. 7.1, the second ÷2 divider is followed by a sign bit circuitry (see Fig. 7.3(a)). It is implemented as two pseudo-differential (i.e., complementary) NAND-gate-based multiplexers with input selection control signals I_{BB-up}[12] and Q_{BB-up}[12]. Based on the 2-bit (i.e., 4-state) selection control, the differential clock pairs of ck_I^{+}/ck_I^{-} or ck_Q^{+}/ck_Q^{-} can be swapped and thus the entire 4-quadrant constellation diagram can be addressed (see Fig. 7.3(b)). Contradictory to Section 4.1.4([67], [69]), the sign bit is located between the second divider and the 25% duty-cycle generator. In this new arrangement, the sign bit circuitry manages the 50% duty cycle clock instead of 25%, which reduces power consumption. Moreover, a simple back-to-back inverter pair (see Fig. 7.3(a)) is employed for further phase alignment which was not feasible in Section 4.1.4([67], [69]).

As a result, by exploiting smaller devices, faster rise/fall times are achievable. Moreover, compared to the transmission-gate-based multiplexer used in Section 4.1.4([67], [69]), the NAND-based multiplexer produces faster rise/fall times. This is because, in the transmission gate, the charging/discharging of the MOS channel is decelerated (see Fig. 4.6(a)).

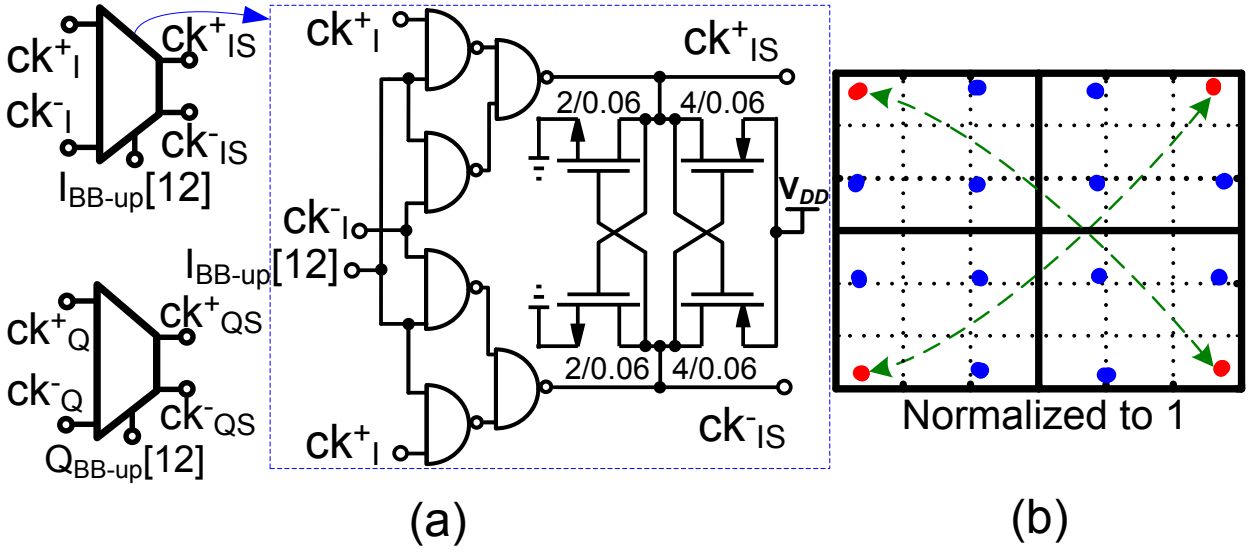

Figure 7.3: (a) Complementary NAND-gate-based sign-bit multiplexer symbol and its related schematic; (b) 16-point constellation diagram.

7.4 Differential Quadrature 25% Duty cycle Generator

The sign bit outputs of ck^{+}_{IS}, ck^{+}_{QS}, ck^{-}_{IS}, and ck^{-}_{QS} are applied to a 25% duty cycle generator (see Fig. 7.4(a)). As stated previously, the orthogonal summing of the I and Q paths is achieved by employing the differential quadrature clocks with a 25% duty cycle. As a result, the 25% duty cycle generator is one of the most important building blocks of the clock generator chain.

The circuit utilized in Section 4.1.3([67], [69]) provides unmatched narrow/wide clock pulses. It signifies that the duty cycle for one pulse might be 31% while 27% for the others. In this work, however, the 25% duty cycle circuit generator of [60] is adopted. It is conceptually illustrated in Fig. 7.4(a). Based on this approach, the 25% clocks at f_0 (ck^{+}_{ID}, ck^{+}_{QD}, ck^{-}_{ID}, and ck^{-}_{QD}) are generated by an AND operation between clocks of (ck^{+}_{I2}/ck^{-}_{I2}) and (ck^{+}_{IS}/ck^{-}_{IS}, $ck^{+}_{QS}/\ ck^{-}_{QS}$) where they operate at $2f_0$ and f_0, respectively. Thus, the 50% duty cycle clocks of ck^{+}_{I2}/ck^{-}_{I2} are used as a reference pulse width for generating ck^{+}_{ID}, ck^{+}_{QD}, ck^{-}_{ID}, and ck^{-}_{QD}. Namely, their pulse width is the same as ck^{+}_{I2}/ck^{-}_{I2} while operating at f_0. Hence, the circuit creates clocks with a precise 25% duty cycle.

The AND operation of the 25% duty cycle generator as well as the sign bit are accomplished utilizing Fig. 7.4(b). This is an asymmetric circuit with respect to the gates of M_{N1} and M_{N2}. The gate capacitance of M_{N2} is smaller than of M_{N1} due to the cascode configuration of M_{N1}/M_{N2}. Otherwise stated, C_{gs} of M_{N2} is in series with the combination of drain-bulk capacitance of M_{N1} and source-bulk capacitance of M_{N2} while C_{gs} of M_{N1} is directly connected to the ground. Therefore, ck^{+}_{I2} and ck^{+}_{IS} are applied to the M_{N2} and M_{N1} gates, respectively. Thus, the AND gate consumes less power. Note that the desired 25%

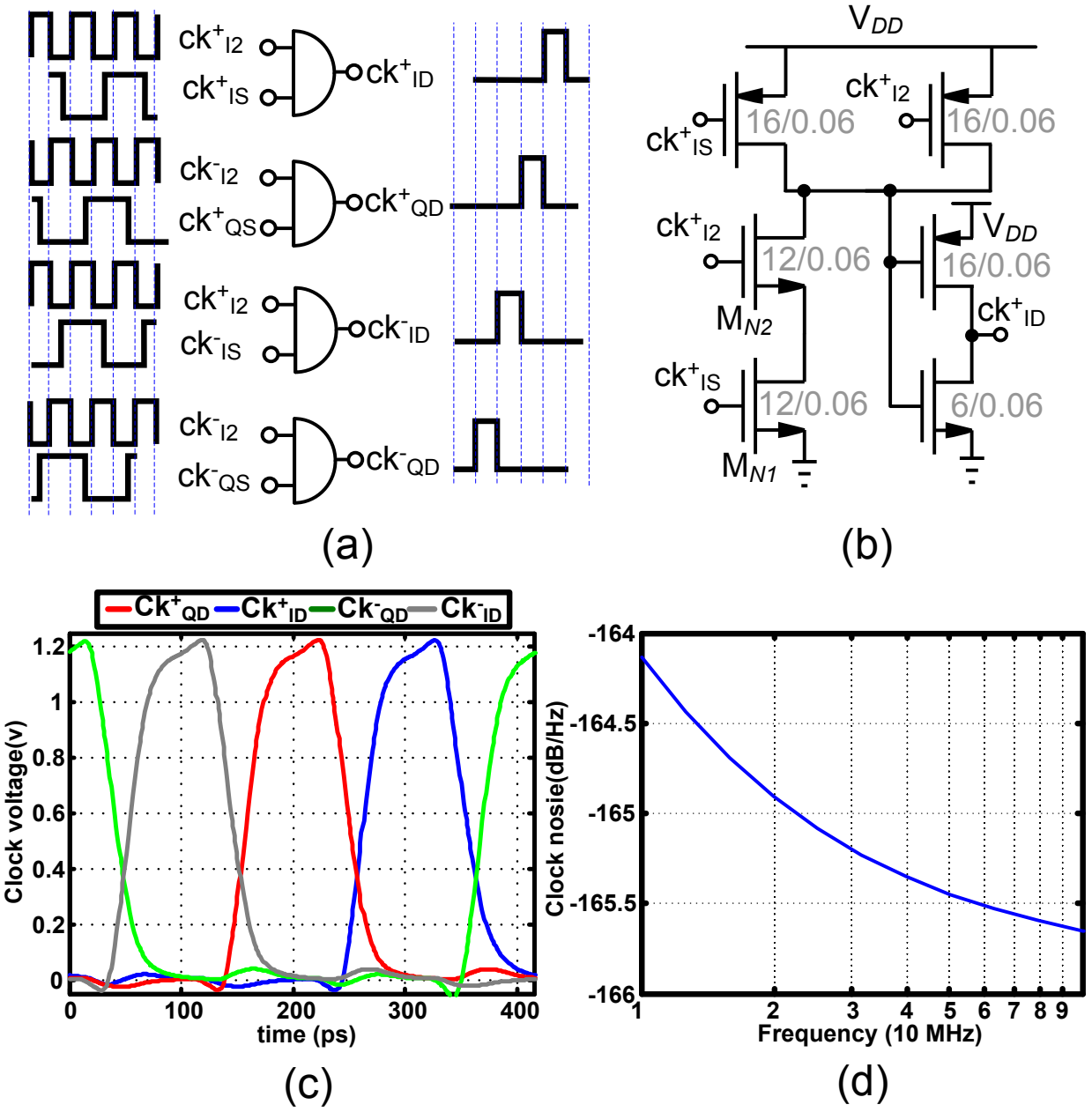

Figure 7.4: (a) 25% duty cycle generator schematic [60]; (b) its AND logic circuit. Post layout simulation results of the clock generation part: (c) 25% clock waveforms; (d) their corresponding clock phase noise.

duty cycle clocks could also be generated using an AND operation of every two adjacent clocks of ck^{+}_{IS}, ck^{+}_{QS}, ck^{-}_{IS}, and ck^{-}_{QS}. The disadvantages would be the asymmetric AND inputs that create unmatched wide/narrow pulses. Thus, the circuit illustrated in Fig. 7.4(a) is the preferred approach.

The post layout simulation results of the differential quadrature clocks of ck^{+}_{ID}, ck^{+}_{QD},

ck_{ID}^{-}, and ck_{QD}^{-} are depicted in Fig. 7.4(c). All clock signals comprise a 25% duty cycle and, most importantly, are matched to each other. Note that their corresponding rise time and fall time will be improved later by utilizing a number of appropriate clock buffers. Furthermore, the post layout clock phase noise is simulated and depicted in Fig. 7.4(d) for the frequency offset range of 10 to 100 MHz. According to this simulation result, the clock noise floor is better than -164 dBc/Hz, which is an adequate number. Thus, the RF-DAC noise floor is primarily limited to the clock generation circuitry, and it will be verified by measurement results.

7.5 Floorplanning of 2×13-bit DRAC

As mentioned previously, the targeted transmitter is an all-digital RF-DAC with 2×13-bit (including sign bit) resolution. I_{BB-up} and Q_{BB-up} represent binary digital codes which must be converted to thermometer codes in order to avoid non-monotonic behavior and mid-code transition glitches [80, 99–101][1]. The use of the pure thermometer code, however, increases the complexity of the encoders, the chip area, interconnect parasitics, and power consumption. Thus, a segmented approach is adopted in this aspect [102]. The segmentation is selected such that 8 bits are used for the MSB and 4 bits for the LSB of the binary input. The philosophical explanation of the selected MSB and LSB in this segmentation arrangement will be disclosed later in Section 7.8. Therefore, the DRAC implementation requires 256 MSB and 16 LSB units.

The design of such a complex RF-DAC requires several iterations between the schematic and layout. The 256 MSB units further split into two sections while the clock generator circuits are situated in the middle (see Fig. 7.5(a)). Moreover, the 128 MSB units of each part are arranged such that they comprise 8 rows and 16 columns (8×16). Subsequently, the I/Q segmented thermometer code requires two types of in-phase and quadrature-phase baseband row and column thermometer codes which are referred to as Row_I/Row_Q as well as Col_I/Col_Q and are generated by row and column encoders. The right MSB unit bank covers the low thermometer code values (i.e., 0–127) while the remaining (i.e., 128–256) are managed by the left bank. Furthermore, the LSB unit comprises 16 small DRAC unit cells which occupies only one row (1×16) at the bottom of the right MSB DRAC unit bank. The MSB DRAC units in each row must be situated in close proximity to each other. Moreover, the dummy DRAC cells are placed at the beginning and end of each row which globally improves the matching of the DRAC unit cells with respect to each other.

In addition, odd rows begin from the left side while the even rows begin from the

[1]Glitches occur when the switching time of different bits in a binary weighted DAC is unmatched, and they add a signal dependent error to the output signal. Moreover, the glitches can be produced by the dynamic behavior of the switches such as charge-injection and clock feedthrough. The generated power of glitches should be less than quantization noise so as to not degrade the dynamic range of RF-DAC.

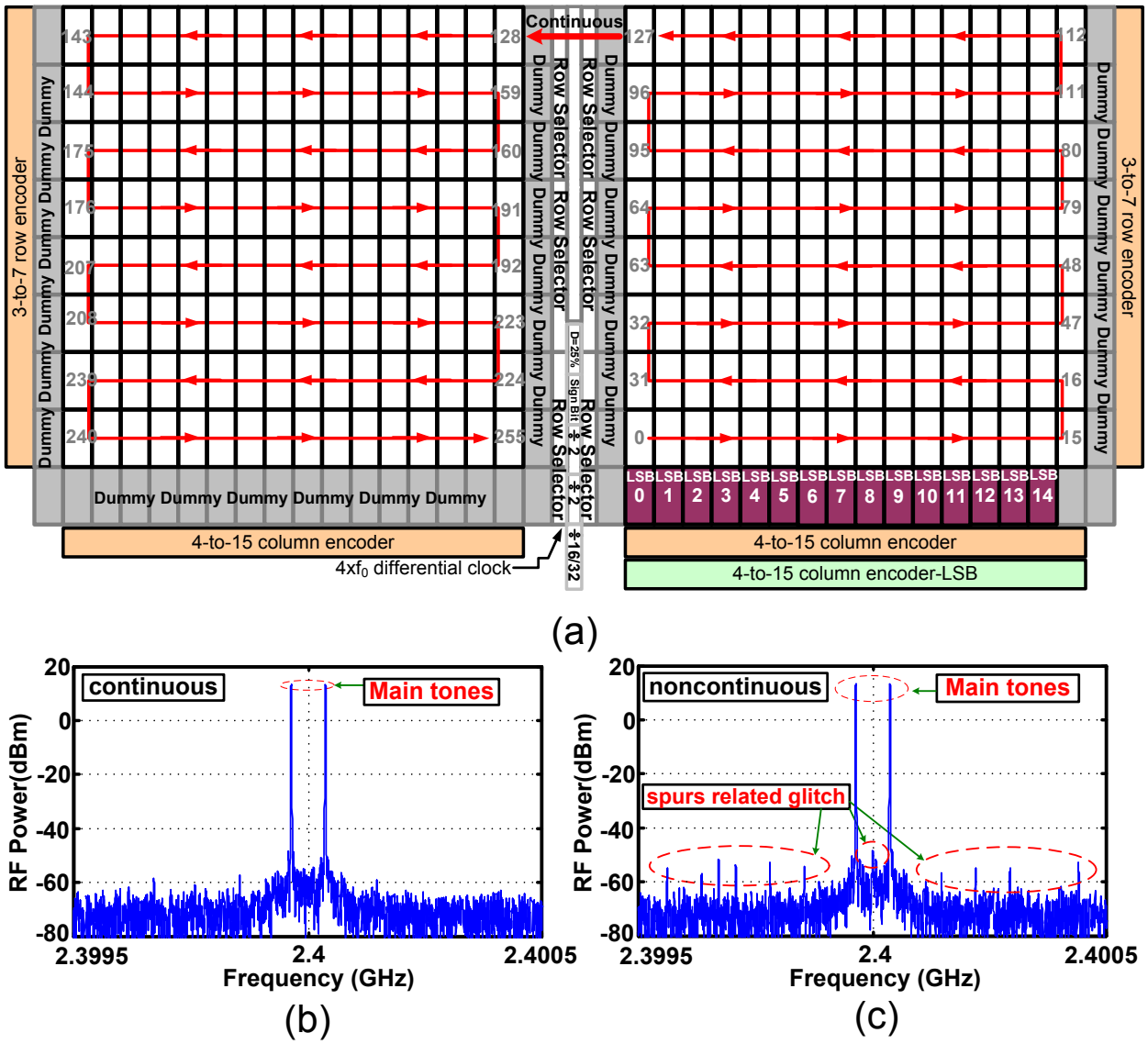

Figure 7.5: (a) 2×13-bit DRAC floor plan. (b) One row detail. (c) Continuous traversal: glitch free spectrum; (d) non-continuous traversal: spectrum with glitches.

right side. This "snake" traverse movement is indicated with arrow lines in Fig. 7.5(a). By doing so, the MSB thermometer units are continuously traversed from an odd to an even row and vice versa. As a result, the differential nonlinearity (DNL) of RF-DAC as well as the glitch related to the dynamic switching of DRAC units are retained below one LSB. Note that the clock trees (clock generating blocks) force DRAC to split into two sections, thus, there would be unavoidable discontinuity between the left and right DRAC banks which would possibly introduce considerable glitches. In order to cross over from the right bank to the left one, the DRAC must adopt the nearest possible path, which is the direct path between cell 127 and 128. This movement is, indeed, referred to as continuous traverse and is indicated in Fig. 7.5(a). On the other hand, if the DRAC might intentionally

follow the faraway probable, hypothetical path, which is the path between cell 127 and 255, consequently, a non-continuous traverse would have occurred. To further justify it, Figs. 7.5(b)-(c) compare the two aforementioned movement scenarios from the right bank to the left one, i.e., continuous and intentionally noncontinuous traverse. Fig. 7.5(c) illustrates that noncontinuous movement generates a significant number of spurs and should thus be avoided. Therefore, as exhibited in Fig. 7.5(a), the movement from the right bank to the left must be performed gently. In conclusion, the continuous traverse, prudent layout as well as employing dummy cells would almost entirely eliminate the dynamic glitch problem.

7.6 Thermometer Encoders of 3-to-7 and 4-to-15

Based on the above segmented arrangement, two 3-to-7 and three 4-to-15 (including the LSB encoder) binary-to-thermometer encoders are employed (five in total) and placed at the left, right, and bottom sides of the DRAC (see Fig. 7.5(a)). The encoders are implemented based on a 2-to-3 binary-to-thermometer encoder depicted in Fig. 7.6(a). In this approach, the LSB (BB_0) and MSB (BB_2) of the thermometer code are produced by OR and AND operations of the two input binary bits (A_0 and A_1), respectively. Moreover, the middle bit of the thermometer code (BB_1) is equal to the input MSB (A_1). The 3-to-7 encoder, however, is implemented in two increments. First, the intermediate 3-bit thermometer codes of Fig. 7.6(a) are created. Using these codes, B_0, B_1, B_2, B_4, B_5, and B_6 bits of the eventual seven-bit thermometer code are generated by OR and AND operations of BB_0, BB_1, BB_2 by A_2, respectively. Moreover, B_4 is also equal to A_2 (Fig. 7.6(b)). Similarly, the 4-to-15 encoder (see Fig. 7.6(c)) is created in two increments employing intermediate 3-to-7 thermometer bits and again applying OR/AND logic operations of the intermediate bits with A_3.

7.7 DRAC Unit Cell: MSB and LSB

The DRAC design was fully described in Section 6.1. In this section, the DRAC unit cell is explained in more detail. The MSB DRAC unit is illustrated in Fig. 7.7(a). This unit consists of four equal and well-matched subsections (sub-DRAC) each comprising its own data and clock inputs. The quadrature input clocks are I_P, Q_P, I_N, and Q_N and, based on these signals, the sub-DRACs are referred to as SD_{IP}, SD_{QP}, SD_{IN}, and SD_{QN}, respectively. Moreover, as mentioned earlier, the related input data thermometer bits are Row_I, Col_I, Row_Q, and Col_Q along with two extra control bits of Row_{I+1} and Row_{Q+1} in which they guarantee that all DRAC unit cells of the previous rows are activated. The sub-DRAC section comprises two parts; a pure digital (logic) and a digital-to-RF conversion part.

The logic part consists of a decoding logic (AND-OR) and a time synchronizer flip-flop. Based on logic condition of its inputs, the AND-OR decoder (see Fig. 7.7(b)) determines

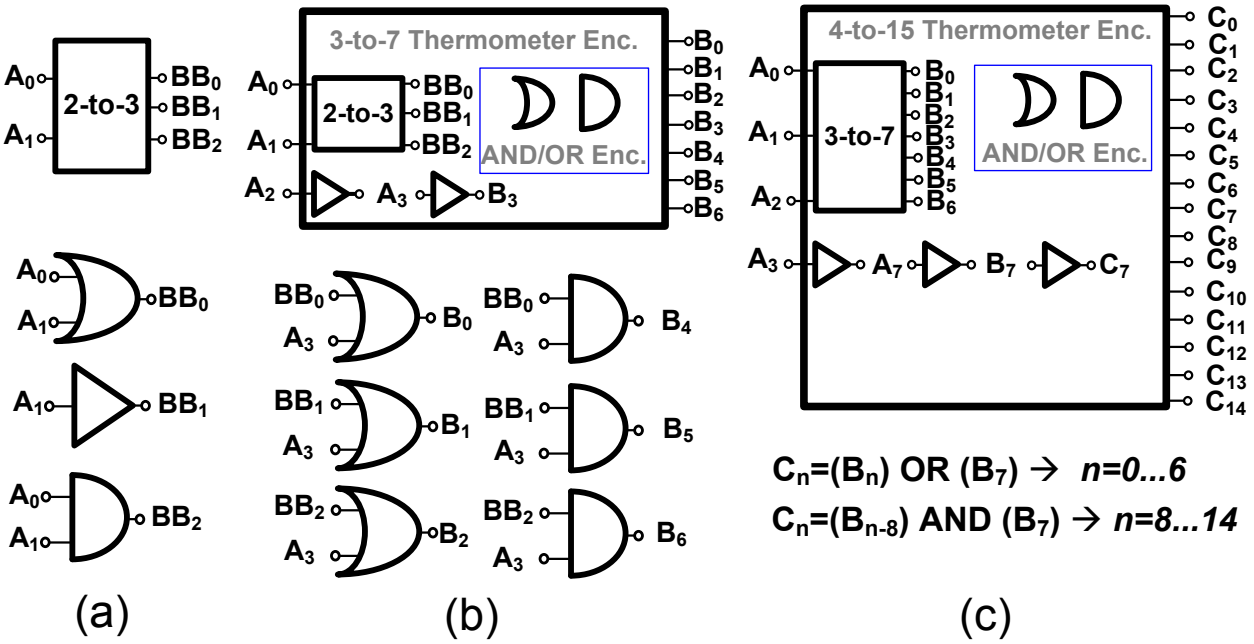

Figure 7.6: (a) 2-to-3; (b) 3-to-7; and (c) 4-to-15 thermometer encoders.

whether or not the sub-DRAC cell should be activated. The master/slave edge triggered flip-flop is employed for synchronizing all DRAC unit cells to its input clock, namely CI_P, CQ_P, CI_N, and CQ_N, in order to reduce undesirable harmonic distortion related to early-late arrival of input data of each DRAC unit cell. Additionally, this flip-flop also behaves as a ZOH interpolator. It comprises two cascaded multiplexer based latches [74], as shown in Fig. 7.7(c). In the sense mode of operation, the input clocks CK_P/CK_N are low/high and, consequently, the input data (D_I) passes through the "lower" pass-gate logic of M_1/M_2 and is subsequently buffered by the cascaded inverters of M_3/M_4 and M_5/M_6. It signifies that the path between D_I and Q_O is transparent. In the store mode, on the other hand, CK_P/CK_N are high/low and, as a result, the "top" pass-gate logic of M_7/M_8 is transparent, and the "lower" one is opaque. Therefore, the two inverters of M_3/M_4 and M_5/M_6 are cross-coupled with each other and latch the digital input signal. All transistors of both the AND-OR decoder logic and flip-flop circuit are implemented with the most minimal possible aspect ratio in 65 nm CMOS, i.e., $W/L = 0.15\mu\text{m}/0.06\mu\text{m}$ to minimize area and power consumption.

As depicted in Fig. 7.7(a), the flip-flop output of the sub-DRAC cell is buffered and subsequently connected to the cascode transistor (M_2, M_4, M_6 or M_8) to handle the input gate capacitance and, consequently, to improve the rise/fall time performance. As stated previously, the gate capacitance of the cascode transistor with an aspect ratio of $W/L = 8\mu\text{m}/0.06\,\mu\text{m}$ is much lower than the input capacitance of M_1 with the same transistor sizing. Therefore, using a moderated buffer size is sufficient enough to satisfy the required data transition conditions. The buffer sizing is indicated in Fig. 7.7(c).

Note that, in lieu of employing these digital components at every sub-DRAC cells, it

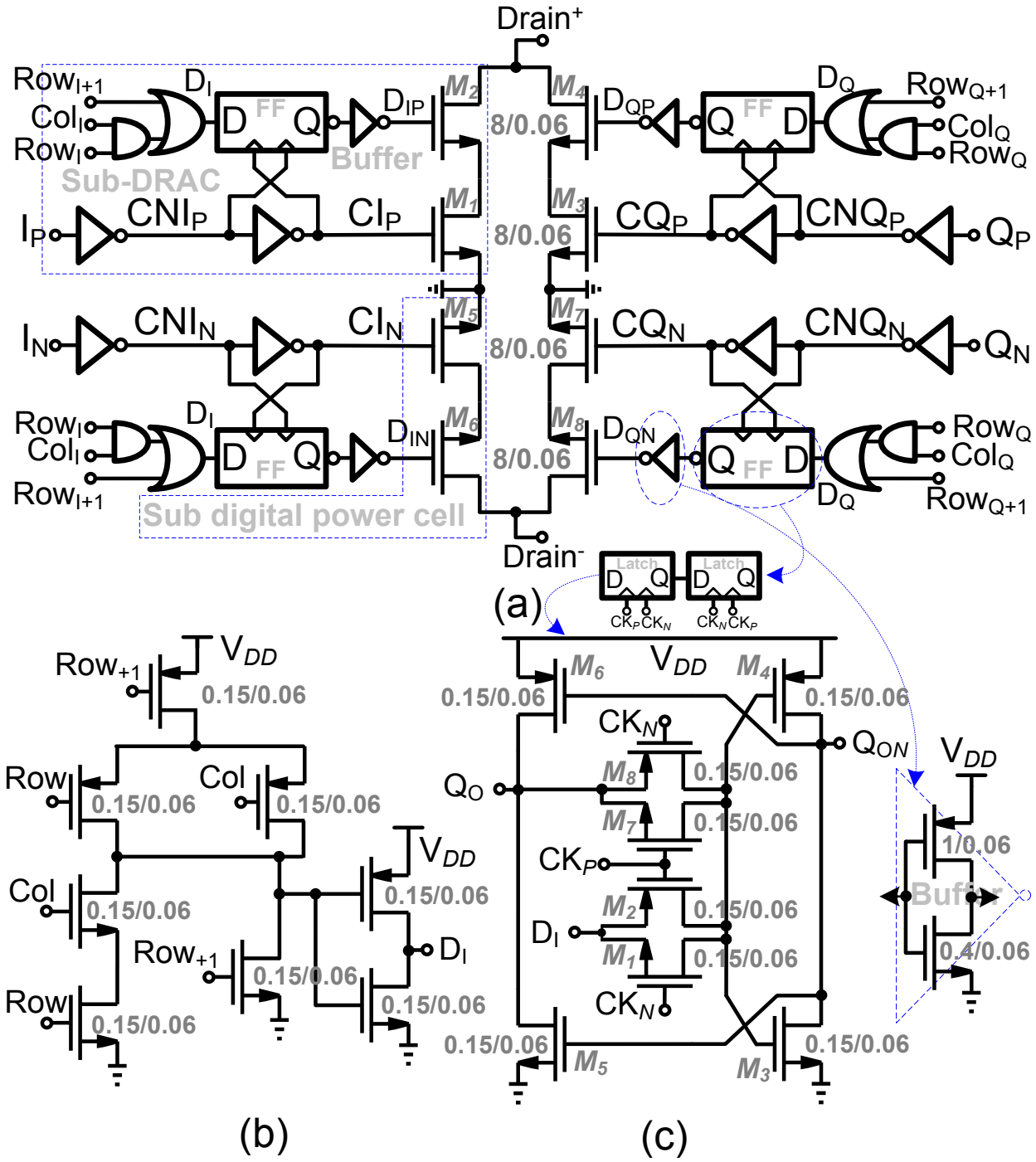

Figure 7.7: (a) MSB DRAC unit cells: pseudo differential quadrature digital power mixer. Schematics of (b) AND-OR decoder; (c) multiplexer based latch including last data buffer.

is feasible to situate them at the on-set of each row and column and share them with the entire row and column. The disadvantages would be inferior timing synchronization as well as greater power consumption due to the fact that they should feed a number of sub-

DRAC cells along with enormous routing metal lines. Moreover, the flip-flop requires as a synchronizing signal either the high-speed upconverting clock or CK_R up-sampling clock. If the digital part is not situated in the DRAC cell and is placed at the on-set of each row/column, consequently, the aforementioned synchronizer clock should also be provided at the beginning of each row/column which results in a more complex layout/floorplanning as well as higher power consumption. As a result, the proposed DRAC cell appears the best viable configuration.

The digital-to-RF conversion part consists of a gated cascode switch (M_1/M_2, M_3/M_4, M_5/M_6, and M_7/M_8) that yields the up-converting 1-bit mixer operation. Furthermore, it is perceived as a sub digital power cell. The cascode transistor (M_2, M_4, M_6, and M_8) alleviates the reliability issue related to the high voltage swing that appears on the output nodes ($Drain^+$, $Drain^-$). Moreover, the cascode configuration also increases the output impedance, which results in improved isolation between the I and Q paths that assists with improved orthogonal combination. The overall quadrature mixer digital power unit cell is formed by electrically combining the outputs of two individual quadrature upconverter mixers (the upside M_1–M_4 and downside M_5–M_8 of Fig. 7.7(a)) that are driven by quadrature input clocks (which also act as four sub digital power cells). Consequently, the entire RF-DAC is now created by simply connecting the corresponding drain nodes of each 256 MSB along with 16 LSB DRAC unit cells together.

As stated, each DRAC unit cell consists of SD_{IP}, SD_{QP}, SD_{IN}, and SD_{QN} unit cells, and their layout arrangement affects the performance of the entire RF-DAC. Fig. 7.8(a) shows one possible solution in which each quadrature sub-DRAC pair, i.e., SD_{IP}/SD_{QP} and SD_{IN}/SD_{QN}, is juxtaposed in two different sub-rows which indicates that the DRAC unit cell is expanded horizontally. In this arrangement, the high-frequency 25% duty cycle quadrature clock pairs of I_P/Q_P and I_N/Q_N are laid out alongside each other. This, subsequently, increases the parasitic coupling capacitance of these clock lines and, as a result, deteriorates the clock rise/fall times. Moreover, since the position of Q_P/Q_N clock lines are different than I_P/I_N, their line capacitances also vary. Thus, Q_P/Q_N and I_P/I_N clock pulses are narrower and wider, respectively. Post-layout circuit simulations of Fig. 7.8(a) demonstrate the rise/fall time as well as narrow/wide pulse problems related to the horizontal layout.

The better solution, however, is to expand the DRAC unit cell vertically and place SD_{IP}, SD_{QP}, SD_{IN}, and SD_{QN} sub-DRAC unit cells in four sub-rows, as illustrated in Fig. 7.8(b). In this arrangement, the parasitic coupling capacitance between the clock lines are almost negligible. The clock lines are also situated in the same positions and are sandwiched between the same sub-DRAC cells. Hence, their related rise/fall time and pulse width are matched with one another. Post-layout simulations in Fig. 7.8(b) substantiate that the vertical expansion is the most appropriate selection. To compensate for the extra vertical area related to the vertical expansion of DRAC unit cell, the entire 256-MSB-cell, as stated previously, comprise 8 rows and 16 columns. Thus, left/right MSB DRAC banks

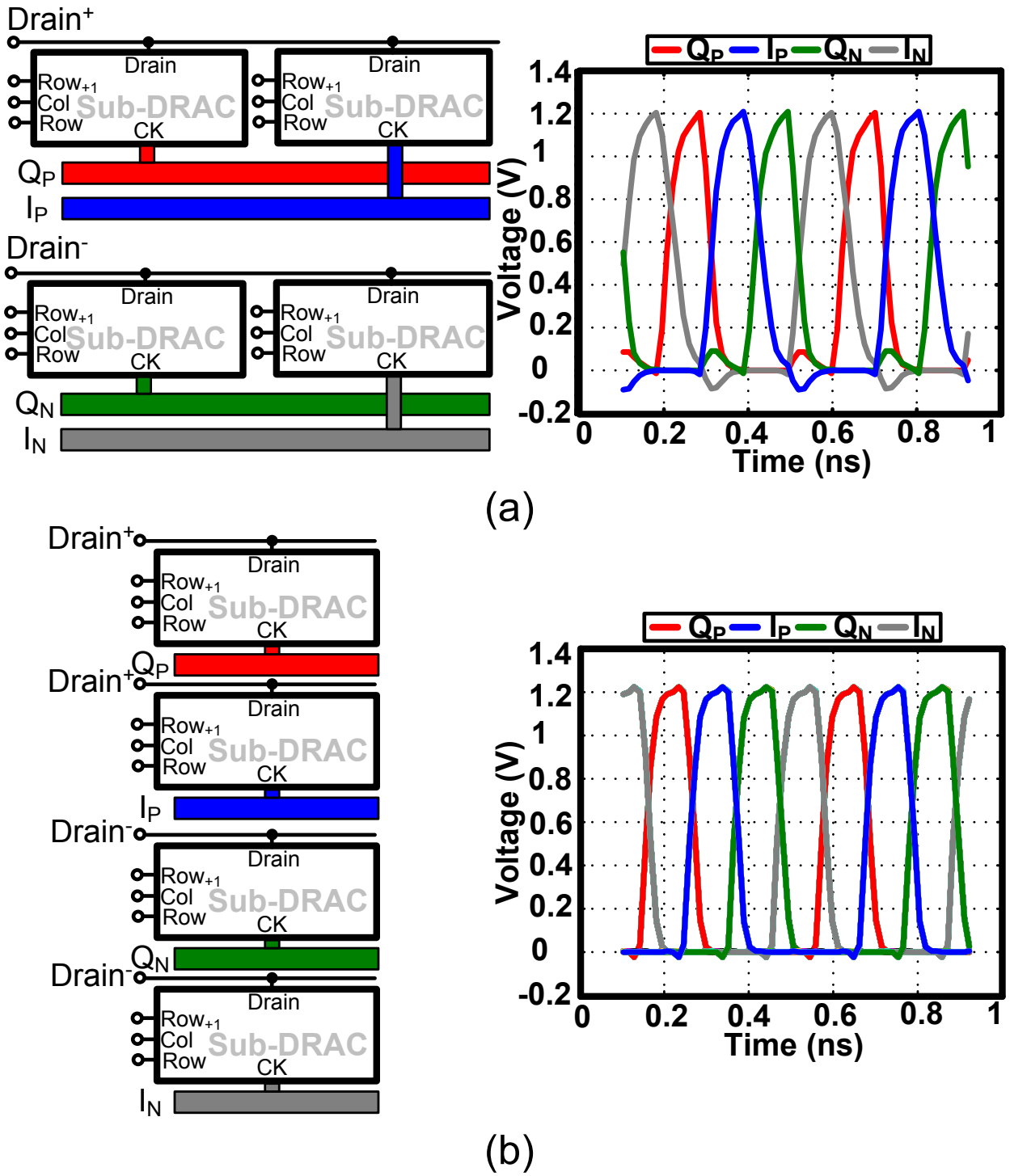

Figure 7.8: DRAC unit sub cells layout: (d) Horizontal; and (e) vertical with their related differential quadrature clock simulations.

become "squarish", which is beneficial for improved area efficiency and shorter clock distribution (i.e., less power dissipation). Fig. 7.9(a) exhibits the eventual DRAC row employing

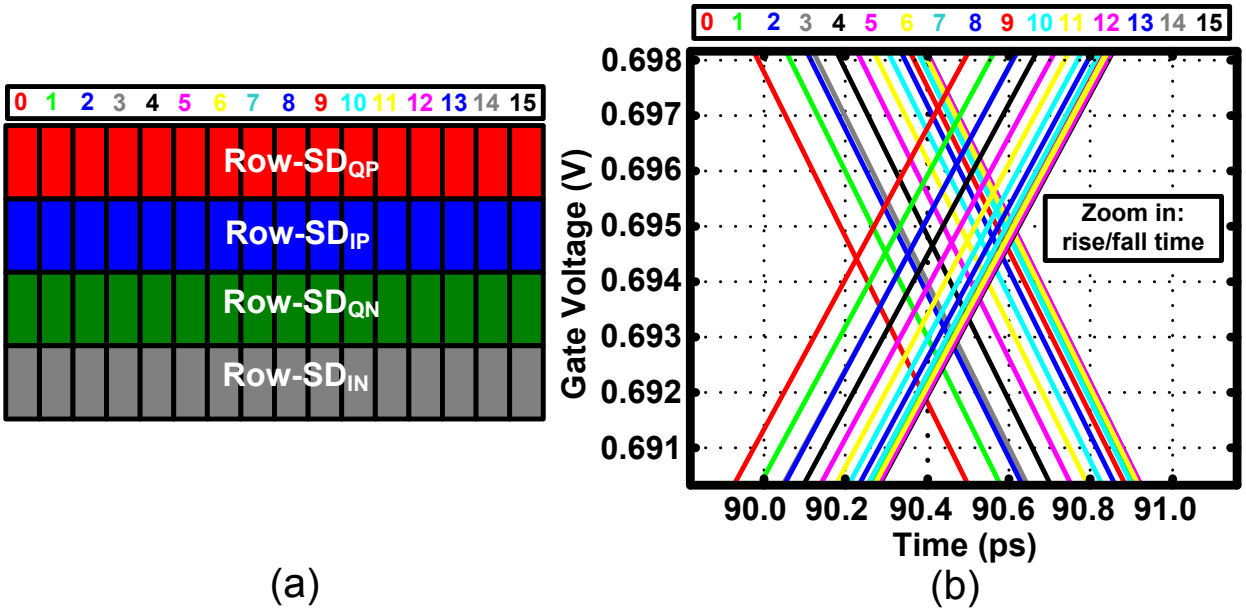

Figure 7.9: (a) DRAC row layout of Fig. 7.5; (a) Its corresponding gate voltage simulations.

vertical layout solution of Fig. 7.8(b). Note that each DRAC unit cell should be clocked almost simultaneously, otherwise, the AM-AM and AM-PM nonlinearity emerge. Based on the post layout simulation results of multiple rows of Fig. 7.5, the time difference between the first (0-cell) and the last column (15-cell) is less than 500 fs, which is a very minimal delay and will not affect the performance of I/Q RF-DAC. Furthermore, according to post layout simulation results, the rise/fall time at all temperature and process corners does not exceed 50 ps. Note that, based on the discussion in Chapter 6, the proposed I/Q RF-DAC can tolerate more than 80 ps rise/fall time while f_0=2.4 GHz.

7.8 MSB/LSB Selection Choices

As stated, each left/right DRAC banks should be arranged such that they comprise X row and Y column in which $Y = 2 \times X$ to maintain their squarish layout form. As mentioned, the DRAC requires a large number of binary-to-thermometer encoders due to employing the thermometer code. As disclosed, each $(\log_2 Y)$-to-$(Y-1)$ binary-to-thermometer encoder is constructed employing a sub $(\log_2 X)$-to-$(X-1)$ binary-to-thermometer one. Nonetheless, employing the pure 100% thermometer code, increases complexity of the subsequent encoders, the chip area, interconnect parasitic and, most importantly, power consumption. Thus, the segmentation approach is adapted which consists of an MSB and an LSB part. The minimum number of LSB is 2 bits. Thus, in that case, each left/right MSB DRAC banks comprise 9 bits while, in each bank, $X = 16$ and $Y = 32$. As a result, they require two 4-to-15 as well as two 5-to-31 encoders. Employing the aforementioned structure in

65 nm CMOS will still not be an adequate or reasonable approach as it occupies more area, adds design complexity and, on top of that, dramatically increases the power consumption. Consequently, the following arrangement is finally adopted: $X = 8$ and $Y = 16$. It should be mentioned that, in the segmentation approach, the selected LSB number of bits should be as small as possible in order to diminish the corresponding DNL, glitches and, in turn, its related distortion. Note that increasing LSB/MSB weight ratio will increase the distortion, hence the optimum ratio must be discovered [99, 100]. For that reason, MSB and LSB are selected as 8 and 4 bits of binary coding, respectively. It should be pointed out that, although, in this work, DPD is employed, it is better to construct a DAC in such a way that it does not require the DPD process to repair the glitches. Note that the DPD also could not manage a substantial amount of distortions which are related to dynamic glitches. Note that the traverse operation in DRAC is an independent operation and does not rely on DPD. In this work, the DPD process is not assigned to remove the gradient mismatch error [2] and its corresponding glitches related to traversing MSB unit cells of the DRAC. As a result, the DRAC arrangement strongly affects the RF-DAC static and dynamic performance. It is worth noting that, as stated, the LSB part of the RF-DAC is also implemented fully segmented in order to affect the following:

1. to improve the matching between LSB cells as well as boost DNL performance;
2. to decrease the glitch related to the dynamic switching of DRAC units.

As previously stated, the segmented LSB approach only requires an extra 4-to-15 binary-to-thermometer encoder which introduces negligible power and area penalty in 65-nm CMOS technology. Fig. 7.10 illustrates the measured DNL of the RF-DAC for which the input code is statically swept from 1 to 40. It should be pointed out that the measured DNL is calculated as follows [78] [79] [80]:

$$DNL(k) = \frac{(V_{out}(k+1) - V_{out}(k)) - \Delta}{\Delta} \tag{7.1}$$

where $V_{out}(k)$ is the RF output voltage of the k-th digital baseband code and the step size Δ is equal to the analog value of LSB. According to the measurement result of Fig. 7.10, the DNL is bounded to a ± 0.2 LSB which indicates an adequate matching between the consecutive codes. As a result, employing a fully segmented LSB part leads to an acceptable matching and, in turn, a reasonable DNL. Note that the jump points at the DNL profile of Fig. 7.10 are related to the transition between the MSB and LSB parts of the RF-DAC.

[2] There are three different types of mismatches: systematic mismatch, random mismatch, and gradient mismatch. The gradient mismatch is related to first or second-order fluctuations over longer length across the chip. It could be minimized by employing similar size, orientation, location, supplies, and also temperature. Moreover, utilizing layout techniques such as common-centroid as well as interdigitation are beneficial.

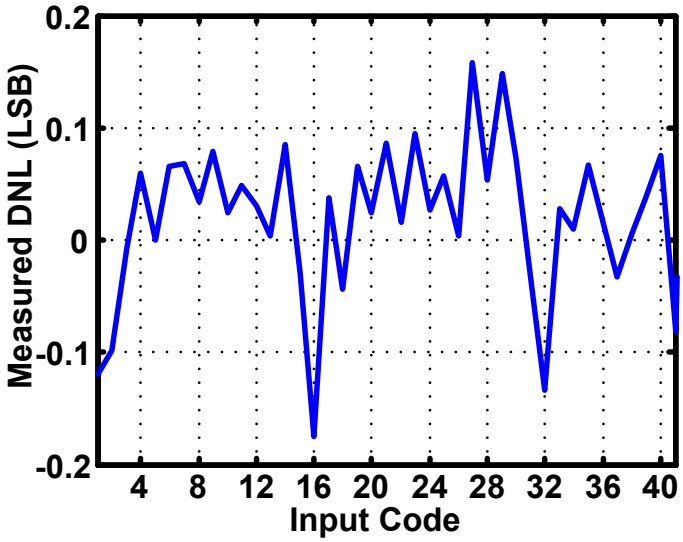

Figure 7.10: The measured Differential nonlinearity of the RF-DAC.

7.9 Digital I/Q Calibration and DPD Techniques

The proposed digital I/Q RF-DAC based transmitter, just as with a typical I/Q transmitter [6] [24], requires an I/Q calibration to balance the I path with respect to the Q path in order to mitigate LO leakage and I/Q image issues. Moreover, as stated above, the I/Q RF-DAC comprises the efficient DPA arrays which produce more than 22 dBm of saturated RF power. Operating at the aforementioned power level leads to compression that causes AM-AM nonlinearity. Otherwise stated, as depicted in Fig. 7.11(a), the G_{on}=$1/R_{on}$ of the turn-on switches changes nonlinearly with respect to the input code and thus creates the AM-AM nonlinearity. Namely, the AM-AM nonlinearity is the result of the code-dependent conductance of the drain node [20]. Furthermore, as stated previously, turning on the switches as well as varying the drain voltage changes the drain-bulk capacitance of the digital power switches (see Fig. 7.11(b)). These varying capacitances in combination with the code-dependent conductance of switches cause a large impedance shift at their related drain nodes, which, subsequently, leads to the AM-PM nonlinearity. Fig. 7.11(c) illustrates the shifting of the load reflection coefficient ($\Gamma_{switch-on}$) of the related DRAC's drain node while sweeping the turn-on switches. Note that both I_{path} and Q_{path} contribute to the AM-AM and AM-PM nonlinearities. In addition, as elaborated above, due to the fact that the passive power combining network affects the RF-DAC's orthogonality, the imperfect orthogonal summing of the I and Q quadrature paths, as a result of inaccurate components of the passive combining network, leads to spectral regrowth [24]. Consequently, the RF-DAC must be digitally predistorted to meet the spectral mask of a communication standard. To address these issues, techniques to address these non-idealities are presented here. It should be pointed out that the following calibration as well as DPD techniques are frequency de-

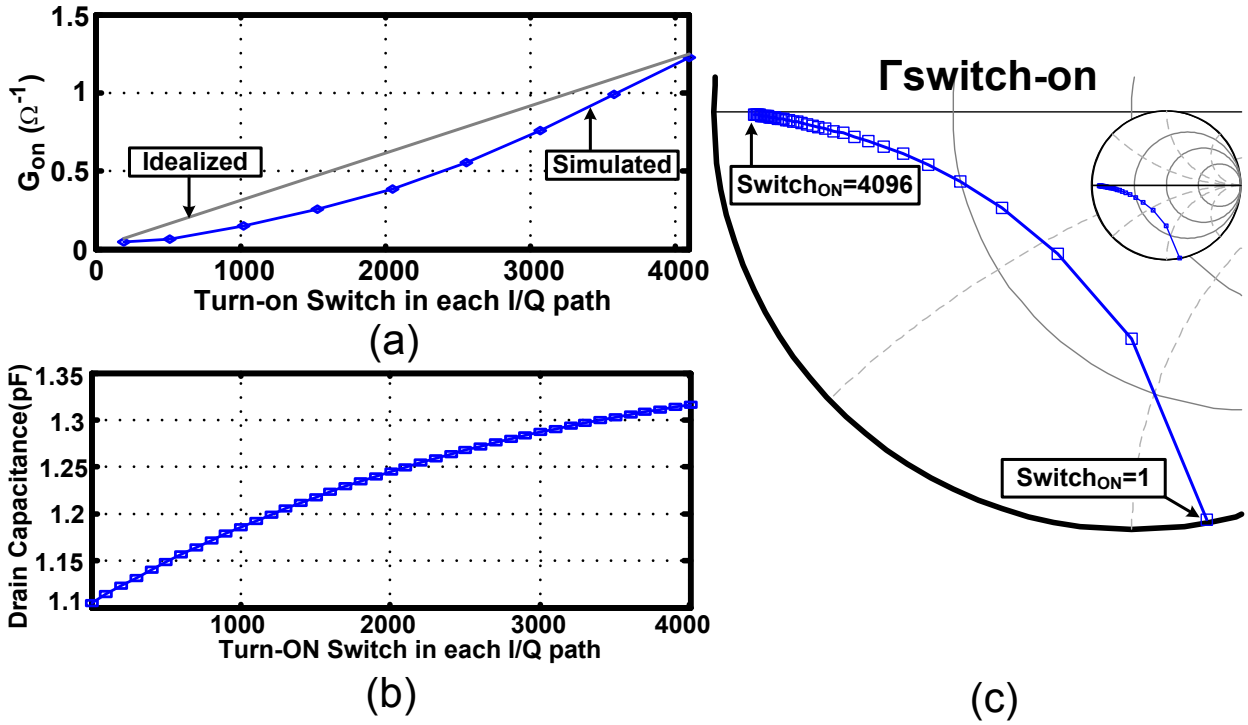

Figure 7.11: Sweeping the turn-on switches (a) G_{on}; (b) drain capacitance; (c) $\Gamma_{switch-on}$.

pendent. In other words, all reported calibration and DPD processes in this dissertation, are performed employing carrier clock at 2.4 GHz. Consequently, they should be updated for other carrier frequencies.

7.9.1 IQ Image and Leakage Suppression

To improve the LO leakage and IQ image suppression, the I/Q RF-DAC should be calibrated. First, (3.4) is rewritten according to clock pulses of I_P, Q_P, I_N, and Q_N.

$$\begin{aligned} IQ_{Ideal}(t) &= I_{path} + Q_{path} \\ &= \cos(2\pi f_{BB} t) \times \left\{ A_{ip}\Pi\left(\frac{t}{T_0/2}\right) - A_{in}\Pi\left(\frac{t}{T_0/2} - 2\right)\right\} \\ &\quad + \sin(2\pi f_{BB} t) \times \left\{ A_{qp}\Pi\left(\frac{t}{T_0/2} + 1\right) - A_{qn}\Pi\left(\frac{t}{T_0/2} - 1\right)\right\} \end{aligned} \tag{7.2}$$

where f_{BB} is the baseband frequency, T_0 is upconverting clock period, and $\Pi\left(\frac{t}{T_0/2}\right)$ represents a 25% duty cycle rectangular pulse clocked at f_0. In other words, the corresponding

Fourier series of Q_P, I_P, Q_N, and I_N can be expressed as follows:

$$Q_P = \Pi\left(\frac{2t}{T_0}+1\right) = \frac{1}{4} - \frac{\sqrt{2}}{\pi}\sin(\omega_0 t) - \frac{1}{\pi}\cos(2\omega_0 t) + \frac{\sqrt{2}}{3\pi}\sin(3\omega_0 t) + \ldots \tag{7.3}$$

$$I_P = \Pi\left(\frac{2t}{T_0}\right) = \frac{1}{4} + \frac{\sqrt{2}}{\pi}\cos(\omega_0 t) + \frac{1}{\pi}\cos(2\omega_0 t) + \frac{\sqrt{2}}{3\pi}\cos(3\omega_0 t) + \ldots \tag{7.4}$$

$$Q_N = \Pi\left(\frac{2t}{T_0}-1\right) = \frac{1}{4} + \frac{\sqrt{2}}{\pi}\sin(\omega_0 t) - \frac{1}{\pi}\cos(2\omega_0 t) - \frac{\sqrt{2}}{3\pi}\sin(3\omega_0 t) + \ldots \tag{7.5}$$

$$I_N = \Pi\left(\frac{2t}{T_0}-2\right) = \frac{1}{4} - \frac{\sqrt{2}}{\pi}\cos(\omega_0 t) + \frac{1}{\pi}\cos(2\omega_0 t) - \frac{\sqrt{2}}{3\pi}\cos(3\omega_0 t) + \ldots \tag{7.6}$$

Moreover, A_{ip}, A_{qp}, A_{in}, and A_{qn} are amplitudes of $I_{path,p}$, $Q_{path,p}$, $I_{path,n}$, and $Q_{path,n}$, respectively. In ideal conditions, their amplitudes are identical and equal to one. As a result, after some iterations, (7.2) is rewritten as

$$IQ_{Ideal} = \frac{2\sqrt{2}}{\pi}\cos(2\pi(f_0 + f_{BB})t) \tag{7.7}$$

Note that, as stated in Section 7.2, due to the phase synchronization between the RF and baseband paths as well as the precise quadrature clock generation utilizing divide-by-four circuitry, the phase imbalance between I_{path} and Q_{path} is zero. This is one of the significant advantages of the proposed I/Q RF-DAC. In reality, however, because of mismatches between A_{ip}, A_{qp}, A_{in}, and A_{qn}, after some iterations and simplifications, (7.7) changes to the following equation:

$$IQ_{non-ideal} = IQ_{Ideal} + C_{image}\cos(2\pi(f_0 - f_{BB})t) + C_{Leakage} \tag{7.8}$$

in which C_{image} and C_{Leakge} are the carrier image and leakage, respectively. To cancel $C_{Leakage}$, a proper DC value (i.e., -$C_{Leakage}$) is added to the original complex-valued baseband signal. Moreover, exploiting a very simple algorithm, the amplitudes of I_{path} and Q_{path} (A_{ip}, A_{qp}, A_{in}, and A_{qn}) change such that C_{image} decreases. As a result, the calibration algorithm should improve the LO leakage and I/Q image. It is worth mentioning again that A_{ip}, A_{qp}, A_{in}, and A_{qn} are the baseband amplitude codes and can easily be set to any value between (-4095...4095)/4096[3].

To prove effectiveness of a simple IQ calibration algorithm, a 2.234 MHz I/Q baseband signal is applied to the chip. Fig. 7.12 illustrates that the simple calibration algorithm can

[3]The I and Q DC codes, in LO leakage calibration, are selected between (-10...10)/4096 while their corresponding I and Q codes for IQ image calibration are selected between (-4095...-4000)/4096 and (+4000...+4095)/4096.

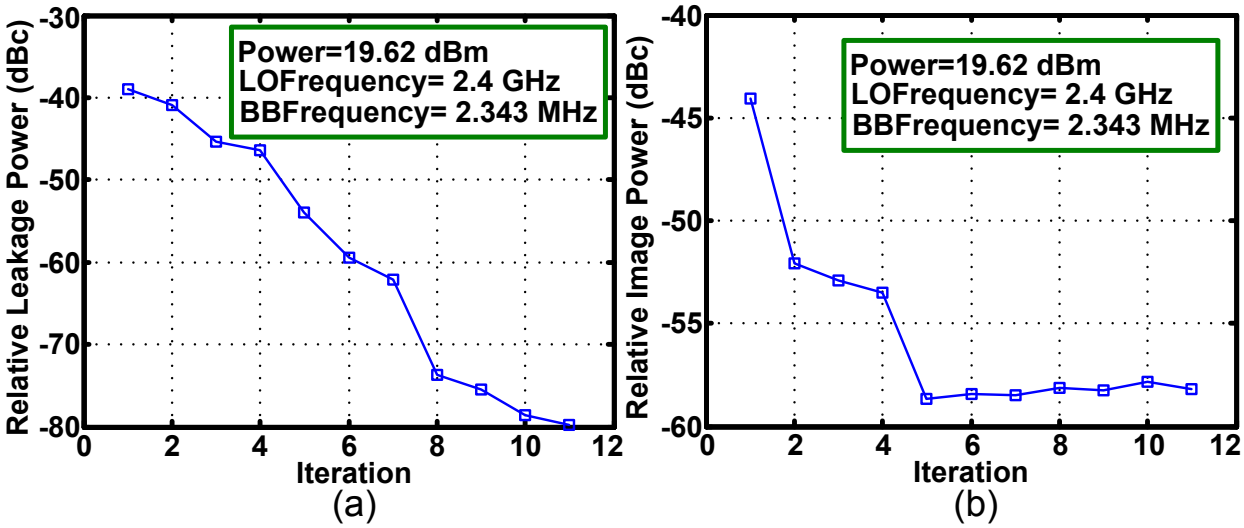

Figure 7.12: Measurements at 2.4 GHz of (a) carrier leakage; (b) image suppression.

significantly improve the LO leakage and IQ image suppression. In this scenario, f_0=2.4 GHz while the output power is 19.62 dBm. Based on this measurement, the I/Q image exceeds -58 dBc after 5 iterations while the LO leakage converges to more than -80 dBc.

Furthermore, to improve the transfer function linearity of the RF-DAC, eight IC chips have been measured and two well-known DPD algorithms have been employed.

7.9.2 DPD Based On AM-AM and AM-PM Profiles

In this approach, a two-tone sinusoidal signal with a frequency of f_m is applied at the baseband input. The AM-AM and AM-PM profiles of the I/Q RF-DAC are then evaluated [103]. First, the LO leakage and IQ image are calibrated (as discussed in Section 7.9.1) and the down-converted envelope and phase of the probed RF output are subsequently collected. After rearranging the measured envelope and phase signals based on the signed 12-bit baseband code range, i.e., -4095 to +4095, the AM-AM and AM-PM characteristics are obtained and are depicted in Fig. 7.13. Note that, even though the RF-DAC's input signals are digital codes, they could be normalized to 1 V and represented as a continuous voltage input. Assuming the RF-DAC is a memoryless nonlinear system, its input-output voltage relationship can be approximated as:

$$\begin{aligned} V_{out} &= f(V_{in}) \\ &= a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 + \ldots \\ &\cong 1.45 V_{in} - 0.0006 V_{in}^2 - 0.46 V_{in}^3 + 0.0005 V_{in}^4 \end{aligned} \tag{7.9}$$

using MATLAB's curve-fitting toolbox, the $V_{out} = f(V_{in})$ profile can be fitted and thus, the $a_1 \ldots a_4$ are evaluated. Moreover, the output-phase/input-voltage relationship (AM-PM

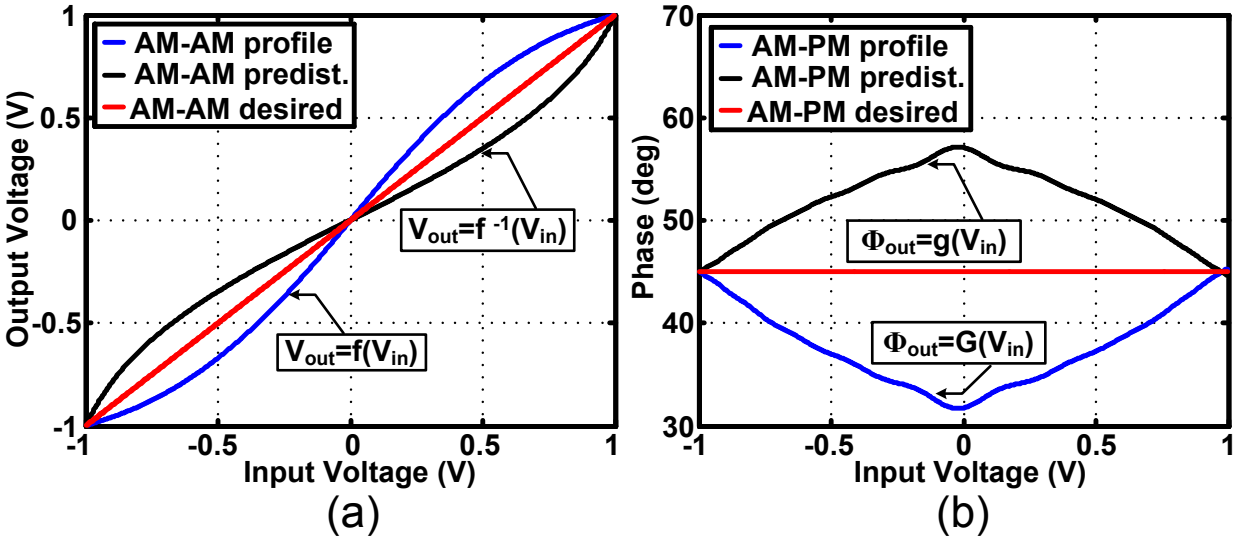

Figure 7.13: Two-tone test envelope and phase profiles: (a) AM-AM (b) AM-PM.

profile) can also be modeled by a polynomial representation as:

$$\begin{aligned} \Phi_{out}|_{deg} &= G(V_{in}) \\ &= \phi_0 + \phi_1 V_{in} + \phi_2 V_{in}^2 + \phi_3 V_{in}^3 + \phi_4 V_{in}^4 + \dots \\ &\cong 34 + 0.34 V_{in} + 16.86 V_{in}^2 - 0.21 V_{in}^3 - 4.7 V_{in}^4 \end{aligned} \tag{7.10}$$

According to Fig. 7.13 and (7.9)-(7.9), the inverse functions of the envelope is as follows:

$$\begin{aligned} V_{out} &= f^{-1}(V_{in}) = f^{-1}(a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 + \dots) \\ &= \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3 + \alpha_4 V_{in}^4 + \dots \\ &\cong 0.572 V_{in} + 0.0002 V_{in}^2 + 0.403 V_{in}^3 + 0.001 V_{in}^4 \end{aligned} \tag{7.11}$$

Moreover, the required predistorted phase profile of Fig. 7.13(b) could be expressed as:

$$\begin{aligned} \Phi_{out}|_{deg} &= g(V_{in}) \\ &= -G(V_{in}) + 90 \\ &= \psi_0 + \psi_1 V_{in} + \psi_2 V_{in}^2 + \psi_3 V_{in}^3 + \psi_4 V_{in}^4 + \dots \\ &\cong 56 - 0.34 V_{in} - 16.86 V_{in}^2 + 0.21 V_{in}^3 + 4.7 V_{in}^4 \end{aligned} \tag{7.12}$$

in which (7.11) and (7.12) are applied to the baseband code. Based on Fig. 7.13, applying the AM-AM predistorted profile makes the desired AM-AM transfer function as a straight line, i.e., $V_{out} = V_{in}$. Moreover, the desired AM-PM characteristic is a constant line, i.e., $\phi_{out} = cte = 45$. It should be mentioned that the AM-AM and AM-PM nonlinearities are added vectorially and, therefore, they cannot cancel each other (see Appendix A.3). Thus, each profile should be corrected accordingly. The measurement results based on these profiles

will be presented in Chapter 8, Subsection 8.3.1. It should be reiterated that the AM-AM and AM-PM profiles are carrier frequency dependent due to the fact that the power combiner circuit elements change their impedance at other frequencies.

7.9.3 DPD Based On I/Q Code Mapping

The second predistortion approach, which is utilized in this dissertation, is performed using a constellation-mapping based DPD algorithm [104–106]. This work, however, proposes a very simple, modified constellation-mapping DPD which is based on 1D mapping of I_{BB-up} and Q_{BB-up}, i.e., 2×1D. A complex modulated baseband data is defined as:

$$\begin{aligned} IQ_{BB}(I_{BB-up}, Q_{BB-up}) &= I_{BB-up} + \mathrm{j} \times \mathrm{Q_{BB-up}} \\ &= A_{IQ}(I_{BB-up}, Q_{BB-up}) \angle \phi_{IQ}(I_{BB-up}, Q_{BB-up}) \end{aligned} \tag{7.13}$$

I_{BB-up} and Q_{BB-up} are demonstrated in Fig. 7.14(a). Moreover, A_{IQ} and ϕ_{IQ} are envelope and phase information of the corresponding baseband data, respectively. Thus, ideally, the modulated RF output of the RF-DAC is expressed as:

$$\begin{aligned} V_{IQ}(I_{BB-up}, Q_{BB-up}) &= IQ_{BB}(I_{BB-up}, Q_{BB-up}) \times \exp(\mathrm{j}\omega_0 \mathrm{t}) \\ &= A_{IQ} \times \exp(\mathrm{j}(\omega_0 \mathrm{t} + \phi_{\mathrm{IQ}})) \end{aligned} \tag{7.14}$$

Nonetheless, due to the fact that RF-DAC is a nonlinear transmitter, as a result, the RF output of the RF-DAC becomes:

$$V_{IQ}(I_{BB-up}, Q_{BB-up}) = (V_I(I_{BB-up}, 0) + \mathrm{j} \times \mathrm{V_Q}(0, \mathrm{Q_{BB-up}})) \times \exp(\mathrm{j}\omega_0 \mathrm{t}) \tag{7.15}$$

where $V_I(I_{BB-up}, 0)$ and $V_Q(0, Q_{BB-up})$ are the corresponding nonlinear complex profiles of I_{BB-up} and Q_{BB-up} in which they are normalized to their related input codes. These profiles are indicated in Fig. 7.14(a). In practice, $V_I(I_{BB-up}, 0)$ and $V_Q(0, Q_{BB-up})$ are acquired as follows: First, due to orthogonal operation of RF-DAC, I_{BB} and Q_{BB} are individually swept from -4095 to +4095. The subsequent RF output is down-converted, and the related baseband complex signals, i.e., $V_I(I_{BB-up}, 0)$ and $V_Q(0, Q_{BB-up})$, are obtained. Next, the inverse function of $V_I(I_{BB-up}, 0)$ and $V_Q(0, Q_{BB-up})$ are evaluated and depicted in Fig. 7.14(b). The in-phase and quadrature-phase DPD profiles are as follows:

$$\begin{aligned} V_{IDPD}(I, Q) &= V_I^{-1}(I_{BB-up}, 0) \\ &= I_{DPD-I} + \mathrm{j} \times \mathrm{Q_{DPD-I}} \end{aligned} \tag{7.16}$$

$$\begin{aligned} V_{QDPD}(I, Q) &= V_Q^{-1}(0, Q_{BB-up}) \\ &= I_{DPD-Q} + \mathrm{j} \times \mathrm{Q_{DPD-Q}} \end{aligned} \tag{7.17}$$

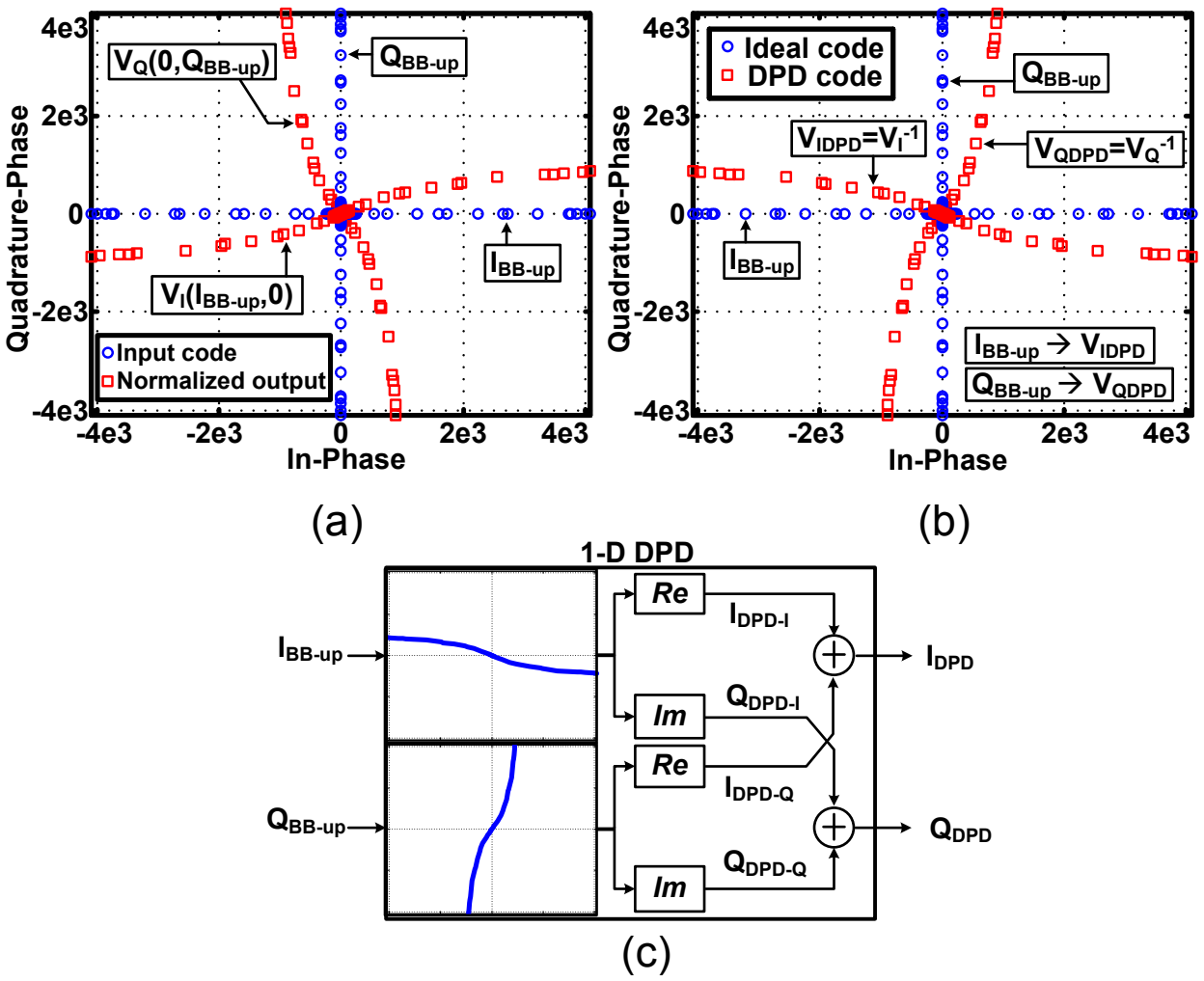

Figure 7.14: (a) Input codes along with their corresponding nonlinear output voltages; (b) DPD in-phase and quadrature-phase input code mapping diagram; (c) Illustration of the open-loop, 2×1D DPD.

Otherwise stated, the following relationships are established between I_{BB-up} and $V_{IDPD}(I,Q)$ as well as Q_{BB-up} and $V_{QDPD}(I,Q)$.

$$\begin{aligned} I_{BB-up} &= V_I\left(V_I^{-1}(I_{BB-up},0)\right) \\ &= V_I\left(V_{IDPD}(I,Q)\right) \\ &= V_I(I_{DPD-I},Q_{DPD-I}) \end{aligned} \tag{7.18}$$

$$\begin{aligned} Q_{BB-up} &= V_Q\left(V_Q^{-1}(0,Q_{BB-up})\right) \\ &= V_Q\left(V_{QDPD}(I,Q)\right) \\ &= V_Q(I_{DPD-Q},Q_{DPD-Q}) \end{aligned} \tag{7.19}$$

Therefore, in this DPD process, I_{BB-up} and Q_{BB-up} are individually mapped to $V_{IDPD}(I,Q)$ and $V_{QDPD}(I,Q)$), respectively.

$$I_{BB-up} \rightarrow V_{IDPD}(I,Q) \tag{7.20}$$

$$Q_{BB-up} \rightarrow V_{QDPD}(I,Q) \tag{7.21}$$

Specifically, this DPD process can be inferred as 1D mapping of two individual signals of I_{BB-up} and Q_{BB-up}, i.e., 2×1D. In particular, since I_{path} and Q_{path} are orthogonal, the DPD does not require a 2D exhaustive search of the entire constellation diagram which is utilized in [66]. Consequently, due to orthogonality, the subsequent I_{DPD} and Q_{DPD} are obtained as follows

$$I_{DPD}(I_{BB-up}, Q_{BB-up}) = I_{DPD-I} + I_{DPD-Q} \tag{7.22}$$

$$Q_{DPD}(I_{BB-up}, Q_{BB-up}) = Q_{DPD-I} + Q_{DPD-Q} \tag{7.23}$$

Fig. 7.14(c) illustrates the open loop, 2×1D DPD. Note that the DPD profiles of V_{IDPD} and V_{QDPD} are obtained only at the beginning of the measurement operation, and they will remain unchanged afterwards[4]. It should be again pointed out that DPD profiles in Fig. 7.14 are carrier frequency dependent due to the power combining network.

Fig. 7.15 depicts the constellation mapping measurement setup structure. Using MATLAB, in-phase and quadrature-phase randomized symbols (I_{symb} and Q_{symb}) are generated and supplied to the I/Q baseband modulator. This block creates QAM signals of I_{BB} and Q_{BB}. Then, to confine the modulation bandwidth, I_{BB} and Q_{BB} get pulsed-shaped using a root raised cosine (RRC) interpolation filter and upsampled to as high as the CK_R rate, which is $f_0/8$ (see also Fig. 7.1). Afterwards, I_{BB-up} and Q_{BB-up} are mapped utilizing (7.20)-(7.23) and Fig. 7.14(b). Next, the predistorted signals (I_{DPD} and Q_{DPD}) are uploaded into two designated on-chip SRAMs. Thereafter, the upconverted RF signal is down-converted using a vector signal analyzer (VSA), and the subsequent down-converted digital in-phase (I_{dw}) and quadrature-phase (Q_{dw}) signals are fed back to MATLAB. Three important steps should be followed. First, the measurement time-delay should be calibrated. Then, the subsequent complex signal phase, i.e., $\phi_d = \angle(I_d + jQ_d)$, should be rotated such that the eventual phase, i.e., $\phi_{syn} = \angle(I_{syn} + jQ_{syn})$, is the same as the original complex phase, i.e., $\phi_{BB-up} = \angle(I_{BB-up} + jQ_{BB-up})$. Finally, I_{syn} and Q_{syn} are down-sampled utilizing a RRC decimation filter to recover the original I/Q baseband modulated signals, i.e., I_{syn-BB} and

[4]As stated previously, due to inaccurate components of the passive power combiner, the RF-DAC test-chip exhibits imperfect orthogonal summation. As a result, it requires only simple 2×1D DPD. Although employing 2D instead of 1D results in a better linearity performance, it is extremely difficult (and very expensive in practice) to obtain 2D DPD profiles.

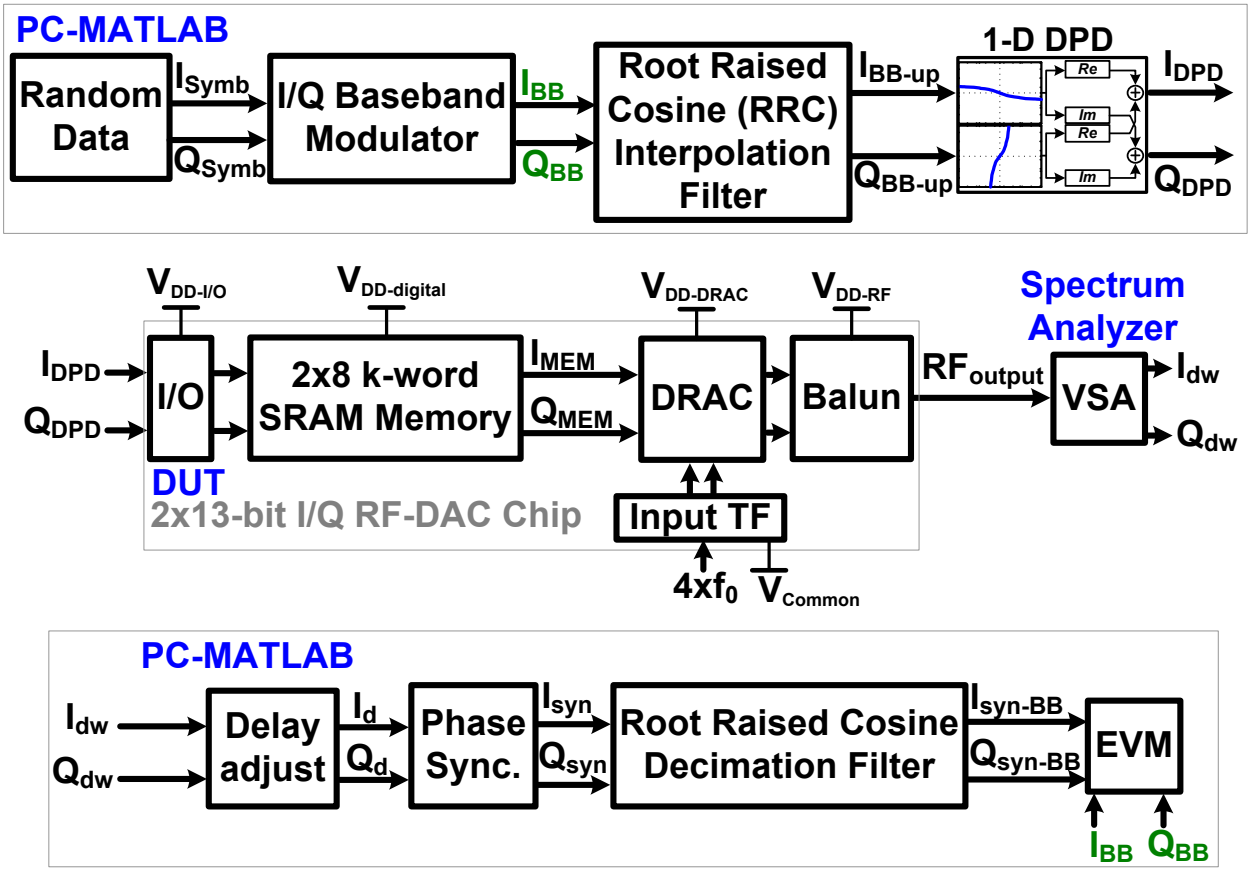

Figure 7.15: DPD measurements constellation mapping flow.

Q_{syn-BB}. Comparing the measured I_{syn-BB}/Q_{syn-BB} with the original I_{BB}/Q_{BB}, the EVM based on (1.3) or [69, eqs. 24] is calculated.

7.9.4 DPD Required Memory and Time

As stated, the DPD is performed at the initiation of the measurement process and is not a background operation. Namely, the DPD profiles, V_{IDPD} and V_{QDPD}, are generated at the initiation and they will subsequently be frozen for the remainder of the measurement process. It is an open loop procedure and, in this work, it is not automated. It is worth mentioning that the two designated on-chip SRAMs are employed in order to upload the upsampled complex baseband signals, i.e., I_{BB-up} and Q_{BB-up}, into them. Nonetheless, due to utilizing the DPD, the predistorted baseband signals, i.e., I_{DPD} and Q_{DPD} are eventually uploaded into them. As stated previously, the memory length is fixed, i.e., l_{mem}=8 k-word. Thus, this work is severely hindered by this limitation. As explained earlier, I_{BB-up} and Q_{BB-up} should be individually swept from -4095 to +4095 in order to obtain the V_{IDPD} and V_{QDPD} DPD profiles, respectively. These two individual processes are illustrated in Fig. 7.16. Note that, as explained later in this chapter, to preserve the continuity in order to alleviate

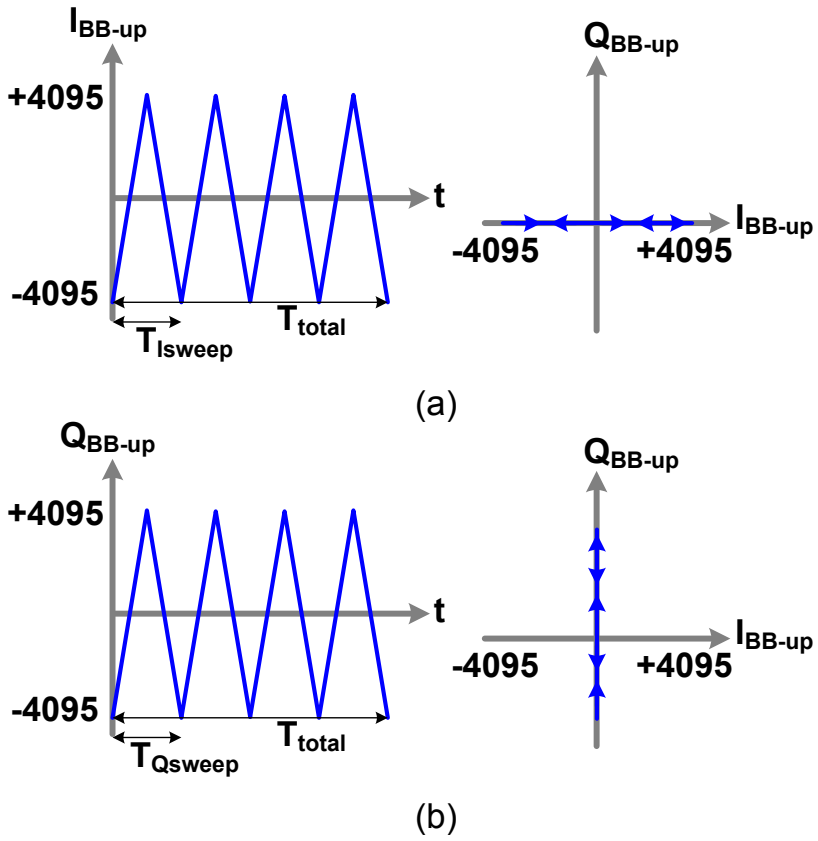

Figure 7.16: DPD sweeping time of (a) I_{path}; (b) Q_{path}.

the unwanted spectral jump, the first data point and the last one should be identical. Thus, the total number of sweeping points should be doubled. In other words, as depicted in Fig. 7.16, this operation comprises two specific paths, from -4095 to +4095 and vice versa which requires 2×8 k=16 k points. Consequently, due to the fact that l_{mem}=8 k-word, every other baseband code value from -4095 to +4095 can only be swept. Hence, the in-phase sweeping time is

$$\begin{aligned} T_{I-sweep} &= 8192 \times \frac{1}{f_{CKR}} \\ &= \frac{8192}{300e6} \\ &\cong 27.31\mu s \end{aligned} \tag{7.24}$$

Also considering the quadrature-phase sweeping time (see Fig. 7.16(b)), the total sweeping time is doubled, i.e., 54.62 μs. Nonetheless, to improve the accuracy of the DPD profiles, as depicted in Fig. 7.16, the sweeping time can be increased to 4 cycles whereby DPD profiles can be extracted while averaging these four cycles. Thus, the total sweeping time is increased to 218.48 μs. Note that, since this time is inversely proportional to f_{CKR}, increasing the upsampling rate not only improves the out-of-band spectral performance but also decreases the DPD calibration time.

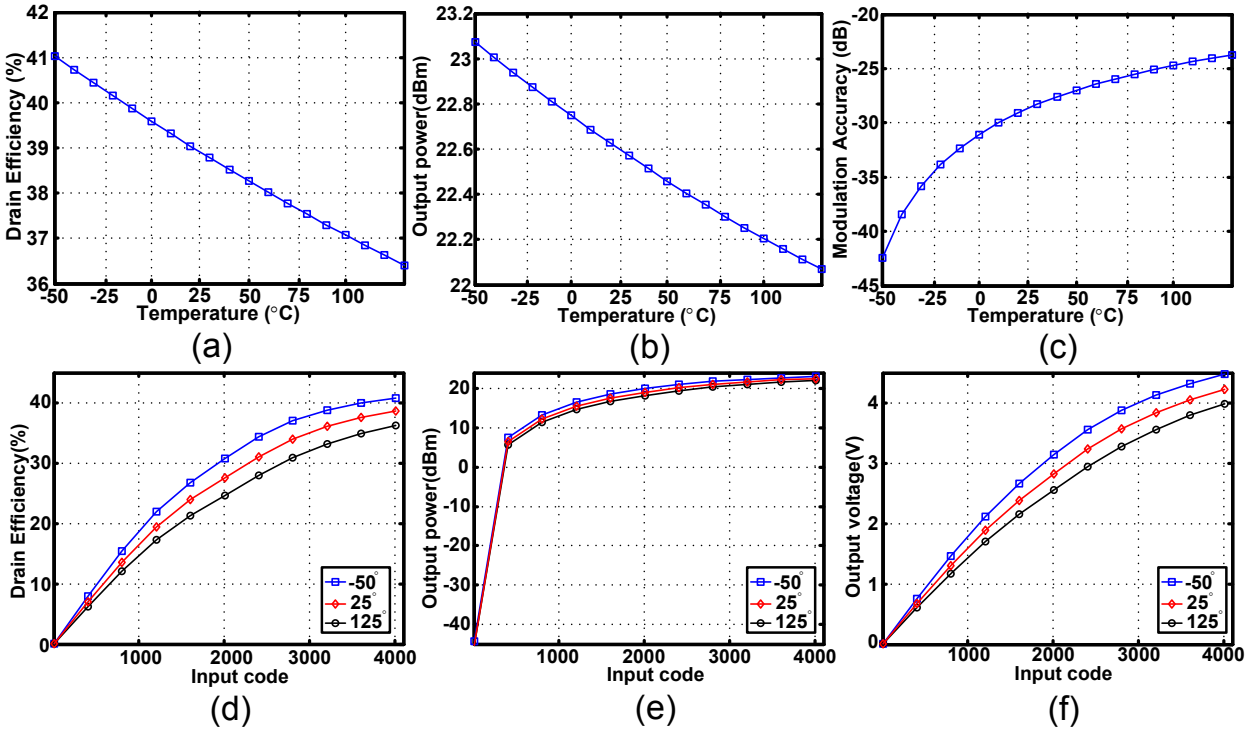

Figure 7.17: Effect of temperature Sweeping on (a) drain efficiency; (b) output power; (c) modulation accuracy. Effect of baseband code sweeping on (d) drain efficiency; (e) output power; (f) output voltage for -50, 25, and 125°C.

7.9.5 DPD Effectiveness Against the Temperature and Aging

DPD depends on the temperature. In order to validate that, a simple simulation is performed in which the corresponding circuit temperature is swept between -50 to 130°C. The simulation results are demonstrated in Fig. 7.17(a)-(c). Moreover, the I/Q baseband input codes of the RF-DAC are swept, and its corresponding drain efficiency, output power, and output voltage are simulated for the temperature of -50, 25, and 50°C which are depicted in Fig. 7.17(d)-(f). According to the simulation results in Fig. 7.17, the I/Q RF-DAC performance depends on the temperature and, thus, its related DPD profiles must be updated for various temperature conditions. Moreover, the aging would not affect the DPD profiles. This argument is confirmed during the measurement process. A number of chips in the period of three to four months are measured, and their corresponding DPD performances were always within 1 or 2 dB of each other which can be tolerated. Therefore, at least, it could be expressed that, for brief periods of time, the effectiveness of the DPD will not be degraded. Checking with the TSMC manual confirms that a significant effect due to aging would not be expected.

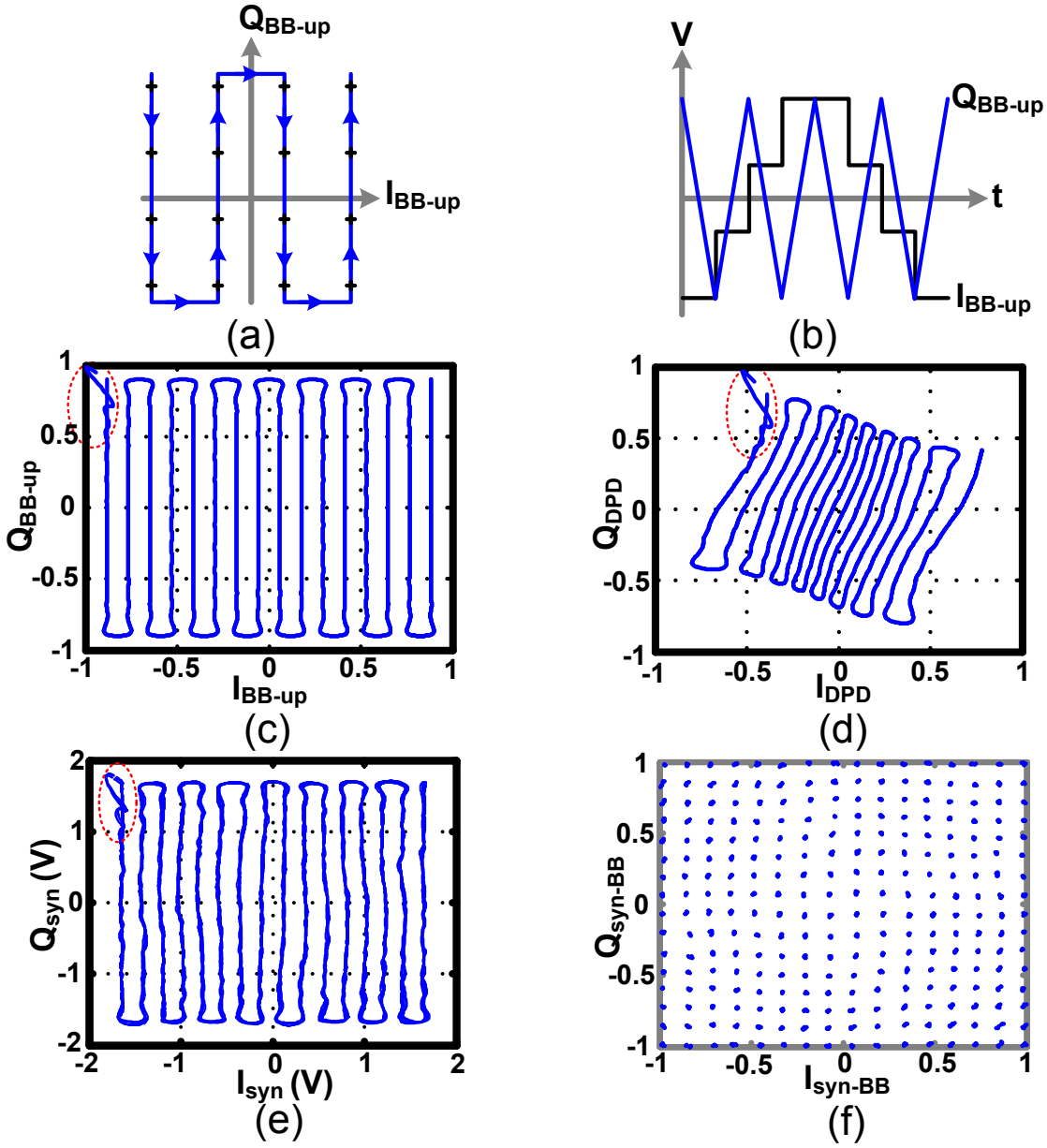

Figure 7.18: DPD measurements: (a) Simplified diagram of 16-symbol I_{BB-up}/Q_{BB-up}; (b) Trajectories of their related time domain waveforms. DPD 256-symbol constellation mapping plots: (c) I_{BB-up}/Q_{BB-up} trajectories; (d) predistorted I_{DPD}/Q_{DPD} trajectories; (e) measured I_{syn}/Q_{syn} trajectories; (f) measured 256-point constellation.

7.9.6 Verification of DPD I/Q Code Mapping

Examining this approach, a 256-symbol modulation is created. Based on a Fig. 7.18(a) concept, the constellation diagram is continuously swept from the top-left to top-right in a "snake"-like manner and traversed back again to its original point in order to preserve continuity. Note that, for simplicity, Fig 7.18(a) only illustrates a 16-symbol constellation

diagram as well as their time domain representations, which is exhibited in Fig 7.18(b). These signals are then upsampled and interpolated using an RRC interpolation filter to produce I_{BB-up} and Q_{BB-up} (see their I/Q trajectories in Fig. 7.18(c)). Next, the resultant signals are predistorted (I_{DPD} and Q_{DPD}) using the lookup table of Fig. 7.18(b) and loaded into two on-chip SRAMs. Fig. 7.18(d) shows the effect of the I/Q DPD mapping on the I/Q trajectories of the original modulated signals. The RF output signal is down-converted, and its corresponding I/Q trajectories are exhibited in Fig. 7.18(e), which demonstrates a good agreement with the original I/Q trajectories of Fig. 7.15(c). I_{syn} and Q_{syn} are then down-sampled and decimated to create the measured constellation diagram (Fig. 7.18(f)). Note that its related EVM, RF power, and drain efficiency are -32 dB, 16.1 dBm, and 19%, respectively. It should be mentioned that, due to the limited data length of I_{DPD}/Q_{DPD} (i.e., 8192), which are repeatedly fed to the DRAC circuit from the first data point to the last, any discontinuity between the first data point and the last one creates an undesirable spectral jump. To alleviate this issue and to preserve the continuity, the data length of I_{BB} and Q_{BB} are doubled and applied to the RRC interpolation filter and then only the half of the data length of the subsequent I_{BB-up} and Q_{BB-up} are exploited and applied to the DPD lookup table. This technique is referred to as wrap-around process. As a result, the beginning points of the I/Q trajectories of Fig. 7.18(c)-(e), indicated with circles, have been shaped in such a way as to insure the continuity of the I/Q signals.

7.10 Conclusion

In this chapter, the implemented wideband, 2×13-bit I/Q RF-DAC-based all-digital transmitter realized in 65-nm CMOS is presented. Employing the orthogonal I/Q combining approach which is proposed in Chapter 3 guarantees the isolation between I_{path} and Q_{path}. Nonetheless, due to inaccurate components of the passive power combiner, the I_{path} and Q_{path} interact with one another. The $4\times f_0$ off-chip single-ended clock is converted to a differential version employing an on-chip transformer. The wide swing, low phase noise, high-speed dividers are incorporated to translate the $4\times f_0$ differential clock to the fundamental frequency of f_0. In the meantime, the complementary quadrature sign bit is used to address four quadrants of the related constellation diagram. The 25% differential quadrature clocks are generated using logic-AND operation between $2\times f_0$ differential clock and f_0 differential quadrature clocks. The 12-bit DRAC is implemented employing a segmentation approach, which consists of 256 MSB and 16 LSB thermometer unit cells. The layout arrangement of the DRAC unit cell proves to be very crucial. It was concluded that the vertical layout would be the most appropriate selection. The LO leakage and I/Q image rejection technique as well as two DPD memoryless techniques of AM-AM/AM-PM and constellation mapping are introduced, which will be extensively utilized in the measurement segment. The DPD techniques are utilized to alleviate the imperfect orthogonal summing of the I_{path} and Q_{path}.

Chapter 8

Measurement Results of the 2×13-bit I/Q RF-DAC

This chapter addresses the related measurement results of the proposed 2×13-bit chip presented in Chapter 7. Section 8.1 thoroughly explains the measurement setup structure. Section 8.2 demonstrates the performance of the chip under continuous-wave conditions. Section 8.3 exhibits its behavior when applying the complex-modulated baseband signal. Finally, Section 8.4 concludes the chapter. The proposed 2×13-bit all-digital I/Q RF-DAC is implemented in a TSMC 65 nm LP CMOS process. Fig. 8.1(a) exhibits the chip micrograph. The chip occupies $1.27\times2\,\mathrm{mm}^2$ with an active area of $0.58\times1.03\,\mathrm{mm}^2$. Moreover, the designated SRAMs occupy an area of $1.27\times1\,\mathrm{mm}^2$ while the remainder is occupied by decoupling capacitors and I/O pads. Note that the DRAC in combination with its corresponding binary-to-thermometer encoders as well as decoupling capacitors occupies only $0.41\times0.41\,\mathrm{mm}^2$. The RF-DAC employs only standard "Vt" transistors. All pads, including the single-ended RF input clock and RF output, are wire-bonded directly to the FR4 board. The RF-DAC ground plane is improved utilizing the following approach. First, all ground pads are wire-bonded using flat bond wire which decreases the equivalent inductance of the bond wire by approximately four times. Second, the chip is situated in a 300 μm deep hole. This makes the bond wires shorter and, thus, the interconnecting inductance is smaller.

8.1 Measurement Setup

For measurements, as depicted in Fig. 8.1(b), the chip requires five different supply voltages namely, $V_{\mathrm{DD-RF}} = 1.2\ldots1.3\,\mathrm{V}$ for the balun center-tap node, $V_{\mathrm{DD-DRAC}} = 1.2\,\mathrm{V}$ for the RF-DAC core, $V_{\mathrm{Common}} = 0.6\,\mathrm{V}$ for the input transformer center-tap node, $V_{\mathrm{DD-digital}} = 1.2\,\mathrm{V}$ for the SRAMs and UART interface[1], and finally $V_{\mathrm{DD-I/O}} = 3.3\,\mathrm{V}$ for I/O supply voltages.

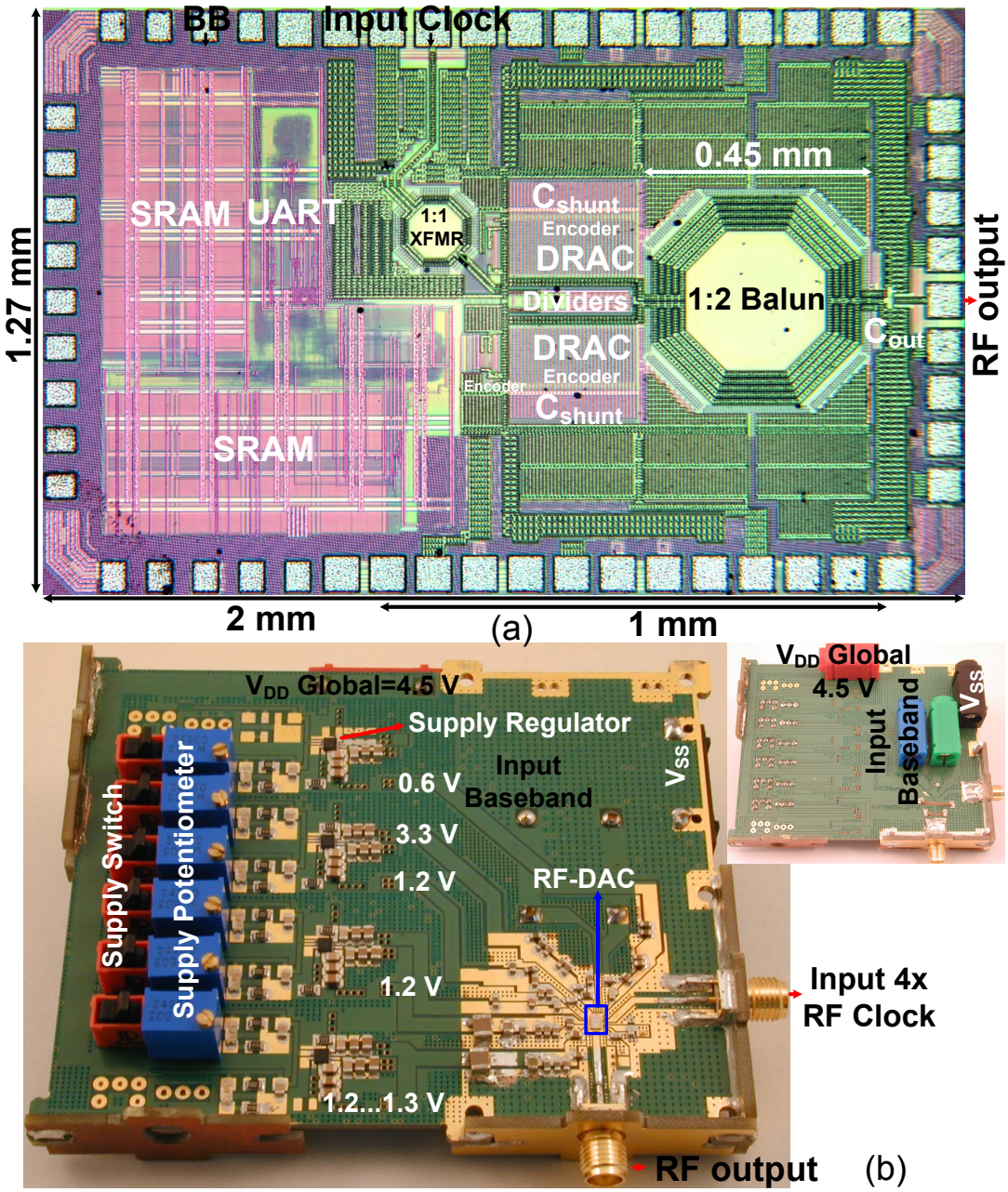

Figure 8.1: (a) Micrograph of the 2×13-bit all-digital I/Q RF-DAC transmitter, (b) front and back view of its related PCB.

They are generated employing on-board regulators, ADP225ACPZ-R7 from Analog Devices, which use a common input supply voltage of 4.5 V. Note that on-board potentiometers are employed to set the required voltages of the on-board regulators in order to adjust the supply voltages. In addition, in order to turn on and off the supply voltages, on-board switches are employed[2]. This configuration allows the entire I/Q RF-DAC chip to be tested using only one battery or supply voltage. Moreover, due to employing the on-chip input transformer,

the input 4× RF clock is a single-ended signal. In addition, as described in Chapter 7, Section 7.2, all required clock signals, including the baseband upsampling clock and the upconverting RF carriers, are generated via the on-chip frequency dividers. Thus, the I/Q RF-DAC only requires one external clock generator which results in a very straightforward board design and the test setup.

To verify the design through measurements, as it was fully explained in Chapter 5 (Fig. 5.1) and also Chapter 7 (Fig. 7.15), first, the I_{BB} and Q_{BB} baseband signals are upsampled and interpolated in software (PC-MATLAB). These upsampled signals, I_{BB-up} and Q_{BB-up}, are subsequently loaded via UART (see Appendix A, Section A.1) into two on-chip SRAMs that are clocked with CK_R of Fig. 7.1. Note that, as stated previously, the clock frequency is f_{CKR}=(1/8) × f_0.

8.2 Static Measurement Results

Earlier simulations demonstrate that the achievable maximum drain efficiency of the I/Q RF-DAC output stage should be well above 44%. Due to the low power arrangement of the forgoing clocking and pre-driver circuitry, the overall system efficiency of the realized monolithic transmitter, based on equations (1.2) and (5.1), should be able to reach 37% at 2.4 GHz for a peak output power level of 22.6 dBm at 1.2 V. Experimental verification shows that, without using any correction for the PCB and SMA connector losses, the peak overall system efficiency occurs at 2.1 GHz and reaches 31.5% with a related peak output power of 22.3 dBm at 1.2 V.

Although the transmitter was verified to work properly from 60 MHz to 3.5 GHz, the most superior performance is achieved in the range of 1.36 to 2.51 GHz where measurements illustrate an output power and overall system efficiency of more than 21 dBm and 21%, respectively (see Fig. 8.2). For this measurement, the carrier frequency is swept from 1.35 to 2.63 GHz in steps of 2 MHz. The supply voltage is also swept from 0.6 to 1.3 V. Fig. 8.2(a)–(b) only indicate the measurement results for 1.2–1.3 V. Based on these results, the peak output power is 22.8 dBm while its related drain efficiency and system efficiency are 42% and 34%, respectively. These results emphasize the wide-band operation of the realized on-chip output balun. Since the resolution of RF-DAC is 2×12 bits, the input baseband codes are swept from -4095 to +4095, and the output power with its related voltage and phase are measured. The measurement results are depicted in Figs. 8.2(c)–(d). Based on Fig. 8.2(c), the static carrier leakage level is more than 70 dB lower than the achievable maximum power.

[1]Courtesy of George Voicu from Professor Cotofana's group in TU-Delft, who designed and synthesized the UART interface.

[2]Courtesy of my group colleagues Amir Ahmadi Mehr, Massoud Tohidian, and Masoud Babaie, who have designed the on-board regulator circuits.

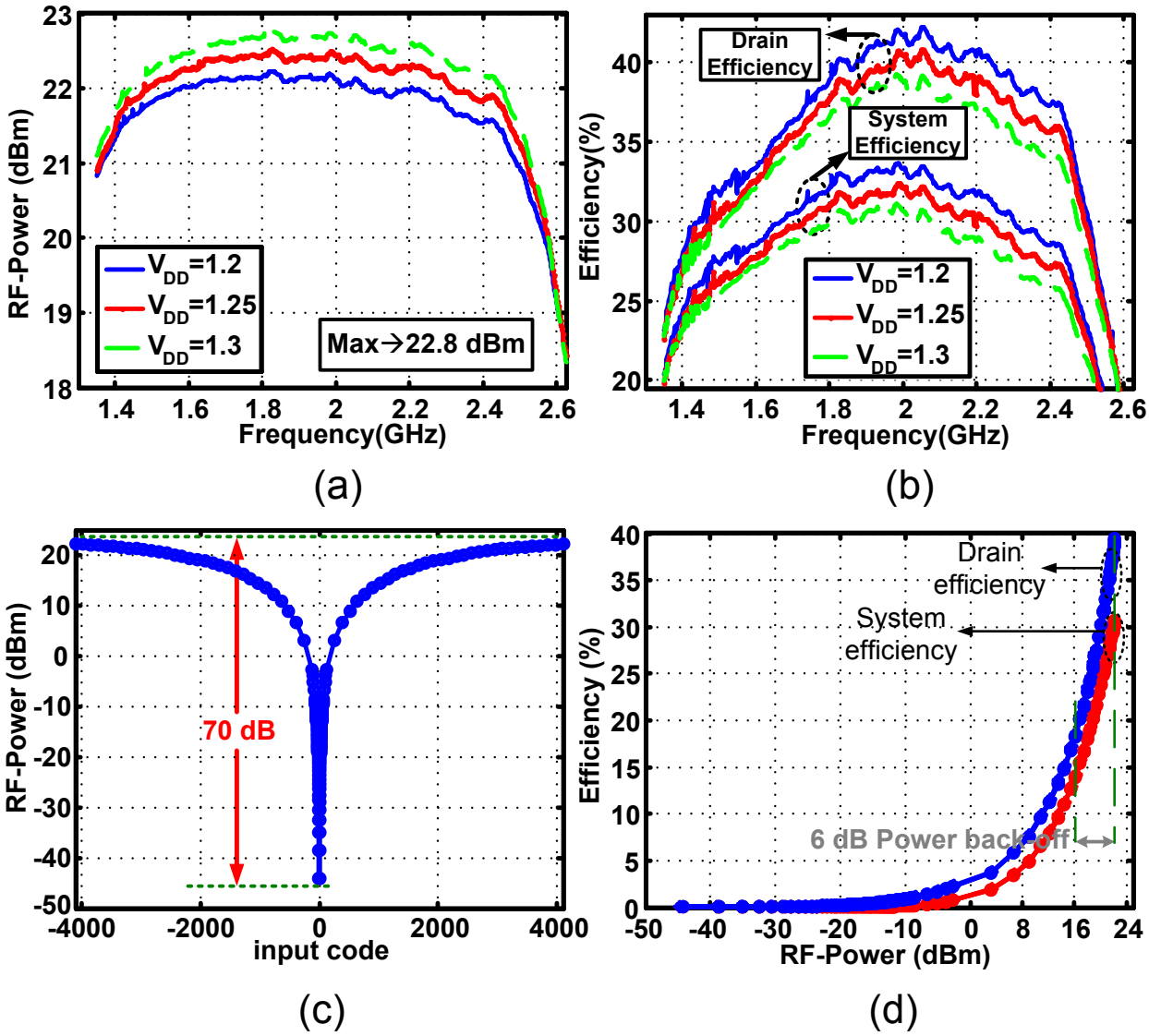

Figure 8.2: RF measurements: (a) RF output power; (b) efficiency of modulator versus frequency; (c) RF output power versus input code; (d) efficiency versus RF output power.

Fig. 8.2(d) exhibits the RF-DAC efficiency versus RF output power. According to Fig. 8.2(d), the drain and system efficiencies at the 6 dB back-off are 19% and 14%, respectively.

The static AM-AM nonlinearity of the digital I/Q transmitter is illustrated in Fig. 8.3(a). As expected, at lower absolute codes (center of the curve), the output voltage changes linearly with respect to the input code. In contrast, at higher codes, the curve begins to saturate. Moreover, Fig. 8.3(b)-(c) indicates the static AM-PM nonlinearity profiles. Based on the measurement results of Fig. 8.3(b), the maximum phase deviation of individual I and Q codes from lower to higher codes is less than 10°. Fig. 8.3(c) indicates that, by changing only the I_{BB-up} or Q_{BB-up} not only changes the amplitude but also changes the output phase that reveals the AM-PM distortion of the RF-DAC. By applying the lookup table of Fig. 7.14(b),

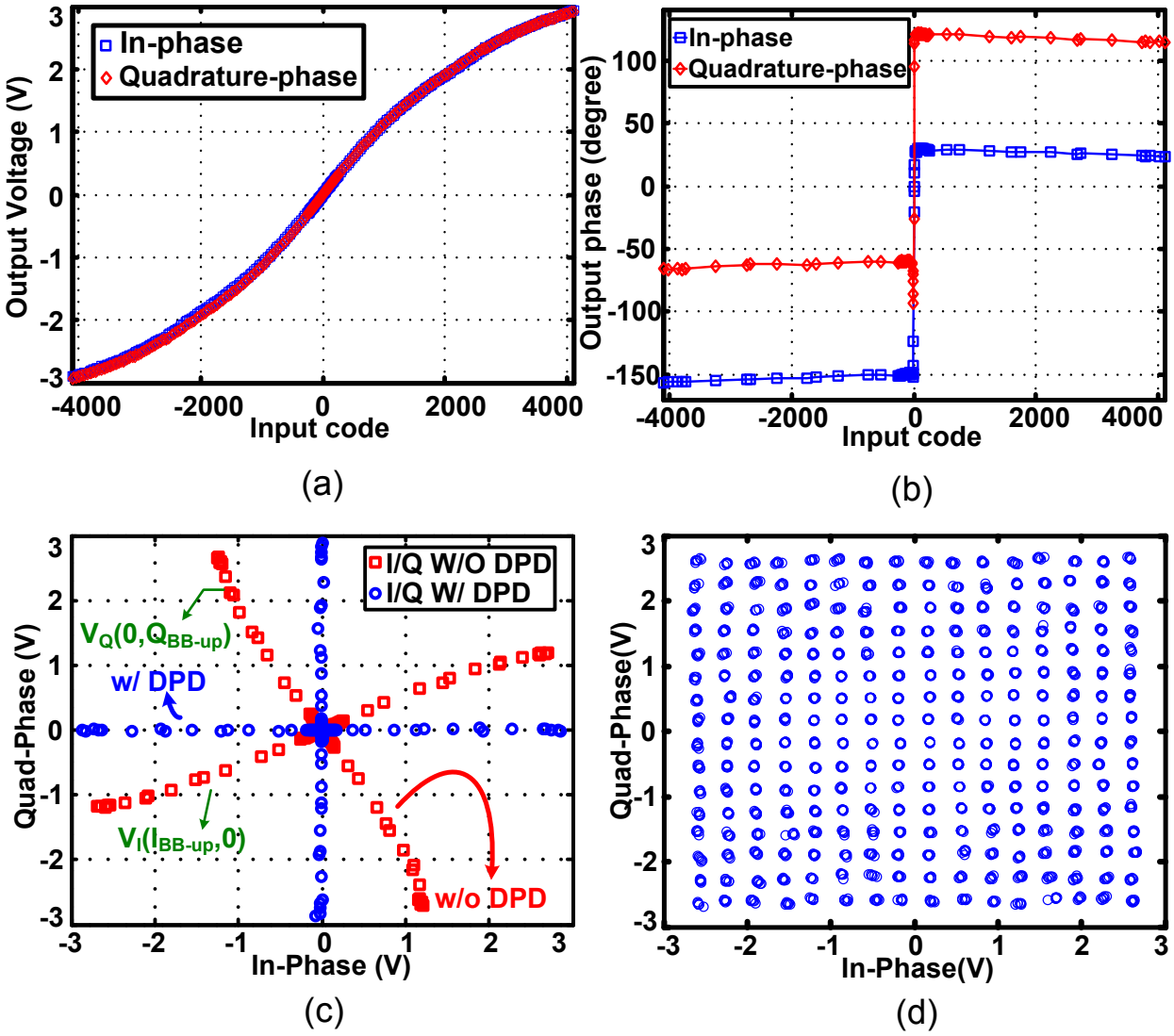

Figure 8.3: Static measurement results: (a) output voltage versus input code; (b) output phase versus input code; (c) simple I/Q constellation diagram with and without DPD; (d) 256-point constellation diagram with DPD.

the static I/Q constellation for a 256-symbol case are measured and depicted in Fig. 8.3(d). Its related EVM is better than -30 dB while the maximum RF power is more than 22 dBm. It should be pointed out that, as seen in Fig. 8.3(d), the RF-DAC exhibits memory effects which might be related to heating up the test-chip. Note that, as stated in Chapter 4, Section 4.2, the measurement results of Fig. 8.3(b)-(d) are obtained as follows: Time domain RF output signals are captured and saved. The FFT of these signals is subsequently calculated, and the amplitudes and phases are plotted to obtain the static constellation diagram of Fig. 8.3(d).

The static phase noise of RF-DAC is measured for various carrier frequencies between 1.5 to 2.5 GHz, and the noise floor is ascertained to be better than -160 dBc/Hz. Fig. 8.4(a)

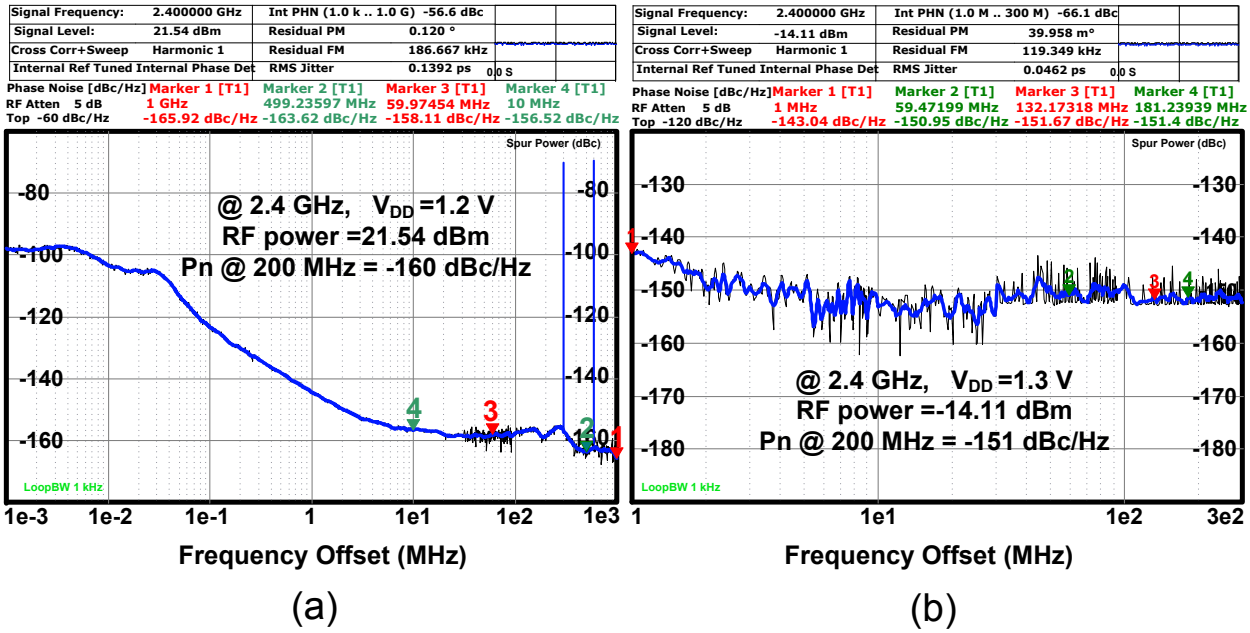

Figure 8.4: Phase noise at 2.4 GHz: (a) full power (b) low power.

shows the RF-DAC phase noise at 2.4 GHz. The maximum baseband code for I_{BB} and Q_{BB} is 4095, which produces 21.54 dBm of RF power. It should be noted that, at 200 MHz frequency offset, the phase noise is -160 dBc/Hz. The figure also indicates two "spurs" at 300 and 600 MHz, which are actually the spectral replicas discussed previously. In this aspect, the ZOH filter operation ensures that these replica levels are below -70 dBc/Hz[3]. Moreover, the RF-DAC phase noise performance is reexamined for lower codes (e.g., 32). Based on Fig. 8.4(b), its related RF power and noise floor reduces to -14 dBm and -165 dBm/Hz, respectively. Note that the shape of the noise floor is primarily related to the external 4× clock generator source. Thus, the limiting factor in the noise floor is related to the noise of the input clock source as well as the corresponding noise of the divider circuitry.

8.3 Dynamic Measurement Results

Dynamic measurements based on employing a modulated baseband signal have also been extensively performed. As stated in Chapter 7, the LO leakage and IQ image suppression performance of I/Q RF-DAC ought to be examined. Moreover, the transmitter's linearity will be explored.

[3]The RF-DAC works in the static mode of operation, hence the ZOH does not create any spectral replicas at multiples of the sampling frequency f_{CKR} away from the f_0 carrier. What is seen is 300/600 MHz clock leakage.

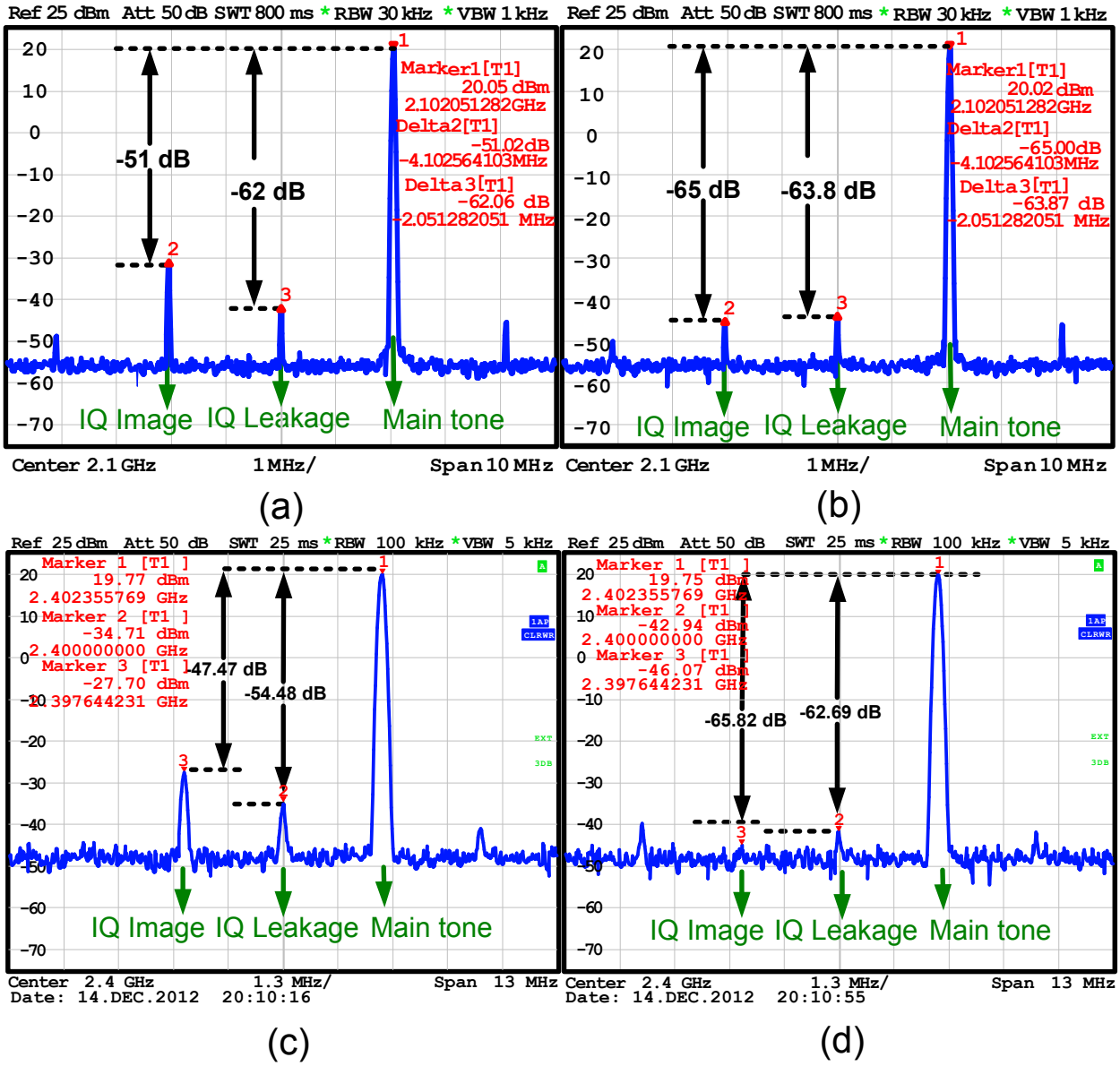

Figure 8.5: Leakage and image suppression: at 2.1 GHz (a) without calibration; (b) with calibration; at 2.4 GHz (c) without calibration; (d) with calibration.

8.3.1 LO Leakage and IQ Image Suppression of I/Q RF-DAC

First, LO leakage and IQ image suppression are examined. For this experiment, the LO frequency is set to 2.1 GHz, and the baseband frequency of I_{BB-up} and Q_{BB-up} signals are approximately 2.05 MHz. Fig. 8.5(a) demonstrates that, even without applying any I/Q calibration, the LO leakage and image levels are -62 dBc and -51 dBc, respectively, at an output power of 20.03 dBm. As such, these numbers are sufficient to meet the specifications of most communication standards. The low image level indicates the superior matching of I and Q paths. Moreover, the use of a divide-by-4 circuit instead of a divide-by-2 approach

also proves to be beneficial in improving the quadrature operation. By applying the I/Q calibration technique of Chapter 7 in Section 7.9.1, the image signal is further reduced by 14 dB (Fig. 8.5(b)). Moreover, the LO leakage and IQ image suppression performance of the RF-DAC is also examined at other frequencies. For example, utilizing a 2.4 GHz carrier signal while applying 2.4 MHz I_{BB-up} and Q_{BB-up} single tone baseband signals, as depicted in Fig. 8.5(c)–(d), the LO leakage and IQ image are approximately the same as in the 2.1 GHz scenario. Note that, based on the static measurement results in Fig. 8.2(a)–(b), RF-DAC performance is optimum at 2.1 GHz frequency instead of the targeted frequency of 2.4 GHz due to an imperfect estimation of the parasitic capacitances. This fact is also obvious by comparing Fig. 8.5(a) with Fig. 8.5(c). According to these dynamic measurement results, without applying calibration, the LO leakage and IQ image performance of the RF-DAC at 2.1 GHz are approximately 7.5 and 3.5 dB more superior than at 2.4 GHz. Nonetheless, utilizing the calibration makes them approximately the same. It should be reiterated that this calibration is carrier frequency dependent due to employing the passive power combiner.

The RF-DAC linearity significantly improves by using either of the two DPD approaches that were discussed previously in Sections 7.9.2 and 7.9.3.

8.3.2 The RF-DAC's Linearity Using AM-AM/AM-PM Profiles

First, utilizing the AM-AM/AM-PM profiles of Section 7.9.2 and applying only a fourth-order memoryless polynomial approximation (7.9) - (7.12), the linearity of the RF-DAC improves more than 25 dBc. Figs. 8.6(a)–(b) demonstrate the two-tone test measurement results before and after using the DPD of Section 7.9.2. In this measurement, the tone spacing is designated at 2.2 MHz, and the total power exceeds 16 dBm. The leakage level is below -55 dBm (-68 dBc) and the third-order intermodulation product (IM_3) is improved to more than -50.4 dBc. Since only the fourth-order polynomial is used, the nonlinearities of higher intermodulation products do not diminish as much as IM_3. Although the DPD improves the linearity of the lower-order odd intermodulation products (i.e., 3^{rd}–7^{th}), it deteriorates higher-order odd intermodulation products (bandwidth expansion). Comparing Figs. 8.6(a)–(b), the 9^{th} to 15^{th} intermodulation products worsen[4].

As stated in Sections 7.9.2, applying AM-AM/AM-PM DPD suppresses the higher intermodulation products from the envelope and phase profiles of the modulated RF signal. According to Figs. 8.6(d), the phase deviation without applying DPD exceeds 10°. Applying DPD, however, makes the phase profile almost constant. Based on the simple expression in Appendix A, Section A.3, 10° produces a significant amount of third order intermodulation (IM_3) which can be as high as -33 dBc. As a result, most of the linearity improvements originate in the phase correction. Note that, to justify the latter argument, a comparison

[4]In Appendix A, Section A.4 a simple explanation is presented in order to disclose the supporting reason for bandwidth expansion of DPD.

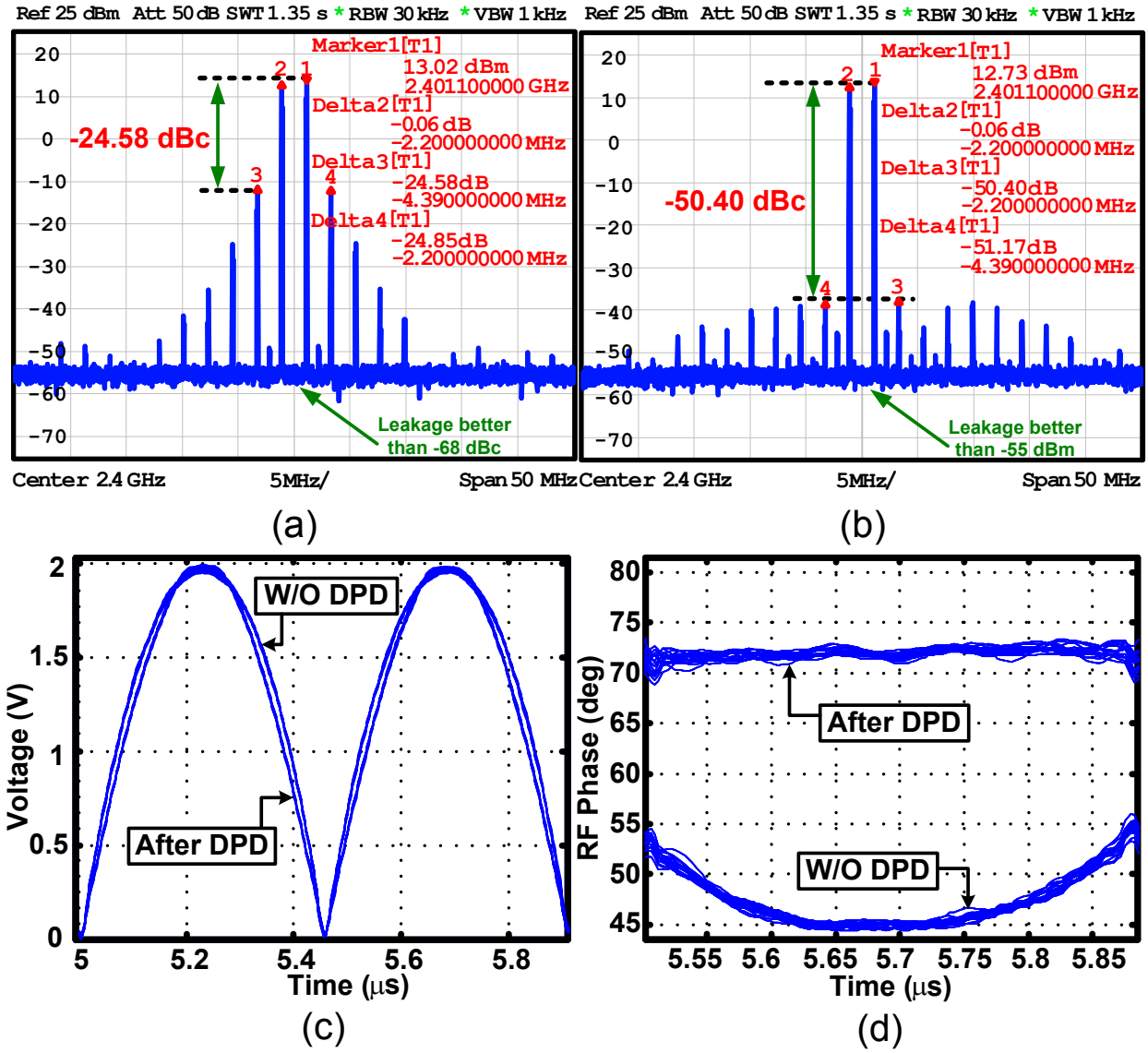

Figure 8.6: Two-tone linearity test: (a) without DPD; (b) with DPD. Its corresponding (c) envelope; and (d) phase.

is made between the frequency contents of the envelope profiles in Figs. 8.6(c). Based on this analysis, the envelope profile is improved only about 3 dB when employing DPD. Thus, the linearity improvements are primarily related to the phase profile correction. It is worth noting that, when utilizing this DPD approach, a number of two-tone as well as multi-tone measurements have been performed in which their related signal bandwidth reaches up to 150 MHz. For example, for a 16-tone test signal with the bandwidth of 3.2 MHz, the spurious free dynamic range (SFDR) is 46 dB. By doubling the bandwidth, the SFDR decreases by 3 dB which could be due to the fact that the "effective" over-sampling rate becomes half.

Note that the AM-AM/AM-PM profiles are created utilizing the measurement results

of the two-tone test. As stated in [107], there are three methods to perform the two-tone test. In this work, the second approach is employed whereby I_{BB-up}=Q_{BB-up}=cos($\omega_m t$) are applied to the RF-DAC chip. The related advantage of utilizing this approach lies in the fact that it is, indeed, a double side band two-tone test scenario which more effectively employs the related bandwidth of the two-tone signal. Otherwise stated, measuring a single side band two-tone signal in which its related tone spacing is 10 MHz requires 60 MHz bandwidth to measure IM_3 components whereas, in the double side band scenario, the required bandwidth is just 30 MHz.

8.3.3 The RF-DAC's Linearity Using Constellation Mapping

In addition, using the constellation-mapping DPD approach of Chapter 7, Section 7.9.3, a variety of I/Q signals have been tested. The QAM signals with different modulation complex points and bandwidths are applied to the transmitter.

First, a single-carrier "7.16 MHz QAM" signal is generated and applied to the chip. Fig. 8.7(a) exhibits the measured spectrum of a single-carrier "7.16 MHz 4-QAM" signal with and without applying the DPD. Utilizing the DPD improves the RF-DAC linearity by more than 19 dB. The adjacent channel power ratio (ACPR) is better than -47.7 dBr while the alternate channel power ratio is better than -49 dBr. The I/Q trajectory and constellation diagram are depicted in Fig. 8.7(b)–(c). The measured EVM is -38 dB. Moreover, Fig. 8.7(d) indicates the amplitude probability profile of the measured down-converted RF signal. Based on that, its mean and peak RF power are 18 dBm and 21.23 dBm, respectively, while its related drain efficiency is 24.9%.

Second, a single-carrier "7.16 MHz 64-QAM" signal is generated and applied to the chip. Fig. 8.8(a) shows the measured spectrum of a single-carrier "7.16 MHz 64-QAM" signal with and without application of the DPD. Utilizing the DPD improves the RF-DAC linearity by more than 16 dB. The adjacent channel power ratio (ACPR) is better than -44 dBr while the alternate channel power ratio is better than -49 dBr. The I/Q trajectory and constellation diagram are depicted in Fig. 8.8(b)–(c). The measured EVM is -33.5 dB. Note that, due to utilizing random in-phase and quadrature-phase codes as well as limited memory depth, 3 out of 64 codes are inaccessible in the original baseband I/Q codes. Thus, the resulting constellation diagram of Fig. 8.8(c) only comprises 61 baseband codes. Moreover, Fig. 8.8(d) illustrates the amplitude probability profile of the measured down-converted RF signal. According to Fig. 8.8(d), its mean and peak RF power are 15.55 dBm and 20.48 dBm, respectively, while the related drain efficiency is 18%.

Third, a single-carrier "21.9 MHz 64-QAM signal" is generated and applied to the chip. Fig. 8.9(a) shows the measured spectrum of a single-carrier "21.9 MHz 64-QAM" signal with and without application of the DPD. Employing the DPD improves the RF-DAC linearity by more than 14 dB. The adjacent channel power ratio (ACPR) is better than -40 dBr while the alternate channel power ratio is better than -43 dBr. The I/Q trajectory and constellation

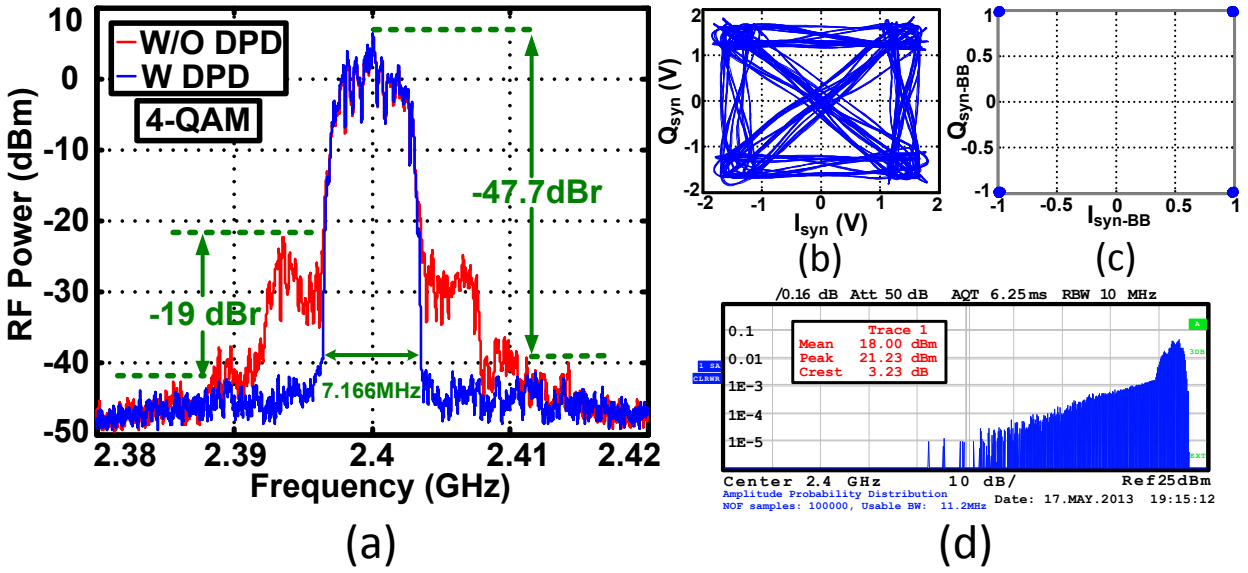

Figure 8.7: "7.16 MHz 4-QAM" measurement results, (a) spectrum with and without DPD; (b) I_{syn}/Q_{syn} trajectories; (c) 4-QAM constellation; (d) amplitude probability distribution.

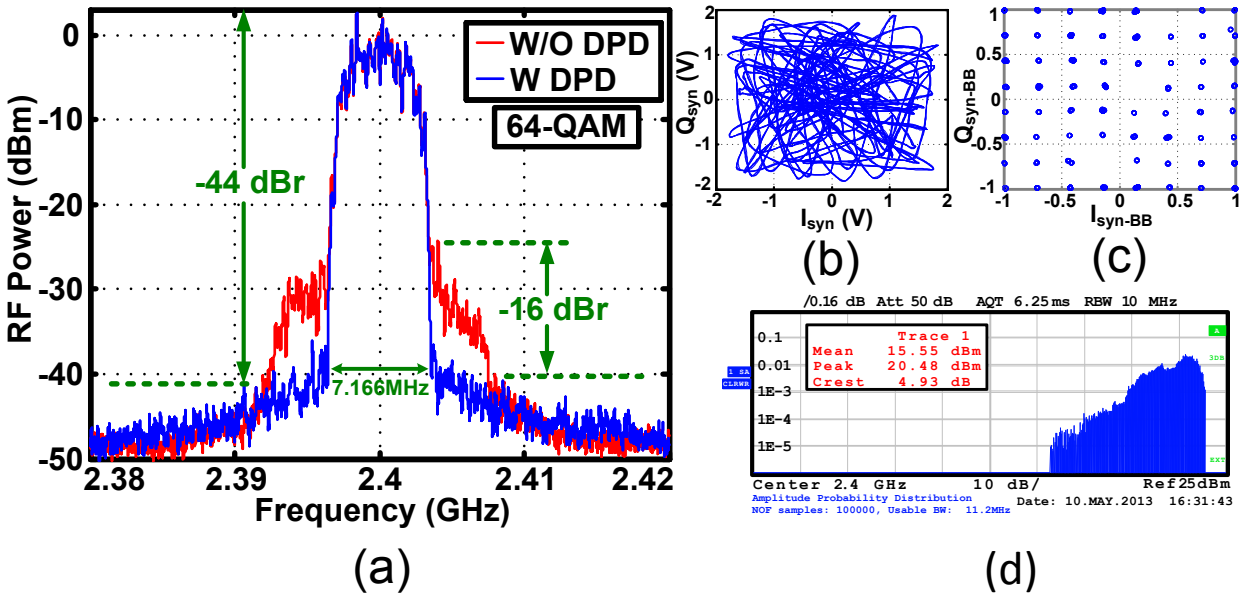

Figure 8.8: "7.16 MHz 64-QAM" measurement results, (a) spectrum with and without DPD; (b) I_{syn}/Q_{syn} trajectories; (c) 64-QAM constellation; (d) amplitude probability distribution.

diagram are shown in Fig. 8.9(b)–(c). The measured EVM is -28 dB. Moreover, Fig. 8.9(d) depicts the amplitude probability profile of the measured down-converted RF signal. Based on Fig. 8.9(d), its mean and peak RF power are 13.30 dBm and 19.32 dBm, respectively, while the related drain efficiency is 14%.

Moreover, the chip is tested using a multi-carrier "20-MHz, 256-QAM, OFDM" sig-

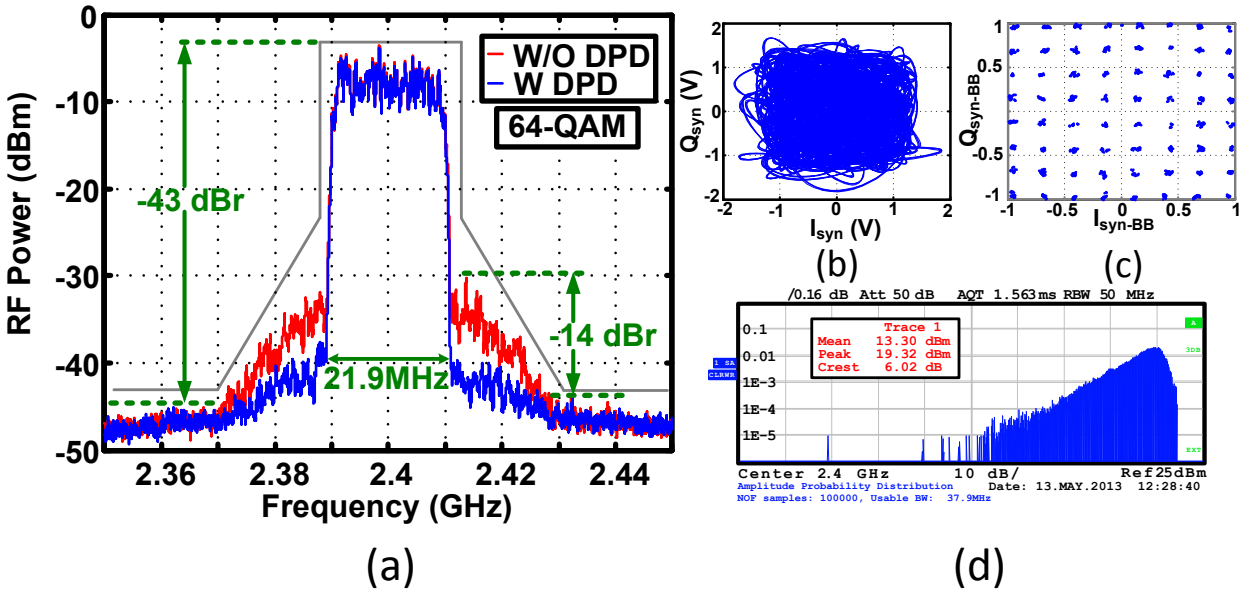

Figure 8.9: "21.9 MHz 64-QAM" measurement results, (a) spectrum with and without DPD; (b) I_{syn}/Q_{syn} trajectories; (c) 64-QAM constellation; (d) amplitude probability distribution.

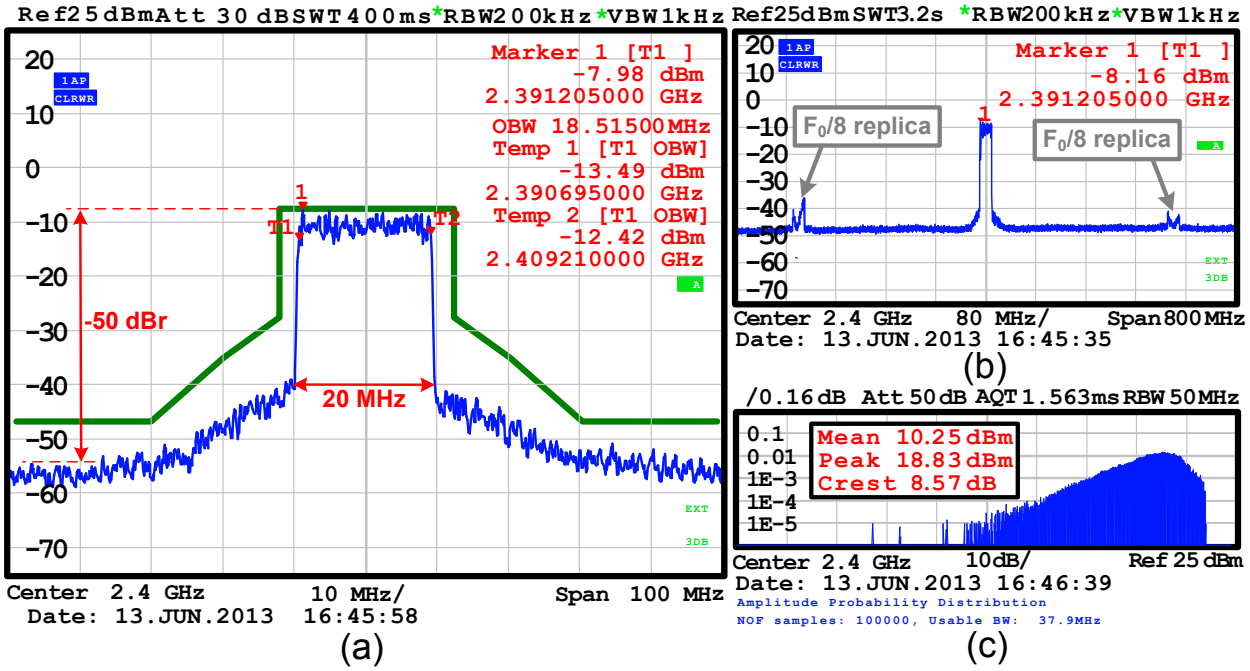

Figure 8.10: "20 MHz 256-QAM OFDM" spectrum using DPD, (a) Close-in; (b) full span; (c) amplitude probability distribution.

nal. The close-in and far-out spectrum measurement results are depicted in Fig. 8.10(a)-(b), respectively. According to the measurement results of Fig. 8.10(a), the close-in linearity exceeds 50 dB. Therefore, it can pass the close-in spectral mask by a large margin. Nonetheless, due to the zero-order-hold operation, its far-out spectrum contains replicas, which are dis-

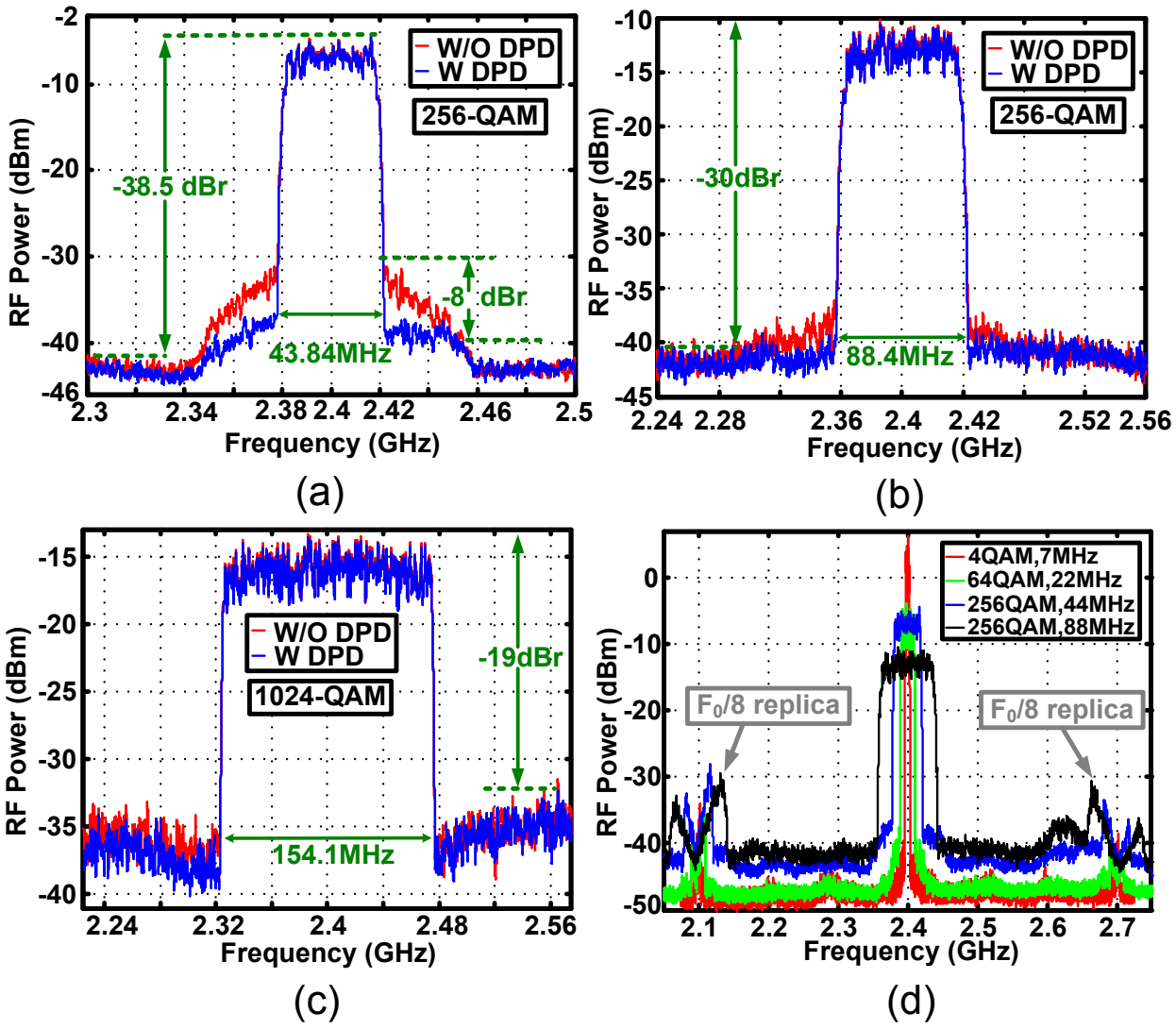

Figure 8.11: Spectrum measurement results of different QAM signals with and without DPD, (a) "44 MHz 256-QAM", (b) "88 MHz 256-QAM", (c) "154 MHz 1024-QAM", (d) QAM spectrum including replicas.

tinguished in Fig. 8.10(b). Additionally, according to an amplitude probability distribution measurement result, which is shown in Fig. 8.10(c), the average power is 10.25 dBm, while its related PAPR is as high as 8.6 dB.

The chip performance is examined for other single-carrier complex QAM signals. The measured spectra of the RF-DAC chip are demonstrated in Figs. 8.11(a)–(c) while employing a single-carrier "44 MHz 256-QAM", "88 MHz 256-QAM", and "154 MHz 1024-QAM", respectively. Since the operational bandwidth of our available VSA is limited to 7 MHz with the possibility of a 20 MHz extension, it was not feasible to measure EVM related to Figs. 8.11(b)–(c). However, it is evidence that the simple DPD lookup table of Fig. 7.14(b) is still relevant up to 44 MHz. The RF-DAC indicates memory effects but only for higher

Table 8.1: Chip performance summary

Technology	65 nm CMOS
Transistor	Standard "Vt", baseline transistor
Power combining network	On-chip balun and capacitors
Input clock, single-ended	On-chip input transformer
Resolution	2×13-bit
Supply voltage	0.6-1.3 V
Operational carrier frequency	60 MHz-3.5 GHz
Max RF power	22.8 dBm
Max drain/system efficiency	42/34%
LO generation current	33 mA @ 2.4 GHz
SRAM memory current	10 mA @ 2.4 GHz, 2×8 k-word
LO leakage / IQ image	> -70 dBc/-58 dBc
Baseband bandwidth	37 kHz. . . 154 MHz @ 2.4 GHz
EVM 256-point/64-QAM	-32/-33.5 dB@15 dBm
Static noise floor full/low power	-160/-150 dBc/Hz
DPD	Simple lookup table

frequencies and, as a result, the DPD lookup table should be amended[5].

The memory effects are due to the limited amount of memory as well as on-chip ground sharing of the clock generation circuitry, digital baseband and the DRAC parts. Additionally, as discussed in Chapter 5, Section 5.1, signals with wider bandwidth exhibit higher out-of-band spectra (see Fig. 8.11(d)). The reason for such a higher noise floor lies in the fact that, due to the fixed upsampling clock rate (f_{CKR}=f_0/8), the "effective" over-sampling rate of wider band signals is lower than for narrower band signals, therefore, the noise floor is higher. Moreover, in this chip, the SRAM memory size is limited to 8 kword which increases the noise floor for wideband signals. Note that for the "154 MHz 1024-QAM" scenario, the DPD improvement is very minimal. The reason lies in the fact that, since the upsampling clock, CK_R, is 300 MHz due to spectral regrowth, the out-of-band spectral images and the main signal spectrum, in this case, a 154 MHz 1024-QAM signal, are conjoined to one another. In addition, note that the DPD profiles are principally created considering only in-band

[5]It should be pointed out that the measurement results in Figs. 8.8–8.11 have been obtained employing only a fixed, static, memoryless lookup table of Fig. 7.14(b).

Table 8.2: Comparison summary of I/Q, Polar, Out-phasing transmitter

Ref	Proc. (nm)	Resol. (bit)[1]	RF Power (dBm)	Drain Eff. (%)	EVM[2] (dB)	BB-BW (MHz)
Nokia [58]	130	11 I/Q	-2	0.04@1.2 V	-34	5
STMicro. [59]	65	12 I/Q	2.6[3]	1.2@1.2 V	-32.4	16
NXP [60, 61]	45	13 I/Q	5	10@1.8 V	-34	5
Intel [64]	32	11 I/Q	27.1	28.8@1.8 V	-25	20
Stanford [17]	180	10 Polar	20.7	23.2@1.7 V	-27	20
Berkeley [21]	65	9 Polar	23.3	43@1.2 V	-28	20
Intel [51]	32	8 Outphasing	26	35@2.0 V[4]	-31.5	40
Mediatek [66]	40	13 I/Q	24.7	37@1.8 V	-36	160
This work [70, 71]	65	13 I/Q	22.8	42@1.3 V	-28	154

[1] Bit-resolution including sign bit with its corresponding architecture of the transmitter.
[2] EVM is reported at maximum reported measurable bandwidth, which are either 5 or 20 MHz.
[3] The average power is reported. Perhaps the peak is 9 dBm with 7% drain efficiency (off-chip balun).
[4] They only reported their system efficiency. Note that their power combining network is off-chip.

nonlinearities. As a result, the DPD profiles must be updated to manage the aforementioned wideband signal. Fig. 8.11(d) also demonstrates the spectral replicas of the ZOH operation of RF-DAC. Based on Section 5.1, one simple solution for decreasing the noise floor and spectral replicas of RF-DAC would be increasing the upsampling clock rate, e.g. f_{CKR}=$f_0/4$ or even higher.

Table 8.1 summarizes the performance of the proposed I/Q RF-DAC. Table 8.2 compares

this work against relevant I/Q publications [58–61, 64, 66]. The proposed RF-DAC and the Mediatek work [66] are evidently more prominent than the rest for demonstrating the most superior performance. However, [66] exploits the 50% duty cycle, 40-nm CMOS technology, supply voltage of 1.8 V, upsampling clock rate of 804 MHz and, most importantly, requires a very sophisticated DPD algorithm. On the contrary, this work uses a very simple DPD lookup table due to the fact that the selected duty cycle is 25%, and the proper power combining network also improves isolation between I_{path} and Q_{path}. The drain efficiency of this work is higher than in [66] and, if our RF-DAC were to be designed in a finer technology node, the drain efficiency would be even higher. Note that, in the Intel SoC work [64], they achieved high RF power with lower drain efficiency due to incorporating a conventional DAC, low pass filter, passive quadrature mixer and class-AB PA. In contrast, the proposed 2×13-bit RF-DAC provides reasonable RF output power with higher efficiency using simpler architecture. In addition, Table 8.2 also presents the best performance numbers of recently published polar [17, 21, 49] and outphasing transmitters [51, 55, 56]. As evidenced, the I/Q transmitters can manage very wideband signals along with more effective EVM. Due to its versatility, high efficiency, wide bandwidth, and fine resolution while requiring only a small chip area, the implemented wideband 2×13-bit all-digital *orthogonal* I/Q RF-DAC is a very promising candidate for future multi-mode/multi-band RF CMOS transmitters.

8.4 Conclusion

In this chapter, the high-resolution wideband 2×13-bit all-digital I/Q transmitter, which was introduced in Chapter 7, is thoroughly measured. First, the chip is tested in continuous-wave mode operation. It is demonstrated that, with a 1.3 V supply and, of course, an on-chip power combiner, the RF-DAC chip generates more than 21 dBm RF output power within a frequency range of 1.36–2.51 GHz. The peak RF output power, overall system, and drain energy efficiencies of the modulator are 22.8 dBm, 34%, and 42%, respectively. The measured static noise floor is below -160 dBc/Hz. Employing a simple calibration algorithm, the digital I/Q RF modulator demonstrates an IQ image rejection and LO leakage of-65 dBc and -68 dBc, respectively. The RF-DAC could be linearized employing either of the two DPD approaches: memoryless polynomial or a 2×1D lookup table. Its linearity is examined utilizing single-tone as well as multi-tone 4/16/64/256/1024-QAM baseband signals while their related modulation bandwidth can be as high as 154 MHz. Using AM-AM/AM-PM DPD improves the linearity by more than 25 dB. Moreover, the static, memoryless constellation-mapping, lookup table DPD is applied to the RF-DAC which improves linearity by more than 14 dB while the measured EVM is better than -28 dB. These numbers indicate that this innovative concept is a viable option for the next generations of multi-band/multi-standard transmitters. It can perform as an energy-efficient RF-DAC in a stand-alone digital transmitter directly (e.g., for WLAN) or as a pre-driver for high-power basestation PAs.

Chapter 9

Conclusion

In this dissertation, the concepts, design, and implementation of high-resolution, wideband, all-digital I/Q RF-DAC in 65-nm bulk CMOS process are discussed. In this aspect, the final chapter of this work is presented. Section 9.1 summarizes the thesis, and it also reiterates the accomplishments that are achieved throughout the thesis. Section 9.2 proposes certain techniques in order to mitigate the related drawbacks of the current implemented RF-DAC transmitter. Moreover, it offers a number of procedures to expand this work to the next level. Finally, Section 9.3 briefly envisions the future direction of RF transceivers.

9.1 The Thesis Outcome

With the proliferation of wireless networks, there is a need for more compact, low-cost, power-efficient transceivers that are capable of supporting the comprehensive communication standards including GSM, WLAN, Bluetooth, GNSS, FM and 4G of 3GPP cellular. To accommodate the ever-increasing appeal of higher data throughputs within the crowded frequency spectrum of 500 MHz to 6 GHz, these communication standards utilize extremely efficient complex-modulated baseband signals in which their related bandwidths can be as wide as 160 MHz. Moreover, due to the extreme cost pressures of consumer electronics, migration to a more advanced nanometer-scale CMOS process, which was primarily developed for fast and low-power digital circuits operating at low supply voltages, is necessary. Additionally, this fast-evolving CMOS technology unfolds the possibility of integrating the entire radio including the DSP as well as the RF transmitter and receiver with just one single chip. Conventionally, the RF transmitter could not be implemented as a fully-integrated circuit like the other building blocks of the corresponding RF transceiver could be as it consists of the bulky DACs, filters, mixers, and the power amplifier (PA). As a consequence of the existing previously mentioned components, especially the PA, the RF transmitter is the most power consuming element of the RF transceivers. This part affects EVM, out-of-band

emission and, most significantly, the battery lifetime of the mobile devices.

Consequently, the objective of this thesis is to implement a novel, fully-integrated RF transmitter which should be power-efficient and, additionally, must support multi-mode and multi-band communication standards. To achieve these ambitious goals, this work has extensively utilized more and more digital circuitry rather than the traditional analog counterparts. Otherwise stated, this thesis attempts to benefit from the ongoing CMOS technology properties which tend to drive the design of cellular and wireless building blocks toward the digital domain where transistors are employed as switches rather than the current sources.

The concise review of the different transmitter architectures has revealed that the efficiency of the polar modulator is higher than the Cartesian (I/Q) counterpart. However, due to the bandwidth expansion of the polar transmitter resulting from employing the nonlinear coordinate rotation digital computer (CORDIC) algorithm to convert in-phase and quadrature-phase baseband data into the envelope and phase information, the I/Q modulator is the preferred architecture as it is able to address very wideband complex-modulated baseband signals while achieving a reasonable power efficiency. Likewise, to simplify the design, gain more benefits from the nanometer CMOS process, and to substantially eliminate the analog circuitry, the digital I/Q architecture is selected rather than the analog counterpart.

The most straightforward digital I/Q modulator, however, suffers from non-orthogonal operation due to overlap between their related 50% duty cycle differential quadrature clocks [66]. The non-orthogonal summation degrades in-band performance such as EVM, and it also deteriorates out-of-band spectrum due to generated spectral regrowth. To improve the foregoing dynamic performance of this modulator, therefore, employing sophisticated digital predistortion (DPD) is inevitable [66]. On the other hand, this dissertation has proposed a novel time-multiplexing orthogonal summation which has utilized the non-overlapping 25% duty cycle differential quadrature clocks. Furthermore, it has been demonstrated that the orthogonal summation can still be obtained even when employing differential quadrature clocks which have a related duty cycle of less than 25 percent. In addition, in contrast to previous publications [60, 61], the orthogonal summation is performed by digital power amplifier (DPA) unit cells that increase the RF output power as well as improve the power efficiency. Thus, the orthogonal digital I/Q modulator represents a radio-frequency digital-to-analog converter (RF-DAC). To validate the orthogonal summing operation, a 2×3-bit all-digital I/Q RF-DAC has been designed and implemented in a TSMC 65-nm bulk CMOS process. According to measurement results, the composite RF signal is the result of vectorial summation of in-phase (I) and quadrature-phase (Q) signals. Hence, the orthogonal summation has been substantiated.

It has been indicated that the direct digital modulation system produces quantization noise together with spectral replicas due to zero-order-hold operation. As stated, the noise performance of the RF-DAC is related to the resolution of the digital power mixer which

is, indeed, a digital-to-RF-amplitude converter (DRAC). Thus, the DRAC executes the orthogonal summing operation, frequency upconverting and, most importantly, RF power amplification. The DRAC outputs are connected to a passive power combiner that facilitates the transformation of the upconverted digital signals into a "high-power" continuous-time RF output in an energy efficient manner. It has been revealed that employing upconverting clocks with the duty cycle of 25% is a necessary, but not sufficient, condition for the orthogonal operation. Consequently, this dissertation has proposed an innovative class-E-based power combiner that properly realizes the orthogonal summing operation in a power-efficient approach. The power combining network comprises a transformer balun together with primary and secondary switch-capacitor tuners. To achieve an efficient high-power RF output, the I/Q RF-DAC is pushed to operate in the saturated power region, thus it must be digitally predistorted (DPD) in order to restore its in-band and out-of-band dynamic performance.

In contrast to [66] utilizing a very straightforward constellation mapping DPD, the out-of-band nonlinearity is improved by almost 19 dB. The proposed constellation mapping DPD is based on one-dimensional (1D) mapping of two individual in-phase and quadrature-phase upsampled baseband signals. In particular, since the in-phase and quadrature-phase paths are orthogonal, the DPD does not require a two-dimensional (2D) exhaustive search of the whole constellation diagram, which is required in [66].

To verify the concept of the proposed high-resolution direct digital RF transmitter, a wideband 2×13-bit all-digital I/Q RF-DAC has been implemented in TSMC 65-nm bulk CMOS process. The maximum power and its related drain efficiency are 22.8 dBm and 42%, respectively. The digital I/Q RF modulator shows an IQ image rejection and LO leakage of -65 dBc and -68 dBc, respectively. Its linearity is examined using single-carrier, complex-modulated 4/16/64/256/1024-QAM as well as multi-carrier 256-QAM OFDM baseband signals, while their related modulation bandwidth is as high as 154 MHz. The measured EVM for a "single-carrier 22MHz 64-QAM" signal is better than -28 dB. The measurement results confirm that the proposed solution is a logical alternative for the future generations of multi-band/multi-standard transmitters.

9.2 Some Suggestions For Future Developments

Although this thesis has introduced a novel 2×13-bit all-digital I/Q RF-DAC that is able to manage very wideband baseband signals, it continues to require further steps to fully comply with the ever-evolving communication standards. Due to the lack of experience and knowledge regarding the digital hardware IC design flow, the digital synthesis, and the limited amount of time, the digital baseband processing (DSP) in this thesis was conducted off-chip. As indicated in previous chapters, the processed baseband I/Q data were transferred and stored in two on-chip SRAM memories. Since the SRAM memories are synchronized with the entire RF-DAC exploiting an on-chip $f_0/8$ clock, the subsequent spectral replicas

resulting from zero-order-hold operation are located at $f_n = f_0 \pm n \times f_0/8$ (see Fig. 5.3 and Fig. 5.4 as well as equations (5.2)-(5.3)). As a result, the following solutions are recommended in order to suppress them further.

- The simplest manner is to increase the clock sampling rate (f_{CKR}) from $f_0/8$ to possibly f_0 [59]. As stated in Chapter 5, its primary disadvantage is greater power consumption which will be less significant as a finer node process such as 28 nm CMOS technology will be used. Note that additional advantages of adopting a higher sampling rate include the improvement of the related dynamic range and the ability to manage wider modulation bandwidths.

- Instead of employing zero-order-hold interpolation, a first-order-hold interpolator will be incorporated [59, 108, 109]. This interpolator provides a double-notch filter, i.e. $\text{sinc}^4((f - f_0)/f_{CKR})$, at $f_n = f_0 \pm n \times f_{CKR}$. Thus, it reduces the amplitude of the related spectral images.

- As an ultimate solution to eliminate even more of the corresponding spectral images, the Farrow interpolator [110] can be used. This interpolator generates a triple notch, i.e., $\text{sinc}^6((f - f_0)/f_{CKR})$, at all multiples of f_{CKR} [108].

Consequently, the entire DSP, including the digital interpolators and their corresponding finite impulse response (FIR) filters, should be implemented in combination with the I/Q RF-DAC. In addition, as stated in Chapters 7 and 8, the linearity of the RF-DAC is improved using constellation mapping DPD so as to suppress the AM-AM and AM-PM nonlinearities of the RF-DAC in order to meet stringent communication standards. Thus, the DPD lookup table must be stored in a designated on-chip SRAM. Note that this lookup table must be positioned before the interpolator blocks in order to minimize the amount of power employed by the low-speed synchronizing clock. As a result of this arrangement, the DPD lookup table must comprise not only the nonlinearity profiles of the RF-DAC but also the non-ideality of its corresponding interpolators and FIR filters. Hence, the DPD operation will be moderately complicated.

Note that, throughout this thesis, the general premise was that the RF-DAC is always loaded by an ideal and fixed 50 Ω ($VSWR$=1) which resembles the impedance of an ideal antenna. Nonetheless, in reality, the antenna's impedance can be anything but 50 Ω. Although based on the brief discussion in Chapter 4, Section 4.1.5, Fig. 4.9(c), the RF-DAC is able to tolerate a small deviation from 50 Ω, yet it can definitely not manage large $VSWR$ as it affects the output power, efficiency, EVM and, most importantly, its linearity. The moderate $VSWR$ such as (1.5:1) can be accomplished by employing coarse tuning switch-capacitor banks. The disadvantage would be larger area, layout complexity and, most importantly, increased power loss due to the related losses of coarse tuning switches. However, in the case of $VSWR$ larger than (2:1), an additional antenna tuning circuitry must be employed and

positioned at the output node of the RF-DAC. Using this technique, various corresponding load reflection coefficients (Γ_L) which are related to the antenna's impedance will be transferred to the origin of the Smith-chart ($\Gamma_L = 0$).

Furthermore, in the proposed digital I/Q transmitter, the corresponding higher harmonic frequency contents of the related LO signal should be diminished. For example, if f_0 is 2.4 GHz, the 2^{nd} and 3^{rd} harmonic rejection ratios of the current RF-DAC chip would be approximately -42 and -20 dBc, respectively. The 2^{nd} harmonic frequency content is primarily due to employing an imperfect balance-to-unbalance (balun) structure. As stated in Chapter 6, Section 6.6, the imbalanced property of the transformer balun is principally due to higher inter-winding capacitance. Moreover, the balun should be laid out symmetrically to improve differential-to-single-ended operation. To legitimize these recommendations, based on the simulation as well as measurement results of the 2×3-bit I/Q modulator in Chapter 4, and due to employing a more balanced transformer structure, the 2^{nd} and 3^{rd} harmonic rejection ratios are -51 and -31 dBc, respectively. Since the modern communication standards require greater than 60 dBc harmonic rejections, the 3^{rd} harmonic frequency must be further filtered out. Thus, the third harmonic frequency suppression is a difficult task and, perhaps, requires novel breakthrough ideas and additional efforts. Note that, since the objective of the I/Q RF-DAC is to operate as a software-defined transmitter, the desired 3^{rd} harmonic rejection filter must be tunable. This fact makes the third harmonic frequency suppression even more sophisticated. As additional way to mitigate this issue, since the 3^{rd} harmonic frequency component of the RF output signal is originated from the LO clock pulse (square waveform), would be to employ an LO clock that only contains fundamental and 2^{nd} harmonic frequency as well as exploiting more linear switches. This would dramatically reduce the subsequent 3^{rd} harmonic frequency content of the RF output signal.

Also, as stated previously, it is worth mentioning that the modern communication standards such as Wi-Fi and 4G of 3GPP cellular, utilize the complex-modulated signals with the relative high peak-to-average power ratio (PAPR) to achieve higher data throughputs within the restricted bandwidth. As a result, the RF-DAC should be efficiently operated not only at its maximum power but also at its power back-off region. For example, wireless communication standards such as WLAN, WiMAX, and LTE exploit the OFDM modulation in which the crest factor could be as high as 20.6 dB. The current RF-DAC can not effectively manage such a high PAPR (see Fig. 8.2(d)). Over the last several decades, three predominant power amplifier architectures have been proposed to efficiently operate in the power back-off region. They are as follows: outphasing [53], Doherty [111] and envelope tracking [112]. The latter approach is only applied to the polar transmitters whereby the PA supply voltage is modulated according to the envelope information while the phase signal drives the saturated PA. Moreover, it is also possible to manipulate its related matching network in such a way that it increasingly compensates the related power losses in the power back-off region [113]. The all-digital I/Q RF-DAC, however, can be upgraded using either the mixed-mode N-way Doherty configuration [103, 114] or the mixed-mode N-way outphasing [106, 115].

9.3 Future Trends

As mentioned in Chapter 1 as well as in this chapter, RF transceivers are directed towards the implementation of a universal radio which manages numerous communication standards. As a result, only very recently, has the introduction of combo chips occurred in order to perform Wi-Fi/Bluetooth/FM or Bluetooth/GNSS/FM communication standards employing only one single chip. These solutions as well as our proposed I/Q RF-DAC, which can also serve as a software-defined-transmitter (SDT) chip, will be the game changer and will reduce the cost, size and, most probably, the weight of mobile devices. In addition, arrays of these devices can be integrated on just one IC chip to realize heterogeneous radios whose modes of operation are defined by the users. Furthermore, these wideband I/Q RF-DACs will accelerate the adaptation of so-called 5G Wi-Fi (802.11ac) or the upcoming communication standards such as the sub-terahertz wireless communication as well as the 5^{th} generation mobile network (5G) into wireless portable devices.

Appendix A

Additional Elaboration

A.1 Universal Asynchronous Receiver/Transmitter

The Universal Asynchronous Receiver/Transmitter (UART) controller takes a byte of data and transmits the individual bits in a sequential style. In other words, the basic job of UART is to convert data from parallel to serial format for the transmission as well as converting data from serial to parallel format during reception. Fig A.1 depicts the block diagram of the implemented UART controller in combination with the two on-chip SRAM memories in the proposed 2×13-bit all-digital I/Q RF-DAC. The upsampled baseband signals are generated in PC (MATLAB) and they are subsequently transferred to the chip via UART protocol. The I/Q data are stored into two on-chip SRAMs. Note that in order to preserve continuity of the baseband input data, two auto-loop memory readout units are exploited.

A.2 Matching Network Equations (Chapter 6)

Based on [94] [23], $f(D)$ and $gt(D)$ are two functions which depend on D_1, φ, and g. For the sake of clarity, these parameters are redefined here. "D_1" is related to the duty cycle of the upconverting clock. In Raab's paper, it is defined as y and is located in [94, Fig. 2] and expressed as:

$$D_1 = \pi \times (1 - D) \tag{A.1}$$

"φ" is the phase difference between the load output voltage and the drain voltage of the switching power amplifier. It is located in [94, Figs. 1 and 2, and eq. 3.8]

$$\varphi(D_1) = \tan^{-1}\left(\left(\frac{-1}{D_1}\right) + \cot(D_1)\right) \tag{A.2}$$

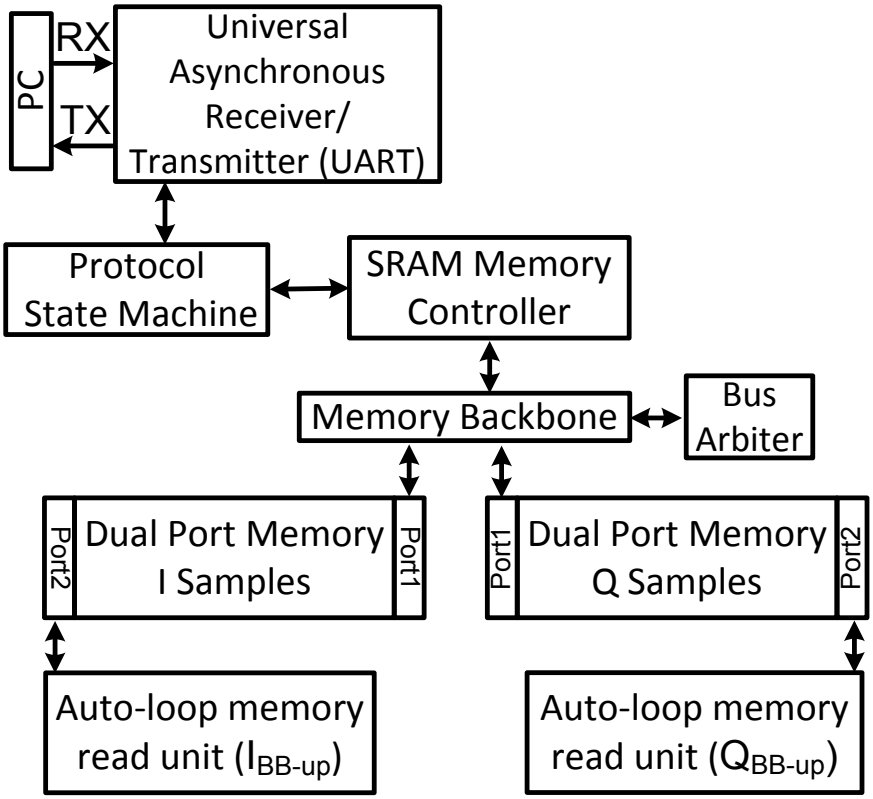

Figure A.1: The schematic of the implemented UART controller along with on-chip SRAMs.

Note that here, ς, the slope of the waveform at the time of turn-on [94, eqs. 3.3 and 3.4], is considered zero. "$g(D_1)$" is a proportionality function which relates the load output voltage (c) with the choke DC current (I_{DC}) and the output load resistor (R_{load}). It can be expressed as [94, eq. 2.19]:

$$g(D_1) = \frac{c}{I_{DC} \times R_{load}} \tag{A.3}$$

It is located in [94, eq. 3.9]:

$$g(D_1) = \frac{D_1}{\cos(\varphi) \times \sin(D_1)} \tag{A.4}$$

Based on [94, eq. 3.11], the capacitor's susceptance is defined as:

$$B(D_1) = \frac{f(D_1)}{R_{load}} \tag{A.5}$$

Consequently, $f(D)$ can be expressed as:

$$f(D) = f(D_1) = \frac{2}{\pi g^2} \times \Big(D_1^2 + D_1 g \sin(\varphi - D_1) - g \sin(\varphi) \sin(D_1)\Big) \tag{A.6}$$

Moreover, $gt(D)$ is a proportionality function that relates the reactance of the L_{add} inductance ("jX" in [94, Fig. 1]) with the output load resistor (R_{load}), and it is defined in [94, eq. 3.28]:

$$X(D_1) = gt(D_1) \times R_{load} \tag{A.7}$$

According to [94, eqs. 3.13-3.15 and 3.18-3.19] "$gt(D)$" is expressed as:

$$gt(D) = \frac{q_n(D)}{q_d(D)} = \frac{q_n(D_1)}{q_d(D_1)} \tag{A.8}$$

where q_n and q_d are determined in ([94, eq. 3.18]). Therefore, for $D = 25\%$, $g(D)$, $f(D)$, and $gt(D)$ are as follows:

$$g(D = 25\%) = 5.79925 \tag{A.9}$$

$$f(D = 25\%) = 0.21322 \tag{A.10}$$

$$gt(D = 25\%) = 3.5619 \tag{A.11}$$

Moreover, DET_2 and DET_1, which are employed in (6.30)-(6.32)are defined to simplify the equations, and these two parameters also depend on B_{Cs}, X_{Ladd}, Z_{RX}, G_{sw}, and R_L :

$$DET_2 = 0.0625 + 4 \times \left(\frac{B_{Cs}}{G_{sw}}\right)^2 \tag{A.12}$$

$$\begin{aligned} DET_1 \;=\; & \left(\frac{1}{4} + \frac{R_L}{|Z_{RX}|^2 \times G_{sw}}\right)^2 - \left(\frac{1}{4} + \frac{R_L}{|Z_{RX}|^2 \times G_{sw}}\right) \times \left(\frac{0.028}{DET_2}\right) + \frac{0.0027}{DET_2} + \\ & \left(\frac{0.011}{DET_2}\right)^2 - 0.02533 + \left\{\left(\frac{B_{Cs}}{G_{sw}}\right) \times \left(1 + \left(\frac{0.09}{DET_2}\right)\right) - \frac{X_{Ladd}}{|Z_{RX}|^2 \times G_{sw}}\right\}^2 \end{aligned} \tag{A.13}$$

Consequently, H, K, and T can be expressed as:

$$\begin{aligned} H \;=\; & \left(-2 + \frac{0.106}{DET_2}\right) \times \left(0.0908 - \left(\frac{0.0056}{DET_2}\right) + \frac{R_L}{|Z_{RX}|^2 \times G_{sw}}\right) - \left(\frac{0.4244}{DET_2}\right) \times \\ & \left(\frac{B_{Cs}}{G_{sw}}\right) \times \left(\left(\frac{B_{Cs}}{G_{sw}}\right) \times \left(1 + \left(\frac{0.09}{DET_2}\right)\right) - \frac{X_{Ladd}}{|Z_{RX}|^2 \times G_{sw}}\right) \end{aligned} \tag{A.14}$$

$$K \;=\; -\left(V_{DD} \times 0.0796\right) - a_1 \times (0.075) - b_1 \times (0.3) \times \left(\frac{B_{Cs}}{G_{sw}}\right) \tag{A.15}$$

$$\begin{aligned} T &= \left(\frac{-0.4244}{DET_2}\right) \times \left(\frac{B_{Cs}}{G_{sw}}\right) \times \left(0.41 - \left(\frac{0.0225}{DET_2}\right) + \frac{R_L}{|Z_{RX}|^2 \times G_{sw}}\right) - \\ &\quad \left(-2 + \frac{0.106}{DET_2}\right) \times \left(\left(\frac{B_{Cs}}{G_{sw}}\right) \times \left(1 + \left(\frac{0.09}{DET_2}\right)\right) - \frac{X_{Ladd}}{|Z_{RX}|^2 \times G_{sw}}\right) \end{aligned} \tag{A.16}$$

A.3 AM-AM/AM-PM Relationship (Chapter 7)

For a memoryless nonlinear power amplifier, the input-output relationship can be expressed with a polynomial approximation:

$$\begin{aligned} V_{out} &= f(V_{in}) \\ &= a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 + \ldots \end{aligned} \tag{A.17}$$

In the two-tone test scenario, the input signal is:

$$V_{in} = \cos\omega_1 t + \cos\omega_2 t \tag{A.18}$$

Applying (A.18) as an input signal in (A.17), the following expression is obtained:

$$\begin{aligned} V_{out} &= f(\cos\omega_1 t + \cos\omega_2 t) \\ &= a_1 (\cos\omega_1 t + \cos\omega_2 t) + a_2 (\cos\omega_1 t + \cos\omega_2 t)^2 + a_3 (\cos\omega_1 t + \cos\omega_2 t)^3 + \ldots \\ &= \left(a_1 + \frac{9}{4} a_3\right) (\cos\omega_1 t + \cos\omega_2 t) + \frac{3}{4} a_3 (\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t) + \ldots \\ &= \mu_1 V(f_m) + \mu_3 V(3f_m) + \ldots \end{aligned} \tag{A.19}$$

where $\mu_3 = \frac{3}{4} a_3$ is the IM_3 product, and

$$V(f_m) = V_{in} = \cos\omega_1 t + \cos\omega_2 t \tag{A.20}$$

is the main two-tone signal and

$$V(3f_m) = \cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t \tag{A.21}$$

is the third order intermodulation signal. The foregoing expressions were obtained assuming only amplitude modulation. In fact, (A.19) indicates the AM-AM relationship between the input and the output signal. If the input is a phase modulated signal, however, the effect of AM-PM must be considered. If the output phase can simply be approximated as [22]:

$$\Phi_{out} = \frac{\Phi}{2}(1 + \cos 2\omega_m t) \tag{A.22}$$

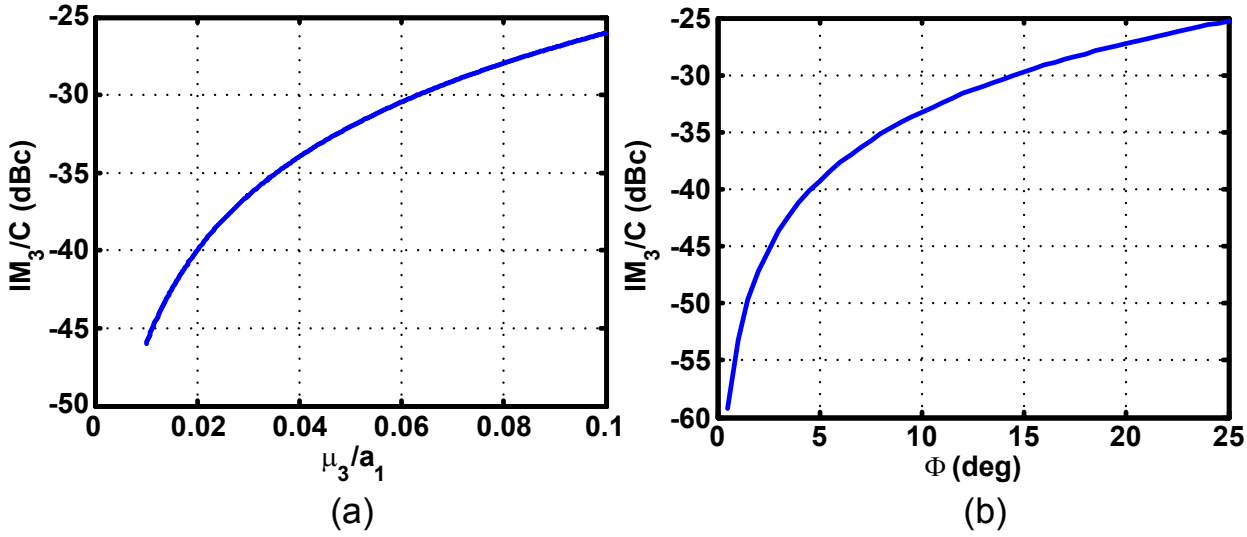

Figure A.2: IM_3/C versus (a) μ_3 (b) Φ.

where Φ is the maximum phase deviation of the phase profile (A.19). The overall RF output can be simply modeled as:

$$\begin{aligned} V_{out} &= (AM-AM)\exp\left(\mathrm{j}(\omega_0 + AM - PM)\right) \\ &= (\mu_1 V(f_m) + \mu_3 V(3f_m) + \dots)\exp\left(\mathrm{j}(\omega_0 + \frac{\Phi}{2}(1+\cos 2\omega_{\mathrm{m}} t)\right) \end{aligned} \tag{A.23}$$

Now, the real part of IM_3 could be simply expressed as follows [22]:

$$\begin{aligned} v_{im3} &= \mu_3 \cos(3\omega_m t) \times \cos\left\{\omega t + \frac{\Phi}{2}(1+\cos 2\omega_m t)\right\} \\ &\cong \frac{\mu_3}{2}\cos\left\{((\omega_0 \pm 3\omega_m)\times t) - \frac{\Phi}{2}\right\} + \frac{\Phi}{8}\sin\left((\omega_0 \pm 3\omega_m)\times t\right) \end{aligned} \tag{A.24}$$

where $\omega_m = 2\pi f_m$ is baseband natural frequency. Based on (A.24), the AM-AM and AM-PM effects are almost orthogonal and could not cancel each other [22]. Fig. A.2 illustrates the IM_3-to-carrier (IM_3/C) based on envelope and phase variations. According to Fig. A.2 and (A.24), if μ_3=0.04, then it produces the IM_3/C of -33 dBc. Furthermore, for 1 and 10 degree of phase deviation, the generated IM_3/C would be -53 dBc and -33 dBc, respectively.

A.4 DPD Bandwidth Expansion (Chapters 7–8)

Note that, as was demonstrated in Subsection 8.3.2, DPD deteriorates higher-order odd intermodulation products. Otherwise stated, it entails a bandwidth expansion and it is, indeed, common for DPD operations. The simple explanation is as follows. Suppose the

nonlinearity profile of a PA or RF-DAC can be expressed as:

$$Y_{out} = X_{in} + X_{in}^2 + X_{in}^3 \tag{A.25}$$

As a result, the predistortion profiles would contain $\sqrt{X}$ term in which its related Taylor series can be approximately expressed as follows:

$$Y_{out} = (\frac{1}{2})X_{in} - (\frac{1}{8})X_{in}^2 + (\frac{1}{16})X_{in}^3 \tag{A.26}$$

Replacing equation (A.26) into (A.25) leads to the generation of up to sixth harmonic. Thus, DPD causes at least twofold bandwidth expansion.

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Summary

[1]Due to the severe cost pressure of consumer electronics, a migration to an advanced nano-scale CMOS processes, which is primarily developed for fast and low-power digital circuits operating at low supply voltages, is necessary, but it forces wireless RF transceivers to exploit more and more digital circuitry. These basic CMOS properties tend to coerce the design of wireless functions towards the digital domain where transistors are utilized as switches rather than current sources. Within the past decade, there have been tremendous efforts towards implementing fully-digital or digitally-intensive RF transmitters in which they demonstrate transmitter designs that operate from baseband up to the pre-power amplifier (PA) stage entirely in the digital domain. In view of this digitalization, the RF transmitter modulator, being the nearest to the antenna as it converts digital baseband modulation samples into an RF waveform, is considered the most critical building block of the transmitter, and it can be in the form of either a polar, Cartesian (I/Q), or an outphasing topology. For wide modulation bandwidths, due to their direct *linear* summation of the in-phase (I) and quadrature-phase (Q) signals and thus the avoidance of the bandwidth expansion, Cartesian modulators are substantiated as the most appropriate choice over their polar or outphasing counterparts. Since the effective modulating sample resolution is the utmost important parameter as it directly impacts the achievable dynamic range, linearity, error vector magnitude (EVM), noise floor, and out-of-band spectral emission, this thesis proposes a wideband, high-resolution, all-digital *orthogonal* I/Q radio-frequency digital-to-analog (RF-DAC).

Chapter 1 briefly provides an overview of the conventional RF radio building blocks. It is discussed that contemporary RF transceivers must support most of multi-mode/multi-band communication standards such as Wi-Fi, Bluetooth, and Fourth Generation (4G) of 3GPP cellular.

In **Chapter 2**, four types of RF transmitter architectures have been briefly described.

[1]Courtesy of Koen Buisman, Marco Pelk, and Mark Stoopman from TU-Delft. Mr. Buisman has translated the summary as well as proposition of this dissertation into Dutch. Then, Mr. Pelk has revised them. Mr. Stoopman has also edited the Dutch version of the proposition.

The analog I/Q modulators are the most straightforward and widely employed RF transmitters. They are later replaced by analog polar counterparts to address their poor power efficiency and noise performance. On the other hand, in the analog polar RF transmitters, their related amplitude and phase signals must be aligned or spectral regrowth is inevitable. Utilizing digitally intensive polar RF transmitters mitigates the latter alignment issue. Nonetheless, polar transmitters suffer from an additional issue that is related to their nonlinear conversion of in-phase and quadrature-phase signals into the amplitude and phase representation. Therefore, the polar RF transmitters are not able to manage very large baseband bandwidth of the most stringent communication standards, therefore, reusing I/Q modulators based on digitally intensive implementation appears to be a reasonable approach to resolve this issue. The digital I/Q RF transmitters, however, suffer again from inadequate power efficiency. Moreover, the combination of in-phase and quadrature phase paths must be orthogonal to produce an undistorted-upconverted-modulated RF signal.

In **Chapter 3**, a novel all-digital I/Q RF modulator is described. Employing an upconverting RF clock with a 25% duty cycle ensures the orthogonal summation of I_{path} and Q_{path}, which avoids nonlinear signal distortion. It was clarified that electric summing of I and Q digital unit array switches is the most appropriate I/Q orthogonal summation approach. Moreover, to address all four quadrants of the constellation diagram, the differential quadrature upconverting RF clocks must be utilized. In addition, it was explained that employing switches instead of utilizing current sources leads to superior noise performance of the all-digital I/Q transmitter.

In **Chapter 4**, a novel 2×3-bit all-digital I/Q (Cartesian) RF transmit modulator is implemented which operates as an RF-DAC. The modulator performs based on the concept of orthogonal summing, which is introduced and elaborated in Chapter 3. It is based on a time-division duplexing (TDD) manner of an orthogonal I/Q addition. By employing this method, a very simple and compact design featuring high-output power, power-efficiency and low-EVM has been realized. The resolution of the experimental RF-DAC presented in this work is only 3-bit (including one sign bit), but it will be demonstrated in the following chapters that the resolution can be increased to 8–12 bits in an unequivocal manner for utilization in multi-standard wireless applications.

In **Chapter 5**, the system design considerations of the proposed high-resolution, wideband all-digital I/Q RF-DAC are discussed. It is demonstrated that the upsampling clock frequency (f_{CKR}), DRAC resolution (N_b), and memory length (l_{mem}) are three important parameters that affect the dynamic performance of the proposed RF-DAC. Based on system level simulation results and the limitation in implementing the RF-DAC test-chip, they are designated as f_{CKR}=300 MHz, N_b=12 bit, and l_{mem}=8 k-word. The effect of these parameters on the in-band as well as out-of-band performance of RF-DAC are investigated. It is concluded that exploiting 13 bits of resolution for quadrature baseband signals is sufficient to meet the most stringent communication requirements.

In **Chapter 6**, the theory and the design procedure of an innovative, differential, orthog-

onal power combining network, which is employed in the proposed all-digital modulator, is thoroughly explained. It is demonstrated that, in order to maintain an orthogonal operation between the in-phase and quadrature-phase paths, the effect of the power combiner on the in-phase and quadrature-phase paths must be considered, otherwise, the linear summation will not occur. As a result, the EVM and linearity performance will diminish. The power combiner consists of a transformer balun as well as its related programmable primary and secondary shunt capacitors. In order to achieve high efficiency at full power of operation, a class-E type matching network is adopted and subsequently modified in order to obtain a minimum modulation error. A switchable cascode structure is exploited to mitigate a reliability issue as well as to perform a mixer operation. Moreover, utilizing a switchable cascode structure also improves the isolation between quadrature paths. Furthermore, it is explained that the power combiner efficiency is primarily related to the transformer balun efficiency. A procedure is introduced in order to design an efficient, compact balun transformer. Also, it is explained that the RF-DAC operates as a class-B power amplifier at the power back-off levels. As a result, its performance in the power back-off region is lowered.

In **Chapter 7**, the implemented wideband, 2×13-bit I/Q RF-DAC-based all-digital modulator realized in 65-nm CMOS is presented. Employing the orthogonal I/Q combining approach which is proposed in Chapter 3 guarantees the isolation between in-phase and quadrature-phase paths. The $4\times f_0$ off-chip single-ended clock is converted to a differential version employing an on-chip transformer. The wide swing, low phase noise, high-speed dividers are incorporated to translate the $4\times f_0$ differential clock to the fundamental frequency of f_0. In the meantime, the complementary quadrature sign bit is used to address four quadrants of the related constellation diagram. The 25% differential quadrature clocks are generated using logic-AND operation between $2\times f_0$ differential clock and f_0 differential quadrature clocks. The 12-bit DRAC is implemented employing a segmentation approach, which consists of 256 MSB and 16 LSB thermometer unit cells. The layout arrangement of the DRAC unit cell proves to be very crucial. It was concluded that the vertical layout would be the most appropriate selection. The LO leakage and I/Q image rejection technique as well as two DPD memoryless techniques of AM-AM/AM-PM and constellation mapping are introduced, which will be extensively utilized in the measurement segment.

In **Chapter 8**, the high-resolution wideband 2×13-bit all-digital I/Q transmitter, which was introduced in Chapter 7, is thoroughly measured. First, the chip is tested in continuous-wave mode operation. It is demonstrated that, with a 1.3 V supply and, of course, an on-chip power combiner, the RF-DAC chip generates more than 21 dBm RF output power within a frequency range of 1.36–2.51 GHz. The peak RF output power, overall system, and drain energy efficiencies of the modulator are 22.8 dBm, 34%, and 42%, respectively. The measured static noise floor is below -160 dBc/Hz. The digital I/Q RF modulator demonstrates an IQ image rejection and LO leakage of -65 dBc and -68 dBc, respectively. The RF-DAC could be linearized employing either of the two digital predistortion (DPD) approaches: memoryless polynomial or a lookup table. Its linearity is examined utilizing 4/16/64/256/1024-QAM

baseband signals while their related modulation bandwidth can be as high as 154 MHz. Using AM-AM/AM-PM DPD improves the linearity by more than 25 dB while the measured EVM is better than -28 dB. Moreover, the constellation-mapping DPD is applied to the RF-DAC which improves linearity by more than 19 dB. These numbers indicate that this innovative concept is a viable option for the next generations of multi-band/multi-standard transmitters. The realized demonstrator can perform as an energy-efficient RF-DAC in a stand-alone digital transmitter directly (e.g., for WLAN) or as a pre-driver for high-power basestation PAs.

Chapter 9 draws the conclusions of the this thesis work and provides recommendations for future research and directions in the field of all-digital RF transmitters for wireless communication applications.

Samenvatting

[1]Door de noodzaak om consumenten elektronica goedkoop te maken, is een migratie naar een geavanceerde nano-schaal CMOS technologie, welke primair voor snelle en laag-vermogens digitale schakelingen by een lage voedingsspanning is gemaakt, noodzakelijk. Dit zorgt ervoor dat RF zendontvangers meer en meer digitale circuits gaan uitbuiten. Deze basis eigenschappen van CMOS schijnen het ontwerp van draadloze function in de richting van het digitale domein te dwingen, waar transistors meer als schakelaar worden gebruikt dan als stroombron. In het laatste decennium is enn ontzagwekkende inspanning gedaan in de richting van het implementeren van volledig digitaal of digitaal intensieve RF zenders waarin zender ontwerpen volledig in het digitale domein zijn gedaan vanaf basisband tot en met de voorversterkers. In het kader van deze digitalisatie wordt de RF modulator als meest kritieke onderdeel van de zender gezien, aangezien deze zich het dichts bij de antenne bevindt en de digitale basisband modulatie samples omzet in een RF golfvorm. Dit kan polair, Cartesisch (I/Q) of als een outphasing topologie geimplementeerd worden. Voor signalen met grote bandbreedte zijn Cartesische modulators bewezen als de meest geschikte keus, dankzij de directe *lineaire* optelling van de in-fase (I) en kwadratuur (Q) component, waardoor expansie van de benodigde bandbreedte wordt vermeden. Aangezien de effectieve resolutie van de modulatie-samples het meest belangrijk is, aangezien dit direct het mogelijke dynamisch bereik, lineariteit, "error vector magnitude" (EVM), ruisvloer en het uitzenden van componenten buiten de band bepaalt, stelt dit proefschrift een breedbandige, hoge resolutie, volledig digitaal, *orthogonale* I/Q radio frequente digitaal naar analoog modulator (RF-DAC) voor.

Hoofdstuk 1 geeft een compact overzicht over conventionele RF radio componenten. Er word bediscussieerd dat hedendaagse RF zendontvangers multi-mode/multi-band com-

[1]Mijn hartelijke dank gaat uit naar de heren K. Buisman, M. Pelk en M. Stoopman van de Technische Universiteit Delft. De heer Buisman heeft zowel de samenvatting als het stellingen van dit proefschrift vertaald in het Nederlands. De heer Pelk heeft de Nederlandse versie van de samenvatting en het stellingen bijgewerkt. De heer Stoopman heeft ook verder het stellingen bijgewerkt.

municatie richtlijnen moeten ondersteunen, zoals Wi-Fi, Bluetooth en de Fourth Generation (4G) van 3GPP voor draadloze telefoons.

In **Hoofdstuk 2**, worden vier typen van RF zender architecturen kort beschreven. De analoge I/Q modulatoren zijn de meest eenvoudige en meest toegepaste RF zenders. Deze worden later vervangen door hun analoge polaire tegenhangers, vanwege hun lage vermogens efficientie en ruis gedrag. Daar staat tegenover dat in het analoge deel van polaire RF zenders de amplitude en fase signalen gesynchroniseerd moeten zijn aangezien anders groei van ongewenste spectrale componenten (spectral regrowth) onvermijdelijk is. Bovendien hebben polaire zenders problemen die gerelateerd zijn aan de niet-lineaire omzetting van de in-fase en kwadratuur componenten in de amplitude/fase representatie. Daarom zijn polaire RF zenders niet in staat om zeer grote basisband bandbreedte van de meest strenge communicatie richtlijnen te verwerken. Daarom schijnt het hergebruik van I/Q modulatoren gebaseerd op digitaal intensieve implementaties een redelijke aanpak om dit probleem aan te pakken. Daarnaast moet de combinatie van een in-fase en kwadratuur paden orthogonaal zijn om een niet verstoord, gemoduleerd, omhoog geconverteerd RF signaal te produceren.

In **Hoofdstuk 3**, is een nieuwe volledig digitale I/Q RF modulator beschreven.Door een omhoog converterende RF klok met 25% verhouding tussen hoog en laag kan de optelling van I en Q orthogonaal gehouden worden, waardoor niet-lineaire verstoring voorkomen wordt. Er word duidelijk gemaakt dat de elektrische optelling van de I en Q componenten met een reeks van digitale schakel eenheden het meest geschikt is. Daarnaast, om alle kwadranten van de constellatie te bereiken, moet een omhoog converterende klok gebruikt worden, welke differentieel en in kwadratuur gebruikt wordt. Verder werd uitgelegd dat het gebruik van een schakelaar tot betere ruis prestaties leidt dan het gebruik van stroombronnen voor een volledig digitale I/Q zender.

In **Hoofdstuk 4**, is een nieuwe 2×3 bit volledig digitale I/Q (Cartesisch) RF zend modulator geimplementeerd welke werkt als RF-DAC. De modulator maakt gebruik van een orthogonale optelling, welke in Hoofdstuk 3 is geintroduceerd. Het is gebaseerd op een tijd-domain duplexing (TDD) methode voor de optelling. Door het gebruiken van deze methode is een eenvoudig, compact ontwerp gemaakt, met hoog uitgangsvermogen, vermogens efficient en lage verstoring (EVM). De resolutie van de experimentele RF-DAC is slechts 3 bit (inclusief een bit die het teken aangeeft), maar in de hierop volgende hoofdstukken wordt gedemonstreerd dat de resulotie onmiskenbaar verhoogd kan worden naar 8-12 bits, voor gebruik in multi-standard draadloze applicaties.

In **Hoofdstuk 5**, worden de systeem ontwerp eisen van de voorgestelde hoge-resolutie, grote bandbreedte volledig digitale I/Q RF-DAC bediscussieerd. Er is aangetoond dat de omhoog sampling klok frequentie (f_{CKR}), DRAC resolutie (N_b), en geheugenlengte (l_{mem}) drie belangrijke parameters zijn, die het dynamische gedrag van de voorgestelde RF-DAC beinvloeden. Gebaseerd op simulaties op de systeem niveau is de RF-DAC testchip geimplementeerd, deze zijn f_{CKR}=300 MHz, N_b=12 bits, en l_{mem}=8 k-word. Het effect van deze parameters op de in-band alsmede buiten-de-band gedrag van de RF-DAC zijn bestudeerd.

Er is geconcludeerd dat het gebruik maken van 13 bits voor de kwadratuur basisband signalen voldoende is, zelfs voor de meest strikte eisen van communicatie voorschriften.

In **Hoofdstuk 6**, wordt op diepgaande de wijze theorie en het ontwerp van de innovatieve, differentiele, orthogonale vermogens samenvoeger uitgelegd, welke is gebruikt in de voorgestelde volledig digitale modulator. Er is aangetoond dat, om orthogonaal gedrag tussen de in-fase en kwadratuur-fase componenten te houden, de invloed van de vermogens samenvoeger hierin moet worden opgenomen, aangezien anders de optelling niet lineair zal zijn. Verder zal het EVM gedrag en de lineariteit afnemen. De vermogens samenvoeger bestaat uit een transformator "balun" alsmede programmeerbare condensatoren aan de primaire en secundaire zijde. Om hoge efficientie bij vol vermogen te bereiken wordt een klasse-E type aanpassingsnetwerk gebruikt en zodanig gedimensioneerd dat een bepaalde minimale fout wordt verkregen. Een schakelbare cascode wordt gebruikt om de betrouwbaarheid te verhogen, alsmede om frequentie menging uit te voeren. Bovendien verhoogdt de cascode de isolatie tussen verschillende kwadratuur paden. Verder is uitgelegd dat de efficiency van de vermogens samenvoeger direct gerelateerd is aan de efficientie van de balun. Een procedure is geintroduceerd om een efficiente compacte balun te ontwerpen. Ook is uitgelegd dat de RF-DAC als klasse-B versterker werkt als het uitgangsvermogen verminderd wordt. Als resultaat dat de prestaties iets afnemen voor lagere uitgangsvermogens.

In **Hoofdstuk 7**, is de geimplementeerde breedbandige 2×13 bit I/Q volledig digitale RF-DAC gepresenteerd, gerealiseerd in 65 nm CMOS. Het gebruik van de othogonale I/Q optelling, welke geintroduceerd is in Hoofdstuk 3, garandeert de isolatie tussen de in-fase en kwadratuur-fase paden. De $4\times f_0$ klok, welke van buiten het IC aangeboden wordt, is geconverteerd in een differentiele klok met gebruik van een transformator op het IC. De snelle delers met grote zwaai en lage faseruis, welke de $4\times f_0$ naar de fundamentele frequentie f_0 delen, zijn gerealiseerd op het IC. Tegelijkertijd zorgt het aanvullende bit dat het teken aangeeft ervoor dat alle vier kwadranten bereikt kunnen worden. De 25% differentiele kwadratuur klok is gemaakt met behulp van AND-logica tussen de $4\times f_0$ en f_0 differentiele kwadratuur klok. De 12 bit DRAC is geimplementeerd in een gesegmenteerde aanpak, welke bestaat uit 256 MSB en 16 LSB thermometer eenheidscellen. De positionering van de DRAC eenheidscel is cruciaal. Er was geconcludeerd dat een verticale plaatsing het meest geschikt is. Het LO lek en de I/Q spiegelonderdrukkings techniek, zoals als twee geheugenloze DPD technieken, namelijk AM-AM/AM-PM en een afbeeldingstechniek op het constellatie diagram zijn geintroduceerd, welke veelvuldig gebruikt zullen worden in het meet gedeelte van dit proefschrift.

In **Hoofdstuk 8**, is de hoge resolutie breedbandige 2×13 bit volledige digitale I/Q zender, welke in Hoofdstuk 7 geintroduceerd is, uitvoerig gemeten. Eerst is de chip getest in de continue draaggolf mode. Er is gedemonstreerd dat met een 1.3 V voeding en een op de chip gerealiseerde vermogens samenvoeger, de RF-DAC chip meer dan 21 dBm RP vermogen binnen een frequentie bereik van 1.36-2.51 GHz kan realiseren. Het hoogste uitgangsvermogen, systeem efficientie en drain efficientie van de modulator zijn respectievelijk 22.8 dBm,

34% en 42%. De gemeten statische ruisvloer is lager dan -160 dBc/Hz. De digitale I/Q RF modulator heeft een IQ spiegelonderdrukking van -65 dBc en een LO lek van -68 dBc. De RF-DAC kan gelineariseerd worden met een van de volgende twee voor-verstorings (DPD) methodes: een polynoom zonder geheugen of een opzoek tabel. Zijn lineariteit is onderzocht met 4/16/64/256/1024-QAM basisband signalen met een bandbreedte van maar liefst 154 MHz. Het gebruik van een AM-AM/AM-PM DPD verbetert de lineariteit met meer dan 25 dB terwijl de gemeten EVM beter is dan -28 dB. Daarnaast is de afbeeldingsmethode van het constellatie diagram gebruikt samen met de RF-DAC, welke de lineariteit met meer dan 19 dB verbeterde. Deze getallen laten zien dat dit innovatieve concept een geschikte keuze is voor nieuwe generaties multi-band/multi-standaard zenders. Het gerealiseerde prototype kan als energie efficiente RF-DAC direct in een autonome digitale zender (e.g. voor WLAN) of als voorversterker voor een hoog vermogens basisstation RF versterkers toegepast worden.

Hoofdstuk 9 worden de conclusies getrokken en worden aanbevelingen gedaan met betrekking tot toekomstig onderzoek, alsmede richtingen in het veld van geheel digitale RF zenders voor draadloze telecommunicatie toepassingen.

List of Acronyms

List of Figures

List of Tables

Acknowledgments

[1] After laboring for approximately 72 months, it is my great pleasure to compose this letter of appreciation. Three outstanding gentlemen have facilitated this course of my life.

First and foremost, Professor Leo de Vreede. Leo, I want to convoy my deepest gratitude to you. It is beyond my ability to explain your role in my life, professionally as well as personally, during the past six years. You admitted me as your PhD student twice. Without your kindness and support, I would not be in the position that I am today. In addition to learning a considerable number of things from you in microwave engineering, you are a true gentleman. It is impossible for me to reiterate all of those things that you have done for me, however, one remarkable example is, during the last year RFIC where you kindly presented our work, you mentioned my name in at least 30 instances. I was under your direct supervision for the first two and half years of my PhD and, in my opinion, we have done a very nice job in designing hybrid class-B/class-J* power devices. It is also worth mentioning the NXP semiconductor which has supported my PhD Project. I must additionally send my gratitude to Professor Rik Jos and Dr. Fred van Rijs. The concept in support of the hybrid class-B/class-J* LDMOS power devices has primarily been proposed by Fred, Rik, and Leo as well. Leo, I am also very grateful to you for affording this opportunity to work with my, then PhD promoter Professor Robert Bogdan Staszewski.

Second, I am very grateful to Professor John Long. As head of the group, you kindly accepted me as a PhD student. During the past six years, you supported me extensively. I remember that the very first official person I met in TU-Delft on the 25^{th} of April 2008, my interview date, was you. I was lost in the 18^{th} floor corridor when you approached me and stated, "You must be Morteza. Leo is waiting for you in his office. I will walk with you and introduce you to him." Then before I began the presentation, you said to me, " Relax. We have accepted you." To be honest, that was a huge relief to me. Moreover, in my two tape-out phases, you were always there and you generously support me. You are a great

[1]Courtesy of Jenny Hill from American Pen. All of this thesis, including this letter has been proof-read by her.

advisor, and it is my honor to be a PhD student in your group.

Last, but not least, I am indebted to my PhD promoter, my officemate, and my friend, Professor Robert Bogdan Staszewski. It is my great and true honor to be your first PhD student. I remember that I first met you in the Dimes lab while I was measuring three-way Doherty power amplifier following your presentation to our group . I must add that I knew about you from 2004-2005 when the ADPLL concept broke in to the academic world. My first impression of you was that this gentleman was so positive. Later, Leo informed me that you were about to join our group, and he suggested me to work directly with you. I believe, I began to work with you gradually beginning in September 2009 and entirely from June 2010. Bogdan, I must confess that I was really amazed with your crazy ideas, and it is no secret that the time-duplexing division I/Q RF-DAC, which is the primary idea of this dissertation, is your invention. I am very grateful to you for allowing me to work on it. In the beginning, this concept was not believed to be feasible even with in our own group. Now, after approximately four years later, in my opinion, it is being accepted and the people in industry as well as in the academic environment have begun to appreciate this idea. Bogdan, I have learned innumerable things from you professionally and personally. I will not forget how you motivated me to write papers, especially the RFIT paper and its subsequent TMTT paper. I believe, those two papers significantly influenced my PhD and were my PhD turning point. You are a courageous gentleman and, with your optimistic view, we have already won the Valorisation Grant phase 1/2. In this context, I want to acknowledge Dutch Technology Foundation (STW) Valorisation Grant phase-2 for supporting the past one and half years of my research in TU-Delft. I also want to acknowledge your wife, Sunisa, who was always very kind to me and provided considerable support.

My appreciation is also extended to my PhD committee members, Professor van Vliet, Professor Wambacq, Professor Heinen, Professor Baltus, and Professor Makinwa. Thank you for reviewing my PhD thesis and providing insightful comments in order to improve this dissertation.

I would like to express our gratitude to Rik Jos, Fred van Rijs, John Gajadharsing, Mark van der Heijden, Robin Wesson, Vittorio Cuoco, Edmond Neo, Jawad Qureshi, and Mustafa Acar from NXP Semiconductors. Moreover, I also would like to appreciate Coen van Bergen from Rohde & Schwarz for his measurement support.

During my PhD, I was so fortunate to interact with many experts at our university. First, Atef Akhnoukh, who significantly supported me during the crucial tape-out phases as well as in the testing phase at the measurement lab. Atef, you are a very kind, generous and, most importantly, patient gentleman. Second, the ever-amazing Wil Straver. Wil, without you, my chips would definitely not work. You taught me many things and were always nice to me. You did not deny my requests which were not even in your professional responsibilities. All of the chip and board pictures of this thesis are taken by you. Thank you very much. Third, Ali Kaichouhi , who supported me extensively during the measurement phase. Ali, you are also a very nice person who was always willing to help me. Fourth, Loek

van Schie, who also assisted me during the measurement phase. Loek, I will not forget your help in creating a suitable screw for my bed. I also should acknowledge our amazing software administrator, Antoon Frehe. Without you, none of my simulations and tape-outs would have not been realized. You were also always kind to me. At the beginning of my PhD, Marysia Lagendijk-Korzeniewski, the Dimes secretary, helped me considerably for which I am thankful. Moreover, Miranda Karsdorp from the HR department also facilitated my move to The Netherlands. I am also grateful to her.

Our beloved group secretery, Marion de Vlieger, is always very helpful and kind to me. Thanks very much, Marion, for smoothly arranging all of the things that I am continuously requesting from you.

The other Professors of our group including Professor Marco Spirito, my friend, Professor Behzad Rejaie, Professor Wouter Serdijn, and Professor Chris Verhoeven, Thijmen Hamoen, Bert Belzer as well as Professor Edoardo Charbon thank you very much for your kindness and support, and I apologize if I ever bothered you.

In my PhD stint, I was very fortuitous to benefit from a number of great friends and colleagues. First and foremost, I want to acknowledge Koen Buisman. Koen, you are not only my first friend and officemate but also helped me substantially. All of my papers were proof-read by you, and you always welcomed my requests. Thank you very much for all of the support and kindness. Mauro Marchetti and David Calvillo Cortes, my friends and officemates. I am very grateful for both of you. Mauro, I am grateful to you for helping me to measure the LDMOS devices with your amazing load-pull setup. You sat with me and spent an immeasurable amount of time in order to achieve the best results. David, Thank you very much for all technical discussions including DPD process. It is also worth mentioning my other Italian friend, Michele Squillante. Michele, you are a very skillful, patient, and kind friend. Thank you very much.

My appreciation is also forwarded to the ever-amazing Marco Pelk. Marco, I have learned many things from you. You taught me how to efficiently utilize the software and hardware during the measurement process and so many things during the three-way Doherty testing phase. Afterward, you taught me how to design a board in ADS. Thank you very much for all your support. I should also mention Jawad Qureshi and Edmond Neo. I learned much from Jawad during the three-way Doherty measurement phase. Thank you very much for supporting me and always being very kind to me. I should acknowledge Cong Huang and Rui Hou as well. Thank you very much to both of you for the support and kindness. Rui, my RFIC paper was also proof-read by you. Moreover, I should send my thankfulness to Gennaro Gentile, Luca Galatro, and Ajay Kumar. Thank you all for your kindness.

In addition, I must send my gratitude to my friends and colleagues on the 18^{th} floor. Mina Danesh, I am very grateful of you. I have learned a lot from you, especially the design of a transformer as well as the PCB board design. Chutham (June) Sawigun and Wanghua Wu whom I lived with for two months. You are my kind friends along with Nitz Saputra, Yi Zhao, Akshay Visweswaran, Imran Bashir, Yanyu Jin, Leonardo Vera, Wei

Liat Chan, Sharon Malevsky, Wu Chi Wing, Coby Huang, Senad Hiseni, Mark Stoopman, Andre Mansano, Sumit Bagga, Zhirui Zong, Wannaya Ngamkham, Marijn van Dongen, Cees Jeroen Bes, Yongjia Li, Yao Liu, Zhebin Hu, Xun Luo, Huizhen Qian, Ying Wu, Augusto Ximenes, Gerasimos Vlachogiannakis, Satoshi Malotaux, Wenlong Jiang, Sandro Binsfeld Ferreira, Duan Zhao and many others I may have forgotten. Thank you all very much for your friendship and support.

My appreciation is also forwarded to George Voicu and Professor S. Cotofana for their help and support.

My fellow Iranian friends on the 18^{th} floor: Masoud Babaie and Mina Shahmohammandi. Although you entered our group later than the others, our friendship began in 2004-2005 when I was a master student at the University of Tehran. I am grateful to both of you. Masoud, thank you very much for such a great friendship. I always enjoy talking with you professionally and personally. Armin Tavakol, Milad Mehrpoo, and Bahar Barati, thank you very much for support and kindness. Armin, my friend, I always enjoy talking with you. Milad and Bahar thank you very much for such a great friendship.

Amir Khan Ahmadi Mehr, thank you very much for great friendship and technical discussion. Massoud Tohidian, Iman Madadi, Mohsen Hashemi, and, last but not least, the genius Professor Reza Lotfi whereby our friendship dates back to 2003. Massoud thank you very much for technical help during measurement phase especially facilitating UART code. Reza, you are a great gentleman, and you have taught me so much and, when I arrived in The Netherlands you assisted me greatly.

My other fellow Iranian friends in TU-Delft: Kamran Souri and Sara Fekri. You are an amazing couple. Thank you very much for such a great friendship. Good luck in your life in the United States. Mahdi Kashmiri and Esmee van der hoeven, you are also my best friends and wish you the best in the next phase of your life. Thank you very much for your support and kindness during my time here in Delft. Saleh Heidari and Samira Amany also thank you very much for your support and kindness. The ever-amazing Hooman Hoornahad, my great friend, thank you very much for your friendship. Good luck for your upcoming PhD defense. Kianoush Souri, Ali Fekri , Daniel Tajari-Mofrad, and Bahman Yousefzadeh, you are the best. Good luck in your life.

I would also to send my gratitude to my friends in Iran and around the world, especially, the genius Dr. Khashayar Salehi, my beloved friend. You have been my best friend for the last 16 years. Thank you very much for always pushing me towards my goals. Mahdi Khafaji, you are my best friend in Europe. Take care. The genius Dr. Vahid Vahidfar as well as Dr. Vahid majidzadeh, I miss both of you. Your are my best friends in Silicon Valley. Vahid Jan, I will not forget your friendship in Tehran as well as in Italy. You deserve to significant achievements in your life. I should acknowledge Bahman Tavassoli, Dr. Hossein Afshari, Dr. Bahman Kheradmand, Sepehr Khodadadi, Ata Seifi, Dr. Mohammad Shahmohamdi, Dr. Reza Ghaderi, Dr. Javad Vaziefehdan, Dr. Amir Amirabadi, Dr. Mohammad Moghadam, Dr. Pouya Hashemi, Professor Mohammad Yavari, Professor Hossein Shamsi, Shahram

Moradi, and Dr. Arash Majd as well. Last, but not least, Yarrollad Koolivand. Thank you very much, Yiri Joon, for such a great friendship. Good luck in your life.

I want to send my gratitude to two of my former teachers and advisors. Professor Omid Shoaei from the University of Tehran from who I learned analog integrated circuit and Professor Ali Fotowat Ahmadi from Sharif Institute of Technology who taught me RF integrated circuit. I am grateful to both of them and wish them the best in their careers and their personal life.

I want to send my gratitude to all prominent Iranian scholars who significantly motivated and inspired me including, Professor Ali Hajimiri, Professor Behzad Razavi, Professor Ali Niknejad, Professor Hossien Hashemi, Professor Ahmad Mirzaei, Dr. Hamid Rategh, Dr. Ahmad and Maryam Rofougaran, Dr. Hooman Darabi, Dr. Masoud Zargari, and Arya Behzad.

My PhD journey might not have begun without the enormous support from my family, especially my parents, sister, brother-in-law, my cousin, Amir, and my uncle, Hamid. With their love and support, my life transition from Tehran to Delft was so easy. Mom and Dad, I am indebted to you both.

In 2010, I married my wife, Haleh Bagheri. During the past four years, which were the most crucial period of my PhD, she was so patient, supportive and helpful. I want to send my deepest gratitude to her. Thanks very much, Haleh, for your love, understating my situation as well as late night work hours which sometimes lasted until midnight.

Finally, I would like to thank all members of my family in Iran, and around the world whom they were extensively supporting me in my PhD stint including: Baba Mehdi, Maman Noushin, Haleh, Sara, Mahmoud, Parsa, Baba joon, Maman joon, Freshteh joon, Baba Habib, Shahram, Fatemeh, Soheil, Sana, Siayna, Daei Nasser, Khaleh Jaleh, Daei mansour, Khaleh Roya, Leyla Khanoom, Daei Hamid, Manijeh Khanoom, Ali Joon, Noushin khanoom, Daei Farhad, Ameh Saeedeh, Sedigeh and Fatemeh, Mozhi, Kooroush, Amir, Neda, Soleyman, Marjan, Ali, Narges, Reza, Mohammad, Golnaz, Mahyar, Saeed, Maryam, Morvarid, Nima, Dina, Romina, Mohammad, Hassan who bought me all books that I need during my BS as well as MS studies, Taghi, Mozhdeh Khanoom, Reza, Ali, Khaleh joon Alavi, Khaleh joon Ensieh, Khaleh joon Morvarid, Khaleh joon Masoumeh, Leyla joon, Daei Mahmoud Goal, Hamid Jan, Haleh joon, Hossein Khan, Batool Khanoom, Masoud Khan, Nahid Khanoom, Bezrouz and Behzad, Alaleh, Ali Jan, Arash, Babaak, Bahar, Shahriar, Shirin, Yasmain, Hanna, Arvin, Alex, Alen, Sam, Brigitte, Rene, Khaleh Soheiyla, Khaleh Soossan, Aghaye Dalir, Arash, Siavash, Piruz, Khaleh Zohreh, Aghaye Fazeli, Abdi, Daei Jan, Faranak Khanoom, Reza Jan, Kamelia Khanoom, Alireza Jan, Nina, and Agha Mehdi.

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May 11, 2014
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