On-chip Temperature Compensation with a Reference Voltage Method for CMOS Image Sensors

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Abstract

This thesis presents a temperature-dependent reference control method to compensate for the temperature effect on CMOS image sensors from -40°C to 125°C. Recently, machine vision has been one of the most important applications for CMOS image sensors. However, the working environment and operation might generate large temperature variations and degrades the performance of CMOS image sensors. In this work, the temperature dependency of the distortion generated in the analog front-end is investigated. A mathematical model has been built to describe the relationship to its temperature dependency. Besides, a temperature-dependent reference control method with 16 different slopes is proposed. This method can control the working condition of the transistors and compensate for the change by reference current or voltage. Besides, the slope design can cover the external noise or mismatch and fulfill the compensation. Finally, it can compensate the signal distortion and prevent the settling error which could generate FPN while maintaining the noise performance. A SPICE simulation and post-simulation are performed to confirm the results of the design.

Key word: CMOS image sensor, temperature compensation, machine vision.

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This thesis is the toughest project I have ever worked on. I could never finish it without the help of others. It is my honor to know all these people.

Delft University of Technology Yu-Chieh Tai
November 21, 2022

"Next to the above is he who cultivates to the utmost the shoots of goodness in him. From those he can attain to the possession of sincerity. This sincerity becomes apparent. From being apparent, it becomes manifest. From being manifest, it becomes brilliant. Brilliant, it affects others. Affecting others, they are changed by it. Changed by it, they are transformed. It is only he who is possessed of the most complete sincerity that can exist on Earth, who can transform."

–*Zhongyong*

Chapter 1

Introduction and motivation

Recently, machine vision has been one of the most important applications for CMOS image sensors. Considering the working environment and operation of machine vision applications, the ambient temperature could change drastically and make the performance of the analog front end in sensors unstable. The images are distorted, making the sensors not reliable. This thesis is motivated by this phenomenon and addresses the problems with a temperature-dependent reference control method. The evaluation factors that are impacted by temperature change are explained and demonstrated with sample images. The proposed method can maintain the performance of CMOS image sensors over the operating temperature and, thus, prevent the distortion induced by the temperature effect.

Section1-1 presents a brief introduction to the recent developments of CMOS image sensors. The motivation and object of this project are presented in Section 1-2. This is followed by the impact of temperature on the image sensor and output images. Finally, the structure of the rest of the thesis is introduced.

1-1 Introduction to the recent developments of CMOS image sensors

In 2006, Sony published a CMOS image sensor structure with a combination of Correlated Double Sampling (CDS) and Digital Double Sampling (DDS) [1]. These operations suppress the noise in the analog and digital domains. After this research was published, this architecture became a common method for CMOS image sensors, and many applications emerged. This structure is widely adopted by many companies in portable devices, surveillance cameras, and digital cameras. These cameras are usually used for capturing images or videos for human eyes. The frame rate ranges from $30fps$ to $60fps$, and the resolution falls between $8M$ to $16M$. Asides from these applications, recently, machine vision is one of the most rapid-growing applications because the accuracy of machine vision has been improved [2]. Machine vision acquires the desired information about the real world through images, and the captured images are read by a machine. It is different from the traditional camera, which captures images for human eyes. The machine vision can be used in the remote control, event monitor, and object detection [3] [4] [5]. To increase efficiency, the frame rate of sensors for machine vision applications should be faster so the machine can have more data at the same time. It is also helpful for machines to shorten the response time. The frame rate for machine vision is higher than $300fps$. For example, a high speed is required for LiDAR to capture the object profile under fast-moving speed [6]. Machine vision also relies on high resolution and dynamic range to capture more details in images to increase accuracy. For example, image sensors in automotive require a wide dynamic range to capture the image in the dark or the tunnel where the contrast of light is strong [7]. These new applications and requirements keep motivating the development and research of high-performance CMOS image sensors.

1-2 Motivation and object of this project

For machine vision, the CMOS image sensors are used to capture the information in the real world; therefore, they are embedded with the machine, and the machine could be placed in different environments that humans cannot reach, such as space applications. These sensors should bear better resistance to the environment. For example, in space, the sensors are exposed to large temperature variations [8]. In addition, to fulfill the high frame rate and high resolution for CMOS image sensors, the Analog-to-Digital Converter (ADC) and the pixels require more current. Therefore, the sensors consume more power, and more heat is generated. The heat results in increasing the temperature, so the temperature could vary during operation. Both environmental and operational factors create a large temperature variation for sensors. As CMOS image sensors are designed and manufactured with a silicon process, the increasing heat impacts the performance of the analog front end and distorts the signal while it is transmitted from pixels to the output [9]. This degradation of image quality could cause wrong decisions in machine vision and deteriorate the accuracy of the machine's performance. To address this issue, research has been developed to investigate the temperature effect on image sensors. [10] tries to build a mathematical model to calibrate the effect of the temperature dependency of the dark current. However, with the recent improvement of the pixel structure, the noise from pixels has been reduced, and the noise from the analog front end has become important. Zimouche et al. [11] proposed a reference

voltage method and employed the temperature-invariant point of drain current to maintain the temperature stability of the logarithmic CMOS image sensor. Wang et al. [12] proposed a model to describe the temperature effect on the linearity of CMOS image sensors. However, none of them focuses on the temperature dependency of the complete readout chain and its impact.

This work aims to investigate the temperature dependency of the analog front end and addresses the issues with the temperature-dependent reference control method. With this design, we can control the operating region of transistors in the analog front and compensate for the temperature impact. Thus, the image quality can be maintained over the operating temperature.

1-3 Temperature impact on the readout chain in CMOS image sensors

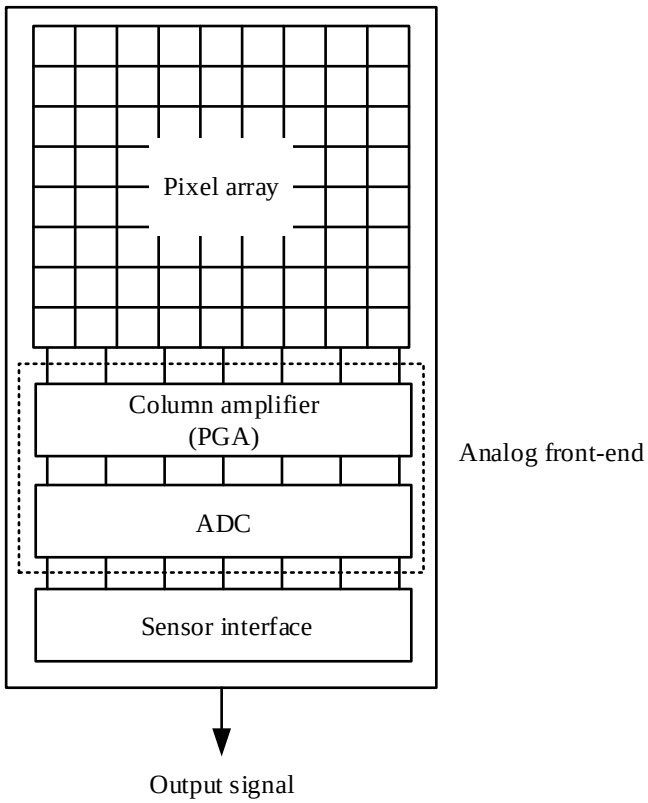

Figure 1-1: A general CMOS image sensor architecture

Fig. 1-1 shows the basic structure of a CMOS image sensor. The light is integrated and converted to a voltage signal by the photodiode. The signal is transmitted by the source follower in the pixel. Followed by the pixel array, the column-parallel Programmable Gain

Amplifier (PGA) is used to control the analog gain and amplify the signal. The ADC transfers the analog signal to digital code to the output. Once the signal is converted to digital code, it is not impacted by the temperature anymore. The source follower in the pixel array, PGAs, and ADCs are part of the analog front end or called the readout chain. The readout chain is sensitive to temperature because they are CMOS devices. The change in temperature impacts the performance of these blocks and thus the output images. Assuming an image sensor is used in automotive. During the movement of the car, the engine keeps working, and the ambient temperature increases. If the sensor is placed under the hood, the temperature of the sensor also increases. It generates some imperfections and degrades the machine vision's performance. According to [9], when temperature increases, the Fixed Pattern Noise (FPN), random noise, and dark current increase, and the gain of the source follower reduces. Fig. 1-2 shows an example of how these imperfections degrade the image.

(a) (b)

Figure 1-2: The simulation results of the example image (a) $15°C$ (b) $90°C$

(a) is the image at $15°C$. (b) is the image at $90°C$. This simulation is adapted from the experiment result in [9]. In [9], the main artifact that is enhanced by the increasing temperature is the FPN and the random noise. For the random noise, it increases by a factor of 2.3. For FPN, it increases by a factor of 4. The noise in this simulation is enhanced by a factor of 4 for demonstration. These strip lines in the images are generated by FPN. It is a fixed pattern and treated as an offset. The random noise includes thermal noise, flicker noise, and dark current shot noise, and they all have strong temperature dependencies. In [9], the total random noise increases almost 100% from $15°C$ to $90°C$. The reset noise, which is generated in the analog front end, increases by around 30%. In addition, these imperfections also deteriorate the evaluation factors of image sensors, such as Signal-to-Noise Ratio (SNR), Dynamic Range (DR), and nonuniformity [13]. Therefore, during driving, these imperfections could distort the image and reduce the accuracy of machine vision. It could result in the wrong decision and traffic accidents.

This work aims to address the temperature dependency of these distortions generated in the readout chain and maintain them at the same level over the operating temperature. We proposed a temperature-dependent reference control method to control the reference condition of transistors in the readout chain or signal range to compensate for the impact of temperatures. It can keep the bandwidth from 30% of variation to 5% and compensate for

the change in the gain of the source follower from 8% to less than 1%. It can reduce the risk of FPN and recover the signal distortion. This method does not require any external control and achieves compensation through its temperature dependency. Besides, the compensation is done in the analog domain, so it does not require post-image processing. With this method, the quality of output images and machine vision performance can be maintained.

1-4 Structure of the thesis

This thesis is composed of four different chapters. The first chapter describes the introduction and motivation of this project. The second chapter explains the temperature dependency of the distortions and proposed solutions. A detailed investigation of temperature impact, the temperature dependency model, and the design procedure of the countermeasures are placed in this chapter. The third chapter focuses on the transistor-level design along with the simulation results. The design procedure is explained, and the simulation results are discussed. Finally, future work and conclusions are made in the last chapter.

Chapter 2

Systematic level models and solutions

This chapter aims to analyze the temperature dependency of the three parameters, the temporal noise, the signal range distortion, and the settling error in the readout chain. The source follower, the PGA and the comparator in the ADC show a different temperature dependency of the temporal noise. The distortion can be impacted by the gain of the source follower. The settling error is caused by the change in the bandwidth. Therefore, the mathematical models are built first to describe the temperature dependency of the temporal noise, gain, and bandwidth. These models are deduced from the basic parameters of CMOS devices and simplified to the functions of temperature. In addition, the joint effect of the reference condition of the transistor and temperature are discussed. Combining two effects, the temperature-dependent reference control method is proposed to maintain the performance and compensate for these distortions. This method can prevent signal distortion and control the bandwidth while maintaining the noise performance.

In Section2-1, the basic theory for the random noise, the FPN, and the distortion of the signal range is explained. The temperature dependency in these three imperfections and their noise models are developed for analysis in Section 2-2. The reference condition of these three imperfections is explained in Section 2-3. The proposed solution to the issue and the final specifications are revealed in Section 2-4.

Notice that the image sensor structure in this project, including pixels, PGAs, and ADCs, are designed by [14]. The author did not implement the sensor architecture in this project. Only the noise analysis of the sensor architecture is open for discussion. The author only focuses on the design of reference generator blocks. The parameters for noise simulation of the source follower and the PGA are listed in Appendix A-1.

2-1 Analysis of the imperfection in the readout chain

In the example of Fig. 1-2, these imperfections originate from the readout chain and could be created by different sources altogether. They are generated by the change in the transistors' parameters. Here we explain the connection between the imperfections and their origins.

2-1-1 Temporal noise

Temporal noise generated in the readout chain is composed of thermal noise and flicker noise of the transistors. In the readout chain, noise is originated from the source follower, the PGA, and the ADC.

Fig. 2-1 shows the block diagram of the noise source in the readout chain. Assume that the analog gain of the PGA and the source follower's gain are one. The total noise power of the readout chain without CDS can be written as

$$\begin{aligned}\overline{V^2_{n,read,total}}(T) &= \overline{V^2_{n,res}} + \overline{V^2_{n,sig}} + 2\overline{V^2_{n,PGA}} + 2\overline{V^2_{n,comp}} \\ &\approx \overline{V^2_{n,totaloff}} + T_{Cn,total} \cdot T\end{aligned} \tag{2-1}$$

Where $\overline{V^2_{n,read,total}}$ is the total noise power generated in the readout chain, including the noise power from the pixel. $\overline{V^2_{n,res}}$ and $\overline{V^2_{n,sig}}$ are the noise power from the source follower in the pixel , $T_{Cn,total}$ is the temperature constant for the total noise power, and $\overline{V^2_{n,totaloff}}$ is the noise power at $-40°C$. Here the total noise power is approximated to the first-order polynomial equation as a function of temperature. Temporal noise increases with temperature and degrades the output image quality.

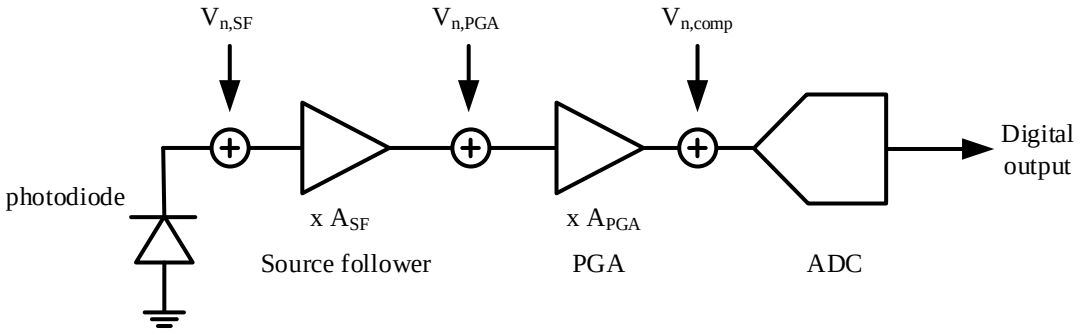

Figure 2-1: The block diagram of noise sources in the complete readout chain

There are two kinds of the pixel structure, 4T pixel and 3T pixel (see Fig. 2-2). The pinned photodiode is used in 4T pixels (Fig. 2-2 (a)). The noise from the photodiode is completely removed because the $n-$ region is completely depleted at the reset phase. In addition, CDS can effectively suppress the reset noise and flicker noise [15]. Therefore, the

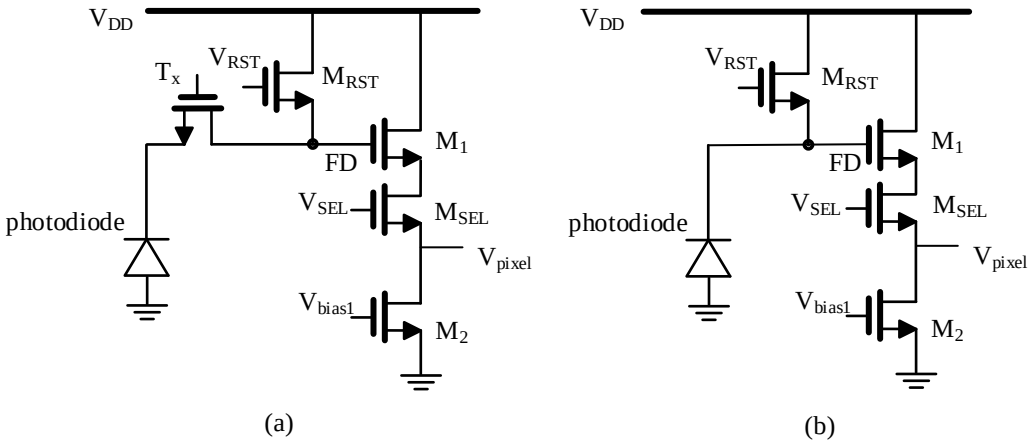

Figure 2-2: The pixel structure (a) 4T pixel (b) 3T pixel

source follower is the main noise source in the 4T pixel. The input-referred noise power of the source follower can be written as

$$P_{in,n,SF} = \int_0^{f3dB} \left(4kT\gamma \left[\frac{1}{g_{m1}}\left(1+\frac{g_{m2}}{g_{m1}}\right)\right]\right) \cdot \frac{\pi}{2} df \tag{2-2}$$

Where $P_{in,n,SF}$ is the total input-referred noise power of the source follower, $f3dB$ is the noise bandwidth of the source follower, k is the Boltzmann constant, T is the temperature, γ is the channel length constant, f is the frequency, g_{m1} and g_{m2} are the transconductance of the transistor in Fig. 2-2 (a) or (b). The transconductance of M_1 and noise bandwidth are the most important factors in controlling the noise.

In the 3T pixel (Fig. 2-2 (b)), the reset noise can not be removed by CDS because the reset and sampling signal are sampled two times and have a weak correlation compared to the 4T pixel. The reset noise is composed of the kTC noise of the reset operation. It can be expressed as

$$\overline{V_{n,reset}^2} = \frac{kT}{C_{FD}} \tag{2-3}$$

Where $\overline{V_{n,reset}^2}$ is the noise power of the reset noise. C_{FD} is capacitance at floating diffusion node, FD in Fig. 2-2 (b). Therefore, compared to the 4T pixel, the 3T pixel has two noise sources, kTC noise and noise of the source follower, so its total temporal noise is higher than the 4T pixel.

The PGA used in this project is a simple OTA, shown in Fig. 2-3. The noise power of the PGA can be written as [16]

$$P_{in,n,PGA}(T) = \int_0^{f3dBPGA} 4kT\gamma \left[\frac{1}{g_{mM1}}\left(1+\frac{g_{mM3}}{g_{mM1}}\right)+\frac{1}{g_{mM2}}\left(1+\frac{g_{mM4}}{g_{mM2}}\right)\right] \cdot \frac{\pi}{2} df \tag{2-4}$$

Where $P_{in,n,PGA}(T)$ is the total input-referred noise power of the PGA at a certain temperature, g_{mM1-4} are the transconductance of the transistors in Fig. 2-3. The input transistors, M_1 and M_2, are the main noise sources in the PGA.

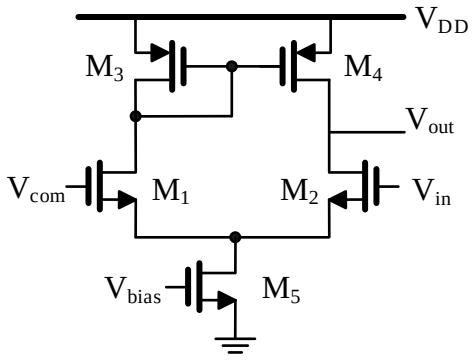

Figure 2-3: The structure of the PGA in this design

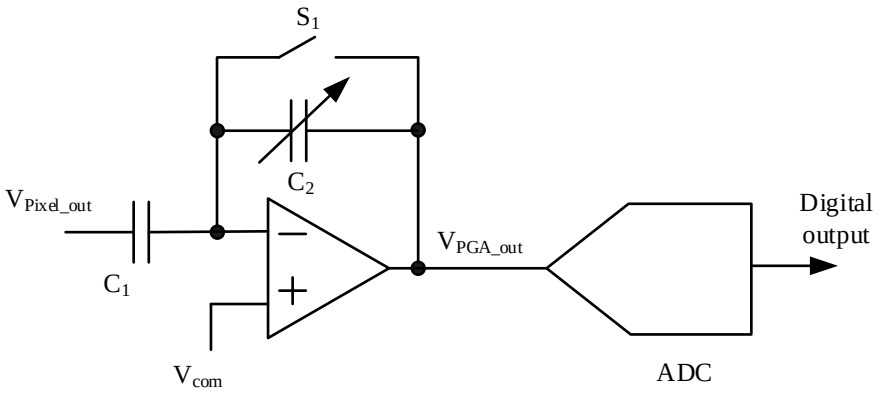

Figure 2-4: The connection of the PGA and the ADC in this project

A Successive-Approximation ADC (SAR ADC) and a clocked comparator are used in this project. A simplified connection is shown in Fig. 2-4. The noise of the comparator is more complicated as it is a linear time-varying system [17]. However, according to the conclusion in [17], it can be seen that the noise of the comparator is proportional to temperature. The switched capacitors of the ADC also generate kT/C noise. However, compared to other noise sources, the kT/C noise generated in ADC is small in this design and can be neglected.

2-1-2 Distortion of the signal

After the signal is integrated, it is converted from charge to a voltage signal. This signal passes the source follower and is multiplied by its gain A_{SF}. After the source follower, it is transmitted to the PGA and amplified again by its analog gain A_{PGA}, and then it is converted to digital code by the ADC. Therefore, if the two factors, A_{SF} and A_{PGA}, change, the signal also changes and is distorted. Besides, if the signal is amplified and exceeds the default signal

range in the ADC, the signal is lost and can not be converted to digital code correctly. The input and output signal can be written as

$$V_{out} = V_{sig} \cdot A_{SF} \cdot A_{analog} \tag{2-5}$$

Where V_{out} is the output signal of the sensor, V_{sig} is the input signal of the sensor, A_{SF} is the gain of the source follower, and A_{analog} is the system analog gain, which can be controlled by the PGA. Assume the gain of the PGA is large enough, and A_{analog} is set to one. We can see that the signal is mainly impacted by the gain of the source follower. The gain of the source follower can be written as Eq(2-6). For simplicity, the channel length modulation is ignored.

$$A_{SF} = \frac{g_m R_o}{1 + (g_m + g_{mb}) R_o} \tag{2-6}$$

Where A_{SF} is the gain of the source follower, R_{on} is the output resistance, and g_{mb} is the body effect parameter.

2-1-3 FPN

In the readout chain, FPN could be generated by the mismatch across pixels, source followers, PGAs, and ADCs. In addition, the settling error is also one of the noise sources of FPN. The variation between transistors generates an offset between source followers, column PGAs, and ADCs. Therefore, these difference appears as a straight light or in a specific pattern in the output images. In addition, the FPN generated by device variation can be calibrated by subtracting the image in the dark and under illumination in the digital domain or by a mathematical model [18].

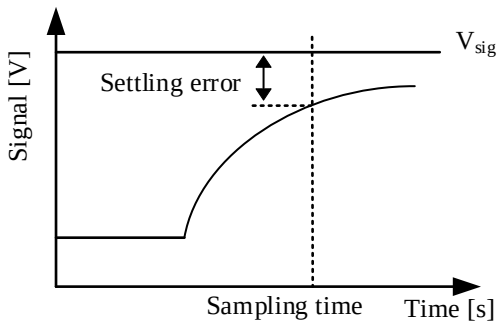

Figure 2-5: The settling error

The bandwidth of the PGA is decided by the settling time requirement of the system (see Fig. 2-5). If the bandwidth is not enough, a settling error is generated. If the ADC has a settling error, the ADC has a signal-dependent error. If the bandwidth has a mismatch between each column, this settling error becomes FPN. The settling error can be expressed as

$$error_{set} = e^{-t/\tau} \tag{2-7}$$

Where $error_{set}$ is the settling error, τ is a time constant, and t is the time. This error is dependent on the signal. Therefore, the error varies in each column if the sensor is illuminated with the polychromatic light source. This FPN cannot be calibrated by image processing as it changes with the signal. Therefore, in this work, we try to analyze and solve this issue.

2-2 Temperature effect analysis

2-2-1 Temperature dependency of the temporal noise

According to Eq (2-3), each component, such as the pixel, source follower, PGA, and comparator, has a different temperature dependency. Fig. 2-6 shows the temperature dependency of the noise in each block.

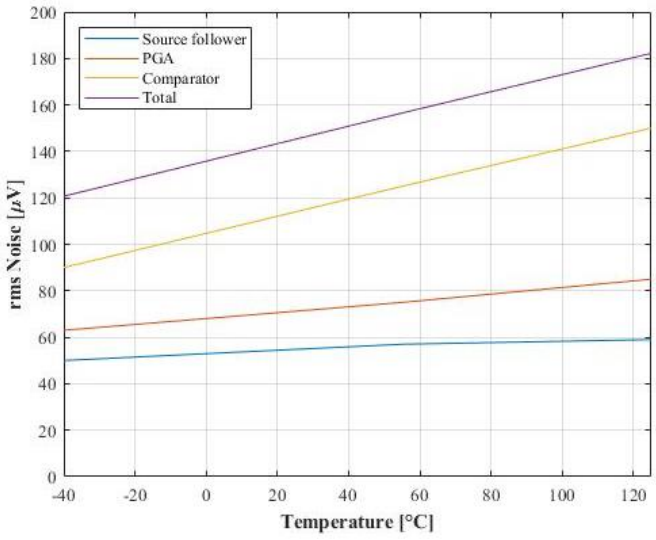

Figure 2-6: The total rms noise in each block as a function of temperature

In Eq(2-1), $T_{c,n,total}$ is the temperature constant of the total noise. It shows the temperature dependency of the total noise and can be expressed as

$$T_{c,n,total} = T_{c,n,SF} + T_{c,n,PGA} + T_{c,n,comp} \tag{2-8}$$

Where $T_{c,n,SF}$, $T_{c,n,PGA}$ and $T_{c,n,comp}$ are the temperature constant of the source follower, the PGA and the comparator. $T_{c,n,SF}$ is $6.7 \times 10^{-12} V^2/°C$, $T_{c,n,PGA}$ is $2 \times 10^{-11} V^2/°C$ and $T_{c,n,comp}$ is $8.7 \times 10^{-11} V^2/°C$. Among them, the comparator is the main noise source and the noise is proportional to the temperature, followed by the PGA and the source follower. The comparator noise here is estimated by static noise analysis. Comparing Eq(2-2) and(2-4), the temperature constant of the PGA is larger because it has more noise transistors, and both input transistors contribute to the noise. For the source follower, it has fewer transistors and only one input transistor. In addition, when the temperature increases, the transconductance

reduces in general. Therefore, as the temperature constant of the noise of the PGA is larger, the noise of the PGA increases more than the noise of the source follower.

2-2-2 Temperature dependency of the signal distortion

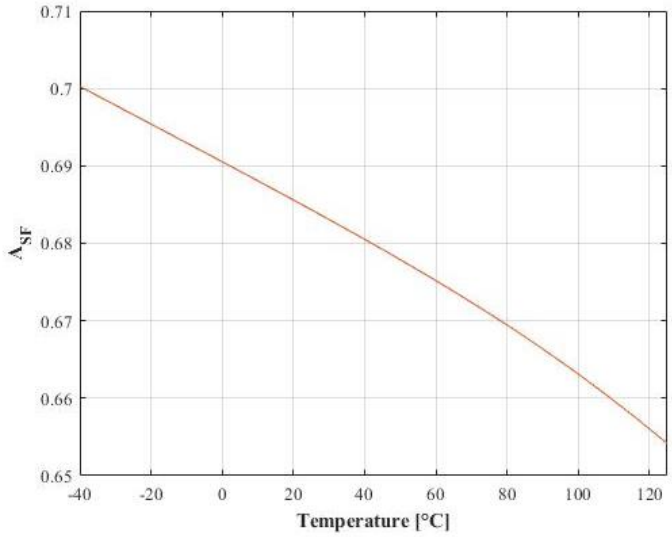

Figure 2-7: The gain of the source follower at different temperatures

The gain of the source follower changes with temperature because of the carrier mobility and the threshold voltage (see Fig. 2-7). The gain of a single source follower is expressed in Eq(2-6). The transconductance is one of the dominant terms to contribute to the temperature dependency of the gain. The transconductance of the body effect is temperature-independent. R_o is inverse-proportional to the drain current. The current source of the source follower copies the current from the reference generator. The core of this reference generator is a Band-Gap Reference (BGR). Therefore, the drain current is invariant with the temperature as it is converted from the BGR. When the temperature changes, the threshold voltage changes. However, as a feedback loop in the reference generator forces the output to follow the output voltage of the BGR, the current thus does not change with the temperature. The transconductance of a transistor can be written as

$$g_m = \sqrt{\frac{1}{2}(C_{ox}\mu W/L)I_D} \tag{2-9}$$

Where g_m is the transconductance of the transistor, C_{ox} is the oxide capacitance, I_D is the drain current, and μ is the carrier mobility of the electrons. For the transconductance, as the drain current, C_{ox}, W, and L are independent of the temperature, the mobility is the dominant parameter that contributes to the temperature dependency. The carrier mobility has a high-order temperature dependency and changes the gain of the source follower. As the temperature increases, carrier mobility reduces. When temperature increases, the electrons

scatter more, and the mobility reduces.

$$\mu(T) = T_0 \cdot (T/T_0)^{T_{C\mu}} \tag{2-10}$$

Where $\mu(T)$ is the mobility at a certain temperature, T_0 is the reference temperature, T is the certain temperature, and $T_{C\mu}$ is the temperature constant and is negative. This equation shows that carrier mobility reduces with increasing temperature [19]. As the μ reduces, the gain of the source follower reduces. Thus, the output signal changes with temperature. Fig. 2-7 shows the temperature dependency of the source follower's gain in this design.

2-2-3 Temperature dependency of the settling error

Here we assume the closed-loop gain of the PGA is one, so the bandwidth of the PGA can be written as

$$\omega_p = \frac{g_{m1,2}}{2\pi C_{out}} \tag{2-11}$$

Where ω_p is the angular frequency of the bandwidth, C_{out} is the total output capacitor, and $g_{m1,2}$ are the transconductances of the input transistor of the PGA. All the components are referred to Fig. 2-3. In Eq(2-11), the transconductance is the dominant term contributing to temperature dependency. C_{out} is insensitive to the temperature. It shows that the bandwidth is proportional to the transconductance, which decreases as temperature increases. As mentioned in Section 2-2-2, the reference current of the PGA is also managed by a BGR. Therefore, when the temperature increases, W, L, and I_D are fixed, and the transconductance decreases because the mobility reduces. Therefore, the bandwidth of the PGA is reduced. In particular, when the bandwidth decreases below the required bandwidth, the settling error increases, and this error will be present in the image. Fig. 2-8 shows the temperature dependency of the bandwidth of the PGA in this design. The bandwidth reduces as temperature increases.

2-3 Reference control and the temperature effect compensation

The signal is deteriorated by the increment of temporal noise, settling error, and distortion induced by the change in temperature. Since the transconductance of each component is the main reason for these three errors, changing the reference condition is helpful to minimize the errors described in the previous chapter. The reference control method and its impact on each component will be investigated in this chapter. As mentioned in the previous chapter, the noise contribution from the switched capacitor of the ADC is negligible. The comparator is biased by the clock signal instead of the analog reference generator, so its reference condition is independent of the reference generator. Therefore, the main discussion in this work is about the source follower and the PGA.

2-3-1 Reference condition of the temporal noise

From the previous research, the noise performance has been investigated, and the mathematical calculation is expressed as Eq(2-2) and Eq(2-4). Since the transconductance of the

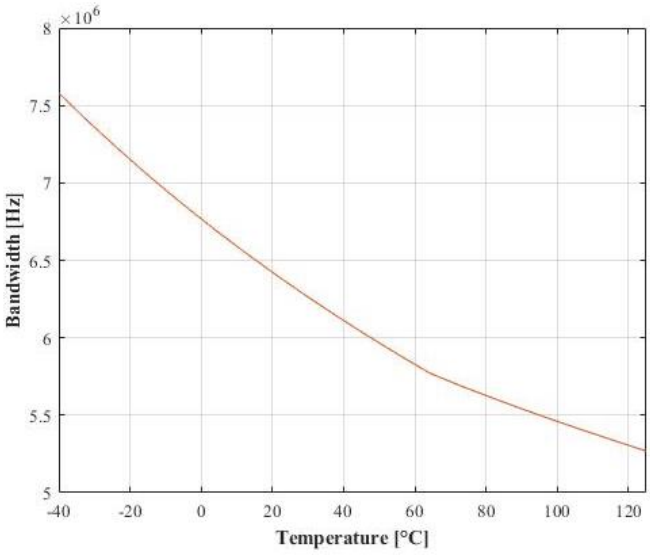

Figure 2-8: The temperature dependency of the bandwidth of the PGA

PGA and the source follower control this noise performance, assuming the gain of the source follower is one, this output-referred noise power calculation is rewritten as function of the reference current as

$$\begin{aligned} P_{out,n,SF} &= S_{out,n,SF} \cdot \frac{g_{m,PGA}}{2\pi C_{out}} \cdot \frac{\pi}{2} \\ &= \frac{\beta_1}{\sqrt{I_{D,SF}}} \cdot \frac{\sqrt{I_{D,PGA}}}{2\pi C_{out}} \end{aligned} \tag{2-12}$$

Where $P_{out,n,SF}$ is the total output-referred noise power of the source follower, $g_{m,PGA}$ is the transconductance of the input transistor of the PGA, and β_1 is the constant term which is invariant with a reference current, and $I_{D,SF}$ and $I_{D,PGA}$ are the reference currents for the source follower and the PGA. Eq(2-12) is simplified as the transconductance is directly proportional to the root square of the reference current. According to Eq(2-12) and the reference current terms, the output-referred noise reduces as the reference current of the source follower reduces and increases as the reference current of the PGA increases. When the reference current of the source follower increases, the transconductance increases. A larger transconductance reduces the output impedance and reduces the noise current and reference current ratio. Therefore, the noise reduces. For the PGA, the increasing reference current increases the bandwidth. When the bandwidth increases, more noise is integrated. Fig. 2-10 shows how the noise changes with the reference current of the source follower: if the current increases, the noise decreases. On the contrary, when the reference current of PGA (I_{DPGA}) increases, noise increases. In addition, as both reference currents are in root square, so the change of the noise is not linear.

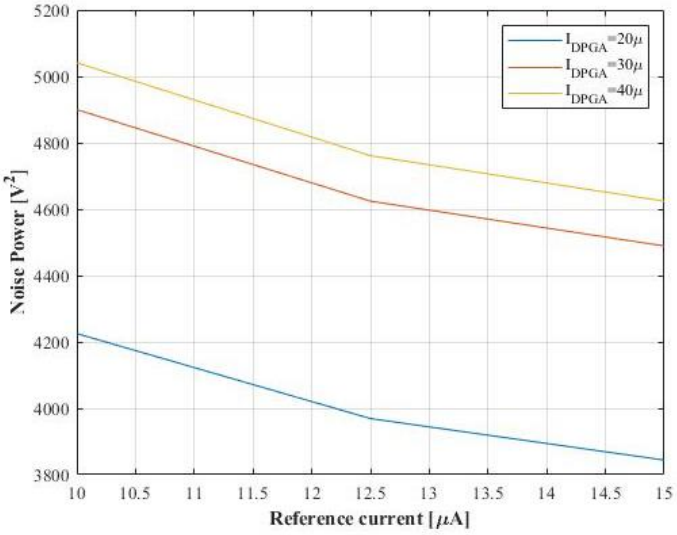

Figure 2-9: The noise power of the source follower under different reference currents

Subsequently, the output-referred noise power of the PGA can be expressed as

$$P_{out,n,PGA} = \alpha_3 \cdot g_{mPGA} \cdot \left(\frac{R_{out}}{1 + g_m R_{out}}\right)^2 \cdot \frac{g_{mPGA}}{2\pi C_{out}} \cdot \frac{\pi}{2} \tag{2-13}$$

Where $P_{out,n,PGA}$ is the noise power of the output-referred noise of the PGA, and α_3 is the constant that is invariant with the reference current. The $\frac{R_{out}}{1+g_m R_{out}}$ term in Eq(2-13) is generated by the negative feedback loop of the PGA. According to Eq(2-13), when the reference current increases, the transconductance increases. The negative feedback, however, forces the noise of the PGA to be maintained at the same level. Therefore, an increasing reference current can not effectively reduce the noise. However, because the gain of the PGA is small, the noise still reduces slightly when the reference increases. When the reference current increases, the transconductance increases as well. However, the output impedance of the PGA decreases faster, so the loop gain becomes weaker. Thus, the feedback can not force the noise to be maintained at the same level, and the noise reduces. Fig. 2-10 shows the rms noise of the PGA. When the reference current increases, the R_{out} reduces, so the noise starts to reduce.

For the PGA, increasing the reference current only slightly reduces the noise because the loop gain reduces. To achieve the temperature compensation, the temperature constant of the total noise should be zero, which can be derived by Eq(2-8)

$$T_{c,n,SF} + T_{c,n,PGA} + T_{c,n,comp} = 0$$

According to the simulation result in Section 2-2-1, assuming the reference current is the same for the PGA and only $T_{c,n,SF}$ is controllable, $T_{c,n,SF}$ should be 13 times larger to compensate for the temperature dependency according to the value of $T_{c,n,SF}$, $T_{c,n,PGA}$ and

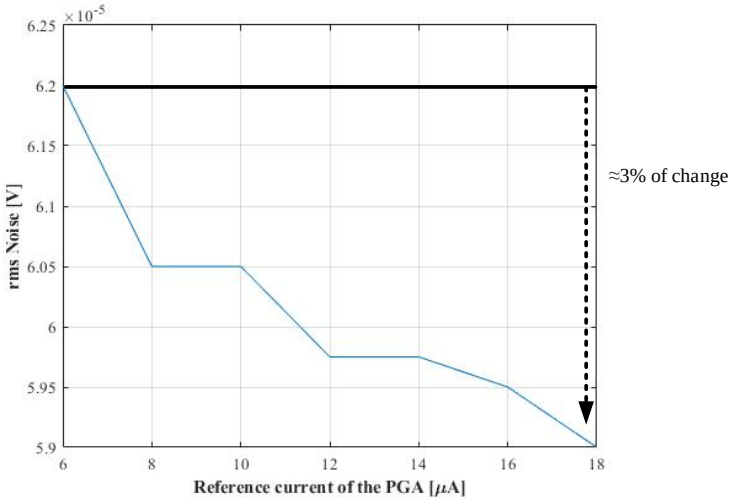

Figure 2-10: The noise of the PGA under different reference currents

$T_{c,n,comp}$ in Section 2-2-1. It is not possible to supply such a large current to the device. However, if the bandwidth of the PGA increases due to other factors, it is possible to compensate for the increasing noise of the source follower by applying the same ratio of the reference current according to Eq(2-12).

2-3-2 Reference condition of the signal

According to Eq(2-6) and Eq(2-9), the gain of the source follower reduces with increasing temperature. To eliminate the signal range distortion caused by the gain, the solution is to control the signal range of ADC. The signal range of ADC also impacts the signal. If the signal range can change with the gain of the source follower, the signal can always fit the signal range, so no exceeding or shrinking signal could happen. The theoretical expression can be written as

$$V_{out} = V_{sig} \cdot A_{SF}(1 + \Delta A_{SF}) \cdot A_{analog} \cdot \Delta Signal\ range \tag{2-14}$$

Where $\Delta Signal\ range$ is the change of signal range in the ADC and ΔA_{SF} is the change of source follower's gain included by temperature variation. Fig. 2-11 explains the working principle of this temperature compensation method. As the temperature increases, the gain of the source follower decreases, so the signal shrinks. The value of $\Delta Signal\ range$ can be designed the same as ΔA_{SF}. In addition, the temperature dependency of $\Delta Signal\ range$ should also follow ΔA_{SF}. Thus, by controlling the signal range in ADC, this variation can be recovered by the same amount of $\Delta Signal\ range$. Fig. 2-7 shows the temperature dependency of the source follower's gain in this project. According to the SPICE simulation, the gain reduces to around 8%. Therefore, combining ΔA_{SF} and $\Delta Signal\ range$ in Eq(2-14), the signal range of the ADC should increase linearly to 8% at the highest temperature to compensate for the signal distortion.

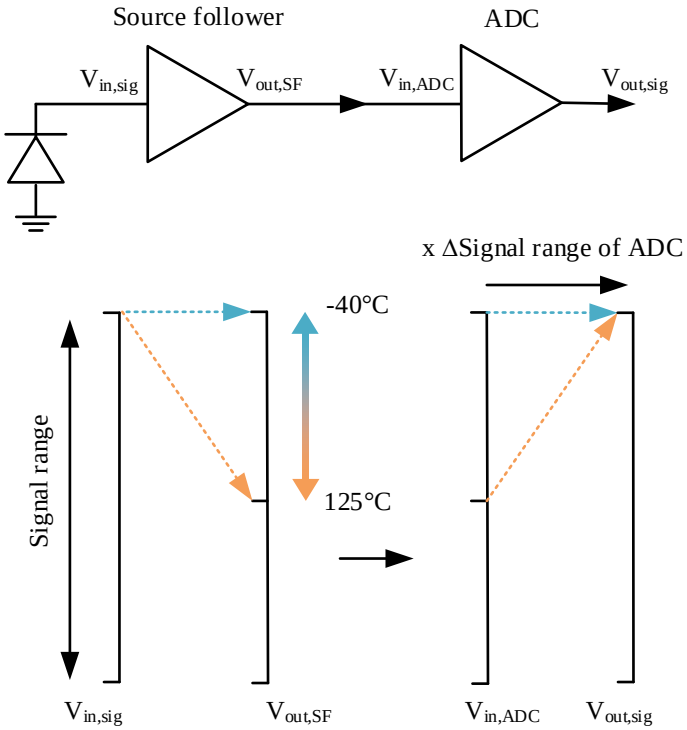

Figure 2-11: The compensation for source follower's gain

2-3-3 Reference condition of the PGA in this project

The bandwidth of the PGA as a function of the reference current can be written as

$$\omega = b_1 \cdot \sqrt{I_{D,PGA}} \tag{2-15}$$

Where ω is the bandwidth of the closed-loop PGA and b_1 is the constant that is invariant with the reference current. This equation is derived from Eq(2-9) and Eq(2-11). As the PGA is used as a unit-gain amplifier, and the transconductance is the main parameter that changes with a reference current, the bandwidth increases when transconductance increases.

As Eq(2-15) indicates, the bandwidth of the PGA is proportional to the transconductance; the transconductance is proportional to the root square of the reference current, assuming the dimensions of the transistor are fixed. A SPICE simulation of the bandwidth of the PGA under different reference currents at $55°C$ is shown in Fig. 2-12. One can see that the curve is pretty linear. It is because the PGA in this design is biased more closely to weak inversion, making the bandwidth increase more linearly with the reference current. However, the result still shows that it is possible to control the bandwidth by the reference current.

Insufficient bandwidth causes FPN. The change in bandwidth can be compensated by the reference current method. As Eq(2-15) indicates, when the reference current increases, the bandwidth increases. On the contrary, the bandwidth is reduced as temperature increases.

Combining the two phenomena, as the reference current increases as temperature increases, the bandwidth can be maintained at the same level. It can be prevented the bandwidth of the readout chain from falling and eliminate the FPN that might be generated due to sampling error. Fig. 2-13 shows the conceptual operation and simulation of this method. The bandwidth reduces with the temperature. However, if the reference current increases with the temperature simultaneously, the bandwidth can be maintained around the same level.

2-4 Final specification

Considering all possible solutions above, all the compensation factors require a specific temperature dependency. Therefore, a Proportional-To-Absolute-Temperature (PTAT) generator is chosen to implement an increasing temperature-dependent reference voltage.

First, a PTAT voltage can be converted to the reference current for the PGA and source followers. It can increase the bandwidth and suppress the noise at high temperatures. The reference current/voltage can be provided by these generators, so the reference condition can change with temperature. Besides, this analog on-chip method has many advantages over the digital compensation methods. First, this method does not require extra memory. Secondly, the sensor does not need to constantly communicate with digital blocks because the on-chip reference voltage will compensate for the change without being controlled by the user, which reduces the processing time. Due to a well-designed temperature dependency of the reference voltage method, the reference block can have different out voltages at different temperatures and automatically compensate for the temperature impact. Fig. 2-14 shows the connection between the PTAT generator and the three main blocks.

In Chapter 1, the impact of temporal noise and distortion has been explained. It can be seen as signal distortion and FPN. Part of the data could be lost in the analog domain if the signal is distorted. In addition, human eyes are sensitive to FPN. Therefore, to solve these two issues, the compensation is around 30% and 8% of increment at maximum temperature for compensating the settling error and the signal distortion. Fig. 2-15 shows the required PTAT curve for compensation. The starting voltage is set as $1V$ because it is the output voltage of the traditional BGR block in this design for comparison. Fig. 2-15 shows that these two blocks require different amount of compensation. Because we need different temperature slope for compensating the settling error and the signal distortion, two PTAT generators are required to generate two temperature slopes. However, considering the power consumption, one PTAT reference generator is implemented, so only one slope can be generated each time. We choose the signal range of ADC as the priority to compensate for preserving the signal integrity. As for the bandwidth, the headroom is assigned to the PGA to prevent the bandwidth from shrinking smaller than the sampling rate. As a trade-off, it generates more noise at low temperatures. In addition, increasing the bandwidth of the PGA introduces more noise from the source follower; therefore, the same amount of PTAT current is used for the source follower. The PTAT reference current can increase the transconductance and compensate for the effect of the bandwidth, according to Eq(2-12).

Therefore, the PTAT reference generator is decided to provide +8% of the linear voltage increment from -40°C to 125°C to compensate for the gain. The same compensation is

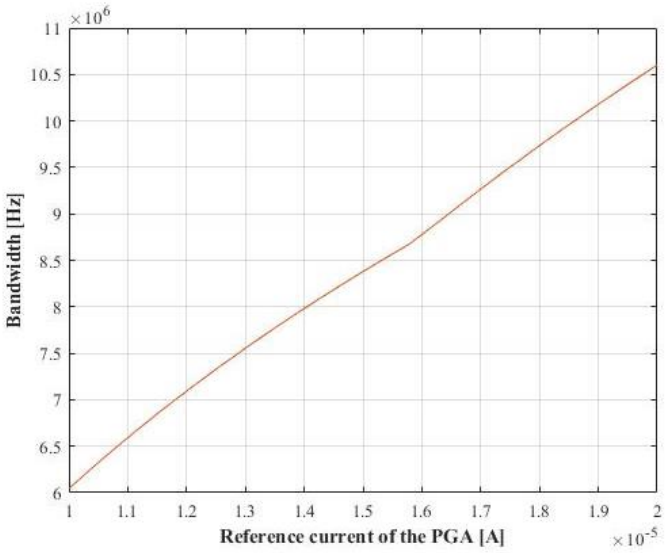

Figure 2-12: The bandwidth of the PGA under different reference current

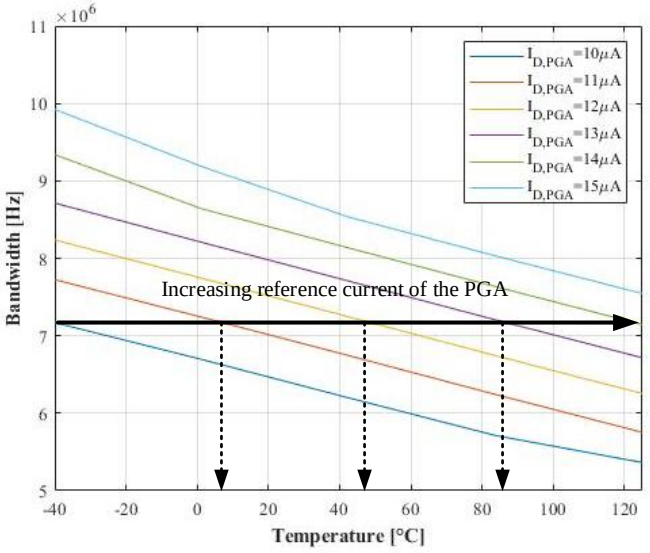

Figure 2-13: The bandwidth of the PGA under different temperatures and reference currents

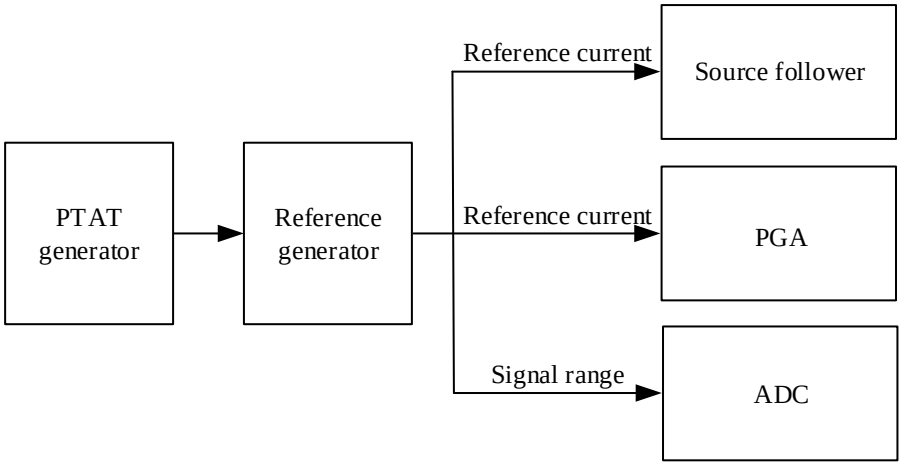

Figure 2-14: The connection between PTAT generator and three main blocks

provided to the source follower and the PGA. The transconductance of the source follower should increase by 3.9% at maximum temperature and the noise of the source follower should be maintained after the compensation of the PTAT reference current. The bandwidth of the PGA should increase by 3.9% at 125°C. This PTAT reference can also compensate for the bandwidth of the PGA by +3.9% at maximum temperature compared to the conventional design.

Source	Term	The change after compensation	The provided compensation
Source follower	g_m	+3.9%	+8.0%
PGA	g_m	+3.9%	+8.0%
	bandwidth	+3.9%	+8.0%
ADC	signal range	+8.0%	+8.0%

Table 2-1: The final compensation for this design

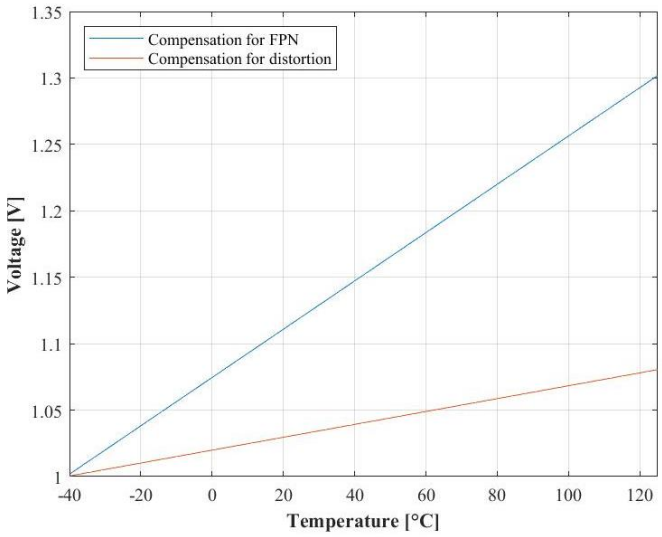

Figure 2-15: The required PTAT curves for the FPN and distortion compensation

Chapter 3

Reference generator design

In the previous chapter, the theoretical model was built to describe the impact of temperature, and a temperature compensation method with the PTAT reference methods operating from -40°C to 125°C is proposed to suppress the temperature dependency of the noise and control the bandwidth. Therefore, with the desired functionalities and specifications, the schematic of PTAT reference generators, including the theory and circuit design procedure, and the implementation methodology, are explained in this chapter.

A conventional BGR is modified to design the PTAT reference generators. The BGR is designed by summing a PTAT and a CTAT current to achieve a fixed voltage output. In this design, we control the gain of the Complementary-To-Absolute-Temperature (CTAT) and PTAT current to achieve a reference with the required temperature slope. Moreover, these PTAT reference generators can provide 16 different slope options due to a resistor ladder structure. This slope options design can cover the mismatch or external noise, aiding the accuracy of the compensation.

The systematic overview is introduced in Section 3-1. Section 3-2 explains the working principle of the PTAT reference generator. Section 3-3 presents the design process from the current values, the resistor ratio, the switched design, to the actual component dimension. Section 3-4 evaluates the non-linearity of the design. Section 3-5 is the verification of the effect of this PTAT reference generator on the source follower, the PGA, and the ADC.

3-1 High-level implementation in the system

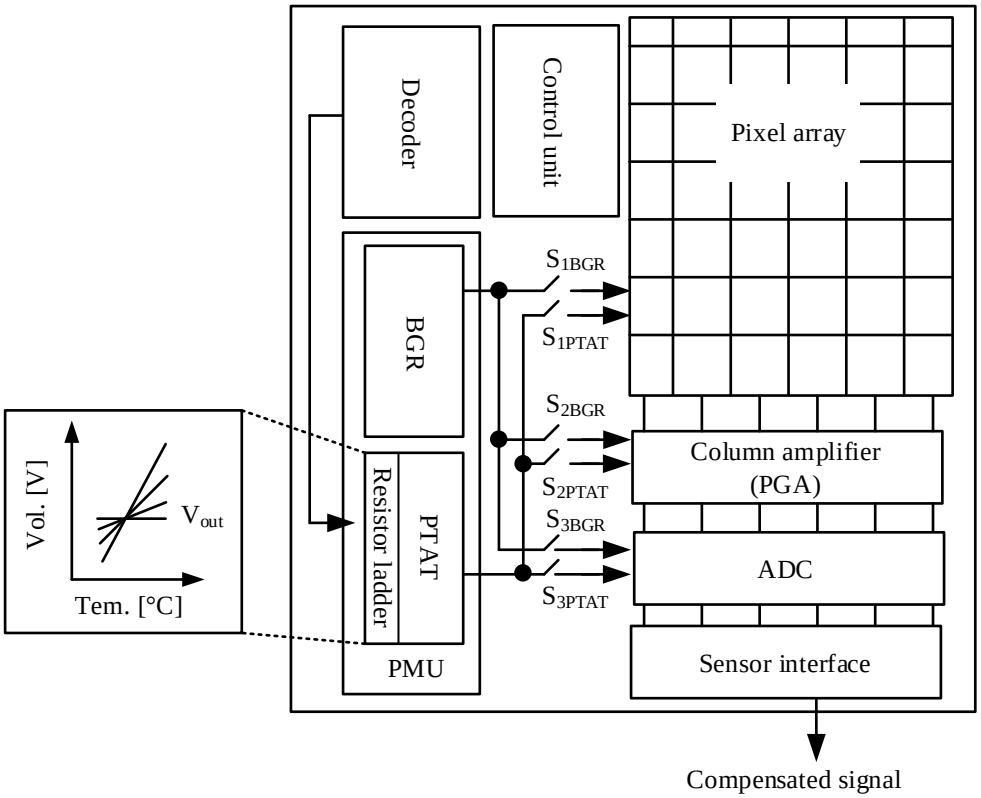

Figure 3-1: The block diagram of the systematic overview

According to the conclusion of Chapter 2, the PTAT reference generator is required to provide a reference current and a voltage for the source follower in the pixels, the PGA, and the ADC. Fig. 3-1 is the block diagram of the imager. The switches in the middle can control the connection between each block ($S_{1\text{-}3BGR}$ and $S_{1\text{-}3PTAT}$). The pixel, the PGA, and the ADC can be chosen to be connected to the PTAT reference generator or to the conventional BGR. With the output of the PTAT reference generators, the Power Management Unit (PMU) generates the reference current for the pixel and the PGA and the reference voltage for the ADC signal range.

Inside the PTAT reference generators, the resistor ladders with switched networks can provide multiple temperature slope options, shown in Fig. 3-2. This design is inspired by [20]. The resistors (R_{1a}, R_{1b}, and R_3) in the rectangle are resistor ladders. The structure of the resistor ladder is shown in Fig. 3-2. There are 16 switches inside the ladder. A decoder is used to control the resistor ladders. The PTAT reference generator can thus provide 16 different slope cases by connecting different resistors. This resistor ladder design can cover the mismatch generated by the variation of the devices inside the reference generator and

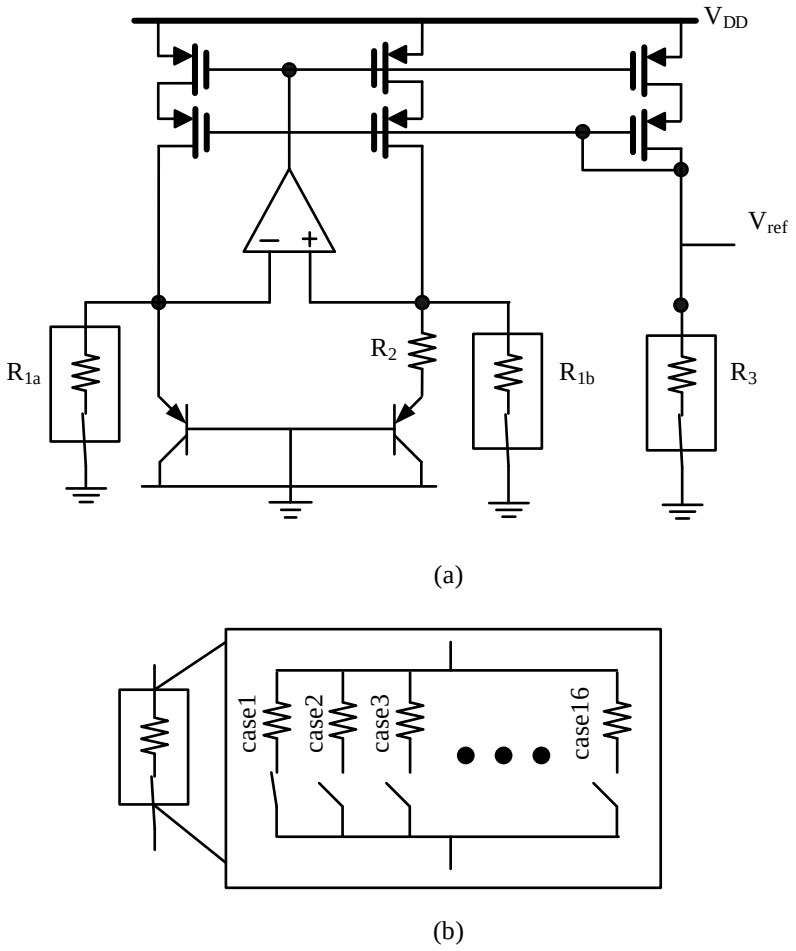

Figure 3-2: The block diagram of switched control (a) The schematic of PTAT reference generator (b) The schematic of the resistor ladder

the readout chain. It can also cover the effects of external noise or process, voltage, and temperature (PVT) during measurements. The slope of the PTAT reference generator's output is decided by the specification concluded in Chapter 2. However, except for the temperature slopes, we still need to consider the output voltage, noise, area, and accuracy as design specifications. The PTAT reference generator should have a +8% increment from the -40°C to 125°C and +0.48$mV/°C$ of the linear temperature slope assuming the starting voltage is 1V. The tolerance is 2.5% of voltage error in PTAT reference generators.

3-2 Working principle of the PTAT reference generator

The PTAT reference generators employ the temperature dependency characteristics of a Bipolar Junction Transistor (BJT). The working principle of a traditional BGR relies on

the temperature dependency of the base-emitter voltage(V_{BE}) of the BJT. The relationship between V_{BE} of the BJT and temperature can be expressed below

$$V_{BE} = \frac{kT}{q} ln\left(\frac{I_C}{I_S}\right) \tag{3-1}$$

Where V_{BE} is the base-emitter voltage, k is Boltzmann constant, T is the absolute temperature in Kelvin, q is the electron charge, I_C is the collector current, and I_S is the saturation current. I_S has high order temperature dependency [21] and it is a process-dependent parameter.

Combining two BJTs and subtracting V_{BE} of them, a PTAT voltage can be obtained. If the two BJTs are biased with the current ratio of $n:1$, and the two BJTs have different sizes of $1:m$, the current density with (1:nm) flows to two BJT respectively, and the base-emitter voltage difference in the two branches (ΔV_{BE}) is the PTAT voltage. The equivalent schematic is shown in Fig. 3-3. The ΔV_{BE} can be expressed as

$$V_{BE2} - V_{BE1} = \frac{kT}{q} ln\left(\frac{nI_C}{I_S}\right) - \frac{kT}{q} ln\left(\frac{I_C}{mI_S}\right) = \frac{kT}{q} ln(nm) \tag{3-2}$$

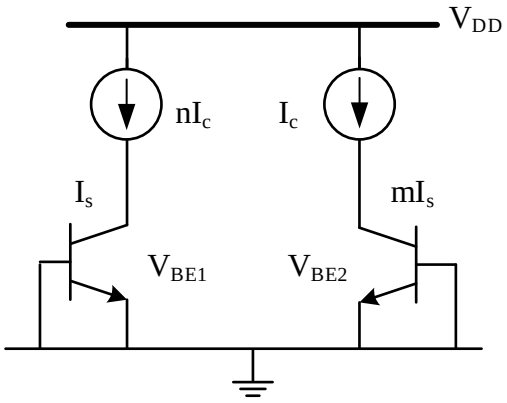

Figure 3-3: The generation of PTAT voltage

Especially, this PTAT voltage is insensitive to any process variation of V_{BE1} and V_{BE2} because the ratiometric relationship cancels out the I_S and I_C term assuming the current ratio is perfectly matched. The temperature dependency of ΔV_{BE} can be expressed as Eq(3-3).

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} ln(nm) \tag{3-3}$$

Similarly, this relationship is directly derived from the V_{BE} without approximation. Thus, this term is independent of temperature and linear, assuming no mismatch.

Finally, by combining V_{BE} and ΔV_{BE}, a reference voltage with different temperature dependencies can be generated.

$$V_{ref} = \alpha \cdot V_{BE} + \beta \cdot \Delta V_{BE} \tag{3-4}$$

Where α and β are fixed gain factors for V_{BE} and ΔV_{BE}. However, in this design, we control the temperature dependency of V_{ref} by adjusting the α and β. Eq(3-5) shows the temperature dependency of V_{ref}. Eq(3-5) is obtained by deriving the temperature term in Eq(3-4). The temperature dependency is also amplified by the gain factors. $\frac{\partial V_{BE}}{\partial T}$ is CTAT and $\frac{\partial \Delta V_{BE}}{\partial T}$ is PTAT. Combining these two terms with gain factors, the required temperature slope can be obtained.

$$\frac{\partial V_{ref}}{\partial T} = \alpha \frac{\partial V_{BE}}{\partial T} + \beta \frac{\partial \Delta V_{BE}}{\partial T} \tag{3-5}$$

The implementation is shown in Figure3-4, which is inspired by [20]. In Fig. 3-4, Q_1 provides the V_{BE1} as the CTAT voltage; Q2 is operated with a different current density from Q1 and generates V_{BE2}. The difference of V_{BE1} and $V_{BE}2$ is ΔV_{BE}. The amplifier is used to generate CTAT voltage at node V_A and node V_B, and PTAT voltage across R_2 by the closed loop. R_{1a} and R_{1b} have the same resistance value. The current flow through R_{1a} and R_{1b} are the same CTAT current. The current flow through R_2 is the PTAT current.

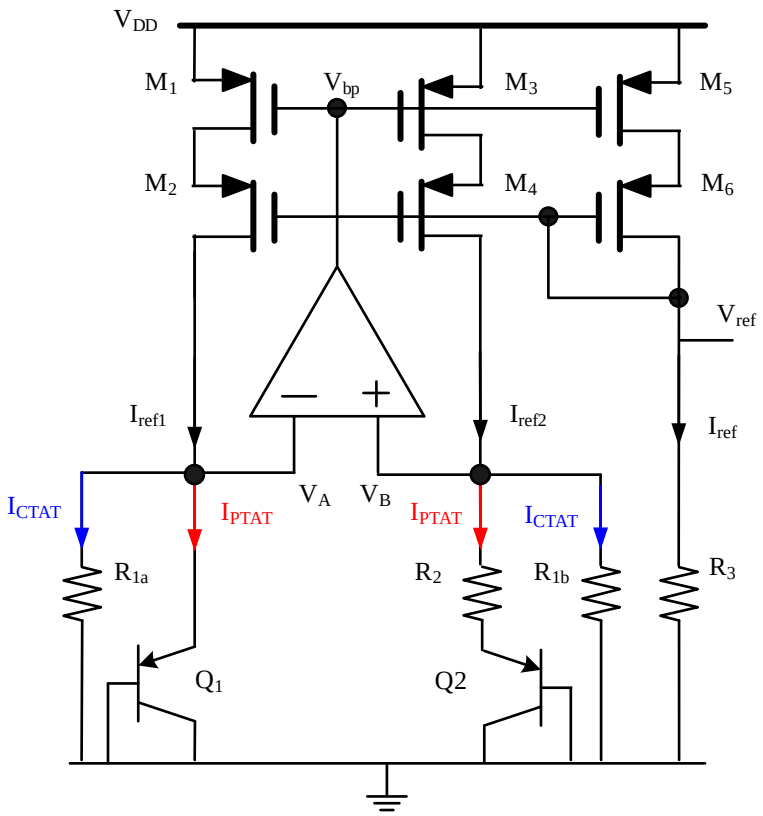

Figure 3-4: The PTAT reference generator in this design

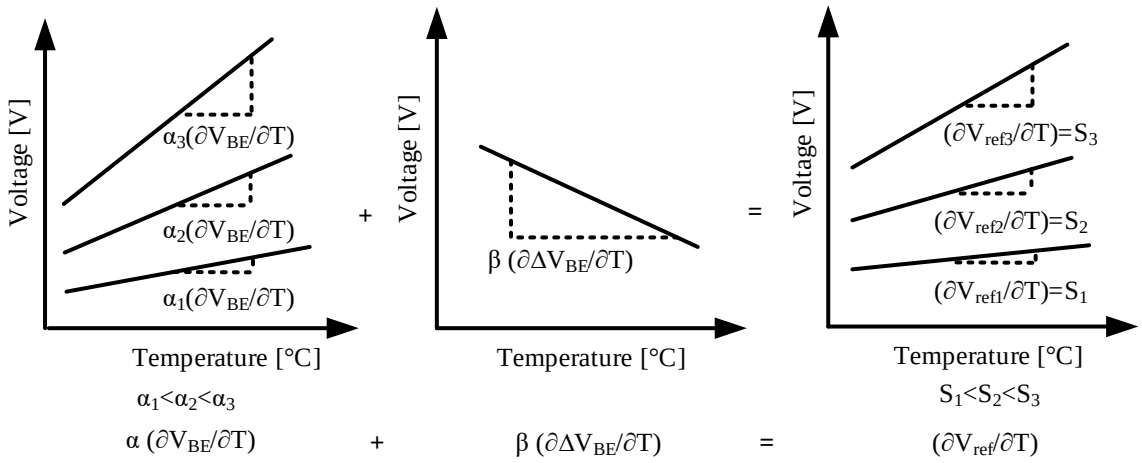

Figure 3-5: The reference voltage by summing V_{BE} and ΔV_{BE} based on Eq(3-5)

$R_{1a,1b}$ and R_2 convert the V_{BE} and ΔV_{BE} to the CTAT and PTAT current, respectively. The relationship is written in Eq(3-6) and Eq(3-7). I_{ref} is the sum of the CTAT and PTAT current. The PMOS transistor dimensions of M_1, M_3, and M_5 are the same, and their gates are connected to a common node. Therefore, the current is copied to the last branch and V_{ref} by R_3.

$$V_{ref} = I_{ref} \cdot R_3 \tag{3-6}$$

$$I_{ref} = I_{ref1} + I_{ref2} = \frac{V_{BE}}{R_1} + \frac{\Delta V_{BE}}{R_2} \tag{3-7}$$

Finally, the reference output can be expressed as

$$V_{ref} = R_3 \left(\frac{V_{BE}}{R_1} + \frac{\Delta V_{BE}}{R_2} \right) = \frac{R_3}{R_1} V_{BE} + \frac{R_3}{R_2} \Delta V_{BE} \tag{3-8}$$

Comparing Eq(3-4) and Eq(3-8), we can have the relationship between the gain factor and resistor ratio as

$$\frac{R_3}{R_1} = \alpha, \frac{R_3}{R_2} = \beta \tag{3-9}$$

Where α is the ratio of R_3 to R_1 and β is the ratio of R_3 to R_2. With this design, the resistor ratio can act as the fixed gain α and β in Eq(3-4) and Eq(3-5). The output voltage can be controlled by the combination of R_1, R_2, and R_3 as long as it does not exceed the output swing.

When R_1 increases, I_{CTAT} reduces. It means the portion of I_{PTAT} increases in I_{ref}. So the temperature dependency increases. Finally, the PTAT slope of the output voltage is less

positive. It can be seen in Fig. 3-5. Notice that the resistor is also temperature-dependent. In this project, a p^+ polysilicon resistor is used. This polysilicon has a negative temperature dependency [15]. The temperature dependency of the resistance can be approximated as

$$R = R_{ref}(1 - \xi \cdot (T - T_{ref})) \tag{3-10}$$

Where R is the resistance, ξ is the temperature dependency of the resistor, which is $0.85m/°C$ in this process. R_{ref} is the resistance of polysilicon at a reference temperature, T is the current temperature, and T_{ref} is the reference temperature. ξ increases as the temperature increases, and it is negative. Thus, the current flows to R_1 and R_2 are scaled by $(1 - \xi \cdot (T - T_{ref}))$. For example, when the temperature increases, the PTAT current increases further, and the CTAT current will reduce less due to this temperature dependency. However, the current mirror copies the sum of two currents, and the output current becomes

$$I_{ref} = \left(\frac{V_{BE}}{R_{1ref}\xi(1 - (T - T_{ref}))} + \frac{V_{BE}}{R_{1ref}\xi(1 - (T - T_{ref}))} \right) \tag{3-11}$$

where output voltage, V_{ref} is

$$V_{ref} = I_{ref} \cdot R_{3ref}\xi(1 - (T - T_{ref})) \tag{3-12}$$

Finally, the temperature dependency of the resistor term is canceled out in the output voltage. Therefore, the slope can be adjusted by controlling the resistor value of $R_{1\text{-}3}$, which composes the gain factors to achieve functionality.

3-3 Design process and implementation

3-3-1 Design of the BGR core

Fig. 3-6 shows the noise sources located inside the BGR and its small signal model [22]. The output-referred rms noise consists of the noise from the BGR core, the transistor M_5, and the resistor R_3, shown as

$$V_{n,out,total} = g_{m5}R_3\sqrt{V_{n,M5}^2 + V_{n,BGR}^2 + \left(\frac{V_{n,R3}}{g_{m5}R_3}\right)^2} \tag{3-13}$$

Where $V_{n,out,total}$ is the total noise of the PTAT reference generator, and g_{m5} is the transconductance of M_5 in Fig. 3-6. Assuming all the transistors are biased in saturation level and strong inversion, the total noise can be written as

$$V_{n,M5}^2 = \frac{4kT\gamma}{g_{m5}^2} + \frac{1}{g_{m5}^2}\frac{k}{C_{ox}WL}\frac{1}{f} \tag{3-14}$$

For $V_{n,BGR}$, assuming the gain of the amplifier is large enough, the closed loop gain of both sides can be approximated to 1. Finally, the RMS noise $V_{n,BGR}$ can be written as

$$V_{n,BGR}^2 = V_{n,A}^2 + V_{n,B}^2 + V_{n,M1}^2 + V_{n,M3}^2 \tag{3-15}$$

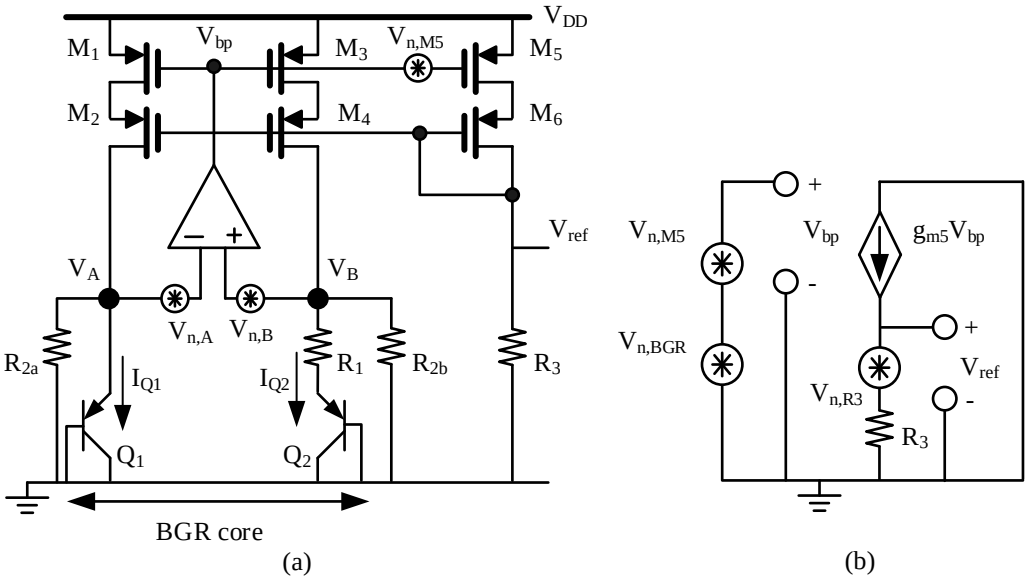

Figure 3-6: The noise model of PTAT reference generator (a)The noise sources in CTAT/PTAT generator (b)Small-signal model

Where $V_{n,A}$ is the total noise in node A, $V_{n,B}$ is the total noise in node B, and $V_{n,M1}$ and $V_{n,M3}$ are the noise from M_1 and M_3. Notice that the noise of the amplifier is contained in $V_{n,A}$ and $V_{n,B}$. Since the design target of the output rms noise has to be below $100\mu V/\sqrt{Hz}$, the resistor R_3 should be less than $100k\Omega$ and larger than $1k\Omega$ for power and stability concern. When the resistor R_3 is $100k\Omega$ the output rms noise is $63\mu V$ with a $10pF$ output load capacitor. Due to the loop structure, the collector current is equal to I_{PTAT}.

$$I_C = \frac{\Delta V_{BE}}{R_1} = \frac{\frac{kT}{q} ln(nm)}{R_1}$$

As n is the ratio of the emitter areas of the two BJTs. First, n is chosen as 24 to minimize the mismatch, as the total bipolar junction $(n+1)$ can compose a square of an integer for better symmetry in layout placement. If n is large, it consumes a lot of power, and also takes up more area. The smaller n, the larger the gain factor required to achieve desired PTAT slope.

For m, the transistor ratio of the current source, M_1, M_3, and M_5, is maintained as 1:1:1. For example, in Fig. 3-6 (a), if the I_{Q1} is the I_C and I_{Q2} is nI_C, as the potential in V_A and V_B is the same, the current flowing to R_{1a} and R_{1b} are both V_{BE}/R_2. However, the current flowing to Q_1 is $(I_C - V_{BE}/R_2)$ and the current flowing to Q_2 is $(nI_C - V_{BE}/R_2)$, which is not the multiplication of an integer anymore, and process variation in V_{BE1} and V_{BE2} is introduced if the current is copied ideally in the both side.

Finally, R_2 is chosen as $5k\Omega$ and I_C is $22\mu A$. We choose a smaller R_2 because R_1 and R_3 should be large to achieve desired PTAT temperature slope. After deciding on the collector current, we can estimate the resistor ratio.

The resistor ratio, α and β, should satisfy two conditions. The sum of V_{BE} and $\Delta\ V_{BE}$ should be $0.9V$ at -40°C, and the sum of the temperature dependency should be $0.48mV/°C$ as the target slope. Therefore, we can calculate the values α and β, shown as

$$\alpha \cdot V_{BE} + \beta \cdot V_{BE} = 0.9$$
$$\alpha \cdot \frac{\partial V_{BE}}{\partial T} + \beta \cdot \frac{\partial V_{BE}}{\partial T} = 0.48$$

The V_{BE} and $\Delta\ V_{BE}$ is $0.744V$ and $0.064V$ at -40 °C. $\frac{\partial V_{ref}}{\partial T}$ and $\frac{\partial \Delta V_{ref}}{\partial T}$ are $-1.5mV/°C$ and $0.27mV/°C$. The final resistor ratio, α is 0.6 and β is 5.4. Notice that the final values of resistor ratio are only used to make the primitive estimation, as the V_{BE} and $\frac{\partial V_{BE}}{\partial T}$ is changing slightly with current and process; therefore, the final value might differ from the calculated result.

$$R_3 = 0.6R_1$$
$$R_3 = 5.4R_2$$

3-3-2 Stability

Stability is another concern in this design. Unlike the traditional BGR, the resistor ratio is exploited in a certain ratio to generate the desired temperature slope instead of temperature-independent voltage output. In this PTAT reference generator, two feedback networks are designed. As described in Fig. 3-7, the left half part is working with a positive feedback network, and the right half part is operating with a negative feedback network. These two feedback networks have to meet the requirement to make this system reliable. First of all, in the positive feedback network, the loop gain has to be smaller than 1.

$$G = \frac{1}{1 + A\beta} \tag{3-16}$$

Where G is the loop gain of the system, A is the gain in the forward path, and β is the gain of the feedback loop. In this structure, the impedance at the negative input of the amplifier is sufficiently small and the feedback on the positive input of the amplifier relaxes the effect of the positive feedback effect. Therefore, this system maintains the stability of the positive feedback network. In addition, the negative feedback should have enough phase margin to prevent from phase shift. In particular, in this structure, the dominant pole is located at the output of the amplifier, and the second pole is located at the positive input of the amplifier. Therefore, the impedance at the positive input of the amplifier has to be small. In addition, this second pole has to be large enough to maintain the negative system stable, and the feedback factor of the negative feedback network and positive feedback network have to be similar. The dominant pole ω_1 and second pole ω_2 are calculated below.

$$\omega_1 = \frac{1}{R_{out,amp} \cdot C_{out,amp}} \tag{3-17}$$

Where $R_{out,amp}$ is the amplifier's output impedance, and $C_{out,amp}$ is the total capacitance in the output node of the amplifier. The second pole can be expressed as

$$\omega_2 = \frac{1}{R_{out,branc} \cdot C_{out,branc}} \tag{3-18}$$

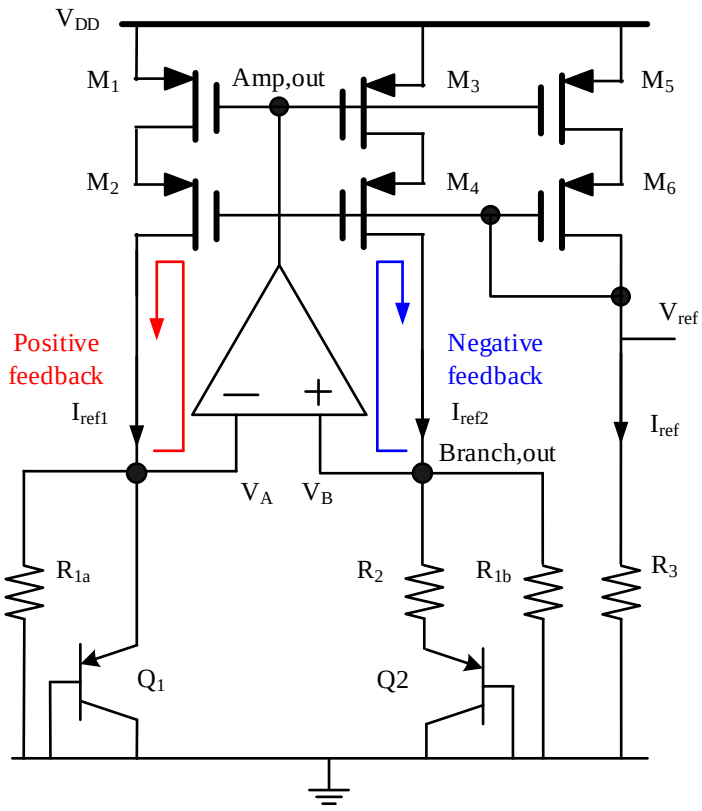

Figure 3-7: The feedback loop in this design

Where $R_{out,branc}$ is the output impedance of the branch, and $C_{out,branc}$ is the total capacitance in the branch seen from node V_A or V_B. To make the first and second poles far enough from each other, we can either add more capacitors in the output node of the amplifier to increase $C_{out,amp}$ to push the first pole to the left or reduce the output impedance to reduce $R_{out,branch}$ to push the second pole to the right. According to the resistor value decided in Section 3-3-1, the phase margin is 64°, which is safe for a stable operation.

3-3-3 Design of multiple slope options

The switches with different resistance pairs are placed to cover the mismatch in the reference generator and readout chain. First, if the mismatch happens in the reference generator, the reference output and slope could deviate, and the accuracy degrades. Secondly, if the mismatch happens in the readout chain circuit, the required slope could be different from the original design and deteriorate the compensation. Therefore, this design with switches can cover the change and offers different options for slopes and maintain the compensation.

To cover as many slopes as possible, we fill the slope options within the swing limit of the

	PTAT
$R_1[\Omega]$	$5.0k$
$R_2[\Omega]$	$40.4k$
$R_3[\Omega]$	$30.0k$
Phase margin of the worst case [°]	64

Table 3-1: The final value of $R_{1\text{-}3}$ in PTAT reference generator

next stage. The reference output should range within $0.9V$ to $1.3V$ so it can bias the input transistors of the PGA and the current mirror in the saturation range. The total number of cases is chosen as 16 due to the limited area. The maximum slope is $+2.4mV/°C$ and the minimum slope is $0.145mV/°C$. The required slope is $0.48\text{mV}/°C$. The slope difference between cases is $0.14\text{mV}/°C$. The corresponding voltage difference at the same temperature between cases is $18.7mV$, which is smaller than the error tolerance in the specification of $25mV$. It means the resolution of the voltage output is $18.7mV$ ($0.3/16 = 18.7m$) for the PTAT reference generator.

As the slope for each switch has been set, for better comparison, all the slopes should intersect at $1V$ and $1°C$. Each slope is composed of a different value of the resistors pair. We control R_1 and R_3 at same time. When R_1 increases, the CTAT slope and the reference voltage reduce; thus the PTAT reference becomes stronger in the output. When R_3 increases, the output slope and the voltage increase. Therefore, with two variables, we can control the temperature slope and output voltage level. The value of the resistor pairs in the resistor ladder is shown in Fig. 3-8 and the reference output of all 16 cases is shown in Fig. 3-9.

The size of the switch transistor is decided by minimizing the mismatch. We take the smallest resistance among all the cases as the standard, $5k\Omega$, the R_2 in the PTAT reference generator. Finally, we chose $15um$ for the width of transistor size for all the switched pairs, and the fraction of mismatch to total resistance is 0.01%.

3-4 Evaluation of the reference output

Fig. 3-10 is the output of Case1 of the generator. The output is not linear. This is because of the non-linearity of V_{BE}. The output voltage is composed of V_{BE} and ΔV_{BE}. However, V_{BE} is not a constant because saturation current has a temperature dependency. This temperature dependency results in the non-linearity of the CTAT curve and impacts the output. The temperature dependency of the saturation current in the bipolar junction can be expressed as [21]

$$I_S = \frac{kTAn_i^2\overline{\mu_p}(T)}{G_B} \tag{3-19}$$

Where G_B is the base Gummel number, which is a process-dependent parameter [23], A is the junction area, n_i is the intrinsic carrier concentration, and $\overline{\mu_p}$ is the mobility of the holes. Except for the temperature term in Eq(3-19), both n_i and $\overline{\mu_p}$ are temperature-dependent parameters and are not linear. The temperature dependency of V_{BE} can be shown in Fig. 3-11.

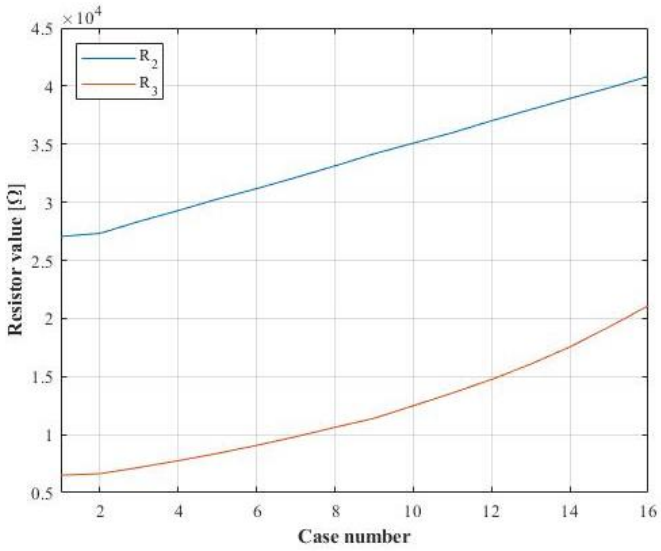

Figure 3-8: The resistor value in each case

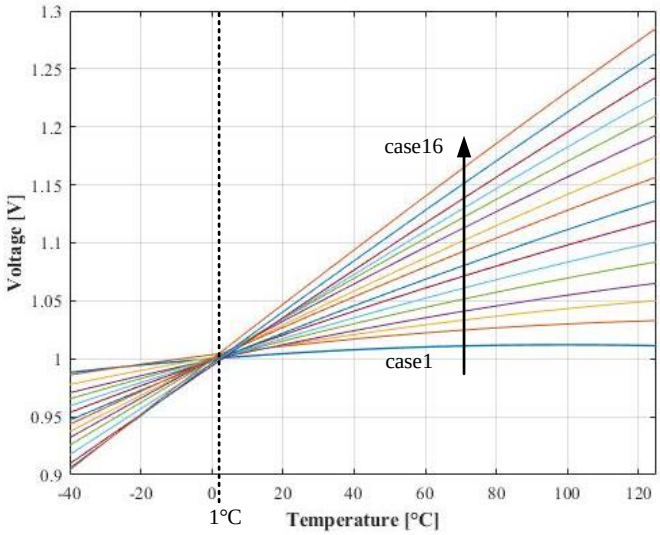

Figure 3-9: The reference output of each case

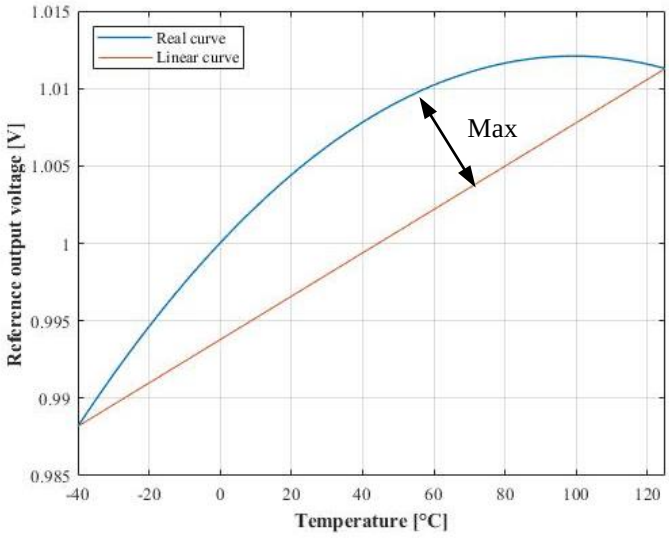

Figure 3-10: The evaluation of the non-linearity of the PTAT reference versus temperature

As the curve indicates, V_{BE} is deviating as a function of temperature from a perfect linear cure. If the V_{BE} is obtained at a certain temperature and we assume the change of V_{BE} is linear, the actual value of V_{BE} is smaller as the temperature gets further from the estimating point, which can be seen by the red circles in the Fig. 3-11. Therefore, the model is built based on the assumption of a linear temperature dependency of V_{BE}, and the non-linearity is measured in the real output. We evaluate the non-linearity by the maximum difference between the real curve and a linear curve connected by the voltage at the minimum and maximum temperature. Fig. 3-10 shows how the evaluation of non-linearity performs in this project.

In Fig. 3-10, the ideal linear curve connects the voltage in the lowest and highest temperatures. The maximum distance is the difference between the linear and real curves. The non-linearity is the distance divided by the voltage at the exact point. The non-linearity is calculated using MATLAB and shown as a percentage. In this design, the target is 2.5% of accuracy tolerance. The worst case is 0.8% in Case 1 and the best case is 0.6% in Case 16. The non-linearity in Case 3 is 0.8%, which is the slope for achieving the compensation. The result is concluded in Table 3-2. Notice that the non-linearity shrinks as the PTAT slope is stronger. This is because the non-linearity generated in the CTAT current and the resistor ratio amplifies the effect of PTAT, suppresses the effect of the CTAT current.

	Target	The worst case	The best case	Case3
Non-linearity	2.5%	0.8%	0.6%	0.8%

Table 3-2: The non-linearity of the output curve

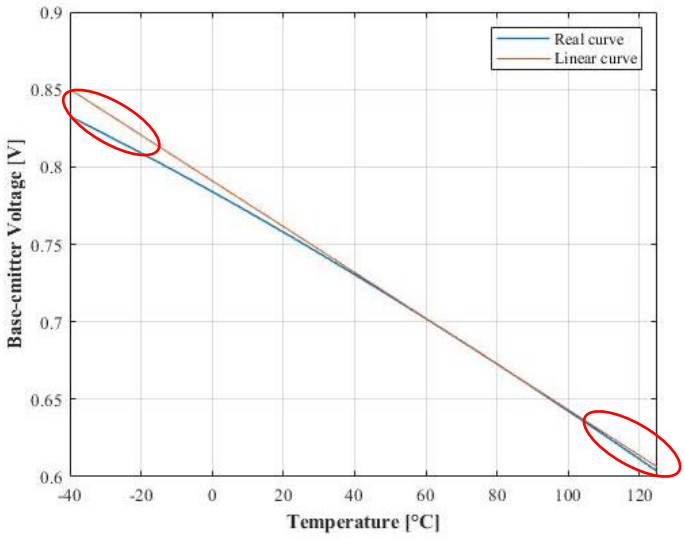

Figure 3-11: The non-linearity of the V_{BE} versus temperature

3-5 Verification

	Simulation result	
Temperature slope $[V/°C]$	$0.44m$	
Non-linearity	0.8%	
Output voltage $[V]$	$-40°C$	$125°C$
	0.98	1.05
Power (total) $[W]$	$-40°C$	$125°C$
	416μ	495μ
Noise $[V_{rms}]$	419μ	
Area (total)	$200\mu m \times 80\mu m$	

Table 3-3: The final simulation result of this design

The circuit is manufactured in $0.18\mu m$ technology from TowerJazz. The total size of the PTAT reference generator takes $200\mu m \times 80\mu m$ of the area. The final simulation result and overall performance of this design are concluded in Table 3-3. The main target is the temperature slope, which matches the specification even considering the non-linearity.

According to Table 2-1, the transconductance of the souce follower, the bandwidth of the PGA and the signal range of the ADC should change after the PTAT referent current is used. The simulation result of the transconductance and gain of the source follower in the pixel, the bandwidth of the PGA, and the signal range are shown in Fig. 3-12 to Fig. 3-15. Notice that the comparison is between a conventional BGR and the PTAT generator.

In Fig. 3-12, the transconductance of the source follower increases by 3.0% at maximum temperature, which is higher than the estimation of 2.7% by Eq(2-9). This comparison is

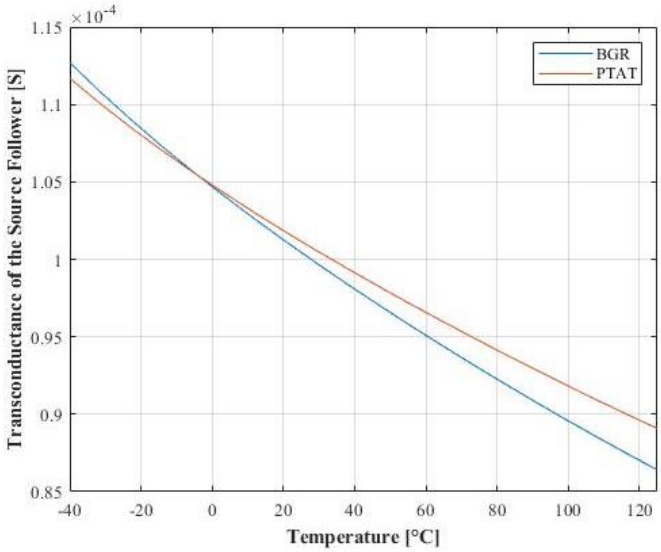

Figure 3-12: The compensation for g_m of the source follower

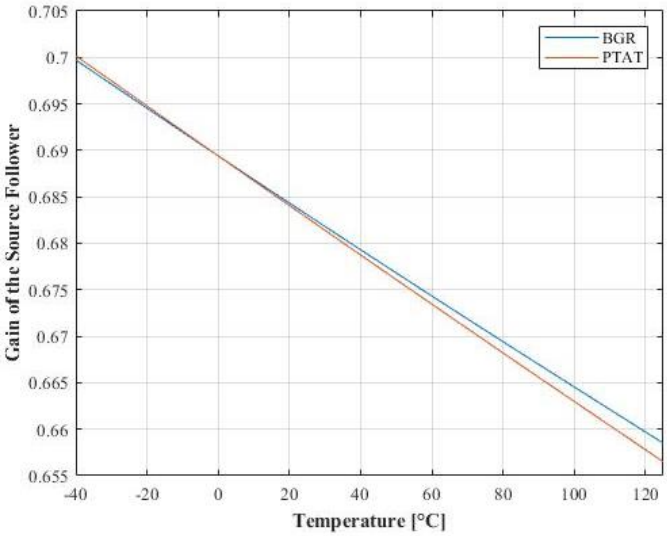

Figure 3-13: The gain of the source follower

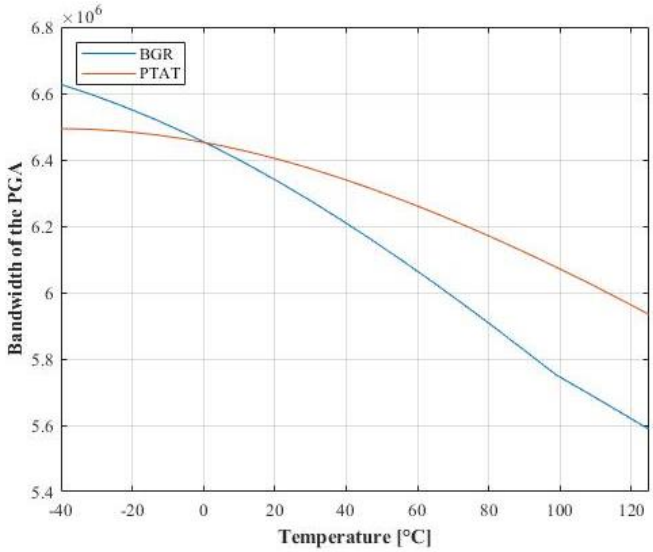

Figure 3-14: The compensation for the bandwidth of the PGA

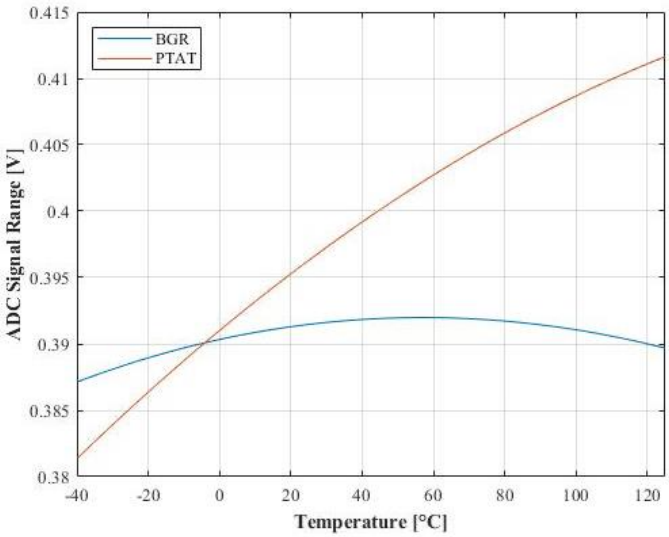

Figure 3-15: The control of signal range in the ADC

	g_m of the source follower		Bandwidth of the PGA		Signal range of the ADC	
	Sim.	Cal.	Sim.	Cal.	Sim.	Cal.
Result	4.4%	3.9%	8.2%	3.9%	8%	8%

Table 3-4: The simulation and calculation result of the PTAT reference generator

done by connecting the reference generator to the conventional BGR and this PTAT generator. First, calculation result is different from Table 2-1, which is 3.9%. This is because 3.9% is obtained by setting reference voltages as $1V$ at $-40°C$. However, we normalize all reference voltages to $1V$ at $0°C$. The voltage at $125°C$ reduces but the slope of the PTAT reference output is the same. There are two reasons to cause the difference between 3.0% and 2.7%. First, the output of the conventional BGR is $0.995V$ instead of $1V$ in the calculation, and the final output of this design is $1.083V$. Therefore, the increment is $(1.05V/0.995V \times 100\% =)5.5\%$. In addition, the reference current changes more than 5.5% because of the channel length modulation in the current mirror. For the gain of the source follower (Fig. 3-13), the gain reduces 7% from $-40°C$ to $125°C$, and the value is lower than 8% as predicted. It is because the PTAT reference current is used, so the gain reduces slightly at high temperatures.

Fig. 3-14 is the bandwidth of the PGA. The bandwidth reduces by 5% compared to the output in which the reference current is generated by a conventional BGR. This result is larger than 2.7% in the calculation result. This is because the PGA in the design is driven closer to weak inversion. In weak inversion, the transconductance is closely proportional to the drain current instead of the root square fashion. Besides, the compensation is not linear. It is because of the non-linearity of the PTAT reference generator and the temperature dependency of the polysilicon resistor. Fig. 3-15 shows the signal range of ADC. The signal range increases 8% from -40$°C$ to $125°C$, which is close to the 8% of theoretical estimation. Notice that the signal range of the BGR output is not straight because of the non-linearity of V_{BE}. In addition, the temperature dependency does not impact the signal range as it is converted back to the voltage and the effect of the resistance is canceled. The conclusive result is shown in Table 3-4.

The layout schematic of the CMOS image sensor is shown in Fig. 3-16. The post-simulation is only performed to evaluate the performance of the PTAT generator. According to the post-simulation, the V_{ref} at -40$°C$, $55°C$, and $125°C$ is only slightly increased by around 0.1%. The $55°C$ is chosen because it is the average operating temperature. The deviation results from the metal layer's parasitic resistance. However, the impact of parasitic resistance is small because of the ratiometric relationship of the resistor ratio.

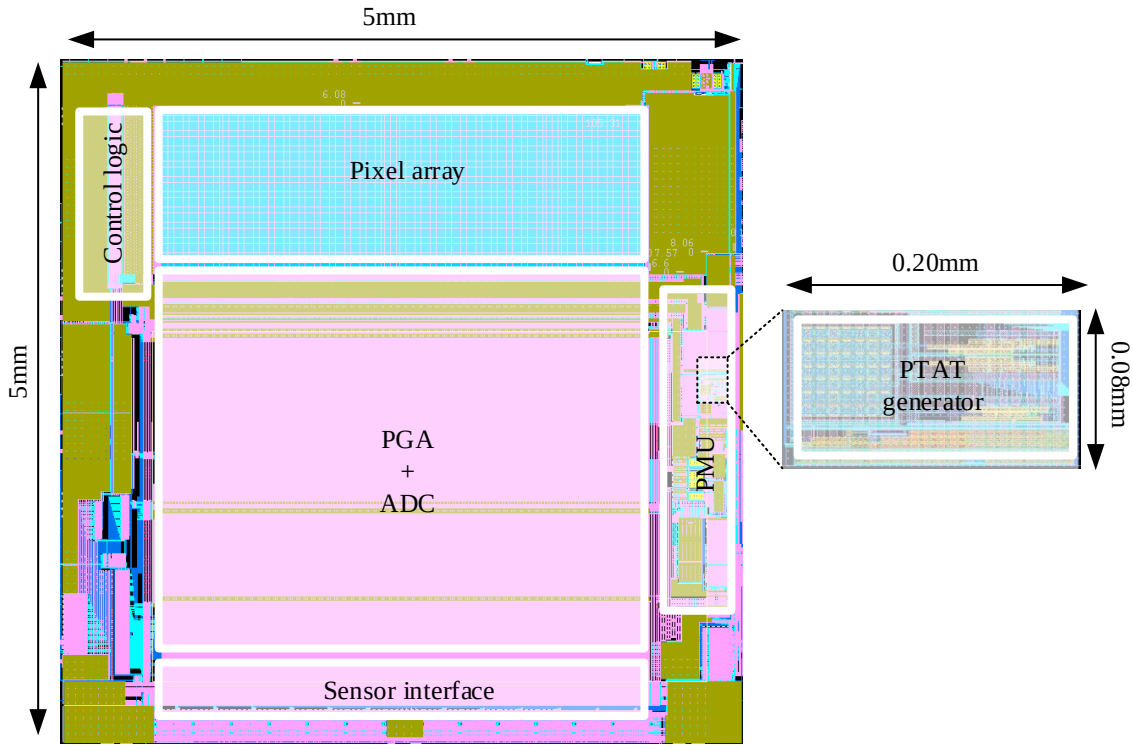

Figure 3-16: The layout of the PTAT reference generator

Chapter 4

Conclusion and future work

This chapter presents the simulation of the expected results by means of the data collected by the SPICE model. As the real chip is not measured, the results can still be estimated by the data and theory. The temperature dependency, the gain, and the bandwidth are examined to see the result of this reference control method. The future work is discussed to explore the potential improvement of this work. Finally, a short conclusion is made to summarize this thesis.

Section 4-1 is the simulation result of this work. Followed by a discussion of future work. Finally, the conclusion is presented.

4-1 Result simulation

Due to the limited time, the actual result of the measurement is not available. However, the simulation is performed to predict the results. The data collected from the SPICE simulation can be used to estimate the evaluation factors in the output images, such as SNR, DR and FPN. The total temporal noise, bandwidth of the PGA and signal range are measured for estimation. Although the performance of the PTAT generator matches the specification, the effect of the non-linearity of the PTAT generator could impose inaccuracy to the results. Therefore, the result of this project is discussed in this section.

4-1-1 Temperature dependency of the temporal noise

Fig. 4-1 and Fig. 4-2 show the temperature dependency of the temporal noise in the 4T pixel and this design. The temporal noise almost remains the same after the compensation. As the conclusion drawn in Chapter 2, the noise from the PGA is remained due to the negative feedback. The noise from source follower also remains the same. The PTAT reference current is used to the PGA, so the bandwidth increases; however, the same amount of PTAT reference current is used to bias the source follower, so the transconductance also increases with temperature. Combining these two effects, the noise can remain at the same level even if the bandwidth in the PGA increases, and SNR is not degraded. In addition, the pixel used in this project is different from conventional 4T pixel [14]. In our pixel structure, the kTC noise is introduced, and the temperature constant of kTC noise is the dominant term.

4-1-2 Compensation of signal distortion

The compensation of signal distortion is estimated by Eq(2-14). The $\Delta Signalrange$ should be equal to the ΔA_{SF} to compensate the signal distortion. Fig. 4-3 shows the temperature dependency of the signal range before and after compensation. The signal at -40°C is normalized to 1 for better comparison. The compensation deviates from a straight line. The non-linearity of the PTAT directly impacts the result. According to the result, the non-linearity is around 1% at the worst point. In addition, since this temperature dependent reference control method is implemented by multiplying another temperature-dependent term $\Delta Signalrange$, the output signal is a second-order polynomial equation as a function of the temperature and the curve is hyperbolic.

4-1-3 Compensation of settling error

Fig. 4-4 shows the modulated bandwidth. The bandwidth increases 8% at the maximum temperature compared to the bandwidth managed by the conventional BGR. As predicted, the bandwidth can be modulated by the temperature-dependent reference control method. Case8 is simulated to show the adequate compensation for bandwidth because its temperature slope matches the required compensation for the bandwidth. The temperature dependency of the bandwidth changes from -17% to +2%. Therefore, the bandwidth does not reduce and a settling error can be prevented. Besides, this design can also relax the design margin when designing the PGA in the sensor. The bandwidth can be maintained and so no margin is required for preventing the bandwidth to shrink smaller than the sampling rate.

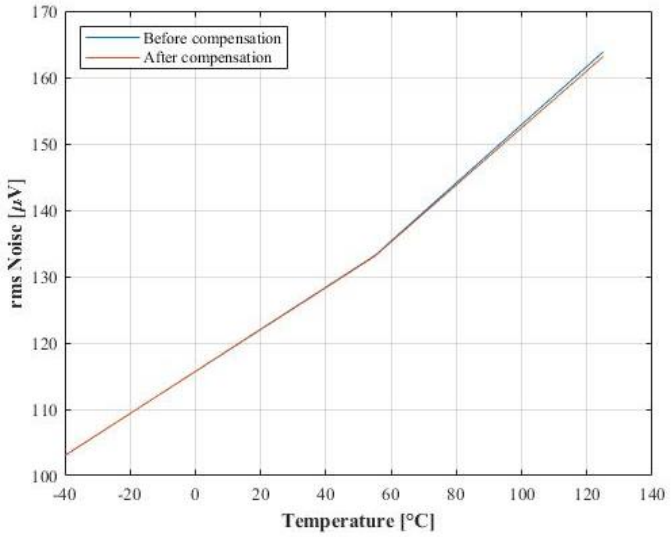

Figure 4-1: The temporal noise simulation of the 4T pixel

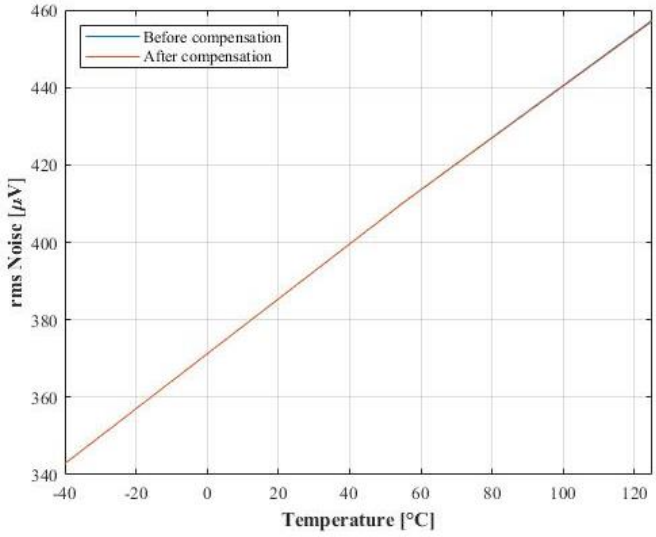

Figure 4-2: The temporal noise simulation of the pixel used in this project

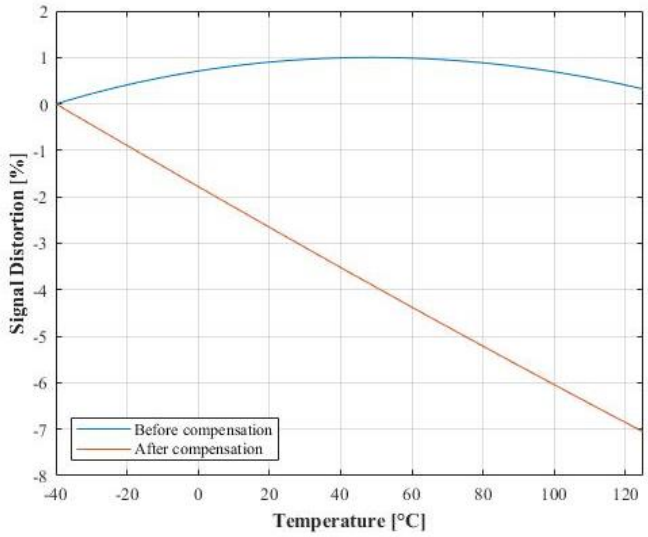

Figure 4-3: The simulation of the signal distortion

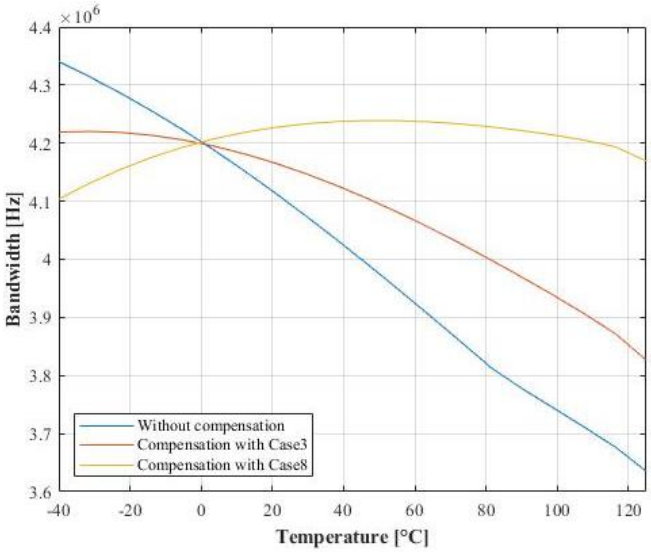

Figure 4-4: The simulation result of the bandwidth

4-2 Future work

Aside from the contribution of this work, due to the time constrains, there are some aspects that could be improved.

1. The practical experiment with measurements should be implemented to support the simulation result. Because the chip did not come back from the manufacturer on time, the chip is not shown and measured in this thesis. The temporal noise level, SNR, DR, signal nonuniformity, and linearity should be measured at different temperatures and compared with the simulation results. In addition, the performance of the PTAT generator should also be measured to be compared with the result in Chapter 3.
2. The power consumption can be further improved by better sizing of the amplifier.
3. The polysilicon resistors can be replaced with other types of resistor. The temperature dependency of polysilicon is not linear, which makes the non-linearity in the reference control method worse, especially for the pixel and the PGA as they are biased with a reference current. There are other resistors that have a linear temperature dependency, such as diffused resistors [15]. This can help to mitigate the non-linearity of the output.

4-3 Conclusion

Recently, machine vision has been one of the most important applications for CMOS image sensors. There are applications of machine vision required to work in harsh environments where the temperature can change drastically. In addition, high-speed, high-resolution and high-dynamic range operation of the sensors can also generate more heat during operation. Both effect results in large temperature variation. This temperature variation changes the performance of the readout chain in CMOS image sensors and distorts the signal. This thesis aims to investigate the temperature impacts on the readout chain and to maintain the sensors' performance with a temperature-dependent reference control method to compensate for the impact of the temperature from -40$^{\circ}C$ to 125$^{\circ}C$. With this method, the distortion of the signal can be prevented and the bandwidth of the PGA can be controlled without introducing more temporal noise. This design can help CMOS image sensors to be more robust to temperature changes in real-life applications.

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Glossary

CDS	Correlated Double Sampling
DDS	Digital Double Sampling
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
FPN	Fixed Pattern Noise
SNR	Signal-to-Noise Ratio
DR	Dynamic Range
SAR ADC	Successive-Approximation ADC
BGR	Band-Gap Reference
PTAT	Proportional-To-Absolute-Temperature
CTAT	Complementary-To-Absolute-Temperature
PVT	process, voltage, and temperature
PMU	Power Management Unit
BJT	Bipolar Junction Transistor

Appendix

A-1: The SPICE simulation of the noise in the readout chain

The parameters for pixel, PGA calculations are listed in Table A-1-1 and Table A-1-2. Notice that these parameters are obtained by SPICE simulation.

Name		Value	
Temperature	-40°C	55°C	125°C
g_{m1} $[S]$	52μ	41μ	35μ
g_{m2} $[S]$	28μ	21μ	18μ
g_{m3} $[S]$	111μ	89μ	77μ
g_{m4} $[S]$	28μ	21μ	17μ
W_1 $[m]$		0.42μ	
L_1 $[m]$		0.6μ	
W_3 $[m]$		1.97μ	
L_3 $[m]$		0.6μ	
I_D $[A]$		9μ	
V_{DD} [V]		3.3	

Table A-1-1: The parameters for the source follower noise simulation

Name		Value	
Temperature	-40°C	55°C	125°C
g_{m1} $[S]$	131μ	110μ	95μ
g_{m2} $[S]$	55μ	48μ	44μ
W_1 $[m]$		134.8μ	
L_1 $[m]$		1.5μ	
W_3 $[m]$		20μ	
L_3 $[m]$		0.6μ	
I_D $[A]$		9μ	
V_{DD} $[V]$		3.3	

Table A-1-2: The parameters for the PGA noise simulation