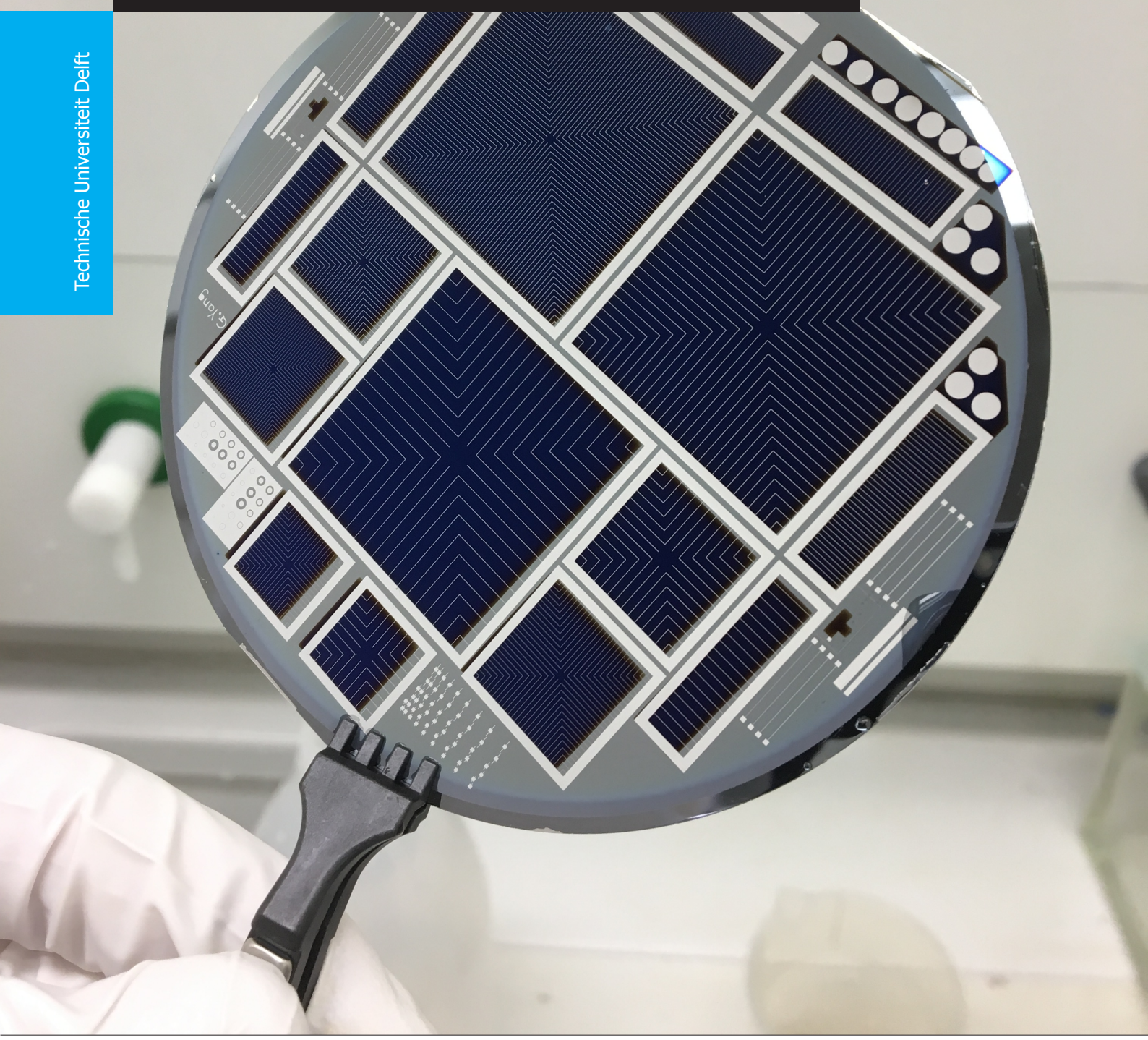
Master Thesis Final Report

High Efficiency SHJ/Poly-Si Hybrid Solar Cells

Guillaume Le Boucher d'Hérouville

Technische Universiteit Delft



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Challenge the future

Master Thesis Final Report

High Efficiency SHJ/Poly-Si Hybrid Solar Cells

by

Guillaume Le Boucher d'Hérouville

Student number: 4595858

in partial fulfillment of the requirements for the Master of Science

Sustainable Energy Technology

at the Delft University of Technology,

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Abstract

High efficiency silicon heterojunction (SHJ) solar cells have already reached more than 26% efficiency [1] when tunnel oxide passivated contacts solar cells just broke the 26% barrier at the beginning of February 2018 [2]. For such devices, major losses occur at both the front and rear contacts where parasitic recombination can be very high. Carrier-selective contacts use a special design in order to build a barrier that would block one specific charge carrier and let the other one go through. A Hybrid solar cell is a combination between a heterojunction solar cell and a TOPCon device, featuring then carrier-selective contacts at both sides. In this thesis, a p-type TOPCon structure is implemented at the rear when the front contact is made of n-type amorphous silicon (a-Si:H).

Intrinsic amorphous silicon (a-Si:H) used as front passivation layer, is deposited on top of crystalline silicon and requires an interface with as few defects as possible to minimize the parasitic recombination velocity. A new pretreatment method studied in this thesis involves the growth of a silicon oxide (SiO_2) on a crystalline silicon substrate, that will allow to get rid of most of the superficial defects after etching and before a-Si:H deposition. Lifetimes of up to 6 ms and saturation current density (J_0) as low as 14 fA/cm^2 can be reached with a 200 nm thick oxide.

As a-Si:H presents a very low lateral conductivity, a transparent conductive oxide (TCO) is needed to transport the charge carriers towards the front metal contacts. The resistivity of such a material should be as low as possible. While increasing the deposition temperature of Indium Tin Oxide (ITO), it has been possible to decrease the resistivity up to 2.5 $\cdot 10^{-4} \Omega$ .cm at a temperature of 130°C, without reducing the optical properties of such a layer.

Finally, manufacturing defects are often introduced during the fabrication process, leading to some shunt losses (low shunt resistance). As we are fabricating several solar cells per wafer, it is most of the time necessary to cut them to get rid of the shunt before doing the measurements. This sensitive step could be avoided with a better isolation of each solar cell. Patterned ITO and metal have been developed in this thesis, allowing to reduce the shunt power losses in the range of $1-2$% without the need to cut the cells.

Contents

1

Introduction

1.1. Photovoltaic Technologies

By the end of 2016, the cumulative worldwide photovoltaic installation reached 320 GW, with more than 76 GW installed for 2016 alone [3]. With an average growth of above 30% for the last years, the trends are still very high for the coming years as reported in the figure 1.1 below according to a scenario from SolarPower Europe [4].

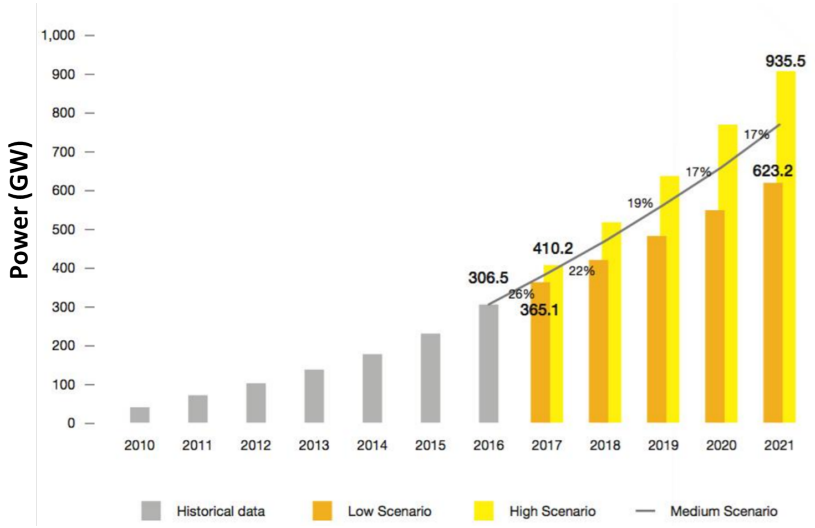


Figure 1.1: World annual solar PV market scenarios 2017-2021 [4].

While taking a closer look to this market, different PV technologies have been used. With more than 90% of the world production in 2016, the Crystalline Silicon (c-Si) technology is dominating the market ahead of the Thin Film solar cells [5]. The basic principle of such technologies is based on

the photovoltaic effect. It can be simplified into 3 fundamental processes. First, the generation of charge carriers due to the absorption of photons in the materials that form the junction. Then, the separation of these photo-generated charge carriers in the junction. Finally, the collection of the photo-generated charge carriers at the terminals of the junction. The separation of charge carriers is possible if some specific materials with semipermeable membranes are used. Usually, some doped materials are used to achieve this property. A Phosphorus-doped material will introduce some excess electrons in the material (n-type material) whereas a Boron-doped material will have some excess holes (p-type). These 2 materials will form a junction of a conduction band (energy Ec) and a valence band (energy Ev) and a photon can only be absorbed if its energy is higher than the energy difference of these 2 bands. This difference $Ec - Ev = Eg$ is defined as the bandgap of a semiconductor material and represents the forbidden states for the electrons. The photovoltaic effect is summarized in figure 1.2 below:

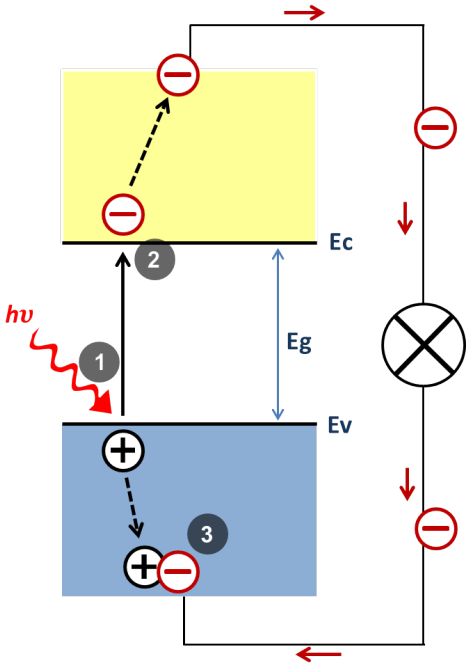


Figure 1.2: Principle of the photovoltaic effect: 1. Generation of charge carriers through the absorption of a photon ($h\nu$). 2. Separation of the electron-hole pair. 3.Collection of the carriers through a circuit and recombination.

1.2. Physical Properties of Silicon

Silicon for PV application is mainly used under three different forms: mono-crystalline (c-Si), poly-crystalline (poly-Si) or hydrogenated amorphous silicon (a-Si:H).

Crystalline silicon presents a very ordered structure with its atoms arranged in a diamond cubic crystal lattice. The orientation of the crystal will lead to some electronic band dispersion and the band diagram of crystalline silicon is shown below [6]:

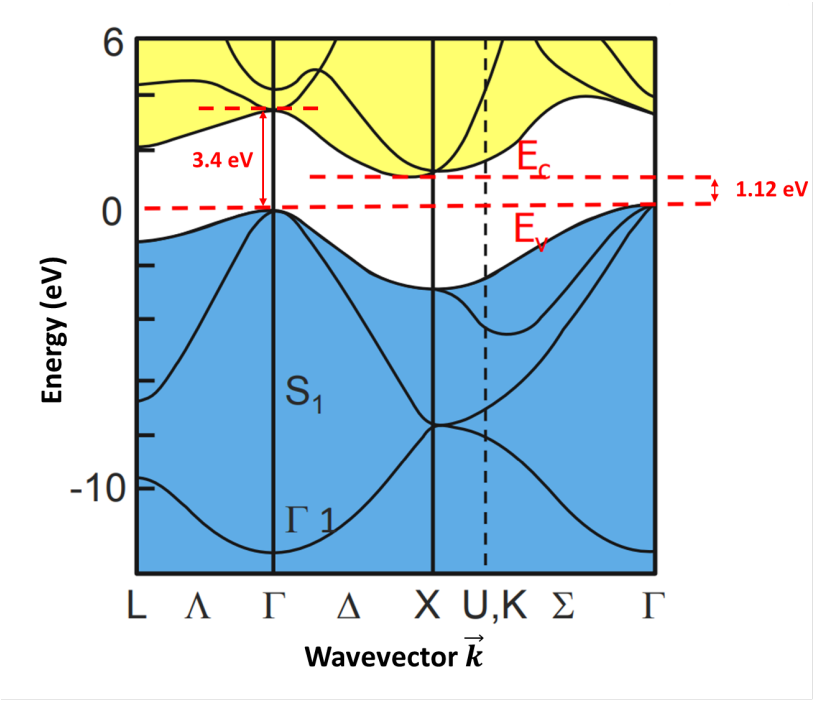


Figure 1.3: The band diagram of crystalline silicon [6].

The lowest energy difference between the conduction band (E_c) and the valence band (E_v) is 1.12 eV and is the bandgap energy of this material, referring to the infrared part of the spectrum (1107 nm). As these 2 energy levels are not aligned, the charge carriers in the valence band have to change their momentum as well as their energy in order to reach the conduction band: it is known as an *indirect bandgap*. It will then be more difficult for the high energy photons to excite the electrons due to this change of momentum. The absorption coefficient of such a material will be lower than for materials with a direct bandgap. It can be noticed in figure 1.3 above that crystalline silicon presents also a direct bandgap of 3.4 eV corresponding to the blue part of the spectrum (364 nm). When the crystal is made of one uniform grain over the whole lattice, it is called monocrystalline silicon (usually confounded with crystalline silicon). However, it is possible to have some materials made out of numerous crystalline silicon lattices next to each other. These materials are called polycrystalline silicon – abbreviated in polysilicon – and present some lattice mismatches at the boundaries between the different crystals. It will introduce some defects because of these different orientations and misalignments, that can lead to recombination losses as it is explained in the next section 1.3. This polysilicon presents nonetheless some advantages, especially in the manufacturing process of this material that is usually easier and cheaper than for monocrystalline silicon.

Contrary to c-Si, amorphous silicon presents a disordered structure. Due to the presence of defects across the lattice, its optical properties are different, leading to weaker performances. However, a hydrogenated form of amorphous silicon (a-Si:H) is usually used and presents the advantage to have some hydrogen atoms passivating most of the defects, especially the dangling bonds, leading to a reasonable defect density around $10^{16} cm^{-3}$ [7]. It will be very interesting in term of passivation

properties as some parasitic recombination can be reduced or avoided, as we will see in the following section 1.3.

1.3. Recombination Effects

As we saw in the section 1.1, recombination is a key factor for the generation of electricity as it drives the collection of the charge carriers after the separation. However, when the carriers recombine before going through the external circuit, it leads to important losses. It is then important to limit the internal recombination when it comes to the design of a solar cell. This losses mechanism will have a negative effect on the lifetime of the charge carriers. Indeed, the highest the recombination rates are, the lowest the lifetime of the minority carriers is. This lifetime can be linked to the different recombination mechanisms lifetime as follows:

$$\frac{1}{\tau_{eff}} = \sum_i \frac{1}{\tau_{r,i}} \tag{1.1}$$

with $\tau_{r,i}$ the lifetimes of the different recombination mechanisms. Three principal recombination mechanisms play a role in the bulk of the material:

- Radiative recombination
- Auger recombination
- Shockley-Read-Hall (SRH) recombination

The Radiative recombination, also called *direct recombination*, occurs mainly in direct bandgap materials. In this case, an electron from the conduction band will directly recombine with a hole from the valence band, releasing a photon. This mechanism is usually neglected when it comes to silicon based solar cells as with an indirect bandgap it is very low.

The Auger recombination involves the presence of three charge carriers. When an electron and a hole recombine, the energy released is transferred to a third carrier that will be excited and will thermalize to go back to an equilibrium state. This recombination mechanism will play an important role with a high concentration of charge carriers, such as heavy doping. It can then be a limiting factor for silicon based solar cells.

The last recombination mechanism involves the presence of defects. An electron (or a hole) can be trapped in the forbidden energy band because of some defects. As its energy is reduced (or increased), it is more likely that a hole (or an electron) can reach the same level and then recombine. This mechanism will also play an important role in silicon based solar cells as defects are present in the bulk as well as at the surface.

Talking about the surface, it is an area with a high probability of recombination – especially the SRH one – because of numerous defects, and it is necessary to tackle this issue in order to fabricate high-efficiency solar cells. The surface lifetime τ_s can be written as:

$$\frac{1}{\tau_s} = \frac{2 \cdot S_r}{d} \tag{1.2}$$

with S_r the effective surface recombination velocity and d the thickness of the material, and it should be as high as possible. The thicker the material is, the less the surface recombination plays a role but it is often important to deal with thin layers in order to minimize some absorption losses. We will see in the following section 1.4 that even the crystalline silicon, with very few defects in the bulk, is very sensitive to the SRH recombination at the surface because of some dangling bonds.

1.4. Homojunction vs Carrier-Selective Contacts

The homojunction solar cells are devices made with one single material. The main losses for such a design are at the Si/metal interface since metals have a very high surface recombination velocity. It is explained by the presence of numerous intermediate states that can become traps for electrons and holes, as highlighted in figure 1.4. It is possible to partially compensate this problem while implementing a heavy-doped Back Surface Field (BSF), introducing a field-effect that prevents the minority charge carriers to reach the contact, as with the successful PERL (Passivated Emitter Rear Locally Diffused) and PERT (Passivated Emitter Rear Totally Diffused) designs.

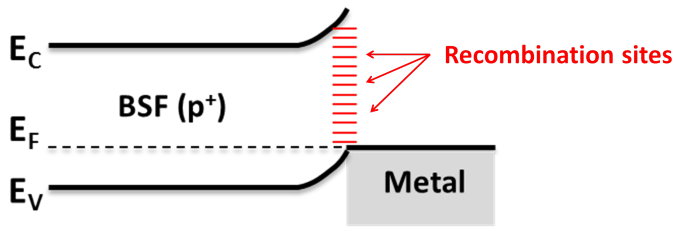


Figure 1.4: Contact recombination sites at the metal interface.

To reduce even more these recombination losses occurring at the front and rear surface, carrier-selective contacts have been developed. They can offer a good passivation including two main features that lead to a reduction of the surface recombination:

- Chemical passivation: dangling bonds at the surface are being saturated with small atoms such as Hydrogen.
- Field-effect passivation: introducing an electric field that will act as a barrier to separate the electrons and holes and avoid an accumulation of both types of charge carriers leading to recombination.

1.4.1. Chemical passivation

We already mentioned in the previous section 1.3 that even with a well structured crystalline silicone, some defects are present at the surface because of *dangling bonds*. This is shown in figure 1.5 below:

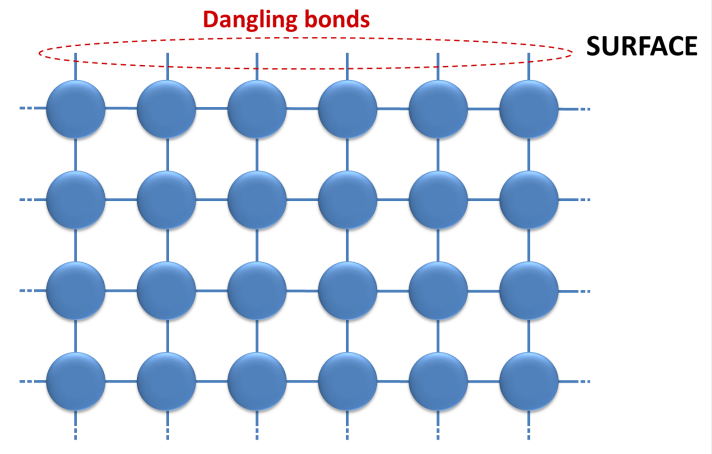


Figure 1.5: Crystalline silicon lattice with dangling bonds at the surface.

These dangling bonds can become good trapping sites for charge carriers leading to recombination especially with the SRH mechanism mentioned above. This problem is particularly important at the front side as the front surface recombination will prevent the charge carriers to be collected, lowering the open-circuit voltage of the device. It can also prevent some charge carriers to reach the bulk of the cell, reducing the current. A chemical passivation can partially solve this problem while depositing a passivating layer that could saturate some of these dangling bonds. The surface defect density is then decreased as we have reduced the amount of trapping sites, and the lifetime of the charge carriers can be significantly increased. Two good candidates for this passivation are hydrogenated amorphous silicon (a-Si:H) that contains around 10% of hydrogen in atomic weight [8] and silicon oxide (SiO_2). A chemical passivation with a-Si:H is highlighted in figure 1.6 below:

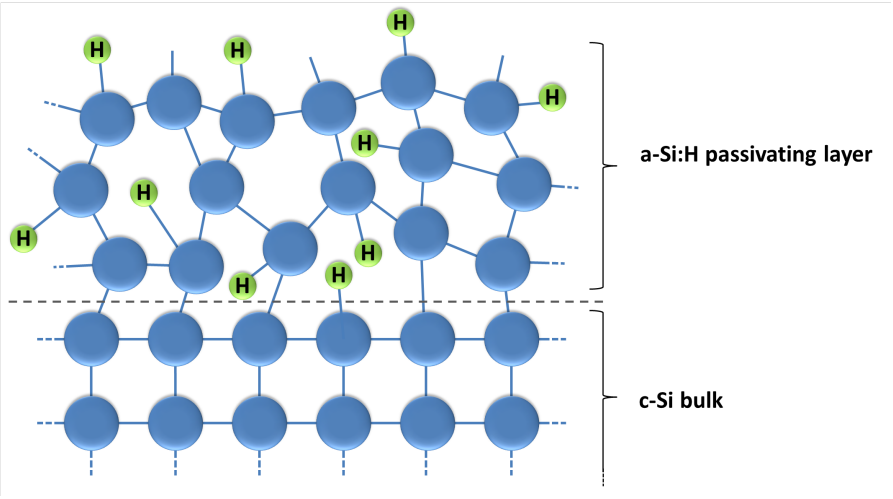


Figure 1.6: Crystalline silicon lattice with a passivating layer of a-Si:H at the surface.

1.4.2. Field-effect passivation

Field-effect passivation can be seen as a shielding of one type of carriers through an electrical field. This electrical field can be created by an additional layer with certain amount of fixed charges (for instance Al_2O_3 for p-type Si or SiO_2 for n-type Si) such that a depletion region width is created and electrons or holes are shielded from the surface [9]. With the presence of this barrier, the recombination can be significantly reduced and the effective lifetime of the charge carriers is increased. A schematic view of the field-effect is presented in figure 1.7 below, with the blue barrier representing either a doping profile or an additional material:

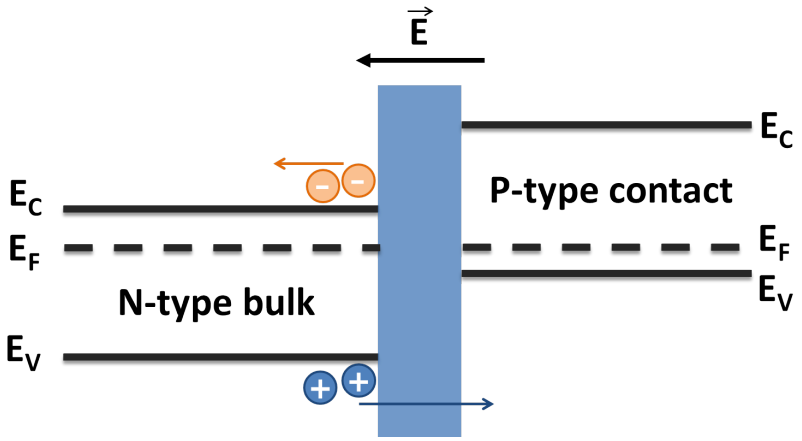


Figure 1.7: Schematic view of a field-effect passivation with an electric field $\vec{E}$ introduced by the blue profile.

One type of charge carrier can reach the contact through a tunneling effect that will be developed in the next section 1.5. The other type of charge carrier is blocked and can not cross the energy barrier and it leads to the desired carrier selectivity.

The development of doping profiles have been considered in the first instance [10] but the introduction of an additional layer as a barrier considered later on showed even better results [11], that is why we decided to implement this passivating method along this thesis.

As some additional layers, such as SiO_2 or a-Si:H, are implemented together with a c-Si bulk, the solar cells using this kind of carrier-selective contacts are part of the heterojunction solar cells family. More details about the mechanisms involved are given in the next section 1.5

1.5. Motivation for Hybrid Solar Cells

In this thesis, together with a c-Si bulk we decided to implement carrier-selective contacts in order to reach high efficiencies as explained in the previous sections.

1.5.1. Heterojunction Solar Cells

The first possible design with carrier-selective contacts would be the Silicon HeteroJunction solar cell (SHJ), with a deposition of a thin layer of intrinsic amorphous silicon ((i) a-Si:H) at the front and the rear.

This layer would first generate a chemical passivation of dangling bonds at the Si surface, reducing the surface defect density. On top of that, it will act as a wide-bandgap material that creates an electrical field across the junction, inducing a barrier for one type of charge carrier. The general structure of such a cell is presented in figure 1.8 below:

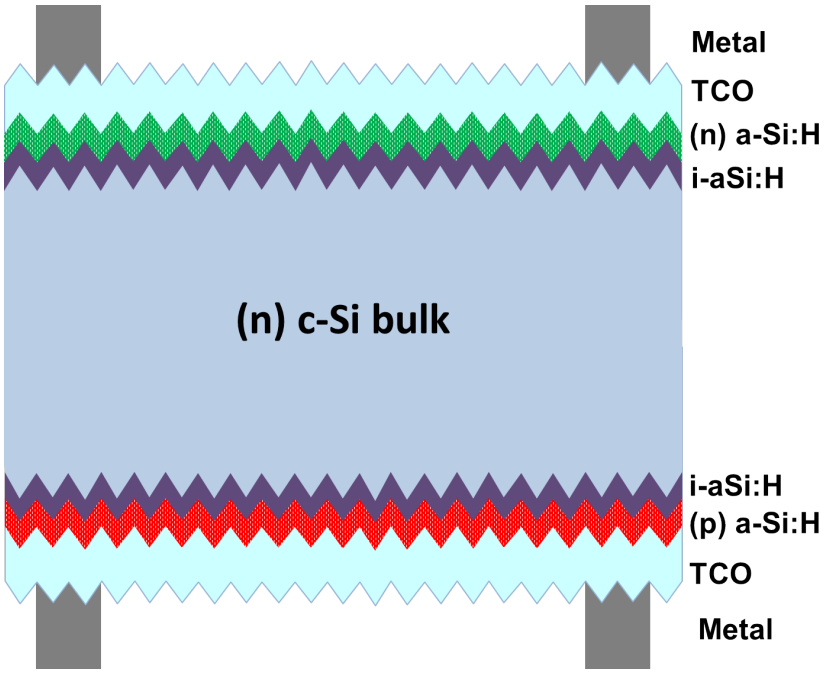


Figure 1.8: Structure of a Heterojunction with Intrinsic Thin Layer (HIT).

A n-type c-Si bulk is generally used as the absorber and is textured in a solution of TMAH (TetraMethylAmmonium Hydroxide) in order to increase the light trapping. Three cleaning cycles in acid baths of the textured wafer followed by a HF dip are necessary before depositing the first amorphous silicon layer in order to get rid of the impurities at the surface as well as the native oxide. Amorphous silicon can be deposited with a Plasma Enhanced Chemical Vapor Deposition (PECVD) process with a gas mix of silane (SiH_4) and hydrogen (H_2). The same process can be used to deposit the doped amorphous silicon with respectively phosphine (PH_3) and diborane (B_2H_6) as precursor gases to form the n-type and the p-type a-Si:H emitter layers. As amorphous silicon presents a very low lateral conductivity, a Transparent Conductive Oxide (TCO) should be deposited at the front side before the metallization, in order to allow the charge carriers to reach the metal contacts.

More details about these different processing steps will be given in chapter 2.

The band diagram in figure 1.9 below shows the mechanism of the carrier-selective contacts induced by the a-Si:H layers.

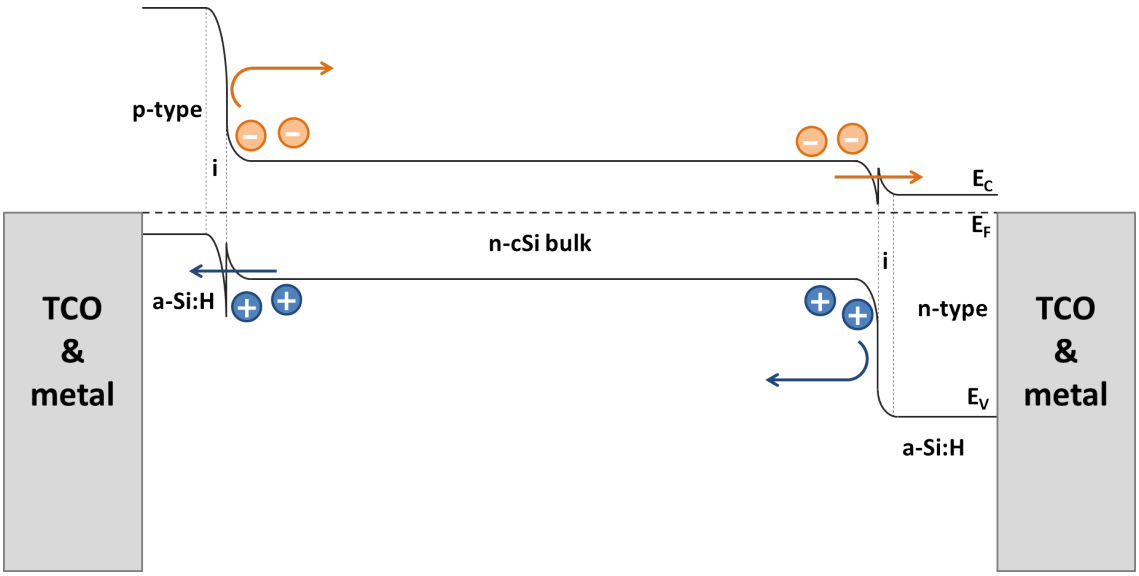


Figure 1.9: Band diagram of a HIT cell.

On the left side, the holes can cross the barrier created by (i) a-Si:H as the energy levels in the valence band (E_V) are almost the same on each side of the barrier, whereas the electrons can not cross because the energy difference of the conduction band (E_C) is too high. The same effect is happening at the right side with the electrons able to cross the (i) a-Si:H barrier while the holes can not due to the energy difference across this layer. To obtain a good quality of carrier-selective contact, the energy difference of the conduction (respectively valence) band across the barrier should be small in order to allow the electrons (respectively holes) to tunnel through it in case of n-contact (respectively p-contact) and it should be high at the other side in order to prevent the electrons (respectively holes) to cross the barrier and reach the p-contact (resp n-contact).

High efficiencies have already been obtained with HIT solar cells such as the world record with front contact reaching 24.7% efficiency [12] and Kanaka reaching more than 26% in 2017 with interdigitated back contact HIT [1].

1.5.2. Tunnel Oxide Passivated CONtact (TOPCon) approach

Another promising approach using some carrier-selective contacts with an interesting potential is the so-called *Tunnel Oxide Passivated CONtact* (TOPCon). This technique started to be developed in the 1980s by E. Yablonovitch and T. Gmitter [13] who realized they could obtain a high V_{oc} of 720 mV while implementing a Semi-Insulating Polycrystalline-Silicon (SIPOS) on both sides of the c-Si wafer. Thanks to the thin oxide layer, the passivation had been significantly improved leading to this increase on V_{oc}. This technique allows to reduce the minority carrier recombination at a good level, similar to the HIT cells introduced in the previous section 1.5.1, with the advantage of a better tolerance to higher temperatures processes.

On the same principle as the intrinsic amorphous silicon barrier introduced previously, an ultra-

thin layer of silicon oxide (SiO_2) grown at the interface between the c-Si bulk and the poly-Si. It will introduce a *chemical passivation* as the oxygen atoms can saturate some dangling bonds of the poly-Si, permitting to reduce the interface defect density (D_{it}) and then the recombination rate at this interface. Besides that, a *field-effect passivation* is also introduced as an energy barrier is created by the SiO_2 layer. A so-called *tunneling effect* can occur leading to a good carrier selectivity: for a n-contact (respectively p-contact), the electrons (respectively holes) are able to tunnel through the SiO_2 whereas the holes (respectively electrons) can not cross the barrier due to the energy difference on either side. This effect, similar to the (i) a-Si:H barrier of HIT cells but with an ultra-thin barrier, is summarized in figure 1.10 below:

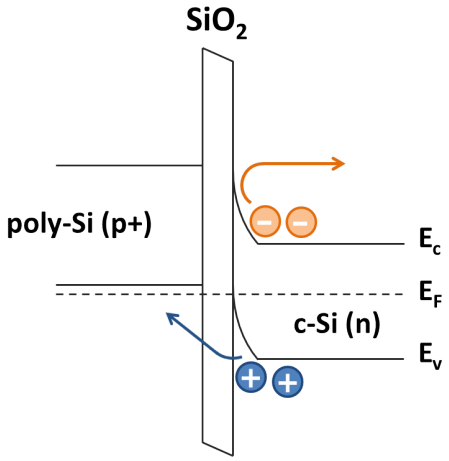


Figure 1.10: Tunnel effect introduced by a SiO_2 layer at a p-contact interface.

Due to this good passivation quality, solar cells with a TOPCon approach can reach high efficiencies such as F. Haase et al. who reached 25% efficiency using an Interdigitated Back Contact (IBC) with poly-Si and TOPCon [14] or A. Richeter et al. who achieved 25.7% employing TOPCon layer at the backside and homojunction at the front side [15]. This last design is shown in figure 1.11:

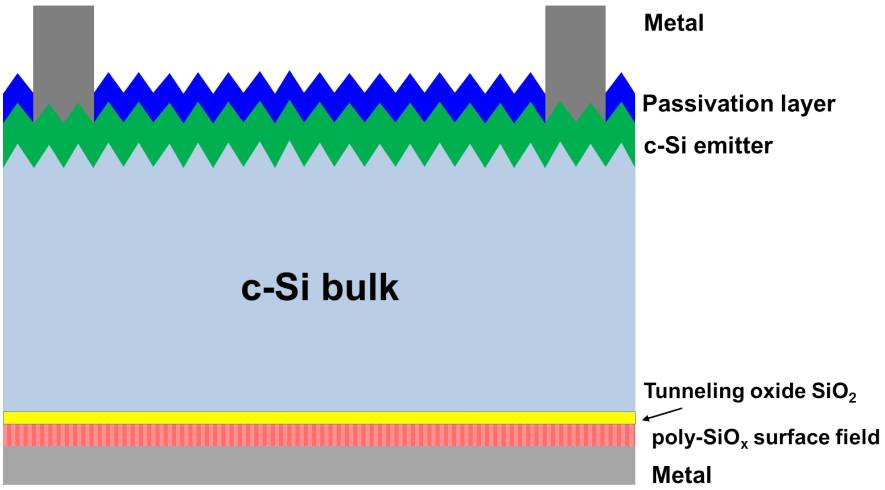


Figure 1.11: Structure of a silicon solar cell with a passivated rear contact.

1.5.3. Hybrid solar cells

Taking into account the two passivating methods introduced in the previous sections 1.5.1 and 1.5.2 an interesting approach would be to combine them. Indeed, we saw that the TOPCon structure leads to substantial parasitic absorption and it is an important problem when it comes to the front contact. On the other hand, the excellent passivation provided by the SiO_2 barrier offers a strong potential. That is why it is possible to consider a silicon heterojunction design including a tunnel passivated contact and an amorphous silicon contact. The structure of such a solar cell is presented in figure 1.12

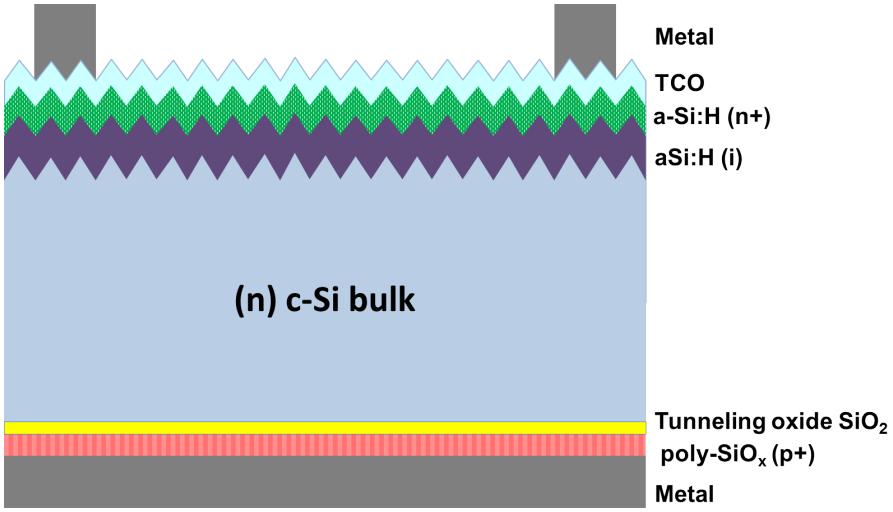


Figure 1.12: Structure of an Hybrid solar cell with poly-Si rear emitter.

It would be possible to consider a n-type front surface field with the same (n) c-Si bulk or even a (p) c-Si bulk with front or back emitter for investigating Hybrid solar cells. However the main focus is on the structure above-mentioned as n-type c-Si substrates present less impurities and then have a lower recombination velocity [16], and boron-doped a-Si:H (p-type) currently give lower minority carrier lifetimes compared to phosphorus-doped a-Si:H (n-type) [17].

The current optimized design for the structure of figure 1.12 includes a 300 μm textured n-type c-Si wafer with 4.5 nm of (i) a-Si:H, 6 nm of (n+) a-Si:H and 75 nm of TCO at the front, as well as an ultra-thin layer of SiO_2 (a few nanometers) and a poly-Si layer of 250 nm thick at the rear. A full area metal is deposited at the back when at the front a mask is used for metallization in order to let the light be absorbed and collect it thanks to the metal fingers and busbars.

The band diagram of the Hybrid solar cell presented in figure 1.12 above can be seen below and underscores the carrier-selective contacts at the front and the back.

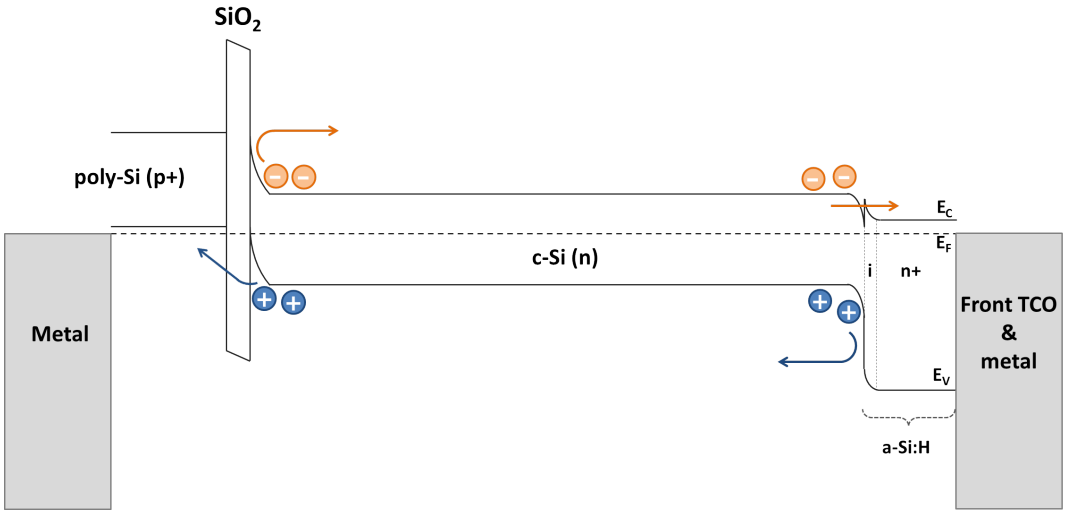


Figure 1.13: Band diagram of an Hybrid solar cell with poly-Si rear emitter.

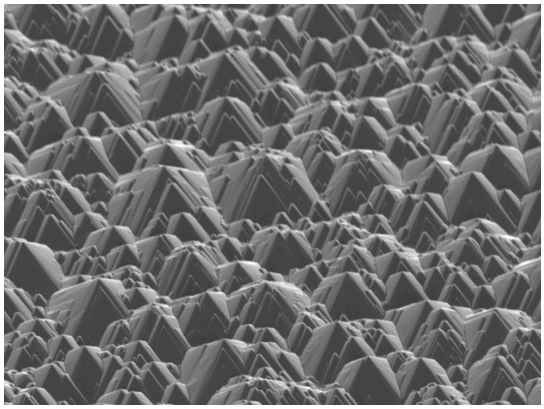
The main losses that have to be tackled for such a solar cell are:

- Recombination losses at the different interfaces, reducing the Voc
- Optical losses preventing a good light absorption in the bulk limiting the J$_{sc}$
- Losses at the carrier transport level, especially when to reach the metal contacts, reducing the Fill Factor (FF)

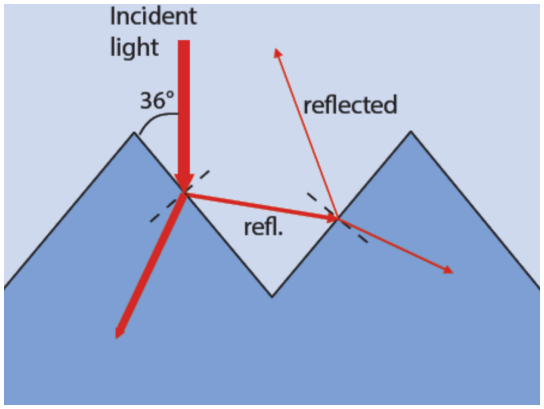
To tackle the recombination losses, especially present at the interfaces, and ensure a good passivation quality, a pretreatment is often needed. The amorphous silicon layer is currently the most sensitive step regarding these impurities and some improvements are possible. Indeed, currently in our group, some cleaning cycles in acid baths are performed in order to reduce as much as possible the defect density at the c-Si surface. Nitric acid (HNO_3) and Hydrofluoric acid (HF) are used and this cleaning process will be detailed in the next chapter 2. The importance of several successive cleanings has been demonstrated within our group and it gives important differences in term of effective lifetimes of minority charge carriers, up to twice longer from 1 to 3 NAOC cycles [18]. Besides that, some impurities can often be introduced during the PECVD process, despite the very low pressure deposition, leading to some serious drops in term of passivation quality. Concerning the optical losses, the wafers used are usually textured in TMAH as mentioned in section 1.5.1 above. This chemical etching towards one specific direction leads to the formation of a layer of pyramids that will allow to trap the light and reduce some reflection losses. The principle of such a texturing can be seen in figure 1.14 below.

Particular attention should be given to these pyramids during the other steps of the Hybrid solar cell fabrication as some chemical treatment can damage them, reducing the light trapping effect and the potential gain in current.

Finally, one important driver to get high-efficiency solar cells is to guarantee a good transport of the charge carriers towards the metal contacts. As we above-mentioned in section 1.5.1, amorphous



(a) SEM image of a TMAH c-Si textured wafer.



(b) Principle of light trapping due to texturing.

Figure 1.14: c-Si textured wafer and light trapping effect [6].

silicon does not present good lateral transport characteristics. However, as in our structure a-Si:H is the front junction, it is necessary for the charge carriers (electrons here) to travel laterally in order to reach the metal fingers and busbars. That is why a TCO is implemented, and it is important to chose a good transparent material in order to avoid some additional optical losses (parasitic absorption, reflection) as well as a material with a good conductivity to facilitate the carrier transport and minimize the negative impact on the Fill Factor.

1.6. Scientific Questions and Structure of the Report

At the end of the previous section 1.5 we highlighted some main drivers that are central in order to reach high-efficiency c-Si heterojunction/poly-Si solar cells. This leads us to 2 main scientific questions that will be considered along this report through analysis and experiments:

- Can we find another pretreatment method allowing to achieve a good passivation for SHJ a-Si:H based solar cells?
- Can we reduce the sheet resistance of the ITO layer in Hybrid solar cells, without losing in light absorption?

The first question aims at improving the current pretreatment method in order to obtain even better effective lifetimes for the minority carriers and thus a better passivation quality, as well as simplifying this method currently time-consuming and not very convenient.

The second question deals with an optimization of the recipe used during the TCO deposition. Currently – and as explained more in detailed later in chapter 4 – 75 nm of Indium Tin Oxide (ITO) is deposited by sputtering under low pressure. The current sheet resistance of such a layer, that should be as low as possible in order to get a good lateral transport, is in the range of 100 Ω/□ (Ω per square) which is relatively high with respect to some works on other TCO conducted in our group. Reasonable values around 30 Ω/□ seem achievable and would lead to a serious gain in Fill Factor.

In addition to that, the whole process of Hybrid solar cells fabrication has been performed during this thesis in order to fabricate some working devices. Some parts of the process can be more or less sensitive as well as the final characterization of the device. For example, the experience shows that it is difficult to measure one single cell of a wafer (containing around 10 solar cells) without cutting it for an isolation purpose, as some shunt resistance can be induced because of the surrounding cells. This lead us to a final scientific question:

- Can we isolate better the different solar cells on a wafer in order to get a higher shunt resistance without the need of cutting each single cell?

This reports includes 6 chapters. After the current introduction, an experiment setup will be developed in chapter 2. Then, the different results of a thermal oxidation as a new pretreatment method will be presented in chapter 3 followed by the results on ITO optimization in chapter 4. Chapter 5 will present the additional steps of the general process of hybrid solar cells fabrication that can lead to an improvement in shunt resistance. The final chapter 6 of this report will summarize the main conclusions and introduce some outlooks for a further work.

2

Experiment setup

2.1. Flowchart of Hybrid Solar Cells

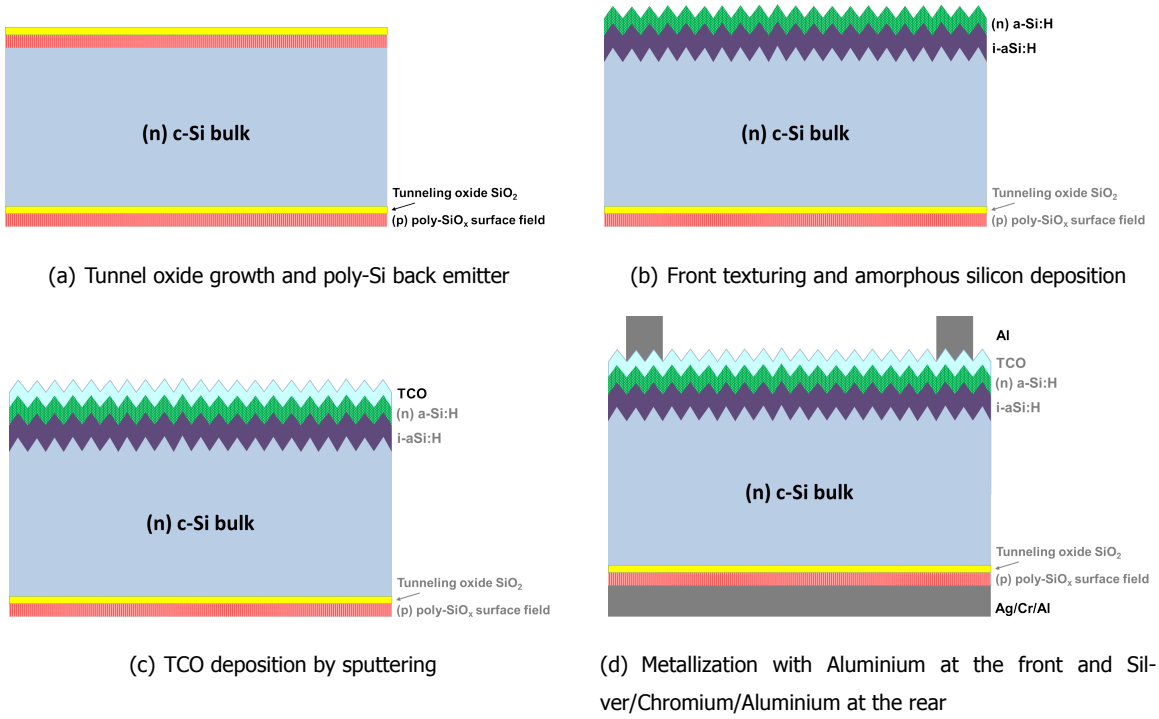
The general process of fabrication of hybrid solar cells is summarized in figure 2.1 below. It leads to the fabrication of Hybrid solar cells according to the structure introduced previously in section 1.5.3 with a rear TOPCon with (p+) poly-Si emitter and a stack of i/n+ a-Si:H as front surface field (FSF) covered with TCO.

- **Tunnel Oxide Growth.**

  The first step of the whole process is the growth of a chemical ultra-thin oxide on top of a [100] flat (n) c-Si wafer for the purpose of creating a barrier for the rear TOPCon contact. One Nitric Acid Oxidation Cleaning – detailed below – and a 0.55% HF bath to remove the native oxide are performed before dipping the wafer during 1 hour in a 69.5% HNO_3 solution at room temperature. This process, called Nitric Acid Oxidation of Silicon (NAOS), allows the formation of a very thin oxide – approximately 1.5 nm thick. This oxide should be kept as thin as possible in order to make the tunnel effect for holes possible but it is difficult to have a good control on it for such small thicknesses. For that reason, thermal oxidation, possible in high temperatures furnaces, does not currently allow us to grow such thin oxides.

- **Poly Silicon Deposition.**

  250 nm of a-Si is then deposited in a furnace on top of the ultra-thin oxide with a Low Pressure Chemical Vapor Deposition process. It will crystallize during the next step to become poly-Si and to be kept at the rear side to play the role of back emitter.



(a) Tunnel oxide growth and poly-Si back emitter

(b) Front texturing and amorphous silicon deposition

(c) TCO deposition by sputtering

(d) Metallization with Aluminium at the front and Silver/Chromium/Aluminium at the rear

Figure 2.1: General process of fabrication of hybrid solar cells.

- **Ion Implantation and annealing.**

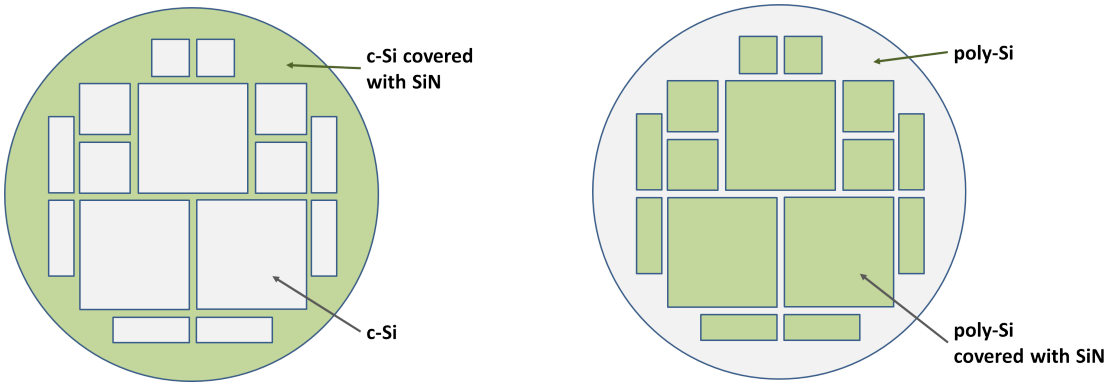
  Boron atoms are then implanted at the rear side, with an energy of 5 keV and a dose of $5{\cdot}10^{15}$ ion/cm^2 in the Varian Implanter E500HP. A 5 min annealing at 950°C in a furnace is then required in order to activate the dopant and crystallize the poly-Si layer.

- **SiN protection and photolithography for patterning.**

  The next structural stage will be the front texturing. However, a few additional steps are needed with the aim of protecting the back side from texturing, which would lead to an etching of the poly-Si/SiO_2. It is possible to deposit some silicon nitride (SiN) through a Plasma Enhanced Chemical Vapor Deposition (PECVD) process in Novellus to act as a protective layer for the back side for the purpose of preventing the texturing to occur. A photolithography step is also added to remove the SiN outside the future solar cells at the back and isolate them as texturing will occur all around. To do so, negative photoresist is coated on top of the SiN. This material changes properties with light: while developing some specific parts under UV light through a hard mask, the photoresist will be open and the SiN can be removed with dry etching under a plasma flow (DRYTEK equipment) or with a wet etching in a BHF bath.

  The same process with positive photoresist is done at the front in order to cover it with SiN around the solar cells for an isolation purpose.

  A plasma cleaning is also done with the TEPLA etcher so as to to remove the photoresist. The wafer is then ready to be textured.



(a) Front side after photolithography.

(b) Back side after photolithography.

Figure 2.2: Front and back sides of a solar cell precursor before texturing.

- **Texturing**

  The wafer is then dipped during 5 min into a TetraMethylAmmonium Hydroxide (TMAH) solution in order to be textured. The $(CH_3)_4N^+$ and HO^- ions will react with the silicon according to the following overall reaction [19]:

$$Si + 2\,(CH_3)_4NOH + 2\,H_2O \longrightarrow 2\,(CH_3)_4N^+ + SiO_2(OH)_2^{2-} + 2\,H_2 \tag{2.1}$$

  This reaction occurs towards the [111] plan and, as the c-Si wafer used has a [100] structure, this etching reaction will create a layer of pyramids of around 5 μm high. This solution does not have any effect on SiN, ensuring a good protection on the parts covered. Finally, this reaction allows the etching of poly-Si where the texturing can take place (outside SiN). At the front, the openings became then textured c-Si.

  After this step, it is possible to remove the SiN at the back thanks to dry or wet etching, as mentioned above.

  A new SiN deposition can be done around the openings on both sides in order to isolate the different solar cells of the future device.

- **Cleaning cycles**

  As mentioned above, at several moments during the process, the wafer needs to be cleaned in an acid bath in order to get rid of some impurities and native oxide. A special cycle called Nitric Acid Oxidation Cycle (NAOC) is used and it consists in dipping the wafer during 10 min in a HNO_3 99% solution at ambient temperature, followed by 6 min of rinsing in deionized (DI) water, then another 10 min dip in a HNO_3 69.5% solution at 110°C followed by 6 min of rinsing in DI water. Finally, a Marangoni cleaning is performed, consisting in a 4 min dip in a HF 0.55% solution followed by 5 min in DI water, so as to remove the surface oxide.

- **Amorphous Silicon Deposition**

  The front side is then ready for a-Si:H deposition on top of the textured c-Si. As discussed in the chapter 1, the quality of this passivation layer is very sensitive to the presence of impurities and an important care is required for cleaning the wafer and the process chambers of the PECVD machine. Thus, 3 NAOC cycles are performed to the wafer while some blank depositions – with the recipe that will be used later – are processed in the PECVD in order to prepare the holders and the chambers and minimize the possible contamination.

  After the last HF bath, the wafer is directly loaded to the PECVD chambers – under vaccuum – in order to avoid the growth of a native oxide in the air environment. The deposition of 4.5 nm of (i) a-Si:H is done at 180°C with silane (SiH_4) and hydrogen (H_2) as gas precursors. It is followed by a deposition of 6 nm of (n) a-Si:H at 180°C in a silane, hydrogen and phosphine (PH_3) gas flow.

- **TCO sputtering**

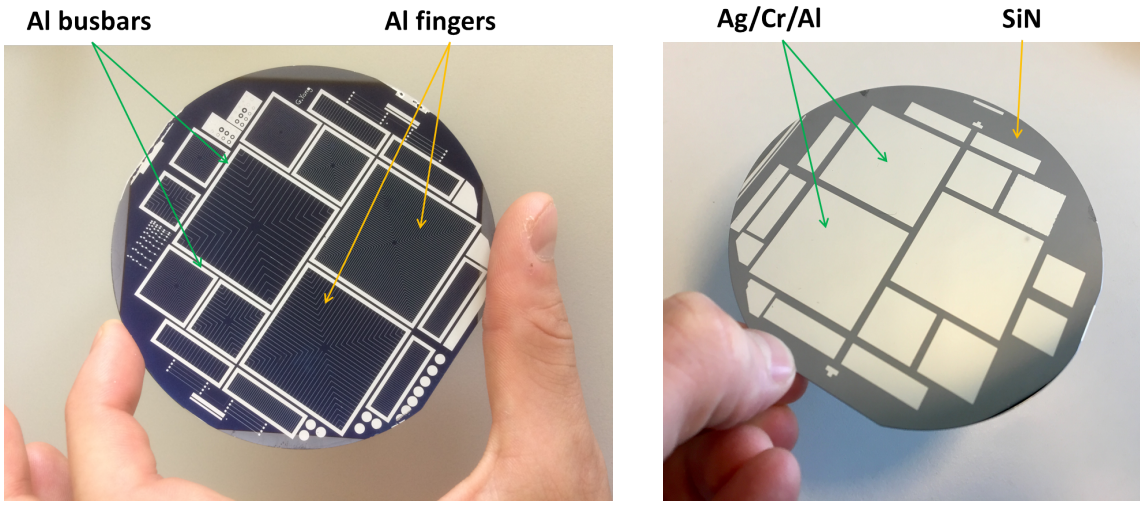
  As mentioned in chapter 1, amorphous silicon does not present good properties in term of lateral transport. A Transparent Conductive Oxide (TCO) is then required as an intermediary to allow the collection of charge carriers at the front metal contact. Such a layer should be transparent in order to let the light be absorbed, and with a good mobility to allow the charge carriers to move laterally and reach the metal. Some process requirements have also to be taken into account, leading to different possible TCOs depending on the situation. Thus, when amorphous silicon is present, the deposition should be done at low and stable temperature. Indium Tin Oxide (ITO) is one of the principal candidate thanks to a good mobility around 20−40 cm^2/Vs and a carrier density around 10^{20} cm^{-3} depending on the film composition and the thickness [20].

  ITO is deposited at low pressure – in the range of $5 \cdot 10^{-4}$ mbar – and the temperature should stay below 180−200°C in order to avoid the crystallization of a-Si:H. With a target of minimizing the reflection at 600 nm, corresponding to the maximal irradiance of the solar spectrum, and taking into account the refractive index of ITO around 1.8, the ITO layer should be around 75 nm thick.

- **Metallization**

  The last step in the fabrication of these solar cells is the metallization, which will allow the collection of the charge carriers and the creation of a current through an external circuit. At the rear it is possible to deposit a full surface area of metal by evaporation. Silver is a good candidate thanks to its low contact resistance with poly-Si compared to any other metal, and to act as a back reflector at long wavelengths [21]. A layer of Aluminium is deposited on top, with a very thin layer of Chromium in between to avoid the formation of AgAl alloy, so as to increase the thickness with a reasonable cost.

Aluminium is evaporated at the front (around $2\mu m$) with a pattern including fingers and busbars. Indeed, the light needs to be absorbed by the semiconductor and the front metal will bring some shading effect, limiting the power output. However, when the finger spacing is too important, losses will come from the front emitter resistivity during the charge carrier transport to reach the metal. A lithography step can be done with a special mask in order to deposit Aluminium only on the fingers and busbars. The results after both front and back metallization can be seen in figures 2.3(a) and 2.3(b) below:



(a) Front side after metallization. (b) Back side after metallization.

Figure 2.3: Front and back sides of solar cells after metallization.

2.2. Characterization Tools for Solar Cells

2.2.1. Lifetime and Implied V_{oc} Measurements

The WCT-120 Sinton instrument has been used in order to determine the effective lifetime of the minority carrier (τ_{eff}) and the implied open-circuit voltage (iV_{oc}) at different stages of the process. The basic principle is based on the emission of an infrared light towards the wafer, changing its conductivity which can be easily measured.

To have access to the lifetime τ, the continuity equation for the excess electron density gives us the following relationship [22]:

$$\tau = \frac{\Delta n}{G - \frac{d\Delta n}{dt}} \tag{2.2}$$

with G the generation rate and Δn the excess minority carrier density.

In case of very short lifetimes, the Quasi-Steady-State (QSS) mode is used and the generation rate is equal to the recombination rate. The previous equation 2.2 becomes:

$$\tau_{QSS} = \frac{\Delta n}{G} \tag{2.3}$$

For lifetimes higher than 200 μs (more relevant for our wafers), the transient mode should be considered with no generation. Equation 2.2 becomes then:

$$\tau_{trans} = \frac{-\Delta n}{d\Delta n/dt} \tag{2.4}$$

The implied open-circuit voltage (iV_{oc}) can also be deducted from the excess minority carrier density:

$$iV_{oc} = \frac{k_B T}{q} \cdot \ln\left(\frac{\Delta n \cdot (N_D + \Delta n)}{n_i^2}\right) \tag{2.5}$$

It is also directly linked to the saturation current density J_0 referring to a high injection of minority charge carriers in the semiconductor:

$$iV_{oc} = \frac{k_B T}{q} \cdot \ln\left(1 + \frac{J_{ph}}{J_0}\right) \tag{2.6}$$

with J_{ph} the photogenerated current density [6]. These 2 parameters will give an information on the recombination losses at high injection: the lower the recombination rate, the higher iV_{oc} and the lower J_0.

2.2.2. Spectroscopic Ellipsometry

In order to calibrate some equipment – such as the PECVD for a-Si:H deposition – or for a characterization purpose, it can be necessary to have access to the thickness of some deposited layers. To do so it is possible to use a spectroscopic ellipsometer. It consists in measuring the change of polarization of a light source after passing through a material. Indeed, the incident light interacts with the material encountered leading to a change in both amplitude and phase of the polarized signal. The complexity of the signals measured usually does not allow to have directly access to the optical parameters such as the thickness or the roughness of the material. Analysis and fitting with existing models should be used instead. The results are acceptable when the material is not too thick (lower than 200 nm). The principle of the measurement is described in the following figure 2.4:

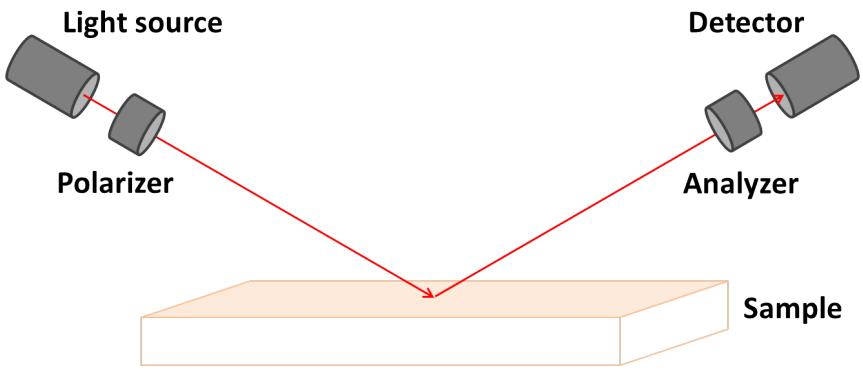


Figure 2.4: Basic principle of the spectroscopic ellipsometer.

For thicker layer (above 200 nm), too many interferences are present and the signal obtained with the above-mentioned ellipsometer is too complicated to fit. It is then possible to use another spectrometer instrument, the ETA-Optik mini-RT. It measures the reflection and the transmission of a light source passing through the wafer whose thickness is unknown. It is then possible to fit the results with some recorded data and have access to the desired thickness.

2.2.3. Reflection and Absorption Measurements

As mentioned in chapter 1, the optical properties of TCO are very important as it should not absorb nor reflect light in order to allow it to reach the bulk of the solar cell. It is possible to characterize these 2 parameters thanks to a spectrometer (Lambda 950 UV/VIS, PerkinElmer). This equipment measures the light intensity of a source after passing through the sample of interest, for different wavelengths, and compares it to a reference measurement. The light source is delivered by a Tungsten-Halogen lamp and a Deuterium that will allow to sweep the whole light spectrum (wavelengths between 175 and 3300 nm). After doing a blank measurement as a reference, it gives access to the transmittance of the material analyzed. In the same way, while measuring the light intensity after being reflected by the sample in question we can have access to its reflectance. These measurements give a good insight of the optical properties of the sample, and can also allow to provide the refractive index n, and extinction coefficient k of the material.

2.2.4. Sheet Resistance Measurements

In order to estimate the electrical quality of the TCOs, the sheet resistance (R_{sheet}) is an important parameter. A 4-point probes method is used to have access to the resistivity through 4 collinear points. The two external probes are used as a current source when the 2 inner points measure the induced voltage as presented in figure 2.5 below.

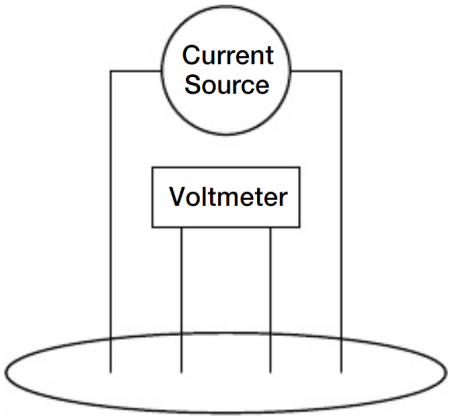


Figure 2.5: Four-Point Probe Resistivity Configuration [23].

This measurement gives access to the sheet resistance (R_{sheet}), an intrinsic value independent of

the size of the sample:

$$R_{sheet} = \frac{\pi}{\ln 2} \cdot \frac{V}{I} \cdot k \qquad [\Omega/\square] \tag{2.7}$$

with I the current source, V the voltage measured and k a correction factor depending on the probes [23]. It is linked with the resistivity ρ of the sample through its thickness t:

$$\rho = R_{sheet} \times t \qquad [\Omega.cm] \tag{2.8}$$

2.2.5. Illuminated J-V Simulator

When the device is finished, it is possible to have access to its external parameters such as the open-circuit voltage (V_{oc}), the short-circuit current density (J_{sc}), the fill factor (FF) and the efficiency (η). To do so, the Wacom illuminated J-V simulator is used. This equipment simulates the solar spectrum (AM1.5, 1000 W/m^2 at 25°C) thanks to a xenon and a hydrogen lamp. The solar cell is placed on a stage under this simulated light source and the J-V curve is obtained for a range of voltages input while varying the load resistance and giving access to the J-V curve of the solar cell.

It is necessary to calibrate this equipment thanks to 2 reference solar cells as the light source can fluctuate a bit and lead to inaccuracies.

A typical J-V curve obtained through this method is presented in figure 2.6 below:

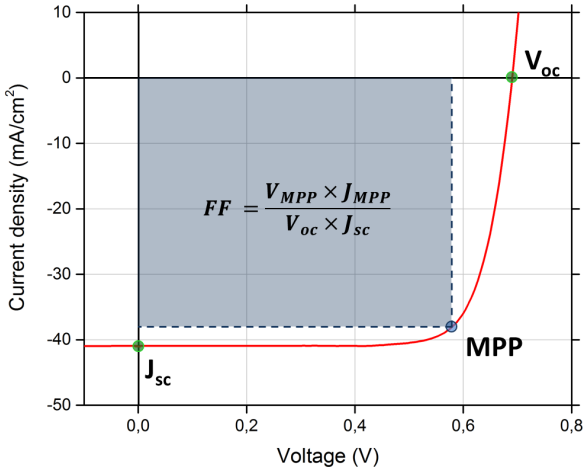


Figure 2.6: Typical JV-curve for a hybrid solar cell.

The short-circuit current density J_{sc} is the maximum current obtained when there is no load applied (short-circuit condition). For Silicon HeteroJunction (SHJ) devices, the current output is mainly driven by the optical properties of the front layers. Indeed the more the light is absorbed in the c-Si bulk, the higher the current is. Thus minimizing the parasitic absorption and reflection of the front layers (TCO and a-Si:H for our particular case) will give a higher current (and J_{sc}). Introducing texturing or

reducing the metal area at the front to reduce shading will also contribute to a better light trapping and lead to higher current densities.

The open-circuit voltage V_{oc} represents the maximum voltage that the cell can deliver when its terminals are not connected (no current density). It depends on the photo-generated current density J_{ph}, assuming that the net current is zero, according to the following equation 2.9 [6]:

$$V_{oc} = \frac{k_b T}{q} \cdot \ln\left(\frac{J_{ph}}{J_0} + 1\right) \tag{2.9}$$

with k_b the Boltzmann constant, T the temperature, q the elementary charge and J_0 the saturation current density. For our hybrid solar cells, parasitic recombination will induce the highest drops in V_{oc}. That is why, as explained in chapter 1, the passivation quality is a key factor to obtain a high output voltage. There is a particular focus in reducing the recombination at the c-Si interfaces (both front and rear) through carrier-selective contacts in order to achieve such high V_{oc}. Impurities and defects will bring recombination centres and thus should be reduced as much as possible.

The maximum power point *MPP* corresponds to the point where the product $J \times V$ (power output) is maximal. It gives access to the Fill Factor FF and then the overall efficiency η of the device:

$$FF = \frac{V_{MPP} \times J_{MPP}}{V_{oc} \times J_{sc}} \tag{2.10}$$

$$\eta = \frac{V_{oc} \times J_{sc} \times FF}{P_{in}} \tag{2.11}$$

with P_{in} the incident power per unit area (in W/m^2) arriving on the cell.

The Fill Factor is mainly influenced by 2 parameters: the shunt resistance R_{sh} and the series resistance R_s. Their effect can be drawn in an equivalent circuit of a real solar cell as described in figure 2.7 below:

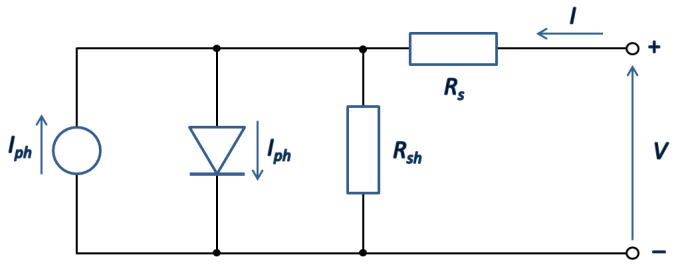


Figure 2.7: Equivalent circuit of a solar cell.

The shunt resistance is mainly due to processing defects as they would induce some secondary circuits preventing the charge carriers to pass through the external circuit. That is why we need a shunt resistance as high as possible to overcome this issue. The effect of the shunt resistance can be seen directly on the J-V curve: the higher the shunt resistance, the more horizontal the J-V curve is around the J_{sc} area.

The series resistance is related to the charge carrier transport. The easier it is for them to travel from the bulk to the external circuit, the lower the series resistance is and the better the output current will be. Thus, for hybrid solar cells, the series resistance is mainly influenced by the conductivity of the bulk, the conductivity of the front surface emitter (or TCO if present) and the contact resistance at the metal interfaces. The effect of the series resistance can be seen directly on the J-V curve: the lower the series resistance, the more vertical the J-V curve is around the V_{oc} area.

These different parameters are strong indicators to characterize the performance of a solar cell and to identify the possible issues/fields of improvement of the solar cell structure of interest.

3

Thermal Oxidation as a Pretreatment for SHJ a-Si:H based solar cells

It has been mentioned in chapter 1 that the quality of a-Si:H passivation is very sensitive to defects and impurities, and a-Si:H deposition requires a robust pretreatment to ensure it. A new method implementing the growth of a thermal oxide is investigating in this chapter to replace the current cleaning cycles.

3.1. Thermal Oxidation of Silicon

With the use of amorphous silicon in the fabrication of solar cells, the Shockley-Read-Hall recombination will play a major role, especially at the Si/a-Si:H interface. In order to keep a good range of lifetime for the minority charge carriers, it is important to reduce the defect density at this interface. So far, three Nitric Acid Oxidation Cycles (NAOC) cleanings were done in our group in order to achieve interesting lifetimes. This method introduces two main issues. First, the long process time – around 2 hours in total – with the need to stay near the wafers during the cleaning for transferring them in the different baths. Besides that, it is important to deposit the amorphous silicon very quickly after these cleaning to prevent a too long contact in the air environment, which would lead to the growth of a native oxide on top of the silicon. It is then not possible to store the wafers after the cleanings, making the whole process of amorphous silicon deposition long and difficult to plan.

Growing a thermal silicon oxide (SIO_2) on top of silicon can be very interesting for the passivation step. Indeed, we will see in this chapter that the growth of this oxide occurs partly under the original surface of silicon. Thanks to the excellent etching selectivity between silicon and silicon oxide it is

possible to get rid of most of the defects present at the surface of silicon. Indeed a dip in a Hydrogen Fluoride (HF) bath will consume the surface oxide according to the following reaction [24]:

$$H_3Si\text{-}OH + HF \rightarrow H_3Si\text{-}F + H_2O \tag{3.1}$$

The H-F molecule is regenerated afterwards and the silicon becomes free of oxide and ready to be processed immediately for amorphous silicon deposition in order to avoid the growth of a native oxide. Together with an expected improvement of the passivation quality (reduction of the surface defect density), it should lead to a simplification of the process as it is possible to grow some oxide on many wafers simultaneously and store them for days before etching them and continuing the process.

When silicon is oxided at high temperature, its volume is expanded as the density of SiO_2 is higher than the one of Si. The oxidation is possible to be conducted under an oxygen flow in furnaces in order to reach high temperatures (usually between 900°C and 1100°C). The silicon is provided by the wafer itself and the oxidation in a dry environment follows the reaction 3.2 below:

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{3.2}$$

It is also possible to consider a wet oxidation with addition of water. In this case, the furnace environment is not filled with a dry oxygen flow, but with a water vapor and the chemical reaction is as follows:

$$Si(s) + 2H_2O(g) \rightarrow SiO_2(s) + 2H_2(g) \tag{3.3}$$

Wet oxidation presents the interest of being much faster, however the silicon oxide features a lower density and it is more difficult to control the oxide thickness making it not optimal for thin oxide layers. That is why the focus of this chapter is on dry oxidation following the reaction 3.2 above.

According to the Deal-Grove model [25], the growth of SiO_2 on top of silicon diffuses inside the original silicon according to the following figure 3.1:

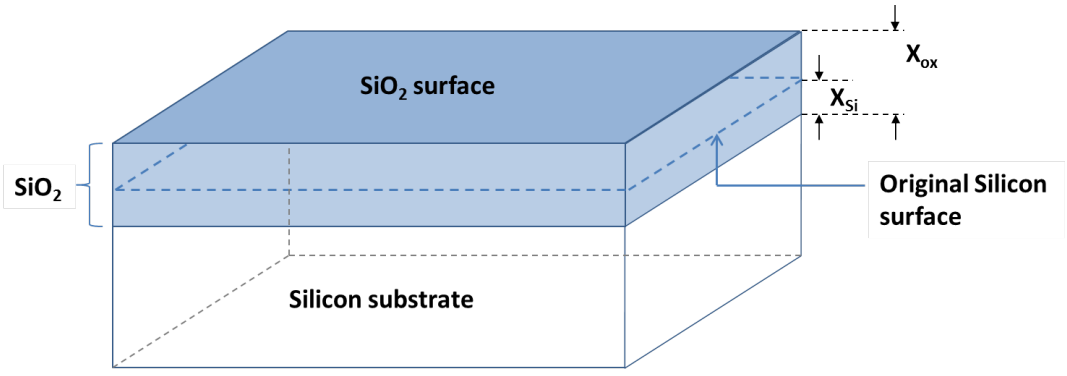


Figure 3.1: Thermal growth of SiO_2 on top of Silicon.

The fraction of oxide grown under the initial surface of silicon is proportional to the ratio between

the densities of Si (N_{Si}) and SiO_2 (N_{SiO_2}). We then have access to the amount of silicon X_{Si} consumed during this reaction:

$$X_{Si} = X_{ox} \cdot \frac{N_{ox}}{N_{Si}} = 0.46 X_{ox} \tag{3.4}$$

Thus, if we grow a 100 nm oxide on top of a silicon wafer, a surface layer of 46 nm of silicon will be transformed in SiO_2. Logically, the thicker the oxide deposited, the deeper it will grow towards the silicon and then the more surface defects will be removed after etching.

3.2. Influence of the Oxide Thickness

3.2.1. Experiments

It is natural to think that we should grow the oxide as thick as possible to get rid of a maximal amount of defects. However, according to the Deal-Grove model, the oxide growth rate is not constant through the oxidation, but slows down with the increase of oxide thickness. That is why it was chosen to study the effect of the oxide thickness – followed by oxide etching and amorphous silicon deposition – on the different external parameters of our wafers (minority carriers lifetime, implied V_{oc}, J_0)

Table 3.1: Oxidation time at 1050°C for different expected oxide thicknesses.

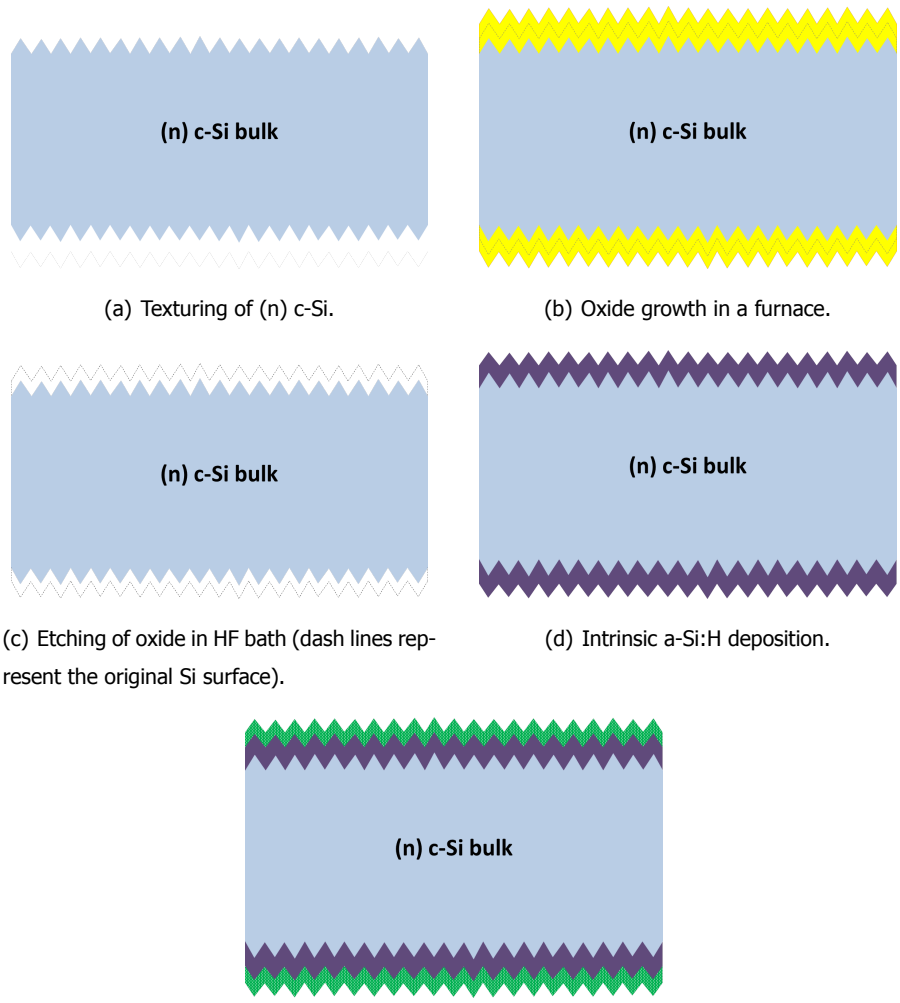
Targeted Oxide Thickness (nm)	**Oxidation Time at 1050°C**
20	9 min, 30 s
40	22 min, 02 s
60	37 min, 34 s
80	65 min, 08 s
100	1 h, 17 min, 42 s
200	3 h, 50 min, 45 s

To test the influence of the oxide thickness on the passivation quality, some oxide with different thicknesses has been grown on both sides of double side textured crystalline silicon wafers. It is possible to store the wafers before the a-Si:H deposition but, just before starting this deposition, it is necessary to remove the SiO_2 layer with a HF dip. The etching rate is proportional to the HF concentration, and for this study a HF bath at 0.55% concentration has been used in order to etch the oxide. The influence of the HF concentration would be interesting to be analyzed as it will change the etching velocity. It will be discussed in the last chapter as an outlook for some future work. Practically speaking, the oxided wafer was placed in this acid bath until it was becoming hydrophobic – meaning that all the oxide is gone away. The indicative etching duration for the different thicknesses are shown in the following table 3.2.

Table 3.2: Etching time of the oxide for different thicknesses

Targeted Oxide Thickness (nm)	Etching Time in BHF 0.55%
20	15 min
40	23 min
60	35 min
80	44 min
100	54 min
200	1 h, 47 min

The different steps of this process with thermal oxidation as a new pretreatrement method are presented in the figure 3.2 below:



(a) Texturing of (n) c-Si.

(b) Oxide growth in a furnace.

(c) Etching of oxide in HF bath (dash lines represent the original Si surface).

(d) Intrinsic a-Si:H deposition.

(e) N-type a-Si:H deposition.

Figure 3.2: Flowchart for Thermal Oxidation Tests

3.2.2. Results

After the a-Si:H deposition, it is possible to measure some external parameters in order to characterize the quality of passivation. All the measurements shown in this chapter have been done after a 30 min annealing at 180°C. First of all, the lifetimes of the minority charge carriers can be measured with the Sinton equipment and the results are presented below:

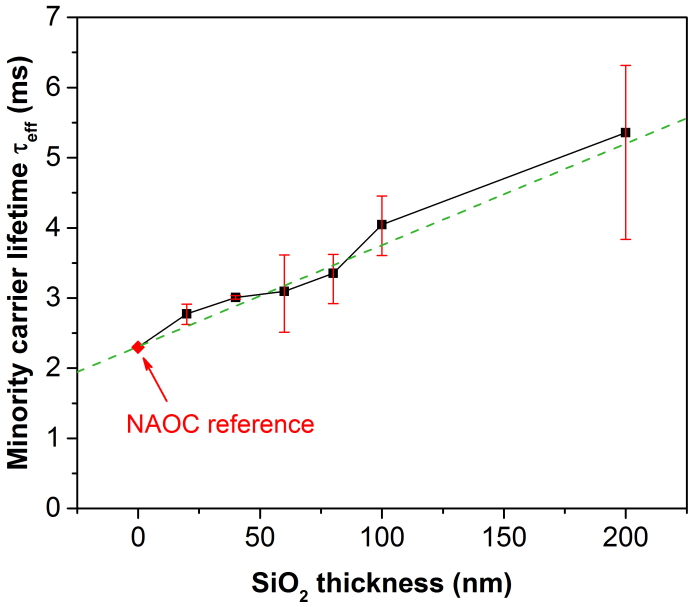


Figure 3.3: Minority carrier lifetime vs oxide thickness.

The reference sample is based on the previous pretreatment method with 3 NAOC cycles for cleaning the wafer. It is noticeable that the lifetime is increased thanks to this new thermal oxidation method, and the thicker the oxide was grown, the better the passivation is. It is related to the important amount of defects that is concentrated at the surface of silicon [26], and then converted into SiO_2 and etch away before the amorphous silicon deposition. The amount of recombination sites is then reduced leading to a higher lifetime. This is confirmed by the saturation current density (J_0), related to the minority carrier lifetime at high injection. The results are shown in figure 3.4 below and it is also correlated to the iV_{oc} (appendix B.1):

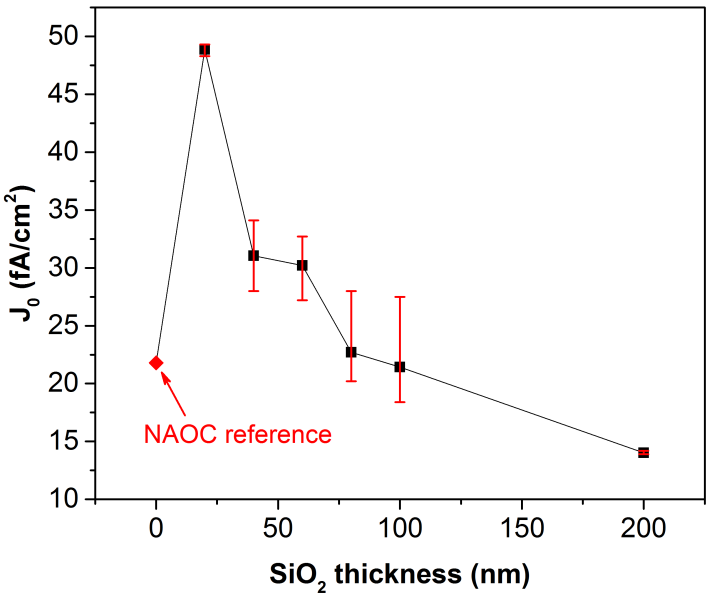


Figure 3.4: J_0 vs oxide thickness.

J_0 gives an information about the recombination at maximum power point and it decreases when the oxide thickness increases. It is logical as with a thicker oxide, it penetrates more under the initial silicon surface, allowing to get rid of more defects after etching. However, we notice that for thin oxide layers (less than 80-100 nm), J_0 is higher than the reference (around 22 fA/cm^2). This observation can be mainly associated with 3 possible reasons.

First, when the oxide is too thin, the amount of Si converted into oxide – 46% of the grown layer according to equation 3.4 – is not important enough and superficial defects are still consequent. The oxidation seems to start playing a major role from 60-80 nm when the amount of superficial silicon segregated from the bulk is sufficient to get rid of a good quantity of defects compared to the NAOC cycles.

Besides that, some recombination centres can also be introduced during the oxidation process. Indeed, when oxide is grown on top of textured silicon, at the tips of the pyramids or between them, some compression or stress can be induced as shown in figure 3.5 below [27]. These forces, most of the time negligible with smooth shapes (such as flat wafers), can play a role with particular shapes, especially with sharp features like pyramids. It can indeed lead to the introduction of lattice defects within the silicon substrate in order to counteract these induced forces, and then recombination sites. This effect would be even more important with a thick oxide as more stress would be induced, however it has to be balanced with the gain from the etching of superficial silicon reducing a lot the surface defect density. As we can reach very low J_0 and high lifetimes with thicker oxides (100-200 nm), this second effect seems to dominate in these situations.

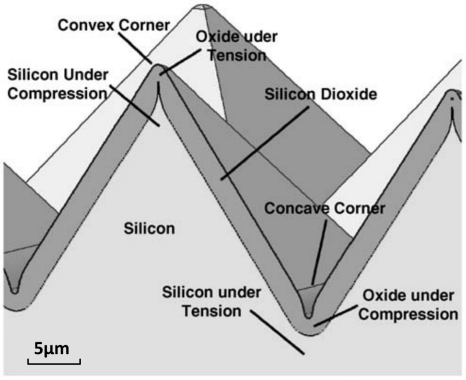


Figure 3.5: Schematic of an oxidized textured silicon surface illustrating the stresses induced [27].

Finally, the etching reaction can induce a negative effect to the textured surface. Indeed, despite the good etching selectivity between SiO_2 and Si, when hydrogen fluoride (HF) reacts at the oxide interface a temporary H_3Si-F molecule is formed and while breaking the Si–O bonds near the c-Si surface, some defects can be introduced. This is especially the case around the tips of the pyramids where the contact surface with the HF solvent is more important. The main risk is a ”rounding effect” when the tips of the pyramid are rounded and less sharpened. Light trapping can then be reduced because of more reflection around the tips, leading to a lower current, and recombination sites can also be introduced in these areas because of lattice defects induced by this rounding effect.

To visually estimate the effect of etching on the texturing quality, it has been possible to observe the textured layer under a Scanning Electron Microscope (SEM). The images before and after etching are presented in figures 3.6, 3.7(a) and 3.7(b) below, for a 20 nm thick oxide on top of a 300 μm textured c-Si wafer:

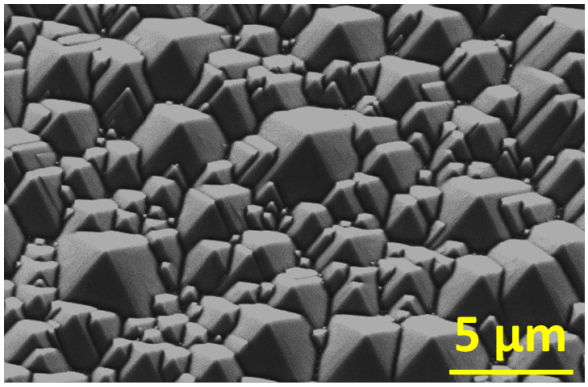
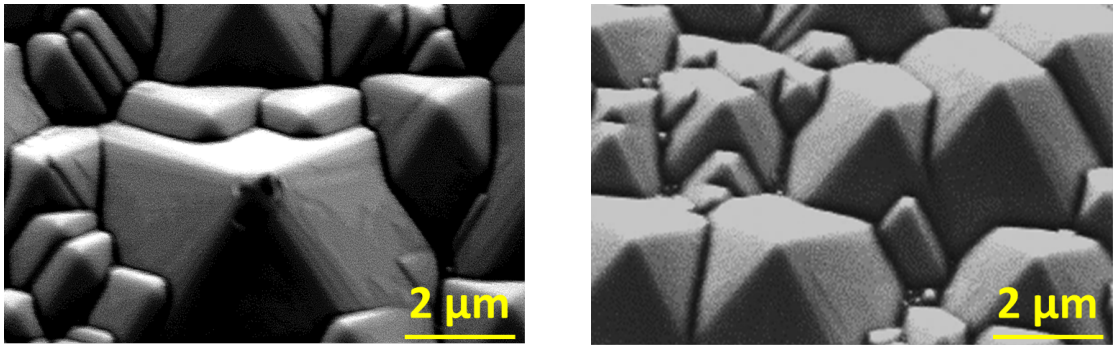


Figure 3.6: SEM image of a textured c-Si wafer after etching of SiO_2.

The result is positive as the pyramids look still quite sharpened and it is possible to compare it with some SEM image of oxided c-Si wafer before etching.



(a) Textured oxide.

(b) Textured silicon after oxide etching in HF bath.

Figure 3.7: SEM images of a textured c-Si wafer before and after SiO_2 etching.

Both images look pretty similar, confirming the fact that, in this case, the HF solution did not bring any significant damage. However, a further possible study could take into account the HF concentration of the etching solution. Indeed, instead of using a 0.55% BHF, it is possible to increase this concentration in order to change the kinetics of the etching reaction 3.1 presented above. We can already imagine that with higher HF concentrations, etching SiO_2 would be faster but the rounding effect would become even more important and thus a limiting factor for our passivation purpose.

3.3. Influence of Temperature

The temperature of the oxidation occurring in the furnace can also play a role on the quality of this reaction. In order to minimize the stress occurring around the pyramids as mentioned in the previous section 3.2.2, it could be interesting to increase the temperature as it plays a role on the diffusivity of oxygen through silicon, which is increased at higher temperatures [28]. The reaction will then be facilitated and faster as the crystal lattice will be more permeable to oxygen. Thermal oxidation of silicon has been achieved for a 100 nm thick SiO_2 layer at 850°C, before etching and a-Si:H deposition (intrinsic & n-type). It is possible to compare the lifetimes and the saturation current density (J_0) with the same experiment done at 1050°C. The results are presented in figure 3.8:

It is clear that the best results are obtained at higher temperature. J_0 is much lower for the 1050°C meaning that recombination at high injection is much reduced, probably because of a better oxidation quality thanks to the improved oxygen diffusion. Further study about the temperature influence is possible, especially for even thicker oxides which present a higher risk of lattice defects, as it will be mentioned in chapter 6.

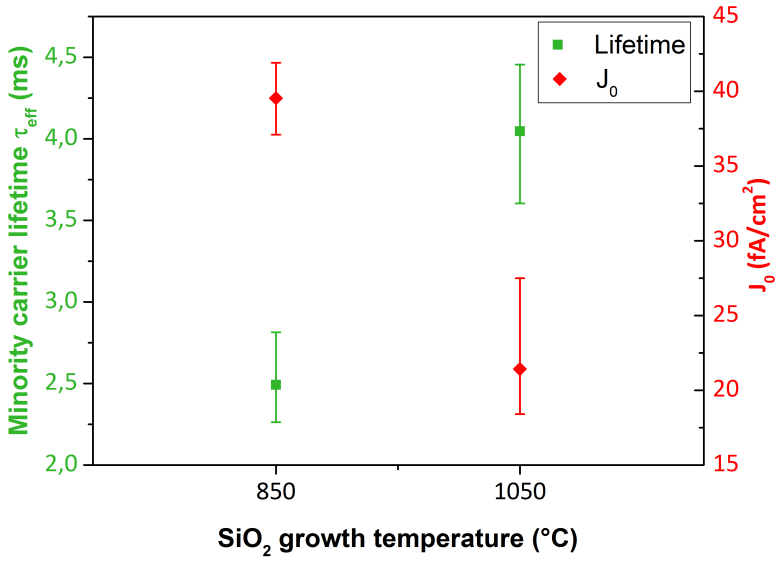


Figure 3.8: J_0 and lifetime vs oxide thickness.

3.4. Possible Implementation in Hybrid Solar Cells Process

When this process will be operational, it will be possible to integrate it in the hybrid solar cell fabrication process. However, as a-Si:H is only deposited at the top of the solar cell precursor some precautions need to be taken especially to preserve the rear passivated contact poly-Si/SiO_2. A possible process taking this new passivation step into account is presented in figure 3.9 below:

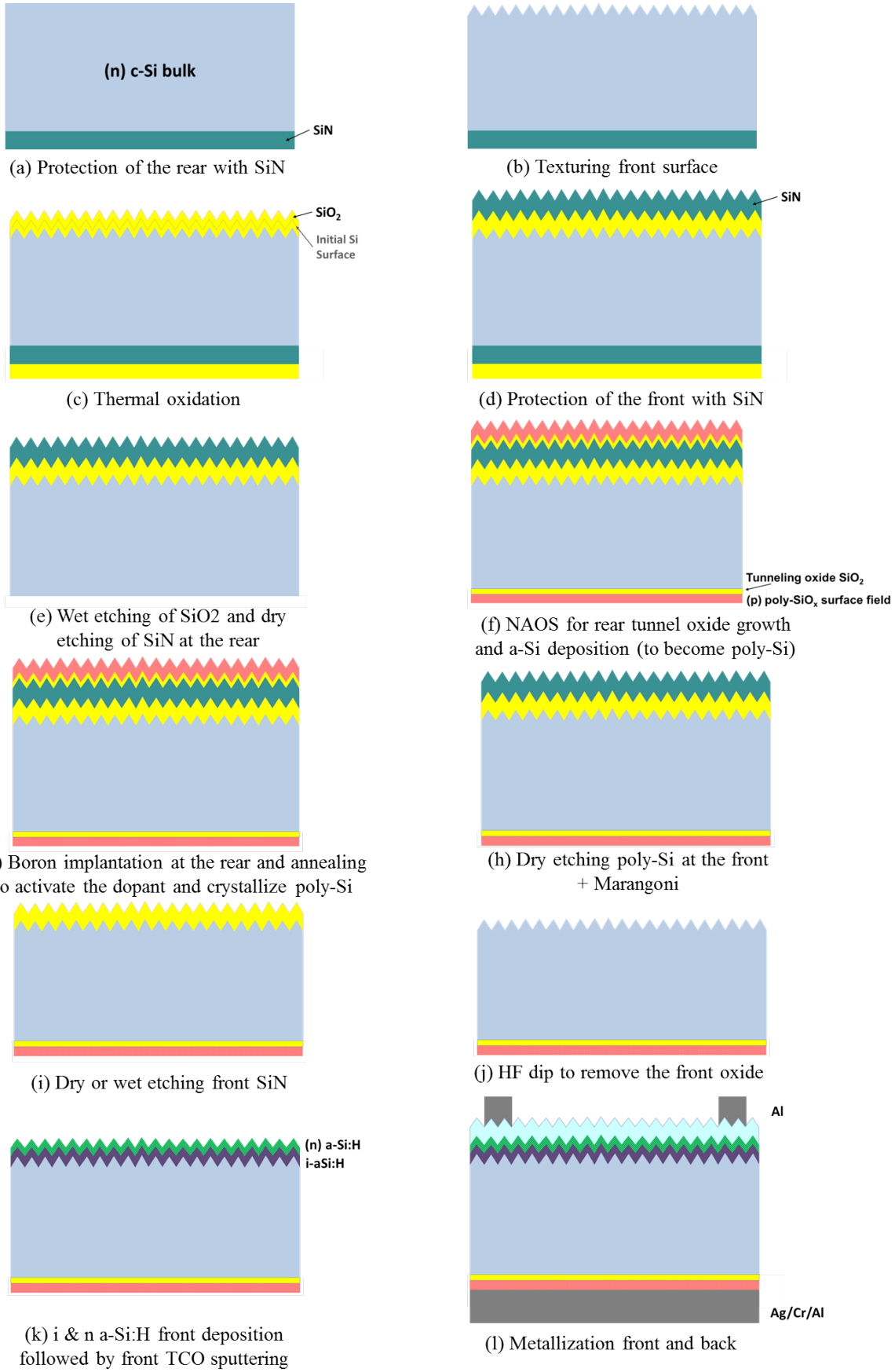


Figure 3.9: Possible flowchart for Hybrid solar cells fabrication with additional oxidation/etching steps.

4

ITO optimization

We saw in chapter 1 that for heterojunction solar cells a Transparent Conductive Oxide (TCO) – such as Indium Tin Oxide (ITO) – is required in order to allow the charge carriers to reach the metal contacts despite the low lateral transport of a-Si:H. This chapter presents a study about optimizing the front ITO layer of a Hybrid solar cell.

4.1. ITO sputtering

ITO is deposited on top of the substrate by sputtering of a ionized gas at low pressure. The general principle of such a process is presented in figure 4.1 below:

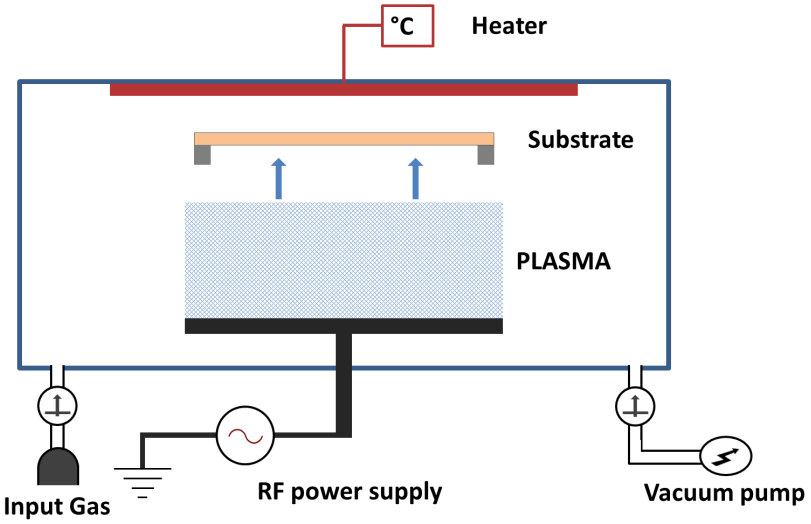


Figure 4.1: Principle of ITO sputtering [29].

The variable parameters that can be adjusted during the process are as follow:

- Heater temperature
- Input gas composition
- Power supplied
- Deposition pressure
- Deposition time

These parameters will influence the ITO thickness as well as the quality of the deposited layer. Dealing with Hybrid solar cells imposes a limit in temperature as a-Si:H can start to crystallize around 180−200°C.

As already mentioned in chapter 2, the sheet resistance R_{sheet} should be as low as possible in order to allow a good charge carrier lateral transport. This parameter gives an information on the amount of free energy states of the ITO: the thicker the layer is, the more free states. Thus, the sheet resistance decreases when the thickness increases as we can see in figure 4.2 below:

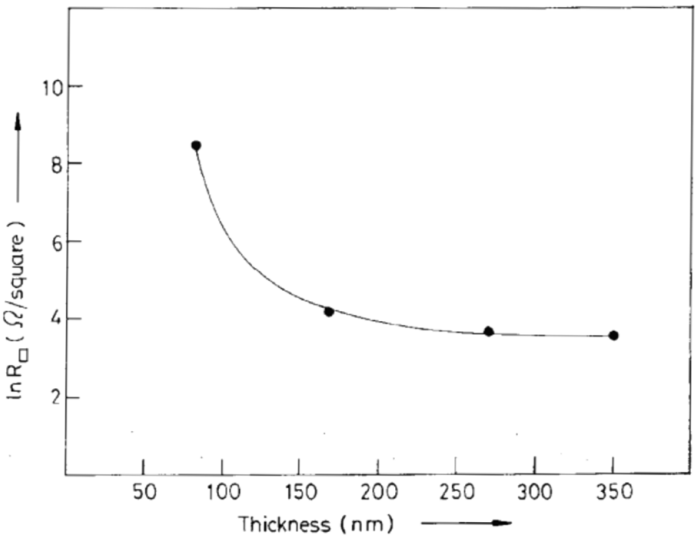


Figure 4.2: Variation of sheet resistance with the ITO thickness [30].

That is why the resistivity of the ITO layer is more interesting to consider as it is directly linked with the sheet resistance and the thickness according to equation 2.8 in chapter 2. Indeed, for an optical point of view, we can not accept a layer too thick as it would have negative effects regarding both reflectance and transmittance.

The current situation in our group uses a 2-steps recipe: first a 10 nm thick ITO is sputtered at a power of 20 W, a pressure of $5 \cdot 10^{-4}$ mbar and a temperature of 110°C, followed by a 65 nm thick ITO layer deposited at 200 W with the same power and the same pressure. The first thin layer acts as

a protective layer, as detailed in the following section 4.2. For a 75 nm targeted thickness, the sheet resistance is in the range of 100 $\Omega/\square$, corresponding to a resistivity of around $7,5 \cdot 10^{-4}\,\Omega$.cm. However, ITO layers with a resistivity lower than $3 \cdot 10^{-4}\,\Omega$.cm have already been developed for heterojunction solar cells [31].

In this chapter, the ITO thicknesses have been measured thanks to the spectroscopic ellipsometer mentioned in section 2.2.2, with 3 measurements done for each wafer: one in the centre and 2 at different corners, giving an information about the uniformity of the deposition.

The sheet resistance has been measured with a 4-probes equipment (section 2.2.4) at 21 different points of each wafer. It gives also a good information on the uniformity of the deposition.

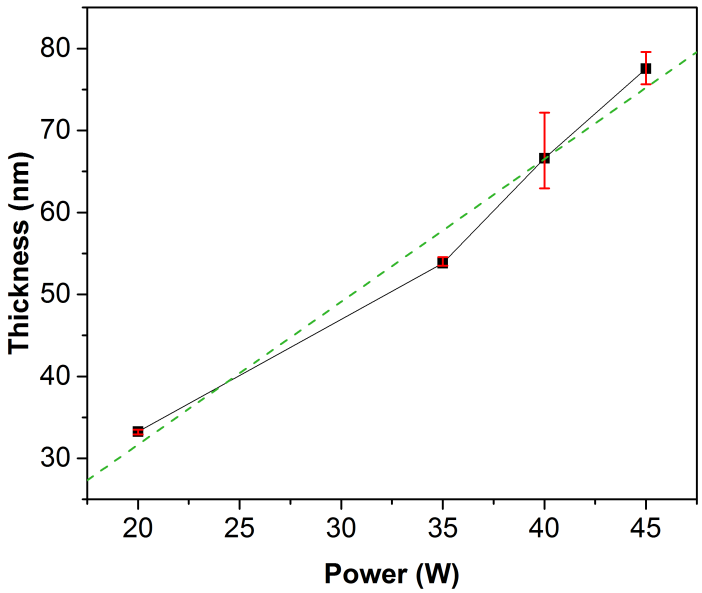
This chapter will mainly focus on optimizing the deposition temperature, as well as the protective layer, in order to reduce the ITO resistivity.

4.2. Protective Layer

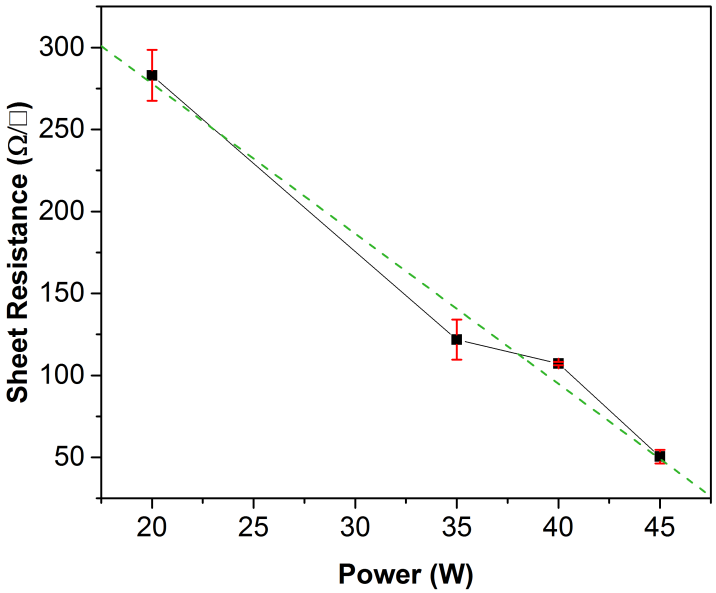
It has been demonstrated that sputtering can cause some damage to the a-Si:H layer under special conditions: the so-called "ion-bombardment" effect [32]. For instance, a too high power will introduce some defects at the a-Si:H surface, reducing the passivation quality and thus the open-circuit voltage (V_{oc}) and the fill factor (FF) [33]. To tackle this problem, it is possible to grow first a thin protective layer under milder condition.

The first question concerns the plasma stability at low power. Indeed, the power will influence the deposition rate: the higher the power, the thicker the layer deposited [34]. In order to introduce milder conditions, it can be interesting to work at a lower power as the deposition would be smoother. Usually, plasma depositions occur in the range of $100 - 200$ W, that is why we can wonder if the 20 W deposition used previously is not too low, preventing a uniform deposition of ITO. Indeed, it is more common to use low powers around 40 W rather than 20 W.

4 samples have been prepared with a ITO deposition on glass at a temperature of 110°C and a pressure of $5 \cdot 10^{-4}$ mbar during 2 hours. The results for the measured thickness and sheet resistance are presented in figures 4.3(a) and 4.3(b) below:



(a) ITO thickness vs deposition power.



(b) Sheet resistance vs deposition power.

Figure 4.3: Low power ITO depositions.

As expected, the higher the power, the thicker the ITO and the lower the sheet resistance. The first remark is that at a power as low as 20 W, the plasma stability seems acceptable. Indeed, both the measured thickness and sheet resistance follow a linear variation with the power, and with a quite good uniformity according to the error bars. However, if the thickness looks even more uniform at low

power, the sheet resistance is a bit less homogeneous. So as to have a more accurate overview of the influence of these 2 parameters, the resistivity has been plotted in figure 4.4 below. It gives indeed an information taking both the sheet resistance and the ITO thickness into account according to equation 2.8.

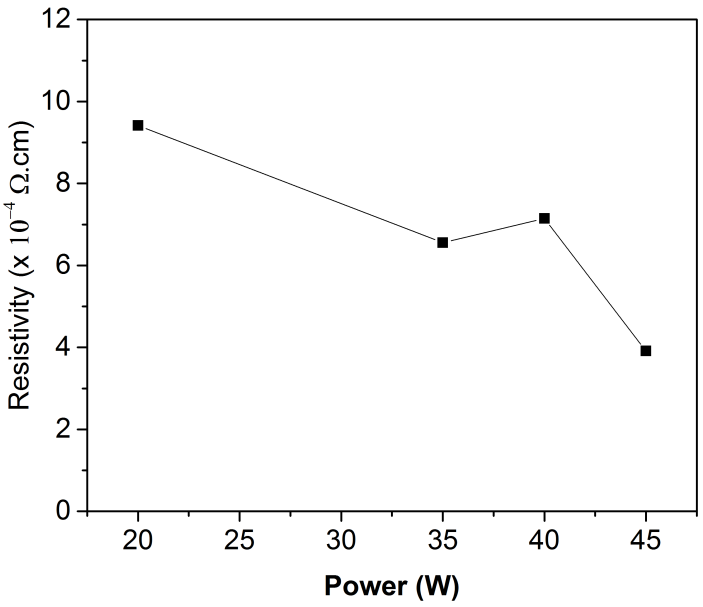


Figure 4.4: ITO resistivity vs deposition power.

We can see that at higher powers the resistivity of ITO decreases. The gain in sheet resistance is indeed more important that the increased thickness induced. For the rest of the study, we will then work in the range of $40 - 50$ W when it comes to the protective layer.

4.3. Effect of Temperature

It has already been mentioned above that it is not possible to process at too high temperatures, because of the presence of a-Si:H, which should avoid to crystallize. However, the impact of the deposition temperature has not been developed yet in our group for such structures, and the current situation uses most of the time a temperature of 110°C for ITO sputtering in case of heterojunction solar cells. As we are still below the limit of $180 - 200$°C when a-Si:H has a high risk to crystallize, it could be interesting to investigate temperatures higher than 110°C, that could indeed bring a positive effect when it comes to minimize the resistivity [35].

A simple experiment has been conducted in the first instance with a 2 hour deposition of ITO at a power of 200 W, a pressure of $5 \cdot 10^{-4}$ mbar and a temperature varying from 110°C to 150°C. The results for the resistivity – obtained thanks to the measured thickness and sheet resistance – are presented in figure 4.5 below:

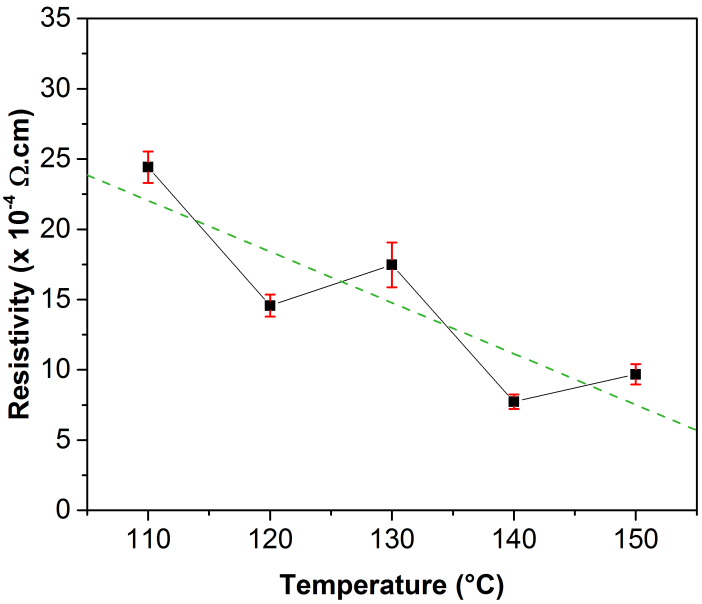


Figure 4.5: ITO resistivity vs deposition temperature.

In that situation, the ITO layer is very thick, inducing some inaccuracies when fitting with existing models during the thickness measurements, even with the ETA-Optik mini-RT instrument. However, the general trend of a decrease of the sheet resistance with an increase in deposition temperature is confirmed with this experiment. We have then a window between 110 and 180°C where we can vary the temperature and find an optimal situation. By experience, 200 W is a high power that could introduce some problem of uniformity. That is why, we will first focus on a power of 100 W for the main deposition (following the protective layer).

For heterojunction solar cells, another approach of protective layer has been analyzed by Aleksandra Gorbatenko for our PVMD group, with a low power deposition (40 W) done together with an increase of temperature from 60 to 110°C. The main purpose of increasing the temperature step by step is to offer some conditions as smooth as possible at the interface a-Si:H/ITO in order to avoid any damage. It is possible to go further in temperature when it comes to deposit ITO after the protective layer, that is why several samples have been prepared with a protective layer at low power and temperature increasing from 60°C to 110, 120, 130, 140 and 150°C, temperature at which the main deposition will occur (power of 100 W). For more clarity, this type of protective layer will be called ”gradient protective layer” in reference to the different steps of temperature increase similar to a gradient of temperature.

All depositions are done with an Argon flow (40 sccm) which will help to carry the ITO towards the target. The different steps for the 130°C deposition are presenting in table 4.1 below.

Table 4.1: Sputtering steps for a 130°C ITO deposition with a protective layer.

Substrate Temperature (°C)	Power (W)	Deposition Time (s)	Comments
60	40	1800	Shutter closed – Pre-sputtering
60	40	100	Protective layer
60	50	200	Protective layer
70	50	200	Protective layer
85	50	200	Protective layer
100	50	200	Protective layer
115	50	200	Protective layer
130	50	200	Protective layer
130	100	2000	Shutter closed – Power ramping up
130	100	2600	Main deposition
130	50	1800	Shutter closed – Power ramping down

The deposition temperature is not directly set but it is the heater temperature that is adjusted through the control software. For the different samples considered, the final deposition temperature was varied, and it was then necessary to adjust the different steps for the protective layer so as to reach the proper temperature at the last step.

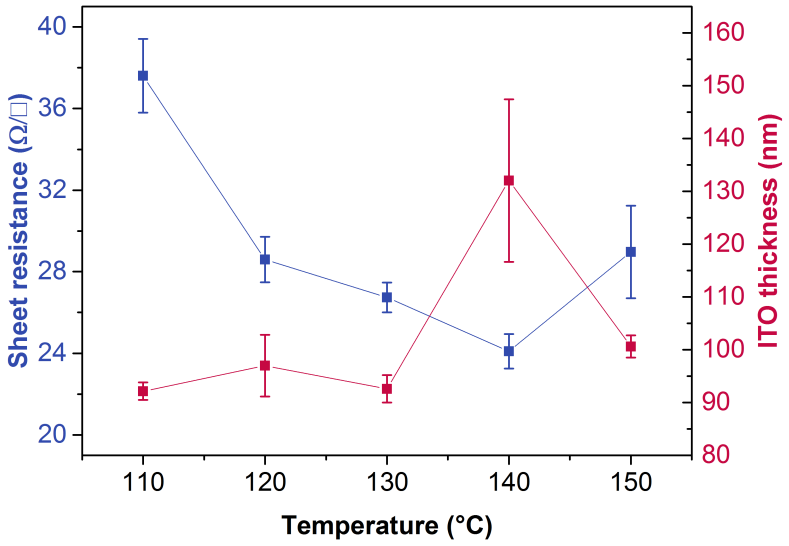


Figure 4.6: Sheet resistance and ITO thickness vs deposition temperature.

The results shown in figure 4.6 above highlight several observations. First in term of sheet resis-

tance, the higher the deposition temperature, the lower the sheet resistance. This is true until 140°C, before observing a rise of the sheet resistance for 150°C. This might be due to a less uniform deposition at higher temperatures. This is confirmed with the thickness measurements also present in figure 4.6 above. Indeed the thickness increases and becomes less uniform for 140°C and 150°C. Besides that, it was visually noticeable that, above 140°C, some relatively important black spots were appearing, especially at the edge of the samples, confirming the problem of uniformity at higher temperatures.

The resistivity for these different samples has been calculated and shows clearly that the optimal process temperature is at 130°C as it can be seen in figure 4.7 below:

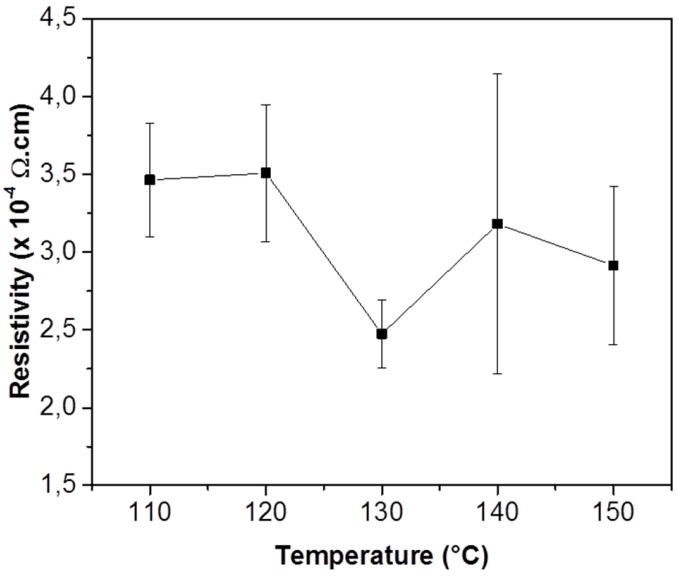


Figure 4.7: ITO resistivity vs deposition temperature.

With an excellent uniformity and three more tests conducted and giving very similar results, the ITO seems to be optimal when deposited at 130°C with a *gradient protective layer*. The resistivity observed is 50% lower compared to the 110°C deposition and even 3 times lower than the previous recipe used for hybrid solar cells in our group. The electrical properties of this layer have then been significantly improved and the better conductivity (related to the carrier mobility [6]) obtained in the ITO should bring a positive effect on the Fill Factor of the final device.

However, the optical properties of such a layer have also to be considered to ensure a good generated current, as we will see in the following section.

4.4. Optical Properties

After having successfully significantly reduced our ITO layer resistivity, it is necessary to verify if its optical properties are still good enough. Indeed, besides the high conductivity (low resistivity) required for the lateral transport of charge carriers towards the metal contacts, the ITO should be highly

transparent with a high transmission and low reflection and absorption, to avoid some optical parasitic losses. Indeed, being the first layer encountered by the light when it reaches the solar cell, the TCO should not prevent the light trapping at the front surface as the maximum amount of light reaching the bulk is required for a high current.

Reflectance and transmittance have been measured for some samples thanks to the Lambda 950 UV/VIS spectrometer (*PerkinElmer*) described in chapter 2. The results for a wavelength sweep between 300 and 1500 nm are presented in figure 4.8 below for 3 different samples: the reference used in the previous process of Hybrid solar cells and two wafers with a *gradient protective layer* (main deposition 110°C and 130°C). The absorbance can also be plotted, and is shown in figure 4.9, as it is linked to both the transmittance T and the reflectance R according to the relation 4.1:

$$I_i = I_t + I_r + I_a \tag{4.1}$$

with I the incident, transmitted, reflected and absorbed light intensity reaching the material of interest. The absorbance A can be then directly obtained for each wavelength thanks to:

$$A = 100 - T - R \tag{4.2}$$

with T and R the transmittance and reflectance.

Note: data of the previous ITO recipe used for Hybrid solar cells are in the range $300 - 1200$ nm.

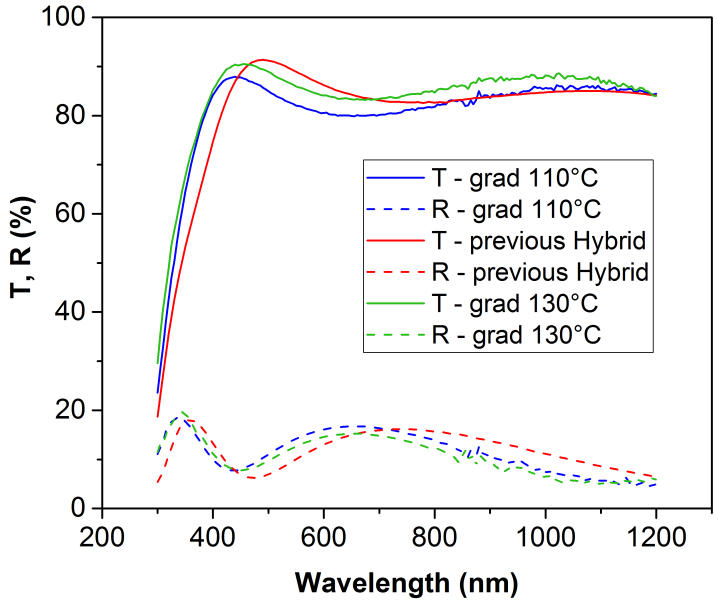


Figure 4.8: ITO transmittance and reflectance vs wavelength for different recipes.

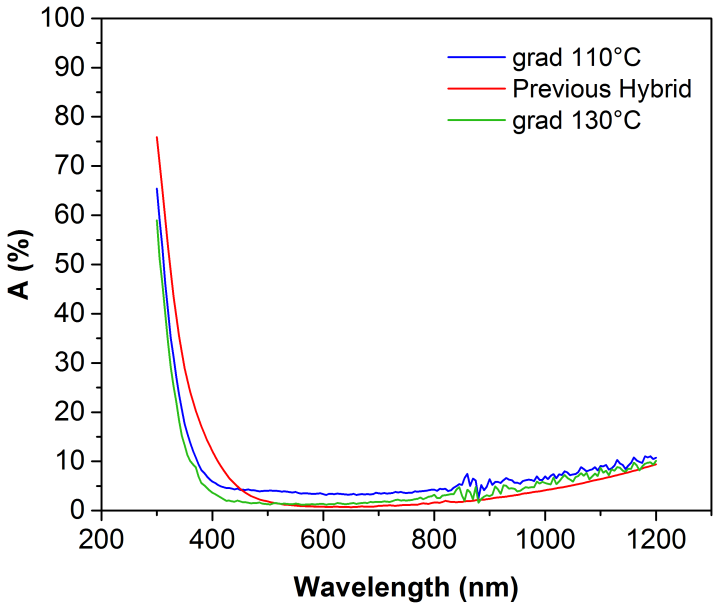


Figure 4.9: ITO absorbance vs wavelength for different recipes.

Both reflectance and transmittance depend on the plasma frequency ω_p, which is the characteristic frequency of electric charges oscillations [36]. The plasma frequency depends on the free charge carrier concentration of ITO (N) according to:

$$\omega_p = e \cdot \sqrt{\left(\frac{N}{m^* \cdot \epsilon_0}\right)} \tag{4.3}$$

with m^* the free-electron mass. A higher plasma frequency will lead to a higher reflection of the incident light, which presents a lower frequency than ω_p. There is therefore a trade-off for the ITO free carrier concentration as the higher it is, the better the conductivity (the lower the resistivity) but the higher the reflectance.

It is clear again that the 130°C deposition gives better results than at 110°C, except for the high wavelengths (higher than 1200 nm) corresponding to a minor part of the solar spectrum. It is also interesting to notice that the deposition at 130°C with a *gradient protective layer* presents similar optical properties, with a better performance for the previous ITO only in the range 500–700 nm. Apart from this small negative difference (not exceeding 3% for the transmittance around 500 nm), the new ITO developed presents even slightly better optical properties, which should lead in a small increase in short-circuit current density (J_{sc}).

To get an even more detailed characterization, the transmittance and reflectance data can be loaded in the SCOUT software (*W.Theiss Hard- and Software*) in order to find a good fitting with some stored models. It is then possible to have access to the refractive index n and the extinction coefficient k for a

certain range of wavelengths. These parameters contribute to the complex refractive index $\bar{n}$ according to the following equation 4.4 below, which give a complete information about the optical losses [37].

$$\bar{n}(\omega) = n(\omega) + i \cdot k(\omega) \tag{4.4}$$

with i the square root of -1.

With these inputs, the material properties in the model are adjusted until the best fitting is reached, as we can see in the following figure 4.10. It is then possible to extract all the optical properties of the material analyzed, such as the n and k coefficients. The values obtained for our best sample (130°C) and the previous recipe used are shown in figures 4.11 and 4.12 below.

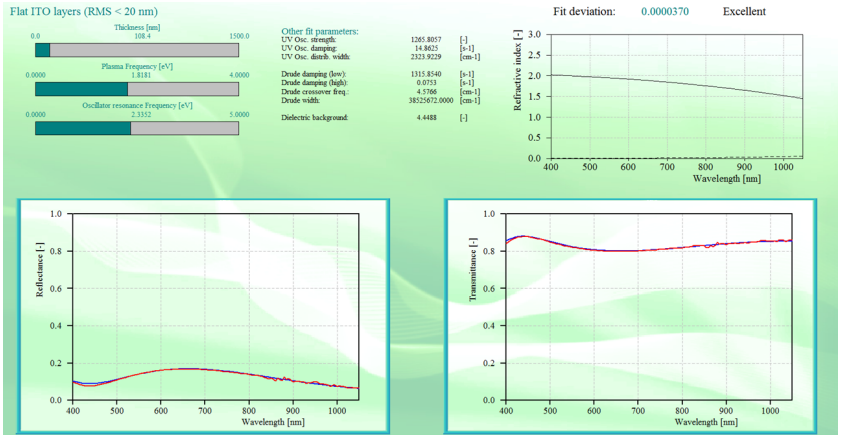


Figure 4.10: Fitting of transmittance and reflectance with existing models through SCOUT software.

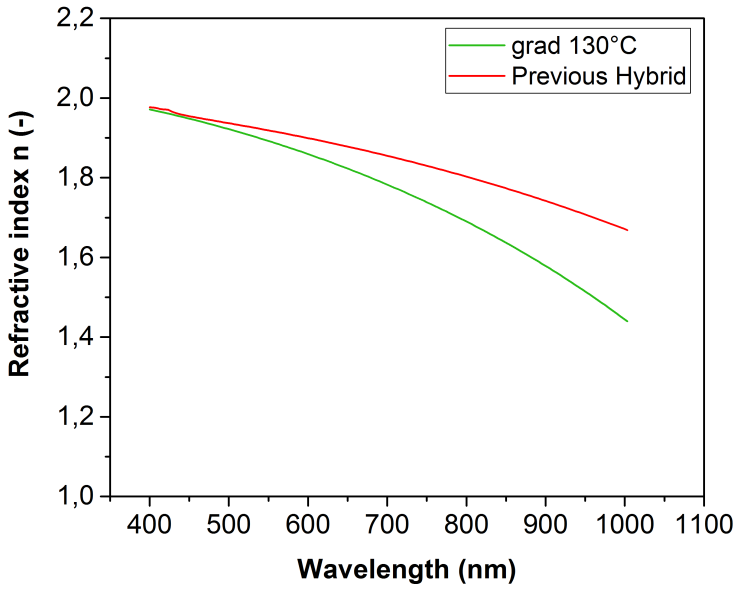


Figure 4.11: ITO refractive index n vs wavelength.

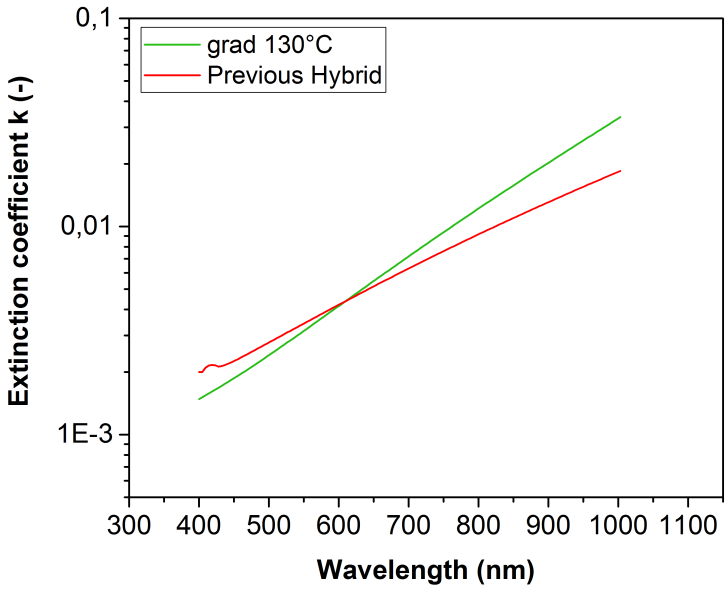


Figure 4.12: Logarithm of ITO extinction coefficient k vs wavelength.

The logarithm of the extinction coefficients k gives similar variation for the new recipe. It is even lower for short wavelengths (below 600 nm) and in the same range as the previous ITO for higher wavelengths. The significant drop in refractive index n for the *gradient protective layer* at 130°C leads to an interesting decrease in reflectance, ensuring a good optical performance for this new ITO layer.

The optical properties of the new ITO developed are quite similar to the previous ITO, with some small additional losses in the range $500-700$ nm but some interesting gains elsewhere in the spectrum. The global effect of this new layer is globally very positive as the electrical gain in term of mobility (through the resistivity drop) is very significant.

5

Isolation of Hybrid Solar Cells

5.1. Effect of shunt resistance

Shunt resistance can introduce important power losses to a solar cell device. Indeed, a low shunt resistance will provide some alternative paths for the current, preventing some charge carriers to travel through the external circuit and leading to a serious current drop. These parasitic paths are usually due to manufacturing defects and should be minimal. Indeed, a current leakage would indeed have a negative effect on the Fill Factor, especially in the short-circuit area where the load resistance is low and the shunt plays a relatively more important role, as we can see in chapter 2 with the equivalent circuit of a solar cell (figure 2.7). Reducing these defects is of great importance to obtain a high efficiency working device and a special care should be paid during the different steps of the fabrication process so as to avoid such damage.

As mentioned in chapter 2, an estimate for the value of the shunt resistance of a solar cell can be determined from the slope of the IV curve near the short-circuit current point as we can see in figure 5.1 below. It is possible to demonstrate that shunt resistance is directly linked to the derivative of current respect to voltage at short-circuit condition [6]. The higher the shunt resistance, the less current leakage and the more horizontal the JV curve is around the short-circuit current area.

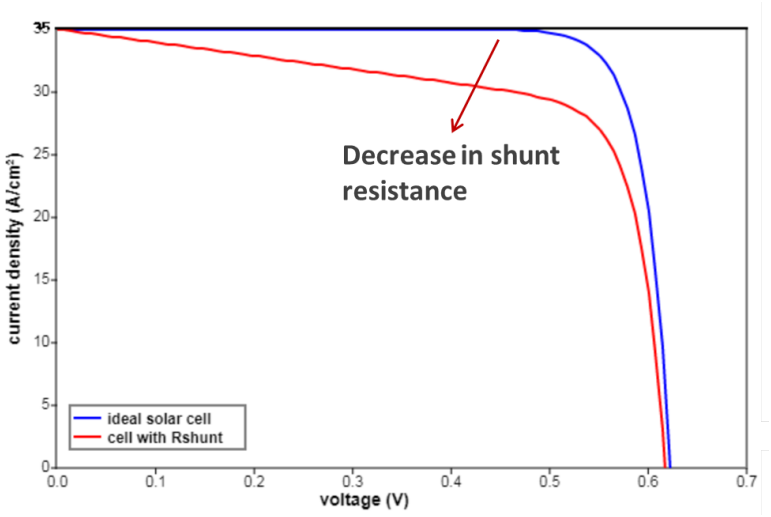


Figure 5.1: Effect of shunt resistance on JV curve [38].

To underscore this shunt resistance effect, we can isolate the power density losses due to the shunt resistance P_{sh} from the power density at maximum power point $P_{mpp,sh}$:

$$P_{mpp,sh} = P_{mpp,0} - P_{sh} \tag{5.1}$$

with $P_{mpp,0}$ the power density at maximum power point without considering any shunt losses. $P_{mpp,0}$ is related to the maximum power point and thus to the Fill Factor FF, the open-circuit voltage V_{oc} and the short-circuit current density J_{sc}. We have then:

$$P_{mpp,0} = V_{mpp} \cdot I_{mpp} = FF \cdot V_{oc} \cdot J_{sc} \qquad \text{with} \qquad FF = \frac{V_{mpp} \cdot I_{mpp}}{J_{sc} \cdot V_{oc}} \tag{5.2}$$

$$P_{sh} = \frac{V_{mpp}^2}{R_{sh}} \tag{5.3}$$

While reorganizing these different equations, we can have an expression of the power density as follows, after taking the shunt losses into account:

$$P_{mpp,sh} = V_{oc} \cdot J_{sc} \cdot FF_0 \cdot \left(1 - \frac{V_{oc}}{I_{sc}} \cdot \frac{1}{R_{sh}}\right) \tag{5.4}$$

with FF_0 the fill factor without any shunt effect. We can see in this equation 5.4 that the fill factor can be rewritten as a "shunted fill factor" FF_{sh} according to:

$$FF_{sh} = FF_0 \cdot \left(1 - \frac{R_{ch}}{R_{sh}}\right) \tag{5.5}$$

with $R_{ch} = \frac{V_{oc}}{I_{sc}}$. We can finally introduce a normalized shunt resistance r_{sh}:

$$r_{sh} = \frac{R_{sh}}{R_{ch}} \tag{5.6}$$

And thus:

$$FF_{sh} = FF \cdot \left(1 - \frac{1}{r_{sh}}\right) \tag{5.7}$$

Equation 5.7 shows us that the higher the (normalized) shunt resistance, the closer to the optimal fill factor the shunted fill factor is. It is an ideality factor in reference to the shunt highlighting its direct effect on the fill factor. An even more accurate empirical expression for the shunted fill factor follows the equation below [39]:

$$FF'_{sh} = FF_0 \cdot \left(1 - \frac{v_{oc} + 0.7}{v_{oc}} \cdot \frac{FF_0}{r_{sh}}\right) \tag{5.8}$$

$$\text{with} \qquad v_{oc} = \frac{V_{oc}}{(nkt)/q} \tag{5.9}$$

In this chapter, we will focus on the first approach, with equation 5.7, as it provides acceptable results in our range of V_{oc} and I_{sc}.

To get rid of the shunt effect, it is usually required to cut the solar cells from a wafer so as to isolate them and prevent some leakage around the edge of the cells. Some recent results of Hybrid solar cells after cutting give the power losses presented in figure 5.2 below for a range of efficiency between 16 and 18%. These 7 cells are 9 cm^2 and from 2 wafers that have been processed at the same time with a different mask design compared to what is used now.

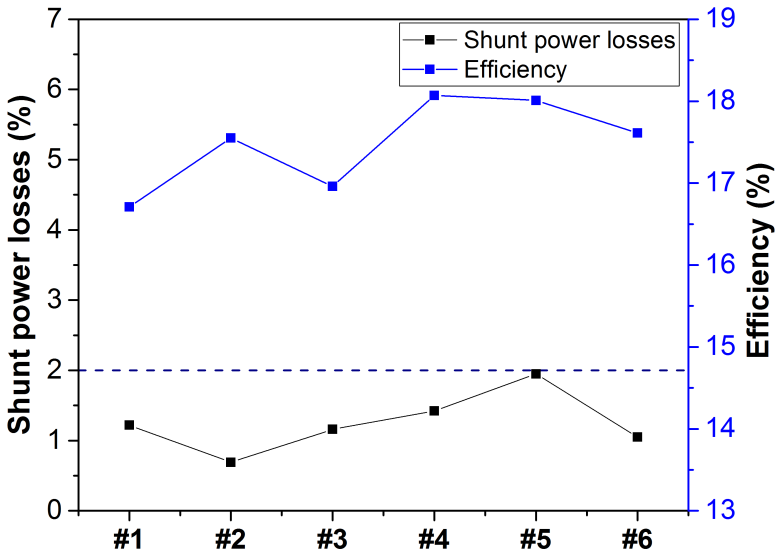


Figure 5.2: Global efficiency and power losses induced by a shunt effect for some Hybrid solar cells.

This values are a good reference as we see that for cut solar cells, the shunt power losses should below 2% and ideally more around 1% to minimize this parasitic effect.

A comparison of this shunt effect before and after cutting the cell for an isolation purpose is presented in table 5.1 below, for a HIT solar cell.

Table 5.1: Shunt losses in HJT solar cells.

	Cell area (m^2)	Fill Factor (%)	Shunt Resistance $(\Omega.m^2)$	Fill Factor losses $1 - 1/r_{sh}$
Shunted cell before cut	0.00078	45.94	0.003117	41.37%
Shunted cell after cut	0.00078	63.87	0.21694	0.82%

The shunt effect can be clearly identified in this situation, as it induces more than 40% losses for a non cut cell, when the same solar cell cut presents less than 1% of shunt losses.

As the cutting step is quite sensitive, with a risk of damaging the cell because of the fragility of such a device, isolating the different solar cells in one wafer would be more practical and would strengthen the robustness of the whole process.

5.2. Patterning ITO and Back Metal

To avoid such manufacturing defects and prevent the charge carriers to use secondary paths, solar cells isolation can be a solution. Indeed, most of these leakages occur at the edge of the cells

Thanks to a hard mask it is possible to deposit ITO and metal locally, with the mask openings corresponding to the future solar cells. The shape of the mask used is presented in figure 5.3, together with the number associated to each cell for the following results.

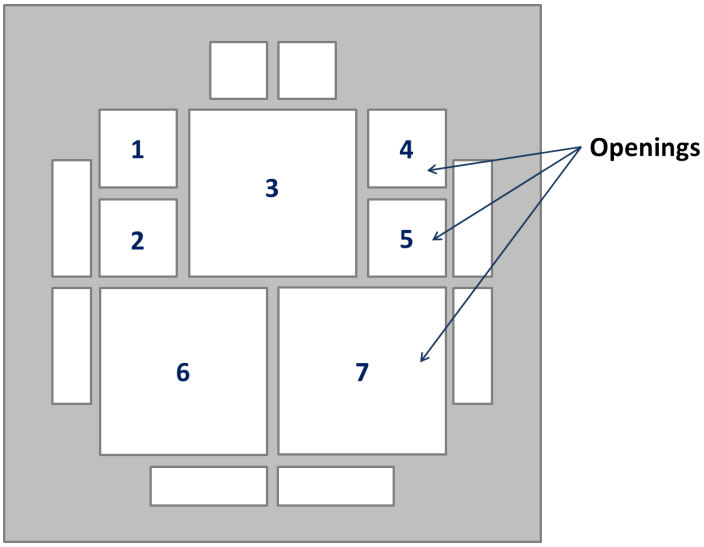
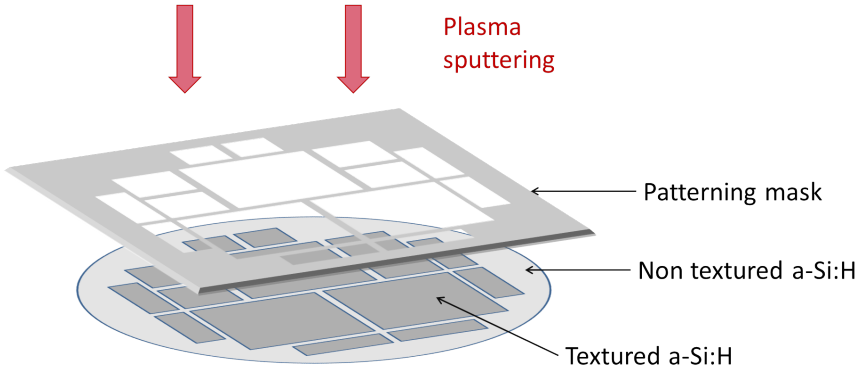


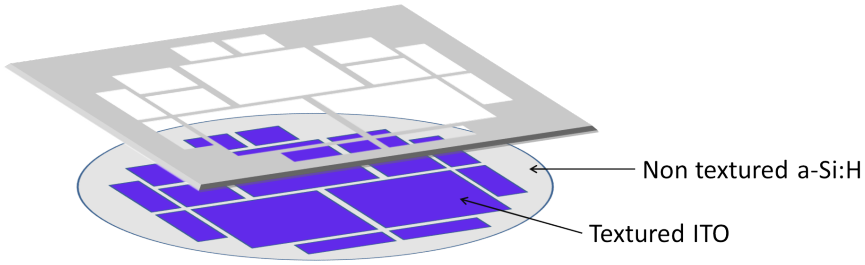
Figure 5.3: Hard mask for metal and ITO patterning.

It is then possible to have a separation between the different cells of one wafer, especially interesting

with ITO and metal that feature the highest conductivities and can then induce more easily some current leakage. The patterning principle is shown in figures 5.4(a) and 5.4(b) below for ITO sputtering, and is similar for metal evaporation at the rear. We can notice that front metal patterning done during the lithography step, when the busbars and fingers appear after a lift-off of photoresist.



(a) During ITO sputtering.



(b) After ITO sputtering.

Figure 5.4: Patterned ITO sputtering of the front side of a Hybrid solar cell.

These patterning steps have been added to the general fabrication process of Hybrid solar cells and the final characterization stage gives access to the shunt resistance of each single solar cells. By varying the load resistance in the Wacom illuminated J-V simulator, it is possible to have access to the output current at low voltage

Usually, the power losses induced by the shunt resistance are around 1% according to equation 5.7. A good target for the isolation is to stay below 2% and the results for ITO and metal patterning are presented in figure 5.5 below:

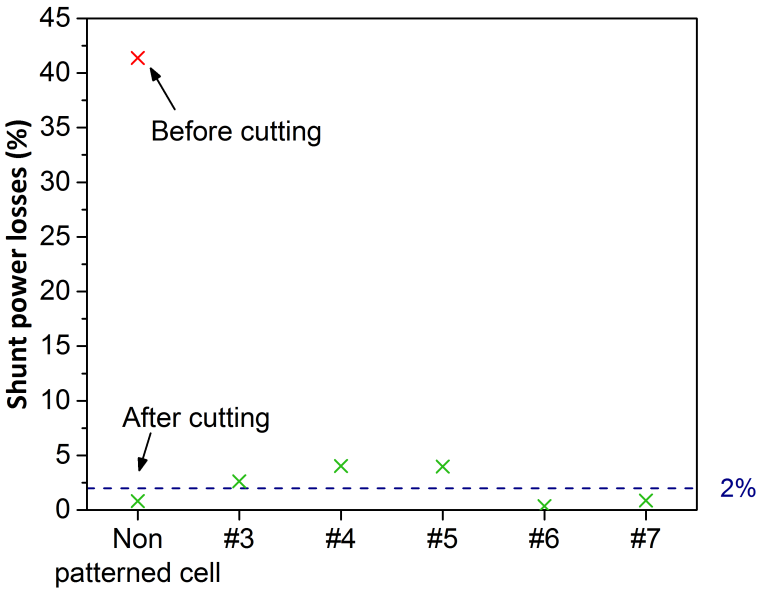


Figure 5.5: Power losses induced by the shunt resistance for different cells of a wafer, with patterned ITO and back metal.

We notice that all measured and calculated values are below 5%, which corresponds to an acceptable shunt loss. It is even better for the large areas solar cells, as two 9 cm^2 solar cells present a shunt power loss of less than 1% when the last 9 cm^2 is around 2.5%. For the smaller cells (4 cm^2) the values obtained are just around 4%, which is a bit too high but come probably from the fact that the alignment between the hard mask and the wafer is not perfect (aligned manually and visually), and this effect is relatively more important for smaller cells.

The external parameters of the measured cells are presented in appendix B.1. The values obtained for the V_{oc} are much lower than expected, most likely because texturing is etching away the poly-Si underneath leading to a high contact recombination.

6

Conclusion and Outlooks

6.1. Conclusions

6.1.1. Thermal Oxidation

A new pretreatment method for the front passivation of Hybrid solar cells has been investigated in this thesis. Currently, in order to minimize the amount of defects at the c-Si/a-Si:H interface, 3 NAOC cleanings and 3 HF dips are performed to the wafers. This is time-consuming and not practical as the a-Si:H deposition should be done immediately after these cleanings to avoid a parasitic native oxide. Growing a thermal oxide on top of c-Si in a dry environment is a promising alternative for this pretreatment step. The SiO_2 layer will indeed partly grow under the original surface of silicon. Thanks to the excellent etching selectivity between c-Si and SiO_2, it is possible to get rid of the silicon oxide in a HF dip. It means that the original c-Si surface has been etched away, reducing considerably the amount of superficial defects.

The SiO_2 thickness has been varied in our experiments, before etching and a-Si:H deposition. A clear trend has been highlighted as when the silicon oxide increases, the lifetime increases while J_0 decreases. Even better results than with the NAOC cleanings can be observed from a 100 nm thick SiO_2 meaning that the amount of defects at the c-Si/a-Si:H interface has been effectively reduced. J_0 below 10 fA/cm^2 and lifetimes above 6 ms can be reached with a SiO_2 in the thickness range of $100 - 200$ nm.

This is even more promising as this method is much more practical than the current situation. It is indeed possible to process up to 30 wafers in the furnace for thermal oxidation. The SiO_2 layer will then act as a protective layer and the wafers can be stored for several days before being etched and processed for a-Si:H deposition.

6.1.2. ITO Optimization

A Transparent Conductive Oxide (TCO) is required at the front side of our Hybrid solar cells as a-Si:H presents a low lateral mobility, preventing a good transport of the charge carriers towards the metal contact. A TCO layer can then be added, with a very low resistivity to counteract this effect. Indium Tin Oxide (ITO) is a common candidate thanks to its good electrical and optical properties. In our group, the ITO layer currently used presents a sheet resistance around 100 $\Omega/\square$ for a 75 nm thickness, which is 3 to 4 times higher with respect to the state of the art [31].

To optimize this ITO layer, it is important to take into account the substrate used. For Hybrid cells, ITO is deposited on top of a-Si:H, and we should avoid to damage this surface as it would reduce the passivation quality. A thin ITO protective layer should then be deposited first, with mild conditions (especially concerning power and temperature). Currently, the deposition temperature never exceeds 110°C, whereas a higher temperature can lead to a lower resistivity. Because a-Si:H is the substrate, the temperature can not be too high to avoid crystallization (starting around 180-200°C). However we demonstrated in this thesis that the optimal deposition leading to a low resistivity and a good uniformity, is achieved with a main deposition at 130°C following a protective layer which includes an increase in temperature by steps at low power. Sheet resistance in the range of $25-30\ \Omega/\square$ has been achieved for 95 nm thick ITO, equivalent to a resistivity as low as 2.4 $\times 10^{-4}\Omega$.cm.

The optical properties of this optimized layer have been analyzed to verify if the gain in conductivity (decrease in resistivity) was not against the light trapping. It revealed that the transmittance is slightly lower than the previous ITO used in the wavelength range of $500-700$ nm, and is higher in the rest of the solar spectrum. The light trapping should remain at a good level and the electrical improvements should lead to an increase in fill factor.

6.1.3. Solar Cells Isolation

When it comes to the whole fabrication process of Hybrid solar cells, it is possible to identify some less robust steps with practical difficulties. For instance, by experience in our group, it is difficult to obtain a non shunted solar cell when it is not isolated. As our solar cell precursors implement usually between 4 and up to more than 10 cells in one wafer. To isolate a single cell before measuring its external parameters, it is then necessary to cut and separate it from the rest. Some alternative current paths are indeed often created through manufacturing defects, especially between the different solar cells of one wafer.

Isolating the different solar cells with special patterning has been investigated for the front ITO deposition and the rear metal evaporation. With such a method, it is possible to reach values of shunt resistance in the range of cut cells, especially for the large area solar cells (9 cm^2) featuring around 1% of shunt power losses. This is already a good decrease, allowing to avoid cutting the solar cells. However, it is possible to reach an even lower power loss (around 0.2%) thanks to an even higher shunt resistance and one option possibly adaptable for this situation is presented in the following

section 6.2.3.

6.2. Outlooks

6.2.1. Thermal Oxidation

Thermal oxidation of silicon showed promising results. It can be completely validated with a better repetition of the experiments, directly related to the a-Si:H deposition very sensitive to contamination. The robustness of this process through a more complete cleaning of the PECVD chambers has already been started to be implemented.

It is also possible for a future study to analyze the influence of the HF concentration for etching, directly linked to the etching velocity. It will indeed have a direct impact on the etching time but also on silicon surface as a too concentrated HF could damage the superficial c-Si as well as rounding the pyramids of the textured layer, leading to a decrease in light trapping. However, if these effects are not too important for some higher concentrations, it can reduce the processing time. One can consider also the use of a high concentrated HF dip to etch away most of the silicon oxide during a shorter time, and the use of a less concentrated HF bath for etching the last nanometers of SiO_2, bringing milder conditions around the c-Si interface.

If the etching can be done faster (with a higher HF concentration), the oxide thickness can be even more increased ($200 - 300$ nm or more) and then a special attention should be paid to the oxidation temperature. Indeed, for thicker oxides, the stress generated around the pyramids (tips, off-peaks) is more important and can generate more significant lattice defects [27]. Lowering the oxidation temperature can reduce these local stresses and thus make a thicker oxide possible to use. Investigating lower temperatures can maybe be beneficial in such a situation.

For thicker thicknesses, it can also be interested to consider wet oxidation, using a water vapor in the furnace instead of an oxygen flow. Even if the silicon oxide is less dense than with dry oxidation, the thicker layers allowed by this process can permit to etch away a thicker superficial silicon and thus a greater amount of defects.

6.2.2. TCO

In this study the protective layer uses powers of 40 or 50 W to ensure a good stability of the plasma. However, the plasma seems to be quite stable also at powers of $20 - 40$ W and it could be interesting to implement a protective layer with the same temperature increase steps, but at a lower power. This could reduce even more the potential damages at the a-Si:H interface.

For the main ITO deposition, after the thin protective layer, it is possible to study the effects of higher powers. Indeed, in this thesis, the power of 100 W was used but power of 200 W are sometimes used in our group, accelerating the process time.

Another promising TCO can also be investigated: Hydrogenated Indium Oxide (IO:H). This material has already proven to have very good electrical properties such as a very high mobility [40]. Combined

with ITO or used alone, its potential is important but it has not been optimized yet in our group for heterojunction solar cells.

Growing a thicker a-Si:H can also be an alternative to the protective layer developed. Indeed, in this case, a part of the a-Si:H deposited could act as a sacrificial layer when sputtering ITO. The desired a-Si:H thickness (6 nm for the final (n+) a-Si:H layer) will be obtained in this case after the ITO deposition.

Finally, the deposition pressure has been kept constant for all the samples considered ($5 \cdot 10^{-4}$ mbar). However, it will play a role on the deposition rate and on the quality of the deposition. A higher pressure usually leads to a faster deposition but it depends on the deposition power and the variation is not linear [41]. While varying the pressure at different powers, it is possible to find an optimal value for an even better mobility.

6.2.3. Isolation of Hybrid Solar Cells

Patterning front ITO and front metal already showed promising results. In order to minimize even more the shunt losses, it is possible to keep on isolating each single solar cell of one wafer. This can also be done before front a-Si:H deposition while covering the surroundings of the future solar cells (outside the opening squares) with an isolating layer such as silicon nitride (SiN). SiN presents indeed a very high resistivity ($10^8 - 10^{15}\Omega$.cm [42]). It is possible to do the same at the back of the cell for the same purpose. A first attempt has already been conducted in this thesis, together with the new patterning process above-mentioned, with shunt power losses as high as 7.4%. This value, lower than some highly shunted solar cells, is quite important and not acceptable compared to the results presented before. This can be due to some alignment issues as well as some problems at the ITO interface that we faced in the end (especially with the lithography step). This SiN isolation remains however a promising feature in our process that could permit to isolate even more each single solar cell of one wafer. The measured external parameters are quite low, especially for the V_{oc} because of an underetching of texturing, touching the poly-Si layer and bringing a high contact recombination.

To solve these issues it could be possible to design 2 different masks with slightly different dimensions in order to prevent this overetching and could also allow to align better the wafer when it comes to patterning.

A

Acknowledgments

After 18 months spent in Delft as a SET Master student, and 10 months within the PVMD group working on this thesis I learned many things, technical skills as well as human experiences. I am glad to have been in a challenging and balanced environment that confirmed my will to work in the energy field and more specifically to deal with solar energy. Besides the excellent technical background gained during this master, the most important remains the priceless human relationships developed in such an open-minded and international context. At the university, in the lab or outside working hours, I had the chance to meet so many different people, and they all brought me something.

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B

Appendices

B.1. $i - V_{oc}$ vs oxide thickness for thermal oxidation study

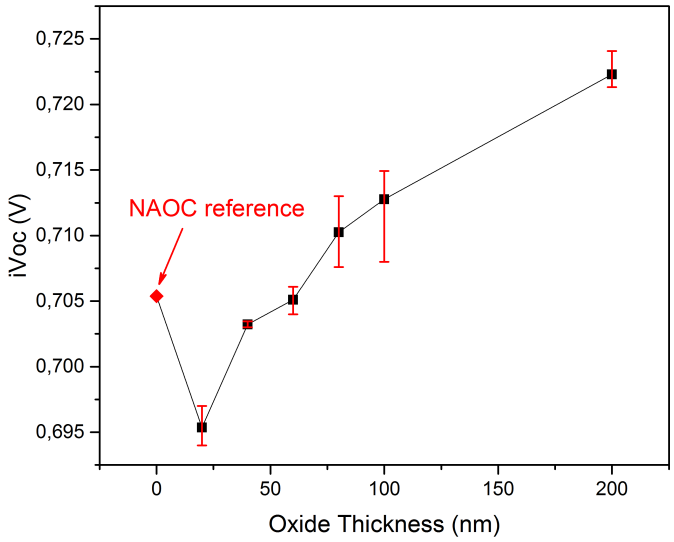

Figure B.1: $i - V_{oc}$ vs oxide thickness.

B.2. External Parameters of Isolated Hybrid Solar Cells

Table B.1: External parameteres of measured isolated solar cells.

	Cell area [m^2]	Efficiency [%]	V_{oc} [V]	I_{sc} [A]	FF [%]	R_{sh} [$\Omega.m^2$]	R_s [$\Omega.m^2$]
DIE3	0.0009	8.27	0.629	0.273	43.29	0.000998	0.000998
DIE4	0.0004	5.38	0.605	0.055	64.67	0.000751	0.000751
DIE5	0.0004	5.43	0.605	0.056	64.60	0.000742	0.000742
DIE6	0.0009	10.99	0.644	0.256	60.11	0.000621	0.000621
DIE7	0.0009	10.52	0.645	0.246	59.83	0.000665	0.000665