Hot qubits in silicon for quantum computation

Eenink, H.G.J.

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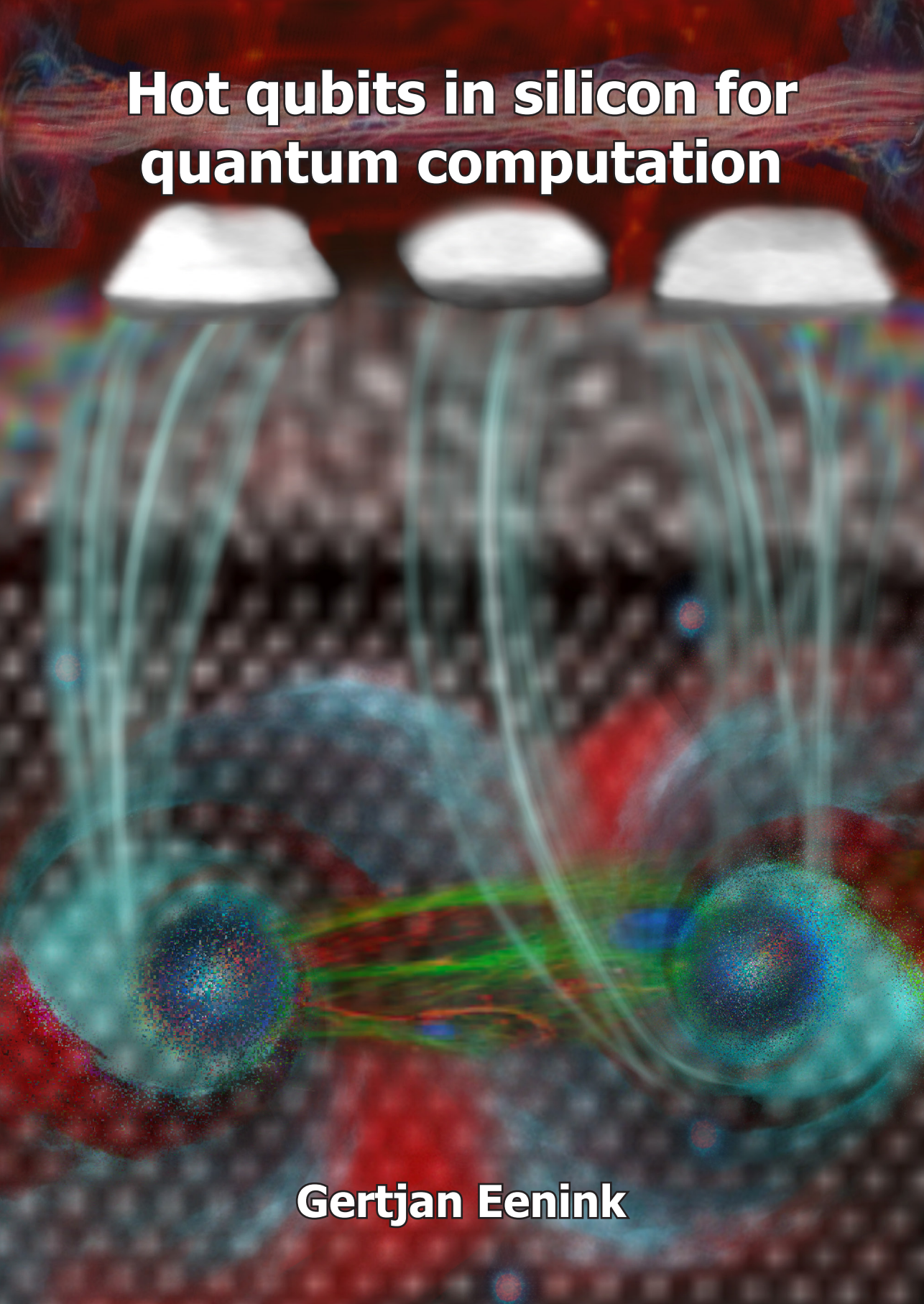
Hot qubits in silicon for quantum computation



Gertjan Eenink

Propositions

accompanying the dissertation

Hot qubits in silicon for quantum computation

by

Harmen Gerrit Johan Eenink

1. Integrated quantum circuits hosting qubits and control electronics are essential for fault tolerant quantum technology. (chapter 4)
2. Spin-lifetime will not define a bottleneck for hot qubit operation with SiMOS. (chapter 6)
3. High-fidelity universal operation can be achieved with hot silicon spin qubits. (chapter 7 and 8)
4. During the NISQ era it is desirable to be able to execute a multitude of native two-qubit gates on a single device. (chapter 8)
5. Multiple qubit platforms should be studied, even if we know which one is most suitable for a large-scale fault tolerant quantum computer.
6. There will be fault tolerant quantum computers built with transistor-like structures, unless this approach turns out to be fundamentally impossible.
7. Setting a daring goal is rewarding, even it turns out to be unachievable.
8. The scientific community would benefit from a diversity that reflects society.
9. Knowing what you don't know is at least as important as all other kinds of knowledge.
10. Reducing media consumption will improve the quality of life.
11. You won't get far if you don't learn from other peoples mistakes.

These propositions are regarded as opposable and defendable, and have been approved as such by the promotors prof. dr. ir. L. M. K. Vandersypen and dr. ir. M. Veldhorst.

Stellingen

behorende bij het proefschrift

Hot qubits in silicon for quantum computation

door

Harmen Gerrit Johan Eenink

1. Geïntegreerde quantum circuits die qubits en aansturingselectronica op dezelfde chip onderbrengen zijn essentieel voor fout-tolerante quantum technologie. (hoofdstuk 4))
2. Spinlevensduur zal geen knelpunt zijn voor hete qubit operatie met SiMOS. (hoofdstuk 6)
3. Hoge-betrouwbaarheid universele operatie kan behaald worden met hete silicium spin qubits. (hoofdstuk 7 en 8)
4. Gedurende het NISQ tijdperk is het wenselijk om een verscheidenheid aan natuurlijke twee-qubit poorten te kunnen uitvoeren op eenzelfde device. (hoofdstuk 8)
5. Meerdere qubit platforms moeten bestudeerd worden, zelf als we weten welke het meest geschikt is voor een fout-tolerante quantum computer op grote schaal.
6. Er zullen fout-tolerante quantum computers gebouwd worden met transistorachtige structuren, tenzij deze aanpak fundamenteel onmogelijk blijkt te zijn.
7. Een stoutmoedig doel stellen is lucratief, zelfs als het onhaalbaar blijkt.
8. De wetenschappelijke wereld zal profiteren van het behalen van een diversiteit die de maatschappij weerspiegelt.
9. Weten wat je niet weet is minstens net zo belangrijk als alle andere vormen van kennis.
10. Het verminderen van media consumptie zal de kwaliteit van leven verbeteren.
11. Je zal niet ver komen als je niet van andermans fouten leert.

Deze stellingen worden opponeerbaar en verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotors prof. dr. ir. L. M. K. Vandersypen en dr. ir. M. Veldhorst.

Hot qubits in silicon for quantum computation

Hot qubits in silicon for quantum computation

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
donderdag 9 september 2021 om 12:30 uur

door

Harmen Gerrit Johan EENINK

Master of Science in Electrical Engineering,
Universiteit Twente, Nederland
geboren te Winterswijk, Nederland

Dit proefschrift is goedgekeurd door de promotoren.

Samenstelling promotiecommissie:

Rector Magnificus,	voorzitter
Prof.dr.ir. L.M.K. Vandersypen	Technische Universiteit Delft, promotor
Dr.ir. M. Veldhorst	Technische Universiteit Delft, copromotor
Onafhankelijke leden:	
Prof.dr.ir. F.A. Zwanenburg	Universiteit Twente
Prof.dr. G.A. Steele	Technische Universiteit Delft
Prof.dr. D.M. Zumbühl	Universität Basel
Prof.dr. J.M. Thijssen	Technische Universiteit Delft
Overige leden:	
Dr. F. Sebastiano	Technische Universiteit Delft

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Contents

Summary

The understanding of quantum mechanics enabled the development of technology such as transistors and has been the foundation of today's information age. Actively using quantum mechanics to build quantum technology may cause a second revolution in handling information. However, to execute meaningful algorithms, large-scale quantum computers have to be built. Such systems are constructed from many qubits, the quantum version of the classical bit. While exciting progress is being made across a range of different qubit platforms, achieving the radical scalability that is necessary to build a large-scale processor could be a roadblock. Huge challenges are put on reproducibility, in- and output connectivity and material quality. Qubits based on the spins of electrons and holes confined in semiconductor quantum dots may have an important advantage in constructing quantum processors. This platform can profit from the advanced semiconductor industry that was responsible for the first computing revolution.

Group IV semiconductors such as silicon and germanium have a high compatibility with industrial semiconductor manufacturing and contain stable isotopes with zero nuclear spin. The materials can be isotopically purified and serve as excellent hosts for spins with long quantum coherence. In Chapter 3 we present quantum dot arrays in silicon metal-oxide-semiconductor (SiMOS), strained silicon (Si/SiGe) and strained germanium (Ge/SiGe). A nearly identical integration scheme based on an overlapping gate structure can be used to define quantum dots in each platform. Each platform has its own opportunities, which are carefully assessed. By employing charge sensing we confirm that all quantum dots can be depleted to the single-electron regime. We compare capacitive crosstalk and find it to be the smallest in SiMOS, relevant for the tuning of quantum dot arrays. Using this cross-platform integration, we can study qubits in each platform with minimal overhead.

Long coherence times, excellent single-qubit gate fidelities and two-qubit logic have been demonstrated with SiMOS spin qubits, making it one of the leading platforms for quantum information processing. However, due to the high disorder at the Si/SiO_2 interface compared to Ge/SiGe and Si/SiGe interface, quantum dots defined in SiMOS are small and achieving sufficient control over single electrons has been a long standing challenge. In Chapter 5 we show experiments on a double quantum dot that can be isolated from its reservoir. We demonstrate a tunable tunnel coupling between single electrons up to 13 GHz and tunable tunnel rates down to below 1 Hz. These results mark an important step towards the required degree of control over the location of and coupling between quantum dots, necessary for the operation of a large array.

To investigate how to build and control such a large array of qubits, we explore the classical-quantum interface in Chapter 4 and determine key challenges that need to be overcome. We propose an architecture for a silicon based quantum

computer processor based on complementary metal-oxide-semiconductor (CMOS) technology combined with SiMOS quantum dots. The result is a dense scalable two-dimensional qubit system based on quantum dot spin qubits, that makes use of transistor-based circuits for control, on which surface code error correction can be implemented. The proposed integration of control electronics critically requires sufficient cooling power. Leading solid-state approaches function only at temperatures below 100 milliKelvin, where cooling power is limited, and this severely impacts the perspective for practical quantum computation. By raising the operating temperature from the conventional milliKelvin regime, different cooling methods with vastly more power become available. This sparks the investigation into the temperature dependence of spin qubits in silicon quantum dots and the development of "hot qubits".

To study the feasibility of these hot qubits, we need to understand the mechanisms behind relaxation and decoherence, as well as their temperature dependence. In Chapter 6 we investigate the influence of temperature and magnetic field on the lifetime of a single-electron spin in a silicon quantum dot. We demonstrate that the spin lifetime T_1 can still be over a millisecond long at a temperature of one Kelvin, providing good prospects for achieving sufficient coherence times at elevated temperatures. We develop a model based on spin-valley mixing and find that having a large valley splitting energy and operation at a low magnetic field can further improve T_1. Additionally, we find a weak temperature dependence of charge noise which shows that qubit operation will only be moderately affected by an increase in temperature.

To demonstrate hot qubit operations we implement spin readout using Pauli spin blockade and use electron spin resonance to drive controlled rotations for two qubits at 1.1 K in Chapter 7 . These experiments show that spin qubits in silicon quantum dots can have sufficient thermal robustness to enable the execution of a universal gate set above one Kelvin. We show individual coherent control of two qubits using CROT gates with a gate time of 660 ns and measure single-qubit fidelities up to 99.3 % using randomized benchmarking. We determine coherence times T_2^* above 2 μs and find a weak temperature dependence, which predicts a robustness against the elevated operating temperature of hot qubits. From randomized benchmarking of two-qubit operations, we determine a primitive gate fidelity of 86 %. The lower fidelity compared to the single-qubit experiments is attributed to decoherence during the time in which the qubits are idle, which is comparable to T_2^*.

To efficiently execute quantum algorithms within the coherence time, the operational overhead can be reduced by being able to execute multiple native two-qubit gates. We can perform fast CPHASE and SWAP gates by pulsing the exchange interaction between the qubits. Usually, these gates are mutually exclusive, since the SWAP requires an exchange interaction much larger than the Zeeman splitting, while a CPHASE requires the opposite. In Chapter 8 we introduce novel adiabatic and diabatic composite sequences that allow the execution of CPHASE and SWAP gates on the same device, achieving a CPHASE gate in 67 ns and a SWAP gate in 89 ns, despite the presence of a finite Zeeman interaction. From numerical sim-

ulations that include electrical noise we predict control fidelities above 99 % for diabatic CPHASE and composite SWAP gates, even for operation above one Kelvin.

These results contribute to the understanding of relaxation and decoherence in silicon quantum dots and are promising for qubit operation at elevated temperatures. This paves the way for quantum integrated circuits hosting the quantum hardware and their control circuitry all on the same chip, providing a scalable approach towards practical quantum information.

Gertjan Eenink

Samenvatting

Het begrijpen van kwantum mechanica heeft de ontwikkeling van technologie zoals transistors mogelijk gemaakt en was de grondslag van het huidige informatietijdperk. Actief gebruik maken van kwantum mechanica om kwantum technologie te bouwen kan een tweede revolutie in het omgaan met informatie veroorzaken. Echter, om zinvolle algoritmes uit te voeren is een kwantumcomputer op grote schaal nodig. Zo een systeem is opgebouwd uit vele kwantumbits, de kwantum versie van de klassieke bit. Terwijl er indrukwekkende vooruitgang geboekt wordt in vele kwantumbit platformen kan de radicale opschaling die nodig is voor een groteschaal processor een knelpunt zijn. Er worden enorme uitdagingen op reproduceerbaarheid, in- en output connectiviteit en materiaal kwaliteit gezet. Kwantumbits gebaseerd op de spins van elektronen en gaten begrensd door halfgeleider kwantumdots hebben wellicht een belangrijk voordeel voor het realiseren van kwantum processoren. Dit platform kan profiteren van de geavanceerde halfgeleider industrie die verantwoordelijk was voor de eerste computer revolutie.

Groep IV halfgeleiders zoals silicium en germanium hebben een hoge compatibiliteit met standaard halfgeleider fabricage en bevatten stabiele isotopen met nul kern spin. De materialen kunnen isotopisch gepurificeerd worden en dienen als uitstekende gastheren voor spins met lange kwantum coherentie. In Chapter 3 presenteren we kwantum dot rasters in silicium metaal-oxide-halfgeleider (SiMOS), gespannen silicium (Si/SiGe) en gespannen germanium (Ge/SiGe). Een bijna identieke integratiemethode gebaseerd op een overlappende electrode-structuur kan gebruikt worden om in elk platform kwantumdots te definiëren. Elk platform heeft eigen voordelen, welke zorgvuldig beoordeeld worden. We benutten ladingsdetectie om te bevestigen we dat alle kwantumdots tot het enkelelektron regime geleegd kunnen worden. We vergelijken capacitieve crosstalk en constateren dat deze het kleinst is in SiMOS, relevant voor het stemmen van kwantumdot rasters. Gebruik makende van deze platformonafhankelijke integratie kunnen we met minimale overhead kwantumbits in al deze platforms bestuderen.

Lange coherentietijden, uitstekende enkelkwantumbit aansturingsbetrouwbaarheid en tweekwantumbitlogica zijn gedemonstreerd met SiMOS spinkwantumbits, hetgeen het één van de leidende platforms voor kwantuminformatieverwerking. Echter, vanwege de hoge wanorde op het Si/SiO_2 raakvlak vergeleken met de Ge/SiGe en Si/SiGe raakvlakken zijn kwantumdots gedefinieerd in SiMOS klein en het behalen van voldoende controle over enkele elektronen is een al lang bestaande uitdaging. In Chapter 5 laten we experimenten zien op een dubbele kwantumdot die geïsoleerd van zijn reservoir kan worden. We demonstreren een stembare tunnelkoppeling tussen enkele elektronen tot 13 GHz en stembare tunnel snelheden tot onder 1 Hz. Deze resultaten laten een belangrijke stap naar de nodige maat van controle over de locatie van en koppeling tussen kwantumdots zien die nodig

is voor de operatie van een groot raster.

Om te onderzoeken hoe een dergelijk groot raster van kwantumbits gebouwd en aangestuurd kan worden verkennen we in Chapter 4 het klassiek-kwantum grensvlak en bepalen kernuitdagingen die overwonnen moeten worden. We stellen een op silicium gebaseerde kwantumcomputer architectuur voor, gebaseerd op complementaire metal-oxide-halfgeleider (CMOS) technologie gecombineerd met Si-MOS kwantumdots. Het resultaat is een schaalbaar tweedimensionaal kwantumbit systeem gebaseerd op spinkwantumbits begrensd door kwantumdots, dat gebruik maakt van op transistoren gebaseerde circuits voor aansturing, waarop *surface code* foutcorrectie geïmplementeerd kan worden. De voorstelde integratie van aansturingselektronica hangt af van het behalen van voldoende koelvermogen. Vooraanstaande *solid-state* benaderingen functioneren alleen op temperaturen onder de 100 mK, waar het koelvermogen gelimiteerd is, en dit heeft een drastisch effect op het perspectief voor praktische kwantumcomputatie. Door de werktemperatuur te verhogen, weg van het gebruikelijke milliKelvin regime, worden andere koelmethoden beschikbaar met enorm veel meer koelvermogen. Dit is de drijfveer tot onderzoek naar de temperatuursafhankelijkheid van spinkwantumbits in silicium kwantumdots en de ontwikkeling van "hete kwantumbits".

Om de haalbaarheid van deze hete kwantumbits te analyseren moeten we de mechanismes achter relaxatie en decoherentie begrijpen, evenals hun temperatuursafhankelijkheid. In Chapter 6 onderzoeken we de invloed van temperatuur en magnetisch veld op de levensduur van een enkele elektronspin in een silicium kwantumdot. We demonstreren dat de spinlevensduur T_1 nog steeds meer dan een milliseconde lang kan zijn op een temperatuur van een Kelvin, hetgeen goede vooruitzichten geeft voor het behalen van voldoende lange coherentietijden op verhoogde temperaturen. We ontwikkelen een model gebaseerd op spin-vallei menging en vinden dat het werken op met lage magnetische velden en het hebben van een hoge valleischeidingsenergie T_1 verder kan verhogen. Verder laat een zwakke temperatuursafhankelijkheid van ladingsruis zien dat kwantumbit operatie maar matig beïnvloed wordt door een verhoging van temperatuur.

Om operaties op hete kwantumbits te demonstreren implementeren we spin uitlezing gebruik makende van Pauli spin blokkade en gebruiken elektron spin resonantie om conditionele rotaties aan te sturen op twee kwantumbits op 1.1K in In Chapter 7. Deze experimenten laten zien dat silicium kwantumdots voldoende thermische robuustheid hebben om de gelegenheid te geven voor de uitvoering van een universele aansturingsset boven een Kelvin. We laten individuele coherente aansturing zien van twee kwantumbits met CROT poorten met een aansturingstijd van 660 ns en meten een betrouwbaarheid tot wel 99.3 % met *randomized benchmarking*. We stellen coherentietijden T_2^* van boven de 2 μs vast en vinden een zwakke temperatuursafhankelijkheid, hetgeen een robuustheid voorspelt tegen de verhoogde werktemperatuur nodig voor hete kwantumbits. Uit *randomized benchmarking* van tweekwantumbitoperaties vinden we een primitieve aansturingsbetrouwbaarheid van 86 %. De lagere betrouwbaarheid in vergelijking met de enkelkwantumbit experimenten wordt toebedeeld aan decoherentie gedurende de tijd waarin de kwantumbits inactief zijn, welke vergelijkbaar is met T_2^*.

Om efficiënt kwantum algoritmes binnen de coherentietijd te kunnen uitvoeren kunnen we de operationele overhead verminderen door te beschikken over meerdere natuurlijke tweekwantumbit poorten. We kunnen snelle CPHASE en SWAP poorten uitvoeren door het pulsen van de uitwisselingsinteractie tussen de kwantumbits. Meestal sluiten deze poorten elkaar uit, omdat de SWAP een veel grotere uitwisselingsinteractie nodig heeft in vergelijking tot de Zeeman splitsing, terwijl een CPHASE het tegenovergestelde nodig heeft. In Chapter 8introduceren we nieuwe adiabatische en diabatische samengestelde reeksen die de uitvoering van CPHASE en SWAP poorten op hetzelfde kwantumsysteem mogelijk maken, waarbij we een CPHASE poort in 67 ns en een SWAP poort in 89 ns presteren, ondanks de aanwezigheid van een eindige Zeeman wisselwerking. Uit numerieke simulaties inclusief elektrische ruis voorspellen we aansturingsbetrouwbaarheden van meer dan 99 % voor diabatische CPHASE en samengestelde SWAP poorten, zelfs als er boven een Kelvin gewerkt wordt.

Deze resultaten dragen bij aan het begrip van relaxatie en decoherentie van spinkwantumbits in silicium kwantumdots en zijn veelbelovend voor kwantumbit werking op verhoogde temperaturen. Dit baant de weg voor geïntegreerde kwantumcircuits die de kwantum hardware en diens aansturingselektronica op dezelfde chip onderbrengen, wat zorgt voor een schaalbare aanpak naar praktische kwantum informatie.

Gertjan Eenink

1

Introduction

I do not fear computers. I fear the lack of them.

Isaac Asimov

Forty years go, the desire to build a quantum computer started. At that time, computers already played a major role in science which inspired Paul Benioff to construct a quantum mechanical description of the classical Turing machine [1]. Parallel to this important step, Yuri Manin [2] and Richard Feynman [3] independently posed the question whether we need a quantum computer for the simulation of certain physics. Due to the exponentially increasing complexity of classical simulations, it might be possible only on a quantum computer to simulate quantum physics. Today, building a quantum computer remains an enormous technological challenge.

1

1.1. Quantum computing and the challenge of scaling up

To build a quantum computer, we need qubits, the quantum mechanical counterpart of a classical bit. Instead of being limited to a classical 0 or 1 state, qubits can also be in a combination of these states (superposition). A system of multiple qubits can furthermore be in an entangled state, where the state of one qubit depends on the other, meaning mathematically that it cannot be expressed as a product of the states of its components.

Quantum algorithms can make use of superposition and entanglement to allow for a powerful and radically different way of information processing. In principle, N qubits can hold the same amount of information as 2^N classical bits. This exponential increase is achieved by storing information in the entanglement between the qubits [4]. The classical information about the described system has to be extracted in a smart way to make it accessible. To provide a conceptual example, we consider a book containing information we are interested in. When you read one page of a classical book, you learn a piece of the information in that book, and reading all pages one by one gives you all the information in the book. The time it takes to read the whole book, as well as the time to find a certain piece of information in the book scales proportionally with the number of pages. Now suppose you read one page of a quantum book, where the information on the pages is highly entangled. Reading any page by itself will give you a random piece of classical information and will collapse the state of the book. Learning the total content of the book requires obtaining many random pieces of information and also takes time proportional to the number of pages. On the other hand, to extract a certain piece of information you can manipulate the quantum information in the book such that reading a page gives you the particular piece that you want. It turns out that there are quantum algorithms that promise to take significantly less (exponentially less!) time to find the relevant information as compared to finding information in a classical book [5, 7].

In other words, the information in an N qubit system is described by 2^N possible states. This superposition of states has to be transformed to a state which returns the required result with a high probability. Applying appropriate quantum logic gates (for example Peter Shor's factoring algorithm [6] and Grover's search algorithm [7]) causes the state amplitudes to interfere, some are amplified and some reduced such that only a few remain. The result (or distribution of results) then depends on a global property of all 2^N possible states [8]. It should be clear now that quantum computers will only have an advantage for certain types of computation and these algorithms would be used to complement classical computing, not replace it.

The required qubits can be implemented on any quantum two-level system that can be prepared in a coherent superposition of 0 and 1. They have been realised in many systems and materials such as trapped ions [9], superconducting transmon qubits [10], spin qubits in donors [11], NV^- centers in diamond [12] and spin qubits in quantum dots [13, 14]. To be able to program and perform any arbitrary quantum algorithm on this system, a "universal" gate set is required. This sets it apart from (analog) quantum simulators and quantum annealers, which can "only" be used to

study systems that are resembled by the simulator. This universal gate set can be built using only single- and two-qubit gates [15].

1.1.1. DiVincenzo criteria

To give direction to the development of the quantum computer, a set of criteria has been proposed that any type of qubit should fulfil, dubbed the DiVincenzo Criteria [16]. In short, we need a (1) scalable physical system with well-characterised qubits, which can be (2) initialized into a simple fiducial state. To perform computation, we need (3) a "universal" set of gates to manipulate these qubits. The qubits need to have (4) long coherence times and we need to be able to (5) measure the state of each qubit. Two additional criteria are required for long-range links, used for quantum communication and connection of quantum computing modules. We need the ability to (6) interconvert stationary and flying qubits and the ability to (7) transmit flying qubits between distant locations.

While multiple qubit systems meet (the first 5 of) these criteria, the biggest remaining challenge is the requirement of having a *scalable* physical system. This statement was in fact put in as a warning phrase to non-scalable systems [17]. Going from experiments with a few qubits to an arbitrary number puts a huge strain on material and device quality. Additionally, addressing all the qubits with a limited amount of lines requires sophisticated control electronics, as well as in- and output routing [18]. A possible solution is to include local control electronics close to the qubits [19] or on a separate chip [20, 21].

As the field developed, it became clear that long quantum computations will be limited by decoherence of the qubits, and that fault-tolerance will be necessary to achieve reliable quantum computing. The principle is that errors caused by decoherence can be detected and corrected for [22]. Error-correcting codes such as surface codes [23, 24] have been developed to achieve fault-tolerance on two dimensional qubit arrays, combining many imperfect "physical" qubits into a perfect "logical" qubit. When the average error probability per quantum gate is kept below a certain critical accuracy threshold, arbitrarily long quantum computations can be performed reliably [25]. The development towards fault-tolerant quantum computation has been formulated in seven stages by Michel Devoret and Robert Schoelkopf, depicted in Fig. 1.1a [26]. These "complexity" steps go beyond the DiVincenzo criteria for physical qubits to error-correction and logical qubits. To reach these steps, we need many physical qubits. A central goal is therefore to build a large array of qubits, which can be controlled and read out at sufficiently high fidelity, using a limited amount of in- and output lines.

1.2. The promise of silicon

Decades of advancements in the silicon CMOS (Complementary Metal Oxide Semiconductor) industry and the large-scale integration of transistor structures enabled the classical computing revolution. Building a quantum computer from the same material may enable to leverage from the existing industry to scale up to large amounts of qubits. This CMOS compatibility is often put forward as an advantage

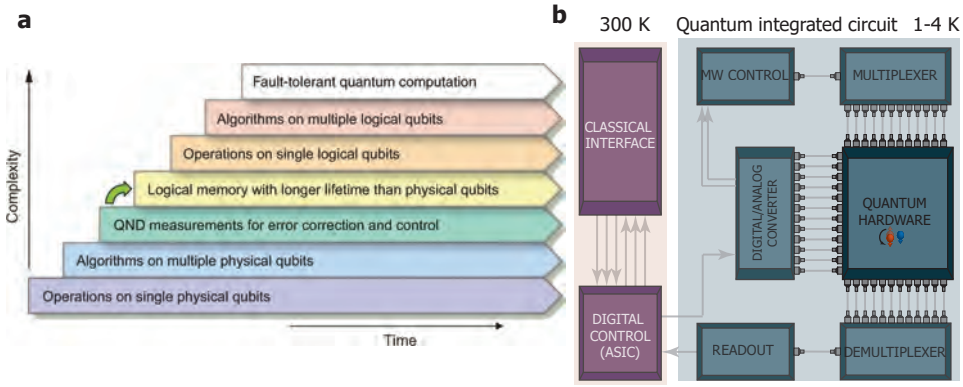

Figure 1.1: **a** The seven stages of complexity in the development of quantum computation. Each step requires full proficiency over the preceding steps. Adapted from Ref. [26]. **b** Quantum integrated circuit as a scalable approach for quantum computation, where the qubits and their control electronics are defined on the same chip. The control functionality that can be integrated is strongly dependent on the available cooling power. When the qubits can be coherently controlled above one Kelvin a broad range of electronics may be integrated, such that communication between room temperature and the coldest stage is limited to only digital signals. Additionally, long-distance spin qubit coupling mechanisms would allow building modular architectures, where widely spaced qubit arrays and local electronics alternate on the same chip, further alleviating fan-out and wiring issues [19].

of any silicon-based platforms. While it is true that many semiconductor fabrication processes can profit from the existing industry, the reality is that this compatibility is often overstated. Translating an academic cleanroom fabrication process to an industrial foundry is far from straightforward. Still, we can capitalize on the respective advantages of both methods. The quick turnaround time and fast feedback cycles of academic processing allow for the rapid development of new methods and proof of principle studies. At the same time, the reproducibility and careful characterisation of the industrial approach serve to standardise this fabrication, and from there scale up. Here lies the strength of parallel development.

Having a qubit technology based on the same underlying principle as transistors enables the integration of control electronics on the same chip [19]. Figure 1.1b conceptually displays a quantum integrated circuit. Inspired by their classical counterpart where only a few control lines are needed to interact with billions of transistors, a quantum integrated circuit hosts the quantum hardware and its electronic control on the same chip to provide a scalable solution [18].

These developments come with a challenge. The operation of these control circuits consumes power and dissipates a significant amount of heat. The cooling power of the dilution refrigerators which keep qubits at their usual operating temperature in the order of $\approx$ 10-100 mK, is quite limited. At higher temperatures (1-4 K), other methods of cooling become available, with vastly increased cooling power. The most simple concept is submersion in liquid helium, which also ensures good heat conduction from the chip. Liquid ^{4}He has a boiling point of 4.2 Kelvin, which can be reduced to 1.3 Kelvin at a reduced pressure using vacuum pumps. Using the more rare isotope ^{3}He reduces these temperatures to 3.2 Kelvin and 0.3 Kelvin

respectively [27].

In those cases, the qubits also need to be operated at these higher temperatures. Thus before we can implement integrated control electronics for industrial large-scale integration of these silicon spin qubits, we need to research how these "hot qubits" behave. Namely, we need to investigate the temperature dependence of readout fidelities, coherence times, and gate fidelities.

1.3. Thesis outline

This thesis aims to provide a feasibility study for the realisation of a quantum computer constructed by advanced semiconductor technology. Chapter 2 starts by introducing theoretical concepts about quantum dots and qubits that are necessary to understand the experiments done in this thesis. In Chapter 3, the fabrication of group IV semiconductor quantum dot devices is explained, and the results obtained in three different material systems platforms are shown and discussed.

Chapter 4 poses a conceptual design for a scalable quantum computer, highlighting key aspects of the design and the importance of uniformity and hot qubit operations. A very suitable material system for this purpose is silicon metal-oxide-semiconductor (SiMOS), as it makes use of the same fundamental materials and processes as standard CMOS. Developments in manufacturing and characterisation can evolve the industry from routinely fabricating millions of room temperature transistors to realising a chip with millions of cryogenic qubits.

The description of experiments on quantum dot devices starts with Chapter 5, which shows the achievement of tunable tunnel coupling between single electrons in SiMOS. This indicates that we have sufficient control over the quantum dots to be able to perform qubit experiments. Chapter 6 builds on this with spin experiments, namely the investigation of the temperature dependence of spin lifetime and charge noise for hot qubits. Chapter 7 extends these experiments to universal two-qubit operations at a temperature above 1 Kelvin and investigates the temperature-dependent qubit coherence.

Finally, Chapter 8 shows the design and implementation of more sophisticated two-qubit gates to increase fidelity and optimize quantum algorithms. The thesis ends by drawing a Conclusion from the previous chapters and providing an outlook on the development of the quantum computer and the role of SiMOS and these experiments within that.

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2

Spin qubits in semiconductor quantum dots

The chances of finding out what's really going on in the universe are so remote, the only thing to do is hang the sense of it and keep yourself occupied.

Douglas Adams

Qubits defined by the spin states of electrons and holes confined in quantum dots define an excellent building block for quantum emergence, simulation, and computation. This chapter reviews the relevant theory of quantum dot and spin physics, used for the experiments in this thesis. The first section describes what semiconductor quantum dots are and how they can be measured. Next, the methods to define, initialize, read and drive spin qubits are discussed. Another section is dedicated to decoherence mechanisms and the effect of temperature. The chapter ends with a comparison of different semiconductor materials and their advantages and disadvantages for spin qubits.

Several review articles are available for more in-depth information [1–3].
This thesis deals with electron exclusively, similar approaches exist for holes [4].

2.1. Semiconductor quantum dots

A quantum dot is a small area (typically a disk about 10 - 100 nm in diameter and often defined in a semiconductor) containing a well-defined number of charges [5]. Electrons in a lateral quantum dot are confined in all three spatial directions and occupy discrete energy levels [6, 7]. Due to Coulomb repulsion, adding an electron requires a charging energy $E_c = \frac{e^2}{C}$, where e is the electron charge and C is the total capacitance of the quantum dot. Tunnelling of electrons to or from the quantum dot is suppressed at low temperatures, where E_c is sufficiently larger than the thermal energy. The number of charges can be added to or subtracted from in a controllable manner, resulting in a well-defined number of charges on a quantum dot. Two or more quantum dots can interact via the capacitative interaction and through the quantum mechanical tunnel coupling [1], where with a strong coupling the electrons are not fully localized anymore.

The quantum dot devices considered in this thesis consist of multi-layer metal gate structures on top of group IV semiconductor substrates. The gates are electrically isolated from the substrate and each other by oxide layers [8]. Applying a positive voltage on the gates results in an electric field that pulls the Fermi level (E_f) above the conduction band energy. Electrons accumulate from reservoir contacts to form a 2-dimensional electron gas (2DEG) in the semiconductor. Confinement in the $\hat{z}$ direction occurs either at the interface of the semiconductor and the oxide (or between the quantum well and the spacer, depending on the material platform used (see section 2.8 and Chapter 3). The potential landscape can be changed by manipulating gate voltages and the 2DEG can be locally depleted, additionally confining the electrons in the $\hat{x}$ and $\hat{y}$ directions. Operated in this way, quantum dots are located under plunger (P) gates, with barrier (B) gates in between them. Manipulation of the P gate voltages then allows for control over the location, electron occupation, energy, and detuning of the quantum dots, while B gates provide additional control over the tunnel barriers between the quantum dots and to the 2DEG reservoir. More details about these material platforms, gate structures, and quantum dot experiments can be found in Chapter 3 and Chapter 5.

2.1.1. Measuring a quantum dot system

Figure 2.1a shows a simplified electric circuit representation of a double quantum dot with a nearby single-electron transistor (SET) charge sensor. Tunable tunnel barriers between the quantum dots and the SET can be controlled by gate voltages. Second-order cross capacitance effects are not displayed. These effects are minimal for SiMOS, (see Chapter 3 for a comparison) and virtual gates can be defined as a linear combination of the physical gates to compensate [9]. The SET is operated in the multi-electron regime. To observe the loading and unloading of single-electrons in the SET, one can measure the current between source (S) and drain (D) to observe periodic Coulomb peaks [5], as depicted in Fig. 2.1b. These peaks show single-electron currents that are spaced proportional to the addition energy E_{add}.

The double quantum dot is usually operated in the few-electron regime. Measuring the charge state without affecting it requires charge sensing [10], as measuring

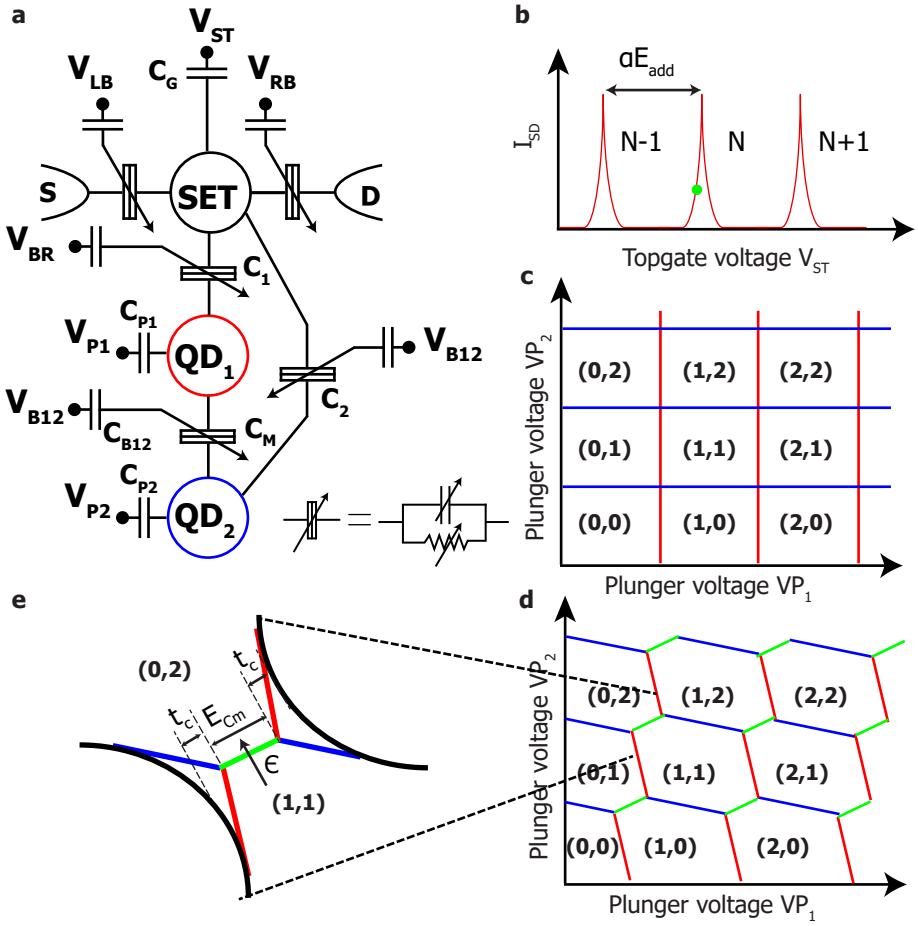

Figure 2.1: **Double quantum dot with a charge sensor. a** Simplified schematic of a double quantum dot (Q_1 and Q_2). Electron occupations and tunnel barriers can be tuned via voltages V_X applied on gate X, capacitively coupled via C_X. The current from source (S) to drain (D) through the single-electron transistor (SET) can be used to measure the electron occupation via charge sensing. Only first-order effects are shown. **b** Current through the SET as a function of top gate voltage (V_{ST}). The peak spacing is proportionally to the addition energy E_{add}. The green dot indicates a suitable position for charge sensing. **c** and **d** Schematics of charge stability diagrams as a function of gate voltage for **c** uncoupled and **d** coupled quantum dots. Red and blue lines correspond to gate voltages where the charge occupations QD_1 and QD_2 change, green lines indicate interdot transitions. The honeycomb structure of **d** is characteristic for a coupled double quantum dot. **e** Zoom in of the two electron interdot transition, indicating mutual capacitance E_{Cm} and tunnel coupling t_c. ϵ marks the detuning axis.

coulomb peaks requires transport of electrons. In charge sensing, we make use of capacitances C_1 and C_2 between the SET and the quantum dots, that couple the quantum dot charge state to I_{dc}. When tuned to a steep flank of a Coulomb peak, as indicated with a green dot in Fig. 2.1b, the current through the SET is highly sensitive to the electric field. As such, the addition or removal of a single-electron

in the quantum dot system results in a large change in current through the charge sensor. To mitigate the effects of drift and cross capacitance, active feedback and virtual gates can be used [9, 11].

Measuring the electron occupancy as a function of gate voltages yields a charge stability diagram. Figures 2.1c and d show these schematically for an uncoupled (c) and a coupled (d) double quantum dot. Solid lines indicate loading and unloading of electrons. Figure 2.1e shows a closeup of an interdot transition for a coupled system. The triple points where the three charge states are energetically degenerate are separated by the mutual charging energy $E_C m$ and the charge addition lines near the triple points are bent as a result of the tunnel coupling t_c. In Chapter 3 we show charge stability diagrams of quantum dot arrays in different materials and Chapter 5 demonstrates control over t_c

2.2. Valley physics

In bulk, the silicon crystal structure has cubic symmetry, which gives a lowest-lying conduction band with sixfold degeneracy [3]. In nanodevices, the four in-plane valleys (belonging to $\hat{x}$ and $\hat{y}$) are lifted to higher energies due to strong confinement, leaving a remaining twofold degeneracy. Strain and electric fields break the inversion symmetry in the $\hat{z}$ direction and the energy difference between the two lowest valleys is labelled as the valley splitting energy E_{vs}. Valley splitting is highly dependent on inversion asymmetry in the material: interface disorder and atomic steps have a large influence. Due to the sharp potential step at the Si/SiO_2 interface, E_{vs} in SiMOS is usually of the order of 0.2 - 0.8 meV [12, 13], while in Si/SiGe values between 0.01 and 0.2 meV are reported [14–17]. Atomic steps at the interface tend to suppress E_{vs} [14, 18], and it can be influenced by the electric field [12, 17] through changing the location of the electron wave function with regard to the interface or by moving the quantum dot over atomic steps. A low E_{vs} has a negative effect on initialisation, readout and control fidelities, and spin-valley coupling can greatly enhance spin relaxation (see Chapter 6). Therefore, the valley splitting should be sufficiently large compared to the electron temperature $k_B T_e$ to prevent a thermal population of the excited valley state [16].

2.3. Electron number

While single-spin qubits make use of a single excess electron [19], this does not strictly require a single-electron quantum dot [20]. Operating quantum dots in the multi-electron regime even holds certain advantages over the single-electron regime, such as a lower susceptibility to charge noise [20–22], faster driving [23] and a higher and more easily tunable tunnel coupling. Electron shell filling of silicon quantum dots can be understood from Fock-Darwin energy levels, where spin $(\uparrow, \downarrow)$ and valley $(v_+, v-)$ give the multiplicity of each orbital state in a two-dimensional quantum dot [23]. A completely filled shell is assumed not to influence operations [24]. Quantum dots containing 3 [25], 5 (Chapter 7 [26]) and 13 [24] electrons have been used as qubits. Two qubit operations of a multi-hole quantum dot with unknown occupation were demonstrated in germanium [27]. Charge occupations

containing a single valence electron (1, 5, 13 and 25) were found to be suitable for qubits, where the impact of orbital excitations resulting from dot deformation could be exploited for faster single-qubit control [23].

2.4. Spin readout

Defining a qubit requires a two-level quantum system, such as the spin state of a single-electron, a spin-1/2 particle. This serves as a single-spin or Loss-DiVincenzo qubit [19]. The states are separated in energy by applying a static magnetic field B_{ext} through the Zeeman effect by $E_Z = g\mu_B B_{ext}$, where g is the electron g-factor ($g \approx 2$ in silicon) and μ_B is the Bohr magneton = 9.274*10^{-21}J/t.

To accurately read out spin states, a combination of charge readout with a spin-to-charge conversion method is required. Elzerman readout [28] (demonstrated in Chapter 6) makes use of the difference in tunnel rates of a spin up and spin down electron to a nearby reservoir. The Fermi energy E_f of the reservoir is tuned to lie between the spin ground and excited states, which are split in Zeeman energy by δ_{E_Z}. An excited state electron can tunnel out, while a ground state can not. For optimal readout fidelity, the tunnel rate Γ_R between the quantum dot and the reservoir should be tuned such that $T_1^{-1} \ll \Gamma_R < BW$ and $\delta E_Z \gg k_B T$.

Elzerman readout has several disadvantages. It requires a nearby electron reservoir, which couples noise into the system [29] and is not available for quantum dots in a 2D array [25, 30]. For quantum control it is desirable to operate at a lower magnetic field, to reduce variations in the qubit resonance frequency due to E_Z and to reduce the requirements of microwave sources. To circumvent the interconnect bottleneck, integrated control electronics will be necessary [31]. The required cooling power for these circuits calls for operation at a higher temperature [32] (see Chapter 1), where more cooling power is available (see section 9.2.2). These wishes are incompatible with Elzerman readout.

Readout is also possible by making use of the Pauli-exclusion principle, where the readout is dependent on the energy gap between the antisymmetric singlet configuration and the three symmetric triplet states [33]. The Pauli exclusion principle forbids electrons to make a transition from the T(1,1) to the S(0,2) state, so the triplet states are blocked. The blockade is lifted if an excited orbital or valley state can be accessed when the detuning energy exceeds the singlet-triplet splitting E_{ST} or valley splitting E_{vs}. PSB readout is performed by changing the detuning ϵ (see Fig. 2.1e) such that the energy levels are tilted to transition from the (1,1) to the (2,0) or (0,2) charge state. In contrast to Elzerman readout, PSB readout does not require a reservoir and the system remains in the projected state after readout. Furthermore, it can be performed at elevated temperatures and reduced magnetic field, Chapter 7 demonstrates readout at T > 1 K and B_{ext} = 650 mT.

PSB readout turns into parity readout when the odd parity $|T_0\rangle$ (1,1) state has significantly faster relaxation compared to the even parity states $|T_+\rangle$ (1,1) and $|T_-\rangle$(1,1) [34]. This effect is strongly dependent on spin-orbit interaction (SOI) and can be compensated for by control over the tunnel rate and detuning at the readout point. The readout fidelity can be improved by employing latched PSB readout, at the disadvantage of requiring a reservoir. The (0,2) charge state is mapped to (1,2),

where the added reservoir transition results in a higher charge signal [35].

2.5. Driving mechanisms

Coherent spin transitions can be achieved by Rabi driving the qubit on its resonance frequency, which is equal to the energy difference between the spin up and spin down state ($hf = g\mu_B B_{ext}$). One approach is Electron Spin Resonance (ESR), which employs a direct oscillating magnetic driving field perpendicular to the static field. This can be implemented by passing a high frequency current through a wire, which may be an on-chip coplanar waveguide transmission line [36] to limit the dissipation of microwave signals [37, 38]. Implementing the stripline using a superconducting material can further reduce dissipation on the qubit plane.

An alternative method is Electron Dipole Spin Resonance (EDSR), where spins can be driven by moving the electron through a magnetic field gradient, causing them to experience an effective oscillating magnetic field. The magnitude of this gradient is determined by spin-orbit interaction, which is generally strong for holes such as in Ge/SiGe [27], nanowires [39] and fin field-effect transistors (FinFETs) [40, 41]. For electrons in bulk silicon, SOI is very weak, the inversion asymmetry of the crystal at the interface can lead to a strong SOI [42]. The magnetic gradient can be enhanced by fabricating micro magnets on top of the device [16, 43]. While it is advantageous to have a strong SOI for fast driving [27], it also enables spin-decoherence by electric field fluctuations (see section 2.6) [44].

2.6. Relaxation and dephasing

Electron spins in semiconductor quantum dot systems can be characterised by the relaxation time T_1, the decoherence time T_2 and ensemble decoherence time T_2^*, where $T_2^* < T_2$. T_1 refers to the time over which the excited $|1\rangle$ state decays to the ground state $|0\rangle$. For spins in silicon, this can range up to seconds [37]. As electric fields cannot cause transitions between pure spins, the relaxation rate is dependent on the mixing of spin and orbit states. Spin-valley mixing has been shown do greatly enhance relaxation rates at the ”hot spot” where the valley splitting energy equals the Zeeman splitting [12], see Chapter 6.

The dephasing time T_2^* refers to the coherence of the superposition state $\frac{|0\rangle+|1\rangle}{\sqrt{2}}$ and notes the typical time it takes before phase information is lost. Usually, T_2^* is much smaller than T_1 and therefore the limiting timescale for quantum operations. T_2^* can range up to several hundreds of microseconds in purified silicon [37]. Magnetic noise originates from fluctuations in the applied external magnetic field B_{Ext}, paramagnetic charge traps and defects at the Si/SiO_2 interface [45], and nuclear spins. Hyperfine interaction couples the electron spin to nuclear spins in the environment [46]. Non-zero spin isotopes such as ^{29}Si nuclear spins can flip, resulting in a change of the effective magnetic field that the electron spin experiences, called the Overhauser field. At lower magnetic fields, the rate of these fluctuations increases, suggesting that the electron spin drives these transitions, which happen more easily when the electron and nuclear Zeeman energies are lower [47]. Nuclear

magnetic noise can be strongly reduced by isotopic purification (see section 2.8). As a result, only a few nuclear spins remain that can be addressed and controlled [48]. Fluctuations of the nuclear spin bath and B_{Ext} are typically slow compared to qubit operations and dynamical decoupling techniques can be applied to extend the dephasing time, resulting in a T_2 of 28 ms in SiMOS [37].

Electric noise, such as phonon and Johnson and 1/f charge noise, does not couple to pure spin states. Nevertheless, as a result of the mixing of spin and orbital states through SOI, electric noise couples to many parameters. In the presence of a large intrinsic (material) or artificial (micromagnet) SOI, relaxation rates are enhanced through an increased coupling of electric noise to phonons [49]. At low temperatures, the main contribution is from Johnson and phonon noise, 1/f charge noise is almost negligible at the qubit transition frequencies [50]. At elevated temperatures, second-order phonon relaxation processes become dominant, as demonstrated in Chapter 6. Electric noise couples to the electron g-factor [37] which affects the resonance frequency of the qubits. Fluctuations in detuning and tunnel coupling reduce the fidelity of two-qubit gates (as shown in Chapter 7) by influencing the exchange interaction [51]. This effect can however be reduced: operation at the symmetry point causes detuning, and as a result the exchange interaction, to be first-order insensitive to detuning noise [44].

2.7. Effects of temperature

"Hot qubits" are operated at an elevated temperature (usually between 0.5 and 4 Kelvin). Spin readout suffers from an increase in temperature in multiple ways. The increase in electron temperature of the SET causes broadening of the SET peaks, eventually causing them to overlap. The reduced charge readout sensitivity limits the temperature range that can be characterised [41]. Spin-to-charge conversion is also affected (see section 2.4). The fidelity of Elzerman readout strongly suffers from the thermal broadening of reservoir energy levels that become comparable with the Zeeman splitting. PSB readout is more robust, the relevant energy scale being the excited state. The quantum dots are directly influenced by an increase in electron temperature, which couples namely into the exchange interaction via detuning. Operation at sweet spots such as the charge symmetry point can be used to mitigate the effects of noise [44]. Sources of Johnson noise such as the reservoir 2DEG that increase with temperature have an additional indirect effect [29]. Electric charge noise shows a linear dependence on temperature (see Chapter 6).

2.8. Materials

Different semiconductor materials with distinct properties are nowadays used to form quantum dots, but pioneering research was mostly done in the gallium arsenide (GaAs) platform [2, 36, 52–55]. This material can be grown using molecular beam epitaxy, resulting in a crystalline heterostructure with a high mobility. Devices can be readily produced and it is still used as a testbed [56]. Advancing to qubits, however, reveals a major disadvantage of this material: many nuclear spins are present [57, 58], resulting in a short dephasing time T_2^* of less than 100 ns [36].

Using CPMG pulses this can be extended to a T_2 of 200 μs [59], and nuclear notch filtering can result in a T_2 of 0.87 ms [60]. This time is still almost two orders of magnitude less than SiMOS [37] and requires a significant overhead of decoupling pulses for specific Larmor frequencies.

To obtain longer coherence times, the quantum computing community has started to work with group IV materials, such as silicon metal-oxide-semiconductor (SiMOS) [8, 37] and silicon germanium (SiGe) heterostructures, with either a silicon (Si/SiGe) [16, 61, 62] or germanium (Ge/SiGe) [27, 63] quantum well. These materials have isotopes that have a net zero nuclear spin [64], and isotopic purification can result in ^{29}Si concentrations below 10 ppm [65]. A record dephasing time T_2^* of 120 μs, with a T_2 of 28 ms have been obtained in an ESR SiMOS device with a a residual 800 ppm ^{29}Si [66]. Experiments on EDSR Si/SiGe devices with a purified quantum well with either 800 [67] or 60 [68] ppm residual ^{29}Si both yield a T_2^* of 20 μs, with a T_2 of 3.1 ms [67]. The similarity illustrates that at these low ^{29}Si concentrations, dephasing is dominated by charge noise coupled in via magnetic field gradients, rather than nuclear magnetic noise [67, 68]. Further research is necessary to determine whether the T_2^* of 833 ns for unpurified Ge/SiGe [27] is electric or nuclear noise limited.

An important difference between the SiMOS and the SiGe heterostructure platforms is the location of the quantum dots. In SiMOS, quantum dots form at the interface between silicon and amorphous silicon oxide, while for SiGe heterostructures the formation happens at an epitaxially grown interface. As a result, SiMOS suffers from more disorder and quantum dots tend to form at unintended locations. The disorder is increased further by electron-beam lithography processing but can be reduced by thermal annealing [69]. This interface also brings an advantage to SiMOS: due to the sharper potential step at the Si/SiO_2 interface compared to the Si/SiGe interface, valley splitting is larger in SiMOS. Where valley splittings between 10 and 300 μeV are reported for Si/SiGe [14–17], a tunable valley splitting between 200 and 1000 μeV is reported for SiMOS [12, 13]. Holes do not experience this valley degree of freedom, instead the relevant energy scale is the orbital splitting resulting from confinement, measured to be 0.25 meV for holes in SiMOS [70] and up to 1 meV for holes in Ge/SiGe [27, 71].

Group IV materials are highly compatible with industrial CMOS manufacturing, where SiMOS holds the greatest resemblance. Quantum dots and qubits are already being made in industrial foundries [72–75] and industrial $^{28}Si/^{28}SiO_2$ substrates were used for all SiMOS samples in this thesis. The next chapter provides a closer comparison and demonstrates the formation of quantum dots in all three group IV platforms.

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3

Quantum dot arrays in silicon and germanium

When a measure becomes a target, it ceases to be a good measure.

Marilyn Strathern

In order for quantum electronics to become practical, large numbers of quantum dots will be required, necessitating the fabrication of scaled structures such as linear and 2D arrays. Group IV semiconductors contain stable isotopes with zero nuclear spin and can thereby serve as excellent hosts for spins with long quantum coherence. In this chapter, we demonstrate group IV quantum dot arrays in silicon metal-oxide-semiconductor (SiMOS), strained silicon (Si/SiGe) and strained germanium (Ge/SiGe). We fabricate using a multi-layer technique to achieve tightly confined quantum dots and compare integration processes. While SiMOS can benefit from a larger temperature budget and Ge/SiGe can make ohmic contact to metals, the overlapping gate structure to define the quantum dots can be based on a nearly identical integration. We realize charge sensing in each platform, for the first time in Ge/SiGe, and demonstrate fully functional linear and two-dimensional arrays where all quantum dots can be depleted to the last charge state. In Si/SiGe, we tune a quintuple quantum dot using the N+1 method to simultaneously reach the few -electron regime for each quantum dot. We compare capacitive crosstalk and find it to be the smallest in SiMOS, relevant for the tuning of quantum dot arrays. These results constitute an excellent base for quantum computation with quantum dots and provide opportunities for each platform to be integrated with standard semiconductor manufacturing.

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3.1. Introduction

Quantum dots have been a leading candidate for quantum computation for more than two decades [2]. Furthermore, they have matured recently as an excellent playground for quantum simulation [3] and have been proposed for the design of new states of matter [4, 5]. Pioneering studies in group III-V semiconductors led to proof-of-principles including the coherent control of electron spins [6, 7], rudimentary quantum simulations [8], and signatures of Majorana states [9]. The group IV semiconductors silicon and germanium have the opportunity to advance these concepts to a practical level due to their compatibility with standard semiconductor manufacturing [10] and the availability of isotopes with zero nuclear spin, increasing quantum coherence for single spins by four orders of magnitude [11]. Furthermore, heterostructures built from silicon and germanium may offer a large parameter space in which to engineer novel quantum electronic devices [12–14].

An initial advancement towards silicon quantum electronics [12] was the design of an integration scheme based on overlapping gates to build silicon metal-oxide-semiconductor (SiMOS) quantum dots [15]. This technique was later adopted in strained silicon (Si/SiGe) [16] and refined by incorporating metals with small grain size and atomic layer deposition (ALD) for layer-to-layer isolation [17] and to enable tunable coupling between single-electrons in SiMOS [18]. These developments in fabrication have led to a great body of results, including high-fidelity qubit operation [19, 20] and two-qubit logic [21–23]. Controlling holes in silicon has been more challenging due to type II band alignment in strained silicon, limiting experiments to SiMOS [24–26]. Strained germanium on the other hand [13, 27, 28] exhibits type I band alignment and is thereby a viable platform in which holes with light effective mass [29] can be confined [30] and coherently controlled [31]. This motivates the development of an integration scheme that can build upon the individual breakthroughs realized in each platform to advance group IV semiconductor quantum dots towards large quantum systems.

Here, we present the fabrication and operation of quantum dots in silicon and germanium, in linear and two-dimensional arrays. We show stability diagrams obtained by charge sensing and report double quantum dots in SiMOS, Si/SiGe, and Ge/SiGe that can be depleted to the last charge state. We compare integration schemes and find that while each platform has unique aspects and opportunities, the core fabrication of overlapping gates defining the nano-electronic devices is remarkably similar. Fabrication is most demanding in SiMOS due to requirements on feature size, but we also find that the resulting devices have the smallest cross capacitance, simplifying tuning and operation. We leverage off the ohmic contact between quantum dots in Ge/SiGe and metals [32] to avoid the need for implants and to provide means for novel hybrid systems. In each case, fabrication starts from a silicon substrate, and integration is compatible with standard semiconductor technology.

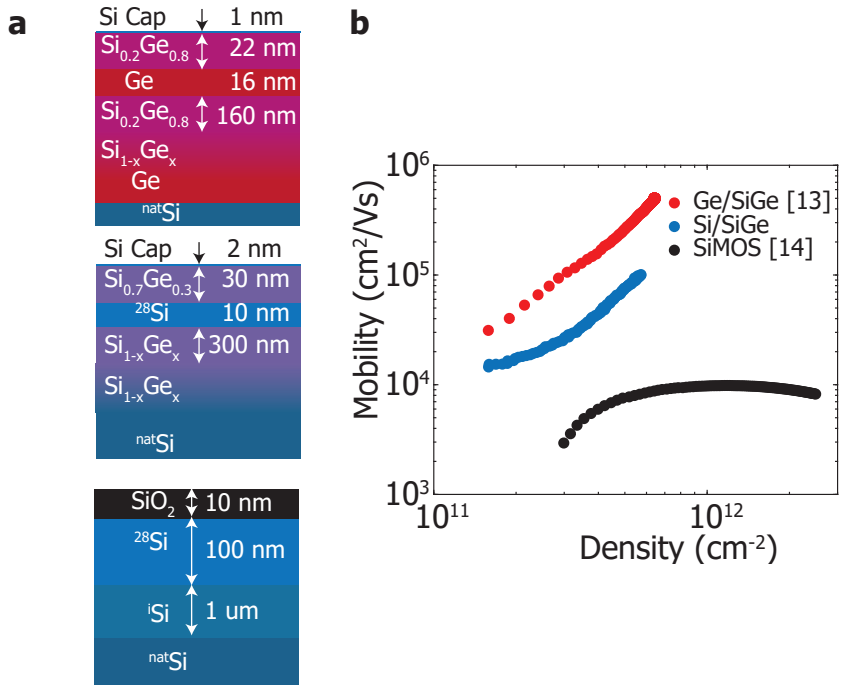

Figure 3.1: **Wafer stack schematics and mobility as a function of carrier density. a** From left to right, SiMOS, Si/SiGe, and Ge/SiGe wafers stacks. For SiMOS, a ^{28}Si epilayer with 10 nm thermal oxide is grown on a 1 μm intrinsic natural Si buffer layer. The Si/SiGe heterostructure consists of a 1.5 μm linearly graded SiGe layer, a relaxed 300 nm SiGe spacer, a 10 nm ^{28}Si quantum well, a 30 nm SiGe spacer, and a 2 nm Si cap. The Ge/SiGe heterostructure consists of 900 nm reverse graded SiGe layer, a relaxed 160 nm SiGe spacer, a 16 nm Ge quantum well, a 22 nm SiGe spacer, and a 1 nm Si cap. **b** Mobility as a function of carrier density measured in each platform. For Ge/SiGe, the peak mobility is greater than 5×10^5 cm^2/Vs and the critical density is 1.15×10^{11} cm^{-2} [13]. The same measurements for Si/SiGe wafers give a peak mobility of 1×10^5 cm^2/Vs and a critical density of 1.2×10^{11} cm^{-2}. SiMOS data taken from [14] shows a mobility of 1×10^4 cm^2/Vs and a higher critical density of 2.5×10^{11} cm^{-2}.

3.2. Material characterization

Figure 3.1a schematically shows the SiMOS, Si/SiGe, and Ge/SiGe wafer stacks used in this study. The SiMOS 300 mm wafers are grown in an industrial complementary metal-oxide-semiconductor (CMOS) fab [14, 18, 33], while the Si/SiGe and Ge/SiGe four-inch wafers are grown using an RP-CVD reactor (ASM Epsilon 2000) [13]. Each platform is grown on a p-type natural Si wafer. The SiMOS structure consists of 1 μm intrinsic natural silicon (^{i}Si) followed by 100 nm ^{28}Si (800 ppm purity) and 10 nm SiO_2 [14]. The Si/SiGe heterostructure begins with a linearly graded $Si_{1-x}Ge_x$ layer, where x ranges from 0 to 0.3. A relaxed $Si_{0.7}Ge_{0.3}$ layer of 300 nm lies below the 10 nm ^{28}Si (800 ppm purity) quantum well which itself is separated from the 2 nm Si capping layer by a second 30 nm relaxed $Si_{0.7}Ge_{0.3}$ spacer layer. The Ge/SiGe wafer stack starts with 1.4 μm of Ge and 900 nm of reverse graded $Si_{1-x}Ge_x$ where x ranges from 1 to 0.8. This lies below a 160 nm $Si_{0.2}Ge_{0.8}$ spacer layer, a 16 nm

Temperature	SiMOS	Si/SiGe	Ge/SiGe
Thermal Budget	1000 °C	750 °C	500 °C

Ohmics	SiMOS	Si/SiGe	Ge/SiGe
Dopant	P^+	P^+	-
Metal	Ti:Pt	Ti:Pt	Al
Annealing	1000 °C, 30 s	700 °C, 30 s	300 °C, 1h

Field Oxide	SiMOS	Si/SiGe	Ge/SiGe
Oxide Window	✔	(1)	(1)

Stack	All Platforms
Bondpads	SiN 150 nm
Gate Layer	Ti:Pd
Isolation	Al_2O_3 ALD

Control	SiMOS	Si/SiGe	Ge/SiGe
mw-Antenna	✔	✔	-
Micromagnet	✔	✔	-
Spin-Orbit	(2)	-	✔

Figure 3.2: **Overview of fabrication scheme for SiMOS, Si/SiGe and Ge/SiGe quantum dots.** The thermal budget of each material prior to gate stack deposition is estimated based on the limiting mechanism of each platform as discussed in the text. In all cases, gates are fabricated from Pd metal with a thin (3 nm) Ti adhesion layer, with layer-to-layer isolation performed via atomic layer deposition (ALD) of Al_2O_3. These two steps can be looped at appropriate thicknesses to form the multi-layer structure. (1) We note the possibility of such an etch exists for the remaining platforms in the case of a Schottky gate architecture (2) We note that spin-orbit based driving of electrons in SiMOS has been demonstrated for singlet-triplet qubits [38] and proposed for single spin qubits [39].

Ge quantum well under compressive strain, a second $Si_{0.2}Ge_{0.8}$ layer of 22 nm and finally a thin Si cap of 1 nm [13].

Figure 3.1b shows a carrier mobility versus density characterization of the three platforms. Hall bar structures were fabricated on coupons cut from the centre of each wafer. Maximum mobility and critical density are extracted at 1.7 K. SiMOS 300 mm processed wafers give a peak mobility value of 1×10^4 cm^2/Vs, as well as a critical density of about 1.75×10^{11} cm^{-2} as shown in another work [14]. At higher densities, SiMOS mobilities fall off due to surface roughness scattering effects [34–36]. In Si/SiGe, we observe a lower critical density of 1.2×10^{11} cm^{-2} and a significantly higher maximum mobility exceeding 1×10^5 cm^2/Vs . Similar studies conducted on natural Si/SiGe grown in an industrial CMOS fab yielded mobilities of 4.2×10^5 cm^2/Vs [37]. This quality improvement observed by moving toward industrial CMOS fab also suggests encouraging prospects for Ge/SiGe, already exhibiting a high maximum mobility of 5×10^5 cm^2/Vs and critical density of 1.15×10^{11} cm^{-2} despite being grown in an academic cleanroom via RP-CVD [13].

3.3. Device fabrication

Figure 3.2 summarises the integration scheme utilized for each platform. The thermal budget is estimated based on the respective limiting mechanisms. For SiMOS, thermal processing is limited by the self-diffusion of natural silicon from the substrate into the ^{28}Si epilayer. From the self diffusion constants measured by Bracht et al. [40], we estimate the point at which the residual ^{29}Si concentration within 1 nm of the Si/SiO_2 interface increases by 1 ppm occurs at 1000 ^oC for time scales above 1 hour, for furnace anneals in a pure argon atmosphere. Consequently, this allows for extensive thermal treatment and annealing of samples. This is highly advantageous, as we have observed that a 15 minute anneal in forming gas at 400 ^oC after the deposition of every gate layer greatly improves the quality of our fine features (see section 3.9.1 for a detailed comparison). In addition, a final end-of-line anneal is conducted to eliminate processing damage at 400 ^oC in forming gas for 30 minutes. In the cases of Si/SiGe and Ge/SiGe, the thermal budget is limited by strain relaxation of the quantum wells, thus the maximum processing thermal budget is given qualitatively by the temperature at which the quantum wells were grown. This is 750 ^oC for strained Si and 500 ^oC for strained Ge [13].

The design of ohmic contacts is tailored to the specific requirements of the device. For both Si platforms, ohmic contact is made via high fluence P ion implantation followed by evaporation of Ti:Pt metallic contacts, creating n^{++} doped, low resistance channels. The oxide is etched locally directly before metal deposition using buffered hydrofluoric acid (BHF). In the case of Si/SiGe, stray capacitance is minimized to ensure maximum power is dissipated in the variable resistance of the sensing quantum dot for RF-readout. Germanium can make direct ohmic contact to metals [32], avoiding the need for implants. We deposit Al and anneal at 300 ^oC for 1 hour in vacuum to assist in Al diffusion into the quantum well. The Al ohmic is defined close to the quantum dots, resulting in a very low resistance channel ideally suited for RF circuits and enabling a tunnel contact that can even be made superconducting [41]. The implementation does however lower the thermal budget of further processing.

Fabrication of each device utilizes a titanium-palladium (Ti:Pd) gate stack with 3 nm of Ti deposited for each layer to assist with adhesion. Pd makes a good gate metal due to its low grain size [17]. Unlike the commonly used material Al, Pd does not self-oxidise and ALD can be used to define sharp dielectric interfaces. For the SiMOS and Si/SiGe devices shown in Fig. 3.3, we utilize a three-layer gate stack that we refer to as the screening layer, the plunger layer and the barrier layer. In order to assist the climbing of overlapping gate features, the initial layer is deposited at 20 nm total thickness, while subsequent layers are at 40 nm. Each layer is isolated from one another via ALD of Al_2O_3 at 7 nm thickness. We measure the dielectric strength of our Al_2O_3 to be greater than 6 MV/cm, allowing potentials of greater than 4 V to be applied between adjacent gates. To leverage off the high quality industrial CMOS fab, we begin fabrication of SiMOS devices on wafers including a 10 nm SiO_2 oxide already grown. To further reduce the likelihood of leakage from gate to substrate, we first grow a thick 10 nm Al_2O_3 blanket layer over the entirety

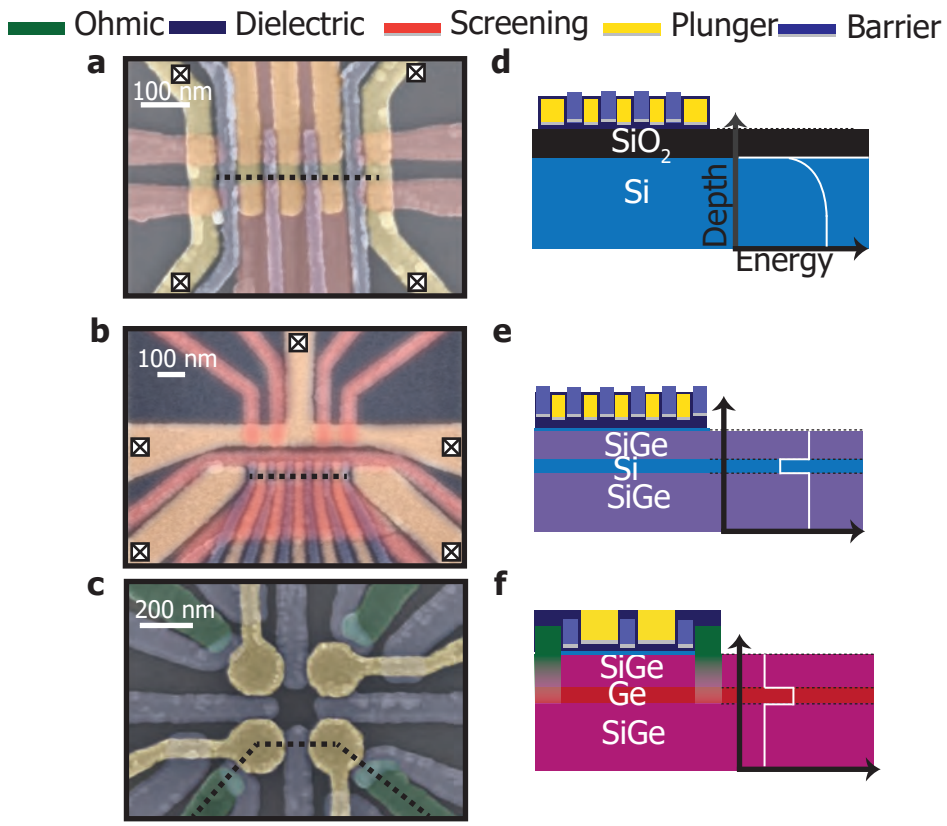

Figure 3.3: **Scanning electron microscope images and corresponding substrate with band bending diagrams and gate stack for each of the devices.** Dotted lines in **a**-**c** indicate the cross-section through the quantum dot channel illustrated in **d**-**f** respectively, and crossed boxes indicate gates that overlap with implanted regions to form ohmic contact. The plunger gates (yellow), the barrier gates (blue) and the screening gates (red) define the quantum dots. **a** SiMOS triple quantum dot linear array. Two SETs function as charge sensors and as reservoirs for the quantum dots on either side of the array **b** Si/SiGe quintuple quantum dot linear array. Two SETs (top) are used for charge sensing. **c** Ge/SiGe (2x2) quadruple quantum dot array. Each quantum dot is tunnel coupled to a metallic lead (green). Measurement can be performed in transport, or using charge-sensing by forming a sensor by coupling two quantum dots. **d**-**f** Cross-section and band structure of metal, dielectric (black) and semiconductor **d** SiMOS, **e** Si/SiGe and **f** Ge/SiGe.

of the substrate. Advantageously, one can etch Al_2O_3 on thermally grown SiO_2 selectively, allowing the definition of a 20x20 μm^2 area where the quantum dot system is defined, which we have measured to significantly reduce low-frequency drifts deduced from charge occupation stability [42] (see section 3.9.2).

The final deposition step is the qubit control layer. The spin-orbit coupling for holes in germanium enables qubit operation by simply applying microwave pulses

to the quantum dot gates [31, 43] and no further processing is required. In silicon, qubit driving can be realized by integrating on-chip striplines [11], which we fabricate using Al or NbTiN, or micromagnets [44], which we integrate using Ti:Co. Quantum dots in Si/SiGe generally have a larger and more mobile electron wave function as compared to SiMOS and thereby benefit most from a micromagnet integration for fast qubit driving.

3.4. Quantum dot arrays

A schematic of each material and associated device is shown in Fig. 3.3 and labelling of the relevant gates are shown in Fig. 3.4. The SiMOS device is a three-layer, triple quantum dot structure with dedicated plungers (P_{1-3}), inter-dot barriers (B_{12}, B_{23}) and reservoir barriers (T_l, T_r). Charge noise resulting from fluctuations of impurities near the quantum dot array is screened by two large metallic gates (C_l, C_u) deposited in the initial layer and kept at a constant potential. These also serve to confine the quantum dots in one lateral dimension. Two single-electron transistors (SETs) are positioned at either side of the quantum dot array, and function as charge sensors for spin and charge readout. The Si/SiGe device is a quintuple quantum dot linear array written in three-layers utilizing a similar architecture to that of the SiMOS device. the quantum dot array contains five plunger gates (P_{1-5}) with inter-dot barriers (B_{12-45}) and reservoir barriers. Dots are confined laterally and screened from charge noise by two confinement gates. Two SETs are positioned parallel to the quantum dot channel. The Ge/SiGe device is a 2x2 quadruple quantum dot array written in two layers. Gates (P_{1-4}) are positioned anti-clockwise in the array and define the potential of the quantum dots. Each pair of adjacent quantum dots share a barrier gate (B_{12-41}) capable of tuning inter-dot tunnel coupling. Coupling of each quantum dot to its reservoir can be controlled via a barrier gate. This device can be operated as a quadruple quantum dot system in transport mode, but for the present work we intentionally tune the inter-dot barrier to form a single hole transistor (SHT) along a dot channel that we subsequently use for charge sensing of the double quantum dot along the opposite channel. For more information about device specific fabrication, see appendix A.1.

To demonstrate the success of our integration scheme, we show that we can create stable quantum dots in each platform. Figure 3.4 shows charge stability diagrams for tunnel-coupled double quantum dots, measured by performing charge sensing. Lock-in techniques are used in the case of SiMOS and Ge/SiGe, where an excitation is placed on an inter-dot barrier gate B_{12} in each case, and the transconductance of our source-drain channel is measured. We use compensation to remain at a sensitive point on our SET/SHT Coulomb peaks [45]. In the case of Si/SiGe, charge readout is performed using RF-reflectometry techniques. A 3 μH kinetic inductor is bonded to the sample source which forms a resonant LC circuit when combined with parasitic capacitance to ground. In each case, we measure a stability diagram and show that we can deplete down to the (0,0) electron/hole charge configuration. We note that the plunger voltages in the case of Si/SiGe required to form double quantum dots in the (1,1) charge occupation are within

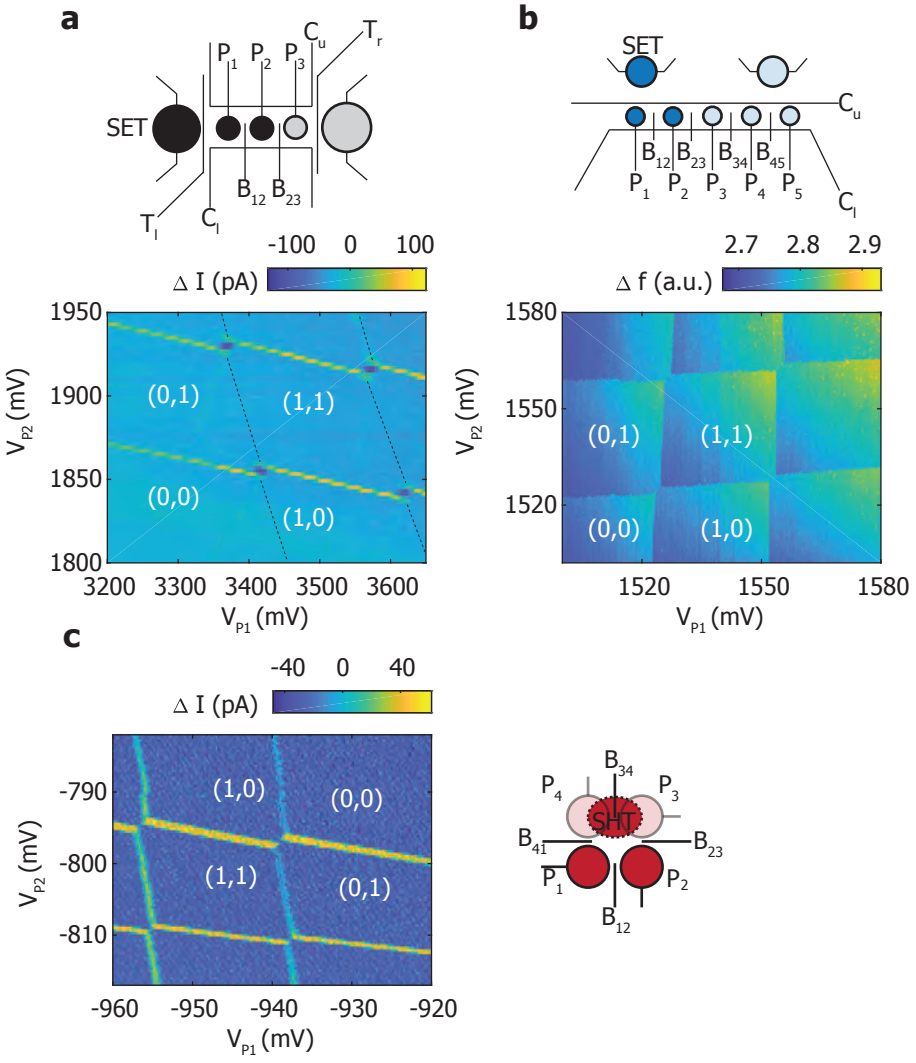

Figure 3.4: **Charge stability diagrams of double quantum dots depleted to the single-electron/hole regime for the three platforms. a** SiMOS double quantum dot. Charge addition lines under P_1 are not visible due to a low tunnel rate from the reservoir. Map taken at 0.44 K using lock-in charge sensing. The excitation is placed on the inter-dot gate B_{12}. **b** Si/SiGe double quantum dot formed under the first two plungers, sensed by the nearest charge sensor via RF-reflectometry utilizing a resonant LC circuit at 84 MHz. Here, the plunger gate voltages are in virtual gate space correcting for weak cross capacitive coupling. **c** Ge/SiGe depleted to the single hole regime. A large single quantum dot is formed under P_3, B_{34} and P_4, by adjusting the tunnel barrier voltage B_{34}, and is used to sense a double quantum dot under P_1 and P_2. The lock-in excitation is placed on the inter-dot tunnel barrier B_{12}.

one charging energy. These remarkably similar tuning parameters are promising with regards to the stringent requirements placed on quantum dot array tune-up in

crossbar architectures [46]. While operation in the single-electron regime in silicon has been routinely achieved before, this work shows the first demonstration of the single hole regime using charge sensing of holes in Ge/SiGe. We attribute the slight difference in slope of the first and second charge addition lines in Fig. 3.4c to a shift in the position of the quantum dot relative to the inter-dot tunnel barrier.

In Fig. 3.5 and Fig. 3.6 we demonstrate that quantum dots can be formed under each dedicated plunger gate. For Fig. 3.5a-c, in each SiMOS quantum dot, lock-in charge sensing is performed by placing an excitation on the respective plunger gates, while trans-conductance in the nearby SET channel is measured. In each case, the first charge transition is visible. For quantum dots formed under plungers P_{2-3}, electron loading is from the right SET which constitutes a reservoir. For the quantum dot under P_1, loading is from the left SET via the gate T_l. The Si/SiGe quintuple quantum dot system in Fig 3.5d-g is tuned using the N+1 strategy [47], reaching the few-electron regime simultaneously for all quantum dots. In Fig. 3.5 we show stability diagrams, in each of which we scan two virtual plunger gates which allow to controllably load a single-electron into each quantum dot. Double quantum dots are formed between each set of adjacent plungers, and sensed using RF-reflectometry like in Fig. 3.4b using the left SET for all configurations. As expected, the observable signal from charge transition lines fades as the quantum dot pairs are formed farther away from the SET. The derivative of the reflected signal is plotted, and shows the (0,0) charge occupancy for each charge stability diagram. For every double quantum dot, loading occurs via the left accumulation gate, leading to latching effects and low tunnel rates in the quantum dots formed farther away from the reservoir. Here, the plunger voltages, while similar, are not entirely within one charging energy, suggesting further improvements to heterostructure uniformity are required to meet strict large-scale array tune-up requirements. Figure 3.6 a-c shows charge sensing operation of the 2x2 quantum dot array fabricated in Ge/SiGe. In each case, a sensing quantum dot is formed in the channel parallel to the double quantum dot by opening the inter-dot barrier such that a large single quantum dot is formed. In the opposite channel, the inter-dot barrier is closed, forming a double quantum dot system in the low tunnel coupled regime.

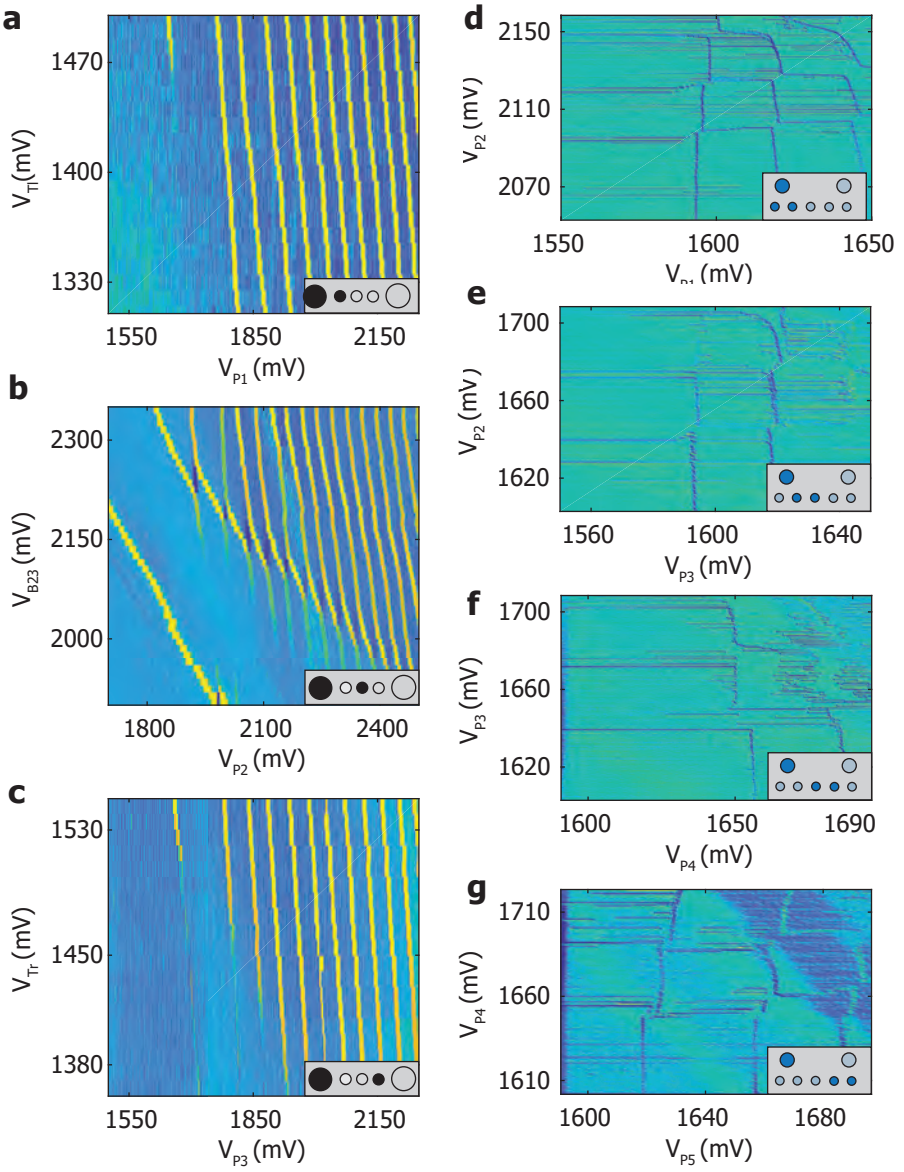

Figure 3.5: **Quantum dot arrays in SiMOS and Si/SiGe.** **a**-**c** SiMOS triple quantum dot device stability diagrams. Each single quantum dot is formed under its respective plunger gate upon which an excitation is placed for lock-in charge sensing. Each quantum dot is depleted to the single charge state. **b** Shows the crossing of the adjacent quantum dot under P_3, through which the quantum dot is loaded. **d**-**g** Si/SiGe double quantum dots tuned up sequentially using the N+1 method [47] to the single-electron regime. True plunger gate voltages are plotted, though virtual gates are swept containing small corrections to adjacent barriers and plungers. Each double quantum dot pair is sensed using RF-reflectometry. The same SET is used for readout in each case, as indicated by the relative signals as each double quantum dot pair is formed farther from the charge sensor. **g** The data has been filtered to remove 50 Hz background noise for data clarity.

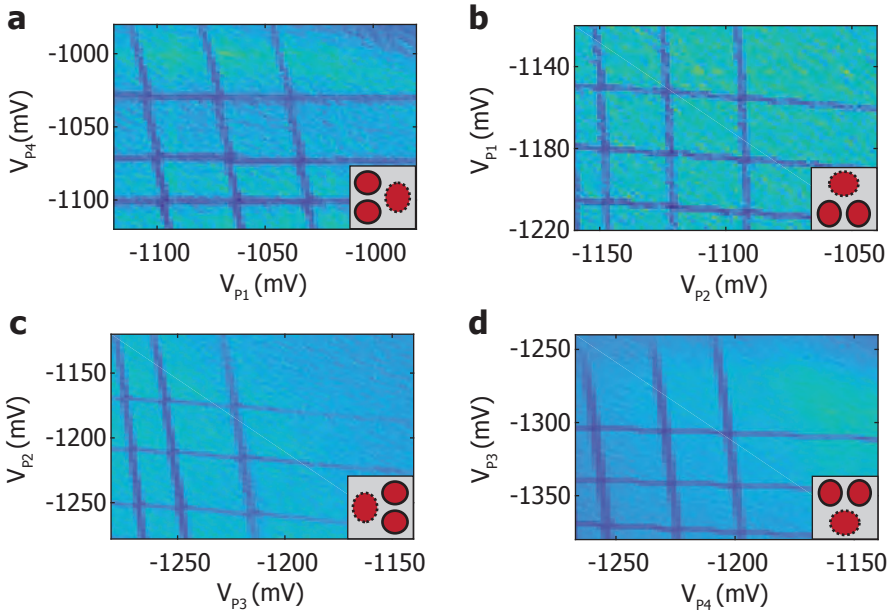

Figure 3.6: **Quantum dot array in Ge/SiGe. a-d** Ge/SiGe 2x2 array double quantum dots formed in each possible configuration. In each case, a charge sensor is formed in the parallel channel by raising the inter-dot coupling to form a large single quantum dot with high hole occupation. Each charge stability diagrams shows RF-sensing of double quantum dots depleted to the last hole occupancy, in the low tunnel-coupled regime.

3.5. Cross capacitance comparison

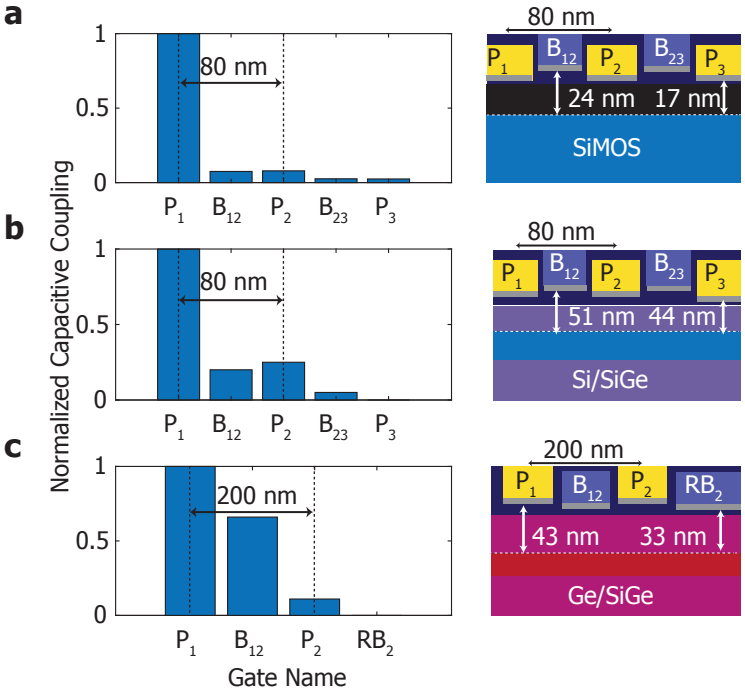

Figure 3.7: **Cross capacitance to neighbouring gates of a quantum dot in the single charge occupancy regime under gate P_1 in each platform.** Each cross-sectional cartoon shows plunger pitch and distance between each relevant gate layer to the center of the quantum well. **a** For SiMOS we observe immediate falloff of cross-coupling due to the tight quantum dot confinement present in SiMOS devices. Here the inter-dot pitches matches that of Si/SiGe at 80 nm. **b** For Si/SiGe we see significant cross-coupling between adjacent plungers and barrier gates. Here the plunger gates are written before the barrier layer and have an inter-dot pitch of 80 nm. **c** Ge/SiGe reveals as expected a slower fall-off of cross-coupling. We attribute this to the larger plunger gate design, made possible by lower hole effective mass. In this case, the plunger gates P_1 and P_2 are written in the layer above the barrier gates B_{12} and RB_2, decreasing coupling to their respective quantum dots. The plunger to plunger pitch is 200 nm.

A significant challenge for larger quantum dot arrays will manifest in tuning. The presence of large capacitive crosstalk in GaAs has led to development of virtual gates and approaches to tune larger systems [47, 48]. To assess the relevance of these approaches for silicon and germanium structures we measure cross capacitance as shown in Fig. 3.7. To obtain the cross-coupling, we measure the slope of the charge addition lines with respect to each gate and normalize by a cross-coupling of unity for the plunger gate associated with the respective quantum dot. Each slope is taken for the first charge transition and in the low tunnel-coupled regime. In SiMOS, cross-coupling is almost negligible, as expected from quantum dots located only 17 nm (10 nm SiO_2 and 7 nm Al_2O_3) below the electric gates. This compares favourably to the cross-coupling observed in Si/SiGe, where falloff

is significantly slower despite sharing equal gate pitch to the SiMOS array. While the cross-coupling in the Ge/SiGe system is the largest and extends over multiple neighbouring gates, it still falls off significantly faster than quantum dots defined in GaAs [47]. For Ge/SiGe, we also observe that the barrier gates have a relatively stronger coupling as compared to the plunger gates, due to their definition in lower layers of the multi-layer stack. Summarizing, we conclude that for SiMOS tuning is most straightforward considering capacitive crosstalk only, while each platform compares favourably to GaAs.

3.6. Roadmap for group IV quantum dots

Quantum computing with group IV semiconductor quantum dots is well entrenched as a promising means to process quantum information. Looking forwards, we identify five focus areas for the community that through shared co-development, will launch the field into new and practical ground.

3.6.1. Industrially manufactured quantum dots

Most quantum devices are fabricated in local academic cleanrooms since the turnaround and feedback from measurement to design and fabrication is fast. However as designs for various types of quantum dot devices converge, an opportunity exists to leverage off the outstanding material quality [14, 37] and processing facilities of industrial fab lines. Devices fabricated utilizing 300 mm wafers grown in an industrial CMOS fab have led to tunable tunnel coupling in SiMOS [18] and investigations into the practicality of high temperature operation [49] which has in turn made possible two-qubit gate operations at 1.1 K [49]. Furthering symbiotic partnerships with industry will prove highly beneficial for the development of uniform quantum dots. The adoption of group IV based semiconductor platforms beyond SiMOS such as strained Si and Ge as well as full 300 mm device fabrication lines would accelerate progress in the field of semiconductor quantum dot based quantum computing, as it has in other fields[50].

3.6.2. Hybrid qubit directions

Since its inception, many quantum systems have been studied as potential qubit candidates for quantum information processing. It has also become clear that each of these quantum systems holds specific collections of properties suited to the various requirements of quantum computation[51]. Resultantly, avenues of research targeting the combination of qubit implementations have emerged to leverage off the advantages of each, to improve qubit quality overall. These hybrid directions are extensive, however, most promising for spin qubits are those combining their fast operation times with systems that reliably conserve the quantum state, such as topologically protected qubits [52]. Here, Ge/SiGe makes an excellent candidate for hybrid spin-Majorana qubits, thanks to its Fermi level pinning, allowing direct ohmic contacts to be formed without the need for implants[31]. An important milestone towards demonstrating a hybrid qubit will be achieving hard gap superconductivity.

3.6.3. Automated tuning

As quantum devices grow in the number of physical qubits, so too do the complexities related to tuning them. Resultantly, a great body of work on the automated tuning of quantum devices has emerged in the last few years in an attempt to address this concern. Due to the relative uniformity of the material, these efforts were pioneered in GaAs based quantum dots, demonstrating automated tuning to the single-electron regime [53, 54] and controllable interdot tunnel coupling [55]. However larger scale arrays have emerged more recently in silicon [56], and computer automated single-electron regime tune-up protocols therein [57]. As material quality and fabrication techniques improve in Group IV semiconductor quantum dot devices, further development of automated tuning protocols will be necessary for the exploration of larger quantum dot systems, in particular automated tuning of interdot tunnel couplings, and protocols for 2D arrays. Furthermore, high fidelity operation of qubits in large-scale quantum devices will require precise operation at exact resonance frequencies and Rabi frequencies, accounting for potential drifts in these parameters over time. Tune-up protocols will therefore have to go beyond charge state control, handling qubit operation also.

3.6.4. 2D scalability

Scale-up of the number of qubits on a quantum device requires the design and implementation of extensible two-dimensional qubit arrays. However, the connection of control wirings for each qubit at large numbers is completely impractical. Problems arise at multiple levels of the control stack. Scaling at the chip level is limited by fanout space and Rents rule [58], while scaling of the wiring is complicated by the limited cooling power and spatial restrictions of dilution refrigerators. As a result, proposals for qubit shared control such as crossbar architectures have been put forward [46], allowing for shared qubit control, work on the operation of qubits at high temperatures has been conducted[49] reducing the cooling power requirements of dilution refrigerators, and proposals for on-chip classical electronics are being experimentally investigated [10]. Solutions to these outstanding hurdles will be crucial to the further development of extensible qubit unit cells and therefore the scaling of quantum devices into practically useful regimes.

3.7. Conclusion

We presented a cross-platform integration scheme for multi-layer quantum dot arrays in group-IV semiconductor hosts. We successfully fabricated linear and 2D arrays of quantum dots and in the group IV platforms SiMOS, Si/SiGe and Ge/SiGe. We demonstrated single-electron and hole occupancy in double quantum dots confirmed by charge sensing. We showed stable quantum dots under each plunger in a SiMOS triple quantum dot linear array, depletable to the final charge state. In Si/SiGe, we demonstrated tune-up of a quintuple quantum dot array utilizing the N+1 method, successfully reaching the few-electron regime in each quantum dot simultaneously. Moreover, we showed we could form and sense double quantum dots in the single hole regime in each configuration of a 2x2 quadruple quantum

dot array in Ge/SiGe. We furthermore compared the capacitive crosstalk between quantum dots and gates. We find that the cross capacitance can be small and therefore argue that future work on strategies for the initial tuning of quantum dot arrays should address disorder rather than capacitive crosstalk, in particular for SiMOS quantum dots. We envision that our realization of an integration scheme to build quantum dots in SiMOS, Si/SiGe, and Ge/SiGe will boost the collective development toward large quantum dot arrays to build, simulate, and compute with quantum information.

3.8. Outlook

The ability to fabricate devices in multiple platforms using a similar process allows us to leverage off the work done in all three, speeding up progress while still making use of the advantage of each platform. Adapting recipes from the well-established SiMOS and Si/SiGe devices allowed for the rapid development of quantum dots and qubits in the new Ge/SiGe platform [31, 59–61].

Which of these platforms is most suitable for a quantum computer remains to be determined. While heterostructures generally have a better interface quality, a whole industry is built around CMOS, which SiMOS can take optimal advantage of. The low mobility of SiMOS, caused by a high interface defect density, could be the limiting factor. Quantum dots are smaller, their locations are dependent on these defects, and the coupling between two adjacent dots is harder to control. Nevertheless, we show in chapter 5 that still a high and tunable tunnel coupling can be achieved. While this places more stringent requirements on the fabrication, having small dots does reduce the sensitivity of the quantum dot to noise by reducing overlap with spin-carrying nuclei. Although the absence of a natural driving mechanism for SiMOS can be a disadvantage, it also removes a source of decoherence. Spin-orbit coupling causes an additional coupling of charge noise to spin noise for Ge/SiGe.

To study its feasibility, the remainder of this thesis will focus on SiMOS. This chapter will end with a discussion of some fabrication improvements specifically for SiMOS devices and the next chapters will study the feasibility of large-scale quantum computing in SiMOS.

3.9. SiMOS fabrication improvements

3.9.1. Gate anneal

In silicon MOS, anneals are generally used to repair damage caused by e-beam exposure [62] and to improve the structural quality of metal gates. We find that for SiMOS quantum dot devices, the quality of the gates can be improved by the incorporation of a forming gas anneal at 400 °C for 15 min each gate deposition. Figure 3.8a shows a scanning electron microscope (SEM) image of a device for which the anneal was implemented. Figure 3.8b-g show SEM and Atomic Force Microscopy (AFM) images for two gate layers of a SiMOS device. We observe a large reduction of surface roughness and sidewall height, which improves further the homogeneity and yield of the metallic gates.

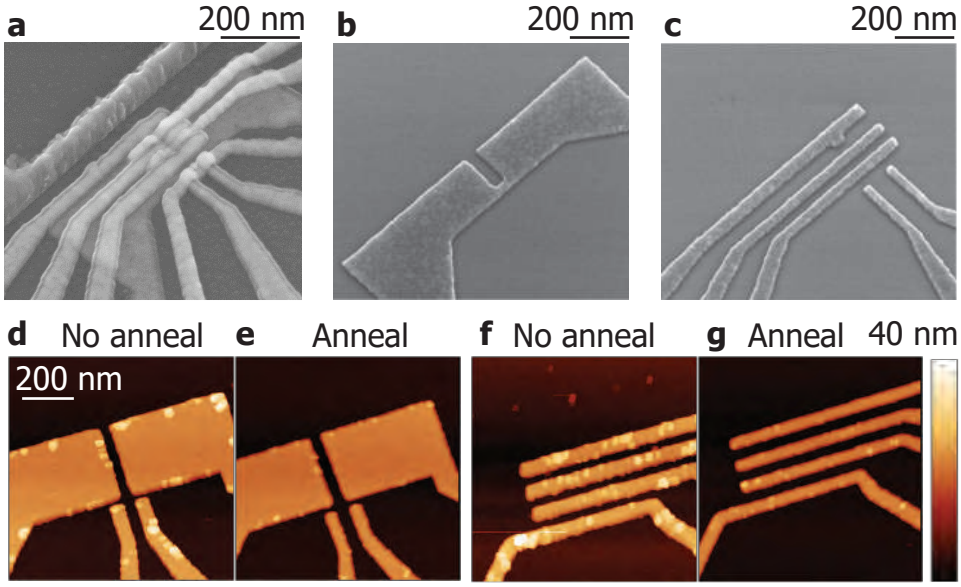

Figure 3.8: **Comparison of annealed gates**. **a**, **b**, **c** SEM images taken under a 30° angle of **a** full device fabricated with a gate anneal. **b**,**c** Separate layers after a gate anneal. **d** - **g** AFM images of separate gate layers **d**, **f** before and **e**, **g** after a gate anneal. The anneal results in a smoother surface with less grains and sidewalls.

3.9.2. Al_2O_3 window etch

Incorporating atomic layer deposition (ALD) of Al_2O_3 into the gate stack introduces further sources of charge noise [42] making it undesirable in the active region of spin qubits. On the other hand, it is necessary to prevent inter-gate leakage when utilizing a Ti:Pd multi-layer gate stack, as well as leakage to the substrate. In the case of SiMOS, fabrication begins on a 10 nm SiO_2 dielectric grown across the substrate. While high in quality, due to the sheer area overlap of gate fan-out, there is a non-negligible probability that a gate may overlap with a region of damaged dielectric. To prevent leakage of gate layers to substrate in our SiMOS stack, we find an initial blanket layer of Al_2O_3 is necessary. An etching process (see Appendix A.1 regarding fabrication details) with a high selectivity of Al_2O_3 over SiO_2 allows us to locally remove this layer in the active region. Figure 3.9 shows charge stability diagrams of two identically processed quantum dot devices in SiMOS where Al_2O_3 was present or where an oxide window was etched. Without etching, charge noise causes significant fluctuations in the quantum dot potential, which can be observed from the constantly shifting charge addition lines in Fig. 3.9a. Instead, when an oxide window is etched, we observe stable transitions, see Fig. 3.9b. We attribute this stability to the removal of the ALD layer beneath the first gate layer. We note that this behaviour is reproducible in and consistent with other SiMOS quantum dot devices fabricated with and without the removal of the initial ALD layer in the quantum dot active region. Whether the fluctuation two level systems (TLSs) is in

the AL_2O_3 itself or in the semiconductor, reducing the oxide thickness is expected to reduce charge noise [42].

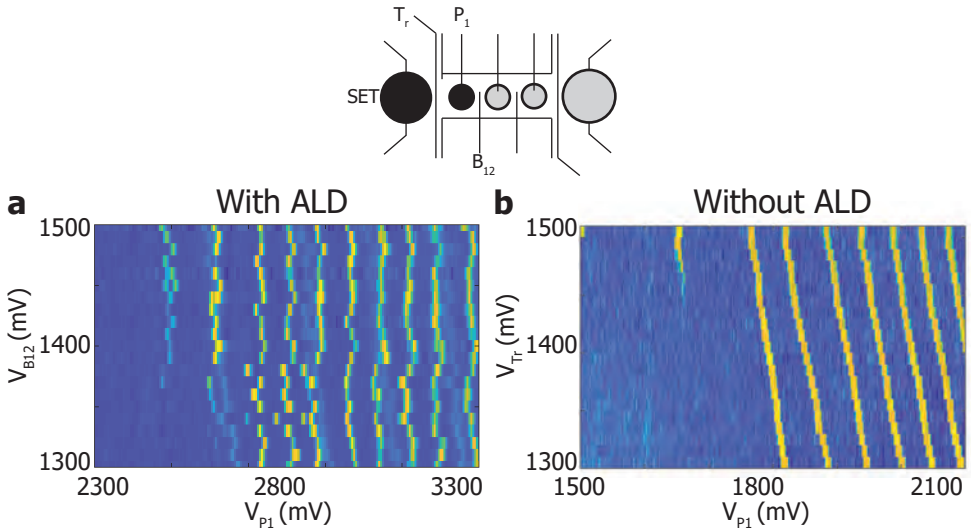

Figure 3.9: **Comparison of charge noise dependent on oxide window.** Charge stability diagrams displaying **a** Typical stability behaviour of a single quantum dot with a layer of Al_2O_3 beneath the screening layer. **b** Device processed with oxide window etch step with significantly improved stability compared to the **a**.

We can also operate this device in transport mode, which in principle could allow for quantum operations on four sets of tunnel coupled qubits. This requires the formation of double quantum dots in each channel, which we show in Supporting Fig 3. Here, we tune the reservoir-dot couplings low by closing the reservoir barrier gates. Formation of double dots is possible in each channel via transport.

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4

Silicon CMOS architecture for a spin-based quantum computer

The menu is not the meal.

Alan Watts

The classical-quantum interface remains a nascent field of exploration. In this chapter we propose an architecture for a silicon-based quantum computer processor based on complementary metal-oxide-semiconductor (CMOS) technology. We show how a transistor-based control circuit together with charge-storage electrodes can be used to operate a dense and scalable two-dimensional qubit system. The qubits are defined by the spin state of a single electron confined in quantum dots, coupled via exchange interactions, controlled using a microwave cavity, and measured via gate-based dispersive readout. We implement a spin qubit surface code, showing the prospects for universal quantum computation. Through the identification of key requirements for a spin qubit based quantum computer, significant challenges to qubit fabrication and operation become apparent. We discuss the challenges and focus areas that need to be addressed, providing a path for large-scale quantum computing.

Parts of this chapter have been published in **Nature Communications 8**, 1766 (2017) [1].

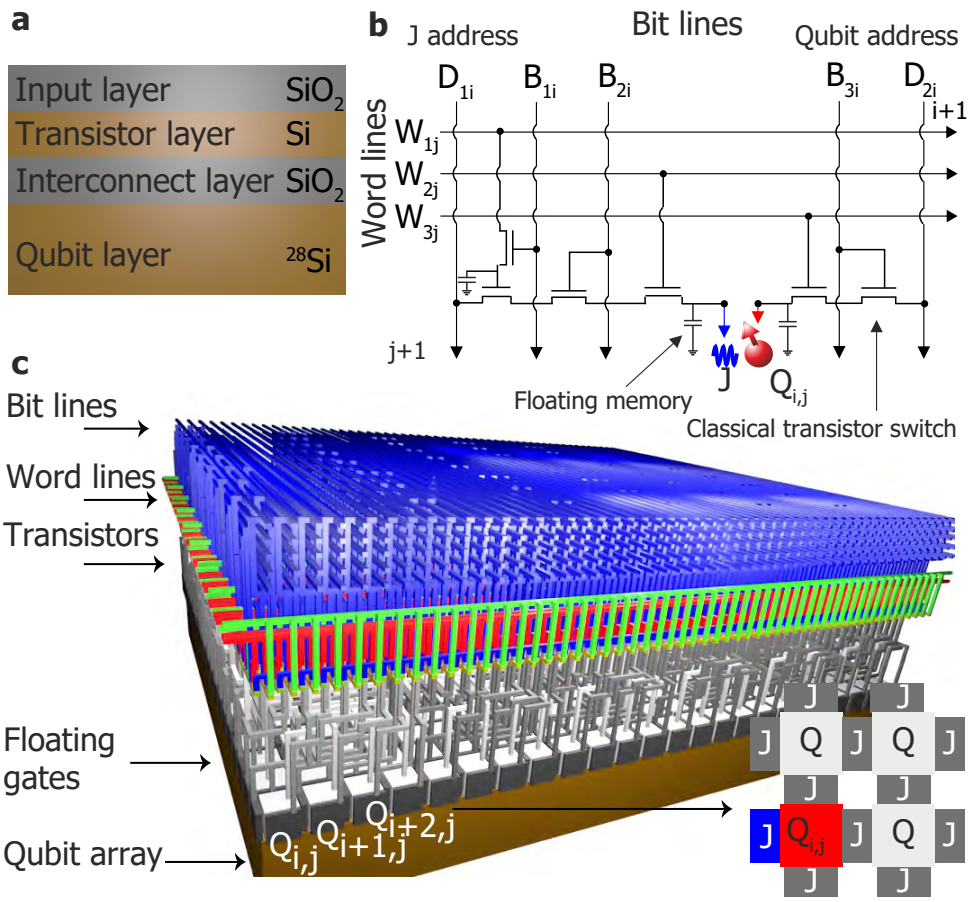

Figure 4.1: **Physical quantum processor.** **a** A silicon-on-insulator (SOI) wafer is processed, such that the bottom layer of isotopically enriched silicon-28 contains the 2D qubit array and the top layer of silicon forms the transistors to operate the qubits. These are interconnected through the oxide regions using polysilicon (or other metal) vias. **b** Electrical circuit for the control of one Q-gate and one J-gate allowing the required individual, row-by-row, or global operations, as explained in the main text. **c** Physical architecture to operate one unit module containing 480 qubits. The inset on the bottom right shows a plan view cross-section through the qubit plane. Each J gate and qubit is connected via the circuit shown in **b**.

4.1. Introduction

Advances in quantum error correction codes for fault-tolerant quantum computing and physical realizations of high-fidelity qubits in multiple platforms give promise for the construction of a quantum computer based on millions of interacting qubits. The most promising routes towards large-scale universal quantum computing all require quantum error correction (QEC) [2], a technique that enables the simulation of ideal quantum computation using realistic noisy qubits, provided that the errors are below a fault-tolerant threshold. Using the most forgiving methods, such as

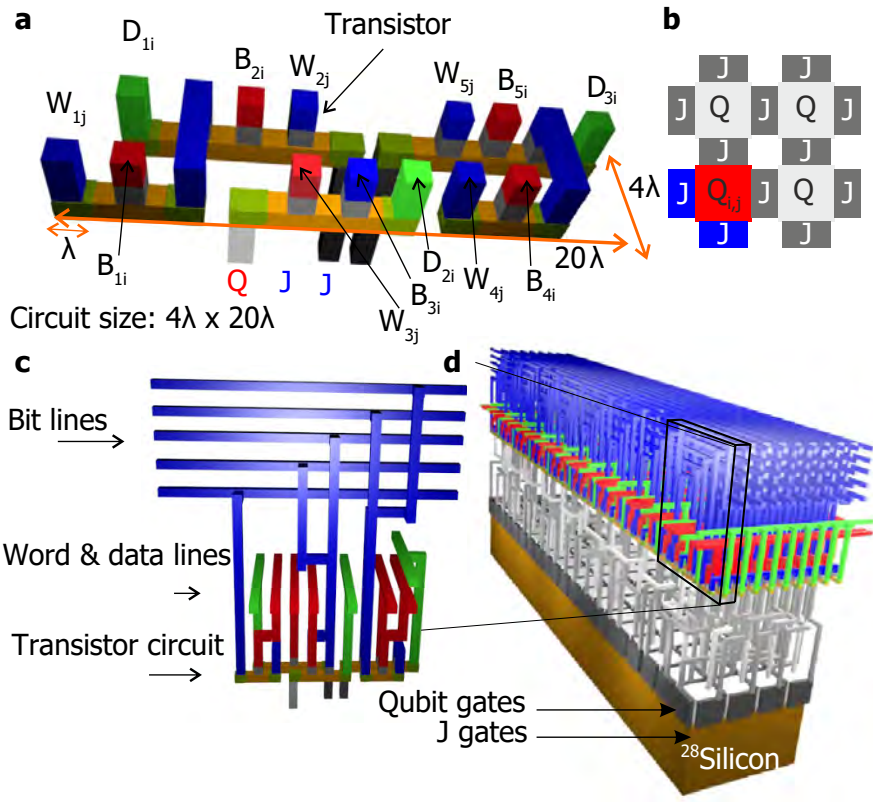

Figure 4.2: **Quantum processor integration scheme. a** Physical circuit for a single-qubit and two J-gates (see schematic **b**). The grey elements in **a** correspond to the transistor switches used to activate a line. The scale λ is the feature size, which is presumed constant for each metal or dielectric layer. **c** Same as **a**, but from a different perspective, in order to show how the word, bit, and data lines connect with the unit cell. **d** In order to match the difference in aspect ratios between the qubit layer and control layer, the control elements for a single-qubit and two J-gates are extended to a 4×20 qubit array. Another extension must be made to accommodate for the surface code sequences shown in Fig. 4.5, so that a single-qubit module becomes a 24×20 qubit array, as depicted in Fig. 4.1.

the two-dimensional surface code [3], these error thresholds can be as high as 1% [4], a level that is now routinely achieved across several qubit platforms [5–11]. However, these approaches also require a platform that can be scaled up to very large numbers of qubits, of order 10^8. Developing scalable qubit arrays constitutes one of the most stringent barriers in the field, even for the most promising platforms.

Silicon CMOS integrated circuits (ICs) are the prototypical example for scalable electronic platforms, now holding transistor counts exceeding billions. This remarkable level of integration is based upon decades of advances in silicon materials technologies [12], and these will also be crucial in the development of high-quality spin qubits. A key architectural aspect of ICs has been the use of parallel addressing via word lines and bit lines facilitating rapid read and write operations on large 2D

arrays of bits. Unfortunately, this method cannot directly be applied to scale qubit arrays. Unlike transistors, the tolerance levels of qubits are small, thereby requiring individual tunability.

Here, we show an advanced architecture for parallel addressing of silicon spin qubits and integrating highly-repetitive error correction methods like the surface code. In addition, we show that individual qubit stabilization is obtained via floating memory gate electrodes that can be routinely reset, similar to dynamic random access memory (DRAM) systems. Together, these allow the design of a platform where the number of addressing lines increases in a scalable manner proportional to $\sqrt{N}$, where N is the number of qubits. While silicon was recognized early on as a promising platform in the seminal work of Kane [13], leading to many novel architectures [14–20], a key and contrasting feature of our approach is that each architectural component is based on existing devices and commercially available technology to provide a scalable solution.

4.2. Physical architecture

The general architecture we propose is depicted in Fig. 4.1. We start with a silicon wafer, including an isotopically enriched silicon-28 layer. After CMOS manufacturing, the top layers host the classical circuitry, and the silicon-28 bottom layer holds the quantum circuit. These are interconnected via metal lines that penetrate the oxide region, see Fig. 4.1a. The fabrication could be performed monolithically, from a single wafer, or include flip-chip technologies to enable the construction of the two circuits separately. We focus here on single spin qubits confined in quantum dots [11]. The tremendous improvements in CMOS technology have resulted in feature sizes that are well below the minimum requirements for quantum dot definition. However, we envision that the small acceptable tolerance levels of qubits will require a certain number of control lines for tunability. In a dense 2D array, this set of requirements will then determine the minimum qubit size for an extendable structure. For complete qubit control, we use a single floating gate for quantum dot definition and a single floating gate for qubit coupling between each qubit. One data line (D_{2i}) is interconnected to each corresponding qubit (Q_i) to tune the qubit resonance frequency (ν_i), while a second (D_{1i}) interconnects to each J-gate to control the exchange coupling between qubits, shown in Fig. 4.1b. To provide individual, row, or global qubit addressing, the data lines are controlled by a combination of word lines (W) and bit lines (B). The required control circuit includes six transistors that connect the data lines via the word lines and bit lines to the floating gates. This circuit is extendable over multiple gates. For simplicity we have shown only one J-gate control structure, whereas an extendable structure contains two.

The size of a physical circuit for a single extendable element, as shown in Fig. 4.2a, will be highly dependent on the specific details of the CMOS fabrication process used. However, by assuming the minimal width of, and separation between, the gates and doped regions is equal to the minimum feature size λ, the classical circuit occupies an area $80\lambda^2$ per qubit. A feature size of 7 nm would require a minimum qubit size of $\approx$ 63 nm $\times$ 63 nm (including half the barrier area that separates the qubits), consistent with experimental realizations of silicon quantum

dot qubits [11, 21]. Large foundries are now capable of manufacturing some features down to this size, but ongoing advances in down-scaling will be needed to fabricate the classical devices assumed here, and so the development of such a quantum computer will therefore need to proceed hand-in-hand with the ongoing advances in semiconductor technology. For example, the industrial 14 nm node has a transistor fin width of only 8 nm, and a transistor gate pitch of 70 nm [22], consistent with a quantum dot size. Nonetheless, further down-scaling or advances in 3D technology would be needed to place several transistors above a quantum dot [23]. Alternatively, multiple transistors could be stacked in different layers, such that each individual transistor can be larger in size.

Generally, the most compact classical circuits have different geometries from quantum circuits. While a 2D qubit plane takes on a square shape due to square (or circular) shaped qubits, we found that this is generally not the case for the most optimal classical control layers. The situation is further complicated by the geometrical layout of the metal connection lines, determined by the quantum error correction implementation. To overcome the complexity in scaling these differently sized circuit components, we use vertically-stacked interconnection layers. After expanding to a large number of qubits, as described below, we can match the aspect ratios of the layers. We start with the basic control structure, which connects to a qubit and two J-gates, with the assumed single linewidth parameter λ, set by the feature size of the fabrication platform, see Fig. 4.2. The aspect ratio of the control structure is $4\lambda \times 20\lambda$. In order to match with a square qubit, we extend the control structure to a set of 20 × 9. This control structure addresses a qubit array 20 × 4, which has the same footprint. However, in order to match the surface code protocol discussed in section 4.5, we again have to extend the structure to hold 54 × 9 classical control structures for 24×20 qubits (note the presence of 6 redundant classical control structures that are required in order to match the aspect ratio).

As the number of qubits increases, the three layers become spatially identical. This point is reached upon expanding the structure to host 480 qubits, and an entire qubit module is shown in Fig. 4.1. Beyond this, further scaling becomes a straightforward replication of this 480 qubit module. A full quantum processor would then contain multiple modules and the edges would be connected to a doped silicon region, serving as an electron reservoir, from which electrons may be sequentially loaded into the qubit array as is done in charge-coupled devices [24]. The word and bit lines of the integrated quantum processor chip will then be connected to classical control and measurement electronics [25] that can reside next to or further away from the quantum chip depending on their level of power dissipation.

4.3. Electrical operation

We now turn to the electrical operation of the qubit module, Fig. 4.3 and Fig. 4.4, and consider a surface code that is specifically designed for quantum error correction and fault-tolerant operation of this CMOS processor, Fig. 4.5. We assume that the complete structure is maintained at cryogenic temperatures (~1 K or less) inside an electron spin resonance (ESR) system, which will be used to apply qubit control pulses. A single electron is loaded into each quantum dot by addressing the corre-

sponding word and bit lines and the electron occupancy is verified by gate-based dispersive readout, as shown in Fig. 4.3 and described further below. Each qubit must be calibrated to its desired qubit resonance frequency by tuning the associated floating memory gate, using electrical g-factor control, as has been demonstrated experimentally [11]. The surface code operation we discuss here requires a total of six different resonance frequencies (see Fig. 4.5). The need for six qubits instead of the more usual four qubits is because the readout is based on parity, which requires two qubits for measurement, as will be discussed in section 4.5 on surface code operations. The qubit gates (Q_{ij}) are calibrated using the data line (D_{ij}) to voltages such that the exchange coupling between adjacent qubits is negligible when the intermediate J-gates are set at an "off" bias point, and for which there is a common value of exchange when the J-gates are set to an "on" bias. Global (i.e. parallel) control is a crucial aspect for large-scale operation. The use of floating memory gates in the proposed architecture here has the significant advantage of enabling the individual tuning of qubits, while having a minimal number of control lines that can then be set to common bias levels, thus enabling global operations.

4.4. Gate-based dispersive readout and initialization

Two popular methods for spin qubit readout are based on spin to charge conversion: readout based on the Zeeman energy (using a reservoir) [26] and readout based on the singlet-triplet energy (via Pauli spin blockade) [27]. In tightly-confined silicon quantum dots, where the next orbital state is typically several meV above the ground state, the first excited state is the next available valley state, and so the relevant energy for the Pauli spin blockade protocol is largely determined by the valley splitting energy, which can be almost 1meV [28]. Both approaches can be made compatible with our control circuitry, but readout based on Pauli spin blockade can offer a number of advantages, including: (i) a larger relevant energy scale leading to higher readout fidelity; (ii) no necessity for a large electron reservoir for each qubit; and (iii) a large magnetic field is not required so that the qubit operating frequencies can be much lower, of order one GHz. We therefore propose to use Pauli spin blockade for parity readout between two spin qubits.

Dispersive readout [29–33] has been considered extensively for multi-dot qubits such as singlet-triplet qubits [27], but here we envision the readout of single spins by exploiting Pauli spin blockade. Single spin states can be projected onto singlet-triplet states using a reference neighbour dot, thus allowing a parity measurement between two qubits. We prepare the system at large detuning in the singlet (0,2) charge state, where the singlet is the ground state. Consequently, we decrease the detuning and pulse to the (1,1) charge state. Due to the Zeeman energy difference between the two dots, the singlet state evolves into the state where in the dot with the larger g-factor the spin state is $|\downarrow\rangle$ and in the dot with the smaller g-factor the spin state is $|\uparrow\rangle$ and this completes the initialization. In order to avoid transitions to other states, the pulsing speed is limited by the tunnel coupling and Zeeman energy difference between the qubits, which can be larger than 100MHz [34].

Qubit readout is based on the reverse process of initialization. We first control the spin of the reference dot (the dot with the larger g-factor) to the state $|\downarrow\rangle$ and

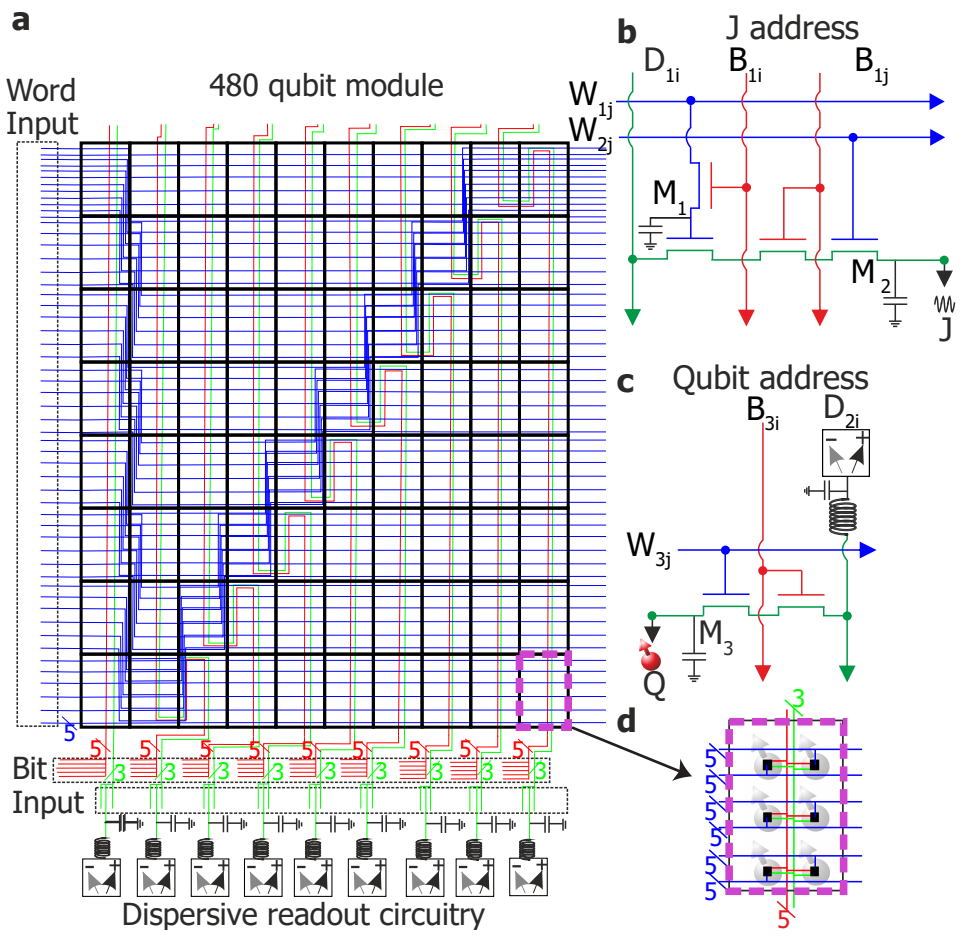

Figure 4.3: **Electrical circuit and qubit addressing scheme.** **a** Electrical wiring of the 480 qubit module. The word lines (W), bit lines (B) and data lines (D) can be addressed to enable global control, to couple and readout row-by-row and to individually (de)select qubits. The W and B lines are grouped in five and the D in three, such that a combination of these forms the lines of the electrical circuit of a single extendable structure, consisting of a single-qubit and two J gates. The zigzag structure in **a** is to accommodate for the different aspect ratios of qubit size and control size, and in order to be consistent with surface code operation. The electrical circuits in **b** and **c** show the corresponding structures to control the qubits and the exchange coupling between them. The floating memories M_1 and M_2 are to maintain the desired electric fields on the respective J and Q gates and may be periodically refreshed. Figure 4.4 shows the typical operation protocol of the electrical circuit shown in **b** and **c**. **d** displays the region that is occupied by 6 qubits, corresponding to a surface code unit cell (see Fig. 4.5b). Note that the word lines are connected to the qubits in an alternating arrangement in order to make the circuit compatible with our spin qubit surface code scheme.

then adiabatically pulse to the (0,2) charge state. If the measurement dot is in the state $|\downarrow\rangle$, the state will remain in the (1,1) charge state due to Pauli spin blockade whereas if the measurement dot is in the state $|\uparrow\rangle$, the end state will be the singlet with (0,2) charge state. Pulsing close to zero-detuning results in a movement of

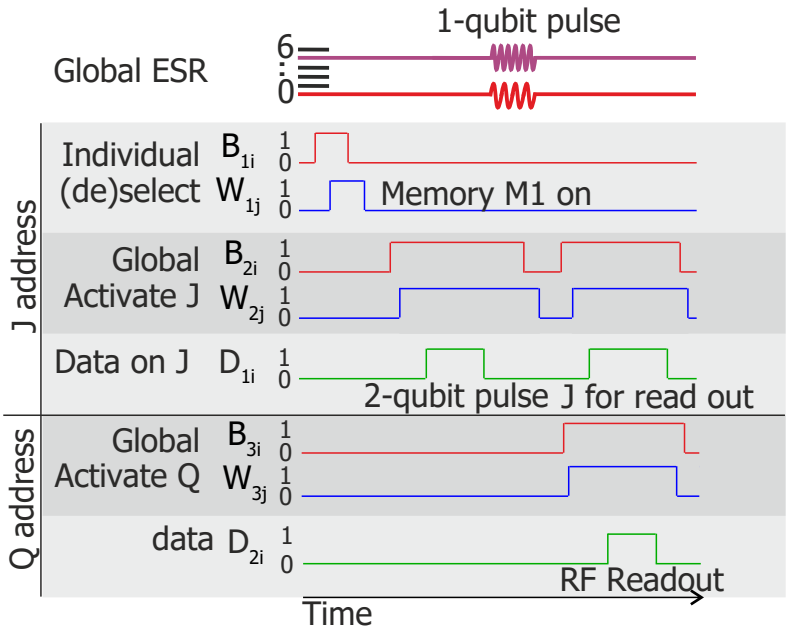

Figure 4.4: **Typical operation protocol** of the electrical circuit shown in Fig. 4.3 **b** and **c**. Individual qubit selection is via lines W_1 and B_1 that (de)charge floating electrodes ($M1$ in **b**) and (dis)connect the data lines from the corresponding J-gates. Two-qubit operations are performed by activating the associated lines W_2 and B_2 and sending a pulse through data line D_1. Global single-qubit operations can be applied by broadcasting an ESR pulse at the resonance frequencies of the corresponding subgroup of qubits at any time of the sequence. Readout is enabled via the lines W_2, B_2, W_3, and B_3. Then a pulse turns on the selected J gates, and RF readout is performed via the data line D_2 connected to the qubit.

charge only if the measurement dot is in the state $|\uparrow\rangle$ and this can be detected using gate-based dispersive readout [29–33], see Fig. 4.2. Avoiding spin relaxation will be a particular challenge to achieve high-fidelity, thus requiring a fast protocol and absence of relaxation hot-spots in the pulsing regime [28].

The readout is performed in a row-by-row manner and the parity analysers are connected to the data lines D_{2i} via bias tees, see Fig. 4.3c. Using classical circuitry, it is possible to frequency multiplex an entire row [35] so that only one RF analyser circuit is needed, however the number of channels will be limited due to crosstalk and finite bandwidth. For large qubit numbers, a combination of multiple analysers, as depicted in Fig. 4.3a, and temporal multiplexing could provide solutions. Operating dispersive readout at 1 GHz enables readout on timescales of order 10-100 ns, so that a large qubit array could be read out well within the single-qubit coherence time of 28ms in ^{28}Si substrates [11]. A combination of these multiplexing schemes can be used depending on available space, frequency bandwidth and time.

To be able to perform parallel operations, an integrated 3D arrangement of the addressing and qubit structures is required, such that a certain combination of word lines and bit lines will address the same particular qubit in each unit cell. This is

implemented in the schematic in Fig. 4.3d, with a unit cell of 2x3 qubits. This size is based on the required 2 data qubits and 4 measurement qubits for surface code operations using parity readout (explained in section 4.3). For other qubit encoding schemes, different unit cells could be preferable. To deselect individual qubits, the J-gates surrounding the relevant qubits are deactivated (see Fig. 4.4), thereby isolating them from the data qubits and creating an additional degree of freedom in the array for quantum computation. This protocol will be particularly relevant for the operation of the defect-based surface code.

4.5. Surface code operations

Surface codes are among the most promising methods for quantum error correction [2, 4]. The standard surface code cycle and unit cell [4] are shown in Fig. 4.5a. The protocol contains a sequence of CNOT operations together with single-qubit Hadamards, readout and initialization steps. An alternating arrangement of data and measurement qubits is used, where two data qubits interact with four measurement qubit neighbours. In our approach, we perform readout with spin to charge conversion based on the singlet-triplet energy (via Pauli spin blockade). This parity readout process requires two qubits, and so the surface code unit cell expands to six qubits, as shown in Fig. 4.5b. This implementation is thus slightly larger than the usual surface code unit cell of four qubits. In order to access all sites, an additional SWAP operation is included (step 5 in Fig. 4.5b). The CNOT operation is realized by a combination of a CPHASE gate interleaved between two single-qubit rotations, shown in Fig. 4.5b. The CPHASE gate is created by turning the interaction on, such that the qubits will acquire a time-integrated phase dependent on the spin state of the coupled qubit [36]. A SWAP operation can be realized in a similar way, but requires the tunable qubit resonance frequency difference to be much smaller than the interaction strength.

The measurement qubits are initialized to $\mathcal{I}$ by adiabatically moving from the (0,2) charge state to the (1,1) charge state, as discussed in the section Gate-based dispersive readout and initialization. Single qubit Hadamard operations and the two-qubit CPHASE and SWAP operations are then performed, followed by measurement of the spin states using dispersive readout. This projective measurement of a system of multiple qubits enables non-destructive quantum error correction of single-qubits. The complete surface code cycle for quantum dot qubits, see Fig. 4.5b, then involves ten steps.

The focus of the work presented here is the design of a manufacturable 2D qubit array architecture, and we envision that many different surface code schemes and even analog quantum simulator algorithms can be constructed based on our design. We therefore do not undertake here a detailed analysis of the particular error thresholds associated with our surface code implementation. A new fault-tolerant error threshold will need to be calculated for each particular qubit encoding and manipulation scheme, and this is a crucial challenge that needs to be addressed in the future. We expect that the associated fault-tolerant error thresholds can be large, given that the number of operations is comparable with those previously reported [4]. Recent demonstrations of single- and two-qubit gates in silicon [11, 36]

provide significant scope to meet all the required fault-tolerant thresholds. Further improvements in two-qubit fidelities are conceivable, for example via operation at the charge symmetry point for a pair of quantum dot qubits [37, 38].

To perform logical quantum operations on the qubit module with a defect-based surface code, qubit deselection is required to create holes for braiding operations [4]. Individual qubit (de)selection is enabled by the circuit shown in Fig. 4.3b, using word and bit lines W_{1j} and B_{1i}. The required holes will be limited, as most physical qubits will be used to create the logical qubits. The infrequent nature of required qubit (de)selection allows for this to be done individually, rather than globally, and we achieve this by deactivating the associated J-gates, thereby isolating the associated data qubits from their measurement qubits.

4.6. Heat dissipation

A critical factor for almost any large-scale computing platform is cooling power. A detailed analysis based on a specific design and targeted operation, going beyond this work, will therefore be highly valuable. Focus areas contributing to the total power dissipation include the dynamic power produced by the J-gates. The power dissipation of a single surface code unit cell, shown in Fig. 4.5b, is $P = CV^2\alpha f$, with C the capacitance of the floating memory, V the switching voltage, and α the activity factor relative to the surface code clock cycle with frequency $f \approx 0.1$ MHz (assuming Rabi frequencies on the order of 1MHz [11]). The surface code unit cell is operated using 54 transistors and during a full cycle the J-gate activity $\alpha = 12$. The floating gate electrodes may be periodically refreshed, as in DRAM technology, but we estimate that for high-fidelity qubit operation RC times beyond one second will be required to avoid significant drifts during operation. We assume this requires a capacitance $C \approx 1$ pF, with an associated Johnson-Nyquist thermal noise $V_{\text{thermal}} = \sqrt{K_B T/C} \approx 1$ µV, providing a tolerable level [36]. Assuming a switching voltage $V = 0.2$ V results then in a power dissipation for a single unit cell of ≈ 50 nW. This power, however, can be dissipated at a higher temperature stage and superconducting lines can connect the circuit to remote current sources isolating the qubit chip from the dissipation.

Dissipation through leakage, however, can pose a serious challenge and will require significant cooling. Recent experiments using floating gates showed drifts of approximately one Coulomb oscillation per hour ($\approx$ 8mV/h) [39], giving prospects that with frequent refreshing minimal voltage shifts will be caused provided dissipation can be handled. Large dilution refrigerators can already provide more than 1 mW cooling power at 100 mK. The ultimate local cooling power is therefore most likely limited by the thermal conductivity of the circuit. We now consider the cooling from the top through the upper layers of the circuit hosting the addressing lines. The thickness will depend on the exact implementation, but assuming ten to twenty stacked metallic layers we estimate that the total thickness of the lines will be below 5 µm. These lines could be made out of polysilicon with a thermal conductivity $\kappa = 100$ W/m/K at temperatures close to zero Kelvin. The surface code unit cell for spin qubits occupies an area 480 λ^2, such that for $\lambda = 7$ nm the available cooling power

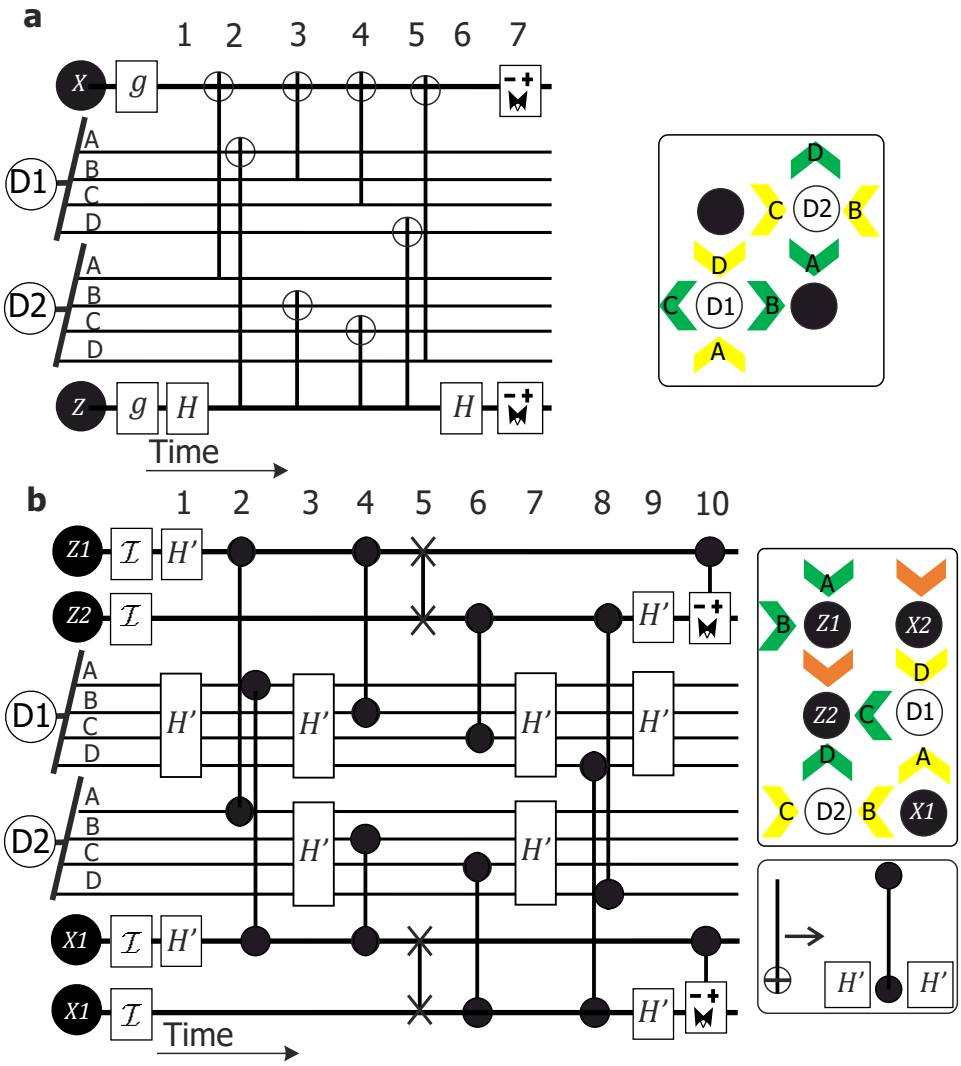

Figure 4.5: **Surface code operation. a** General surface code operation [4] and **b** surface code operation for spin qubits. To match this error correction scheme with a spin qubit system, the CNOT gate is decomposed into CPHASE and Hadamard operations, which are elementary operations for quantum dot qubits. CPHASE operations with quantum dot qubits usually result in additional $\hat{z}$ rotations, which can be corrected using single-qubit gates. Here this is included in the Hadamard, resulting in a Hadamard-like operation. Readout is via a parity measurement requiring two quantum dots, such that a unit cell consists of six (schematic in **b**) instead of the usual four (schematic in **a** [4]) qubits. A single unit cell contains now two data qubits, D_1 and D_2, and four measurement qubits, Z_1, Z_2, X_1 and X_2. Each of these qubit classes has a well-defined independent qubit resonance frequency. To enable all nearest neighbour operations, an additional SWAP operation is included, resulting in protocol **b**. A single cycle of initialization, control, and readout corresponds to ten steps. Note that the labels A, B, C and D refer to the data qubits associated with the respective measurement qubit.

is ≈ 500 nW/K per unit cell. Taking the 50 nW estimate of the power dissipation of a unit cell, we thus estimate that the architecture can operate at 100 mK, even if all dynamical power is dissipated at the lowest temperature stage. We note that while this is a rough estimate, silicon metal-oxide-semiconductor (MOS) spin qubits have a significant potential for qubit operation at higher temperatures, due to the large energy scales of their excited states and measured valley splittings, exceeding 10 K [28]. Further reductions in the required cooling power can be made by reducing the operation voltage, which is foreseeable at cryogenic temperatures, but possibly also by utilizing single-electron-transistors for the switching elements [40], thereby significantly lowering the switching voltage.

A more specific analysis of the dissipated power will need to be done for different layouts, to determine the main contributors and limits. A significant challenge will be the design of nano-sized capacitors; which will likely require a vertical geometry to meet the small feature sizes set by the quantum dot dimensions. Depending on operation temperature, required resolution, and shaped pulses that can reduce sensitivity to noise, capacitor values below 1 pF could be sufficient. An important engineering challenge will therefore be the optimization and demonstration of capacitors that are comparable in size with the quantum dots.

4.7. Discussion

The conceptual architecture shown here demonstrates that an array of single electron spins confined to quantum dots in isotopically purified silicon can be controlled using a scalable number of control lines. We have shown that the often argued compatibility of silicon spin qubits with standard CMOS technology is non-trivial. However, the proposal presented here for quantum dot qubits, provides scope for fabrication made consistent with standard CMOS technology and opportunities to scale up to thousands or even millions of qubits. Provided that the down-scaling of CMOS transistors continues as anticipated, the control and measurement circuitry described can be integrated with qubits of a size that have already been experimentally demonstrated [11, 21, 36]. The combination of ESR control, exchange coupling and dispersive readout of this design enables surface code operations to be performed using this platform. A key advantage is the possibility of global qubit control, so that many qubits can be addressed within the qubit coherence time.

The proposed architecture is based on the current experimental status of silicon qubits and requires multiple transistors per qubit, significantly challenging CMOS manufacturing capabilities. Advancements in device uniformity and reproducibility could lower the number of required transistors. For example, with more uniform qubits the tuning circuitry and associated floating gates might not be needed. Additionally, operating at low magnetic fields will result in uniform qubit frequencies, avoiding the need for g-factor tuning. This limits functionality, since single-qubit gates can then be applied only globally, but universal computing is still possible using the local two-qubit gates. We anticipate that 2D arrays with such limited functionality can be realized in the near future, and will aid in the development of the universal quantum processor as presented here.

The architectural concept of using floating gates to compensate qubit-to-qubit

variations, and the integration of crossbar technology to efficiently address a large qubit array, could be applied to a number of platforms, including spin qubits based on either Si/SiO_2 or Si/SiGe heterostructures, and adapted for various modes of operation such as single spin qubits [11, 21], singlet-triplet qubits [41], exchange-only [42] or hybrid qubits [43]. The system we considered here requires only local exchange interactions, but the architecture could also be incorporated into larger architectures that include long-range qubit coupling [15, 44–46], for example to interconnect quantum structures as presented here. While we consider the fabrication including a single layer of classical elements, a more advanced and complex fabrication process could include multiple stacked layers to allow for more complex classical electronics per qubit, or for a separate control circuit that is purely dedicated for calibration and stability. A more sophisticated design could also include frequency multiplexing along a row, allowing global readout. These are a few of the many opportunities for spin qubits that could provide solutions to the challenges presented here, including the limited available cooling power at lower temperatures and the requirement for small feature sizes. While the full fabrication and operation of our architecture is a formidable task, we believe that the identification of the key requirements for a spin qubit quantum computer fully engineered using semiconductor manufacturing paves the way towards an era of large-scale quantum computation; using the same silicon chip technology that has defined our current information age.

4.8. Outlook

The architecture proposed in this chapter is based on a dense array of qubits with individual control, but one might also think of different archetypes. The qubit array can be split up into smaller modules, connected via long range couplers, with room for control electronics in between [47]. A crossbar layout can greatly reduce the number of necessary control lines by using shared control, granted there is sufficient uniformity of qubits [48]. A sparsely populated array [49] puts less strict requirements on the density of qubits and control electronics. A crucial aspect in any architecture is the integration of control electronics and dealing with their heat dissipation [47]. Below 100 mK, cooling power is limited. At higher temperatures, above 1 Kelvin, different methods with orders of magnitude higher cooling power become available. This has sparked the field of hot qubits, experimenting on qubit operation at higher temperatures. In any case, development is required in multiple areas. The following chapters of this thesis address recent results that are relevant for this architecture.

The proposed exchange coupling control by using a J-gate requires control over the tunnel coupling between two quantum dots by a single gate, which will be demonstrated in a SiMOS double quantum dot device in **chapter 5**. To be able to operate at elevated temperatures, it is crucial to understand the temperature dependence of qubits. **Chapters 6 and 7** describe an investigation of the temperature dependence of several properties of SiMOS spin qubits, and their operation at temperatures above 1 Kelvin. Similar work done in parallel at the University of New South Wales [50] as well as experiments on hole spin qubits [51] further supports

these milestones achieved in silicon.

In addition to this academic work, industry partners have joined the effort of qubit fabrication and SiMOS quantum dots are now reproducibly fabricated in foundries [52–55]. These developments bring us closer to the point where qubits can be fully integrated into classical silicon electronics, allowing us to take full advantage of the industry compatibility of this technology.

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5

Tunable coupling and isolation of single electrons in SiMOS quantum dots

The more we value things outside our control, the less control we have.

Marcus Aurelius

This chapter demonstrates the achievement of a highly tunable tunnel coupling between single electrons in SiMOS quantum dots. Long coherence times, excellent single-qubit gate fidelities and two-qubit logic have been demonstrated with silicon metal-oxide-semiconductor spin qubits, making it one of the leading platforms for quantum information processing. Despite this, a long-standing challenge in this system has been the demonstration of tunable tunnel coupling between single electrons. Here we overcome this hurdle with gate-defined quantum dots and show couplings that can be tuned on and off for quantum operations. We use charge sensing to discriminate between the (2,0) and (1,1) charge states of a double quantum dot and show excellent charge sensitivity. We demonstrate tunable coupling up to 13 GHz, obtained by fitting charge polarization lines, and tunable tunnel rates down to below 1 Hz, deduced from the random telegraph signal. The demonstration of tunable coupling between single electrons in a silicon metal-oxide-semiconductor device provides significant scope for high-fidelity two-qubit logic toward quantum information processing with standard manufacturing.

Parts of this chapter have been published in **Nano Letters 19**, 8653-8657 (2019) [1].

5.1. Introduction

Quantum computation with quantum dots has been proposed using qubits defined on the spin states of one [2], two [3] or more [4, 5] electrons. In all these proposals, a crucial element required to realize a universal quantum gate set is the exchange interaction between electrons. The exchange interaction is set by the tunnel coupling and the detuning, and gaining precise control over these parameters enables to define and operate qubits at their optimal points [6–9]. Excellent control has already been reported in GaAs [6, 7, 10], strained silicon [11, 12] and more recently in strained germanium [13–16]. Reaching this level of control in silicon metal-oxide-semiconductor (SiMOS) quantum dots is highly desired as this platform has a high potential for complete integration with classical manufacturing technology [17–19]. This becomes apparent from many proposals of architectures for large-scale quantum computation [2, 20–25] that make use of full control over the exchange interaction. However, current two-qubit logic with single spins in SiMOS is based on controlling the exchange using the detuning only [26] or is executed at fixed exchange interaction [27].

A first step toward the required control has been the demonstration of tunable coupling in a double quantum dot system operated in the many-electron regime, where gaining control is more accessible owing to the larger electron wave function [28, 29]. More recently, exchange-controlled two-qubit operations have been shown with three-electron quantum dots [30]. However, tunnel couplings between single electrons that can be switched off and turned on for qubit operation still remain to be shown in SiMOS.

In this work we show a high degree of control over the tunnel coupling of single electrons residing in two gate-defined quantum dots in a SiMOS device. The system is stable and no unintentional quantum dots are observed. We are able to measure charge transitions using a sensitive single-electron-transistor (SET) as charge sensor and characterize the system in the single-electron regime. From a comparison of charge stability diagrams of weakly and strongly coupled double quantum dots, we conclude that we control the tunnel coupling by changing quantum dot location. We show that we can effectively decouple the double quantum dot from its reservoir and control the inter-dot tunnel coupling of the isolated system with a dedicated barrier gate. We quantify the tunability of the coupling by analysing charge polarisation lines and random telegraph signals, and find tunnel couplings up to 13 GHz and tunnel rates down to below 1 Hz.

5.2. Device layout

Figure 5.1a shows a scanning electron micrograph (SEM) of a SiMOS device nominally identical to the one measured and Fig. 5.1b shows a schematic cross-section of the quantum dot region along the dashed line in Fig. 5.1a. A high quality wafer is realized [17] with a 100 nm ^{28}Si epilayer with an 800 ppm residual ^{29}Si concentration [31], covered by 10 nm thermally grown SiO_2. Ohmic contacts are made by defining highly doped n^{++} regions by phosphorus-ion implantation. We use an overlapping gate integration scheme [11, 32, 33] and use palladium (Pd) gates,

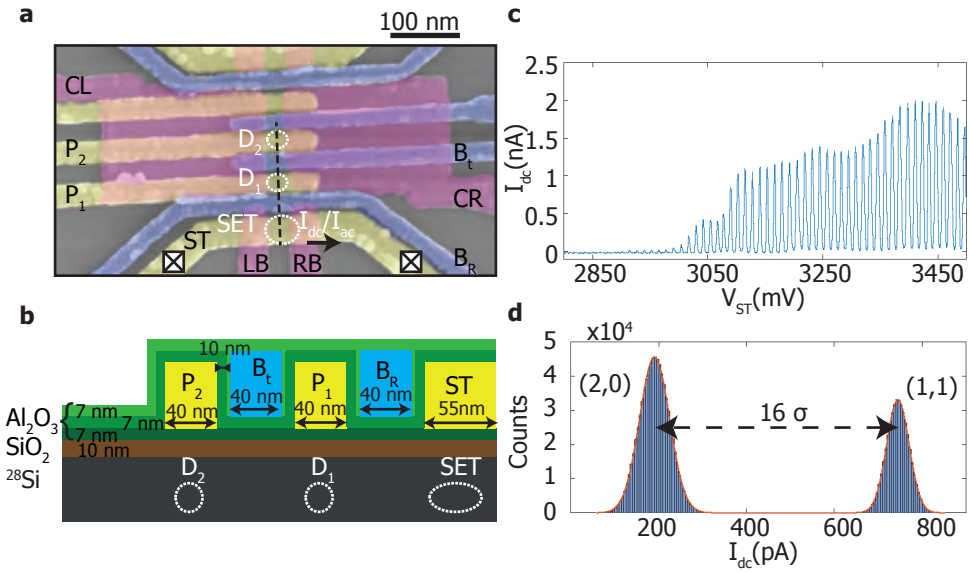

Figure 5.1: **Device layout and SET characterisation.** **a** False-colour scanning electron micrograph (SEM) of a device identical to the one measured. Purple, yellow and blue colourings correspond to the first, second and third metal layers respectively. Crossed boxes indicate the ohmic source and drain contacts used to measure I_{dc} and I_{ac}, circles indicate the intended location of the quantum dots D_1 and D_2 and the single-electron-transistor (SET). The quantum dots are defined using gate electrodes P_1 and P_2, confined laterally using CL and CR. B_t controls the tunnel coupling between the quantum dots and B_R the tunnel coupling to the SET. **b** Schematic of a cross-section of the device along the quantum dot region (dashed line in **a**), indicating key dimensions and dot locations. **c** Transport source-drain current I_{dc} versus top gate voltage V_{ST} of the SET defined using gate electrodes ST, LB and RB. Regular spacing of Coulomb peaks indicates a well-defined quantum dot, ideal for charge sensing. **d** Histogram of the charge sensor current as a response to (2,0)-(1,1) tunneling events. The counts are extracted from 4655 single-shot traces with integration time t_i= 82 μs, measurement bandwidth 0-50 kHz, and bin size b = 5 pA. The peaks are fitted with a double Gaussian with $\sigma_{(2,0)}$ = 34.1 pA and $\sigma_{(1,1)}$ = 25.5 pA, giving a peak spacing of over 16 $\sigma_{(2,0)}$.

which have the beneficial property of small grain size [34]. The gates are electrically isolated by an Al_2O_3 layer grown by atomic layer deposition. The sample is annealed at 400 °C in a hydrogen atmosphere to repair e-beam induced damage to the silicon oxide and to reduce the charge trap density [35, 36].

5.3. Charge readout

Figure 5.1c shows the current through the SET, electrostatically defined using gates ST, LB and RB, that is used as charge sensor and as an electron reservoir. The highly regular coulomb peak spacing indicates a well-defined quantum dot, which has a constant charging energy of approximately 0.9 meV. We extract a gate capacitance of 13 aF, in agreement with a simple parallel plate capacitor model. We form a double quantum dot between the confinement barriers CL and CR, using the gates P_1 and P_2 to tune the quantum dot potentials. B_t and B_R are used to control the

tunnel coupling between the quantum dots and from the quantum dots to the SET, respectively.

We characterize the charge readout sensitivity by recording the random telegraph signal (RTS) originating from the tunnelling of the electrons between the (2,0) and (1,1) charge states with $\Gamma_c \approx 48$ Hz, with Γ_c being the inter-dot tunnel rate. The fidelity of the (2,0)-(1,1) charge readout is often limited by the sensitivity of the charge sensor to inter-dot transitions. We have designed and positioned the SET with respect to the double quantum dot in such a way that this sensitivity is maximized. Figure 5.1d shows a histogram of the measured readout signal, using an integration time $\tau = 82$ μs. We fit the counts with a double Gaussian curve with $\mu_{(2,0),(1,1)}$ and $\sigma_{(2,0),(1,1)}$ the mean and standard deviation of the Gaussian distributions corresponding to the two charge states. We find $\Delta\mu_{(2,0)-(1,1)} > 16\ \sigma_{(2,0)}$ corresponding to an excellent discrimination between the (2,0) and (1,1) charge states.

5.4. Strong and weak coupling of a double quantum dot

To precisely measure charge transitions, we implement charge sensing using a lock-in amplifier and apply a square wave excitation at $f_{ac} = 77$ Hz on the gate B_t. Figure 5.2a and 5.2b show the double quantum dot charge stability diagrams of the charge sensor response as a function of V_{P2} and V_{P1} for weak ($V_{Bt} = 2.9$ V) and strong ($V_{Bt} = 3.6$ V) coupling. Horizontal and vertical blue lines indicate the loading of an additional electron from the SET to quantum dots D_1 (located under the gate P_1) and D_2 (located under P_2) respectively, while diagonal yellow lines indicate electron transitions between the two quantum dots. We do not observe more charge transitions at voltages lower than the measured range and we conclude that the double quantum dot is in the single electron regime. In order to highlight the difference between weak and strong coupling, Fig. 5.2c and 5.2d show higher resolution maps of the (2,0)-(1,1) anticrossing.

When we set a weak inter-dot coupling, charge addition lines of D_2 are barely visible in the charge stability diagram, because of the low tunnel rate between D_2 and the reservoir. This indicates that the tunnel rate is significantly smaller than the excitation frequency applied to the gate. Similarly, at the (2,0)-(1,1) inter-dot transition, no transitions between the quantum dots can be observed because of the low inter-dot coupling. The loading of the first electron in D_2 can only be observed from the shift of the D_1 charge addition line, caused by the mutual capacitance E_m of the two quantum dots. Only in the multi-electron regime where the quantum dot wave functions are larger and have more overlap, the coupling is sufficiently high to observe charge transition lines.

When the inter-dot coupling is strong, charge addition lines belonging to D_2 are visible near the anticrossings and at high V_{P1}, where Γ_{R2} is increased. Additionally, t_c and E_m are increased and we observe a honeycomb shaped charge stability diagram, with clearly visible inter-dot transition lines, even when only a single electron is loaded on each quantum dot.

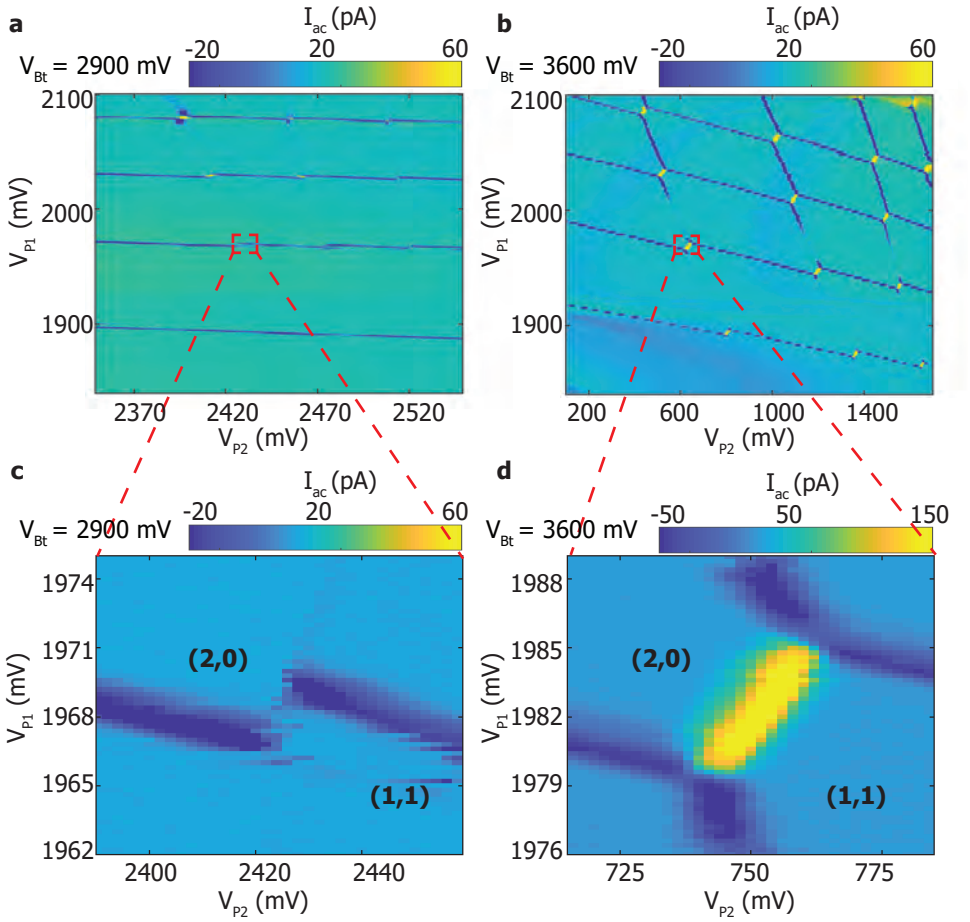

Figure 5.2: **Double quantum dot charge stability diagrams. a**, **b** Charge stability diagrams of the charge sensor response I_{ac} as a function of voltages V_{P_2} and V_{P_1} of a double quantum dot for weak (**a**, V_{Bt} = 2.9 V) and strong (**b**, V_{Bt} = 3.6 V) coupling. Electrons are loaded from the SET. Transitions with a tunnel rate $\Gamma < f_{ac}$ are not visible. **c**, **d** High resolution zoom in of the (2,0)-(1,1) anticrossing for both weak (**c**) and strong (**d**) tunnel coupling.

We estimate the relative location and size of the quantum dots from the gate voltage differences $\Delta V_{P1(2)}$ needed to load the second electron with respect to the first electron. We additionally use the cross-capacitances $\alpha_{r1(2)}$ of the plunger gates, determined by measuring the shift in $V_{P1(2)}$ of the charge transition line of the first electron in $D_{1(2)}$ as a function of a step in $V_{P2(1)}$, where $\alpha_{r1(2)}$ is the ratio between the shift and the step.

When the coupling is weak, we find $\Delta V_{P_1} \approx 70$ mV, $\alpha_{r1} < 0.05$ for D_1 and $\Delta V_{P2} \approx 50$ mV, $\alpha_{r2} \approx 0.33$ for D_2. We conclude that we have a system of two weakly coupled quantum dots located under P_1 and P_2.

We now analyse how the locations of D_1 and D_2 change from the changes in

ΔV_P and α_r. For D_1, both ΔV_{P1} and α_{r1} are almost independent of the coupling. For D_2, ΔV_{P2} increases by a factor 11, from $\Delta V_{P2} \approx 50$ mV for weak coupling to $\Delta V_{P2} \approx 550$ mV for strong coupling, while α_{r2} increases by a factor 5, from 0.3 to 1.5. The increase in α_{r2} can be explained by a change in the location of D_2 toward the gate P_1, to a position partly below the gate B_t. This change of quantum dot location will decrease the lever arm and this is likely the cause of the increase in ΔV_{P2}. We conclude that tuning from weak to strong coupling causes the location of D_2 to shift from a position mostly under P_2 to a position partly below B_t, while D_1 is stationary under P_1. The ease with which D_2 can be displaced additionally suggests that no unintentional quantum dots are formed between barrier gates.

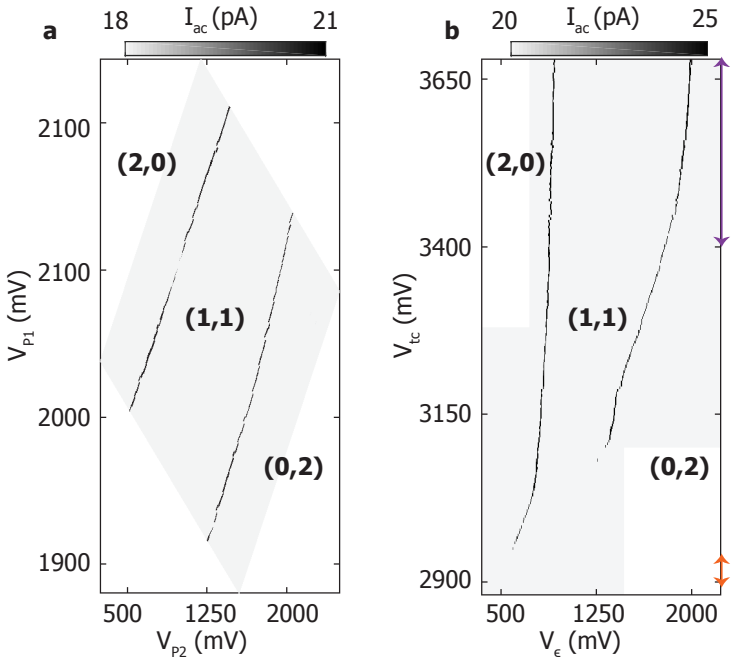

Figure 5.3: **Charge stability diagrams of an isolated double quantum dot. a** Map of the isolated (2,0)-(1,1) and (1,1)-(0,2) anticrossings as a function of V_{P2} and V_{P1}. No additional electrons are loaded into the quantum dot islands due to a negligible Γ_R. **b** Map of the (2,0)-(1,1) and (1,1)-(0,2) anticrossings as a function of detuning and barrier voltage. The relative lever arm between V_{tc} and V_ϵ changes at lower barrier voltages, due to a change in quantum dot location. The orange and purple arrows indicate the ranges in which the tunnel coupling was determined using RTS and polarisation line measurements respectively, see Fig. 5.4.

5.5. Isolation of the quantum dot system

By reducing V_{BR}, the tunnel rate Γ_R between the the SET reservoir and the quantum dots can be reduced and the loading and unloading of electrons can be prevented, resulting in an isolated quantum dot system [37, 38]. Because the reservoir is connected to room temperature electronics, decoupling the quantum dot from it

may provide the advantage of reduced noise [39]. Figure 5.3a shows the (2,0)-(1,1) and (1,1)-(0,2) anticrossings as a function of V_{P2} and V_{P1} when the coupling is strong. Only inter-dot transition lines are present over a wide range of voltages, much larger than the ΔV_P extracted in the previous section. This implies that no additional electrons are loaded, as a result of a negligible coupling to the reservoir. The ability to control the inter-dot transitions of a double quantum dot without loading additional electrons provides good prospects for the operation of quantum dot arrays that are only remotely coupled to reservoirs, as proposed in quantum information architectures [20, 22, 23]. We control the tunnel coupling t_c with the

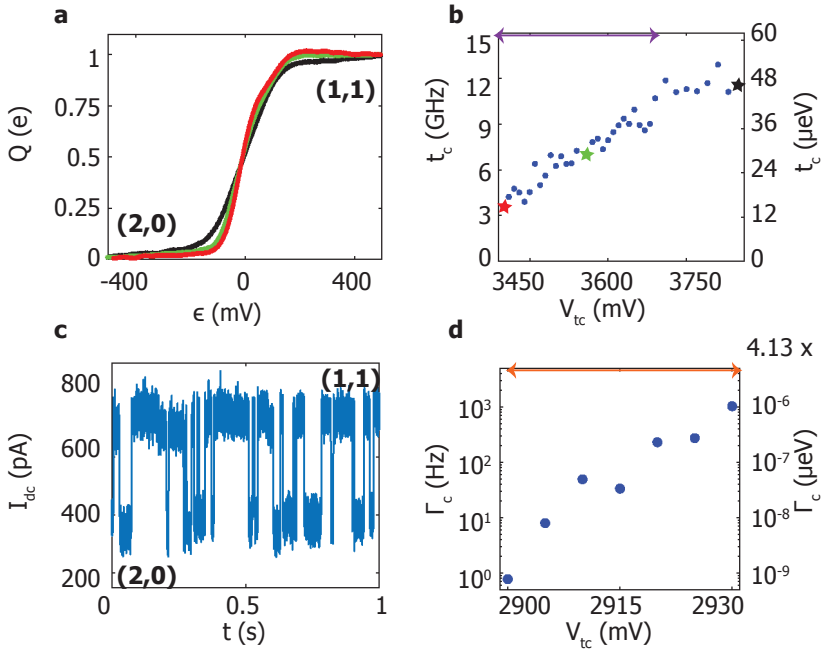

Figure 5.4: **Tunnel coupling control of an isolated double quantum dot.** **a** Polarization lines (excess charge Q as a function of detuning ϵ) across the anticrossing for high t_c (black, V_{tc} = 3.85 V), intermediate t_c (green, V_{tc} = 3.6 V) and relatively low t_c (red, V_{tc} = 3.4 V). **b** Extracted t_c from polarization lines as a function of V_{tc}, where we find tunable t_c up to 13 GHz. **c** RTS for weak coupling V_{tc} = 2.910 V. **d** Extracted Γ_c from RTS measurements as a function of V_{tc}, demonstrating tunable tunnel rates down to below 1Hz.

gate B_T. To compensate for the influence of V_{Bt} on detuning ϵ and on-site potential U, we implement virtual gates using a cross-capacitance matrix [10, 40, 41] and convert V_{P2}, V_{P1} and V_{Bt} to ϵ, U and t_c. Figure 5.3b shows the (2,0)-(1,1) and (1,1)-(0,2) anticrossings as a function of the new set of virtual gates V_ϵ and V_{tc}. For both transitions the inter-dot line vanishes at low V_{tc}, meaning that the coupling has been largely switched off. We observe that for the (1,1)-(0,2) anticrossing, the transition line disappears at $V_{tc} < 3.1$ V, while for the (2,0)-(1,1) anticrossing this happens for $V_{tc} < 2.95$ V. The variation may come from a small asymmetry in the system.

5.6. Tunable tunnel coupling

We tune the double quantum dot to a significantly coupled regime and quantitatively analyse the system by taking charge polarization lines. Figure 5.4a shows charge polarization lines at high, intermediate and relatively low tunnel couplings within this regime. We measure the charge sensor response Q as a function of detuning ϵ and fit the data according to a two level model that includes cross-talk of ϵ to the charge sensor and the influence of the quantum dot charge state on the charge sensor sensitivity [10, 42]. From the thermal broadening of the polarization line at low tunnel coupling, we extract the lever arm of V_ϵ for the detuning axis $\alpha_\epsilon \approx 0.04$ eV/mV, by assuming the electron temperature to be equal to the fridge temperature of 0.44 K.

For relatively low tunnel couplings, we observe in the charge polarization lines deviations from the model for a two-level system [42] (see the red curve in Fig. 5.4a with $\epsilon > 0$). This deviation can also not be explained by a modified model that includes valley states, considering an adiabatic detuning sweep and assuming zero temperature [43]. While these measurements were done adiabatically, the elevated temperature of 0.44 K can cause a non-negligible population of valley or other excited states. These excited states can cause a charge transition at a different detuning energy, thereby giving rise to a deviation. A large tunnel coupling can increase the relaxation rate of these excited states and thus decrease their population. As a consequence, the charge polarization lines are in agreement with the model for a two-level system [42] at larger tunnel couplings.

At tunnel couplings below 3 GHz, the thermal broadening of the polarization line prevents accurate fitting. Instead of the tunnel coupling energy t_c we determine the inter-dot tunnel rate Γ_c, which is proportional to the square of the tunnel coupling [44–46]. We measure the RTS (Fig. 5.4c) at the (2,0)-(1,1) transition and fit the counts C of a histogram of the tunnel times T to $C = Ae^{-\Gamma_c T}$, where A is a normalisation constant. In the measurements we have tuned V_ϵ such that $\Gamma_{c(2,0)-(1,1)} \approx \Gamma_{c(1,1)-(2,0)}$.

Figure 5.4b shows a t_c as a function of V_{tc}, demonstrating tunable tunnel coupling in the strong coupling regime and Fig. 5.4d shows the obtained Γ_c as a function of V_{tc} from 1 kHz down to below 1 Hz. We note that we can further reduce the tunnel rate to even smaller rates simply by further reducing V_{tc}.

A change in barrier height or width results in an exponential change in t_c and in Γ_c. When the tunnel coupling is low, D_2 is located mainly under P_2, and a change in V_{tc} has a significant impact on the barrier. Correspondingly, we observe an exponential dependence of Γ_c versus V_{tc}. When the tunnel coupling is high, D_2 is located mostly under B_t and the impact of V_{tc} on the barrier is vanishing. As a result we observe a seemingly linear dependence of t_c versus V_{tc} from 3 up to 11 GHz that saturates around 13 GHz for $V_{tc} > 3675$ mV.

5.7. Conclusions

We have demonstrated control over the tunnel coupling of single electrons residing in a double quantum dot in SiMOS. The inter-dot coupling of the (2,0)-(1,1)

charge transition can be controlled by a barrier gate which changes the quantum dot location. We have demonstrated control over the tunnel coupling in the strong coupling regime from 3 to 13 GHz, as well as control over the tunnel rate in the weak coupling regime from 1 kHz to below 1 Hz. Achieving this degree of control in an isolated system constitutes a crucial step toward independent control over detuning and tunnel coupling for operation at the charge symmetry point [6, 7], and reaching the control required for large-scale quantum computation with quantum dots [2, 20–25]. While SiMOS systems are often said to be severely limited by disorder, the excellent control shown here provides great prospects to operate larger arrays fabricated using conventional semiconductor technology.

5.8. Outlook

Achieving a high and tunable tunnel coupling between single electrons serves as a confirmation of correct quantum dot definition and a high degree of control. Nevertheless, spin qubit operations are not limited to single spins (see Chapter 2) and higher electron occupations might be necessary to achieve a higher tunnel coupling. Chapter 7 [47] demonstrates qubit operations with 5 electrons in one of the quantum dots, while the other contains a single electron. Experiments with 13 electrons in one quantum dot [48] and 3 electrons in each [38] have also been demonstrated.

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6

Spin lifetime and charge noise in hot silicon spin qubits

I discovered that if one looks a little closer at this beautiful world, there are always red ants underneath.

David Lynch

In this chapter we investigate the magnetic field and temperature dependence of the single-electron spin lifetime in silicon quantum dots and find a lifetime of 2.8 ms at a temperature of 1.1 K. We develop a model based on spin-valley mixing and find that Johnson noise and two-phonon processes limit relaxation at low and high temperature respectively. We also investigate the effect of temperature on charge noise and find a linear dependence up to 4 K. These results contribute to the understanding of relaxation in silicon quantum dots and are promising for qubit operation at elevated temperatures.

Parts of this chapter have been published in **Physical Review Letters 121**, 076801 (2018) [1].

6.1. Introduction

Electron spins in semiconductor quantum dots [2] are considered to be one of the most promising platforms for large-scale quantum computation. Silicon can provide key assets for quantum information processing, including long coherence times [3, 4], high-fidelity single-qubit rotations [3, 4] and two-qubit gates [5–7], which have already enabled the demonstration of quantum algorithms [7]. Quantum dots based on silicon metal-oxide semiconductor (SiMOS) technology provide additional prospects for scalability due to their compatibility with conventional manufacturing technology [8, 9], which opens the possibility to co-integrate classical electronics and qubits on the same wafer to avoid an interconnect bottleneck [10, 11]. However, control electronics will introduce a power dissipation that seems incompatible with the available thermal budget at temperatures below 100 mK, where qubits currently operate. Understanding and improving the robustness of qubits against thermal noise is therefore crucial, while operating qubits beyond 1 K could entirely resolve this challenge.

Spin relaxation and charge noise are two essential metrics for quantum dot qubits. While the spin lifetime T_1 can be of the order of seconds in silicon quantum dots [12–14], exceeding by orders of magnitude the dephasing time T_2^* [3], it is presently unclear how T_1 will be affected by temperature and whether it will become the shortest timescale for quantum operations at elevated temperatures. Spin qubits are also sensitive to charge noise, and electrical fluctuations can reduce qubit readout and control fidelities. The temperature dependence of these two parameters is therefore vital in evaluating the prospects for hot spin qubits.

Here we investigate in detail the temperature dependence of spin relaxation and charge noise of a SiMOS quantum dot. We construct a model based on direct and two-phonon transitions including all spin and valley states of the lowest orbital. The model provides good agreement with the experiments and we conclude that while at low temperatures T_1 is limited by Johnson noise, probably originating from the two-dimensional electron gas (2DEG) channels present in the device, two-phonon processes determine the relaxation rate above 200 mK. Based on our results we predict how the spin lifetime can be improved by decreasing the magnetic field and increasing the valley-splitting energy. Furthermore, we investigate the charge noise and measure a rather weak temperature dependence.

6.2. Device operation

Figure 6.1a shows a scanning electron microscope (SEM) image of a quantum dot device, realized in isotopically enriched silicon (^{28}Si), identical in design to the one measured. Figure 6.1b presents the charge stability diagram of the device, showing charge transitions originating from three quantum dots, and we deplete one quantum dot to the last electron. From the temperature dependence of the transition width (see section 6.9) we extract a lever arm $\alpha_{P1} = 0.12$ eV/V. We tune the tunnel rate between the quantum dot and the reservoir by controlling the gate P2 (see Fig. 6.1c), which moves the position of the quantum dot thereby changing the distance to the reservoir. During the experiment, since the DC signal of the sensing

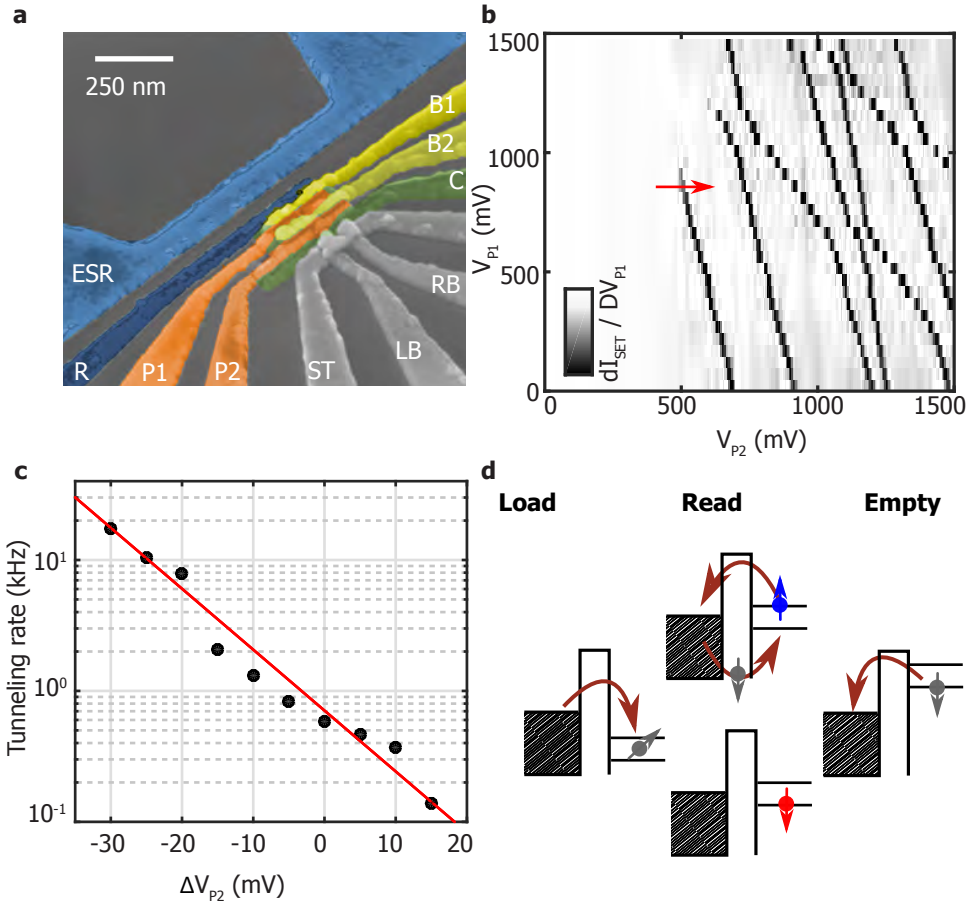

Figure 6.1: **Operation scheme of quantum dot device. a** Scanning electron microscope image of a device identical to the one measured. R is the reservoir gate, P1, P2, B1 and B2 are the plunger gates, and C confines the electrons in the dots. LB and RB are the left and right barrier of the quantum dot used for sensing, and ST is used both as top gate and reservoir. The ESR line can be used for spin manipulation. **b** Charge stability diagram of the device measured via a double lock-in technique [15]. The transition lines, due to the different slope, can be attributed to three coupled quantum dots. The red arrow shows the (0→1) charge transition relevant for the experiment. **c** Tunnelling rate between the dot and the reservoir as a function of V_{P2}. ΔV_{P2}=0 corresponds to the value set during the experiment. The red line is an exponential fit. **d** Pulsing sequence used to perform single-shot readout of the electron spin [16] in the case $E_Z < E_{vs}$. Above the valley splitting there is also an intermediate level between the ground and excited spin state, corresponding to the spin-down state of the excited valley.

dot is filtered with a 2 kHz low pass filter, the dot-reservoir tunnel rate is set to approximately 700 Hz.

As shown in Fig. 6.1 d, we measure the spin lifetime by applying a three-level voltage pulse to the gate P1, while monitoring the DC current of the sensing dot. First, we inject an electron into the quantum dot, we read out the spin state, and we finally empty the quantum dot [16]. An additional level is added to the pulse

after the empty phase in order to cancel out any DC offset. We measure the spin-up fraction as a function of load time and extract T_1 by fitting the data with an exponential decay function.

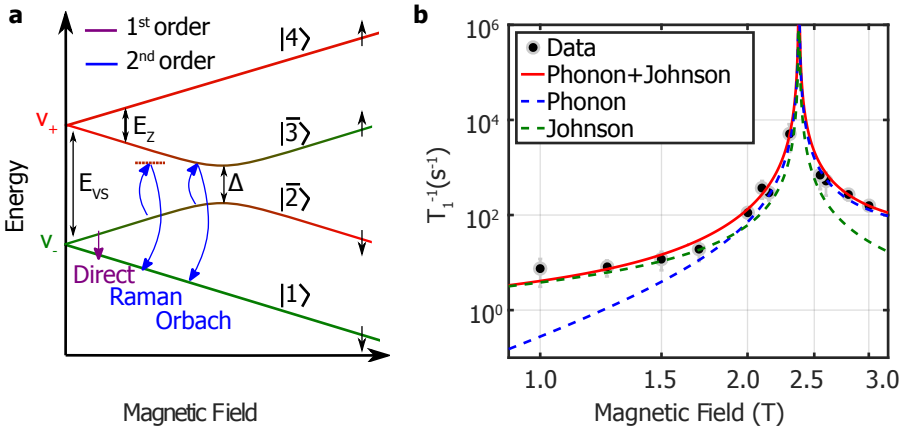

Figure 6.2: **Valley induced relaxation.** **a** Energy levels in a silicon quantum dot, showing both valley and spin degrees of freedom. As an example, the transition $\Gamma_{\bar{2}\bar{1}}$ is sketched in first-order and in second-order via virtual and resonant transitions. **b** Relaxation rate as a function of magnetic field. The fittings include contributions from Johnson and phonon mediated relaxation obtained through the model explained in the main text. From the fittings of the magnetic field and temperature dependence we extract $E_{vs} = 275\ \mu$eV, $\Gamma_0^J(E_{vs}/\hbar) = 2 \cdot 10^{-12}$ s, $\Gamma_0^{ph}(E_{vs}/\hbar) = 6 \cdot 10^{-12}$ s and $\Delta = 0.4$ neV.

6.3. Magnetic field dependence of T_1

The measured T_1 as a function of magnetic field (applied in the [010] direction) is plotted in Fig. 6.2b and the temperature dependence for three different magnetic fields is shown in Fig. 6.3a, b and c. Thermal broadening of the reservoir limits the experimentally accessible regime. At base temperature (fridge temperature < 10 mK, electron temperature 108 mK (see section 6.9) we measure a maximum T_1 of 145 ms at $B_0 = 1$ T. We find that even when increasing the temperature to 1.1 K, T_1 is 2.8 ms. This is more than an order of magnitude larger than the longest T_2^* reported in silicon quantum dots [3].

In order to understand the magnetic field and temperature dependence of the relaxation rate, we need to consider the mixing between spin and valley. In silicon the four lowest spin-valley states are [17]: $|1\rangle = |v_-, \downarrow\rangle$, $|2\rangle = |v_-, \uparrow\rangle$, $|3\rangle = |v_+, \downarrow\rangle$, $|4\rangle = |v_+, \uparrow\rangle$ (see Fig. 6.2a). In presence of interface disorder, spin-orbit interaction can couple states with different valleys and spins, introducing a channel for spin

relaxation [14]. This leads to the eigenstates $|1\rangle, |\bar{2}\rangle, |\bar{3}\rangle, |4\rangle$, where:

$$|\bar{2}\rangle = \left(\frac{1-a}{2}\right)^{1/2} |2\rangle - \left(\frac{1+a}{2}\right)^{1/2} |3\rangle \tag{6.1}$$

$$|\bar{3}\rangle = \left(\frac{1+a}{2}\right)^{1/2} |2\rangle + \left(\frac{1-a}{2}\right)^{1/2} |3\rangle . \tag{6.2}$$

Here we have $a = -(E_{vs} - \hbar\omega_z)/\sqrt{(E_{vs} - \hbar\omega_z)^2 + \Delta^2}$, where Δ is the splitting at the anticrossing point of the states $|2\rangle$ and $|3\rangle$, E_{vs} is the valley splitting and $\hbar\omega_z$ the Zeeman energy. In the presence of electric fields, the electrons in the excited states $|\bar{2}\rangle$ and $|\bar{3}\rangle$ can relax to the ground state $|1\rangle$, because they are in an admixture of spin and valley states. We define a relaxation rate Γ_{sv}, corresponding to $\Gamma_{\bar{2}1}$ and $\Gamma_{\bar{3}1}$ before and after the anticrossing, respectively. The resulting expression is [18]:

$$\Gamma_{sv} = \Gamma_{v_+v_-}(\omega_z) F_{sv}(\omega_z) \tag{6.3}$$

where $\Gamma_{v_+v_-}$ is the pure valley relaxation rate and $F_{sv}(\omega_z) = (1 - |a(\omega_z)|)$. When $E_{vs} = E_z$, the function F_{sv} peaks and the spin relaxation equals the fast pure valley relaxation [14]. From the location of this relaxation hot spot we determine a valley splitting E_{vs} of 275 μeV, comparable with values reported in other works [3].

Possible sources of electrical noise include $1/f$ charge noise, Johnson noise, and phonon noise. We measure small values for charge noise (see Fig. 6.4) and thus neglect their contribution, further justified by the high frequencies of 20-100 GHz, associated with the Zeeman energies studied here ($1\ \mathrm{T} < B_0 < 3\ \mathrm{T}$). We also neglect the Johnson noise coming from the circuits outside the dilution refrigerator since all room temperature electronics are well filtered. The most relevant of these noise sources is the arbitrary waveform generator used to apply voltage pulses. However, the corresponding lines are attenuated by 12 dB and have an intrinsic cut-off frequency of 1 GHz, making the noise in the 20-100 GHz range negligible. Another possible source of Johnson noise is the resistive 2DEG, which generates electric field fluctuations that have a capacitive coupling to the quantum dot. In the present device, the main contribution is likely due to the 2DEG underneath the reservoir gate, which is in close proximity to the quantum dot.

The remaining contributions are Johnson noise and phonons. The pure valley relaxation for these two cases is given by [14, 18]:

$$\Gamma^{J}_{v_+v_-}(\omega) = \Gamma^{J}_{0} \cdot \left(\frac{\omega}{\omega_{vs}}\right)[1 + 2n_b(\hbar\omega, k_{\mathrm{B}}T)] \tag{6.4}$$

$$\Gamma^{ph}_{v_+v_-}(\omega) = \Gamma^{ph}_{0} \cdot \left(\frac{\omega}{\omega_{vs}}\right)^5 [1 + 2n_b(\hbar\omega, k_{\mathrm{B}}T)], \tag{6.5}$$

where $\hbar\omega$ is the energy difference, $\omega_{vs} = E_{vs}/\hbar$ is a normalization constant and n_b is the Bose-Einstein distribution. The two contributions can be distinguished by the different magnetic field dependence that follows from $\omega_z F_{sv}(\omega_z)$ in the case of Johnson noise and from $\omega_z^5 F_{sv}(\omega_z)$ for phonons. As shown in Fig. 6.2b the magnetic

field dependence of T_1 at base electron temperature can be explained in terms of Johnson mediated relaxation dominant at low fields, and a phonon contribution, mainly relevant for $\hbar\omega_z > E_{vs}$.

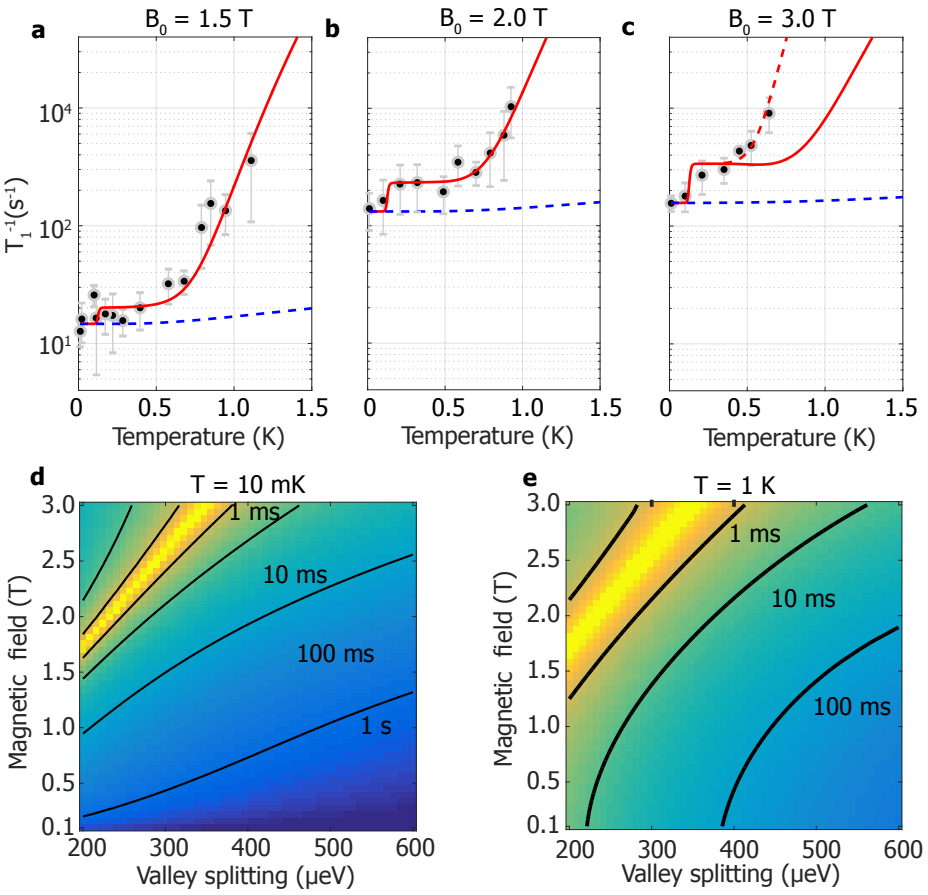

Figure 6.3: **Magnetic field and valley splitting dependence of the relaxation rate. a-c** Temperature dependence of the relaxation rate at $B_0 = 1.5$ T **a**, 2 T **b** and 3 T **c**. The red line is a fit taking into account Johnson and phonon noise in first and second-order. The red dashed line includes possible contributions coming from the coupling with the excited orbital states. First-order processes are shown in the dashed blue line. **d,e** Relaxation rate as a function of magnetic field and valley splitting for $T = 10$ mK **d** and for $T = 1$ K **e** as extracted from the model discussed in the main text.

6.4. Temperature dependence of T_1

We now turn to the temperature dependence, shown in Fig. 6.3a, b and c. As shown in Eq. (6.4) and (6.5), the temperature dependence is the same to first-order for phonon and Johnson noise and given by $1+2n_b(\hbar\omega_z, k_\mathrm{B}T)$. If $\hbar\omega_z \gg k_\mathrm{B}T$ spontaneous phonon emission dominates and the relaxation rate is temperature

independent, while for $\hbar\omega_z \ll k_B T$ it increases linearly with temperature. The relaxation rates caused by first-order processes are shown by the blue lines in Fig. 6.3a, b and c, which fit the low temperature region of the plots. However, the same processes cannot justify the rapid increase of T_1 measured at higher temperatures. In order to explain the full temperature dependence we also need to take into account two-phonon processes.

As depicted in Fig. 6.2a, these transitions happen in a two-step process via intermediate states. These intermediate transitions can be energy-conserving and energy non-conserving (virtual) processes, since energy must be conserved only between the initial and the final state. We obtain a two-phonon process by expanding the spin-phonon interaction in second-order perturbation theory [19]:

$$\Gamma_{if}^{(2)} = \frac{2\pi}{\hbar}\left|\sum_k \frac{V_{fk}V_{ki}}{E_i - E_k + \frac{1}{2}i\hbar\Gamma_k}\right|^2 \delta(E_i - E_f), \tag{6.6}$$

where V_{fk}, V_{ki} are the matrix elements between the states and $1/\Gamma_k$ is the lifetime of the intermediate state, which depends on all first-order processes between k and the other states. The square of the matrix elements is proportional to the valley relaxation rate $\Gamma_{v_+v_-}$. Relaxation through Johnson noise can also be expanded in second-order perturbation theory, however, the temperature dependence is much weaker (see section 6.8) and its contribution will therefore be neglected.

Since the thermal energy is comparable to the level splitting in the temperature window 0.5-1 K, absorption processes cannot be neglected. In order to understand the relaxation dynamics we have developed a model that includes all possible transitions between the four spin-valley states in first and second-order. For completeness, we have also included in the model the weak coupling between the states $|1\rangle$ and $|4\rangle$. We evaluate all the transition rates and we use them to solve a 4x4 system of coupled differential rate equations given by:

$$\frac{dN_i}{dt} = -N_i \sum_{j\neq i} \Gamma_{ij} + \sum_{j\neq i} \Gamma_{ji} N_j \quad \text{for} \quad i,j = 1, \bar{2}, \bar{3}, 4, \tag{6.7}$$

N_i being the population of the state i. The red lines in Fig. 6.3a, b and c, show the relaxation rates as obtained from Eq. 6.3, 6.6 and 6.7 (see also section 6.8). The good agreement between model and experiment provides an indication that, even at high temperatures, relaxation is dominated by spin-valley physics. The rates relevant to the relaxation process are found to be the spin-flip transitions involving the three lowest states: $\Gamma_{\bar{2},1}$, $\Gamma_{\bar{2},\bar{3}}$ and $\Gamma_{\bar{3},1}$, $\Gamma_{\bar{3},\bar{2}}$ at E_z below and above E_{vs} respectively. The relaxation rate above 200 mK consists of a flat region followed by a rising part. We attribute this behaviour to the second-order process described by Eq. 6.6. We consider separately the contributions of the resonant ($|E_i - E_k| \ll \hbar\Gamma_k$) and off-resonant transitions ($|E_i - E_k| \gg \hbar\Gamma_k$). In the first case, known as Orbach process [20], the second-order relaxation is proportional to $\left|V_{fk}V_{ki}\right|^2/\Gamma_k$ (see section 6.8). At sufficiently low temperatures, the spin lifetime depends exponentially on

the temperature since the numerator is proportional to n_b and the denominator is temperature independent. We therefore theoretically predict the brief steep rise around 150-200 mK. At high temperatures Γ_k also becomes proportional to n_b and the temperature dependence vanishes. This explains the main flat region that we observe in Fig. 6.3a, b and c. For off-resonant transitions, known as Raman process, the relaxation rate scales polynomially with the temperature. As discussed in section 6.8, in the case of phonon-mediated transitions, a T^9 temperature dependence is obtained. The Raman process dominates over the Orbach process above 500 mK (see Fig. 6.3a, b and c).

As we can see from Fig. 6.3c, the increase in the relaxation rate at $B_0 = 3$ T does not match the model predictions above 500 mK, suggesting contributions to the relaxation from a different source rather than the valley mixing. We rule out second-order contributions from Johnson noise because of the much weaker temperature dependence. Possible contributions might come from a second-order process involving the excited orbital states, which is expected to give a T^{11} temperature dependence as discussed in section 6.8. Coupling to orbital states can potentially give a magnetic field dependence that would make it not observable at lower fields. Coupling to orbital states mediated by direct processes give rise to a B_0^2 field dependence; this phenomenon is known as Van Vleck cancellation, a consequence of Kramer's theorem [21]. For two-phonon processes, Van Vleck cancellation together with the spin-valley mixing can potentially give an even stronger field dependence.

The spin lifetime can be increased by reducing the spin-valley coupling. As shown in Eq. 6.1 and 6.2, it can be strongly increased by reducing the applied magnetic field or by increasing the valley splitting energy. In SiMOS the valley splitting can be electrically controlled and increased to $E_{vs} \approx 1$ meV [3, 22]. Figure 6.3 d and e show the magnetic field and the valley splitting energy dependence of the relaxation rate for $T = 10$ mK and $T = 1$ K, using the parameters extracted from our numerical fittings of the experimental data. These results predict a spin lifetime at 1 K of approximately 500 ms, when $B_0 = 0.1$ T and $E_{vs} = 575$ μeV. The relaxation at low magnetic fields is predicted to be dominated by second-order processes even at low temperature, due to the stronger field dependence of the first-order processes.

6.5. Temperature dependence of charge noise

We now turn to charge noise measurements. In a minimal model, charge noise can be attributed to defects that can trap or release charges, giving rise to electrical noise with a characteristic 1/f spectrum [23]. We measure the charge noise in our device as current fluctuations of the sensing dot tuned to a regime with a high slope dI/dV, to maximize the sensitivity. The time trace of the current is converted to voltage noise by dividing by the slope; then the spectrum is obtained through a Fourier transform. The same process is repeated in Coulomb blockade in order to subtract the baseline noise coming from the electronics [24]. Finally, the voltage fluctuations are converted to energy fluctuations by using the lever arm $\alpha_{ST} = 0.18$ eV/V of the sensing dot. The spectra shown in Fig. 6.4a scale as 1/f

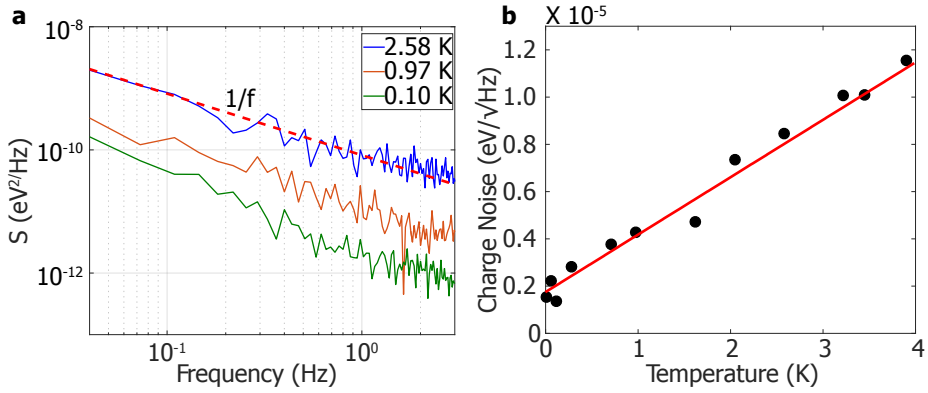

Figure 6.4: **Charge noise measurements.** **a** Spectra obtained for three different temperatures. At higher frequencies the 1/f signal is masked by white noise. **b** Charge noise at a frequency of 1 Hz as a function of temperature fitted with a linear function.

for the probed frequency regime. Fig. 6.4b shows the temperature dependence of the charge noise at a fixed frequency of 1 Hz. We observe a linear increase of the charge noise over more than one decade of temperature (0.1-4 K), changing from approximately 2 $\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ to 12 $\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$. This is indicating a different relation than predicted by a simple model, which assumes an equal distribution of thermally activated fluctuators with relaxation rates distributed according to a Lorentzian. This model would give rise to a square root temperature dependence of the charge noise amplitude [23]. The offset measured at low temperature can be attributed to electrical noise that couples to the sensing dot via the gates. This remarkably weak dependence suggests that qubit operation will only be moderately affected when increasing temperature.

6.6. Conclusion

In summary, we have investigated the magnetic field and temperature dependence of the spin lifetime and measured $T_1 = 2.8$ ms at 1.1 K and $T_1 = 145$ ms at base temperature. Relaxation occurs through electric field fluctuations that cause spin transitions mediated by spin-valley coupling. At temperatures below 200 mK the dominant noise source is Johnson noise, while second-order phonon processes dominate at higher temperatures. We have also shown how the spin lifetime can be further improved by operating in low magnetic fields and tuning to high valley splitting energies. In particular SiMOS devices have the advantage of a large and tunable valley splitting, whereas in Si/SiGe it is typically no larger than 100 μeV [25]. Future work aimed at improving lifetimes could focus on schemes that do not explicitly require a large magnetic field, such as readout via Pauli spin blockade. In addition, we have measured the temperature dependence of the charge noise and find consistency with a linear trend from 100 mK to 4 K.

Leading solid-state approaches for large-scale quantum computation focus on

decreasing the operation temperature down to the milliKelvin regime. Instead, the long spin lifetimes at elevated temperatures and the weak charge noise reported here indicate that such low temperatures are not a fundamental requirement for spins in SiMOS quantum dots, providing an avenue for the demonstration of spin qubits with operation temperatures above one Kelvin.

6.7. Outlook

This chapter shows that the spin lifetime is not a limiting factor for hot qubit operation, and how it can be extended even further. Furthermore, experiments using a vector magnet have shown that the hotspot relaxation is highly anisotropic and can be reduced by more than two orders of magnitude [26]. While the results from this chapter provide insight on the temperature dependence of noise and relaxation sources, several more aspects are critical for qubit operation at higher temperatures. Chapter 7 extends on this chapter by demonstrating one- and two-qubit operation at a temperature of 1 Kelvin, as well as looking into the temperature dependence of T_2. Work done in parallel at UNSW Sydney compares the performance of qubits over a range of temperatures [27].

6.8. Second-order processes and rate equations

The preceding sections drew some conclusions about the temperature dependence of the spin relaxation process. This section serves to provide a more rigorous justification. As an example, Fig. 6.5a and b show the relevant contributions to the relaxation rate for $B_0 = 2$ T. The low temperature regime is dominated by a first-order process between the states $|\bar{2}\rangle$ and $|1\rangle$. According to Eq. 6.4 and 6.5, it is composed of a flat initial part followed by a linear increase. At higher temperatures, the second-order process mediated by phonons between the states $|\bar{2}\rangle$ and $|\bar{3}\rangle$ becomes dominant. We can better understand its functional form by expanding the terms in Eq. 6.6:

$$\Gamma_{\bar{2}\bar{3}}^{(2)} \propto \int_0^{\omega_d}\int_0^{\omega_d}\left|\sum_{k\neq 2,3}\frac{c_{2k}\,c_{k3}}{\Delta E_{\bar{2}k}-\hbar\omega'+\frac{1}{2}i\hbar\Gamma_k}\right|^2 \omega'^5\omega''^5[1+n_b(\hbar\omega')]n_b(\hbar\omega'') \\ \delta(\Delta E_{\bar{3}\bar{2}}+\hbar\omega'-\hbar\omega'')d\omega' d\omega'', \tag{6.8}$$

where ω_d is the Debye frequency and the coefficients c_{ij} come from the overlap between the states i,j due to mixing between spin and valley. In silicon, the electron-phonon interaction is mediated by deformation potential phonons. Therefore, the matrix elements have an additional factor ω^2 with respect to the standard interaction with piezoelectric phonons, because of the $\sqrt{q}$ dependence of the strain caused by deformation potential phonons, where q is the wavenumber.

As discussed in the preceding sections, $\frac{1}{2}\hbar\Gamma_k$ represents the energy width of the k state, determined by its lifetime. Since the ground state of the system $|1\rangle$ has, at least at low temperature, a long lifetime compared to the state $|4\rangle$, $\Gamma_4 \gg \Gamma_1$,

we can neglect the transitions through the state $|4\rangle$ in the sum of Eq. 6.8. In the following, we will consider separately the contributions to the integral coming from off-resonant ($\hbar\omega' \neq \Delta E_{\bar{2}1}$) and resonant ($\hbar\omega' \approx \Delta E_{\bar{2}1}$) phonons.

In the off-resonant case and at sufficiently high temperatures, phonons with frequencies $\hbar\omega \gg \Delta E_{\bar{2}1}, \Delta E_{\bar{3}\bar{2}}$ are well populated and Eq. 6.8 can be rewritten as:

$$\Gamma_{\bar{2}\bar{3}}^{(2)} = C_R T^9 \int_0^{\hbar\omega_d/k_B T} \frac{e^x}{(e^x-1)^2} dx \tag{6.9}$$

and the relaxation rate scales to a good approximation as T^9. In the intermediate regime $\Delta E_{\bar{2}1} \gg \hbar\omega \gg \Delta E_{\bar{3}\bar{2}}$, the term $\hbar\omega'$ in the denominator of Eq. 6.8 can be neglected and the relaxation rate scales as T^{11}. In our experimental case, the energy differences between the levels are comparable with each other and thus this last regime is not visible in the experimental data. Instead, if we consider coupling with orbital states, these conditions apply and a T^{11} dependence is expected. The power laws we found are strictly related to the power of the ω terms in Eq. 6.8, which depends on the particular nature of the electron-phonon interaction. For example, in GaAs, where piezoelectric phonons dominates over deformation potential phonons, the power is reduced to three instead of five, which leads to a T^5 and T^7 temperature dependence. In case of Johnson mediated relaxation an even weaker temperature dependence is obtained.

In the resonant case, we have $\hbar\omega' \approx \Delta E_{\bar{2}1}$ and Eq. 6.8 can be approximated as:

$$\Gamma_{\bar{2}\bar{3}}^{(2)} = C_O \frac{[1+n_b(\Delta E_{\bar{2}1})]n_b(\Delta E_{\bar{2}1}+\Delta E_{\bar{2}\bar{3}})}{\Gamma_1}, \tag{6.10}$$

where the lifetime of the k state is in general evaluated as the inverse of the sum of all first-order processes between k and the other states and it is ultimately limited by the time scale of the experiment. At sufficiently low temperatures, Γ_k is temperature independent and the relaxation rate depends exponentially on the temperature according to $\Gamma_{\bar{2}\bar{3}}^{(2)} \propto n_b(\Delta E_{\bar{2}1}+\Delta E_{\bar{2}\bar{3}})$. At higher temperatures, Γ_k becomes also proportional to $n_b(\Delta E_{\bar{2}1}+\Delta E_{\bar{2}\bar{3}})$ and the relaxation rate is given approximately by $1+n_b(\Delta E_{\bar{2}1})$, which is temperature independent for $k_B T \ll \Delta E_{\bar{2}1}$ and linear dependent for $k_B T \gg \Delta E_{\bar{2}1}$. In our experimental case, this linear dependence is masked by the the Raman process. The resonant and off-resonant transitions can thereby explain all the different regimes that we see in Fig. 6.5a.

The rates in first and second-order are used to solve the 4x4 system of coupled differential rate equations:

$$\begin{bmatrix} \dot{N}_1 \\ \dot{N}_2 \\ \dot{N}_3 \\ \dot{N}_4 \end{bmatrix} = \begin{bmatrix} -\sum_{j\neq 1}\Gamma_{1j} & \Gamma_{21} & \Gamma_{31} & \Gamma_{41} \\ \Gamma_{12} & -\sum_{j\neq 2}\Gamma_{2j} & \Gamma_{32} & \Gamma_{42} \\ \Gamma_{13} & \Gamma_{23} & -\sum_{j\neq 3}\Gamma_{3j} & \Gamma_{43} \\ \Gamma_{14} & \Gamma_{24} & \Gamma_{34} & -\sum_{j\neq 4}\Gamma_{4j} \end{bmatrix} \cdot \begin{bmatrix} N_1 \\ N_2 \\ N_3 \\ N_4 \end{bmatrix}. \tag{6.11}$$

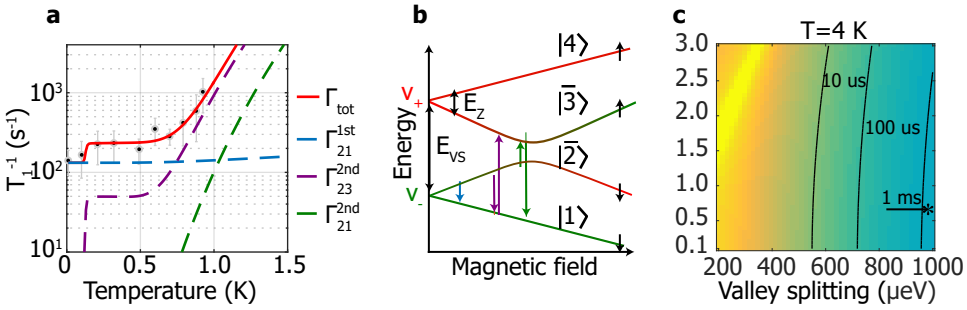

Figure 6.5: **High temperature operation. a** Relaxation rate as a function of temperature for B_0=2 T. The dashed coloured lines show the relevant transition rates, including the first-order process between the states $|\bar{2}\rangle$ and $|1\rangle$ and second-order transitions via the states $|1\rangle$ and $|\bar{3}\rangle$. **b** The relevant transitions shown in the plot in **a** are sketched in an energy diagram. **c** Magnetic field and valley splitting dependence of the relaxation rate at a temperature of 4 K. Lifetimes larger than 1 ms are accessible with a valley splitting close to 1 meV.

N_i being the population of the state i. For each temperature we extract the four eigenvalues of the matrix. Among the four, one equals zero and corresponds to the stationary population of the levels after the relaxation process is over. Two are much greater than the inverse time scale of the experiment and are therefore discarded, since they correspond to exponential decays not observable in the experiment. Finally, the remaining one represents the time constant that characterizes the single exponential decay of the spin-up fraction as a function of load time. This rate is shown in Fig. 6.5a, b and c.

As shown in Fig. 6.3 the spin lifetime can be further improved by working in a low magnetic field and high valley splitting regime. Fig. 6.5c show this dependence at a temperature of 4 K, where second-order phonon processes dominate the relaxation process. Even at this relatively high temperature, we extract lifetimes larger than 1 ms for a valley splitting close to 1 meV, which is a very promising result for future scalability of these systems.

We did not discuss relaxation due to the residual ^{29}Si nuclei. However, the presence of nuclei mainly affects the dephasing of the electron spin rather than relaxation, due to the large Zeeman energy mismatch. The modulation of hyperfine coupling by phonons is also suppressed in natural silicon due to the low concentration of ^{29}Si nuclei [28]. The effect can be expected to be even smaller in our case, where the substrate is made of ^{28}Si.

6.9. Electron temperature and lever arm

Both the base electron temperature and the lever arm of the quantum dot have been extracted by a unique measurement, where the width of the charge transition (0→1) shown by the red arrow in Fig. 6.1b is measured as a function of the nominal fridge temperature [29]. The charge stability diagram shown in Fig. 6.1b, is measured via a double-lockin technique, where the transconductance dI_s/dP_1 of the sensing dot is measured by applying an AC excitation V_{AC} to the gate P1. During the map, the

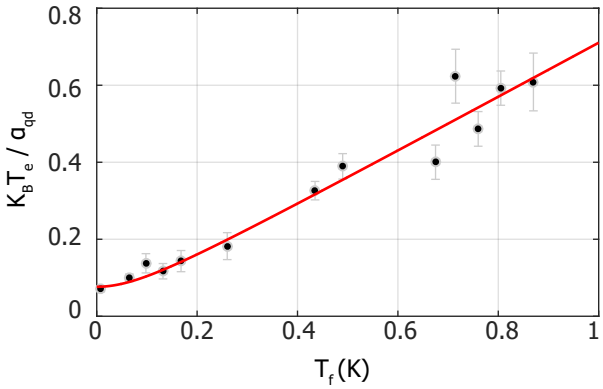

Figure 6.6: **Lever arm measurement.** Width of the (0→1) charge-state transition as a function of the fridge temperature. The red line is a fit according to Eq. 6.12 and 6.13. At sufficiently high temperatures, T_e equals T_f and the transition width increases linearly with a slope proportional to the inverse of the lever arm. At low temperature T_f becomes smaller than T_0 and the transition width becomes independent of T_f.

current I_s of the sensing dot is kept at the most sensitive point by using a digitally-controlled feedback. The width of the transition is determined by V_{AC} for large AC excitations and by the thermal broadening due to the finite electron temperature T_e when $V_{AC} \ll k_B T_e$. In these conditions the transconductance dI_s/dP_1 is proportional to the derivative of the Fermi-Dirac distribution:

$$\frac{dI_s}{dP_1} = a \cosh^{-2}\left(\frac{\alpha_{P1}(P_1 - b)}{2k_B T_e}\right) + c, \tag{6.12}$$

where a, b and c are fitting parameters and α_{P1} is the lever arm of the quantum dot. The electron temperature T_e depends on the nominal fridge temperature T_f and the base electron temperature T_0 according to:

$$T_e = \sqrt{T_0^2 + T_f^2}. \tag{6.13}$$

We fix the gate P2 such that the tunnel rate between dot and reservoir is maximized and therefore the signal to noise ratio in the charge stability diagram is also maximized. We sweep gate P1 in the direction of the first charge transition. During the sweep we apply an AC excitation to gate P1 of 15 μV at 133 Hz.

Fig. 6.6 shows the width of the transition as a function of T_f. The width is for all points much higher than the excitation applied to gate P1 meaning that we are in the conditions of a thermally limited transition. From the fit we extract a lever arm of $\alpha_{P1} = 0.122 \pm 0.005$ eV/V and a base electron temperature of $T_0 = 108 \pm 13$ mK.

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7

Universal quantum logic in hot silicon spin qubits

Let us strive for the impossible. The great achievements throughout history have been the conquest of what seemed the impossible.

Charlie Chaplin

The previous chapters have shown that quantum dots can be formed and operated at elevated temperatures. We investigated the temperature dependence of two important parameters: spin lifetime and charge noise. Sufficiently long lifetimes and moderate temperature dependence of charge noise were measured, encouraging for the operation of hot qubits. However, a high-temperature two-qubit logic gate still needs to be demonstrated. In this chapter we will show that silicon quantum dots can have sufficient thermal robustness to enable the execution of a universal gate set above one Kelvin. We obtain single-qubit control via electron-spin-resonance (ESR) and readout using Pauli spin blockade. We show individual coherent control of two qubits and measure single-qubit fidelities up to 99.3 %. We demonstrate tunability of the exchange interaction between the two spins from 0.5 up to 18 MHz and use this to execute coherent two-qubit controlled rotations (CROT). The demonstration of 'hot' and universal quantum logic in a semiconductor platform paves the way for quantum integrated circuits hosting the quantum hardware and their control circuitry all on the same chip, providing a scalable approach towards practical quantum information.

Parts of this chapter have been published in **Nature 580**, 355-359 (2020) [1].

7.1. Introduction

Spin qubits based on quantum dots are among the most promising candidates for large-scale quantum computation [2–4]. Quantum coherence can be maintained in these systems for extremely long times [5] by using isotopically enriched silicon (^{28}Si) as the host material [6]. This has enabled the demonstration of single-qubit control with fidelities exceeding 99.9% [7, 8] and the execution of two-qubit logic [9–12]. The potential to build larger systems with quantum dots manifests in the ability to deterministically engineer and optimize qubit locations and interactions using a technology that greatly resembles today's complementary metal-oxide-semiconductor (CMOS) manufacturing. Nonetheless, quantum error correction schemes predict that millions to billions of qubits will be needed for practical quantum information [13]. Considering that today's devices make use of more than one terminal per qubit [14], wiring up such large systems remains a formidable task. In order to avoid an interconnect bottleneck, quantum integrated circuits hosting the qubits and their electronic control on the same chip have been proposed [4, 15, 16]. While these architectures provide an elegant way to increase the qubit count to large numbers by leveraging the success of classical integrated circuits, a key question is whether the qubits will be robust against the thermal noise imposed by the power dissipation of the electronics. Demonstrating a universal gate set at elevated temperatures would therefore be a milestone in the effort towards scalable quantum systems. First steps towards this direction have already been taken in an experiment by Yang et al. [17] by demonstrating a device that can be operated as a two-qubit system at a temperature of 40 mK and continues to have good single-qubit properties when the temperature is increased above one Kelvin.

Here, we solve this challenge and combine initialization, readout, single-qubit rotations and two-qubit gates, to demonstrate full two-qubit logic in a quantum circuit operating at 1.1 Kelvin. We furthermore examine the temperature dependence of the quantum coherence which we find, unlike the relaxation process [18], to be hardly affected in a temperature range T = 0.45 K - 1.25 K.

7.2. Device operation

Figure 7.1a shows the silicon quantum dot device. The qubits are realized in an isotopically purified ^{28}Si epi-layer with a ^{29}Si residual concentration of 800 ppm. The fabrication of the quantum dot device is based on an overlapping gate-scheme to allow for tightly confined quantum dots [21, 22]. Electrons can be loaded either from the reservoir or from the single-electron-transistor (SET) [19], which is also used for charge sensing. To allow for coherent control over the electron spins, AC currents are applied through the on-chip aluminum microwave antenna.

Figure 7.1b shows a charge stability diagram of the double quantum dot, where the qubits Q1 and Q2 and their coupling are defined by using the gates P1, B12, and P2. Since we can freely choose the occupancy of the two quantum dots we tune to the regime where we obtain optimal exchange coupling, which we find with one and five electrons for Q1 and Q2 respectively. We then operate the system

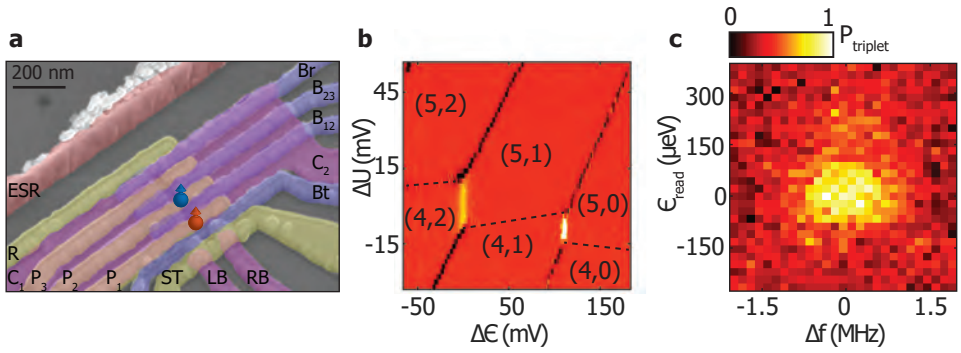

Figure 7.1: **Hot qubit device operation. a** Scanning Electron Microscope (SEM) image of a quantum device identical to the one measured. Gates P1 and P2 define the two quantum dots and gate B12 controls the inter-dot tunnel coupling. The SET is defined by the top gate ST and the two barriers RB and LB, and it is used both as charge sensor and as reservoir [19], while the tunnel rate is controlled by Bt. The gates C1 and C2 confine the electrons in the three quantum dots. Gates R, Br, P3 and B23 are kept grounded during the experiment. **b** Electron occupancy as a function of detuning energy between the two quantum dots ϵ and on-site repulsion energy U. The data have been centred at the (4,2)-(5,1) anticrossing. The electron transitions have been measured via a lock-in technique [20], by applying an excitation of 133 Hz on gate B12. Both electrons are loaded from the SET, with Q2 having a tunnel rate significantly lower than Q1. **c** Readout signal as a function of readout position ϵ_{read} and microwave frequency applied to Q2. When the readout level is positioned between the singlet-triplet energy splitting and the microwave frequency matches the resonance frequency of Q2, we correctly read out the transition from the state $|\downarrow\uparrow\rangle$ to the blocked state $|\uparrow\uparrow\rangle$.

close to the (5,1)-(4,2) charge anticrossing.

Single spins are often initialized via energy-selective tunnelling to a nearby reservoir [23]. However, this method requires a Zeeman splitting much higher than the thermal broadening, limiting the fidelity and making the method unpractical for high-temperature operation. Instead, Pauli spin blockade offers a convenient mechanism to perform initialization and readout [4, 24], with a relevant energy scale corresponding to the singlet-triplet energy splitting, which is set by the large and tunable valley splitting energy in silicon metal-oxide-semiconductor (SiMOS) devices [25]. This method is more robust against thermal noise and enables independent optimization of the qubit operation frequency. We choose to set the magnetic field to B = 0.25 T, which corresponds to addressable qubits with Larmor frequencies ν_{Q1} = 6.949 GHz and ν_{Q2} = 6.958 GHz in the absence of exchange interaction. This low frequency operation reduces the qubit sensitivity to electrical noise that couples in via the spin-orbit coupling [26]. It additionally simplifies the demands on the electronic control circuits and reduces the cable losses.

7.3. Single-qubit characterisation

The pulse sequence used in the experiment is schematically shown in Fig. 7.3a. The sequence starts by pulsing deep into the (4,2) charge state, where the spins quickly relax to the singlet state. An adiabatic pulse to the (5,1) regime is applied to initialize the system in the $|\downarrow\uparrow\rangle$ state. At this position in detuning energy ϵ, single-

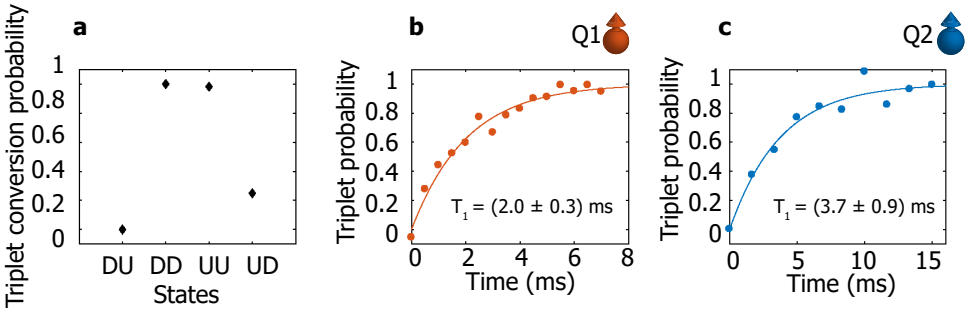

Figure 7.2: **Spin to charge conversion and spin lifetimes. a** Normalized probability that the four two-electron spin states are detected as a triplet state. The probability that the triplet antiparallel spin state is correctly identified as a triplet can be lowered by the non perfect adiabaticity of the pulse and by a faster triplet-singlet relaxation **b-c** Single-spin relaxation times of Q1 and Q2. The measurements are performed by fitting the decay of the states $|\downarrow\uparrow\rangle$ and $|\uparrow\downarrow\rangle$ to the $|\downarrow\downarrow\rangle$ state. We extract $T_{1(Q1)} = 2.0$ ms and $T_{1(Q2)} = 3.7$ ms, consistent with the previous chapter [18]. Triplet probabilities have been normalized to remove readout errors.

and two-qubit gate operations are performed by applying a microwave burst with variable frequency and duration. The sequence ends by adiabatically pulsing to the anticrossing where readout is performed. The antiparallel spin state with the lowest energy (which is in this experiment the state $|\downarrow\uparrow\rangle$) couples directly to the singlet (4,2) charge state. The remaining antiparallel spin state ($|\uparrow\downarrow\rangle$) and the two parallel spin states ($|\uparrow\uparrow\rangle$, $|\downarrow\downarrow\rangle$) couple to the three triplet (4,2) charge states. This allows maaping of the $|\downarrow\uparrow\rangle$ and the other basis states to different charge configurations ((4,2) or (5,1) states), which can be read out using the SET. As shown in Fig. 7.1c, the optimal readout position can be obtained by sweeping ϵ and applying a π-pulse to Q2. From the detuning lever arm of $\alpha_\epsilon = 0.044$ eV/V, extracted from the thermal broadening of the polarization line, we find a readout window of 155 μeV where we can efficiently discriminate between the singlet and triplet states.

In this high-temperature operation mode, the readout visibility is mainly limited by the broadening of the SET peaks. In order to maximize our sensitivity we subtract a reference signal from each trace, then we average and normalize the resulting signal. Relaxation processes can differ for the four two-electron spin states, leading to a different readout visibility. Figure 7.2a shows the normalized readout amplitude for all four states. The probability to correctly read out an $|\uparrow\downarrow\rangle$ state is significantly lower than for the two parallel spin states and the $|\downarrow\uparrow\rangle$ state. This can be attributed to a faster relaxation that can occur due to some finite coupling between the $T_{(1,5)}$ and $S_{(1,5)}$ states. A non-perfect adiabaticity of the pulse can also reduce conversion fidelities. In this experiment we use a ramp time of 1 μs and an integration time of 40 μs limited by the cut-off of the current to voltage converter.

We additionally measure the spin lifetimes of both qubits by measuring the decay of the states $|\downarrow\uparrow\rangle$ and $|\uparrow\downarrow\rangle$ to $|\downarrow\downarrow\rangle$. The state $|\uparrow\downarrow\rangle$ is initialized via a double spin flip following the PSB initialisation discussed above. Figure 7.2b shows the decay traces, from which find values of $T_{1(Q1)} = 2.0$ ms and $T_{1(Q2)} = 3.7$ ms, consistent with the

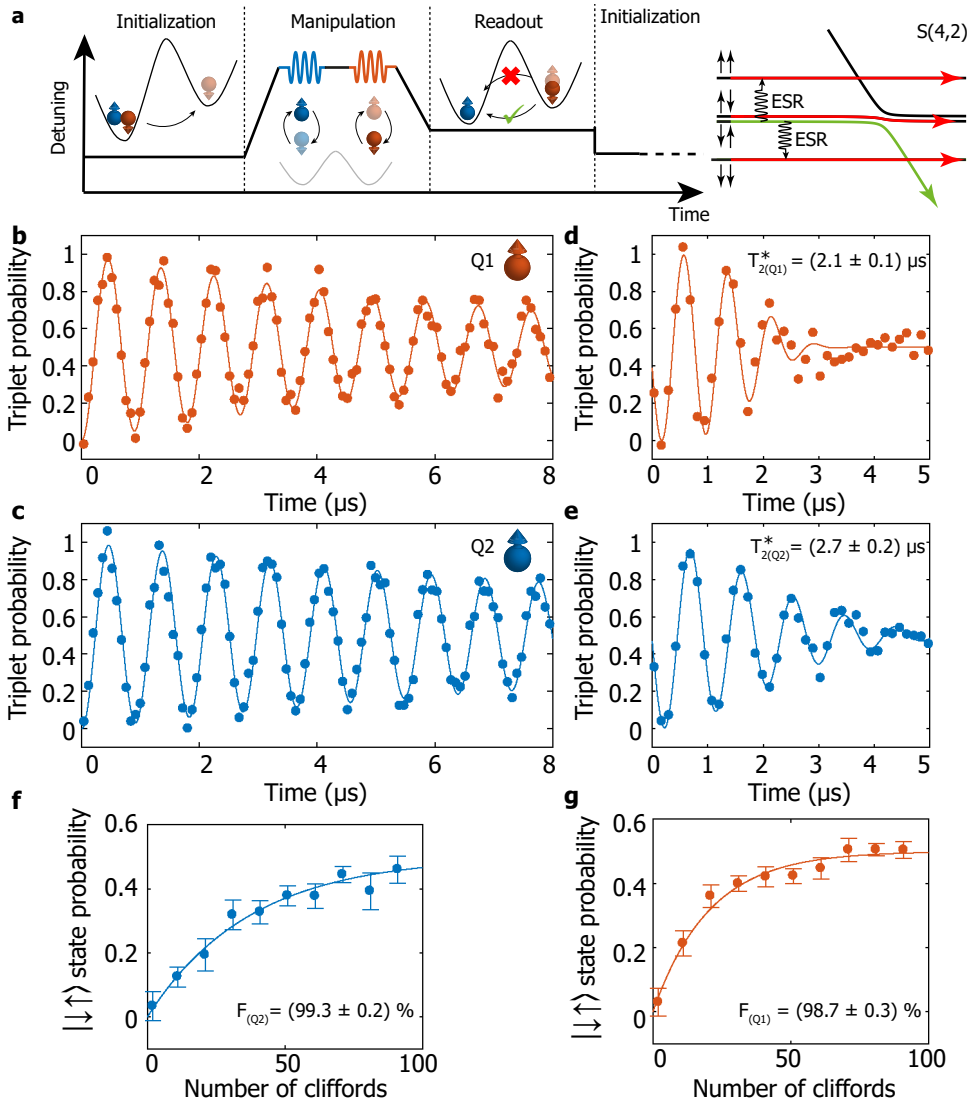

Figure 7.3: **Single-qubit characterization at 1.1 K. a** Pulse sequence used for the experiments. Qubits Q1 and Q2 are defined on the spin states of single-electrons, the remaining four electrons in Q2 fill the first levels and do not contribute to the experiment. A voltage ramp allows adiabatic transitions between the (5,1) and (4,2) charge states. Each measurement cycle consists of two of these sequences. The second cycle contains no microwave pulses and it is used as a reference to cancel low-frequency drifts during readout. **b-c** Rabi oscillations for both qubits as a function of the microwave pulse duration. We extract decay time constants $T_{2(Q1)}^{Rabi} = 8\ \mu$s and $T_{2(Q2)}^{Rabi} = 14\ \mu$s. **d-e** Decay of the Ramsey fringes for both qubits. The data correspond to the average of four traces where each point is obtained from 500 single-shot traces. **f-g** Randomized benchmarking of the single-qubit gates for both qubits. Each data point is obtained from 500 averages of 20 Clifford sequences, for a total of 10.000 single-shot traces. The fidelity reported refers to the primitive gates, while a Clifford-gate contains on average 1.875 primitive gates. We have normalized the state probabilities to remove the readout errors.

results presented in the previous chapter [18].

Figure 7.3b-g shows the single-qubit characterization of the two-qubit system. We observe clear Rabi oscillations for both qubits (Fig. 7.3b, c) as a function of the microwave burst duration. From the decay of the Ramsey fringes (Fig. 7.3d, e) we extract dephasing times $T^*_{2(Q1)} = 2.1$ μs and $T^*_{2(Q2)} = 2.7$ μs, comparable to experiments at similar high temperature [17]. These times are significantly shorter than the longest reported times for ^{28}Si [5], however they are still longer than the dephasing times for natural silicon at base temperature [10, 11].

We characterize the performance of the single-qubit gates of the two qubits by performing randomized benchmarking [27]. In the manipulation phase we apply sequences of random gates extracted from the Clifford group, followed by a recovery gate that brings the system to the $|\downarrow\downarrow\rangle$ and $|\uparrow\uparrow\rangle$ states for Q1 and Q2 respectively. By fitting the decay of the readout signal as a function of the number of applied gates to an exponential decay we extract qubit fidelities $F_{Q1} = 98.7 \pm 0.3$ % and $F_{Q2} = 99.3 \pm 0.2$ %, with the second one above the fault-tolerant threshold.

7.4. Two-qubit gates

We now turn to the two-qubit gate characterization. The ability to tune the exchange interaction [2] is the basis to perform two-qubit operations with electrons in quantum dots. By turning on the exchange interaction, either by controlling the detuning energy or the tunnel coupling, the resonance frequencies of each qubit shift depending on the spin state of the other qubit. The central inset in Fig. 7.4a shows this frequency shift for both qubits as a function of the detuning energy between the two quantum dots, with and without a π-pulse applied to flip the spin state of the other qubit. The full exchange spectrum is composed of the transitions f_1 ($|\downarrow\uparrow\rangle \longrightarrow |\downarrow\downarrow\rangle$), f_2 ($|\uparrow\uparrow\rangle \longrightarrow |\uparrow\downarrow\rangle$), f_3 ($|\downarrow\downarrow\rangle \longrightarrow |\uparrow\downarrow\rangle$) and f_4 ($|\downarrow\uparrow\rangle \longrightarrow |\uparrow\uparrow\rangle$). The exchange interaction J can be extracted as the differences $f_2 - f_1$ and $f_4 - f_3$, from which we measure tunable J in the range 0.5 - 18 MHz (see Fig. 7.6a). At even larger exchange couplings the readout visibility drastically reduces, which we attribute to a decrease of T_2^* (see Fig 7.6b). By fitting the exchange spectrum we extract a tunnel coupling t_c = 0.8 GHz and a Zeeman energy difference δE_z= 9.1 MHz.

Having demonstrated the tunability of the exchange interaction, we use this to demonstrate two-qubit operation. When the exchange is turned on, the resulting shift in resonance frequency can be used to implement state selective ESR transitions (CROT), which are equivalent to a CNOT gate up to single-qubit phases. Figure 7.4 shows controlled oscillations for both qubits, with the control qubit set either to the spin down or spin up state, where we have set the exchange interaction to J = 2.5 MHz. When we prepare the state of the control qubit such that the target qubit is in resonance with the external microwave control, we observe clear oscillations of the target qubit as a function of the microwave burst duration, with no significant decay after multiple rotations. When we flip the state of the control qubit, the resonance frequency of the target qubit is shifted and the target qubit is not driven by the microwave control.

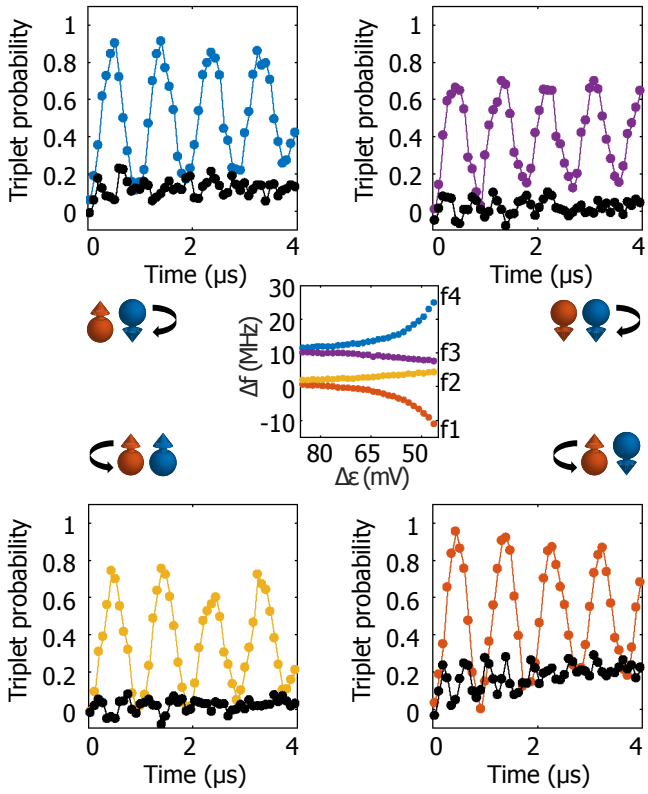

Figure 7.4: **Exchange and two-qubit logic at 1.1 K.** Conditional rotations on all the frequencies f_i, the colour code refers to the central inset showing the full exchange diagram measured as a function of detuning (the frequency offset is 6.948 GHz). The black lines correspond to the same transition f_i driven with the control qubit in the opposite state. An initialization π-pulse and recovery π-pulse are applied to the control qubit for the sequences where either Q1 is in the spin down state or Q2 is in the spin up state. All Rabi frequencies are set to approximately 1 MHz by adjusting the power of the microwave source to compensate for the frequency dependent attenuation of the fridge line. Even when the exchange interaction is turned on we find the resonance frequencies of both qubits to be stable over the course of several hours (see Fig. 7.7).

In order to investigate the coherence of the two-qubit logic, we apply a sequence where we interleave a CROT operation with duration 2π in between two $\pi/2$ single-qubit gates applied to the control qubit with variable phase θ. As shown in Fig. 7.5a, when we invert the second $\pi/2$ pulse ($\theta = \pi$) this cancels out the π phase left by the CROT operation on the control qubit and we correctly measure transitions to the $|{\downarrow\downarrow}\rangle$ and $|{\uparrow\uparrow}\rangle$ states. This demonstrates the execution of a coherent CROT, since the control qubit maintains its coherence even when the target qubit is driven.

To show the universality of our gate set we also demonstrate two-qubit randomized benchmarking. We apply random gates from the 11520 two-qubit Clifford group, recover the state to the $|{\downarrow\uparrow}\rangle$ and measure how the singlet probability decays over the number of applied gates. The decay is shown in Fig. 7.5c and the primitive

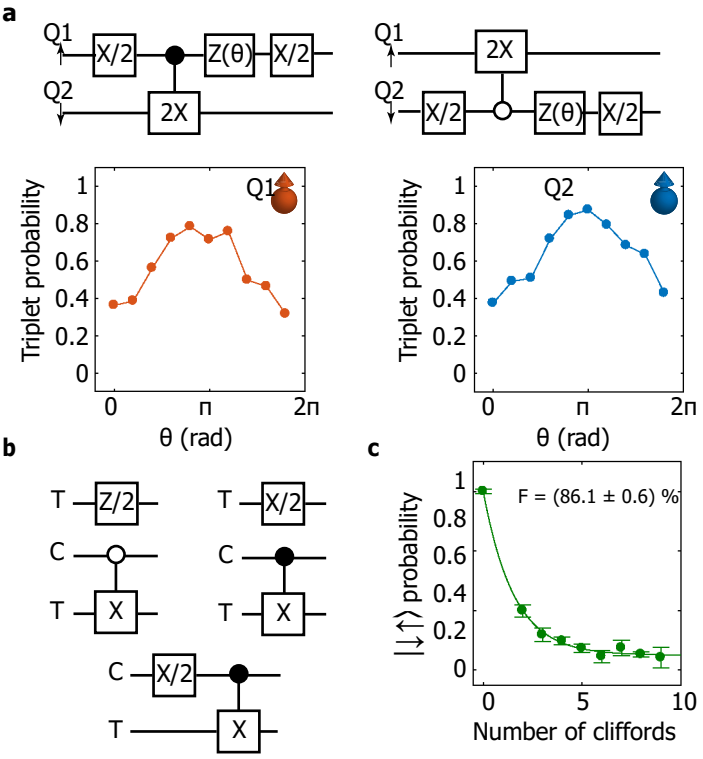

Figure 7.5: **Exchange and two-qubit logic at 1.1 K. a** Phase acquired by the control qubit during a CROT operation. A CROT gate, together with a Z-rotation of $\pi/2$ on the control qubit is equivalent to a CNOT operation. Z gates are implemented by a software change of the reference frame. **b** Primitive gates used to generate the two-qubit Clifford group (11520 gates in total). On average, each Clifford contains 2.5694 primitive gates. Since the Z/2 gates are implemented via a software change of the reference frame, they are not included in the gate count. All gates shown in the figure (except for the Z/2 gate) are implemented with two $\pi/2$ controlled rotations. The compilation scheme is identical to the one in [12]. **c** Decay of the $|\downarrow\uparrow\rangle$ state probability as a function of the number of two-qubit Cliffords applied. A recovery gate returns the system to the $|\downarrow\uparrow\rangle$ state. Since we include the recovery gate in the Cliffords count, the first data point corresponds to $N_{\text{Cliff}} = 2$. Each data point corresponds to the average of 150 random sequences. The fidelity F = 86.1 ± 0.6 % corresponds to the average fidelity of the primitive gates shown in **c**. We have normalized the state probabilities to remove the readout errors.

gates used in 7.5b. The lower fidelity (F = 86.1 ± 0.6 %) compared to the single-qubit benchmark can be attributed to the longer time spent by the qubits idling, which causes them to decohere faster. Possible improvements include simultaneous driving of two transitions to reduce idling times, optimized pulse shaping to reduce accidental excitations of nearby transitions and operation at the symmetry point [28, 29].

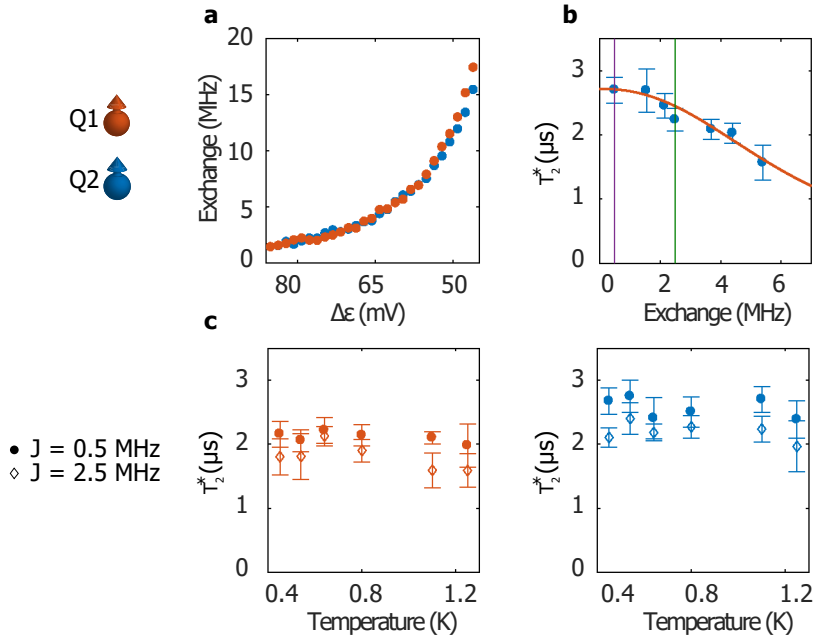

Figure 7.6: **Dephasing dependence on temperature and exchange interaction.** **a** Exchange energy measured as a function of detuning. The data correspond to $f_2 - f_1$ and $f_4 - f_3$ as obtained from Fig. 7.4a. **b** Dephasing time of Q2 as a function of the exchange interaction, fitted with a model taking into account gaussian quasi static noise.**c** Temperature dependence of the dephasing times with the exchange interaction set to the minimum obtained by sweeping ϵ (J = 0.5 MHz) and with the exchange interaction set to acquire the CROT operations of Fig. 7.4a (J = 2.5 MHz).

7.5. Temperature dependence of T_2^*

To further investigate the quantum coherence of the system we measure the decay of the Ramsey fringes for different values of the exchange interaction, see Fig. 7.6b. We find that by increasing the exchange interaction the coherence is reduced, which we explain by the increased qubit sensitivity to electrical noise. We can fit the data with a model that includes quasi-static electrical noise coupling in via the exchange interaction and via the Zeeman energy difference between the two qubits. From the fit we extract the fluctuation amplitudes $\delta_\epsilon = 21$ μeV (corresponding to a power spectrum at 1 Hz of $A_\epsilon \approx 6$ μeV/$\sqrt{\text{Hz}}$) and $\delta_{E_Z} = 400$ kHz. The noise in ϵ is comparable with values extracted at fridge base temperature [30], and consistent with charge noise values extracted from current fluctuation measurements of SETs [18, 31]. To analyse the thermal impact, we characterize the temperature dependence of T_2^* for two values of exchange ($J = 0.5$ MHz and $J = 2.5$ MHz) and we find it to be approximately stable in the range T = 0.45 K - 1.25 K (see Fig. 7.6c). While weak dependencies of T_2^* have been reported in other single-qubit experiments [17], we observe here that the weak temperature dependence is maintained even when the exchange interaction is set to an appreciable value where we can perform two-qubit logic.

The origin of the electrical noise limiting T_2^* can potentially come from extrinsic or intrinsic sources. Although we cannot rule out all extrinsic noise sources, we have confirmed that attenuating the transmission lines does not affect the T_2^* and we thus rule out a direct impact of the waveform generator and the microwave source. When intrinsic charge noise is the dominant contribution, a simple model based on an infinite number of two-level fluctuators (TLFs) predicts a square root dependence of the dephasing rate on the temperature [32]. If we assume a large ensemble of TLFs, a linear temperature dependence is expected (see Chapter 6 [18]) assuming that the number of 'activated' TLFs increases with temperature. For a large ensemble the noise spectral density reads [32]

$$S(\omega) \propto \int_{2\pi f_{\mathrm{rf}}}^{2\pi f_{\mathrm{uv}}} \mathcal{P}(\nu, T) S(\omega, \nu)\, d\nu, \tag{7.1}$$

where $\mathcal{P}(\nu, T)$ describes the contribution of the process with a switching rate between ν and $\nu + d\nu$, thus, the probability density of a TLFs that contributes to the dephasing process. Assuming a temperature dependent switching rate $\nu = \nu_0 e^{-E/(k_B T)}$ leads to $\mathcal{P}(\nu, T) = \mathcal{P}(E, T)|\partial\nu/\partial E|^{-1}$ and one finds $\mathcal{P}(\nu, T) = \mathcal{P}(E, T) k_B T/\nu$ [32]. Assuming a constant distribution of activation energies, $\mathcal{P}(E, T) =$ const and inserting this into Eq. 7.1 the characteristic $1/f$ noise with a linear temperature dependence can be reproduced [30],

$$S(\omega) \approx \mathcal{P}(E, T) k_B T \frac{2\pi}{\omega} \equiv \frac{A_\epsilon}{\omega} \tag{7.2}$$

for $2\pi f_{\mathrm{rf}} \leq \omega \leq 2\pi f_{\mathrm{uv}}$. However, recent work shows that the assumption of a constant distribution of activation energies $\mathcal{P}(E, T)$ is not entirely valid, deviations from this assumption have been observed in SET measurements [33], and this can lead to anomalous temperature dependencies. The small size of quantum dots, in particular SiMOS qubits, may lead to only a few TLFs being relevant for the dephasing and these may explain the observed weak temperature dependence. The power spectral density of a single TLF is given by [32]

$$S(\omega, \nu) = \frac{A}{2\cosh^2[E/(2k_B T)]} \frac{\nu}{\nu^2 + \omega^2}. \tag{7.3}$$

Here, A is the coupling strength of the fluctuations, E the (activation) energy gap between the two states of the TLF, and ν the switching rate. An explanation for the weak temperature dependence of T_2^* that is observed arises from the fact that Eq. 7.3 saturates if $k_B T \gg E$. Assuming that only a few TLFs couple to our system there is only a small probability to find a TLF which has an activation energy E exactly in the temperature range between 0.4 K till 1.2 K. The same arguments hold if instead of a two-level fluctuator an Anderson impurity is the origin of charge noise [34].

We also analyse the stability of the system in the low-temperature regime. Figure 7.7 shows the drift of frequencies f_1 and f_2 over the course of more than 5 hours. Despite the elevated temperature, the frequency peaks, which are approximately 1

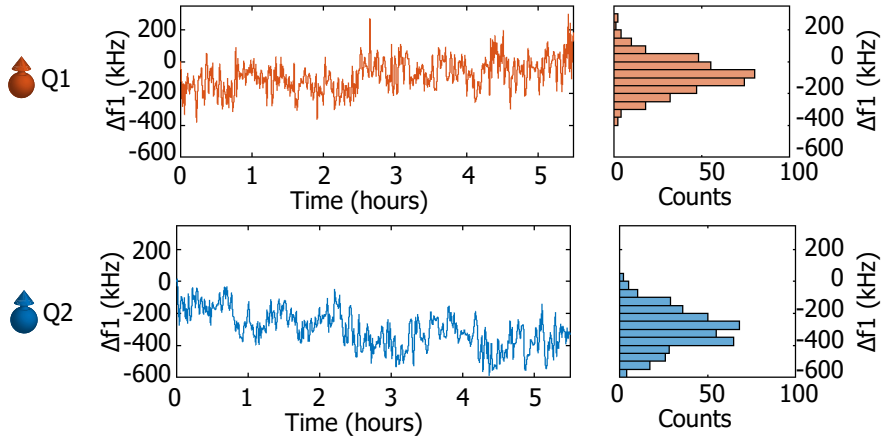

Figure 7.7: **Time dependence of resonance frequencies** f_1 and f_4 of Q1 and Q2 respectively. The exchange interaction is set to 2.5 MHz. The data have been offset by 6.9491 GHz and 6.9620 GHz for f_1 and f_4 respectively.

MHZ broad, shift only by 200-300 kHz, which doesn't put a lot of constraints on the calibration routines. The qubit resonance frequencies fluctuate due to the always-on exchange interaction, causing small variations in detuning ϵ and on-site energy U to directly couple directly to frequency. We can correlate the frequency fluctuations to variations in the readout point, meaning that low-frequency charge noise dominates over magnetic noise. Therefore, the ability to turn the exchange interaction completely off should drastically reduce the magnitude of these fluctuations, simplifying the calibration routines even further.

Importantly, the weak dependence of T_2^* on temperature makes silicon qubits remarkably robust against temperature, enabling to execute a universal quantum gate set. The ability to operate lithographically defined qubits above one Kelvin resolves one of the key challenges toward the integration of quantum hardware and control electronics on the same chip. This integration can reduce the number of lines going from room temperature to the device and, at the same time, greatly simplify on-chip wiring, facilitating the realization of quantum integrated circuits for large-scale quantum computation.

7.6. Outlook

The demonstration of hot qubit operations is an important milestone toward the realization of a SiMOS quantum computer. While fault-tolerant fidelity has not been reached, the results of this chapter are a proof of principle and the weak temperature dependence shows that it feasible to increase the operating temperature of qubits. Experiments on holes in silicon at temperatures up to 4.5 K [35] further support this robustness against temperature. Because T_2^* currently is the limiting factor for two-qubit gate fidelity, the next chapter will suggest optimisations in qubit control.

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8

High-fidelity two-qubit gates in silicon above one Kelvin

Yesterday's sensation is today's calibration,
and tomorrow's background.

Richard P. Feynman

Qubit logic is commonly implemented by pulsing the exchange interaction, to realize a CPHASE gate, or via driven rotations, to realize a CROT gate. Despite demonstrations of entangling SWAP oscillations, the integration with single-qubit control to create a universal gate set as originally proposed for single spins in quantum dots has remained elusive. In this chapter we show that we can overcome these limitations and execute a multitude of native two-qubit gates, together with single-qubit control, in a single device, reducing the operation overhead to perform quantum algorithms. We demonstrate single-qubit rotations together with the two-qubit gates CROT, CPHASE and SWAP. Furthermore, we introduce novel adiabatic and diabatic composite sequences, which allow the execution of CPHASE and SWAP gates on the same device, despite the finite Zeeman energy difference. Both two-qubit gates can be executed in less than 100 ns and, by theoretically analysing the experimental noise sources, we predict control fidelities exceeding 99%, even for operation above one Kelvin.

Parts of this chapter have been published as a preprint in arXiv 2007.09034 (2020) [1].

8.1. Introduction

Two-qubit gates are at the heart of quantum information science, as they may be used to create entangled states with a complexity beyond what is classically simulatable [2], and ultimately may enable the execution of practically relevant quantum algorithms [3]. Optimizing two-qubit gates is therefore a central aspect across all qubit platforms [4]. In quantum dot systems, two-qubit gates can be naturally implemented using the exchange interaction between spin qubits in neighbouring quantum dots [5]. Pulsing the interaction drives SWAP oscillations when the exchange energy is much larger than the Zeeman energy difference of the qubits [5, 6], while it results in CPHASE oscillations when the Zeeman energy difference is much larger than the exchange energy [7]. Single-qubit gates need also to be implemented to access the full two-qubit Hilbert space, and this requires distinguishability between the qubits. This is commonly obtained through the spin-orbit coupling [8] or by integrating nanomagnets [9, 10], causing significant Zeeman energy differences. Realizing a high-fidelity SWAP-gate in this scenario would require extremely large values of exchange interaction. For this reason, the CPHASE operation has been the native gate in experimental demonstrations of two-qubit logic when the exchange interaction is pulsed [11–13]. An alternative implementation of two-qubit logic can be realized by driven rotations, which become state dependent in the presence of exchange interaction and can be used to realize CROT operations [14–17]. Driving rotations can also be used to realize a resonant SWAP gate [18], which can be used to perform state swapping.

While universal quantum logic can be obtained by combinations of single-qubit rotations and an entangling two-qubit operation [19], the ability to directly execute a multitude of two-qubit gates would reduce the number of operations required to execute practical algorithms. Here, we demonstrate on the same device the implementation of the CROT, SWAP, and CPHASE, which are all essential gates in quantum computing and error correction applications. SWAP operations can in particular be useful in large quantum dot arrays, providing a means to achieve beyond nearest-neighbor connectivity. We overcome the limitations imposed by the finite Zeeman energy difference between the qubits by introducing novel control sequences, which also allow the execution of the CPHASE and the SWAP in short time scales and a predicted high-fidelity. Moreover, we demonstrate these operations at temperatures exceeding one Kelvin. The cooling power at these elevated temperatures is much larger and thereby more compatible with the operation of classical electronics, such that quantum integrated circuits based on standard semiconductor technology become feasible [20–22].

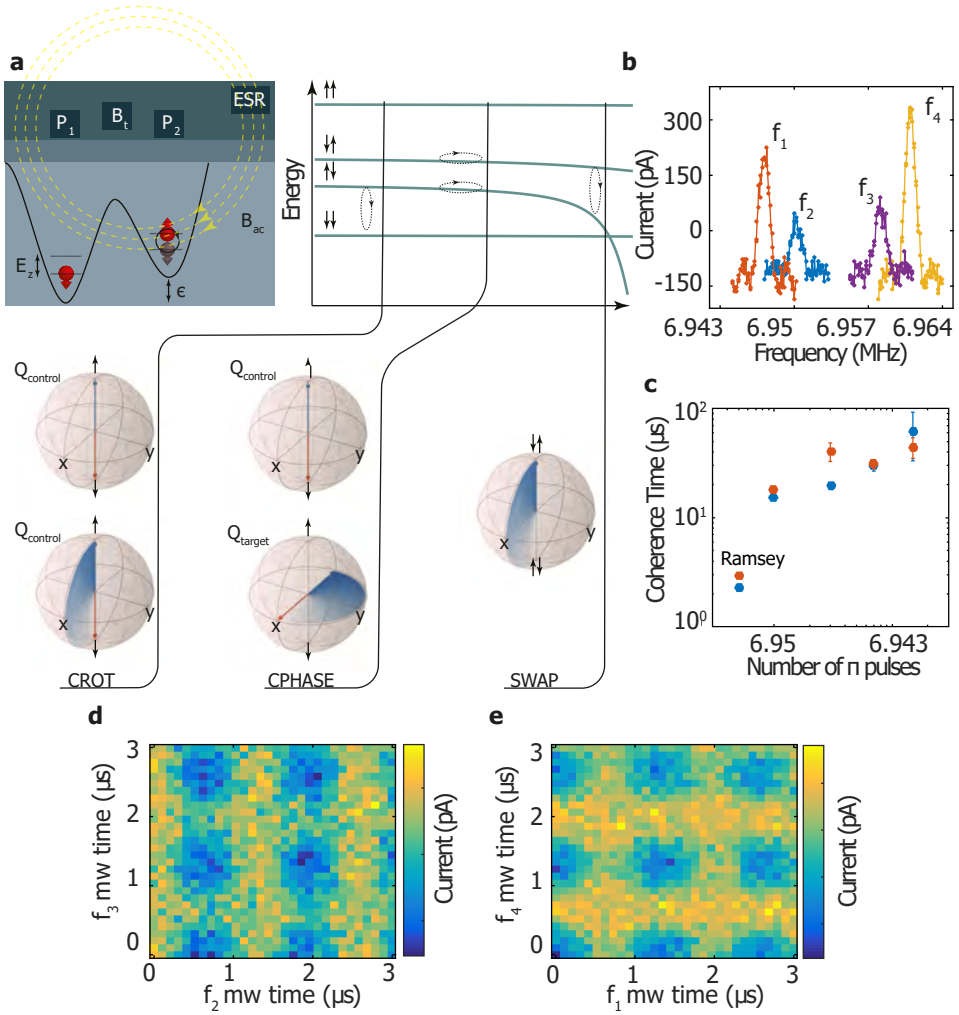

Figure 8.1: **Two-qubit gates and quantum coherence of silicon spin qubits operated at a T = 1.05 K. a** Schematic representation of the double quantum dot system. The device is the same as used in Chapter 7. Two plunger gates (P_1 and P_2) and one barrier gate (B_t) are used to control the detuning energy ϵ and the tunnel coupling t between the quantum dots. Spin manipulation occurs via electron-spin-resonance (ESR) using an on-chip microwave line. The energy diagram displays the four electron spin states as a function of ϵ. We exploit both driven rotations and pulsed exchange for coherent control. Controlled rotations (CROTs) can in principle be executed at all points where $J \neq 0$, given that gate times are appropriately set. CPHASE gates are conveniently executed when the exchange interaction is much smaller than the Zeeman energy difference between the qubits, while SWAP oscillations can be realized when the exchange interaction is much larger. **b** Using ESR control we find the four resonance frequencies of the two-qubit system. Here, the exchange interaction is tuned to 3 MHz. The spectrum is composed of the frequencies: f_1 ($|\uparrow\downarrow\rangle \longrightarrow |\downarrow\downarrow\rangle$), f_2 ($|\downarrow\downarrow\rangle \longrightarrow |\downarrow\uparrow\rangle$), f_3 ($|\uparrow\uparrow\rangle \longrightarrow |\downarrow\uparrow\rangle$) and f_4 ($|\uparrow\downarrow\rangle \longrightarrow |\uparrow\uparrow\rangle$). **c** Coherence times as a function of the number of refocusing π pulses. Here, the exchange is set to 2 MHz. The plot includes the dephasing times measured through a Ramsey experiment to allow comparison. **d-e** Realization of CROT operations. Rabi oscillations of the target qubit are controlled by the spin state of the control qubit. We find controlled rotations on all the four resonance frequencies f_1, f_2, f_3, f_4.

8.2. Two-qubit system

The experimental two-qubit system is based on electron spin states confined in a silicon double quantum dot as schematically shown in Fig. 8.1a. The silicon double quantum dot is fabricated using an overlapping gate architecture on a silicon wafer with an isotopically enriched ^{28}Si epilayer of 800 ppm residual concentration of ^{29}Si [17, 23]. In order to obtain an optimal exchange coupling between the electrons, qubits $Q1$ and $Q2$ are defined with N_{Q1} = 1 and N_{Q2} = 5, where N is the charge occupancy. Spin readout is performed at the (1,5)-(2,4) charge anticrossing, where the $|\downarrow\uparrow\rangle$ tunnels to the singlet (2,4) charge state, while the other spin states are blocked because of the Pauli exclusion principle. By using an adiabatic pulse from the (2,4) to the (1,5) region, we initialize the system in the $|\downarrow\uparrow\rangle$ state. Because of the limited sensitivity of the single-electron-transistor (SET) that we use for charge readout, we average the single-shot readout traces and subtract a reference signal. We therefore obtain a current signal, proportional to the probability to have a blocked state. We note that the readout fidelity can be further improved, even at these higher temperatures [24], but here we focus on the coherent control. We perform spin manipulation via electron spin resonance (ESR) using an on-chip aluminum microwave antenna. All measurements have been performed in a dilution refrigerator at a temperature of $T_{\text{fridge}} = 1.05$ K and with an external magnetic field of $B_{\text{ext}} = 250$ mT.

8.3. Controlled rotations

Similar to the experiments in Chapter 7we control the exchange interaction J via the detuning ϵ between the two quantum dots and we measure couplings from $J = 2$ MHz up to $J = 45$ MHz, as measured from the frequency of SWAP oscillations and the shift in the energy of the qubit resonance frequencies. By fitting the exchange spectrum we extract a Zeeman energy difference between the two qubits $\Delta E_z = 11$ MHz, which originates from the electron g-factor variations due to spin-orbit coupling. This frequency difference is large enough to have a negligible impact on qubit control fidelities. The fitting suggests a negligible dependence of ΔE_z on detuning, further supported by the small magnetic field applied and the absence of external magnetic gradients. Figure 8.1b shows the four resonance frequencies of the two-qubit system when $J = 3$ MHz. At this value of exchange interaction we tune the π-rotation times to be $t_{\text{CROT}} = 660$ ns such that we synchronize the Rabi oscillations of the target transition with the closest off-resonant transition in order to suppress crosstalk [25]. From Ramsey experiments on frequencies f_1 and f_4 we measure dephasing times $T^*_{2,Q1} = 2.3$ µs and $T^*_{2,Q2} = 2.9$ µs. The Carr-Purcell-Meiboom-Gill (CPMG) pulse sequence can extend the coherence times, by filtering out the low-frequency noise. As shown in Fig. 8.1c, we measure a maximum $T_{2,Q1} = 63$ µs and $T_{2,Q2} = 44$ µs when 15 refocusing pulses are applied, setting new benchmarks for the coherence time of quantum dot spin qubits at temperatures above one Kelvin.

When the exchange interaction is set to a non-zero value, it is possible to realize the CROT via driven rotations since the resonance frequency of one qubit depends

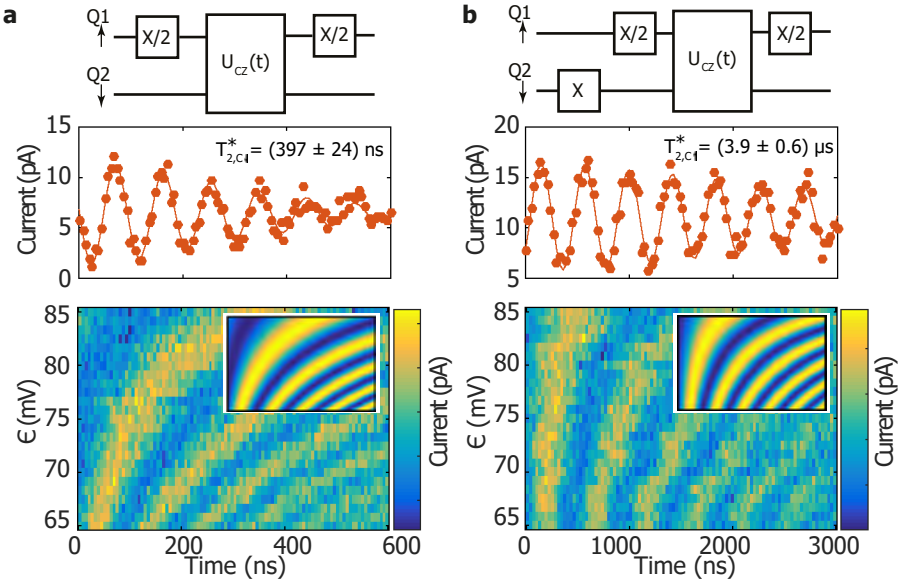

Figure 8.2: **Adiabatic CPHASE operation at T = 1.05 K. a-b** Conditional phase oscillations by adiabatically pulsing the detuning energy ϵ to increase the exchange interaction J, measured using the quantum circuit depicted in the top panels. The antiparallel spin states acquire a phase with respect to the parallel states, resulting in coherent oscillations as a function of the duration of the detuning pulse. At smaller detuning values, the exchange interaction increases resulting in faster oscillations. Due to the exchange interaction, the energy difference $E_{\downarrow\uparrow} - E_{\downarrow\downarrow}$ (measured in **a**) is smaller than $E_{\uparrow\uparrow} - E_{\uparrow\downarrow}$ (measured in **b**), resulting in an acquired phase on the target qubit (T) that is dependent on the state of the control qubit (C).

on the state of the other qubit. This CROT gate is a universal two-qubit gate and equivalent to a CNOT gate up to single-qubit phases [17]. Figures 8.1d-e show controlled rotations by setting both configurations of target and control qubits.

8.4. CPHASE gate

An alternative way to achieve a universal gate set is through the implementation of the CPHASE gate. Moving in detuning energy toward the (1,5)-(2,4) charge anticrossing lowers the energy of the antiparallel $|\downarrow\uparrow\rangle$ and $|\uparrow\downarrow\rangle$ states with respect to the parallel $|\downarrow\downarrow\rangle$ and $|\uparrow\uparrow\rangle$ spin states. Therefore, pulsing the detuning for a time t results in a phase gate on the target qubit conditional on the spin state of the control qubit. When the total phase $\phi = \phi_{|\downarrow\uparrow\rangle} + \phi_{|\uparrow\downarrow\rangle} = (2n+1)\pi$ with n integer, a CPHASE gate is realized [7]. A high-fidelity implementation of such a gate requires a Zeeman energy difference between the two qubits much larger than the exchange interaction, in order to suppress the evolution of the exchange gate [5]. This condition is conveniently met in devices with micromagnets [12, 14], where the CPHASE is the most natural choice as the native two-qubit gate.

In our system, ΔE_z is comparable in magnitude to the accessible J, due to the small B_{ext} applied. This means that a detuning pulse will also cause the $|\downarrow\uparrow\rangle$ and

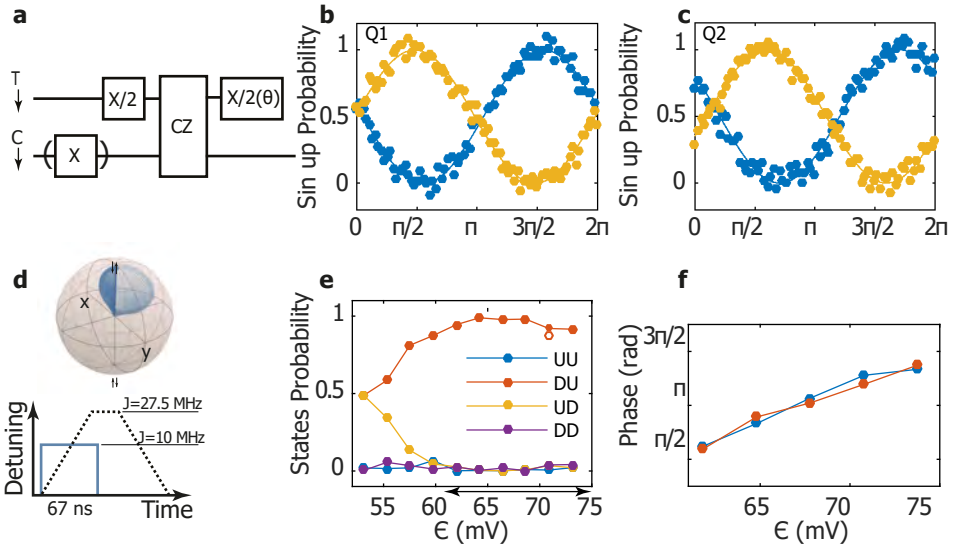

Figure 8.3: **Adiabatic and diabatic CPHASE operation at T = 1.05 K. a** Schematic of the quantum circuit to verify CPHASE operation. The adiabatic detuning pulse of the CPHASE gate is tuned such that the antiparallel spin states acquire a total phase of π. The exchange is increased to J = 27.5 MHz using a ramp t_r = 60 ns and the total gate time is t_{CPHASE} = 152 ns. b-c We verify CPHASE operation by measuring the normalized spin-up probability, obtained through conversion of the readout current, and observe clear antiparallel oscillations. **d** Schematic representation of an adiabatic (dashed black) and a diabatic (solid blue) CPHASE. **e** The diabatic CPHASE is optimized by changing the amplitude of ϵ and measuring the probabilities of the four possible spin states. Due to the finite Zeeman difference (ΔE_z = 11 MHz) SWAP-interactions are not negligible. However, the exchange can be tuned such that the states undergo rotations of 2π. **f** We tune and optimize this by measuring the phase, projected to the spin states through a $\pi/2$-pulse on the target qubit. We obtain a diabatic CPHASE for t_{CPHASE} = 67 ns.

8

$|\uparrow\downarrow\rangle$ states to undergo SWAP rotations. While these rotations occur along a tilted angle due to the non-zero ΔE_z, they can still reduce the fidelity of the CPHASE gate. In order to avoid unwanted SWAP rotations we implement an adiabatic detuning pulse, by ramping ϵ to the desired value instead of changing it instantaneously (see schematic in Fig. 8.2b). In this way, a high-fidelity CPHASE gate can still be realized with an arbitrarily small ΔE_z at the cost of a longer gate time. In Fig. 8.2a and 8.2b we change the duration of a detuning pulse in between a Ramsey-like experiment on Q1, with and without a π pulse applied to Q2. The frequency of the oscillations of Q1 depends strongly on the spin state of Q2, thereby demonstrating a controlled phase operation. Because of the finite Zeeman energy difference, the antiparallel $|\downarrow\uparrow\rangle$ state shifts significantly more in energy than the $|\uparrow\downarrow\rangle$ state. Consequently, the oscillations in Fig. 8.2a are significantly faster than in Fig. 8.2b. Similarly, the decay time in Fig. 8.2b is significantly longer than in Fig. 8.2a because of the lower sensitivity to electrical noise. In Fig. 8.3a-c the pulse time is calibrated such that the total phase $\phi = \pi$. We measure this in a Ramsey-like experiment where we probe the phase acquired by the target qubit for different control qubit states.

From Fig. 8.3b and c we can observe that the resulting oscillations are nicely out-of-phase, which demonstrates the CPHASE gate. We achieve a gate time t_{CPHASE} = 152 ns, which is mostly limited by the adiabatic ramps which take t_{r} = 60 ns. From a comparison with simulations we find that the contribution of both ramps to the total phase ϕ is approximately 1.7π.

This gate time can be significantly sped up with the implementation of a geometric CPHASE gate, that does not require adiabaticity [26]. For the implementation of this gate we synchronize the unwanted exchange oscillations with the total gate duration, i.e. our gate performs a CPHASE evolution while the exchange oscillations performs a complete cycle. For a perfectly diabatic pulse the condition for the exchange interaction is:

$$J = (4J_{\mathrm{res}} + \sqrt{3\Delta E_z^2 + 4J_{\mathrm{res}}^2})/3, \tag{8.1}$$

where J_{res} is the residual exchange interaction at the point where we perform CROT gates.

Figures 8.3c-e show the experimental implementation of the geometric CPHASE gate. We sweep the amplitude of the detuning pulse and monitor the spin state probabilities in (see section 8.9) during exchange oscillations, and the total phase acquired by the antiparallel spin states. We notice that when $\epsilon \approx 68$ mV, the antiparallel spin states execute a 2π rotation, while acquiring a total phase shift of π. At this value of detuning we measure $J \approx 10$ MHz and therefore in agreement with Eq. 8.1. The total gate time is reduced here to $t_{\mathrm{CPHASE}} = 67$ ns.

8.5. SWAP gate

We now turn to the implementation of a SWAP gate, the originally proposed quantum gate for quantum dots [5]. Despite the experimental demonstration of exchange oscillations [6, 27, 28], its implementation together with single-qubit gates is rather challenging because of the requirement of a negligible Zeeman difference between the qubits. In the following, we will discuss a novel protocol that can overcome this problem and allow for a high-fidelity SWAP gate, even in the presence of a finite ΔE_z.

In order to observe SWAP oscillations, we implement a sequence where we initialize in the $|{\downarrow}{\uparrow}\rangle$ state and pulse ϵ for a time t. Clear exchange oscillations between the $|{\downarrow}{\uparrow}\rangle$ and the $|{\uparrow}{\downarrow}\rangle$ state are visible when the detuning pulse is diabatic (see Fig. 8.4a), where the oscillation frequency is $f_{\mathrm{SWAP}} = \sqrt{J^2 + \Delta E_z^2}$. As we make the pulse more adiabatic by ramping ϵ, the oscillations disappear and the regime becomes suitable for a CPHASE implementation as discussed before. Even when the detuning pulse is perfectly diabatic, we do not obtain a perfect SWAP due to the finite ΔE_z. Instead, the spin states rotate in the Bloch sphere around the tilted axis of rotation $r = (J, 0, \Delta E_z)^T$, similar to what happens for off-resonant driving. Figure 8.4c and 8.4d show that when starting in the $|{\downarrow}{\uparrow}\rangle$ state, a maximum $|{\uparrow}{\downarrow}\rangle$ state probability of 64% is obtained in $t_{\mathrm{SWAP}} = 18$ ns, which is in agreement with our simulated predictions (see section 8.7).

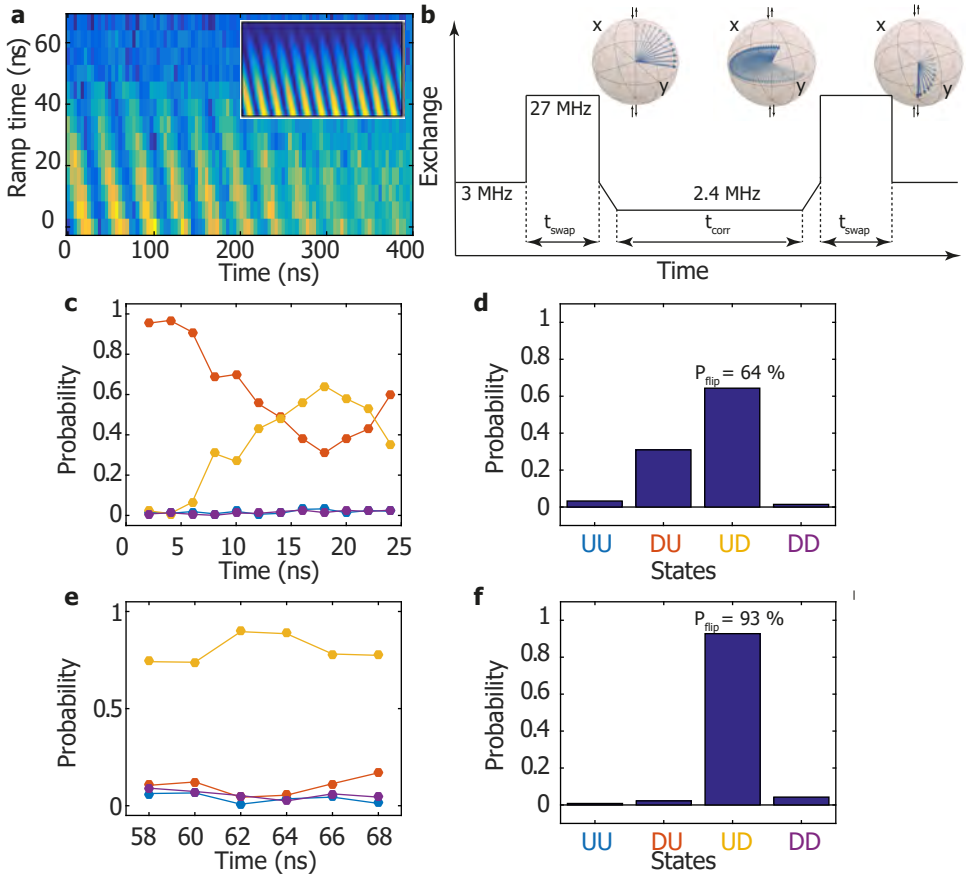

Figure 8.4: **Pulsed SWAP and composite exchange pulse for high-fidelity SWAP at T = 1.05 K. a** SWAP oscillations as a function of the ramp time for a detuning pulse such that $J = 23$ MHz. When the pulsing becomes adiabatic with respect to variations in J, the exchange oscillations are suppressed. In order to maximize the readout signal we project the $|\uparrow\downarrow\rangle$ to the $|\uparrow\uparrow\rangle$ with a π pulse on f_2. **b** Pulse sequence of the composite SWAP gate to correct for errors coming from the finite Zeeman energy difference. The Bloch spheres on top show the time evolution when starting in the $|\downarrow\uparrow\rangle$ state, with the Bloch vector depicted in nanosecond time steps. We first diabatically pulse the exchange to $J = 27$ MHz, in order to bring the state on the equator of the singlet-triplet Bloch sphere. Then we correct for the phase offset with an adiabatic exchange pulse to $J = 2.4$ MHz. We complete the state flip with another exchange pulse to $J = 27$ MHz. **c-d** Probabilities of the four spin states as a function of the SWAP interaction time. The states $|\uparrow\uparrow\rangle$ and $|\downarrow\downarrow\rangle$ are not affected, while the states $|\downarrow\uparrow\rangle$ and $|\uparrow\downarrow\rangle$ oscillate. Due to the finite Zeeman difference we achieve a maximum $|\uparrow\downarrow\rangle$ state probability of 64 % for $t_{\mathrm{SWAP}} = 18$ ns. The exchange interaction is set to $J = 27$ MHz. **e** Spin state probability after applying the composite SWAP and as a function of the adiabatic pulse time t_{corr}, from which we find the optimum $t_{\mathrm{corr}} = 62$ ns. **f** Spin state probability after executing the composite SWAP sequence starting from the initial state $|\downarrow\uparrow\rangle$. Compared to the detuning pulse as shown in **d** we find a clear improvement in the spin flip SWAP probability.

8.6. Composite gates

Composite pulse sequences [34, 35] can correct for the tilted axis of rotation. It is possible to achieve full population transfer with an exchange sequence consisting

a

	Gate time (ns)	F_{ideal}(%)	F_{noise}(%)
CROT	660	99.4	89.0
CPHASE	152	99.9	97.8
Diabatic CPHASE	67	99.9	99.4
SWAP	19	84.3	84.2
Composite SWAP	89	99.9	99.4

b

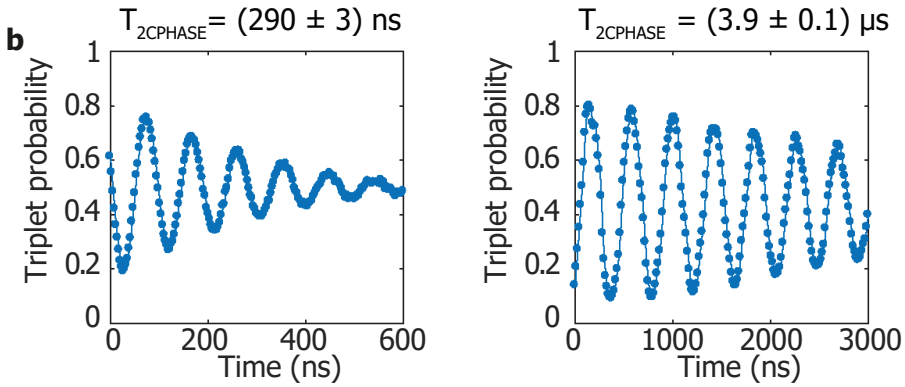

Figure 8.5: **Gate times and simulated fidelities for silicon qubits at T = 1.05 K. a** Gate times and simulated fidelities for all the two-qubit gates discussed in the main text, where F_{ideal} represent the fidelity in the absence of noise and F_{noise} takes into account the experimental noise at 1.05 Kelvin. We find high-fidelity two-qubit gates can be obtained in silicon above one Kelvin, by using diabatic CPHASE or composite SWAP sequences. The CROT fidelity is calculated as a conditional π-flip for better comparison. Good agreement is obtained with previous experiments [17], confirming that the simulated noise is an accurate estimate of the real noise. Further improvement in the fidelities of the CROT and the CPHASE may be obtained by incorporating pulse shaping [29–33]. **b** Simulated data for the sequence used in Fig. 8.2a and b.

of alternating diabatic and adiabatic exchange pulses. The corresponding time evolution operators in the odd parity subspace are:

$$U_{\mathrm{r}} = e^{i\Phi_{\mathrm{r}}} e^{i\theta_{\mathrm{r}} r\cdot\sigma} \tag{8.2}$$

$$U_{\mathrm{z}} = e^{i\Phi_{\mathrm{z}}} e^{i\theta_{\mathrm{z}}\hat{Z}} \tag{8.3}$$

for a diabatic and an adiabatic pulse respectively. Here $\sigma = (\hat{X}, \hat{Y}, \hat{Z})$ is the vector consisting of the Pauli matrices, $\Phi_{\mathrm{r,z}} = J t_{\mathrm{r,z}}/2$ the accumulated entangling phase during the pulse, and $\theta_{\mathrm{r,z}} = t_{\mathrm{r,z}}\sqrt{J^2 + \Delta E_{\mathrm{z}}^2}/2$ the angle of rotation. The condition for a SWAP gate is $U_{\mathrm{tot}} = U_{\mathrm{r}} U_{\mathrm{z}} U_{\mathrm{r}} U_{\mathrm{z}_2} U_{\mathrm{r}_2} \cdots \equiv \hat{X}$. The number of necessary pulses depends on the angle of rotation; obviously a minimal pulse sequence requires $|\Delta E_{\mathrm{z}}| \leq J$. In the typical regime of operation for devices with micromagnets, where

$J < \Delta E_z$, a multi-step sequence is required. In the limit $J \ll \Delta E_z$ many steps are necessary and the pulse sequence becomes gradually an ac signal giving rise to the ac-SWAP gate [18]. Furthermore, it is essential to include the global phase which corresponds to a conditional phase evolution in the full two-qubit space and needs to vanish when implementing a SWAP gate. This protocol is highly versatile and can also produce maximally entangling gates, i.e., $\sqrt{\text{SWAP}}$ if $U_{\text{tot}} \equiv i\hat{X}/2$ and iSWAP for $U_{\text{tot}} \equiv i\hat{X}$. While finding an optimal sequence for such a composition can be done in general following the procedure of [35], here we extend these considerations into a multi-qubit space, which gives rise to additional constraints.

A possible minimal length solution for a SWAP gate is sketched in Fig. 8.4b and the trajectory of the qubit state is seen in the inset. In the experiment, we calibrate the exchange interaction at all stages of the pulse, fix the time of the diabatic pulses to 12 ns and sweep the length of the adiabatic pulse t_{corr} in order to find the best point. Figure 8.4e shows how the four spin probabilities change when sweeping t_{corr}. We find an optimal $t_{\text{corr}} = 62$ ns and the four spin state probabilities for a total pulse duration $t_{\text{SWAP}} = 88$ ns are plotted in Fig. 8.4f. The SWAP probability exceeds 90%, where the remaining error is dominated by miscalibrations, inaccuracies in the gates needed to reconstruct the spin state probabilities, and state-preparation-and-measurement (SPAM) errors.

8.7. Simulation of fidelities

For all the two-qubit gates we obtain the fidelities by numerically solving the time-dependent Schrodinger equation $i\hbar\dot{\Psi}(t) = H(t)\Psi(t)$ using a step size $t = 50$ ps. We have confirmed that a faster sampling rate does not change the simulation results. In order to resemble real setups and to avoid sampling problems, we filter all time-dependent signals using a high-pass filter with a cut-off frequency of 300 MHz. All simulations are performed using the Heisenberg Hamiltonian

$$H(t) = \Delta E_z(\epsilon)(S_{\text{z,1}} - S_{\text{z,2}})/2 + J(\epsilon)(S_1 \cdot S_2 - 1/4), \tag{8.4}$$

where $S_i = (S_{\text{x,i}}, S_{\text{y,i}}, S_{\text{z,i}})$ is the spin operator of the electron in quantum dot i. The parameters $\Delta E_z(\epsilon)$ and $J(\epsilon)$ are the qubit frequency difference and the exchange interaction which both depend on the detuning ϵ.

To include the effect of decoherence we add stochastic fluctuations of the detuning, $\epsilon \to \epsilon + \delta\epsilon(t)$ to each run of the time evolution and average the resulting density matrix. To emulate the effect of $1/f$ charge noise we generate time-dependent fluctuations $\delta\epsilon(t)$ following a $S(\omega) = A_\epsilon/f$ spectral density using the method described in Ref. [36, 37]. The amplitude of the noise A_ϵ is set such that it reproduces the decay time of the exchange oscillations measured experimentally. Using the same value of noise we then simulate the Ramsey sequences of Fig. 8.2a and 8.2b and we show the results in Fig. 8.5b. The decay times that we extract are in agreement with the measured decays $T^*_{2,\text{C}\downarrow} = (397 \pm 24)$ ns and $T^*_{2,\text{C}\uparrow} = (3.9 \pm 0.6)$ µs

The table in Fig. 8.5a shows the fidelities associated with the two-qubit gates CROT, CPHASE, and SWAP. Here, F_{ideal} represents the simulated fidelities taking into account the relevant parameters, but neglecting any decoherence. We find

$F_{\text{ideal}} > 99\%$ for all gates except the SWAP, which is limited in fidelity by the finite ΔE_z.

We have also modelled the decoherence assuming 1/f noise as the dominant noise source.

By fitting the experimental data in Fig 8.2a and 8.2b, we conclude that our model can reproduce the decoherence with good agreement. Based on these simulations we determine F_{noise}. The fidelity of the CROT and the CPHASE gate are significantly affected by the noise, due to the relatively long gate times, and we find that the predicted CROT fidelity F_{noise} = 89 % is close to the experimentally measured fidelity F = 86 % [17]. The SWAP, diabatic CPHASE and composite SWAP are less affected by the noise and in particular we predict that both the diabatic CPHASE and composite SWAP can be executed with fidelities above 99 %.

8.8. Conclusion

While experimental data will be needed to validate these predictions, these results showcases how a multitude of native two-qubit gates can be executed with high fidelities and remarkable gate speeds. The limiting factor to the fidelities is the charge noise, as we have to significantly pulse the detuning to control the exchange interaction. Significant improvements can be expected by keeping the detuning at zero and instead pulsing the tunnel coupling, as this scheme is to first-order insensitive to charge noise.

The ability to execute a diverse set of high-fidelity two-qubit gates defines silicon quantum dots as a versatile platform for quantum information. The low magnetic field operation and the small Zeeman energy difference between qubits is furthermore beneficial for the realization of scalable qubit tiles, as it supports high-fidelity shuttlers and on-chip resonators for long-distance qubit links. Moreover, the ability to execute quantum logic at temperatures exceeding one Kelvin provides a pathway to quantum integrated circuits that host both the qubits and their control circuitry for scalable quantum hardware.

8.9. Reconstruction of the spin state probabilities

In order to readout the spin states we average all single-shot readout traces and subtract a reference sequence in which no gates are performed. The corresponding readout signal is therefore a current that is proportional to the probability of having a blocked state. In order to be able to reconstruct the four probability amplitudes $|A|^2, |B|^2, |C|^2, |D|^2$ of an arbitrary state $\psi = A\,|\uparrow\uparrow\rangle + B\,|\uparrow\downarrow\rangle + C\,|\downarrow\uparrow\rangle + D\,|\downarrow\downarrow\rangle$ it is necessary to know the current signal of the four spin states $\{\alpha \longrightarrow |\downarrow\uparrow\rangle, \beta \longrightarrow |\uparrow\uparrow\rangle, \gamma \longrightarrow |\downarrow\downarrow\rangle, \delta \longrightarrow |\uparrow\downarrow\rangle\}$. By initializing the $|\downarrow\uparrow\rangle$ state and then using the four frequencies $\mathrm{f}_1, \mathrm{f}_2, \mathrm{f}_3, \mathrm{f}_4$ we can reach all spin states and therefore measure the parameters $\alpha, \beta, \gamma, \delta$.

Once we measure the current signals for all spin states we need to gain information about the state ψ. We therefore apply the following sequences and measure the parameters $\phi_0, \phi_1, \phi_2, \phi_3$:

- Sequence: prepare state ψ and then measure. We measure a current ϕ_0 equal to:

$$\phi_0 = |A|^2\beta + |B|^2\delta + |C|^2\alpha + |D|^2\gamma \tag{8.5}$$

- Sequence: prepare state ψ, apply a π pulse on f1, and then measure. We measure a current ϕ_1 equal to:

$$\phi_1 = |C|^2\beta + |B|^2\delta + |A|^2\alpha + |D|^2\gamma \tag{8.6}$$

- Sequence: prepare state ψ, apply a π pulse on f0, and then measure. We measure a current ϕ_2 equal to:

$$\phi_2 = |A|^2\beta + |B|^2\delta + |D|^2\alpha + |C|^2\gamma \tag{8.7}$$

- Sequence: prepare state ψ, apply a π pulse on f2, apply a π pulse on f1, and then measure. We measure a current ϕ_3 equal to:

$$\phi_3 = |C|^2\beta + |A|^2\delta + |B|^2\alpha + |D|^2\gamma \tag{8.8}$$

Therefore we have the following system of equations, that we want to solve for the probabilities $|A|^2, |B|^2, |C|^2, |D|^2$:

$$\begin{bmatrix} \beta & \delta & \alpha & \gamma \\ \alpha & \delta & \beta & \gamma \\ \beta & \delta & \gamma & \alpha \\ \delta & \alpha & \beta & \gamma \end{bmatrix} \cdot \begin{bmatrix} |A|^2 \\ |B|^2 \\ |C|^2 \\ |D|^2 \end{bmatrix} = \begin{bmatrix} \phi_0 \\ \phi_1 \\ \phi_2 \\ \phi_3 \end{bmatrix} \tag{8.9}$$

We solve the system by inverting the matrix:

$$\begin{bmatrix} |A|^2 \\ |B|^2 \\ |C|^2 \\ |D|^2 \end{bmatrix} = \begin{bmatrix} \beta & \delta & \alpha & \gamma \\ \alpha & \delta & \beta & \gamma \\ \beta & \delta & \gamma & \alpha \\ \delta & \alpha & \beta & \gamma \end{bmatrix}^{-1} \cdot \begin{bmatrix} \phi_0 \\ \phi_1 \\ \phi_2 \\ \phi_3 \end{bmatrix} \tag{8.10}$$

Finally the resulting amplitudes are normalized. The extracted probabilities correspond to the diagonal parts of the density matrix ρ which may violate $\sum_i \rho_{ii} = 1$ due to measurement and gate errors. In order to ensure the physicality of our results we perform a maximum-likelihood estimation [38] using the diagonal elements of the density matrix.

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9

Conclusion and outlook

Problems that remain persistently insoluble should always be suspected as questions asked in the wrong way.

Alan Watts

In this thesis we have taken a close look at several potential semiconductor platforms for quantum computation, narrowed down on SiMOS and proposed an architecture. To limit the number of control lines, we require integrated control electronics and consequently "hot qubits". The following chapters focused on the optimization and characterisation of high ($\approx$ 1 Kelvin) temperature operation of spin qubits in SiMOS quantum dots. In this final chapter I will comment on the significance of these results, discuss improvements that could be made and suggest possible further research. Finally, I will discuss challenges of large-scale quantum computing and the feasibility of implementing it in silicon.

9.1. Conclusion

The goal of my research over the past four years was to demonstrate the feasibility of hot qubits in the silicon metal-oxide-semiconductor platform, to take advantage of the highly advanced CMOS processing. The results are encouraging for the integration of quantum technology with the classical computing industry, a milestone towards achieving the radical scaling that is necessary.

We presented an integration scheme that can be used for quantum dot arrays in the group IV semiconductor platforms SiMOS, Si/SiGe and Ge/SiGe in Chapter 3, allowing us to study each material with minimal overhead. This allowed for a rapid development of quantum dots and qubits in the new Ge/SiGe platform [1–4]. It is still undetermined which platform is the best for a large-scale quantum computer, a quantitative comparison will be necessary such that a proper analysis of the trade-offs is possible. To focus the research, we narrowed down on SiMOS, chosen to take maximum advantage of the compatibility with conventional CMOS technology

The architecture for a SiMOS based quantum processor that is proposed in Chapter 4 provides an example of fundamental components that are required: a dense two-dimensional qubit system based on quantum dot spin qubits, that makes use of transistor-based control circuits for control, on which surface code error correction can be implemented. Significant challenges to quantum dot control and qubit operation become clear. Furthermore, it motivated the investigation into the temperature dependence of qubits and the development of ”hot qubits”. By raising the operating temperature from the conventional milliKelvin regime, different cooling methods with vastly more cooling power become available. This allows for the integration of control electronics on the same chip.

Due to the high disorder at the Si/SiO_2 compared to Ge/SiGe and Si/SiGe, quantum dots defined in SiMOS are very small, and achieving sufficient control over single electrons has been a long-standing challenge. In Chapter 5 we demonstrated a high degree of control over the location of and coupling between quantum dots in SiMOS. We achieve a tunable tunnel coupling of up to tens of GHz between single electrons, marking an important step towards sufficient control for the operation of a large array of quantum dots. Further work should show that this amount of control is possible for more than two quantum dots, in a linear or 2D fashion, where all nearest neighbour couplings can be controlled.

To study the feasibility of hot qubits, we need to understand the mechanisms behind relaxation and decoherence, as well as their temperature dependence. The influence of temperature and magnetic field on the lifetime of a single-electron spin is investigated in Chapter 6. We demonstrate that T_1 can still be over a millisecond long at a temperature of one Kelvin, providing good prospects for achieving sufficient coherence times, also at higher temperatures. We develop a model based on spin-valley mixing and find that the spin lifetime T_1 can be further improved by operating at a low magnetic field with a sufficiently large valley splitting energy. Additionally, the weak temperature dependence of charge noise shows that qubit operation will only moderately be affected by an increase in temperature.

The combination of several achievements in Chapter 7 enables the demonstration of universal logic with qubits above 1 Kelvin, an important milestone for hot

qubits. We implement hot spin readout using Pauli spin blockade, and use electron spin resonance to drive controlled rotations for two qubits. We demonstrate universality by performing two-qubit randomized benchmarking, where we achieve a primitive gate fidelity of 86 %. The relatively low fidelity compared to the single-qubit experiments is attributed to decoherence during the time in which the qubits are idle, which is comparable to T_2^*. We analyse the effect of temperature of T_2^* and find a weak temperature dependence, which predicts a robustness against the increase in operating temperature necessary for hot qubits.

To improve the gate fidelity and to reduce the operation overhead of quantum algorithms, we develop multiple native two-qubit gates in Chapter 8. We implement entangling SWAP and CPHASE operations using novel adiabatic and diabatic composite sequences and gain an order magnitude in operating speed. These gates are usually mutually exclusive, but here we perform them on the same device in the presence of a finite Zeeman interaction. Especially in the NISQ era where hardware is very limited, gains in efficiency are critical to increase the possible practical algorithms that can be demonstrated.

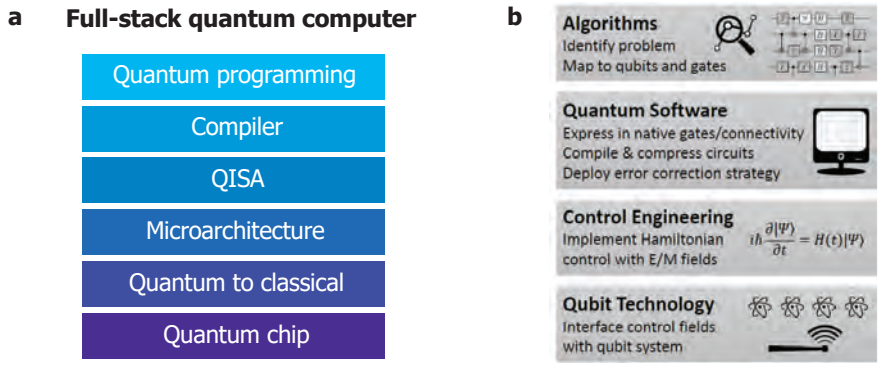

Figure 9.1: **Quantum computer layers. a** Illustration of the quantum computing full-stack. Figure adapted from [5]. **b** Levels of the quantum computer stack. Figure from [6].

9.2. Outlook: scalable quantum hardware

The work described in this thesis shows key developments for large-scale integration of silicon quantum dot spin qubits and great prospects for the feasibility of a silicon spin based quantum computer. Still, many multidisciplinary challenges remain before we can build a quantum computer, ranging from quantum information to quantum software compiling to quantum hardware. To map these challenges, it can be useful visualise a full-stack quantum computer. Figure 9.1a depicts a visualisation of the layers of such a system [5], where multiple modular layers connect the quantum chip all the way to the programming of applications. Figure 9.1b shows a distribution of the quantum computing stack into four main aspects [6]. Advances on all levels as well as tight integration between them will be required to realise their potential. Designing a general-purpose reconfigurable array will cost too much in

overhead, especially in the early days of large-scale quantum computing. Close collaboration between the developers of each stack layer will be necessary, hardware needs to be designed with applications in mind and vice versa.

The connectivity of the qubit array should be designed to anticipate the demands of the error correcting codes and algorithms that should be performed. Nevertheless, while exploring potential applications it is important for efficient algorithms to have a gate set with multiple two-qubit gates. For example, constructing a SWAP gate out of CPHASEs and CROTs would result in a gate time significantly slower than the sequence discussed in Chapter 8. A SWAP gate can be compiled using 3 consecutive CROT gates, which would give a total SWAP time of $\approx 2\,\mu s$. A SWAP gate compiled from the much faster CPHASE gate requires 11 primitive operations [7], which include 8 single-qubit gates and would therefore give an even larger overhead. Therefore, the composite exchange sequence can improve the gate time by more than one order of magnitude.

This way, computation time can be reduced to reduce the impact of noise and decoherence obtained. While there are many challenges on every part of the stack, the remainder of this outlook will focus on aspects of the essential quantum hardware chip.

9.2.1. Device and materials

Since the inception of the idea of a spin-based quantum computer, multiple proposals and discussions of architectures have been published, varying in detail and scope [8–13]. The general thought is that involvement from industry partners will be necessary to realize a large-scale system, and integrated control electronics will be required to overcome the interconnect bottleneck [5]. Industrial efforts are currently mostly focused on fin and nanowire based quantum dots [14–18], as these are more compatible with standard CMOS processes in contrast to the planar devices presented in this thesis. Quantum dots routinely form at the corners of nanowires, where the shape of the nanowire has a much larger effect than defects. The physics governing the spins in these quantum dots are mostly the same but there are notable differences in the confinement, which is more symmetric for nanowire quantum dots with wrap-around gates as there is less $\hat{z}$ confinement. Results from academia about the feasibility of these systems are necessary because of the slower industrial development cycle. A hybrid approach also exists, where a combination of optical and electron beam lithography is used for a high throughput of devices for mass standard semiconductor characterisations as well as cryogenic measurements [19]. Employing similar technology for Si/SiGe or Ge/SiGe is a challenge, as the formation of fins degrades the strain of the buried quantum well. Research on these sorts of devices is currently limited to manually deposited, chemically grown nanowires [20, 21] and patterned "hut" wires [22, 23]. Recently, foundry-made planar Si/SiGe devices were presented [24] which provide good prospects for adopting heterostructures in industrial quantum dot fabrication.

To compare the material quality of different group IV platforms, one can not simply use mobility data, as mobility is a bulk property that peaks at high carrier density and does not directly translate to quantum dot performance. The percolation den-

sity is a better metric that characterises disorder relevant for quantum dots [25]. Using either of these metrics, SiMOS performs way worse than the heterostructure platforms, giving rise to the small quantum dot size. Efforts are underway for multiplexed characterization of nano devices [26], and experiments to measure large numbers of single-electron transistors and quantum dots should give more insight. Control over single electrons in SiMOS has been demonstrated in Chapter 5, but this is not routinely achieved in all devices. The current gate pitch is just on the threshold of being sufficient for this degree of control and improvements in fabrication are required to routine achieve full control over tunnel coupling and detuning of single electrons. The exposure, development, deposition and liftoff processes need to be optimised to push the gate size to its lower limits. In the current process, the oxide thickness between gate layers is over-dimensioned because it used to be the main suspected point of leakage. A direct improvement could be made by finding the minimal oxide thickness where there is no gate to gate leakage in the required operating voltage range. A thinner oxide will also increase the lever arm and reduce charge noise from charge traps in the oxide. This additionally allows us to reduce the separation between the gates which further increases the degree of control over the quantum dots.

9.2.2. Operating temperature of quantum hardware

Picking a temperature at which the quantum computer will operate is mostly dependent on the cooling methods, where 0.3K for pumped ^{3}He and 1.2K for pumped ^{4}He are obvious contenders. While ^{3}He is rare, long-term production can be increased if there is demand [27]. To achieve the necessary raw cooling power, a pumped ^{3}He bath seems the most viable option. Proper packaging with high thermal conductance and a large surface area will be essential to get the dissipated heat out of the sample. Another gain can be made by thermally isolating the control electronics from the qubits, for example by having them connected only by superconducting leads. This ensures that heat generated in the control electronics does not reach the qubits. A final step could be made by designing a hybrid cooling system where the qubit part of the chip is cooled through a separate coldfinger, thermally isolated from the ^{3}He bath. This way, both the qubits and the control electronics can be kept at their optimal operating temperatures.

9.2.3. Readout of a qubit array

High fidelity readout is a critical aspect of large-scale quantum computation. Most experiments in this thesis made use of charge sensing readout: the measurement of the DC current through a single electron transistor nearby the quantum dots. The integration time (usually on the order of 30 μs - 1 ms) limits the bandwidth to tens of kHz. The readout time becomes the bottleneck to performing spin-qubit experiments and limits fidelity. Instead, we can measure the RF reflectometry response of the SET using high-frequency LC impedance matching techniques [28], which have enabled single-shot readout with only several microseconds of integration time, achieving a bandwidth above 100 MHz and a charge readout fidelity of >99.9% [29, 30]. Real-time feedback control can be implemented to maintain sen-

sitivity of the charge sensor [31]. For this purpose, a resonating circuit is connected to the source of the SET. To prevent RF leakage, careful sample design is required to ensure a well-matching contact resistance and low parasitic capacitance of the 2DEG [30]. Next to this "Ohmic-style" approach, there is the "split-gate style", where the RF signal is connected to the accumulation gate of the SET ("ST" for the devices in this thesis) which is capacitively coupled to the 2DEG [32]. The gate is split such that one part has a low parasitic capacitance and can be used for RF sensing while the other part is used as an independent lead gate that provides a high-impedance channel to the Ohmic contact to prevent leakage of the RF signal.

An alternative readout method uses the dispersive interaction of a quantum system with a resonator, where the complex impedance of (spin-dependent) tunneling between two quantum dots can be measured [33–38]. An integration time of 1 μs (1GHz bandwidth) with a fidelity of 99.7 % has been achieved. Here, the resonating circuit is connected to a quantum dot gate such that the RF response is conditional on the quantum dot charge state, which manifests as an additional quantum capacitance [39]. This removes the need for a charge sensor by directly coupling the qubit to a resonator, putting fewer constraints on the design when scaling up. On-chip integration of the resonator can further reduce losses. The current device design can be improved by fabricating an on-chip resonator using a superconducting material with a high kinetic inductance, such as NbTiN. This resonator can extend to the quantum dot area to function as one of the gates for optimal integration.

Performing readout of all qubits in a large array will require smart implementation of these readout circuits as it is not possible to have a dedicated resonator for every qubit. The typical footprint of a resonator is in the order of 100 $\times$ 100 μm, which can be reduced to less than a square μm by employing nanowire kinetic inductors [40]. Multiplexing resonating circuits [41] or shuttling the qubits to readout locations [42, 43] can further reduce the overhead. Once again, careful design and implementation are necessary, as the quality factor of these resonators suffers from the ever-present dielectric materials in CMOS manufacturing. Overcoming these challenges and integrating large-scale readout will be a major milestone for realising a large scale qubit array.

9.2.4. High-fidelity qubit control

Performing large-scale quantum operations requires advanced control methods, which start at the single-qubit level. When examining single-qubit gate quality, we can use the quality factor Q, the number of qubit operations available before coherence is lost (specifically defined as the Rabi decay time normalized by the manipulation time T_x) [44]. In Chapter 7 and Chapter 8, the relatively short T_2^* was the main limiting factor for qubit gate fidelities. This was most apparent for two-qubit gates, where the qubits spend a lot of time idling, and resulting randomized benchmarking fidelities were lower. Dephasing during idling is not covered by Q. This illustrates the importance of picking the right metrics for qubit fidelity, as well as designing optimal control pulses. Long operation times lead to long idling times, which in turn leads to qubit dephasing. We predict fidelities over 99.9% for new

implementations of two-qubit gates. Randomized benchmarking or quantum state tomography experiments should still be performed to confirm these numbers.

Pulse shaping and optimization techniques such as GRAPE [45] can be used to further improve gate fidelities by reducing crosstalk and to reduce sensitivity to inhomogeneities in the qubit resonance frequencies. A single spin does not directly couple to electric noise, but it can couple in via multiple mechanisms, and could turn out to be the largest bottleneck for qubit coherence. Electrical noise dominated nuclear noise on a device where the spin is coupled to a local micromagnet [44]. Further experiments are necessary to figure out whether the intrinsic SOI of electrons in silicon limits coherence for devices without micromagnets.

Electrical noise also couples into the exchange interaction. Full control over the tunnel coupling and detuning will enable operation at the charge symmetry point [46, 47], where the gate is first-order insensitive to charge noise. During the experiments of this thesis, the exchange interaction could be controlled only by detuning, between 0.5 and 15 MHz. Switching this coupling fully off during single-qubit rotations would increase the coherence of the idle qubit.

To progress towards the development of a large qubit array, the next experiments in SiMOS should extend three qubits in a triple quantum dot, to show the feasibility of operations to a linear array [48]. After achieving control over the tunnel coupling between the three electron spins, we can perform three-qubit experiments. We can use the third spin as an ancilla qubit for independent readout of the other two spins and study coherence and spin-to-charge conversion fidelities.

Globally addressing all qubits in a large array will be another major challenge. The currently used ESR and EDSR methods both require local structures, a transmission line and a micro magnet respectively, which would also require their own control lines. A potential solution was already anticipated in the 1998 Kane proposal for a silicon quantum computer, using a single global microwave control magnetic field [8]. A first step has been made by implementing a three-dimensional dielectric resonator on top of the chip, divided by a 200 μm sapphire spacer [49]. When using this approach the bandwidth of the driving frequency is limited by the resonator, so careful tuning of magnetic field and stark shift will be required to bring all qubits into the driving range. Automated procedures will be necessary to tune up a uniform qubit array. These procedures have been shown for charge occupancy and tunnel coupling [50–52] in a linear array. Hardware and software developments will be required to perform these corrections in real-time. Finally, to compensate for valley splitting and g-factor differences these procedures need to be extended to readout sequences, exchange interactions, qubit resonance frequencies and Rabi frequencies. Solving these challenges will allow for efficient qubit operations on a large array of spin qubits.

9.2.5. Fault tolerance

Qubit operation inherently has errors, and correcting these errors causes an overhead. Schemes for fault-tolerant quantum computing such as the surface code [53] combine several physical qubits to form a logical qubit that is more robust to errors. Alternatively, by combining multiple electron spins, different types of

qubits can be defined. For example, a quadrupolar exchange-only spin qubit consists of four electrons in three quantum dots and is highly robust against charge noise and nuclear spin dephasing [54]. Using more complex qubits does put more constraints on qubit operations, as exchange-only qubits require complex pulse sequences [55] and QUEX qubits require coupling to high frequency resonators. To optimally use an array of electron spins, a trade-off between the number and complexity of physical qubits will have to be made. The optimum will differ between the Noisy Intermediate-Scale Quantum (NISQ) era, where the goal is for quantum circuits of limited size to surpass the performance of classical computers, and the large-scale quantum computing era, where full fault tolerance is desired [56].

9.3. Impact of the quantum computing race

While we are still far from having realized a fully functional fault-tolerant universal quantum computer, we are now on the verge of stepping into the NISQ technology era. Here, systems of 50-100 qubits with noisy gates and no quantum error correction start performing tasks beyond the capabilities of classical computers [56]. In 2019, a team from Google claimed "Quantum Supremacy", performing a task that a classical computer can not do [57]. While the claim is disputed by their rival IBM [58], it is undeniable that an impressive milestone for quantum computing has been reached. Even if there turns out that to be a fundamental reason that a fault-tolerant quantum computer can not be built, this would still be a major scientific result, forcing the physics community to evaluate the correctness and shortcomings of quantum mechanics.

The promise of a world-changing application is having a profound impact on both the scientific and industrial community. There is an increasing influx of grants for research related to quantum computing and fundamental research is gaining commercial attention and support. The investment of industry partners like Intel into the fabrication of quantum dots forces them to reconsider which factors are important for device and material quality. Due to the complexities and trade-offs at each layer, it is critical that quantum computers are designed with the whole stack in mind, being aware of opportunities at the interfaces between the different levels. Critical for these developments is a high level of interdisciplinary collaboration between the physics, electrical engineering and computer science communities, jointly working toward a new era of computing.

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A

Appendix: methods

In this appendix, additional details of the experimental setup and methods and the device fabrication recipe are described.

A

A.1. Extended multi-platform fabrication recipe

Here we present the full fabrication process for each platform, specifically for the devices fabricated and studied in the main text.

In the case of SiMOS, fabrication begins on a natural silicon wafer, with 1 um of intrinsic silicon grown, followed by 100 nm epilayer ^{28}Si, and a 10 nm thermally grown oxide [1]. First, tungsten (W) markers are patterned, which are used to define implant windows via electron beam lithography (EBL). After exposure, phosphorus ions (P^+) at 6 keV are implanted to create highly negatively doped (n^{++}) regions in each die. An activation anneal is conducted in a rapid thermal processor (RTP) at 1000 ^oC for 30 seconds. A buffered hydro-fluoric (BHF) etch removes oxide in bond-pad areas, where Ti:Pt (5:55 nm) metallic contacts are deposited, creating ohmic contacts. A second layer of Ti:Pt markers are also written in this step. Next, a blanket Al_2O_3 ALD layer of 10 nm is grown across the entire sample. A small 20 x 20 μm^2 area is exposed and etched away in the vicinity of the quantum dot formation area. This improves dot stability (see above). Large rounded rectangular regions are then exposed in regions where wirebonding is expected, and 150 nm of SiN is sputtered. These create safer bondpads with which to bond to, reducing leakage and improving device yield. The SiMOS device presented in the work utilizes a three layer Ti:Pd gate stack. (3:17, 3:37, 3:37 nm). After each layer, the device is annealed in an RTP furnace for 15 minutes at 400 ^oC in forming gas, then a layer of ALD is grown at 7 nm thickness. Next, the qubit control layer is deposited. This can either be an Al or NbTiN antenna of 100 nm thickness for Electron spin resonance driving, or a Ti:Co micromagnet (5:195 nm) for Electron dipole spin resonance. The final step is an end of line anneal at 400 ^oC for 30 minutes in forming gas in an RTP.

The Si/SiGe 5 dot linear array begins on a natural silicon substrate. A linearly graded $Si_{1-x}Ge_x$ layer is deposited where x ranges from 0 to 0.3. A relaxed $Si_{0.7}Ge_{0.3}$ layer of 300 nm lies below the 10 nm ^{28}Si (800 ppm purity) quantum well which itself is separated from the 2 nm Si capping layer by a second 30 nm relaxed $Si_{0.7}Ge_{0.3}$ spacer layer. The initial marker layer is written using optical lithography and is formed by etching away the SiO_2. Next, a BHF dip removes native oxide selectively where ohmic contacts of Ti:Pt (5:55 nm) are evaporated, alongside a second set of markers. Gate stack fabrication of the device is almost identical to that of SiMOS. It is a 3-layer Ti:Pd stack of the same thicknesses, interlayer isolated via 7 nm of Al_2O_3. However, we do not employ a gate anneal between gate layers, despite this technically being possible within the context of thermal budget. For control, both striplines and micromagnets are available, however we prefer the electrical driving option since electron wave functions in Si/SiGe tend to be more mobile and hence EDSR provides a route to faster driving. We do not conduct an end of line anneal on SiGe devices.

	SiMOS	Si/SiGe	Ge/SiGe
Deposit marker layer 1 Material M	W markers E-beam Litho	Etched markers Optical Litho	-
Open implant windows at energy E fluence n	E = 6 keV n = $1x10^{16}$ cm^{-2}	E = 20 keV n = $5x10^{15}$ cm^{-2}	-
Anneal and activate at temperature T, time t in an RTP, nitrogen atmos- phere	T = 1000 C t = 30 s	T = 700 C t = 30 s	-
Define and write second marker layer Ti:Pt (5:55 nm)	✔	✔	✔
HF etch, imidiately before evaporation of Ohmics (material M) at thickness t	M = Ti:Pt t = 5:55 nm	M = Ti:Pt t = 5:55 nm	M = Al t = 30 nm
1 h vacuum anneal at 300 °C Gate Isolation ALD Al_2O_3 thickness t	t = 10 nm	t = 5 nm	t = 10 nm
Transene etch ALD in active window 50 °C	✔	-	-
Deposit gate stack in layers L at thicknessess t_L with gate anneal T = 400 °C, 15 mins in Forming gas. Interlayer ALD thickness t.	t_{scr} = 3:17 nm t_{plg} = 3:37 nm t_{bar} = 3:37 nm t_{ALD}= 7 nm Gate anneal ✔	t_{scr} = 3:17 nm t_{plg} = 3:37 nm t_{bar} = 3:37 nm t_{ALD}= 7 nm Gate anneal x	t_{bar} = 3:17 nm t_{plg} = 3:37 nm t_{ALD}= 10 nm Gate anneal x
Deposit qubit control layer Micromagnet or MW Antenna Thickness t, material M	Antenna M = Al t = 100 nm	Micromagnet M = Ti:Co t = 5:200 nm	-
End of Line Annneal T = 400 °C, 30 mins Forming gas.	✔	-	x

A

For the fabrication of the Ge/SiGe 2x2 array, we begin with a natural silicon substrate, upon which 1.4 μm of Ge and 900 nm of reverse graded $Si_{1-x}Ge_x$ where x ranges from 1 to 0.8 is grown. This lies below a 160 nm $Si_{0.2}Ge_{0.8}$ spacer layer, a 16 nm Ge quantum well under compressive strain, a second $Si_{0.2}Ge_{0.8}$ layer of 22 nm and finally a thin Si cap of 1 nm[2]. Ti:Pt EBL markers are then defined for future alignment. A short HF acid etch is conducted immediately before depositing 30 nm Al on regions where ohmic contact is desired. An advantage of the Ge/SiGe platform is the possibility of ohmic formation extremely close (within ≈ 100 nm) of the quantum dot. Devices are then placed under vacuum for 1 h at 300 ^{o}C causing Al to diffuse through the heterostructure into the quantum well forming ohmic contact. Atomic Layer Deposition is then performed covering the sample in a 10 nm Al_2O_3 blanket. The gate stack consists of two layers, barrier and plunger. The barrier layer is deposited at 20 nm total thickness utilizing the Ti:Pd stack (3:17 nm). The plunger layer is deposited at 40 nm total thickness (3:37 nm). No further processing is required as the large intrinsic spin-orbit interaction of holes in Ge/SiGe provides a native electric driving mechanism [3].

A.2. Experimental setup

The experiments in this thesis have been performed in Bluefors dry dilution refrigerators. In chapter 6 an LD400 model was used with a base temperature $T_{base} \approx$ 10 mK. In chapters 5, 7 and 8a LD-HE model was used with a base temperature of $T_{base} \approx 0.45$ K, operated at T = 1.1 K. The fridges operate based on the circulation of a ^{3}He/^{4}He mixture. The LD400 model has a mixing chamber with a dilution unit as the final temperature stage, where a phase separation between a concentrated ^{3}He phase (almost 100 % ^{3}He) and a dilute phase (about 6.6% ^{3}He and 93.4% ^{4}He). The flow of ^{3}He through the mixture provides the cooling power of the fridge.

Connected to the lowest temperature stage of the fridge (still plate for LDHE, mixing chamber plate for LD400) is a cold finger, which serves as a stable thermal anchor and to mount a printed circuit board (PCB) that hosts the sample. The sample is glued to the PCB and contact pads on the sample are wirebonded to leads on the PCB. The PCB supports 33 DC lines and 10 high frequency (hf) that are connected via a 50 pins flexible flat cable (FFC) and SMP connectors, respectively. The high frequency lines are connected via bias-tees with a cut-off frequency of $\approx$ 100 Hz.

From the PCB, the DC lines are filtered at the mixing chamber stage by a copper power filter, where high frequency signals (> 1 GHz) are attenuated via the eddy currents created in the copper grains. Additionally at this lowest temperature stage the signals go through a two-stage low-pass filter board with either 30 Hz for slow, low noise gates or 150 kHz for fast Ohmics. From this board the signals reach the room temperature matrix modules as twisted pairs, thermally anchored at every temperature stage. Voltages are applied using home-built battery-powered digital-to-analog-converters (DACs) over a voltage range of -4 to 4 V with a 16 bit resolution and a cut-off frequency of

We apply a source-drain bias voltage to the single-electron transistor and measure the current using an in-house built transimpedance (current-to-voltage) am-

plifier with a gain of 10^9 and a cut-off frequency of ≈ 50 kHz. This signal is further amplified, low-pass filtered and measured with a digitizer (analog-to-digital converter, ADC), either a spectrum 4421 with 16 bit resolution and a sampling rate of 250 MS/s or a Keysight M3102A with 14 bit resolution and a sampling rate of 500 MS/s.

The hf lines are used to apply pulse sequences to the gates and microwave signals to the stripline for spin driving. From the PCB to the mixing chamber plate, the pulse lines are connected with flexible graphite-coated cables with a cut-off frequency of ≈ 1 GHz while the microwave line uses a semi-rigid coax cable with a higher cut-off frequency. The signals run from the mixing chamber plate to room temperature through CuNi coax cables (or graphite-coated cables in case of the experiments in chapter 6). At each temperature stage, the signal can be attenuated. The amount of attenuation is a trade-off between noise reduction and the range of voltage that can be applied on the gates, where the gates usually have an attenuation of ≈ 15-25 dB while the microwave lines have ≈ 6-15 dB.

The pulse sequences used for the experiments in chapter 3 and 5 and 6 are generated by an arbitrary waveform generator (AWG) Tektronix AWG5014C with a 14 bit resolution and a sampling rate of 1.2 GS/s, connected to the control computer using an Ethernet cable. For the two-qubit experiments in chapter 7 and 8 we instead made use of two four-channel Keysight M3202A modules with 14 bit resolution and 1 GS/s. For the experiments in chapter. These AWG modules are mounted in a rack that also hosts the M3102A digitizer that allows for faster waveform uploads, and is addressed via PCI express. The Keysight system offers a much faster (<10 ms) waveform upload compared to the Tektronix (up to 100 s for complicated waveforms) offering a significant advantage for fast measurements. Furthermore, the M3102A digitizer has an integrated Field Programmable Gate Array (FPGA) that can be used to perform on-board averaging and live feedback in combination with the M3202A AWG's.

Microwave signals are generated by a Keysight PSG8267D vector source with a frequency output range of 250 KHz - 20 GHz at a power of up to 30 dBm, connected to the control computer using an Ethernet cable. ESR signals are generated using the internal IQ-mixer, driven by two output channels of the AWG. Multiple qubits can be addressed by setting the vector source to an intermediate frequency and IQ-mixing the signal with a (co)sine wave generated by two channels of the AWG.

Single-qubit randomized benchmarking

The single-qubit Clifford group C_1 consists of 24 rotations. We implement the group using X and Y rotations, using the primitive gates: $\{I, \pm X/2, \pm Y/2, \pm X, \pm Y\}$. On average one Clifford gate contains 1.875 primitive gates. We implement the gates using only frequencies f_1 and f_4 for Q1 and Q2 respectively. The complete list of gates is given in the following table:

The phase control needed to implement X and Y rotations is achieved using the internal I-Q mixer of the microwave source. The fidelity reported in Chapter 7 refers to the average fidelity of the gates in the generator group. All error bars are 1 standard deviation from the mean.

A

Single-qubit Cliffords
I
X
Y
Y, X
X/2, Y/2
X/2, -Y/2
-X/2, Y/2
-X/2, -Y/2
Y/2, X/2
Y/2, -X/2
-Y/2, X/2
-Y/2, -X/2
X/2
-X/2
Y/2
-Y/2
-X/2, Y/2, X/2
-X/2, -Y/2, X/2
X, Y/2
X, -Y/2
Y, X/2
Y, -X/2
X/2, Y/2, X/2
-X/2, Y/2, -X/2

Two-qubit randomized benchmarking

The two-qubit Clifford group C_2 consist of 11520 elements c_2 with properties $c_2^\dagger P c_2 \in \pm P$ where P are the Pauli operators. We generate the Clifford gates in our experiment using the set of conditional rotations in Fig. 7.4a where two subsequent conditional rotations implement a primitive gate. We compile the Clifford gates from the set of primitive gates together with virtual Z/2 gates on both qubits and search for combinations with the minimal amount of gates. The resulting average Clifford gate consists of 2.5694 primitive gates which are calibrated such that each conditional rotation takes exactly 330 ns, with the exchange interaction set to 3 MHz. To minimize cross-talk, the timing and the exchange interaction are chosen such that the off-resonant pulse is synchronized with the resonant pulse. All error bars are 1 standard deviation from the mean.

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Work hard, play hard, so they say. To blow off some steam from the hard work, I've enjoyed many great nights with **Erwin**, **Tineke**, **Martina**, **Henri**, **Rianne**, **Joran**, **Laurens** and **Rutger**. Thanks for all the great memories!

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Gertjan Eenink

May 4th 1993, Winterswijk, The Netherlands

2004–2011 **Secondary School VWO Natuur & Techniek**
Ulenhof College, Doetinchem

2011–2014 **Bachelor of Science in Electrical Engineering**
Universiteit Twente, Enschede

Undergraduate project in the group of prof. dr. ir. F.A. Zwanenburg
Investigating the effect of shell thickness and core diameter on electrical transport properties of Si-Ge shell-core nanowires

2014–2017 **Master of Science in Electrical Engineering**
Universiteit Twente, Enschede

Internship in the group of prof. A.S. Dzurak, UNSW, Sydney
Design of a CMOS architecture for a spin-based quantum computer

Graduate project in the group of prof. dr. ir. F.A. Zwanenburg
Highly tunable hole quantum dots in Si-Ge shell-core nanowires

2017–2021 **PhD in Experimental Physics**
Delft University of Technology

Doctoral research in the group of dr. ir. M. Veldhorst
Hot qubits in silicon for quantum computation

List of Publications

8. *High-fidelity two-qubit gates in silicon above one Kelvin*
L. Petit, M. Russ, **H.G.J. Eenink**, W.I.L. Lawrie, J.S. Clarke, L.M.K. Vandersypen and M.Veldhorst,
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L. Petit, **H.G.J. Eenink**, M. Russ, W.I.L. Lawrie, N.W. Hendrickx, S.G.J. Philips, J.S. Clarke, L.M.K. Vandersypen and M.Veldhorst,
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W.I.L. Lawrie, **H.G.J. Eenink**, N.W. Hendrickx, J.M. Boter, L. Petit, S.V. Amitonov, M. Lodari, B. Paquelet Wuetz, C. Volk, S.G.J. Philips, G. Droulers, N. Kalhor, F. Van Riggelen, D. Brousse, A. Sammak, L.M.K. Vandersypen, G. Scappucci and M. Veldhorst,
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5. *Tunable coupling and isolation of single electrons in silicon metal-oxide-semiconductor quantum dots*
H.G.J. Eenink[*], L. Petit[*], W.I.L. Lawrie, J.S. Clarke, L.M.K. Vandersypen and M. Veldhorst,
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[*] These authors contributed equally.

4. *Quantum transport properties of industrial $^{28}Si/^{28}SiO_2$*
D. Sabbagh, N. Thomas, J. Torres, R. Pillarisetty, P. Amin, H. C. George, K. Singh, A. Budrevich, M. Robinson, D. Merrill, L. Ross, J. Roberts, L. Lampert, L. Massa, S. V. Amitonov, J. M. Boter, G. Droulers, **H. G. J. Eenink**, M. van Hezel, D. Donelson, M. Veldhorst, L. M. K. Vandersypen, J. S. Clarke, and G. Scappucci, **Physical Review Applied 12**, 014013 (2019).

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