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Influence of Control and Limiter Schemes on Sequence-Domain Fault Models of Grid-Forming Inverter-Interfaced Distributed Generators

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***Abstract*—Unlike synchronous generators, the fault response of grid-forming (GFM) inverter-interfaced distributed generators (IIDGs) is notably governed by the selection of control and current limiting strategies rather than inherent physical traits. While recent research has focused on the sequence domain fault model of GFM IIDGs, a research gap exists in elucidating the influence of control and current limiting schemes on this model's characteristics. This article aims to fill this void by examining how different control and current limiting schemes influence the positive and negative sequence impedances in the phasor-domain fault model of GFM IIDGs. This investigation encompasses droop-based, virtual synchronous machine-based, and virtual oscillator-based reference generation controls alongside rotating and stationary reference-frame-based voltage controls. Furthermore, saturation-based, latching-based, circular and virtual impedance-based current limiting schemes are analyzed. To achieve this goal, a thorough numerical simulation study is conducted. Findings indicate that outer reference generation controls exhibit minimal impact. Conversely, the choice of voltage control and various current limiting schemes emerge as the predominant factors shaping the sequence models of GFM IIDGs. These analyses and results are instrumental in devising reliable protection strategies within inverter-based grids, as a comprehensive understanding of electrical elements in the sequence domain is imperative for effective protective measures.**

***Index Terms*—Current limiters, fault analysis, grid-forming inverters, sequence domain modeling, voltage controllers.**

I. Introduction

POWER systems are subjected to major changes in which large synchronous machines (SMs) are replaced by smaller inverter-interfaced distributed generators (IIDGs) utilizing voltage source inverter (VSI) topology. While most IIDGs currently operate as grid-following (GFL) units, various grid-forming (GFM) control strategies have emerged to equip IIDGs with characteristics resembling SMs [1], [2]. GFM IIDGs, featuring droop, virtual synchronous machine (VSM), and virtual oscillator (VOC)-based characteristics, swiftly adjust local voltage and frequency during contingencies [3], [4]. Leveraging IIDGs for primary frequency control offers significant advantages, particularly in low-inertia networks, by rapidly mitigating frequency fluctuations before resorting to load shedding.

GFM IIDGs are highly sensitive to inevitable grid disturbances and are prone to failures during grid faults, as they typically withstand a maximum current of only about 1.2–2.0 per unit [5]. Traditionally, IIDGs could be tripped to prevent damage from overcurrent. However, during faults, GFM IIDGs must stay connected to the grid [6], following the low-voltage ride-through (LVRT) rules outlined in emerging regulatory standards, including the IEEE Standard 1547 [7]. Implementing different current limiting functions and the *voltage controller* schemes with due consideration for transient stability is essential [8]. Representing any piece of electrical equipment in the sequence domain is vital for analyzing power flow and short-circuit events. While power flow analysis requires only positive-sequence models, short-circuit analysis necessitates the inclusion of zero-sequence, positive-sequence, and negative-sequence models. However, the diversification of control schemes adopted by GFM IIDGs leads to the complexity of determining a suitable model under faults. Expanding traditional fault analysis techniques to include IIDGs involves representing GFL IIDGs as ideal current sources and GFM IIDGs as ideal voltage sources during fault periods, as described in [9], [10]. However, it is noted that the models under faults lack accuracy during the sub-transient and transient periods [11]. To better reflect the transient response of IIDGs, the dynamic characteristic of control systems needs to be considered [12]. Several studies have attempted to investigate the fault response of GFM IIDGs [13], [14], along with developing corresponding fault models [15], [16]. Reference [17] explores the effects of various current limiters on the dynamics of GFM IIDG control systems. Models proposed in [18] assume normal operating conditions, where IIDG voltages remain nominal and

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balanced, rendering them unsuitable for fault analysis. Another study [19] proposes per-phase IIDG models for fault scenarios, yet these models lack completeness as they do not consider the sequence domain. Furthermore, a study by [20], [21] introduces a sequence domain model for GFM IIDGs alongside a specific control and fault limiter approach to characterize sequence impedances. Nonetheless, the applicability of these findings is limited for GFM IIDGs employing different controllers and current limiters.

Based on a comprehensive analysis of fault response studies conducted on GFM IIDGs, several recurring observations become apparent: i) the fault response of GFM IIDGs is notably influenced by the selection of control schemes and methods for current limitation, rather than their intrinsic physical characteristics, ii) these control schemes and fault-limiting methods showcase effective performance during balanced operations and ample fault ride-through during symmetric faults, iii) however, during unbalanced operation, particularly in asymmetrical fault scenarios, the utilization of diverse control and fault limiter schemes by GFM IIDGs introduces heightened complexity in comprehending their behavior. However, to the best of the authors' knowledge, there exists a gap in research regarding the assessment of how the control and limiter schemes of GFM IIDGs affect the parameters of the sequence domain fault model. This article seeks to address this void by providing the following contributions:

- To delve deeper into the response of GFM IIDGs to unbalanced faults, the analysis objectives are categorized into three main groups: i) reference generation control, ii) voltage control and iii) current limiting schemes.
- To encompass a wide range of conventional scenarios, this paper selects and analyzes three of the most commonly used reference generation controls. These include P-f/Q-V droop control, virtual inertia-based VSM control, and Andronov-Hopf-based VOC control.
- For the voltage control scheme, this study examines two of the most widely used voltage control methods. These include the nested and multi-loop outer-voltage-inner-current control structure designed in dq-domain and $\alpha\beta$-domain.[1]
- This paper analyzes a comprehensive set of current limiting schemes, including saturation-based methods, latching-based methods prioritizing the d and q axes, circular limiter and virtual impedance-based limiting schemes.
- This paper provides a detailed examination for the sequence domain model of GFM IIDG to assess the influence of all the above-mentioned control and current limiting schemes on its characteristics. This investigation aims to pinpoint the primary factors, within the control and current limiting schemes, that affect the unbalanced fault behavior of GFM IIDGs.

[1]IEEE Standard 2800 [22] specifies requirements for the sequence component current injection capability of inverters during fault conditions. While sequence component-based dq-domain control is recommended in several existing studies [23], [24], these control strategies are not addressed and are beyond the scope of this work.

To achieve that, a comprehensive electromagnetic transient simulation study with systematic replication of a variety of unbalanced conditions is conducted, encompassing detailed modeling of these diverse controls and current limiting strategies typically utilized in GFM IIDGs. The possible applications of this comprehensive investigation are:

- The outcomes of this work can be used to provide valuable information on the impact of control and current limiting schemes on the sequence domain fault model of GFM IIDG for integration into fault analysis software or modules utilized by protection engineers.
- The insights obtained from this work can be instrumental in facilitating the design of necessary modifications or novel protection schemes tailored for GFM IIDG-dominant power system networks.

This article is organized as follows. In Section II, the state-of-the-art conventional control and limiter schemes of GFM-IIDGs are presented. In Section III, various control and limiter schemes, along with the sequence domain model of GFM IIDGs under study, are described. In Section IV, the analysis of the impact of the control and limiter schemes on the fault model during unbalanced conditions is investigated using a simulation study. Finally, Section V provides conclusions.

II. State-of-The-Art on Conventional Control and Limiter Schemes for GFM IIDGs

A. Control System of GFM IIDGs

GFM IIDGs are typically linked to the power system network at point-of-common-coupling (PCC) via first-order LC filters to mitigate high-frequency switching effects. The voltage-loop controller forms the core of the control structure, enabling GFM IIDGs to operate as controllable voltage sources at the point of connection with the network.

1) Scheme for Voltage Loop Control: Designing the voltage controller for GFM IIDG is a multifaceted task involving: 1) ensuring reference tracking, disturbance rejection, and harmonic compensation capability amidst diverse linear and non-linear loads, 2) addressing dynamic variations of the output load current to enhance dynamic response, and 3) accommodating the unknown nature of the GFM IIDG's output loading, which can significantly impact system behavior. Various types of control and their advancements in outer-voltage-inner-current control schemes for GFM IIDGs are proposed in the state-of-the-art while assuming the loading of the network is balanced [25]. Literature suggests two broad classifications of the voltage controller design, such as controller design in $\alpha\beta$-domain and controller design in dq-domain. Due to ease in the controller synthesis process and implementation, controllers designed in dq-domain are more commonly used than controllers designed in $\alpha\beta$-domain. Irrespective of the design domain, numerous voltage control strategies have been proposed in the literature during past decades for the GFM IIDG system [25].

2) Schemes for Reference Generation Control: The reference generation logic of a GFM IIDG, such as battery-based uninterrupted power supply (UPS), is employed based on the

following tasks: 1) sharing active and reactive load demand power of the network among multiple GFM IIDGs, and 2) controlling and regulating network voltage and frequency under recommended limits. In [25], different control approaches for GFM-IIDGs are discussed. *Droop-law*-based reference generation controls are most common and widely accepted both in industry and academia [3]. The advantage of the *droop-law*-based control is its capability of autonomy and communication-less power-sharing operation and its easy implementation. There are many non-droop-based voltage reference generation logics available in the literature based on the *leader-follower* method [26], *virtual oscillator control* (VOC)-based GFM control [27], *virtual synchronous machine* (VSM)-based GFM control [28].

B. Limiter System of GFM IIDGs

The limiter system maintains the uninterrupted operation of GFM IIDG systems during network faults, preventing semiconductor damage. It employs a control strategy with limiting functionalities to restrict fault current during disturbances. After fault clearance, the IIDG smoothly resumes normal operation, which is crucial for transient stability. Various current and voltage limiting strategies have been proposed in the literature for GFM IIDG systems [29]. These systems often use instantaneous saturation limits to prevent current or voltage signals from surpassing set thresholds. This approach is simple to implement and effectively controls the signals within a controller. Another approach involves latched limits, which measure the signal and adjust it to a predetermined limit when it surpasses a specific threshold [30]. Anti-windup protection, crucial for controllers in GFM IIDGs constrained by limiting circuits [31], prevents integrator wind-up and ensures the fault recovery capability of GFM-IIDG [32]. The widely explored virtual impedance-based current limiting method restricts fault currents by adjusting the voltage-reference command via a complex-valued fault-current-dependent feedforward term in the voltage-control loop [33]. A dynamic damping approach using virtual impedance control has been suggested [34], although these studies predominantly concentrate on balanced three-phase faults in GFM IIDGs [35].

III. Control and Limiter Schemes of GFM IIDGs and Sequence Model Under Study for Analysis

The fault response of GFM IIDGs is primarily influenced by control systems and current limiting methods rather than physical parameters [13]. While control schemes in Section II come through in balanced and symmetrical fault scenarios, they face challenges during unbalanced and asymmetrical faults due to diverse control strategies and fault-limiting schemes [11]. This complexity warrants empirical investigation using time-domain electromagnetic transient (EMT) simulations.

A. Control and Limiter Schemes of GFM IIDGs Under Study

For the EMT simulation study of GFM IIDG, the following types of voltage reference generation controllers, fault limiters with voltage-loop controllers are selected:

1) Schemes of Voltage Loop Controller: The following voltage loop controllers are studied here:

$[\mathcal{C}_1]$ $\underline{\mathrm{dq-domain\ Voltage\ Controller}}$: The conventional outer-voltage-inner-current controller operates within the synchronous reference frame (i.e., dq-domain) architecture, depicted in the top-left of Table I. In the inner-current controller, $i^{\mathrm{d}}_{\mathrm{L,ref}}$ and $i^{\mathrm{q}}_{\mathrm{L,ref}}$ serve as reference signals tracked by $i^{\mathrm{d}}_{\mathrm{L}}$ and $i^{\mathrm{q}}_{\mathrm{L}}$ outputs, respectively. A proportional-integral (PI) compensator is utilized, with parameters $k^{\mathrm{p}}_{\mathrm{c}} = L_{\mathrm{f}}/\tau_{\mathrm{c}}$ and $k^{\mathrm{i}}_{\mathrm{c}} = R_{\mathrm{f}}/\tau_{\mathrm{c}}$ selected for a desired time constant τ_{c}, typically in the range of 0.5-2 ms [36]. Feed-forward voltage signals, $v^{\mathrm{d}}_{\mathrm{c}}$, $v^{\mathrm{q}}_{\mathrm{c}}$, and cross-coupling signals $-\omega_{\mathrm{N}} L_{\mathrm{f}} i^{\mathrm{q}}_{\mathrm{L}}$ and $\omega_{\mathrm{N}} L_{\mathrm{f}} i^{\mathrm{d}}_{\mathrm{L}}$ enhance disturbance rejection capability, where ω_{N} denotes the nominal angular frequency in rad/s. In the outer-voltage controller, $v^{\mathrm{d}}_{\mathrm{C,ref}}$ and $v^{\mathrm{q}}_{\mathrm{C,ref}}$ are the reference signals tracked by $v^{\mathrm{d}}_{\mathrm{C}}$ and $v^{\mathrm{q}}_{\mathrm{C}}$, respectively. A PI compensator enables reference tracking, with parameters ($k^{\mathrm{p}}_{\mathrm{v}}$ and $k^{\mathrm{i}}_{\mathrm{v}}$) determined based on the *symmetrical optimum* method [36] to achieve desired phase margin and gain cross-over frequency. Current feed-forward signals, $i^{\mathrm{d}}_{\mathrm{O}}$, $i^{\mathrm{q}}_{\mathrm{O}}$, and cross-coupling signals $-\omega_{\mathrm{N}} C_{\mathrm{f}} v^{\mathrm{q}}_{\mathrm{C}}$, $\omega_{\mathrm{N}} C_{\mathrm{f}} v^{\mathrm{d}}_{\mathrm{C}}$ bolster disturbance rejection capability for the voltage control loop.

$[\mathcal{C}_2]$ $\underline{\alpha\beta-\mathrm{domain\ Voltage\ Controller}}$: The conventional outer-voltage-inner-current controller operates within the stationary reference frame (i.e., $\alpha\beta$-domain) architecture, illustrated in the top-right of Table I. In the inner-current controller, $i^{\alpha}_{\mathrm{L,ref}}$ and $i^{\beta}_{\mathrm{L,ref}}$ serve as reference signals for the outputs, i^{α}_{L} and i^{β}_{L}, respectively. The similar PI compensator is used here for ease in synthesis of the controller and time-scale separation of the outer voltage loop and the inner current loop [37], [38]. Feed-forward voltage signals, v^{α}_{c} and v^{β}_{c}, enhance disturbance rejection capability. Notably, in the stationary frame control, there are no cross-coupling feed-forward signals. In the outer-voltage controller, $v^{\alpha}_{\mathrm{C,ref}}$ and $v^{\beta}_{\mathrm{C,ref}}$ are the reference signals tracked by v^{α}_{C} and v^{β}_{C}, respectively. A PR controller with two gain parameters, $k^{\mathrm{p}}_{\mathrm{v}}$ and $k^{\mathrm{r}}_{\mathrm{v}}$, is utilized. For a desired phase margin and gain cross-over frequency, parameters of the voltage controller ($k^{\mathrm{p}}_{\mathrm{v}}$ and $k^{\mathrm{r}}_{\mathrm{v}}$) can be designed [36]. Current feed-forward signals, i^{α}_{O} and i^{β}_{O}, bolster disturbance rejection capability for the voltage control loop.

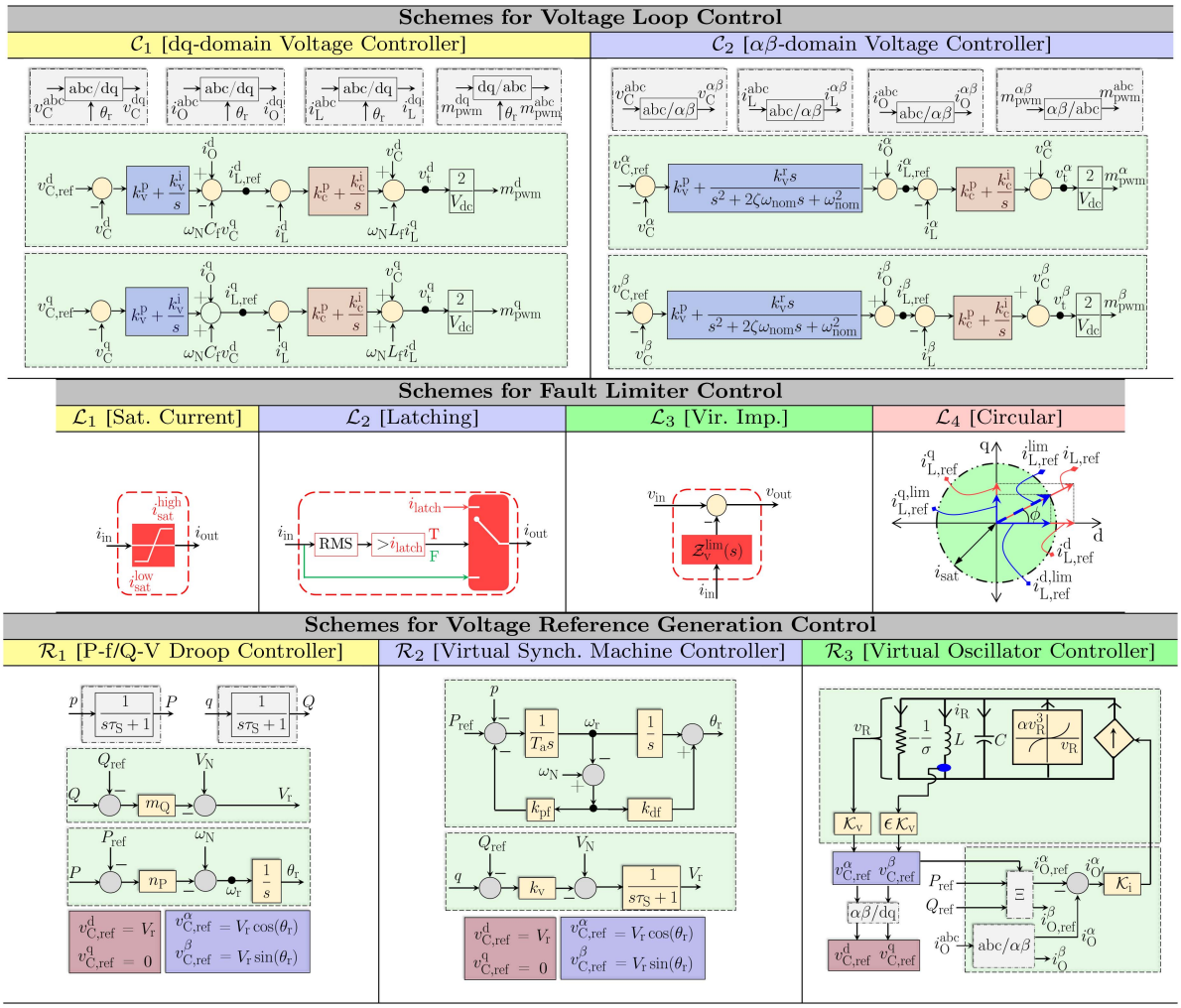
2) Schemes of Fault Limiter Control: The following fault limiters are studied here:

$[\mathcal{L}_1]$ $\underline{\mathrm{Inst.\ Current\ Saturation\ Limiter}}$: The instantaneous current saturation limiter [31] is a hard limit on the inductor current references, $i^{\mathrm{d}}_{\mathrm{L,ref}}$ and $i^{\mathrm{q}}_{\mathrm{L,ref}}$, for $\mathcal{C}_1$ of Table I. Whereas, for $\mathcal{C}_2$ of Table I, the hard limit is on $i^{\alpha}_{\mathrm{L,ref}}$, and $i^{\beta}_{\mathrm{L,ref}}$. The d-axis priority-based instantaneous current saturation limiter for $\mathcal{C}_1$ follows the following equations [39]:

$$\left|i^{\mathrm{d,lim}}_{\mathrm{L,ref}}\right| = \mathtt{min}\left(i_{\mathrm{sat}}, \left|i^{\mathrm{d}}_{\mathrm{L,ref}}\right|\right), \tag{1}$$

$$\left|i^{\mathrm{q,lim}}_{\mathrm{L,ref}}\right| = \mathtt{min}\left(\sqrt{i^2_{\mathrm{sat}} - \left(i^{\mathrm{d,lim}}_{\mathrm{L,ref}}\right)^2}, \left|i^{\mathrm{q}}_{\mathrm{L,ref}}\right|\right). \tag{2}$$

TABLE I
SCHEMES FOR VOLTAGE LOOP CONTROL, FAULT CURRENT LIMITER, AND VOLTAGE REFERENCE GENERATION CONTROL UNDER STUDY



The q-axis priority-based instantaneous current saturation limiter for $\mathcal{C}_1$ follows the following equations [40]:

$$\left|i_{\mathrm{L,ref}}^{\mathrm{d,lim}}\right| = \mathtt{min}\left(\sqrt{i_{\mathrm{sat}}^2 - \left(i_{\mathrm{L,ref}}^{\mathrm{q,lim}}\right)^2}, \left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|\right), \tag{3}$$

$$\left|i_{\mathrm{L,ref}}^{\mathrm{q,lim}}\right| = \mathtt{min}\left(i_{\mathrm{sat}}, \left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|\right). \tag{4}$$

An instantaneous hard current saturation limiter will clip the peak of the sinusoidal signal in case of $\mathcal{C}_2$. This will result in distorted output currents. To address this problem, a circular current saturation limiter is usually implemented for $\mathcal{C}_2$ with the following equations [34], [35]:

$$i_{\mathrm{L,ref}}^{\alpha\beta,\mathrm{lim}} = \begin{cases} i_{\mathrm{L,ref}}^{\alpha\beta}, & \text{if } \sqrt{(i_{\mathrm{L,ref}}^{\alpha})^2 + (i_{\mathrm{L,ref}}^{\beta})^2} \leq i_{\mathrm{sat}}, \\ i_{\mathrm{L,ref}}^{\alpha\beta} \dfrac{i_{\mathrm{sat}}}{\sqrt{(i_{\mathrm{L,ref}}^{\alpha})^2 + (i_{\mathrm{L,ref}}^{\beta})^2}}, & \text{otherwise}, \end{cases} \tag{5}$$

where i_{sat} is usually selected as 1.2-1.5 pu of the nominal current of the IIDG. An instantaneous current saturation limiter is relatively easy to implement. However, it leads to current distortion in case of $\mathcal{C}_2$ during asymmetrical faults because the current reference, $i_{\mathrm{L,ref}}^{\alpha\beta}$, describes an ellipse in the stationary plane to which a circular instantaneous limit is applied.

[$\mathcal{L}_2$] Latching Current Limiter: Latching current limiter allows a mode change in the current values in which the IIDG control switches to a predefined inductor fault current reference, i_{latch}, instead of the reference current signals [34], [35]. It is held at that value until the inductor current reference magnitude drops below a reset threshold, i_{reset}. In the dq frame, the limiter follows the following equations [41]:

$$i_{\mathrm{L,ref}}^{\mathrm{d,lim}}, i_{\mathrm{L,ref}}^{\mathrm{q,lim}} = \begin{cases} i_{\mathrm{L,ref}}^{\mathrm{d,sat}}, i_{\mathrm{L,ref}}^{\mathrm{q,sat}} \text{ if } i_{\mathrm{L,ref}} \geq i_{\mathrm{sat}}, \\ i_{\mathrm{L,ref}}^{\mathrm{d}}, i_{\mathrm{L,ref}}^{\mathrm{q}} \text{ if } i_{\mathrm{L,ref}} \leq i_{\mathrm{latch}}, \end{cases} \tag{6}$$

where, $i_{\mathrm{L,ref}} = \sqrt{(i_{\mathrm{L,ref}}^{\mathrm{d}})^2 + (i_{\mathrm{L,ref}}^{\mathrm{q}})^2}$. Also, the selection of $i_{\mathrm{L,ref}}^{\mathrm{d,sat}}$ and $i_{\mathrm{L,ref}}^{\mathrm{q,sat}}$ should satisfy $\sqrt{(i_{\mathrm{L,ref}}^{\mathrm{d,sat}})^2 + (i_{\mathrm{L,ref}}^{\mathrm{q,sat}})^2} = i_{\mathrm{sat}}$. In case of the d-axis priority-based latching for $\mathcal{C}_1$, $i_{\mathrm{L,ref}}^{\mathrm{d,sat}}$ and $i_{\mathrm{L,ref}}^{\mathrm{q,sat}}$ are selected as follows [42]:

$$i_{\mathrm{L,ref}}^{\mathrm{d,sat}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{d}}}{\left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|} \times \mathtt{min}\left(\left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|, i_{\mathrm{sat}}\right), \tag{7}$$

$$i_{\mathrm{L,ref}}^{\mathrm{q,sat}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{q}}}{\left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|} \times \mathtt{min}\left(\left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|, \sqrt{(i_{\mathrm{sat}})^2 - \left(i_{\mathrm{L,ref}}^{\mathrm{d,sat}}\right)^2}\right). \tag{8}$$

In case of the q-axis priority-based latching for $\mathcal{C}_1$, $i_{\mathrm{L,ref}}^{\mathrm{d,sat}}$ and $i_{\mathrm{L,ref}}^{\mathrm{q,sat}}$ are selected as follows [43]:

$$i_{\mathrm{L,ref}}^{\mathrm{d,sat}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{d}}}{\left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|} \times \mathtt{min}\left(\left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|, \sqrt{(i_{\mathrm{sat}})^2 - \left(i_{\mathrm{L,ref}}^{\mathrm{q,sat}}\right)^2}\right), \tag{9}$$

$$i_{\mathrm{L,ref}}^{\mathrm{q,sat}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{q}}}{\left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|} \times \mathtt{min}\left(\left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|, i_{\mathrm{sat}}\right). \tag{10}$$

In case of the angle priority-based latching for $\mathcal{C}_1$, $i_{\mathrm{L,ref}}^{\mathrm{d,sat}}$ and $i_{\mathrm{L,ref}}^{\mathrm{q,sat}}$ are selected as follows [44]:

$$i_{\mathrm{L,ref}}^{\mathrm{d,sat}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{d}}}{\left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|} \times \mathtt{min}\left(\left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right|, \left|i_{\mathrm{L,ref}}^{\mathrm{d}}\right| \times \frac{i_{\mathrm{sat}}}{i_{\mathrm{L,ref}}}\right), \tag{11}$$

$$i_{\mathrm{L,ref}}^{\mathrm{q,sat}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{q}}}{\left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|} \times \mathtt{min}\left(\left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right|, \left|i_{\mathrm{L,ref}}^{\mathrm{q}}\right| \times \frac{i_{\mathrm{sat}}}{i_{\mathrm{L,ref}}}\right). \tag{12}$$

Latching equation for α-β domain control for $\mathcal{C}_2$ is selected as follows [45]:

$$i_{\mathrm{L,ref}}^{\alpha\beta,\mathrm{lim}} = \begin{cases} i_{\mathrm{L,ref}}^{\alpha\beta} \frac{i_{\mathrm{sat}}}{i_{\mathrm{L,ref}}}, & \text{if } i_{\mathrm{L,ref}} \geq i_{\mathrm{sat}}, \\ i_{\mathrm{L,ref}}^{\alpha\beta}, & \text{if } i_{\mathrm{L,ref}} \leq i_{\mathrm{latch}}, \end{cases} \tag{13}$$

where, $i_{\mathrm{L,ref}} = \sqrt{(i_{\mathrm{L,ref}}^{\alpha})^2 + (i_{\mathrm{L,ref}}^{\beta})^2}$. To prevent limit cycle behavior of the inserted non-linearity, i_{reset} is selected to be below i_{sat} yet above the current magnitude at rated power operation at the lowest nominal voltage. [$\mathcal{L}_3$] Virtual Impedance Limiter: Unlike $\mathcal{L}_1$ and $\mathcal{L}_2$, the virtual impedance-based limiter is applied to voltage reference signals rather than inductor current reference signals and is primarily used for GFM IIDGs. This is achieved by integrating a complex-valued fault-current-dependent feed-forward term into the voltage-control loop. The expressions for the virtual resistance, R_{vir}, and virtual inductance, L_{vir}, are as follows:

$$R_{\mathrm{vir}} = \begin{cases} k_{\mathrm{p}}^{R_{\mathrm{vir}}} \left[\mathtt{RMS}(i_{\mathrm{L}}) - i_{\mathrm{sat}}\right], & \text{if } \mathtt{RMS}(i_{\mathrm{L}}) - i_{\mathrm{sat}} \geq 0, \\ 0 \text{ otherwise}, \end{cases}$$

$$\omega_{\mathrm{N}} L_{\mathrm{vir}} = X_{\mathrm{vir}} = \sigma_{\mathrm{X/R}} R_{\mathrm{vir}}. \tag{14}$$

Here, $\mathtt{RMS}(i_{\mathrm{L}}) := \sqrt{(i_{\mathrm{L}}^{\mathrm{d}})^2 + (i_{\mathrm{L}}^{\mathrm{q}})^2}$ for $\mathcal{C}_1$, and $\mathtt{RMS}(i_{\mathrm{L}}) := \sqrt{(i_{\mathrm{L}}^{\alpha})^2 + (i_{\mathrm{L}}^{\beta})^2}$ for $\mathcal{C}_2$. $k_{\mathrm{p}}^{R_{\mathrm{vir}}}$, and $\sigma_{\mathrm{X/R}}$ are the virtual impedance proportional gain and X/R ratio of the virtual impedance, respectively. The parameter $k_{\mathrm{p}}^{R_{\mathrm{vir}}}$ is tuned to limit the current magnitude to a suitable level during overcurrent in the steady state, while $\sigma_{\mathrm{X/R}}$ ensures good system dynamics during the overcurrent. When the virtual impedance-based limiter is activated, the following equations are followed in the voltage control loop for $\mathcal{C}_1$ [33]:

$$v_{\mathrm{C,ref}}^{\mathrm{d,lim}} = v_{\mathrm{C,ref}}^{\mathrm{d}} - R_{\mathrm{vir}} i_{\mathrm{O}}^{\mathrm{d}} + X_{\mathrm{vir}} i_{\mathrm{O}}^{\mathrm{q}}, \tag{15}$$

$$v_{\mathrm{C,ref}}^{\mathrm{q,lim}} = v_{\mathrm{C,ref}}^{\mathrm{q}} - R_{\mathrm{vir}} i_{\mathrm{O}}^{\mathrm{q}} - X_{\mathrm{vir}} i_{\mathrm{O}}^{\mathrm{d}}. \tag{16}$$

Similarly, when the virtual impedance-based limiter is activated, the following equations are followed in the voltage control loop for $\mathcal{C}_2$ [34], [35]:

$$v_{\mathrm{C,ref}}^{\alpha,\mathrm{lim}} = v_{\mathrm{C,ref}}^{\alpha} - (R_{\mathrm{vir}} + sL_{\mathrm{vir}})\, i_{\mathrm{O}}^{\alpha}, \tag{17}$$

$$v_{\mathrm{C,ref}}^{\alpha,\mathrm{lim}} = v_{\mathrm{C,ref}}^{\beta} - (R_{\mathrm{vir}} + sL_{\mathrm{vir}})\, i_{\mathrm{O}}^{\beta}. \tag{18}$$

[$\mathcal{L}_4$] Circular Magnitude Limiter: The circular limiter scheme is a magnitude limiting logic with angle priority of the inductor current of the IIDG [45]. The logic schematic is shown in Table I. It limits the magnitude of the current, $i_{\mathrm{L,ref}}$, inside the circle of radius i_{sat} by limiting it to $i_{\mathrm{L,ref}}^{\mathrm{lim}}$ in such a way that the pre-fault angle is maintained. The limiter logic follows the following equations:

$$i_{\mathrm{L,ref}}^{\mathrm{lim}} = \begin{cases} i_{\mathrm{sat}}, \frac{i_{\mathrm{L,ref}}^{\mathrm{q}}}{i_{\mathrm{L,ref}}^{\mathrm{d}}} = \frac{i_{\mathrm{L,ref}}^{\mathrm{q,lim}}}{i_{\mathrm{L,ref}}^{\mathrm{d,lim}}} = \phi & \text{if } i_{\mathrm{L,ref}} > i_{\mathrm{sat}}, \\ i_{\mathrm{L,ref}}, & \text{if } i_{\mathrm{L,ref}} \leq i_{\mathrm{sat}}, \end{cases} \tag{19}$$

where, $i_{\mathrm{L,ref}} = \sqrt{(i_{\mathrm{L,ref}}^{\mathrm{d}})^2 + (i_{\mathrm{L,ref}}^{\mathrm{q}})^2}$ and $i_{\mathrm{L,ref}}^{\mathrm{lim}} = \sqrt{(i_{\mathrm{L,ref}}^{\mathrm{d,lim}})^2 + (i_{\mathrm{L,ref}}^{\mathrm{q,lim}})^2}$. Note that the limiter scheme in $\alpha\beta$ domain is inherently circular in nature because of the sinusoidal nature of the current signals unlike in dq domain. Also it is important to mention here that the magnitude-based angle-priority in circular limiter is a generic version of d/q-axis priority-based limiter. In all three cases, the magnitude is still maintained under the circle of radius i_{sat}, but the decomposition of d-axis and q-axis is different in these cases.

3) Schemes of Voltage Reference Generation Control: The following reference generation controls are studied here:

[$\mathcal{R}_1$] P $\sim$ f/Q $\sim$ V Droop Controller: Droop control involves the use of active and reactive power as control variables, where the droop gains determine the steady-state power sharing among inverters. Here, the $P \sim f$ and $Q \sim V$ droop controls are treated as proportional controllers with coefficients n_{P} and m_{Q}, respectively. The error signals $e_{\mathrm{P}} := P_{\mathrm{ref}} - P$ and $e_{\mathrm{Q}} := Q_{\mathrm{ref}} - Q$ are defined, where P and Q are the control variables and P_{ref} and Q_{ref} are the references. Initially, $v_{\mathrm{C}}^{\mathrm{abc}}$ and $i_{\mathrm{O}}^{\mathrm{abc}}$ are used to determine instantaneous active power, p, and reactive power, q, using the following equations:

$$p = \left[v_{\mathrm{C}}^{\mathrm{a}} i_{\mathrm{O}}^{\mathrm{a}} + v_{\mathrm{C}}^{\mathrm{b}} i_{\mathrm{O}}^{\mathrm{b}} + v_{\mathrm{C}}^{\mathrm{c}} i_{\mathrm{O}}^{\mathrm{c}}\right], \tag{20}$$

$$q = \frac{1}{\sqrt{3}}\left[i_{\mathrm{O}}^{\mathrm{a}}\left(v_{\mathrm{C}}^{\mathrm{b}} - v_{\mathrm{C}}^{\mathrm{c}}\right) + i_{\mathrm{O}}^{\mathrm{b}}\left(v_{\mathrm{C}}^{\mathrm{c}} - v_{\mathrm{C}}^{\mathrm{a}}\right) + i_{\mathrm{O}}^{\mathrm{c}}\left(v_{\mathrm{C}}^{\mathrm{a}} - v_{\mathrm{C}}^{\mathrm{b}}\right)\right]. \tag{21}$$

p and q are passed through low-pass filters with the time constant, $\tau_{\mathrm{S}} \in \mathbb{R}_{>0}$, to obtain P and Q as described by

$$P = \left[1/\left(\tau_{\mathrm{S}} s + 1\right)\right] p,\ Q = \left[1/\left(\tau_{\mathrm{S}} s + 1\right)\right] q. \tag{22}$$

In summary, the droop law is as follows:

$$\omega_{\mathrm{r}} = \omega_{\mathrm{N}} - n_{\mathrm{P}}(P - P_{\mathrm{ref}}),\ V_{\mathrm{r}} = V_{\mathrm{N}} - m_{\mathrm{Q}}\left(Q - Q_{\mathrm{ref}}\right), \tag{23}$$

where, $\omega_{\mathrm{r}} = \dot{\theta}_{\mathrm{r}}$, ω_{N} and V_{N} are the nominal frequency and voltage. The reference signals for the voltage controller are generated as shown in the lower left of Table I. Reference [3] is utilized for the design guidelines in this study.

[$\mathcal{R}_2$] Virtual Synchronous Machine Controller: Emulating a synchronous machine, known as VSM, is a direct method to integrate GFM capabilities into an IIDG. VSM-based IIDGs employ the swing equation and damping of virtual mass inertia, akin to synchronous machines. As an illustrative example for VSM control methods, as shown in $\mathcal{R}_2$ of the Table I, the VSM uses the following swing equation with proper damping:

$$T_{\mathrm{a}} \frac{\mathrm{d}\omega_{\mathrm{r}}}{\mathrm{d}t} = P_{\mathrm{ref}} - p - P_{\mathrm{D}},\ P_{\mathrm{D}} = k_{\mathrm{pf}} \left[\omega_{\mathrm{N}} - \omega_{\mathrm{r}}\right], \tag{24}$$

where p is the measured instantaneous output active power of the IIDG given in (20). P_{ref}, and P_{D} are the reference and damping power, respectively. Here, T_{a} denotes the virtual inertia in the swing equation, which can be adjusted as needed. While the damping coefficient is typically fixed in physical synchronous machines, this parameter can be freely chosen in VSM IIDGs. It directly influences the relationship between active power and frequency, defining the slope of the P-f characteristic, denoted as k_{pf}. k_{df} is introduced to dampen oscillations between generators, affecting the oscillatory angle output according to the following form:

$$\theta_{\mathrm{r}} = \int \omega_{\mathrm{r}} \mathrm{d}t + k_{\mathrm{df}} \left[\omega_{\mathrm{N}} - \omega_{\mathrm{r}}\right]. \tag{25}$$

In the Q-V loop, k_{v} is chosen as the slope of the Q-V characteristic and τ_{S} is the excitation time constant. Finally, it is ascribed by the following form:

$$V_{\mathrm{r}} = \left[V_{\mathrm{N}} - k_{\mathrm{v}} \left(q - Q_{\mathrm{ref}}\right)\right] \frac{1}{1 + \tau_{\mathrm{S}} s}, \tag{26}$$

where q is the measured instantaneous output reactive power of the IIDG given in (21). Q_{ref} is the reference, respectively. Reference [28] is utilized for the design guidelines in this study.

[$\mathcal{R}_3$] Virtual Oscillator Controller: A VOC is a nonlinear control strategy, which makes an IIDG reproduce the dynamics of a weakly nonlinear limit-cycle oscillator called the Andronov Hopf system. The equations for the inductor current, i_{R}, and the capacitor voltage, v_{R}, are given below:

$$L \frac{\mathrm{d}i_{\mathrm{R}}}{\mathrm{d}t} = v_{\mathrm{R}},\ C \frac{\mathrm{d}v_{\mathrm{R}}}{\mathrm{d}t} = \sigma v_{\mathrm{R}} + \alpha v_{\mathrm{R}}^3 - i_{\mathrm{R}} + \mathcal{K}_{\mathrm{i}} i_{\mathrm{O}'}^{\alpha}. \tag{27}$$

The virtual capacitance, inductance, and conductance are given by C, L, and σ, and the nonlinear voltage-dependent current source is parameterized by α. Here, $i_{\mathrm{O}'}^{\alpha}$ is given by:

$$i_{\mathrm{O}'}^{\alpha} = i_{\mathrm{O}}^{\alpha} - i_{\mathrm{O,ref}}^{\alpha}, \tag{28}$$

$$\begin{bmatrix} i_{\mathrm{O,ref}}^{\alpha} \\ i_{\mathrm{O,ref}}^{\beta} \end{bmatrix} = \underbrace{\frac{2}{3||v_{\mathrm{C,ref}}^{\alpha\beta}||^2} \begin{bmatrix} v_{\mathrm{C,ref}}^{\alpha} & v_{\mathrm{C,ref}}^{\beta} \\ -v_{\mathrm{C,ref}}^{\beta} & v_{\mathrm{C,ref}}^{\alpha} \end{bmatrix}}_{\Xi} \begin{bmatrix} P_{\mathrm{ref}} \\ Q_{\mathrm{ref}} \end{bmatrix} \tag{29}$$

The controller is interfaced via voltage and current scaling values, $\mathcal{K}_{\mathrm{v}}$ and $\mathcal{K}_{\mathrm{i}}$, respectively. Also, $\epsilon = \sqrt{L/C}$. As shown in Table I the output voltage command is given by:

$$v_{\mathrm{C,ref}}^{\alpha} = \mathcal{K}_{\mathrm{v}} v_{\mathrm{R}},\ v_{\mathrm{C,ref}}^{\beta} = \epsilon \mathcal{K}_{\mathrm{v}} i_{\mathrm{R}}. \tag{30}$$

P_{ref} and Q_{ref} are the references, respectively. Reference [27] is utilized for the design guidelines in this study.

B. Equivalent Model of GFM IIDGs in Sequence Domain

The Th é venin equivalent circuit representation of a GFM IIDG is ascribed by the following form:

$$v_{\mathrm{C}}^{\mathrm{xy}} = \mathcal{G} v_{\mathrm{C,ref}}^{\mathrm{xy}} - \mathcal{Z} i_{\mathrm{O}}^{\mathrm{xy}}, \tag{31}$$

where, xy = dq or xy = $\alpha\beta$ in case of $\mathcal{C}_1$ or $\mathcal{C}_2$ of Section II-I-A-1, respectively. Moreover, depending on $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$ of Section III-A-3, $v_{\mathrm{C,ref}}^{\mathrm{xy}}$ differs for both $\alpha\beta$ and dq domain. Typically, controllers are designed to ensure that the GFM IIDG behaves as a controllable voltage source with voltage $v_{\mathrm{C,ref}}^{\mathrm{xy}}$ and minimal impedance by maintaining $\mathcal{G} \approx 1$ and $\mathcal{Z} \approx 0$. Both the voltage reference generation control and the voltage loop controller are responsible to maintain the voltage source behavior of the GFM IIDG. However, this applies only when controller action is unrestricted by current-limiting strategies, as discussed in Section III-A-2. When current limiters bound controller outputs, the behavior of $\mathcal{G}$ and $\mathcal{Z}$ changes significantly, largely influenced by the type of voltage reference generation control, voltage controller, and fault current limiter. During different types of faults (symmetrical and asymmetrical), the active and reactive output power of the IIDG changes dramatically. Due to the low-pass filtering effect, voltage reference generation control signals, $v_{\mathrm{C,ref}}^{\mathrm{dq}}$ or $v_{\mathrm{C,ref}}^{\alpha\beta}$ from $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$ (Section III-A-3), maintain their pre-fault characteristics, exhibiting minimal change. While it is true that the average values of active and reactive power (processed through the low-pass filter) will eventually settle at final values different from their pre-fault values, the time frame considered in this work for calculating the positive and negative sequence impedances is lesser than the time constant of the low-pass filter. This ensures that the changes in the voltage magnitude and frequency of the internal voltage source, caused by the averaged active and reactive power, do not influence the characteristics of the internal voltage source. However, suppose the time constant of the low-pass filter in the voltage reference generation controller is significantly lower. In that case, these changes in voltage magnitude and frequency must be considered during the computation of the positive and negative sequence impedances. In such a case, calculating $\overline{E}$ would require measuring the internal voltage signal from the GFM inverter controller. Specifically, this measurement would involve the output of the voltage reference generation controller, including $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$. However, this consistency is not observed in $v_{\mathrm{C}}^{\mathrm{dq}}$, $i_{\mathrm{O}}^{\mathrm{dq}}$ and $v_{\mathrm{C}}^{\alpha\beta}$, $i_{\mathrm{O}}^{\alpha\beta}$ signals, resulting in unbalanced voltage and current outputs during asymmetrical faults despite balanced voltage reference signals. This behavior leads to the sequence-domain equivalent circuit of a GFM IIDG through the following equations:

$$\overline{V}_{\mathrm{C}}^{+} = \overline{E} - \mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}} \overline{I}_{\mathrm{O}}^{+},\ \overline{V}_{\mathrm{C}}^{-} = -\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}} \overline{I}_{\mathrm{O}}^{-}. \tag{32}$$

TABLE II
GFM-IIDG AND SYSTEM PARAMETERS UNDER STUDY

GFM-IIDG	Value
Ratings	3-ϕ, 480 V, 60 Hz, 120 kVA, $V_{\rm dc}$ = 1 kV
LC Filter	$L_{\rm f}$ = 150 μH, $R_{\rm f}$ = 5 mΩ, $C_{\rm f}$ = 110 μF
Controller [$\mathcal{C}_1$]	$\{k_{\rm v}^{\rm p}, k_{\rm v}^{\rm i}, k_{\rm c}^{\rm p}, k_{\rm c}^{\rm i}\} = \{0.04, 16.78, 0.6, 20\}$
Controller [$\mathcal{C}_2$]	$\{k_{\rm v}^{\rm p}, k_{\rm v}^{\rm r}, k_{\rm c}^{\rm p}, k_{\rm c}^{\rm i}, \zeta\} = \{0.1, 150, 0.6, 20, 0.003\}$
Controller [$\mathcal{R}_1$]	$\{\tau_{\rm S}, n_{\rm P}, m_{\rm Q}\} = \{0.5$ s, 0.0042 Hz/kW, 0.2 V/kVAr$\}$
Controller [$\mathcal{R}_2$]	$\{\tau_{\rm S}, T_{\rm a}, k_{\rm pf}, k_{\rm df}, k_{\rm v}\} = \{0.5$ s, 1.8 s, 0.02 kW.s/rad, 0.03, 0.2 V/kVAr$\}$
Controller [$\mathcal{R}_3$]	$\{\mathcal{K}_{\rm i}, \mathcal{K}_{\rm v}, \sigma, \alpha, L, C\} = \{0.2, 125, 10\ \Omega^{-1}, 7.5\ {\rm A/V^3}, 39.9\ \mu{\rm H}, 176.3$ mF$\}$
Limiter [$\mathcal{L}_1 - \mathcal{L}_4$]	$\{i_{\rm sat}, i_{\rm latch}, i_{\rm reset}, k_{\rm p}^{R_{\rm vir}}, \sigma_{\rm X/R}\} = \{1.2$ pu, 1.2 pu, 1.05 pu, 0.8 Ω/A, 2$\}$

Grid [$v_{\rm g}^{\rm abc}$]
3-ϕ, 60 Hz, 0.48 kV, 120 kVA
X/R = 5
SCR $\in \{0.1, 0.5, 1, 2, 4, 8\}$
Local Load
120 kVA, pf = 0.85
Fault
$R_{\rm f} \in [0.01\ 0.1]\ \Omega$
Type = LG, LL, LLG

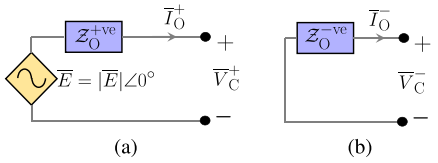


Fig. 1. Equivalent (a) *positive-sequence*, and (b) *negative-sequence* fault model of grid-forming inverter-based-resources.

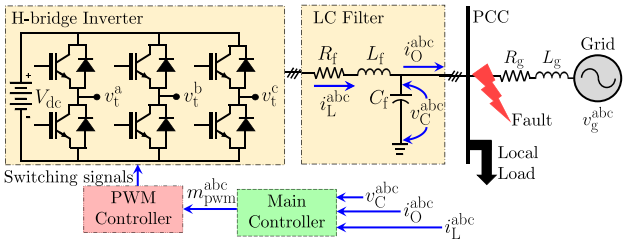


Fig. 2. Fundamental building blocks and power circuit of an IIDG.

The equivalent circuit model in the sequence domain is shown in Fig. 1. Here, $\overline{E} = v_{\rm C,ref}^{\rm d} + jv_{\rm C,ref}^{\rm q}$ in case of $\mathcal{C}_1$ and $\overline{E} = v_{\rm C,ref}^{\alpha} + jv_{\rm C,ref}^{\beta}$ in case of $\mathcal{C}_2$. As $v_{\rm C,ref}^{\rm dq}$ or $v_{\rm C,ref}^{\alpha\beta}$ does not change before and after the fault due to the slow filter response, the pre-fault value of $v_{\rm C}^{\rm dq}$ or $v_{\rm C}^{\alpha\beta}$ are equal to $v_{\rm C,ref}^{\rm dq}$ or $v_{\rm C,ref}^{\alpha\beta}$ according to the (31) with $\mathcal{G} \approx 1$ and $\mathcal{Z} \approx 0$. In other words, the phasor $\overline{E}$ can be computed using the pre-fault terminal voltage of the GFM IIDG. $\mathcal{Z}_{\rm O}^{+\rm ve}$ and $\mathcal{Z}_{\rm O}^{-\rm ve}$ are the equivalent *positive-* and *negative-sequence* impedance of the GFM IIDG. $\overline{V}_{\rm C}^{+}$, $\overline{V}_{\rm C}^{-}$, and $\overline{I}_{\rm O}^{+}$, $\overline{I}_{\rm O}^{-}$ are the *positive-* and *negative-sequence* output voltage and the output current of the GFM IIDG, respectively. It is important to observe that the voltage behind the sequence-impedances is present only in the circuit in *positive-sequence* domain as these controls under study do not include any sequence-domain control explicitly. Usually, a three-phase three-leg IIDG topology cannot produce any *zero-sequence* current due to the absence of grounding. In other words, the magnitude of *zero-sequence* impedance is theoretically infinite, and voltage reference generation control, voltage control, and current-limiter do not have any impact on the *zero-sequence* impedance of the GFM IIDG.

IV. ANALYSIS OF EMT SIMULATION RESULTS

A. Procedure of EMT Simulation Study

The system under study is shown in Fig. 2 and the parameters are tabulated in Table II. During simulation in on-grid conditions, the value of grid resistance, $R_{\rm g}$, and inductance, $L_{\rm g}$, are determined based on the selected SCR and the X/R ratio. To compute the various parameters of (32), multiple time-domain electromagnetic transient (EMT) simulation studies are conducted with the following steps:

$\mathcal{S}1$: perform an asymmetrical fault across the terminal of the IIDG of Fig. 2, in either on-grid or off-grid condition.

$\mathcal{S}2$: vary the fault type and impedance so that the voltage unbalance factor (quantified by the ratio between the *negative-sequence* voltage magnitude and *positive-sequence* voltage magnitude at the terminal of the GFM IIDG, V^-/V^+, in percentage) covers a range of around 20% to 90%.

$\mathcal{S}3$: for each case, calculate the per-unit *positive-sequence* and *negative-sequence* phasor of the output voltage, $v_{\rm C}^{\rm abc}$, and the output current, $i_{\rm O}^{\rm abc}$, denoted by $\overline{V}_{\rm C}^{+}$, $\overline{V}_{\rm C}^{-}$, and $\overline{I}_{\rm O}^{+}$, $\overline{I}_{\rm O}^{-}$, respectively, in the steady state after each fault.

$\mathcal{S}4$: for each simulation, in the pre-fault condition, the GFM IIDG is loaded at the rated condition by terminating a load across the GFM IIDG. Compute the phasor of the pre-fault terminal voltage of the IIDG and that is designated as $\overline{E}$.

$\mathcal{S}5$: calculate $\mathcal{Z}_{\rm O}^{+\rm ve} = (\overline{E} - \overline{V}_{\rm C}^{+})/\overline{I}_{\rm O}^{+}$, $\mathcal{Z}_{\rm O}^{-\rm ve} = -\overline{V}_{\rm C}^{-}/\overline{I}_{\rm O}^{-}$.

$\mathcal{S}6$: repeat these steps for various combinations of voltage controller schemes, $\mathcal{C}_1$, $\mathcal{C}_2$, various combinations of fault current limiter logic schemes, $\mathcal{L}_1$, $\mathcal{L}_2$, $\mathcal{L}_3$, various combination of voltage reference control schemes, $\mathcal{R}_1$, $\mathcal{R}_2$, $\mathcal{R}_3$.

B. Impact on the Sequence Model of GFM IIDGs

In this sub-section, following questions are answered:

$\mathcal{Q}1$) How does the design of the outer voltage reference generation controls (i.e. $\mathcal{R}_1$, $\mathcal{R}_2$, $\mathcal{R}_3$ of Section III-A-3) influence the nature of $\mathcal{Z}_{\rm O}^{+\rm ve}$ and $\mathcal{Z}_{\rm O}^{-\rm ve}$?

$\mathcal{Q}2$) How does the fault-limiters (i.e. $\mathcal{L}_1$, $\mathcal{L}_2$, $\mathcal{L}_3$ of Section II-I-A2) influence the nature of $\mathcal{Z}_{\rm O}^{+\rm ve}$ and $\mathcal{Z}_{\rm O}^{-\rm ve}$?

$\mathcal{Q}3$) How does the design of the voltage loop controls (i.e. $\mathcal{C}_1$, $\mathcal{C}_2$ of Section III-A-1) influence the nature of $\mathcal{Z}_{\rm O}^{+\rm ve}$ and $\mathcal{Z}_{\rm O}^{-\rm ve}$?

1) Impact of Voltage Reference Generation Control: Fig. 3(a) and (b) show the magnitude ($|\mathcal{Z}_{\rm O}^{+\rm ve}|$ and $|\mathcal{Z}_{\rm O}^{-\rm ve}|$) and phase angle ($\angle\mathcal{Z}_{\rm O}^{+\rm ve}$ and $\angle\mathcal{Z}_{\rm O}^{-\rm ve}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with dq-domain voltage control ($\mathcal{C}_1$) and instantaneous current saturation limiter with d-axis priority ($\mathcal{L}_{1\rm d}$) with droop-based ($\mathcal{R}_1$), VSM-based ($\mathcal{R}_2$), and VOC-based ($\mathcal{R}_3$) voltage reference control for different voltage imbalance factors. Fig. 4(a) and (b) show the magnitude ($|\mathcal{Z}_{\rm O}^{+\rm ve}|$ and $|\mathcal{Z}_{\rm O}^{-\rm ve}|$) and phase angle

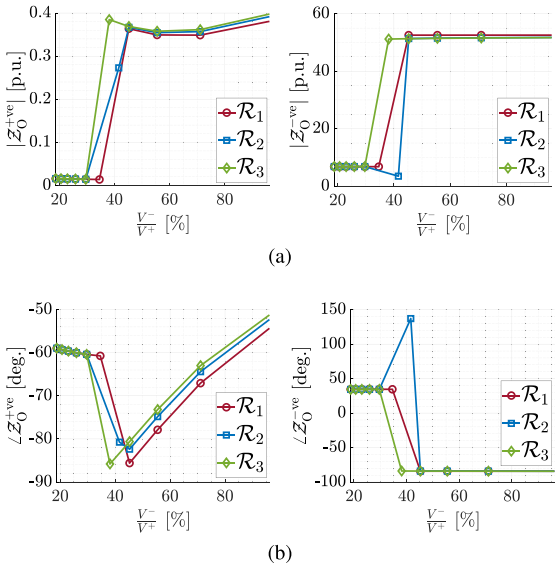


Fig. 3. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with dq-domain voltage control and instantaneous current saturation limiter with d-axis priority with droop-based ($\mathcal{R}_1$), VSM-based ($\mathcal{R}_2$), and VOC-based ($\mathcal{R}_3$) voltage reference control for different voltage imbalance factors.

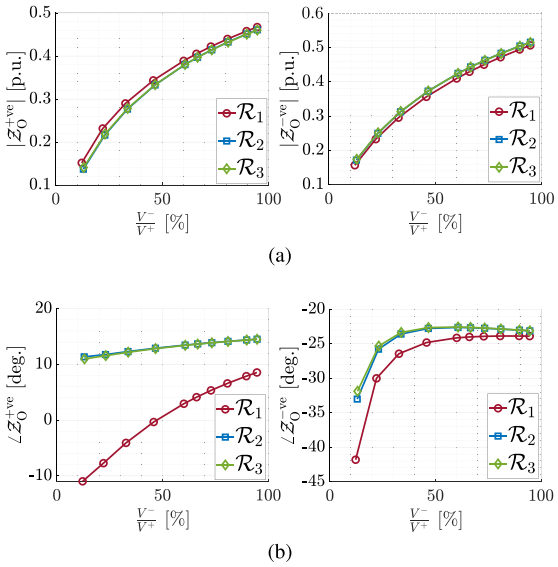


Fig. 4. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with $\alpha\beta$-domain voltage control and instantaneous current saturation limiter with droop-based ($\mathcal{R}_1$), VSM-based ($\mathcal{R}_2$), and VOC-based ($\mathcal{R}_3$) voltage reference control for different voltage imbalance factors.

($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with $\alpha\beta$-domain voltage control ($\mathcal{C}_2$) and instantaneous current saturation limiter ($\mathcal{L}_1$) with droop-based ($\mathcal{R}_1$), VSM-based ($\mathcal{R}_2$), and VOC-based ($\mathcal{R}_3$) voltage reference control for different voltage imbalance factors. It is observed that in both cases, the variation of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ are close to each other during $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$. Especially, the variation of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$,

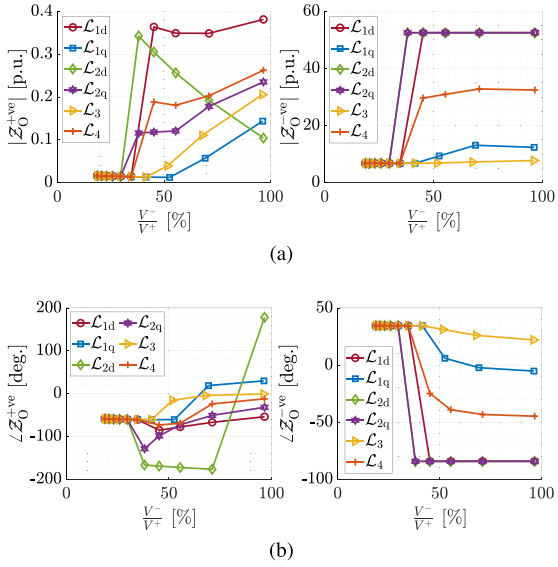


Fig. 5. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme and dq-domain voltage control and with instantaneous current saturation limiter in d-axis ($\mathcal{L}_{1\mathrm{d}}$), q-axis ($\mathcal{L}_{1\mathrm{q}}$), latching current limiter in d-axis ($\mathcal{L}_{2\mathrm{d}}$), q-axis ($\mathcal{L}_{2\mathrm{q}}$), virtual impedance-based limiter ($\mathcal{L}_3$), and circular magnitude limiter ($\mathcal{L}_4$) for different voltage imbalance factors.

$|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$ are quite close to each other w.r.t. the variation with $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$. The difference in the phases, especially in $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ in Fig. 4(b) where $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ in case of $\mathcal{R}_1$ differs from $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ in case of $\mathcal{R}_2$ or $\mathcal{R}_3$, is due to the slight mismatch in the pre-fault conditions of the GFM IIDG during the EMT study. All the phasor quantities are determined w.r.t. the reference phasor, $\overline{E}$. These EMT simulation results empirically conclude that the type of the voltage reference generation scheme ($\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$) has minimal impact on the type of the equivalent sequence impedances under fault.

2) Impact of Current Limiting Schemes: Fig. 5 shows the magnitude ($|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$ and $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$) and phase angle ($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme ($\mathcal{R}_1$) and dq-domain voltage control ($\mathcal{C}_1$) and with instantaneous current saturation limiter in d-axis ($\mathcal{L}_{1\mathrm{d}}$), q-axis ($\mathcal{L}_{1\mathrm{q}}$), latching current limiter in d-axis ($\mathcal{L}_{2\mathrm{d}}$), q-axis ($\mathcal{L}_{2\mathrm{q}}$), virtual impedance-based limiter ($\mathcal{L}_3$), and circular magnitude limiter ($\mathcal{L}_4$) for different voltage imbalance factors. Fig. 6 shows the magnitude ($|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$ and $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$) and phase angle ($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the GFM IIDG with droop-based voltage reference generation scheme ($\mathcal{R}_1$) and $\alpha\beta$-domain voltage control ($\mathcal{C}_2$) and with instantaneous current saturation limiter ($\mathcal{L}_1$), latching current limiter ($\mathcal{L}_2$), and virtual impedance-based limiter ($\mathcal{L}_3$) for different voltage imbalance factors. The results show here that the variations of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ w.r.t. the different unbalance factor are significantly different from each other depending on the selection of the fault current limiter logic. For instance in Fig. 5(a) and (b), it is observed that during lower unbalance factor (designated by the medium impedance asymmetrical faults), $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ are all same as the fault limiter logic is not yet hit by the

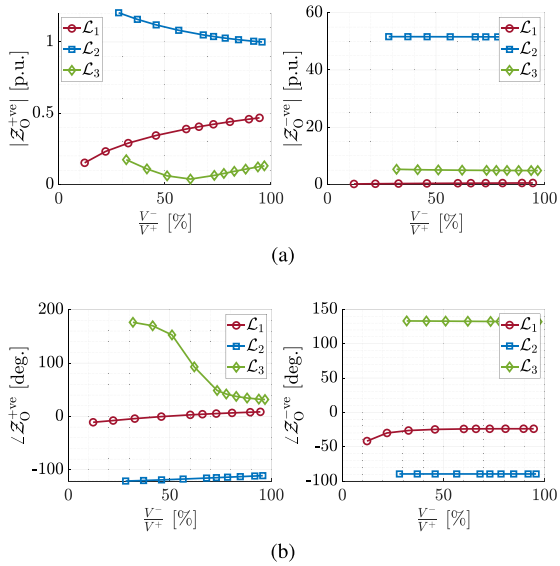


Fig. 6. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme and $\alpha\beta$-domain voltage control and with instantaneous current saturation limiter ($\mathcal{L}_1$), latching current limiter ($\mathcal{L}_2$), and virtual impedance-based limiter ($\mathcal{L}_3$) for different voltage imbalance factors.

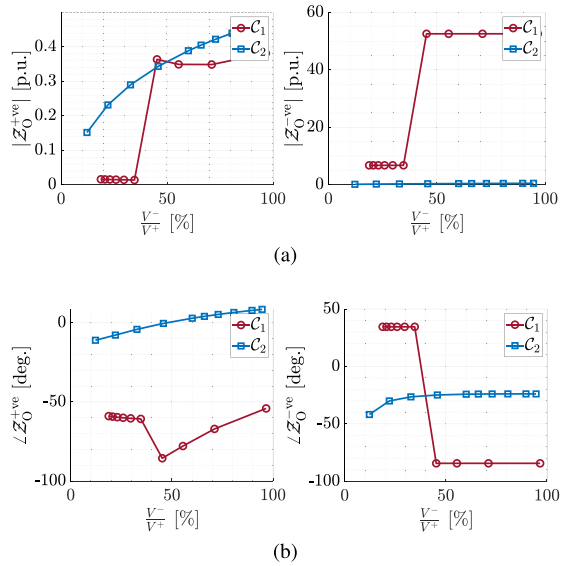


Fig. 7. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme with dq-domain voltage control combined with instantaneous current saturation limiter in d-axis and $\alpha\beta$-domain voltage control combined with instantaneous current saturation limiter for different voltage imbalance factors.

fault condition. However, for a higher value of unbalanced factor (designated by the low impedance asymmetrical faults), $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ diverge from each other depending on the selection of the fault current limiter logic. However, in case of Fig. 6(a) and (b), the similar trajectory are not observed. This will be explained later as it is related to the selection of the voltage control logic and the corresponding behavior under faults. However, it is consistently observed in Fig. 6(a) and (b) also that the nature of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ are significantly different from each other depending on the selection of the fault limiter logic. These EMT simulation results empirically conclude that the type of fault current limiter logic ($\mathcal{L}_{1\mathrm{d}}$, $\mathcal{L}_{1\mathrm{q}}$, $\mathcal{L}_{2\mathrm{d}}$, $\mathcal{L}_{2\mathrm{q}}$, $\mathcal{L}_3$, $\mathcal{L}_4$ in case of $\mathcal{C}_1$, and $\mathcal{L}_1$, $\mathcal{L}_2$, $\mathcal{L}_3$ in case of $\mathcal{C}_2$) has significant impact on the type of the equivalent sequence impedances under fault.

3) Impact of Voltage Controller Loop: Fig. 7 shows the magnitude ($|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$ and $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$) and phase angle ($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme ($\mathcal{R}_1$) with dq-domain voltage control ($\mathcal{C}_1$) combined with instantaneous current saturation limiter in d-axis ($\mathcal{L}_{1\mathrm{d}}$) and $\alpha\beta$-domain voltage control ($\mathcal{C}_2$) combined with instantaneous current saturation limiter ($\mathcal{L}_1$) for different voltage imbalance factors. Fig. 8 shows the magnitude ($|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$ and $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$) and phase angle ($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme ($\mathcal{R}_1$) with dq-domain voltage control ($\mathcal{C}_1$) combined with latching current limiter in q-axis ($\mathcal{L}_{2\mathrm{q}}$) and $\alpha\beta$-domain voltage control ($\mathcal{C}_2$) combined with latching current limiter ($\mathcal{L}_2$) for different voltage imbalance factors. The results show here that the variations of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ w.r.t. the different unbalance factor are significantly different from each other depending on

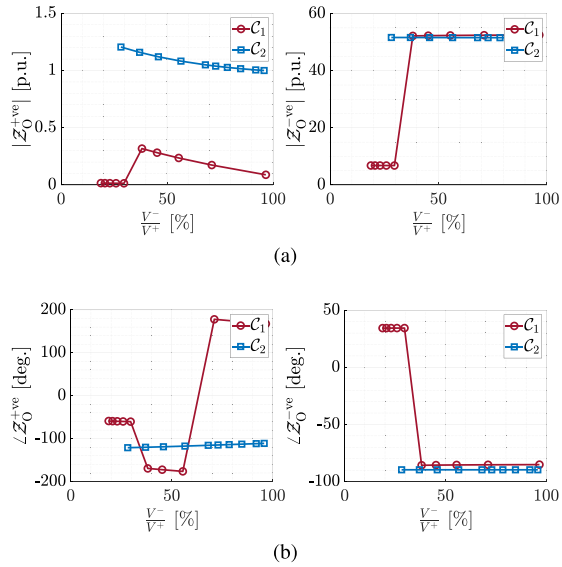


Fig. 8. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme with dq-domain voltage control combined with the latching current limiter in q-axis and $\alpha\beta$-domain voltage control combined with latching current limiter for different voltage imbalance factors.

the selection of the type of the voltage controller. For instance in Figs. 7(a) and 8(a), there is a sudden jump in both $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$ after around 35% of unbalance factor. In and more than 35% of unbalanced factor, both the instantaneous current saturation limiter with d-axis priority and latching current limiter with q-axis priority hits the limit. However, the nature of $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$ in case of $\mathcal{C}_2$ doesn't follow the similar trend. The fundamental reason of this difference in the nature is the performance of the inner-current controller in these cases after

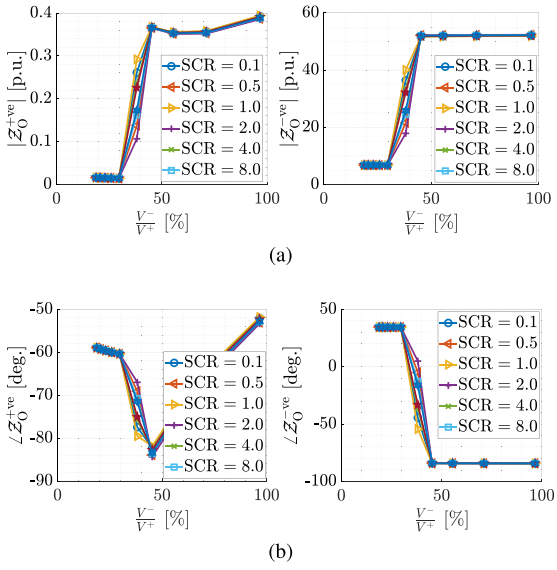


Fig. 9. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme with dq-domain voltage control combined with saturation current limiter in d-axis for different voltage imbalance factors in on-grid condition with various SCR values.

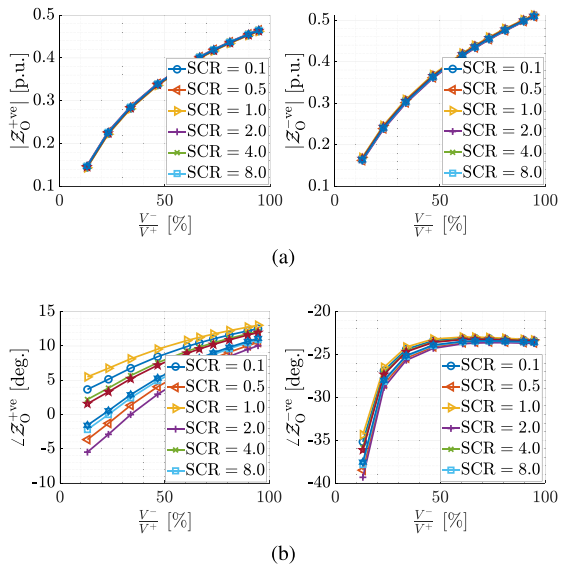


Fig. 10. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme with $\alpha\beta$-domain voltage control combined with latching current limiter for different voltage imbalance factors in on-grid condition with various SCR values.

the limits are hit. It is important to note that the $\alpha\beta$ component of unbalanced three-phase signals remains sinusoidal and as a result, the performance of the proportional+integral controller in the inner-current controller in $\mathcal{C}_2$ maintains the sinusoidal nature of the output current even if the reference signal, generated by the current limiter logic, is not tracked properly. Therefore, the sudden change in the trajectory in the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$ are not observed, rather a smooth trajectory is observed. However, dq component of unbalanced three-phase signals consists of a DC signal added with peak-clipped sinusoidal 2ω component (either in d component or in q component or in both depending on the axis-priority logic) where ω is the fundamental frequency of the three-phase signal. The performance of the proportional+integral controller in the inner-current controller in case of $\mathcal{C}_1$ deteriorates quite significantly as peak-clipped distorted signal deteriorates the performance of the proportional+integral controller. However, it is consistently observed in Figs. 7 and 8 also that the nature of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ are significantly different from each other depending on the selection of the reference-frame for the voltage controller. These results empirically conclude that $\mathcal{C}_1, \mathcal{C}_2$ have a significant impact on the type of equivalent sequence impedances under fault.

4) Impact of On-Grid Mode With Varying SCR: Figs. 9 and 10 show the magnitude ($|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$ and $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$) and phase angle ($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme ($\mathcal{R}_1$) with dq-domain voltage control ($\mathcal{C}_1$) combined with instantaneous current saturation limiter in d-axis ($\mathcal{L}_{1\mathrm{d}}$) and with $\alpha\beta$-domain voltage control ($\mathcal{C}_2$) combined with instantaneous current saturation limiter ($\mathcal{L}_1$) for different voltage imbalance factors in on-grid condition under various SCR values, respectively. The results show here that the variations of the $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ w.r.t. the different unbalance factor are quite similar for different SCR values of the grid and also similar with the values determined under off-grid condition. For instance, the nature of $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ in Fig. 9(a) and (b) resemble with the nature in the case of $\mathcal{C}_1$ of Fig. 7(a) and (b). Similarly, the nature of $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ in Fig. 10(a) and (b) resemble with the nature in the case of $\mathcal{C}_2$ of Fig. 7(a) and (b). Similar findings are observed with all other types of voltage reference generation schemes, voltage controller type and the current limiter logic. The fundamental reason behind this is that the $\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$, $\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ of the GFM IIDG are dominantly influenced by the GFM IIDG filter circuits and the controller parameters. Hence, the off-grid and on-grid operations with varying SCR values have an insignificant impact on the type of equivalent sequence impedances under fault.

TABLE III
SELECTED PARAMETERS OF CONTROLLER AND LIMITER

Controller, Limiter	Values of the parameters
$\mathcal{C}_1^{[2]}, \mathcal{C}_1^{[2]}, \mathcal{C}_1^{[3]}$	$\tau_{\mathrm{c}} = \{250, 250, 125\}\mu$s, phase margin $= \{53^\circ, 45^\circ, 45^\circ\}$ crossover freq. $= \{1.3\mathrm{k}, 1.6\mathrm{k}, 3.3\mathrm{k}\}$ rad/s
$\mathcal{L}_{1\mathrm{d}}^{[1]}, \mathcal{L}_{1\mathrm{d}}^{[2]}, \mathcal{L}_{1\mathrm{d}}^{[3]}$	$i_{\mathrm{sat}} = \{1.2, 1.3, 1.4\}$ pu

5) Dominant Impacts of Controller and Limiter Parameters: Fig. 11 shows the magnitude ($|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$ and $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$) and phase angle ($\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$) of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme ($\mathcal{R}_1$) with dq-domain voltage control ($\mathcal{C}_1$) combined with instantaneous current saturation limiter in d-axis ($\mathcal{L}_{1\mathrm{d}}$) for different voltage imbalance factors while varying selected parameters in controller and the current limiter (as tabulated in Table III), respectively. The relation with the $k_{\mathrm{v}}^{\mathrm{p}}$, $k_{\mathrm{v}}^{\mathrm{i}}$, $k_{\mathrm{c}}^{\mathrm{p}}$, and $k_{\mathrm{c}}^{\mathrm{i}}$ of Table II with

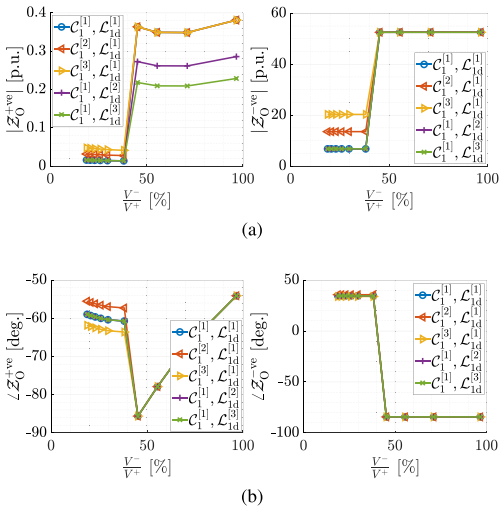


Fig. 11. Magnitude and phase angle of the *positive-sequence* and *negative-sequence* output impedance of the GFM IIDG with droop-based voltage reference generation scheme with dq-domain voltage control combined with saturation current limiter in d-axis for different voltage imbalance factors under selected parameters of controller and limiter from Table III.

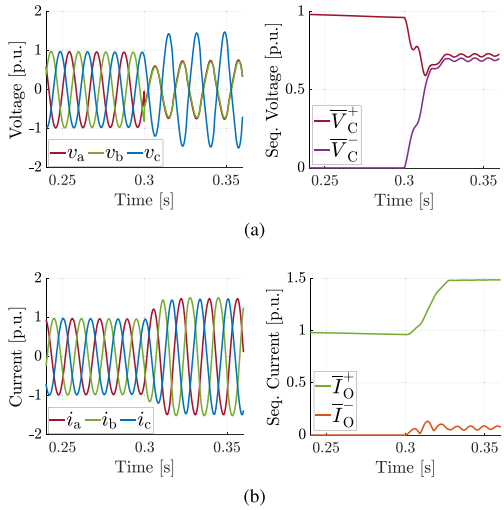


Fig. 12. Figure of (a) instantaneous and sequence voltages, and (b) instantaneous and sequence fault currents while the GFM IIDG is operating with droop-controlled voltage controller in dq domain with saturation-based fault current limiter with d-axis priority, under AB fault with $R_{\mathrm{f}} = 0.01$.

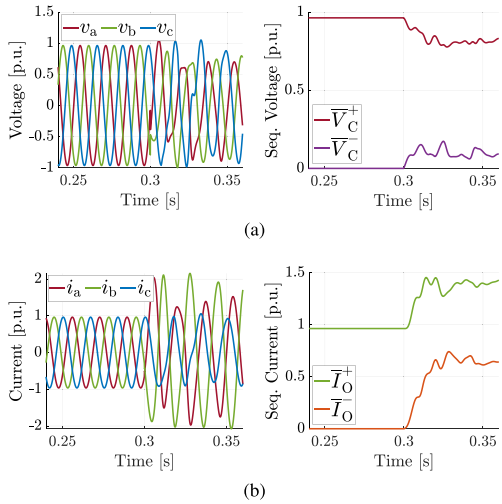


Fig. 13. Figure of (a) instantaneous and sequence voltages, and (b) instantaneous and sequence fault currents while the GFM IIDG is operating with droop-controlled voltage controller in $\alpha\beta$ domain with instantaneous saturation-based fault current limiter, under AB fault with $R_{\mathrm{f}} = 0.625$.

parameters of Table III is defined in reference [36]. It is observed that variations in parameters of $\mathcal{C}_1$ controller cause variation in $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ till the unbalance factor where current limiter doesn't hit. Once the current limiter hits due to higher unbalanced factor resulting from severe fault, the variation in $|\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}|$, $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$, $\angle\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\angle\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ is dominant by the variation in the parameters of the limiter, $\mathcal{L}_{1\mathrm{d}}$. This is an interesting observation that concludes that the sensitivity of the nature of the $\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ and $\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ w.r.t. the selection of the controller and limiter scheme depends on the condition of current limit hitting case caused by the severity of the fault.

C. Discussions

The following conclusions are based on the obtained results of the study conducted in Section IV-B:

- *Impacts of Control and Limiter:* The voltage reference generation control has minimal impact on the type of the equivalent sequence impedances in the fault model of GFM IIDG. The dominant influencing factors are the voltage controller and the fault current limiter schemes.
- *Impacts of Reference-frame of Control:* As observed in Fig. 7(a), $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$ when the voltage controller is designed in $\alpha\beta$-domain, $\mathcal{C}_2$, is not as high as when designed in dq-domain, $\mathcal{C}_1$, with a saturation limiter $\mathcal{L}_1$. As a result, Figs. 12 and 13 shows the fault response with the configuration of $\mathcal{R}_1$-$\mathcal{C}_1$-$\mathcal{L}_1$ and $\mathcal{R}_1$-$\mathcal{C}_2$-$\mathcal{L}_1$, respectively. It is observed that under unbalanced fault $\mathcal{R}_1$-$\mathcal{C}_2$-$\mathcal{L}_1$ results significant *negative sequence* current magnitude with respect to the *positive-sequence* current. in comparison with the $\mathcal{R}_1$-$\mathcal{C}_1$-$\mathcal{L}_1$.
- *Negative-sequence Current Suppression:* Figs. 5(a) and 6(a) show that $|\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}|$ is low in both $\mathcal{C}_1$ and $\mathcal{C}_2$ with a virtual impedance-based limiter $\mathcal{L}_3$. This implies that during an unbalanced fault with a current limiter scheme of $\mathcal{L}_3$, irrespective of the type of the voltage controller (either $\mathcal{C}_1$ or $\mathcal{C}_2$), the GFM IIDG does not have the same suppressing effect on the *negative-sequence* current. As observed in Figs. 14 and 15, there is a significant amount of *negative-sequence* current magnitude after the corresponding unbalanced faults for both the cases.
- *Nature of Sequence Impedances:* In all observed results, both the *positive-sequence* and *negative-sequence* impedance exhibit predominantly inductive characteristics. Notably, the computed values of $\mathcal{Z}_{\mathrm{O}}^{+\mathrm{ve}}$ or $\mathcal{Z}_{\mathrm{O}}^{-\mathrm{ve}}$ do not include contributions from the grid-side filter inductance or corresponding parasitic resistance in this study, as the GFM IIDG is equipped with an LC filter. Therefore, the

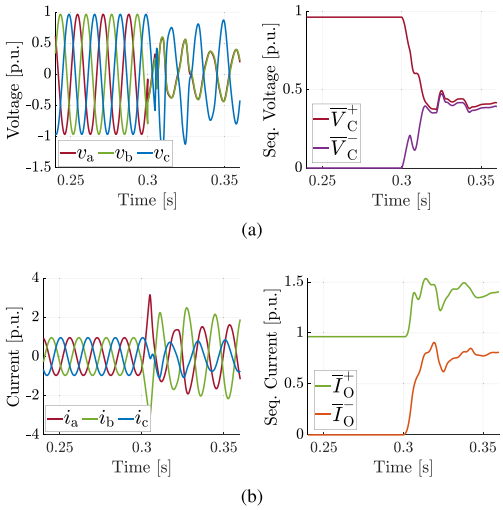


Fig. 14. Figure of (a) instantaneous and sequence voltages, and (b) instantaneous and sequence fault currents while the GFM IIDG is operating with droop-controlled voltage controller in dq domain with virtual impedance-based fault current limiter, under AB fault with $R_{\mathrm{f}} = 0.01$.

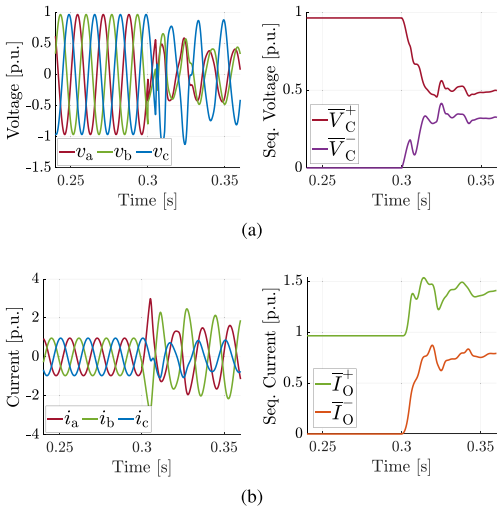


Fig. 15. Figure of (a) instantaneous and sequence voltages, and (b) instantaneous and sequence fault currents while the GFM IIDG is operating with droop-controlled voltage controller in $\alpha\beta$ domain with virtual impedance-based fault current limiter, under AB fault with $R_{\mathrm{f}} = 0.625$.

observed characteristics in the sequence domains primarily stem from the controller and current limiter operations.

V. Conclusion

This study delves into diverse control and current limiting strategies and investigates their repercussions on the positive and negative sequence impedances within the sequence domain fault model of GFM IIDGs. Results from an extensive numerical simulation study elucidate that voltage reference generation controls, such as droop control, virtual synchronous machine control, and virtual oscillator-based control, manifest negligible influence on the nature of the positive and negative sequence impedances of GFM IIDGs. Conversely, it is found that the selection of voltage control methodologies such as outer-voltage-inner-current controller designed in dq-domain or in $\alpha\beta$-domain emerges as one of the principal determinants in shaping the sequence models of GFM IIDGs. Furthermore, current limiting schemes such as d/q axis-priority-wise saturation- or latching- or circular magnitude or virtual impedance-based limiting schemes are identified as the primary factors influencing the sequence models of GFM IIDGs. As a future work, a comprehensive exploration will be undertaken to assess the influence of anti-windup protection schemes, employed in the voltage controller, on the fault model of GFM IIDG. Moreover, the control and limiter scheme are considered unchanged before and after the fault in this work. In the case of change in the controller/limiter (e.g., priority logic changes from d to q-axis), the fault current behavior of the GFM IIDG during transient as well as in steady-state will be different than the case when the priority logic is unchanged. Further investigations on the sequence impedances in these cases will be done in future.

References

[1] Y. Lin et al., "Research Roadmap on Grid-Forming Inverters," National Renewable Energy Lab. (NREL), Golden, CO, USA, Tech. Rep. NREL/TP-5D00-73476, 2020.

[2] J. Matevosyan et al., "Grid-forming inverters: Are they the key for high renewable penetration?," *IEEE Power Energy Mag.*, vol. 17, no. 6, pp. 89–98, Nov./Dec. 2019.

[3] J. M. Guerrero, L. G. De Vicuna, J. Matas, M. Castilla, and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1205–1213, Sep. 2004.

[4] H.-P. Beck and R. Hesse, "Virtual synchronous machine," in *Proc. 9th Int. Conf. Elect. Power Qual. Utilisation*, 2007, pp. 1–6.

[5] H. Wu, X. Wang, and L. Zhao, "Design considerations of current-limiting control for grid-forming capability enhancement of VSCs under large grid disturbances," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 12081–12085, Oct. 2024.

[6] S. Pola, M. A. Azzouz, and M. Mirhassani, "Synchronverters with fault ride-through capabilities for reliable microgrid protection during balanced and unbalanced faults," *IEEE Trans. Sustain. Energy*, vol. 15, no. 3, pp. 1663–1676, Jul. 2024.

[7] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources With Associated Electric Power Systems Interfaces–Amendment 1: To Provide More Flexibility for Adoption of Abnormal Operating Performance Category III*, IEEE Std 1547a-2020 (Amendment to IEEE Std 1547-2018), pp. 1–16, 2020.

[8] R. Luo, H. Gao, F. Peng, and Y. Guo, "An adaptive low-voltage ride-through method for virtual synchronous generators during asymmetrical grid faults," *IEEE Trans. Sustain. Energy*, vol. 15, no. 3, pp. 1589–1600, Jul. 2024.

[9] M. Abdel-Akher and K. M. Nor, "Fault analysis of multiphase distribution systems using symmetrical components," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2931–2939, Oct. 2010.

[10] T. N. Boutsika and S. A. Papathanassiou, "Short-circuit calculations in networks with distributed generation," *Electric Power Syst. Res.*, vol. 78, no. 7, pp. 1181–1191, 2008.

[11] C. A. Plet, "Fault Response of Inverter-Based Distributed Generation," Ph.D. dissertation, Imperial College London, London, U.K., 2012.

[12] C. A. Plet, M. Graovac, T. C. Green, and R. Iravani, "Fault response of grid-connected inverter dominated networks," in *Proc. IEEE PES Gen. Meeting*, 2010, pp. 1–8.

[13] N. Nimpitiwan, G. T. Heydt, R. Ayyanar, and S. Suryanarayanan, "Fault current contribution from synchronous machine and inverter based distributed generators," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 634–641, Jan. 2007.

[14] N. Baeckeland, D. Venkatramanan, M. Kleemann, and S. Dhople, "Fault behavior of inverter-based resources: A comparative study for grid-forming and grid-following control paradigms," in *Proc. IECON–48th Annu. Conf. IEEE Ind. Electron. Soc.*, 2022, pp. 1–6.

[15] H. Zhang, R. Liu, C. Xue, and Y. Li, "Active power enhancement control strategy of grid-forming inverters under asymmetrical grid faults," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1447–1459, Jan. 2024.
[16] Z. Li, K. W. Chan, J. Hu, and S. W. Or, "An adaptive fault ride-through scheme for grid-forming inverters under asymmetrical grid faults," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12912–12923, Dec. 2022.
[17] Z. Shuai, C. Shen, X. Yin, X. Liu, and Z. J. Shen, "Fault analysis of inverter-interfaced distributed generators with different control schemes," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1223–1235, Jun. 2018.
[18] D. Ramasubramanian and V. Vittal, "Positive sequence model for converter-interfaced synchronous generation with finite DC capacitance," *IEEE Trans. Power Syst.*, vol. 33, no. 3, pp. 3172–3180, May 2018.
[19] W.-M. Guo, L.-H. Mu, and X. Zhang, "Fault models of inverter-interfaced distributed generators within a low-voltage microgrid," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 453–461, Feb. 2017.
[20] B. Mahamedi, J. G. Zhu, M. Eskandari, L. Li, and A. Mehrizi-Sani, "Analysis of fault response of inverter-interfaced distributed generators in sequence networks," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2018, pp. 1–9.
[21] B. Mahamedi and J. E. Fletcher, "The equivalent models of grid-forming inverters in the sequence domain for the steady-state analysis of power systems," *IEEE Trans. Power Syst.*, vol. 35, no. 4, pp. 2876–2887, Jul. 2020.
[22] *IEEE Standard for Interconnection and Interoperability of Inverter-Based Resources (IBRS) Interconnecting With Associated Transmission Electric Power Systems*, IEEE Std 2800-2022, pp. 1–180, 2022.
[23] J. Dolado Fernández, J. Eloy-Garcia, S. Arnaltes, and J. L. Rodríguez-Amenedo, "Sequence control strategy for grid-forming voltage source converters based on the virtual-flux orientation under balanced and unbalanced faults," *Energies*, vol. 16, no. 7, 2023, Art. no. 3056.
[24] M.-A. Nasr and A. Hooshyar, "Controlling grid-forming inverters to meet the negative-sequence current requirements of the IEEE standard 2800-2022," *IEEE Trans. Power Del.*, vol. 38, no. 4, pp. 2541–2555, Aug. 2023.
[25] P. Unruh, M. Nuschke, P. Strauß, and F. Welck, "Overview on grid-forming inverter control methods," *Energies*, vol. 13, no. 10, 2020, Art. no. 2589.
[26] J. M. Guerrero, L. Hang, and J. Uceda, "Control of distributed uninterruptible power supply systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2845–2859, Aug. 2008.
[27] B. B. Johnson, S. V. Dhople, J. L. Cale, A. O. Hamadeh, and P. T. Krein, "Oscillator-based inverter control for islanded three-phase microgrids," *IEEE J. Photovolt.*, vol. 4, no. 1, pp. 387–395, Jan. 2014.
[28] F. Wang, L. Zhang, X. Feng, and H. Guo, "An adaptive control strategy for virtual synchronous generator," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5124–5133, Sep./Oct. 2018.
[29] H. Wang, X. Pei, Y. Chen, Y. Kang, and Y.-F. Liu, "Short-circuit fault protection strategy of parallel three-phase inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 1736–1742.
[30] X. Pei and Y. Kang, "Short-circuit fault protection strategy for high-power three-phase three-wire inverter," *IEEE Trans. Ind. Informat.*, vol. 8, no. 3, pp. 545–553, Aug. 2012.
[31] N. Bottrell and T. C. Green, "Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3786–3797, Jul. 2014.
[32] Y. Khayat, P. Chen, M. Bongiorno, B. Johansson, and R. Majumder, "FRT capability of grid-forming power converters: An anti-windup scheme," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 12842–12855, Oct. 2024.
[33] A. D. Paquette and D. M. Divan, "Virtual impedance current limiting for inverters in microgrids with synchronous generators," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1630–1638, Mar./Apr. 2015.
[34] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Current limiting control with enhanced dynamics of grid-forming converters during fault conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1062–1073, Jun. 2020.
[35] C. Liu, X. Cai, R. Li, and R. Yang, "Optimal short-circuit current control of the grid-forming converter during grid fault condition," *IET Renewable Power Gener.*, vol. 15, no. 10, pp. 2185–2194, 2021.
[36] A. Yazdani and R. Iravani, *Voltage-Sourced Converters in Power Systems*, vol. 34. Hoboken, NJ, USA: Wiley, 2010.
[37] P. C. Loh, M. J. Newman, D. N. Zmood, and D. G. Holmes, "A comparative analysis of multiloop voltage regulation strategies for single and three-phase UPS systems," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1176–1185, Sep. 2003.
[38] Q. Lei, F. Z. Peng, and S. Yang, "Multiloop control method for high-performance microgrid inverter through load voltage and current decoupling with only output voltage feedback," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 953–960, Mar. 2011.
[39] L. Huang, H. Xin, Z. Wang, L. Zhang, K. Wu, and J. Hu, "Transient stability analysis and control design of droop-controlled voltage source converters considering current limitation," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 578–591, Jan. 2019.
[40] X. Zhao and D. Flynn, "Freezing grid-forming converter virtual angular speed to enhance transient stability under current reference limiting," in *Proc. IEEE 21st Workshop Control Model. Power Electron.*, 2020, pp. 1–7.
[41] C. A. Plet and T. C. Green, "Fault response of inverter interfaced distributed generators in grid-connected applications," *Electric Power Syst. Res.*, vol. 106, pp. 21–28, 2014.
[42] K. G. Saffar, S. Driss, and F. B. Ajaei, "Impacts of current limiting on the transient stability of the virtual synchronous generator," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1509–1521, Feb. 2023.
[43] B. Fan and X. Wang, "Fault recovery analysis of grid-forming inverters with priority-based current limiters," *IEEE Trans. Power Syst.*, vol. 38, no. 6, pp. 5102–5112, Nov. 2023.
[44] M. Eskandari and A. V. Savkin, "On the impact of fault ride-through on transient stability of autonomous microgrids: Nonlinear analysis and solution," *IEEE Trans. Smart Grid*, vol. 12, no. 2, pp. 999–1010, Mar. 2021.
[45] B. Fan, T. Liu, F. Zhao, H. Wu, and X. Wang, "A review of current-limiting control of grid-forming inverters under symmetrical disturbances," *IEEE Open J. Power Electron.*, vol. 3, pp. 955–969, 2022.

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