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Liu, Lian

DOI
10.4233/uuid:b0547662-21c7-4da6-ae91-b30facf3aa01

Publication date
2019

Document Version
Final published version

Citation (APA)
Liu, L. (2019). *Protection of multi-terminal HVDC systems: Algorithm development and performance verification by EMT simulations*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:b0547662-21c7-4da6-ae91-b30facf3aa01

PROTECTION OF MULTI-TERMINAL HVDC SYSTEMS

ALGORITHM DEVELOPMENT AND PERFORMANCE VERIFICATION BY EMT SIMULATIONS

PROTECTION OF MULTI-TERMINAL HVDC SYSTEMS

ALGORITHM DEVELOPMENT AND PERFORMANCE VERIFICATION BY EMT SIMULATIONS

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Reactor Magnificus Prof. dr. ir. T.H.J.J. van der Hagen
Chair of the Board for Doctorates
to be defended publicly on
Wednesday 11 December 2019 at 10:00 o'clock

by

Lian LIU

Master of Electrical in Electric Power System and Automation
Wuhan University, Wuhan, China
born in Wuhan, China.

This dissertation has been approved by the promotors.

Composition of the doctoral committee:

Rector Magnificus	Chairperson
Promotor Dr. ir. Marjan Popov	Delft University of Technology
Promotor Prof. ir. M. A. M. M. van der Meijden	Delft University of Technology
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Prof. ir. P. Vaessen	Delft University of Technology

This research was financially supported by China Scholarship Council (CSC).

Keywords:	Multi-terminal HVDC, HVDC converter, DC circuit breaker, Power system transients, Protection
Cover designed by:	Zhiwei Liu
Cover image source:	HVDC light valve hall © Copyright 2016 Photo: ABB
Printed by:	Ipskamp Printing, Enschede, The Netherlands

ISBN 978-94-028-1825-3

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

CONTENTS

SUMMARY

IN recent decades, the electrical power system has evolved into a new phase, in which the renewable energy resources are massively integrated into the grid. This change is mainly inspired by global policies that intend to reduce greenhouse gas emissions and decrease the society's reliance on fossil fuels by replacing them with sustainable energy sources. The good examples are the *European Network of Transmission System Operators for Electricity* (*ENTSO-E*) that intends to integrate a high degree of renewables in Europe's energy system, and the *West-East Electricity Transmission Project* that delivers wind energy from the northwest to the southeast of China.

One important technology used to connect renewable energy resources is the high voltage direct current (HVDC) system based on the voltage source converter (VSC). Aside from the simple point-to-point HVDC link, the multi-terminal HVDC (MTDC) system is another option to connect these remote energy resources. In the MTDC system, the generation units are usually unsynchronized turbines that are interfaced with power-electronic-based converters. As such, the responses of the MTDC system after faults occur are drastically different from the conventional AC systems that are based on synchronized generators. Since the development of an MTDC system is an important process, the research on the matter must be carried out.

In an electrical power system, the transient events refer to a system's response shortly after disturbances occur, such as the generation loss, the load shedding, the transmission line tripping, and the fault. This thesis focuses on the MTDC system's protection based on the system's transient events after faults. Due to the low impedance of the DC system and the low inertia of the HVDC converter, a fault in the DC system can spread quickly throughout both the DC and AC sides. Usually, the transient behavior of the HVDC system must be observed within several milliseconds, and it is a challenge to simulate the transient phenomena of a large HVDC system. The reason is that the accuracy of the electromagnetic transient (EMT) simulation heavily depends on how detailed the modeling system is: an extremely detailed system, such as one based on physical features of the semiconductor, cannot be modeled smoothly in the EMT application, while a too much simplified system cannot ensure accurate simulation results. Therefore, it means that a compromise must be made between modeling efficiency and accuracy. Consequently, this thesis implements an efficient method that ensures the efficient simulation of large-scale MTDC system and its accurate transient phenomena. By using this method, the responses of an HVDC link after faults occur can be determined. More importantly, they can be classified into different stages, and the thesis explains the mechanism of each stage. Furthermore, the thesis discusses the impact of grounding methods on the HVDC converter's post-fault responses.

Since the ultimate purpose of protection is to increase the reliability of the entire system, the concept of protection is divided into two aspects in the thesis:

1. Enhancing the robustness of each facility and component in the power system against faults.
2. Enhancing the functionality of the protective measures to clear the fault.

This thesis arrives at a feasible solution for each aspect. First, the MMC, which is the most crucial component in an HVDC system, is modified to become more tolerant towards DC faults. Although the modified MMC suffers from high power losses during partial-load conditions, a controlling method is proposed to deal with this problem so as to find a solution that makes HVDC technology more efficient and affordable.

In addition, since transient events are fast, powerful processing methods are needed to translate them into critical and useful information of the system. In the relevant chapter, the conventional Fourier Transform (FT), the short-time Fourier Transform (STFT), the discrete wavelet transform (DWT), the stationary wavelet transform (SWT), and the median absolute deviation (MAD) are compared to assess their performances when processing a typical fault current signal in an HVDC system. Afterwards, the appropriate techniques are determined to establish the fault detecting algorithms.

At the same time, since the characteristics of the fault must be generalized as the inputs of signal processing methods, the thesis analyzes the voltages and currents of healthy and faulty lines based on the traveling-wave theory, which is a well-known method used for the analysis of power systems with long transmission lines and cables. The voltage and current features are obtained in the Laplace domain and the time domain respectively, upon which the two protection methods based on the chosen processing methods are illustrated to "interpret" these features. Finally, according to their application ranges, these two protection methods are coordinated in the final protection scheme.

Working as an acting unit in the protection scheme, the DC circuit breakers (DCCBs) are the devices used to isolate the faults from the system. As such, the DCCB is also designed and modeled in the thesis. When embedding the DCCB into an HVDC protection scheme, the two following factors are considered:

1. The limits of the DCCB: The limits of a DCCB can be caused by its components' attributes, such as the potential breakdown of the capacitor and the quenching capability of the vacuum bottle. Although these limits are usually neglected in the system-level modeling, this thesis argues that they should be taken into account.
2. The rate of the DCCB: The DC system's voltage level and the DC fault current's range are the two main parameters determining the rate of a DCCB. A lower rate means that failure during fault clearance is highly possible, while a higher rate means that more resources are needed, such as an excessively large capacitor.

Upon considering these factors, a more practical design and calibration procedure for the DCCB is suggested in the thesis. These two factors are coordinated in the set-up of the protection scheme as well.

In the protection scheme, the primary protection consists of two parts. The first one is the DC line protection, which is composed of the above-mentioned transient-based protection methods and the second one is the DC bus protection, which implements a mature current differential protection. In addition, since the failures can occur

in the protection system, the backup protection is proposed in the scheme as well. In order to verify the protection scheme, a series of fault scenarios are simulated in the PSCAD/EMTDC environment.

SAMENVATTING

IN de afgelopen decennia is het elektriciteitsvoorzieningssysteem een nieuwe fase ingegaan, waarin duurzame energiebronnen massaal in het elektriciteitsnet geïntegreerd worden. Deze verandering is voornamelijk gebaseerd op mondiaal beleid dat beoogt de uitstoot van broeikasgassen te verminderen en de samenleving minder afhankelijk te maken van fossiele brandstoffen door deze te vervangen door duurzame energiebronnen. Goede voorbeelden hiervan zijn het 'European Network of Transmission System Operators for Electricity' (ENTSO-E), dat een grote hoeveelheid duurzame energie wil integreren in het Europese energiesysteem, en het 'West-East Electricity Transmission Project, dat windenergie van het noordwesten naar het zuidoosten van China transporteert.

Een belangrijke technologie die gebruikt wordt om duurzame energiebronnen aan te sluiten, is HVDC (High-Voltage Direct Current) gebaseerd op VSC- (Voltage Source Converter)-technologie. Afgezien van de eenvoudige 'point-to-point' HVDC-verbinding, is MTDC (Multi-Terminal HVDC) een andere mogelijkheid om afgelegen energiebronnen aan te sluiten. In MTDC zijn de productie-eenheden meestal asynchrone generatoren die aangesloten zijn via op vermogenselektronica-gebaseerde converters. Als gevolg hiervan verschilt de respons van het MTDC-systeem op netfouten drastisch van conventionele AC-systemen die gebaseerd zijn op synchrone generatoren. Aangezien de ontwikkeling van een MTDC-systeem een belangrijk proces is, moet onderzoek hiernaar worden uitgevoerd.

In een elektriciteitsvoorzieningssysteem verwijzen transiënte verschijnselen naar de respons van een systeem kort nadat zich verstoringen voordoen, zoals het verlies van productievermogen, het afschakelen van belasting, het uitschakelen van een transmissielijn of een netfout. Dit proefschrift richt zich op de beveiliging van het MTDC-systeem op basis van transiënte verschijnselen in het systeem ten gevolge van netfouten. Vanwege de lage impedantie van het DC-systeem en de lage inertie van de HVDC-converter, kan een verstoring in het DC-systeem zich snel naar zowel de DC- als de AC-zijde verspreiden. Gewoonlijk moet het transiënte gedrag van het HVDC-systeem binnen enkele milliseconden bestudeerd worden en is het een uitdaging om de transiënte fenomenen van een groot HVDC-systeem te simuleren. De reden hiervoor is dat de nauwkeurigheid van de simulatie van Elektromagnetische Transiënten (EMT) sterk afhangt van hoe gedetailleerd de modellering is: een extreem gedetailleerd systeem, zoals een systeem gebaseerd op fysieke kenmerken van een halfgeleider, kan niet eenvoudig gemodelleerd worden in EMT simulaties, terwijl een te veel vereenvoudigd systeem geen nauwkeurige simulatieresultaten kan opleveren. Dit betekent dat een compromis gesloten moet worden tussen de efficiëntie van de modellen en hun nauwkeurigheid. Daarom hanteert dit proefschrift een efficiënte methode die zorgt voor efficiënte simulatie van een grootschalig MTDC-systeem en de nauwkeurige transiënte fenomenen. Met behulp van deze methode kan de respons van een HVDC-verbinding na het optreden van netfouten wor-

den bepaald. Belangrijker is dat deze in verschillende stadia kunnen worden ingedeeld en dit proefschrift verklaart daarom het mechanisme van elk stadium. Verder bespreekt dit proefschrift de impact van aardingsmethoden op de respons van de HVDC-converter als gevolg van een netfout.

Omdat het uiteindelijke doel van netbeveiliging is om de betrouwbaarheid van het hele systeem te vergroten, is het concept netbeveiliging in dit proefschrift verdeeld over twee aspecten:

1. Verbetering van de robuustheid van elke faciliteit en elk component in het elektriciteitsvoorzieningssysteem tegen netfouten.
2. Verbetering van de functionaliteit van de beveiligingsmaatregelen om de netfout te verhelpen.

Dit proefschrift presenteert een haalbare oplossing voor elk aspect. Ten eerste is de MMC (Multi Modular Converter), het meest cruciale component van een HVDC-systeem, aangepast om toleranter te worden tegen DC-netfouten. Hoewel de aangepaste MMC aan hoge vermogensverliezen lijdt tijdens gedeeltelijke belasting, wordt een besturingsmethode voorgesteld om dit probleem aan te pakken om zo een oplossing te vinden die de HVDC-technologie efficiënter en betaalbaarder maakt.

Omdat transiënte verschijnselen kort zijn, zijn bovendien krachtige methoden nodig om deze te vertalen in kritieke en nuttige informatie over het systeem. In het betreffende hoofdstuk zijn de conventionele Fouriertransformatie (FT), de 'Short-Time' Fouriertransformatie (STFT), de 'Discrete Wavelet'-Transformatie (DWT), de 'Stationary Wavelet'-Transformatie (SWT) en de 'Median Absolute Deviation' (MAD) vergeleken om hun prestatie bij het verwerken van een typische netfoutstroom in een HVDC-systeem te beoordelen. Daarnaast worden de juiste technieken bepaald om de netfoutdetectie-algoritmen vast te stellen.

Omdat de eigenschappen van de netfout gegeneraliseerd moeten worden als input van signaalverwerkingsmethoden, analyseert dit proefschrift tegelijkertijd de spanningen en stromen van gezonde en defecte lijnen op basis van de 'traveling wave'-theorie, een bekende methode die gebruikt wordt voor de analyse van elektriciteitsnetten met lange transmissielijnen en -kabels. De spanning- en stroomeigenschappen worden bepaald in respectievelijk het Laplace-domein en het tijdsdomein, waarna de twee beveiligingsmethoden gebaseerd op de gekozen berekeningsmethoden als voorbeeld worden genomen om deze kenmerken te interpreteren. Ten slotte worden deze twee beveiligingsmethoden voor hun toepassing ingeregeld in het uiteindelijke beschermingsschema. De DC-vermogensschakelaars (DCCB's) vormen een cruciale schakel in het beveiligingsschema, omdat deze gebruikt worden om de netfouten in het systeem te isoleren. Als zodanig is de DCCB ook in dit proefschrift ontworpen en gemodelleerd. Bij het inpassen van de DCCB in een HVDC-beveiligingsschema worden de volgende twee factoren in overweging genomen:

1. De grenzen van de DCCB: De grenzen van een DCCB kunnen worden veroorzaakt door de eigenschappen van de componenten, zoals de mogelijke uitval van de condensator en de uitdovingscapaciteit van de vacuümkamer. Hoewel de limieten meestal worden verwaarloosd in de modellering op systeemniveau, betoogt dit proefschrift dat hiermee rekening moet worden gehouden.

2. De snelheid van de DCCB: het spanningsniveau van het DC-systeem en het bereik van de DC-foutstroom zijn de twee belangrijkste parameters die de snelheid van een DCCB bepalen. Een lagere snelheid betekent dat een storing tijdens het oplossen van netfouten zeer goed mogelijk is, terwijl een hogere snelheid betekent dat grotere middelen nodig zijn, zoals een te grote condensator.

Op basis van deze factoren wordt in dit proefschrift een meer praktische ontwerp- en kalibratieprocedure voor DCCB's voorgesteld. Deze twee factoren worden ook beschouwd in de opzet van het beveiligingsschema.

In het beveiligingsschema bestaat de primaire beveiliging uit twee delen. De eerste is de DC-lijnbeveiliging, die is samengesteld uit de bovengenoemde transiënten-gebaseerde beveiligingsmethoden en de tweede is de DC-railbeveiliging, die een volwaardige differentiaalbeveiliging vormt. Omdat fouten ook kunnen optreden in het beveiligingssysteem, is de reservebeveiliging ook in het schema opgenomen. Om het beveiligingsschema te valideren, is een aantal netfoutscenario's gesimuleerd in PSCAD/EMTDC-omgeving.

PREFACE

To my dearest family and friends.

Lian Liu
Delft, October 2019

1

INTRODUCTION

This chapter briefly introduces the history of the electrical power system. It reveals a trend and direction pertaining to the future of the electricity transmission system. While HVDC technology is in many ways superior to conventional HVAC technology, it brings about significant challenges which are also discussed in this chapter. Several key technical issues in the HVDC domain are illustrated, followed by the related research questions and methodology.

1

1.1. EVOLUTION OF ELECTRICITY TRANSMISSION SYSTEM

ELECTRICITY has been an important form of secondary energy in modern society since it has been commercialized in late 1870s [1]. During that time, electrical power was operated in a direct current (DC) system, driven by a steam-engine DC generator. The main limitation of the DC system at that time was that generators delivered power to short distances which because of the considerable power losses and voltage drop through the low-voltage circuits. After the inventions of the three-phase transformers and generators, the electricity industry evolved to rely on the alternating current (AC) system. By using the AC systems, the voltage levels can be operated and transformed more easily, thus implying that the electricity can be delivered to long distance with lower losses. Furthermore, the simpler and cheaper AC generators and motors facilitated the widespread usage of the AC system [1].

Although most existing electric power networks are still AC networks, the DC system became more prominent within the industry and academia since the invention and application of line-commutated converter (LCC) based on mercury arc valves. Since then, the development of a high voltage DC (HVDC) system has been feasible. After the advent of thyristor valves, the LCC converter has been able to achieve a higher voltage and power ratings with a reduced size and complexity. Therefore, this scientific advancement solved the aforementioned problem that had been haunting DC technology throughout the past century.

In recent decades, HVDC technology has markedly improved due to the creation of the latest full-controllable power electronic devices, i.e., gate turn-off thyristor (GTO) and insulated-gate bipolar transistor (IGBT). Unlike the thyristors that can only be turned on, the full-controllable devices can also be turned off. By utilizing this feature, a novel concept of AC/DC converters has been achieved in the form of the voltage source converter (VSC). More importantly, the VSC can realize local control of active power and reactive power, or AC and DC voltages due to its ability to be turned off. According to the Institute of Electrical and Electronics Engineers (IEEE) Transmission and Distribution Committee, over 150 HVDC transmission projects would be operated and planed by 2015 [2], and the number is still increasing, such as the projects COBRAcable [3] and NordLink [4] that will be commissioned by 2019 and 2020 respectively.

1.2. ADVANTAGES OF HVDC TECHNOLOGY

Modifying an electricity network is a considerable political and economic issue. It is inevitable that problems will arise when implementing HVDC technology, such as the construction costs of converter stations, the maintenance of delicate equipment, the long-term configuration of the transmission line system, and the environmental impacts among other things. However, the benefits brought about by this technology make it widely acceptable. When compared to conventional AC systems, HVDC systems, especially the advanced VSC-based systems, have the following economic benefits:

1. Higher efficiency

   In an AC system, power is transported by periodic voltage and current with certain frequencies, i.e., 50Hz or 60Hz. The reactive power transfer introduced by the phase difference between time-variant voltage and current occupies a part of the

transmission line capacity. In addition, the alternating current only flows through a path that is close to the surface of a conductor; this so-called "skin effect" increases the equivalent resistance of a conductor and results in a greater power losses. By contrast, the voltage and current in the DC system transfer constantly without periodic alternating, meaning that only active power is delivered and that the power loss is lower due to the absence of the skin effect and reactive power.

The quantitative comparison between two power transmitting methods is reported in [5]. Depending on the voltage level and construction details, HVDC transmission losses are quoted as being approximately 3.5% per 1,000 km, which are 30% to 40% less than that of AC systems at the same voltage level as shown in Figure 1.1. In the same figure, considering the terminal costs, line costs and losses, we can observe that after the Break-Even Distance, the total cost of employing a DC network becomes lower. On the other hand, the reactive power flowing in a long-distance AC transmission line becomes extremely high. This reactive power flow reduces AC voltage stability; thus, an excessively long transmission line or cable jeopardizes the power quality within a AC system. Consequently, if a remotely located power source is connected to the main power grid, it will be better to use a DC network.

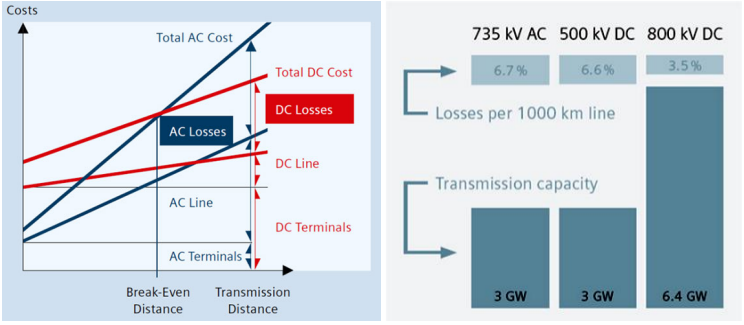

Figure 1.1: A comparison of the power losses and transmission distances involved with AC and DC systems [6]

2. Connecting different asynchronous AC systems

   There are two typical frequencies that are used globally when operating AC systems: 50Hz and 60Hz. The selection of working frequency differs in different countries, and it is impossible to directly link two unsynchronized systems together as they would totally collapse. Fortunately, this problem is solved by using the back-to-back HVDC technology which prevents the direct connection of different-frequency systems while ensuring the exchange of electrical power. Two good examples are the Rivera Back-to-Back HVDC Link interconnecting Uruguay (50Hz) and Brazil (60Hz) [7], and, the back-to-back system linking the western (60Hz) and eastern (50Hz) regions of Japan. With the help of HVDC technology, these countries and regions have a more robust electrical system.

3. Enhancing controllability and stability of a power system

1

First and foremost, providing a sustainable power supply is the most important task of a power system. It means a power system should provide consumers uninterrupted energy with manageable collateral effects [8]. The small signal stability, lack of reactive power supply, voltage stability, electromechanical oscillations, and transient stability are common challenges that can occur in networks that transmit a large amount of power over long distance transmission lines. Because of the independent control capability of active and reactive power, the use of VSC-HVDC systems in AC networks has proven to be an advantageous solution for these cases. By embedding VSC-HVDCs in AC grids, it is possible to enhance their stability and have greater control over power flow [9–11]. When linking two AC systems, HVDC connection can additionally guarantee the autonomy of each system. In fact, these advantages make it even more preferable to connect together the power systems of different countries or regions. For example, Figure 1.2 illustrate the numerous HVDC networks located in Western Europe.

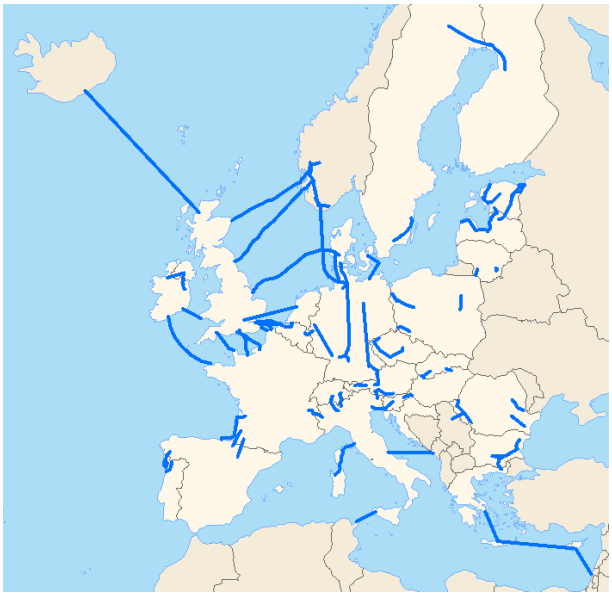

Figure 1.2: Some HVDC projects in Europe [12].

4. Smaller environmental impact

   Since global environmental problems are becoming more obvious, the power industry has been attempting to reduce greenhouse gas emissions,e.g. CO_2, by using renewable resources, such as energy supplied by wind power plants. HVDC technology offers an effective solution for integrating the renewable resources into the electrical network due to high controllability of HVDC. More importantly, given that the usage of the HVDC system results in low power losses, there would be less energy wasted. Consequently, this technology is also promising to decrease the CO_2 emissions in the countries that heavily depend on energy from fossil fu-

els. This is evident in the 1100kV, 3000km ultra-high-voltage DC (UHVDC) link that transmits power from Xinjiang region in the northwest of China to the Anhui province in Eastern China [13].

Applying the HVDC system also involves using less land and reducing the visual impact of having multiple transmission lines. This is evident in Figure 1.3, where the right-hand image demonstrates that the DC system only requires half or one-third of the constructing area (right of way) that the AC system, depicted in the left-hand image, requires to achieve the same power rating and voltage level.

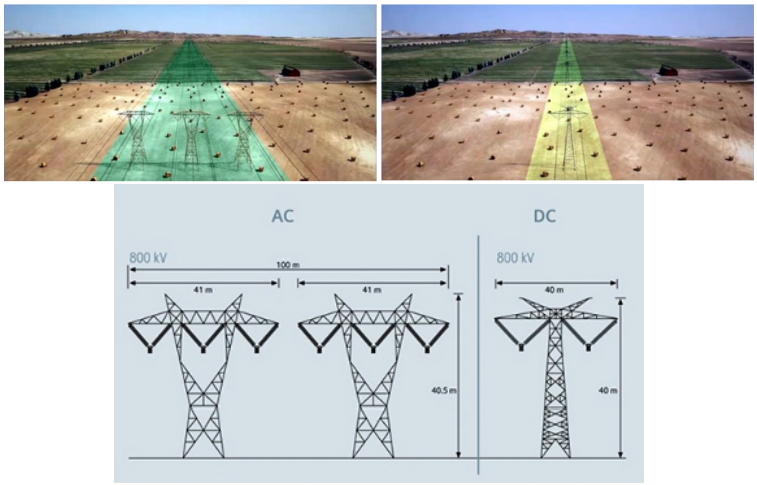

Figure 1.3: Comparing the landscape when AC and DC transmission networks are installed [6].

1.3. RESEARCH BACKGROUND

1.3.1. A PROMISING OPTION FOR THE FUTURE ELECTRICAL POWER SYSTEM

The above-mentioned advantages have made electrical industries all around the world consider HVDC technology as an important solution for building the future electricity network. The independent controls of VSC on active and reactive powers have better enabled the realization of the multi-terminal HVDC (MTDC) network. The application of the MTDC aims at using HVDC converters to connect multiple AC systems or power plants through one DC network. In addition, the dependent controls of HVDC converters offers enhanced reliability and functionality [14]. As of year 2014, there have been three MTDC projects in China [15], with the most recent one being the five-terminal HVDC project in Zhoushan, commissioned by the State Grid in 2014. The project has designed ratings of ±200 kV, 400/300/100/100/100 MW, and has electrically linked a series of small islands in the city of Zhoushan to the mainland. The future MTDC transmission networks, such as the North Sea Transnational Grid for the integration of offshore renewable power sources at large quantities and farther distances, will further improve trade, enhance competition, and contribute to the security of supply to the onshore end users [16].

At present, the VSC is classified as the two-level converter, the three-level converter and the modular multilevel converter (MMC), whose configurations have different arrangements of power electronic devices. One concern about the two- and three-level converter is their harmonic injection, which is caused by their pulse width modulation (PWM) methods based on the area equivalence principle. This issue is improved tremendously by MMC technology, which adopts modulation techniques such as step firing PWM and shifted-carrier PWM. The resulting power losses of the MMC (at around 1%) are lower than those of the two-level counterpart [17–19]. Additionally, because a direct series-connection of IGBTs or GTOs is not necessary, the MMC does not need the gate drives as sophisticated as those of the two and three-level converters. Therefore, the firing circuits of MMCs would have higher reliability.

1.3.2. TECHNICAL SOLUTIONS FOR PROTECTING MTDC NETWORK

During DC faults in an HVDC system, the converters become uncontrollable diode bridges when the GTOs or IGBTs are switched off for self-protection. Take the configuration of a two-level converter in Figure 1.4 as an example, the anti-parallel diodes are exposed to DC faults. The figure also demonstrates that the bridge now allows fault current to flow through both the AC and DC sides. As the diodes have a close-to-zero resistance, the current discharged from the AC to the DC side rises until it reaches an excessive value that cannot be sustained by the diodes. Eventually, a series of problems occur due to this situation, which includes the fact that [20]:

- The uncontrollable converter makes power transmission impossible.
- The short circuit on the DC side eventually causes the AC system to collapse due to the uncontrollable bridge.
- The short-circuit currents are too high for the diodes which will be damaged after a certain period of time; although the fault can be cleared by an AC circuit breaker, these electronic elements cannot survive the clearing time because it is always longer than 10ms.
- In MTDC systems, all system components contribute to the fault current; thus, an unacceptable level of overcurrent stress is imposed on the system.

Therefore, these challenges should be addressed in the following topics related to MTDC protection, which are of interests within both the industry and academia:

1. Novel VSC HVDC converters

   The AC/DC converters play a significant role in operating the power systems: they control power flow, balance DC voltage, and can support an AC grid or even passive loads. Thus, improving their defense against DC faults is necessary to ensure the power system's availability. At present, the full-H bridge (FB) MMC, together with other variants described in [22], can totally isolate the DC faults because of their specific configurations. However, the requirement of installing a large number of power electronic devices can result in high switching losses, and it hinders the widespread application of FB-MMCs. The requirements of power electronic devices per phase by different MMC configurations are summarized in [22], which

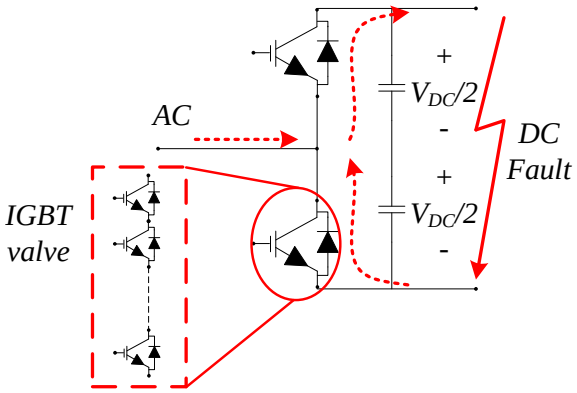

Figure 1.4: The fault current path of an IGBT-based two-level converter during fault (only one phase is shown). [21]

shows that the half-H bridge (HB) MMC requires the least number of these devices. Due to economic reasons, research is also conducted on the novel fault-tolerant converters [20, 23]. Although these converters cannot totally isolate the faults, they can decrease the peak fault current and shorten the duration of overcurrent, thus a lower level of overcurrent stress. As such, it is much easier to isolate a lower level fault by using other devices or mechanisms, such as DC circuit breaker (DCCB), which is another significant topic in HVDC domain.

Besides the configuration, the controlling philosophies of VSCs need to evolve, as new control loops are necessary to support the successful operation of the new converter configurations. For example, regarding the MMC, different circulating current suppression controllers (CCSCs) are demonstrated respectively in [24–26] to eliminate circulating currents within three phases. Another example is the complex inner loop controller of the hybrid MMC that can suppress circulating current [22]. In the meantime, the modeling methods of complex VSC need to be upgraded as it would otherwise be too difficult to simulate a large number of power electronic devices simultaneously.

2. Fast DC circuit breakers

   The circuit breakers (CBs) are widely used to clear the faults in traditional AC systems, i.e. AC circuit breaker (ACCB). Furthermore, the concept of CB has been expanded into the domain of the HVDC power system [27]. Unlike the AC system, the DC current and voltage have no zero-crossing points that are essential to interrupt the fault. Therefore, DCCBs must create a zero-crossing point for the sake of establishing a robust HVDC network, and the acting time of DCCB has to be fast.

   The typical configuration of a mechanical DCCB is depicted in Figure 1.5 [28]. In addition, the advanced hybrid DCCB (Figure 1.6) has been achieved by ABB Group [29]. While the former usually operates slower than the latter, the operating time of a mechanical DCCB can be improved using new technologies [28]. By contrast, the hybrid DCCB has an ultra-fast current interrupting capability and the negligible

conducting losses. However, as a common drawback of applying semiconductor devices, hybrid DCCB's high price makes it less favorable.

Working as a DC transformer [30], the DC/DC converters can be used to isolate DC faults as well [31]. However, they are not considered as DCCB in the thesis. The reasons are:

- The DCCB is enough for clearing faults in the MTDC system modeled in the research.
- The DC/DC converters are more favored in large-scale MTDC systems for the power and voltage regulations, e.g., 11-terminal HVDC system by the International Council on Large Electric Systems (CIGRE) [32].

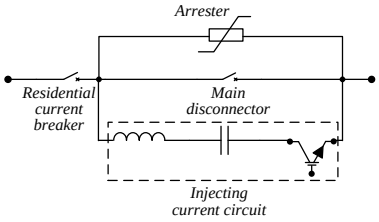

Figure 1.5: Mechanical DCCB [28].

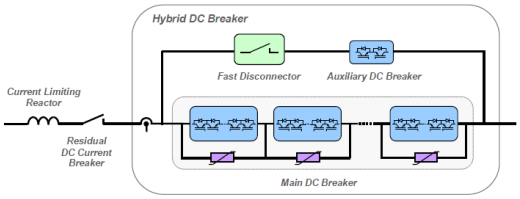

Figure 1.6: Hybrid DCCB by ABB [29].

3. Reliable protection schemes

The present protection methods are insufficient to protect HVDC systems from fast-propagating DC faults. This is because traveling-wave protection and voltage derivative protection are not sensitive to the high-impedance ground fault; the differential protection introduces a long time delay, while under voltage protection has low reliability. These protection methods are reviewed and summarized in [33], and they cannot satisfy the requirements needed to have a reliable HVDC system.

Although the distance protection in [34] provides an opportunity to identify the fault, the accurate fault location (or distance) cannot be obtained through this method. This is because that this method uses the finite impulse response filters (FIRs) to curve fit the time-domain expression of transmission lines, and these filters introduce errors especially when the fault is close to the remote end [34].

There are also boundary protection methods in [35–38]. On the upside, they have remarkable time responses, but on the downside, these transient-based methods may malfunction if lightning strikes. A fast protection and fault location method based on the rate of change of voltage (ROCOV) is proposed in [39]. However, the ROCOV would be impacted by the sampling frequency and noise in the signal. Therefore, it is necessary to develop better protection methods for HVDC systems, so that their reliability can be enhanced.

1.4. RESEARCH QUESTIONS AND METHODS

The key research question asked in this thesis is ***"How to protect an MTDC system in a reliable and selective manner?"***. The answers to this question should serve the purpose of establishing a protection mechanism that can function consistently when a fault condition occurs (reliable) while only isolating the faulty section in a power system (selective); thus, any unwarranted, false trips should be avoided [40]. As the protection issue should be considered thoroughly and cautiously, the research is dedicated to a methodology for planning an MTDC network from the selection of the converter to the set-up of the protection scheme. More specifically, this question has been divided into five sub-questions in order to obtain in-depth results, and based on the results in [41] the time frame of the transient signals being analyzed in the five sub-questions is 10ms after the fault's occurrence, as this is the most important time scope for the protection of power electronic devices. The five sub-questions are as follows:

1.4.1. WHAT IS AN APPROPRIATE AC/DC CONVERTER CONFIGURATION TO ESTABLISH AN MTDC NETWORK?

As mentioned before, the VSC-type converters have outstanding controllability of active and reactive power. Therefore, it can support both DC and AC systems. Nevertheless, in order to support a sustainable system, the converters should also have other important capabilities such as higher power transferring efficiency, higher fault tolerability, and lower device requirements. These features can be designed by certain converter configurations.

Among the available configurations, the HB MMC has been selected as an object of study because of its high efficiency during power transfer and its near-to-zero AC harmonic impacts on normal operation. On the other hand, modeling HB-MMC-based MTDC network is no longer problematic in electromagnetic transient (EMT) applications because of the efficient modeling method of MMC [32, 42]. As such, this enables the study of multi-terminal MMC-based network. The other types of MMCs are not considered, because they demand much more devices than the HB-MMC, even though they can isolate faults from both the AC and DC sides, e.g., the FB MMC requires twice as many power electronic devices as HB-MMC [22] does.

Although the HB-MMC is very efficient, its original design cannot isolate DC faults. This begs the question: what can be done to the HB-MMC configuration to improve its resistivity against DC faults? To obtain convincing results, the converter has been modeled in EMT application (PSCAD/EMTDC) while following the parameters from CIGRE documentation [32]. In addition, the cable model is achieved through the Frequency De-

pendent (Phase) Model [43, 44], thus taking into account more realistic traveling-wave phenomena.

1.4.2. HOW TO DETECT DC FAULTS IN A FAST AND ACCURATE WAY?

Successful fault detection in the current or voltage is the precondition for activating the following protective process to clear fault, for example, in terms of the relays sending commands and the DCCBs interrupting fault currents. However, the MTDC system makes this challenging for a number of reasons. The major reasons include the complex topology of an MTDC network, the approximate light speed of a fault-introduced surge and the AC/DC converters' vulnerability against the surge in long duration.

Additionally, as there are inevitable delays generated during the protecting procedure (e.g., the algorithm's performing time, the signal's transmitting time in the channels, and the DCCB's acting time), when the fault-caused wave arrives at a converter, the protection must detect it and send command to DCCB within 2ms. Therefore, the detecting algorithm should be able to process the transient signal during this time frame without giving a false trip order.

At present, it has been found that the wavelet transform (WT) techniques, including discrete wavelet transform (DWT) and stationary wavelet transform (SWT), possess a good time-response when processing abrupt signals. Although it is widely used in video and audio processing [45–47], it has been introduced into fault detection [38, 48], as the similar time-varying features are shared with these fault signals. Another method is median absolute deviation (MAD) [49], which can locate the outliers in a discrete data series. In the meantime, the fault current and voltage waveforms contain data that have the same properties as those of outliers [50]. Hence, prompting the question: which one would be a more effective method to detect a fault quickly and accurately?

It is also important to determine the indicators of DC faults. In a typical point-to-point HVDC system, the transient information provided by either DC voltage or DC current is enough to indicate a fault surge due to the simplicity of the system's configuration. However, this begs the question: in a more complex topology of an MTDC system, what indicators are required to ensure a reliable fault detection?

1.4.3. HOW TO ENSURE THE PROTECTION'S SELECTIVITY?

Selectivity is an important requirement for a protection scheme, and it means a protection scheme should only isolate the faulty section, thus minimizing the affected area of a fault. For this reason, a power grid is divided into different protection zones, which are monitored through the use of corresponding protection relays that are only responsible for the faults in their own protection zones.

To achieve selective protection, the relays could communicate with each other to prevent maloperation from taking place. Nevertheless, the protection would need extra processing time as the signal cannot be transferred instantly, and its reliability is extremely low when the signal channels are lost. On the contrary, if the communication is abandoned, the protection should work independently as it completely relies on local information. Hence, it is important to research the question: what can be improved to guarantee the selectivity of the protection scheme?

1.4.4. HOW TO EMBED THE DCCB INTO THE PROTECTION SCHEME?

While blocking an FB MMC can isolate the faults simultaneously, it is not the best option because it disables all of the converter's functions, thus violating the system's availability. By contrast, DCCBs are more suitable as the main protective devices in a protection system because they can be operated based on protection's selectivity.

Although a protection scheme may be composed of different protection methods for certain protection zones, and the faults in these zones possess unique features, the DCCBs need to comply with all of them. This means that the design of the DCCB must be customized accordingly, such as by being bidirectional when it is required in both DC line and DC bus fault interruptions [51]. Additionally, the DCCB has its own component-related limits. For instance, as an important category of active DCCBs, the vacuum CB's successful fault interruption relies on the *di/dt* of injected current at interruption instant as the vacuum switch can only extinguish the arc when *di/dt* is within a critical range [52, 53]. Due to these limits, the DCCB's operating range of fault currents must be defined well to ensure that it can successfully interrupt faults after receiving the command from a higher level control in the protection scheme, e.g., a fault detecting unit. Therefore, it is important to investigate how to coordinate DCCBs and protection scheme.

1.4.5. WHAT IS THE IMPACT OF GROUNDING METHODS?

In two and three-level converters, the capacitors must be installed on the DC side, storing energy during the power transfer and thus maintaining the DC voltage. In opposition to this, the multi-level converters do not need them due to their bridge configurations: the energy is stored evenly in the cell capacitor of each sub-module (SM). Therefore, installing extra capacitors on the DC side of MMCs does not aid its normal operation.

However, when the DC capacitors are implemented on the DC side of MMC converters, their midpoint can serve as a grounding point. Since there is no available standards for the DC side grounding in HVDC systems, the possible grounding options deserve analysis, such as grounding through a resistor, a capacitor, or an inductor. Consequently, the discharge of DC capacitors in both pole-to-pole and pole-to-ground faults would change the responses of the system. As the protection scheme is based on the analysis of these responses, questions arise: what is the impact of grounding methods on these responses? Furthermore, how to improve the protection scheme if the grounding method have an adverse impact?

Although it is not applied in practice, the solid grounding of a symmetrical monopolar MTDC system [54, 55] is considered to be a point of reference in the thesis. This grounding method is applied to calibrate the protection scheme, while other types are used to test the calibrated scheme. As such, the protection scheme should be readjusted accordingly.

1.5. OUTLINE OF THE THESIS

The outline of this thesis is as follows:

Chapter 2 introduces the VSCs with respect to their working mechanisms, configurations and control methods. Then, the chapter analyzes the responses of VSC converters to DC faults occur with regard to pole-to-pole and pole-to-ground faults. The

responses of the converter stations determine specifications of the protection system as it is understandable that the post-fault behaviors differ according to the different converter configurations. Besides this, the grounding method is discussed due to its impact on the currents and voltages after faults. They are also important inputs when calibrating protection schemes. In this chapter, the HB-MMC-based point-to-point HVDC system is modeled in PDCAD to demonstrate the fault simulation due to its high efficiency and promising application.

Chapter 3 briefly reviews state-of-the-art VSCs, especially those that are able to block and tolerate faults. Then a fault-tolerant LCL MMC is presented, followed by an optimized control of this converter. The purpose of this controlling method is to decrease power losses under partial loads while maintaining its ability to suppress fault current.

Chapter 4 analyzes three methods to process fault-incident transient signals. A four-terminal HVDC network is modeled based on the LCL MMC described in Chapter 3. Then a fault scenario is carried out with this MTDC network, and the data of a fault current are collected. With the obtained transient signal, the Fast Fourier Transform (FFT), discrete wavelet transform (DWT), stationary wavelet transform (SWT), and median absolute deviation (MAD) techniques are discussed according to their abilities to process these transient signals. They are evaluated based on two criteria: the first one is the time it takes to detect disturbances in signals as high signal-processing efficiency can facilitate the fault clearance, and the second one is the characterization of the disturbance, as it is otherwise difficult to set the necessary threshold.

Chapter 5 discusses two fault detecting methods under the MTDC circumstances. For the sake of selectivity, the criteria for distinguishing between faults in and out of a defined protection zone (i.e. internal fault and external fault) are proposed based on the features of WT and MAD techniques. After determining their respective thresholds, two sets of protection are proposed, and their performances are discussed in relation to different fault scenarios. Additionally, according to the concept of unit protection, it is assumed that the relays of DWT-based protection are communicated through fiber optic, and the introduced time delay is calculated with a speed of 200km/ms. In an attempt to protect the DC bus, the current differential protection is introduced, and its time responses to internal and external faults occur are analyzed.

Chapter 6 demonstrates the design of the mechanical DCCB. To ensure reliable DC-side fault interruption, the critical di/dt of the injecting current is accounted when dimensioning the circuit breaker. An algorithm is suggested in this chapter, which is used to obtain optimized component sizes in a DCCB. At the same time, the design considers using DCCB to interrupt load current, which is necessary for the purpose of maintenance in practice. The effectiveness of the proposed mechanical DCCB and the optimizing algorithm is verified in this chapter as well.

Chapter 7 reviews the ideas of the previous chapters and puts forward a comprehensive protection strategy. According to the configuration of modeled system, the primary protection and backup protection are decided to protect the DC line and the DC bus. The considered DCCB is the one that has been previously explained in **Chapter 6**. A series of fault scenarios are further applied to test the robustness of the protection scheme. Lastly, the simulations are carried out using both PSCAD/EMTDC and Real Time Digital Simulator (RTDS) platforms, and the simulation results are discussed in detail.

Chapter 8 concludes the thesis and discusses the proposals for future research.

1

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2

THE MMC AND ITS RESPONSE TO DC FAULTS

Although LCCs are classic and still in operation for numerous HVDC projects, their controllability is not high enough to support an MTDC network. After years of development, HVDC technology has made become more advanced due to the invention of the VSC-type converter that can locally control the power flow and voltage. The more independent control makes VSC-type converters more suitable for the building of an MTDC grid. As such, this chapter introduces and discusses the application and function of VSC-type converters. The post-fault responses of an MMC-based point-to-point HVDC network are also analyzed, which considers pole-to-pole and pole-to-ground faults. Furthermore, the impact of grounding methods is also discussed.

2.1. A BRIEF OVERVIEW OF VSC TECHNOLOGY

DUE to the application of high power full-controllable switches (GTOs and IGBTs), VSC-type converters are considered to be the most advanced ones which have evolved from two and three-level converters to MMC converters. The two or three-level converters are designed as PWM controlled voltage sources. Usually, IGBTs are designed to be connected in series within a valve on each converter arm and are switched on or off at the same time to create the square voltage wave. The width of the generated square wave is in accordance with the principle of equivalent areas. The configuration of two-level VSC is demonstrated in Figure 2.1, where it only shows one phase that consists of two arms: upper and lower arms.

By contrast, MMCs use series-connected SMs of HB [1] [2] or FB [3]. By design, the capacitors of SMs that are located on each arm are inserted or bypassed in every switching step in order to closely approximate the sinusoidal waveform. A special balancing algorithm is required to maintain one SM capacitor's voltage as a constant and as equal to the others' as possible. Figure 2.1 also depicts the configuration of HB-MMC, which has two arms in one phase as well. The number of SMs on each arm defines the level of an MMC, i.e. ***N*** SMs means ***N+1***-level MMC [4].

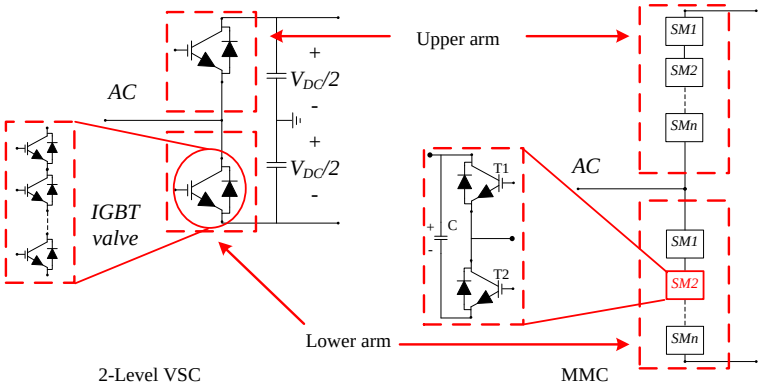

Figure 2.1: Configurations of two-level converter and HB-MMC. Only one phase is shown.

One advantage of using MMCs instead of other kinds of VSCs is that former only produces negligible high-frequency harmonics due to the high sinusoidal approximation. Therefore, having additional filtering may not be necessary. This is in contrast to the two-level converters which produce highly distorted voltage waveforms and rely on filtering to smooth out the voltage wave. Another advantage of utilizing MMCs is less switching losses. In two and three-level converters, all IGBTs are switched at frequencies close to the PWM carrier frequency (usually being thirty-three times that of the fundamental frequency). However, in MMC-based systems, the switching frequency of each IGBT is only between one to three times as much as the fundamental frequency. Thus, the gate firing system has higher reliability and effectiveness.

A typical VSC HVDC station is shown in Figure 2.2, including other basic elements besides VSC such as:

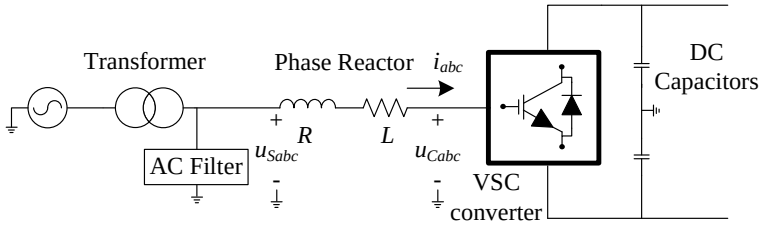

Figure 2.2: A typical VSC HVDC station.

- Phase reactors: They are required at VSCs' AC terminals to allow for active and reactive power control. In two-level VSCs, phase reactors are also sized to help limit the ripple current on the AC side caused by the PWM switching below an acceptable level.
- AC filters: Shunt high-pass filter branches are required to eliminate switching harmonics from the AC voltage, and they are essential to two and three-level VSCs. However, they may or might not be required in multilevel converters, depending on the number of steps and the size of the cell capacitors.
- Transformer: The transformer works as an interface between the VSC and the AC system. It is used to adapt the grid voltage to a suitable voltage level for the VSC. The transformer can also provide a second stage of ripple current attenuation.
- DC capacitors: The primary purpose of DC capacitors is to limit the DC voltage ripple within a predefined limit, particularly when PWM switching is applied. These capacitors are strictly necessary for the two-level converters, although they can be avoided in multilevel converters, since the cell capacitors in SMs on the six arms have already served as storage elements on the DC side. The DC capacitor can also function as a storage element that helps maintain the power balance during transient events.

2.2. THE OPERATING PRINCIPLE OF AN MMC

In this dissertation, the HB-MMC is modeled to establish an MTDC network because of its high efficiency. The HB sub-module of this type of converter is depicted in Figure 2.1. The T1 and T2 are two IGBTs that control the bypassing or the inserting of the capacitor within an SM, in which case the output voltage of the SM is either 0 or the capacitor voltage V_C. During the insertion, the AC current flows through the capacitor and T2, or its anti-paralleled diode, enabling the energy exchange. Meanwhile, during the bypass, the AC current flows through T1 or its anti-paralleled diode. These two states together with their output voltages are depicted in Figure 2.3. The block state is in use only for the initial capacitor charging state, or for protection purposes during the AC or DC faults. When this happens, the current can only flow through two anti-paralleled diodes, whose conducting states depend on external circuit.

It is important to note here that the diode anti-paralleled with T1 provides a path for the alternating current when an SM is bypassed, while that with T2 offers a charging path for the capacitor, which is not an ideal voltage source. The increasing voltage shown

in Figure 2.3 illustrate the process of charging as well, which is regulated by a specific capacitor voltage balancing algorithm that is further explained in Section 2.3.2.

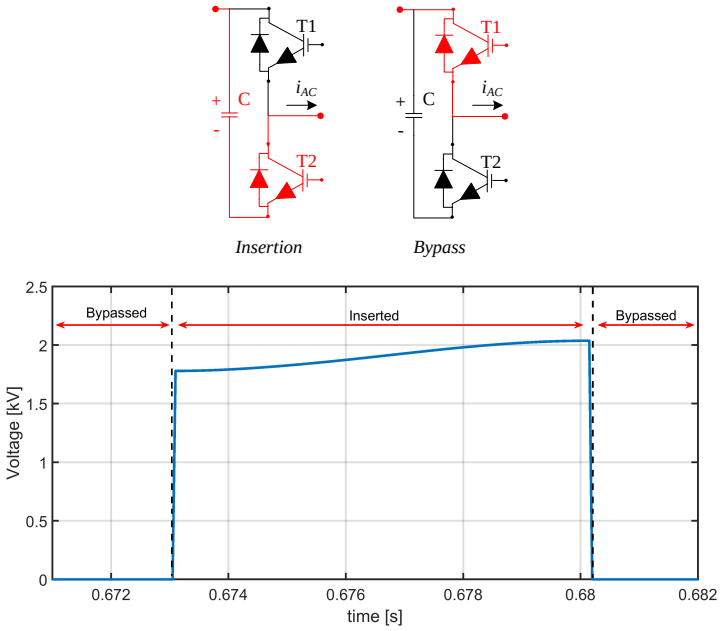

Figure 2.3: Performances of an SM during the inserted and bypassed states.

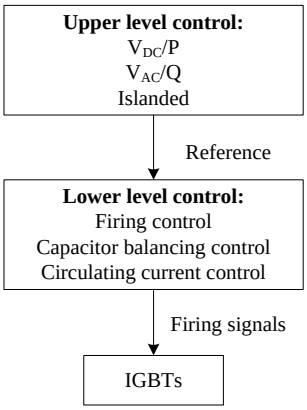

Figure 2.4: Two-level control of MMC.

2.3. CONTROLLING AN MMC

In this dissertation, the two-level control for the VSC [5] is implemented. The upper level of this control generates the reference voltage wave depending on the VSC's con-

trol mode, such as its DC voltage/active power, AC voltage/reactive power and islanded control mode. Based on the higher hierarchical reference, the lower-level control provides valve firing signals and ensures that each cell capacitor's voltage remains constant and in compliance with a predetermined value. The schematic of the two-level control is depicted in Figure 2.4.

2.3.1. UPPER-LEVEL CONTROL

NON-ISLANDED CONTROL

In this control, the VSC regulates the active and reactive powers flowing through its bridge. The reference is generated by making use of the vector control philosophy, which can be explained by investigating the AC side of the HVDC station as shown in Figure 2.2. Then, we can obtain the equation based on Kirchhoff's voltage law (KVL):

$$L\frac{di_{abc}}{dt} = -Ri_{abc} + u_{Sabc} - u_{Cabc} \tag{2.1}$$

By multiplying the matrix of Eq. 2.2:

$$P = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.2}$$

on both sides of Eq. 2.1,the three-phase system quantities can be transformed into *dq* system quantities:

$$\begin{cases} L\frac{di_d}{dt} = -Ri_d + \omega Li_q + u_{Sd} - u_{Cd} \\ L\frac{di_q}{dt} = -Ri_q - \omega Li_d + u_{Sq} - u_{Cq} \end{cases} \tag{2.3}$$

This Park Transform [6] facilitates the controls in the AC system with rotating coordinates.

If the VSC output voltage is assumed to be determined by the proportional integral (PI) controller, then there would be:

$$\begin{cases} u_{Cd} = -\left(K_p + \frac{K_I}{s}\right)\left(i_{d\_ref} - i_d\right) + \omega Li_q + u_{Sd} \\ u_{Cq} = -\left(K_p + \frac{K_I}{s}\right)\left(i_{q\_ref} - i_q\right) - \omega Li_d + u_{Sq} \end{cases} \tag{2.4}$$

Then, substituting Eq. 2.4 into Eq. 2.3 yields:

$$\begin{cases} L\frac{di_d}{dt} = -\left[R - \left(K_p + \frac{K_I}{s}\right)\right] i_d - \left(K_p + \frac{K_I}{s}\right) i_{dref} \\ L\frac{di_q}{dt} = -\left[R - \left(K_p + \frac{K_I}{s}\right)\right] i_q - \left(K_p + \frac{K_I}{s}\right) i_{qref} \end{cases} \tag{2.5}$$

In Eq. 2.5 the superscript *ref* means reference values or the set point of i_d and i_q, and it is obvious that i_d and i_q are decoupled. Therefore, based on Eq. 2.4, the decoupled inner current PI controller of upper level control can be represented in Figure 2.5. In this figure, the phase-lock loop (PLL) is used to align phase A with the d axis and obtain AC grid frequency. The outer controller is also shown, and it is used to generate the reference currents automatically based on a user-defined MMC operating mode: the

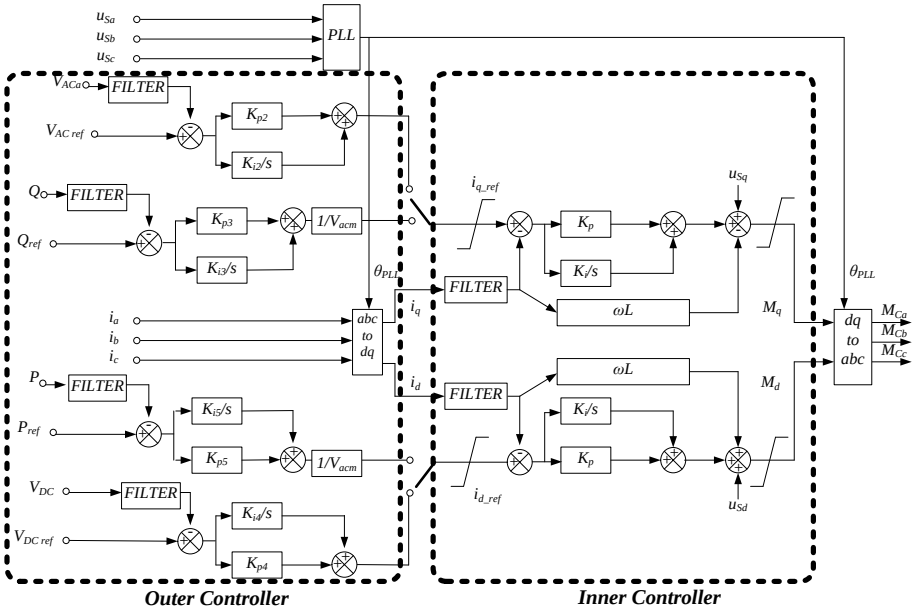

Figure 2.5: Non-islanded upper level control of an MMC.

i_{dref} is controlled by either the active power loop or the DC voltage loop, while i_{qref} is controlled by the reactive power loop or the AC voltage loop.

In the active power control loop, the changing rate of the power order (P_{ref}) should be limited to a pre-specified slope so as to achieve a stable response from the controller. Similarly, the filters are designed to apply ramps to any changes in the DC voltage, the AC voltage, and the reactive power orders. Additionally, as a part of the V_{DC} control mode, a voltage droop factor can be integrated into the control loop, although this is not shown in Figure 2.5. When the droop is activated, it will determine the power sharing and voltage levels of the terminals. In general, these two loops help to enhance the stability of the HVDC systems.

ISLAND CONTROL

This control is specific for the VSC that is used to support an islanded AC system with either passive loads or limited generation. This control also serves as a solution when a VSC is connecting a very weak AC system. Using this control, the VSC only generates an AC voltage waveform according to the user's specifications of frequency and amplitude.

Figure 2.6 shows the control loop of the islanded VSC, whereby the angle reference is generated by an oscillator that is unlike the PLL of a non-islanded control. This is because the purpose of island control is to provide stable voltage and frequency to the islanded AC system (otherwise it cannot be supported), while the non-islanded control aims to regulate the active and reactive powers between the AC and the DC systems. In addition, it is noticeable that the frequency droop is adopted when a VSC and the AC system connected to it have comparable generation capacities. Afterwards, the power

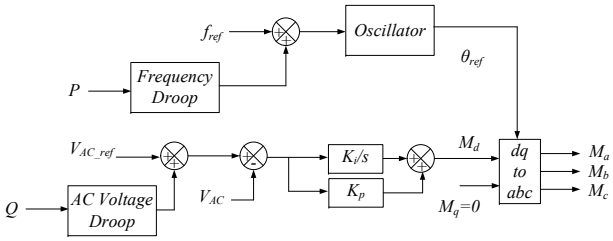

Figure 2.6: Island upper-level control of an MMC.

sharing can be coordinated between the VSC and the AC system. In addition, when a VSC is in islanded mode, and another one or more voltage-controlling units are connected to the same bus, the VSC needs an AC voltage droop to solve the conflict with other units pertaining to voltage control.

2.3.2. LOWER-LEVEL CONTROL

The objective of the low-level control is to provide firing orders to the IGBT cells so that a voltage waveform is reproduced according to the modulation indices from the upper-level control, while simultaneously balancing the cell capacitor voltages. This control strategy determines the IGBT's firing signals which are dependent on two factors: the requirement of inserting or bypassing an SM, and the direction of the current.

MODULATION TECHNIQUES

The task of initiating the order of insertion or bypass can be carried out by using different modulation techniques, with the most widely implemented ones being the step firing PWM [1] and the shifted-carrier PWM [2]. The former discretizes the sinusoidal voltage reference first, after which the firing orders are given whenever there is a step in the discretized waveform. Meanwhile, the latter uses shifted-carrier waveforms to compare with the reference waveform. Whenever the value of the reference is greater than that of the carrier wave, the order is given to insert an SM in the upper arm; whenever the reference value is lower, the SM in the lower arm must be inserted.

In Figure 2.7, a thirty-step firing PWM and a thirty shifted-carriers PWM are shown with sinusoidal references. The output waveforms of both techniques are in agreement with the sinusoidal references; it is understandable that using a higher level step or more shifted-carriers can generate a better approximate sinusoidal output voltage. The insets in Figure 2.7 reveal the difference between these two techniques when tracking the references. Due to that there are 200 SMs installed on each arm of the converter bridge in the modeled HVDC systems, these two modulation techniques have similar performances, and the step firing PWM is selected in all of the MMC models. Although there are other algorithms besides these two, including phase-decomposition PWM [7], space-vector PWM [8], and the improved selective harmonic elimination method [9, 10], they are not discussed.

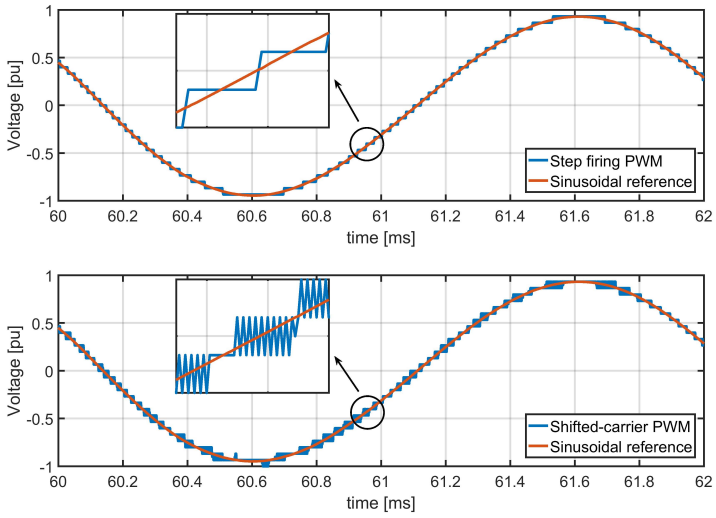

Figure 2.7: Performances of two PWM techniques.

CIRCULATING CURRENT SUPPRESSION CONTROL

In the lower-level control, the capacitor voltages of all SMs are regulated within an acceptable range. For example, the SMs with the lowest or the highest capacitor voltages are switched in according to the direction of an arm current. Since the regulated capacitor voltages are varied, there are circulating currents among the three-phase units. In [11], the circulating current phenomenon is investigated, showing that for different load phase angles, the circulating current is in the negative sequence, and its main frequency is the second harmonic of the AC system.

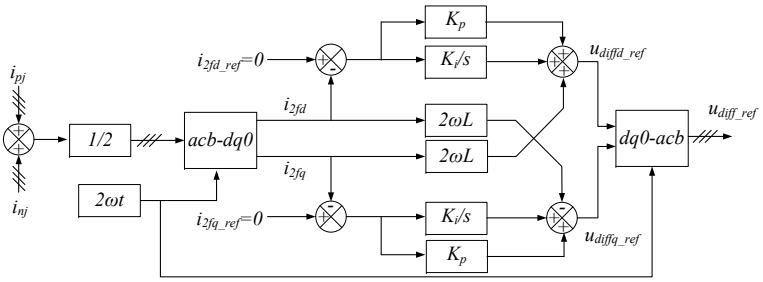

Figure 2.8: Circulating current suppressing control loop.

This current does not influence the currents of the AC and DC sides. However, it distorts the arm current and increases the rated current of the sub-modules, which negatively influences the performance through increasing the converter losses [12]. In order to reduce the effects of the circulating current, [13] introduces a circulating current

suppression control that is also applied in this dissertation. The corresponding control scheme is depicted in Figure 2.8. It is noticeable that the circulating currents flow in the negative sequence with a double line-frequency [12], transforming the three-phase currents from the *acb* to *dq0* system with $2\omega t$, as illustrated in Figure 2.8. The ω comes from the PLL in the upper-level control.

CAPACITOR VOLTAGE BALANCING CONTROL

The final stage of the lower-level controller is the capacitor balancing controller. During MMC applications, the voltages of the SM capacitors on one arm must be maintained at a similar level for the operation to succeed. Hence, the firing pulses must be generated cautiously.

A common method used to balance the SM capacitor voltages is the sorting method [14], which sorts out the SM capacitor voltages in one arm from the highest to the lowest magnitudes. Afterward, based on the modulation indices, the lower-level controller will insert the SMs with the highest voltages to allow them to discharge when the arm current is negative. By contrast, it will insert the SMs with the lowest voltages to be charged when the arm current is positive. In this way, monitoring and sampling the capacitor voltages at a sufficient frequency ensures that they are naturally balanced.

2.4. MODELING AN MMC

In order to analyze the transient phenomena, the VSC-based system is modeled in the EMT program which applies Dommel's algorithm [15, 16]. This algorithm intends to solve the following matrix equation:

$$[G]_{N\times N} \times [V]_{N\times 1} = [I]_{N\times 1} \tag{2.6}$$

in which $[G]$ is the conductance matrix of the whole network, $[V]$ is the vector of the given nodal voltages, and $[I]$ is the current vector. These matrices' sizes are determined by N that is the number of electrical nodes in the entire system. In each time step, the simulated system is divided into two sections: the matrices with subscript A which contain the nodes with the known voltages and those with B that contain the nodes with unknown voltages. As such, Eq. 2.6 is rearranged as follows:

$$\begin{bmatrix} G_{AA}G_{AB} \\ G_{BA}G_{BB} \end{bmatrix}_{N\times N} \times \begin{bmatrix} V_A \\ V_B \end{bmatrix}_{N\times 1} = \begin{bmatrix} I_A \\ I_B \end{bmatrix}_{N\times 1} \tag{2.7}$$

Taken from Eq. 2.7, the unknown voltage vector $[V_B]$ is obtained through the formula:

$$[G_{BB}] \times [V_B] = [I_B] - [G_{BA}] \times [V_A] \tag{2.8}$$

and it is recalculated in each time step. Although the inverse of the matrix $[G_{BB}]$ is not calculated directly, its size significantly influences the computation time of one time step, as it solves $[G_{BB}]^{-1}$ using the forward solution (or the forward triangularization as described in [17]) and the back substitution.

At present, there are six types of VSC models used in different grid studies [18], with the most simulating-efficient method to model MMC being the Type 4 model [16, 18–20]. The Type 4 model drastically reduces the electrical node number based on the

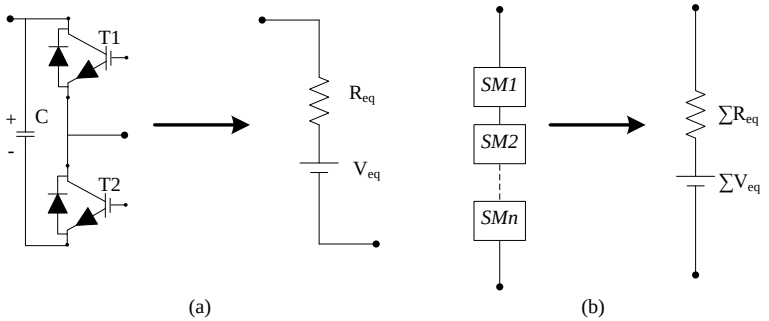

Figure 2.9: Efficient modeling of an MMC. (a) The equivalent circuit of one sub-module. (b) The equivalent circuit of one arm.

Model type	Relative computing time	Type of simulation tool	Type of studies
Type 1	NA	Circuit simulation tool	Not suitable for grid studies
Type2	1000	EMT	Detailed studies of faults in submodules; used to validate simplified models
Type 3	900		Detailed studies of faults in submodules; used to validate simplified models
Type 4	30		Detailed studies of AC and DC faults close to converter
Type 5	2		Studies of AC and DC transients: high level control system and design-harmonic studies
Type 6	1.5		Studies of remote AC and DC transients
Type 7	0.01	Power flow tools	Power flow

Table 2.1: Summary of model types [18]. Type 1: Full physics based models. Type 2: Full detailed models. Type 3: Models based on simplified switchable resistances. Type 4: Detailed equivalent circuit models. Type 5: Average value models based on switching function. Type 6: Average value models. Type 7: Power flow models.

Thevenin equivalent in Figure 2.9, which determines the nodal matrix size of the MMC. More importantly, this model still reveals the accurate impact of the capacitor in each sub-module. Thus, the simulation of an MMC-based multiterminal HVDC system is possible, and this type of model is consequently applied in this thesis. All the suitable fields of research pertaining to these models are listed in Table 2.1 [18].

2.5. RESPONSE OF AN MMC TO DC FAULTS

In reference [21], the two-level converter's behavior is analyzed for pole-to-pole and pole-to-ground faults. However, because of the different converter bridge configurations, the MMC reacts differently to DC-side faults. Therefore, it is necessary to analyze and comprehend the post-fault responses of the MMC, since they are fundamental to the design and calibration of the system protection.

2.5.1. RESPONSE TO A POLE-TO-POLE FAULT

The point-to-point MMC-based system (***DCS1***) published by CIGRE is implemented here as a case study. The configuration of this symmetrical monopolar system is depicted in Figure 2.10. In order to clearly explain the converter's responses, the DC capacitors are not installed, and more details of this system can be found in [18]. A permanent solid pole-to-pole fault is applied at 10ms, and its location is 100km away from converter Cm-A1. The two converters will be blocked when the DC current on either pole exceeds 6kA. The low DC voltage protection is not included in the model.

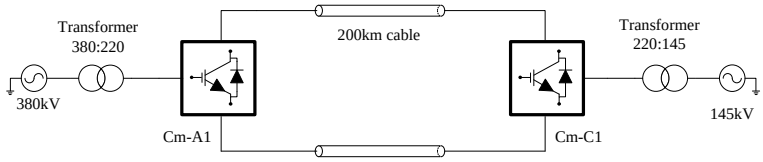

Figure 2.10: The configuration of the studied system: DCS1.

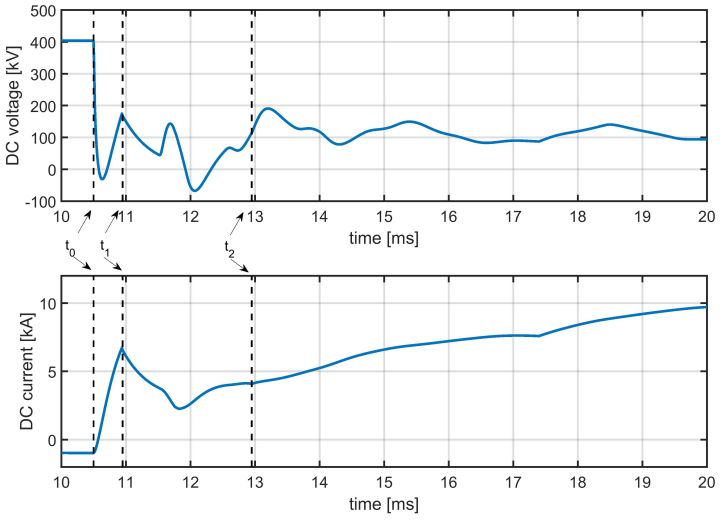

Figure 2.11: The DC voltage and current of converters after a pole-to-pole fault. t_0=10.5ms, t_1=10.95ms, t_2=12.9ms.

The positive pole current and the pole-to-pole voltage measured at the DC terminal of converter Cm-A1 are plotted in Figure 2.11. It is evident that the fault surge arrives at the converter terminal around t_0=10.5ms. Afterward, the current climbs to a high value, while the system voltage simultaneously and quickly drops to zero. The negative voltage in Figure 2.11 is caused by the minus *di/dt* during the propagation of the incident surge. If we observe the responses in more detail, there are three sub-stages:

1. Sub-module capacitor discharging (t_0<t<t_1)

   The t_1 is the blocking instant of Cm-A1, before which the capacitors in all sub-modules are forced to discharge. The voltages and currents of the top four sub-modules on the upper arm of phase A are shown in Figure 2.12. The discharging results in a rapid increase of current from t_0 to t_1. The increasing rate of current is impacted by the inductor elements, such as the arm inductor, DC current limiter, and the distributed inductor along with the transmission line or cable. Correspondingly, the voltage of each capacitor decreases despite the fact that the controller is still regulating all the sub-modules during this period.

   The blocking instant is determined by the pre-defined overcurrent and/or undervoltage protection philosophies. The former is related to the rating of applied sub-module, and the latter, although it is not applied in the case study, is activated when the DC voltage is lower than a predefined value (e.g., 0.8 per unit (pu)). It is noticeable that the capacitor voltages of SMs do not decrease to zero after blocking which means that the converter bridge is still in a charged state (although it is not fully charged). As the pre-charging of SM capacitors is a prerequisite for MMC's normal operation [22], the MMC can recover faster than two and three-level converters, since the uncontrolled DC capacitors in these two types of converters would discharge completely after the faults.

2. Arm current decaying (t_1<t<t_2)

   Even a converter is blocked, and the sub-module capacitors are bypassed, the arm currents, which now are residual currents from the first stage, cannot vanish immediately due to the electromotive potential on arm inductor. Therefore in this period, the arm current can only decay through the anti-parallel diodes (i.e., free-wheeling diodes), and the waveforms of the three upper arm currents are shown in Figure 2.13. It is also clear that the AC current starts to contribute at around 11.9ms due to the fact that two arm-currents decay to zero, which are the upper arm of phase C and lower arm of phase B if Figures 2.13 and 2.14 are to be compared.

3. AC current infeed (t>t_2)

   As mentioned above, the AC contribution begins when two arm-currents decay to zero. Furthermore, when the residual currents in three arms decrease to zero, the DC current is totally injected from the AC side. When observing Figure 2.13, it is evident that these three specific converter arms are the upper arm of phase A, lower arm of phase B, and upper arm of phase C. The AC infeed is shown in Figure 2.14 when t>t_2. At t_2, the DC current is equal to the AC current supplied in phase B. After t_2, the converter becomes a three-phase uncontrollable diode bridge.

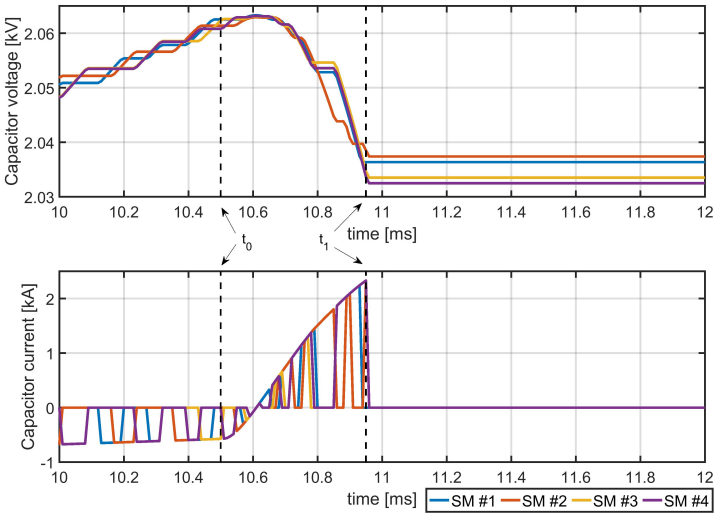

Figure 2.12: Discharging of SM capacitors. t_0=10.5ms, t_1=10.95ms.

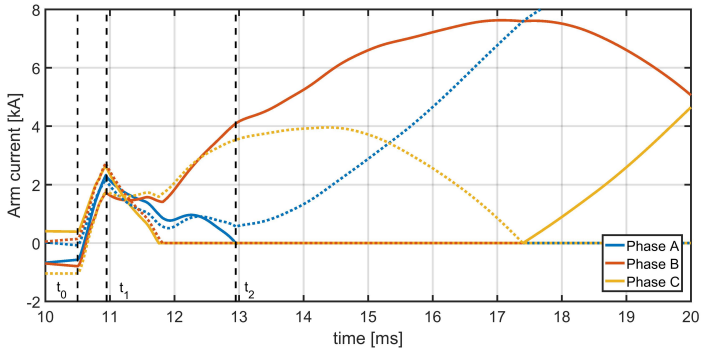

Figure 2.13: Arm currents during a fault (solid lines for upper arms, dotted lines for lower arms). t_0=10.5ms, t_1=10.95ms, t_2=12.9ms.

2.5.2. RESPONSE TO A POLE-TO-GROUND FAULT

The pole-to-ground fault occurs more frequently than the pole-to-pole fault, although the latter is much more severe. Similarly, a permanent negative pole-to-ground fault is applied in the system, which is same to the previous section, at a distance of 100km away from converter Cm-A1 at 10ms. The converters can experience the same three post-fault stages as those that take place during a pole-to-pole fault, as indicated in Figure 2.15, which shows the sub-module capacitor discharging stage (t_0<t<t_1), the arm current decaying stage (t_1<t<t_2), and the AC current infeed stage (t>t_2).

It is significant to point out that both the AC and DC currents depicted in Figure 2.15

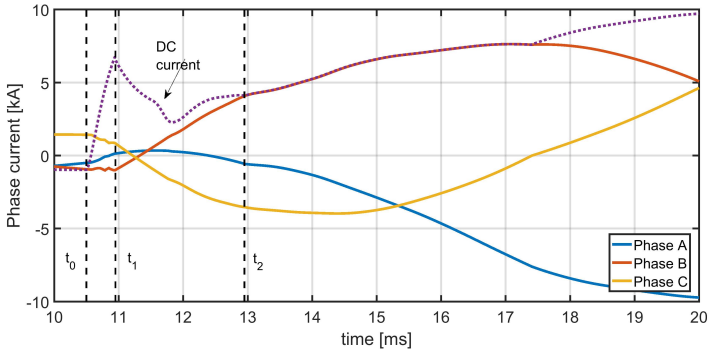

Figure 2.14: AC phase currents. t_0=10.5ms, t_1=10.95ms, t_2=12.9ms.

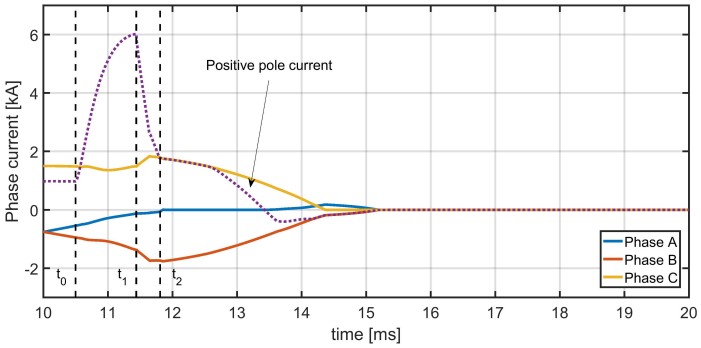

Figure 2.15: The converter's response to a pole-to-ground fault. t_0=10.5ms, t_1=11.44ms, t_2=11.81ms.

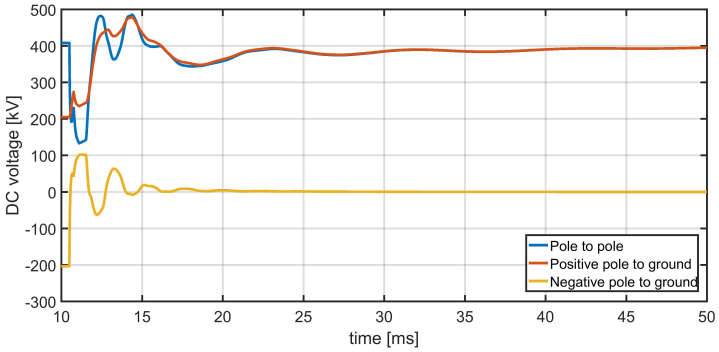

Figure 2.16: DC voltages responding to a pole-to-ground fault.

decrease to zero after a certain instant, which is 15.2ms. The main reason is that although the negative cable is short-circuited to the ground, the pole-to-pole voltage can

still be close to 1pu=400kV (i.e., the pole-to-pole voltage shown in Figure 2.16), which is higher than peak value of AC line-to-line voltage (V_{peak} = 220 kV * 1.41 = 310kV) and thus indicates that the freewheeling diodes are reverse biased. On the other hand, due to the same reason, the positive pole (the healthy one) has to endure a transient overvoltage of 1.1825pu (473kV), which is also evident in Figure 2.16. The gradual voltage increase of the healthy cable is caused by the energy exchange among the stray capacitance along with the DC line, the inductance in the converter station, the leakage inductance in the transformer, and the line inductance [23]. Consequently, a large amount of thermal energy is dissipated within the healthy cable, damaging the conductors and insulators. To counter this, the surge arresters are usually implemented at the remote ends of a line to absorb a certain amount of this energy [24]. In this way, the transient overvoltage can be limited to a safe level [23].

2.5.3. IMPACT OF THE GROUNDING METHOD

Currently, there are several options available when grounding an HVDC converter. These options vary according to the specific configurations of HVDC systems: a low impedance grounded asymmetric monopolar system, a high impedance grounded symmetric monopolar system, and a low or high impedance grounded bipolar system [25–27]. Although there are no clear choices for grounding a multi-terminal HVDC system [27], these choices can influence the cost of system, the design of protection system, and the extensibility of the grid. Moreover, the number of options increases significantly when considering all of the possible grounding methods, such as solid grounding, grounding through an impedance, or leaving the system ungrounded [28]. Some options of grounding methods are shown in Figure 2.17 [26], and it is important to research on all of them.

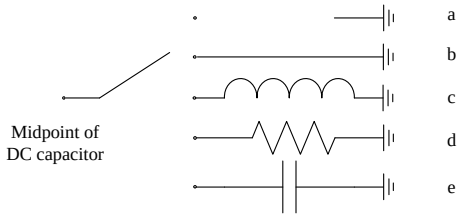

Figure 2.17: Basic grounding options: a. floating; b. solid grounding; c. grounding through an inductor; d. grounding through a resistor; e. grounding through a capacitor.

Although it is unnecessary for the applied symmetrical point-to-point MMC-based HVDC system, it is still feasible to install capacitors across the two poles of an MMC converter. The mid-point of DC capacitors provides a grounding point, like that shown in Figure 2.2, and the DC capacitors themselves must be taken into account when the system is grounded. In the following context, the DC capacitors are considered by default when discussing the grounding, with the capacitors linked on positive pole and negative pole being referred to as the positive DC capacitor and the negative DC capacitor, respectively.

The grounding method plays a significant role when there is a pole-to-ground fault, as there could be a path for fault current flowing through the DC capacitor, then the soil,

and finally back to the system. Here, based on [26, 27], the considered scenarios include floating (U.G.) with and without DC capacitors, solid grounding, resistance grounding (20Ω resistor), inductance grounding (50mH inductor), and capacitance grounding (6.5μF capacitor). Due to the high similarities between the floating and grounding through a high resistance, the latter is not considered.

The responses of ungrounded converter are depicted in Figure 2.18, where it is clear that the negative capacitor begins to discharge when a fault surge arrives at 10.5ms. The discharging current is dominant for the first peak of the fault current. Since there is no path through the soil, the negative capacitor can only discharge through the cables. Nevertheless, the maximal fault currents are similar in both shown cases as determined by the discharging of the SM. Due to the fact that the DC capacitor works as a voltage source during the fault, its transient voltage is directly superposed to the system voltage. Therefore, the healthy pole experiences a faster increase in voltage and a higher transient overvoltage.

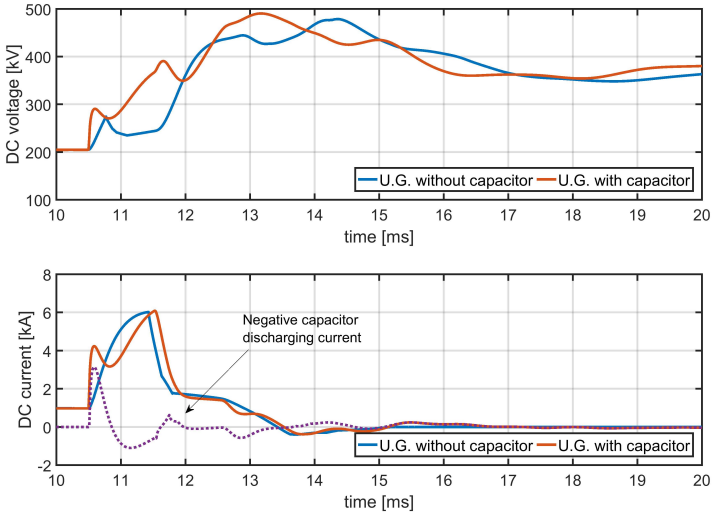

Figure 2.18: The impact of DC capacitors on an ungrounded system experiencing a pole-to-ground fault. Top plot: healthy pole voltage. Bottom plot: faulty pole current.

During the transient period after a pole-to-ground fault occurs, the energy exchange is inevitable in the system and is recognized by the oscillations that are shown in Figure 2.19. In the meantime, the inductor and capacitor elements in the system can only store electromagnetic energy and exchange it with external circuit, thus possible causing higher transient overvoltages, as illustrated in Figure 2.19 pertaining to the healthy poles in both the inductor and capacitor cases. Nevertheless, they are passive elements, so the voltages of these two cases eventually decrease to similar levels because of the presence of ohmic elements in the system. On the contrary, the solid grounding and resistance grounding have lower overvoltage stress.

Due to the DC capacitors in all of the considered grounding scenarios, the domi-

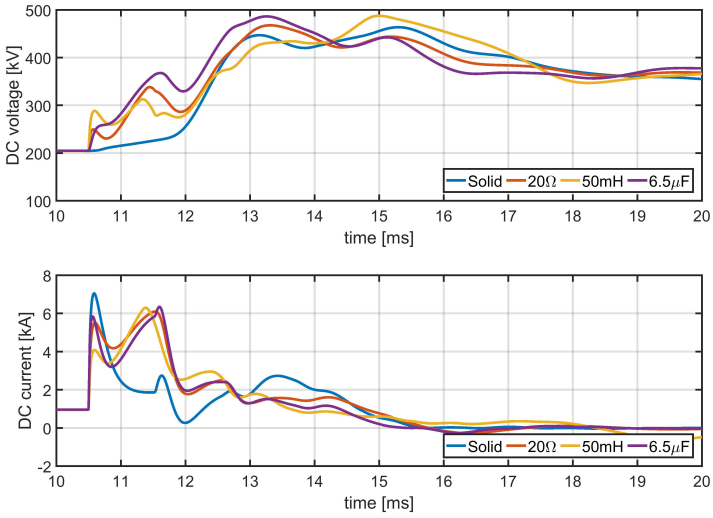

Figure 2.19: The impact of grounding impedance on a grounded system experiencing a pole-to-ground fault. Top plot: healthy pole voltage. Bottom plot: faulty pole current.

nant discharging takes place in the first peak of the fault current, as seen in the bottom graph of Figure 2.19. Specifically, the solid grounding can introduce the largest first peak current, because of the faster fault current increasing in solid grounding. However, this case has the lowest second peak current, because the converter can be blocked earlier, whereby the SM capacitor's discharging contributes less to the second peak current. By contrast, groundings through a resistor and an inductor, and a capacitor give larger second peak currents, since the former two can respectively restrain the current amplitude and its increasing rate, and the capacitor decreases the equivalent capacitance as it is in series with the negative DC capacitor in the pole-to-ground fault. Consequently, the discharging of SMs contributes more to the second peak current, which is also quite similar to the "U.G. with capacitor" case illustrated in Figure 2.18. After the early fast transients from 10-15ms take place, all four currents decay to zero over a longer period of time, as shown in Figure 2.20. It is intelligible that the inductor has an impact on the damping frequency, as opposed to the negligible impact of the resistor and capacitor.

In the case of a pole-to-pole fault, neither one of the grounding elements affects the response of the converter due to the absence of the discharging path through the soil, which excludes the grounding elements from the circuit during the fault. At this moment, the only crucial component is the DC capacitors. In Figure 2.21, the responses of the positive pole current and pole-to-pole voltage of MMC are traced in relation to a permanent pole-to-pole fault. It is clear that capacitors can help in stabilizing the DC voltage as its decreasing rate is lower after capacitors are installed. However, the fault current increases faster, as the first peak of current appears almost simultaneously when the incident surge arrives. It is evident that the discharging of the DC capacitor is dominant during the first peak, as shown in Figure 2.21, which is similar to the case of a

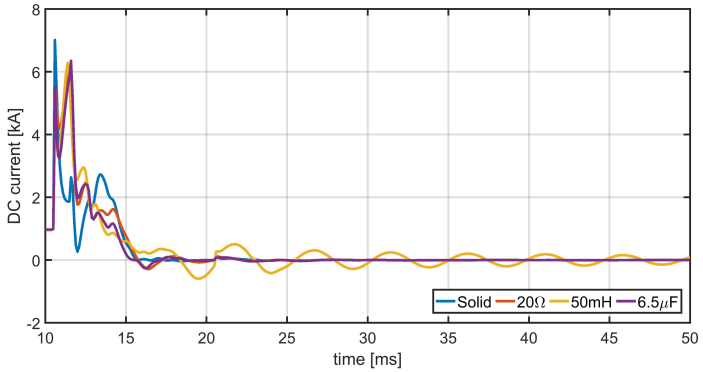

Figure 2.20: The faulty pole currents with different grounding impedances over a longer period of time.

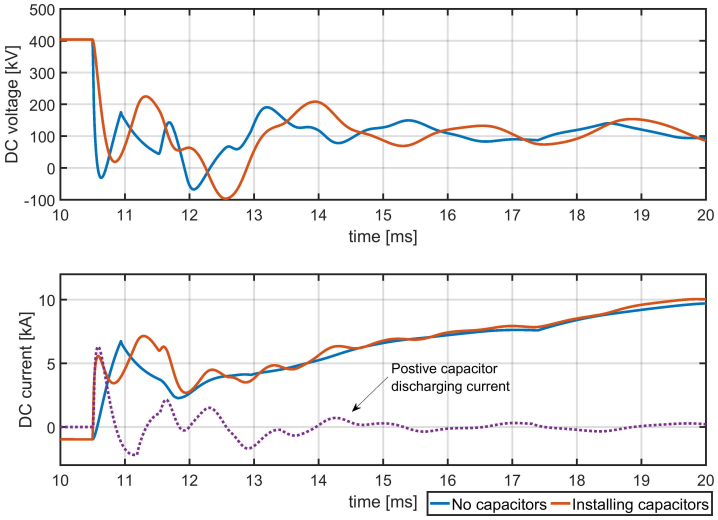

Figure 2.21: The impact of a DC capacitor under a pole-to-pole fault. Top plot: the pole-to-pole DC voltage. Bottom plot: the positive pole current.

pole-to-ground fault.

2.6. CONCLUSION

In this chapter, the MMC is introduced, and its configuration and controlling philosophy are illustrated. Although the MMC shares the same upper-level control with two- and three-level converters, its lower-level control is much more sophisticated in terms of the SM capacitor voltage balancing algorithm and circulating current suppression algorithm, which uniquely apply to the MMC.

In general, the post-fault response of an MMC can be categorized into three stages. The first stage is always dominated by the capacitor discharging. More specifically, when there are no DC capacitors installed, the SM capacitor discharging is the main factor that contributes to the initial peak current; when the DC capacitors are installed, their discharging causes the current to rise more steeply. In order to prevent the converter from being damaged by excessively high current, the converter must block itself. After the residual current of the first stage decays, the converter becomes an uncontrollable diode bridge. At this point of time, since the fault resistance is usually very small, the fault must be isolated from the system. Otherwise, the AC infeed could impose an incredible amount of current stress on the converter and cable.

According to the simulations, the pole-to-pole fault is the most severe type of fault that can occur, since both AC and DC systems can eventually collapse if the fault is not isolated. The converter is forced to endure an extremely high current due to the SM capacitor discharging and the AC infeed through freewheeling diodes. When the MMC converter is grounded, the DC capacitor's fast discharging makes the need of protection much more urgent.

For a pole-to-ground fault, the response of a symmetrical monopolar system is sensitive to the grounding elements. All the considered grounding methods can contribute to steep transient currents. Therefore, the protection may need to be adjusted and improved based on the attributes of all the components in an HVDC converter, such as the rating and heat dissipation of power electronics. Even though there is no steady state current during a pole-to-ground fault, the possible overvoltage stress requires that all DC lines sustain the rated DC system voltage and that the surge arresters are necessarily applied to limit transient overvoltage. Additionally, the rate of surge arresters must be increased when the HVDC system is grounded through an inductor or a capacitor.

So far, there is no practical grounded MMC-based system, yet the solid grounding system is chosen as a frame of reference to calibrate the protection scheme due to the lower overvoltages and faster DC current damping. Other methods of grounding can also be used to test the protection system after calibration.

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3

DESIGNING AND MODELING FAULT-TOLERANT MODULAR MULTI-LEVEL CONVERTER

Serving as the main energy conversion facilities in the HVDC networks, the VSCs' performances play a significant role in the functioning of the system. In the previous chapter, the post-fault behavior of an MMC is analyzed, whereby it is evident that faults need to be isolated in a very short period of time. In order to protect a VSC from DC faults, numerous novel solutions have been published concerning protection. This chapter provides a brief overview of the VSC technologies that can block and tolerate faults and presents an MMC with inductor-capacitor-inductor (LCL) passive circuit. More importantly, the power-lossless control strategy for this type of converter is determined accordingly.

3.1. A BRIEF OVERVIEW OF VSCS

BASED on the discussion of the post-fault behavior of MMC, it has been confirmed that HVDC systems require urgent protection. It is not suitable to clear the DC faults by opening the ACCB since the latter is time-consuming, and if it is a small MTDC system, a system blackout might occur during ACCB's long operating time. Hence, the DC grids need DCCBs installed on the DC sides [1]. However, developing the DCCB that can quickly interrupt the fault current is very challenging [2]. In addition, while the semiconductor-based DC circuit breaker is now commercially available [3], it suffers from a fault current magnitude limitation, and its operating time can be extended in long transmission systems.

Alternatively, it is feasible to regulate the DC fault current at the VSCs [4]. If the fault amplitude level in the entire DC grid is reduced, the demand to have better protection can become less pressing. In order to achieve the VSC that is capable of regulating fault current, one solution is to use a FB-MMC [5], as it can totally prevent the DC and AC faults transferring to each other side. Nevertheless, the FB-MMC requires twice as many power electronic devices as HB-MMC does, when they are of same level. These large number of switches are problematic because they can result in considerable power losses. A similar drawback can be found in the alternative arm multilevel converter [6], the cascaded multilevel converter [7], and the hybrid MMC [8]. In addition, the number of required devices on one phase of different MMCs are classified in [8], as shown in Table 3.1, where N refers to the number of SM cells on one arm of converter. Other examples of complex multilevel converters are demonstrated in [9]. The high capital costs could also be a factor that limit their widespread adoption.

ITEM (per phase)	HB-MMC	FB-MMC	CD-MMC	CC-MMC	TL-MMC	FB-HMMC	CD-HMMC	CC-HMMC	TL-HMMC
IGBTs	$4N$	$8N$	$5N$	$8N$	$6N$	$5.76N$	$4.88N$	$5.76N$	$4.88N$
Diodes	$4N$	$8N$	$7N$	$8N$	$8N$	$5.76N$	$6.64N$	$5.76N$	$5.76N$
Semiconductors	$8N$	$16N$	$12N$	$16N$	$14N$	$11.52N$	$11.52N$	$11.52N$	$10.64N$
Semiconductors in current path	$2N$	$4N$	$3N$	$4N$	$4N$	$2.88N$	$2.88N$	$2.88N$	$2.88N$
Series connection of switches	No	No	No	Required	No	No	No	Required	No
Number of shoot-through modes	$2N$	$4N$	$2N$	$4N$	$2N$	$2.88N$	$2N$	$2.88N$	$2N$

Table 3.1: A comparison of MMCs with different configurations [8]. HB-MMC: half-H bridge MMC. FB-MMC: full-H bridge MMC. CD-MMC: clamp double MMC. CC-MMC: cross-connected MMC. TL-MMC: three-level MMC. FB-HMMC: FB hybrid MMC. CD-HMMC: CD hybrid MMC. CC-HMMC: CC hybrid MMC. TL-HMMC: three-level cell-based hybrid MMC.

3.2. FAULT-TOLERANT LCL MMC

Based on the Type 4 model discussed in the second chapter, the HB-MMC with an LCL filter [4, 10, 11] is introduced and designed in this section. From an economic point of view, this LCL MMC is highly efficient and is much more fault-tolerant than a conventional HB-MMC. Although the FB-MMC can completely block a DC fault, it is not considered here due to its exorbitant cost.

3.2.1. BASIC CONCEPT OF DESIGN

Assuming that there is an LCL installed on the AC side of a VSC, an HVDC network can be established, as demonstrated in Figure 3.1. From this figure, it is possible to obtain the basic equations regarding one phase:

$$\begin{aligned} j\omega L_1 \overline{I_{1ac}} &= \overline{V_{1ac}} - \overline{V_c} \\ j\omega C \overline{V_c} &= \overline{I_{1ac}} + \overline{I_{2ac}} \\ j\omega L_2 \overline{I_{2ac}} &= \overline{V_{2ac}} - \overline{V_c} \end{aligned} \tag{3.1}$$

In these equations, the $\overline{I_{1ac}}$, $\overline{I_{2ac}}$, $\overline{V_{1ac}}$, $\overline{V_{2ac}}$ and $\overline{V_c}$ are phasors in root mean square (rms) that respectively stand for AC currents (i_{1ac}, i_{2ac}), line-to-neutral AC voltages (v_{1ac}, v_{2ac}) on the two sides of the LCL circuit, and the capacitor voltage (v_c). The converter shown in Figure 3.1 can be considered to be either a two-level, three-level or an MMC VSC converter.

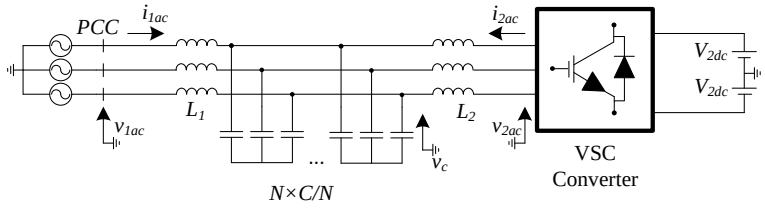

Figure 3.1: The schematic of an LCL-VSC.

After rearranging the Eq. 3.1, the phasors $\overline{I_{1ac}}$, $\overline{I_{2ac}}$ and $\overline{V_{2ac}}$ are expressed in Eq. 3.2, and the coefficients k_1, k_2, and k_3 are described in Eq. 3.3:

$$\begin{cases} \overline{V_C} = \left(L_1 \overline{V_{2ac}} + L_2 \overline{V_{1ac}}\right) \Big/ k_3 \\ \overline{I_{1ac}} = \left(k_1 \overline{V_{1ac}} - \overline{V_{2ac}}\right) \Big/ j\omega k_3 \\ \overline{I_{2ac}} = \left(k_2 \overline{V_{2ac}} - \overline{V_{1ac}}\right) \Big/ j\omega k_3 \end{cases} \tag{3.2}$$

where

$$\begin{cases} k_1 = 1 - \omega^2 L_2 C \\ k_2 = 1 - \omega^2 L_1 C \\ k_3 = L_1 + L_2 - \omega^2 L_1 L_2 C \end{cases} \tag{3.3}$$

Then, these equations can be transformed from the rotating *abc* frame to the *dq* frame:

$$\overline{V_{1ac}} = V_{1acm} \angle \theta_1 = V_{1acd} + jV_{1acq} \tag{3.4}$$

$$\overline{V_{2ac}} = V_{2acm} \angle \theta_2 = V_{2acd} + jV_{2acq} \tag{3.5}$$

and $\overline{V_{2ac}}$ should be controlled. After assuming that the d-axis is aligned with $\overline{V_{1ac}}$, Eq. 3.4 and Eq. 3.5 can be rewritten as:

$$\overline{V_{1ac}} = V_{1acd} = V_{1acm} \tag{3.6}$$

$$\overline{V_{2ac}} = \left(M_d + jM_q\right) \cdot \frac{V_{2dc}}{\sqrt{2}} \tag{3.7}$$

M_d and M_q are modulation indices of the d- and q-axes:

$$V_{2acm} = M\frac{V_{2dc}}{\sqrt{2}} \tag{3.8}$$

$$M = \sqrt{M_d^2 + M_q^2} \tag{3.9}$$

It is only then that the active power and the reactive power transfer utilizing rated design (which is normally a desired design) can be obtained using:

$$P_{1r} = -P_{2r} = \frac{s_r M_r M_{qr} V_{2dc}^2}{2\omega k_{3r}} \tag{3.10}$$

$$Q_{1r} = \mathrm{Im}\left[\overline{V_{1acr}} \cdot \overline{I_{1acr}}^*\right] = \frac{\left(k_{1r} s_r M_r - M_{dr}\right) s_r M_r V_{2dc}^2}{2\omega k_{3r}} \tag{3.11}$$

$$Q_{2r} = \mathrm{Im}\left[\overline{V_{2acr}} \cdot \overline{I_{2acr}}^*\right] = \frac{\left(k_{2r} M_r - s_r M_{dr}\right) M_r V_{2dc}^2}{2\omega k_{3r}} \tag{3.12}$$

the parameter s_r represents the rated step ratio of and LCL circuit:

$$s_r = V_{1acm}/V_{2acm} \tag{3.13}$$

In the above equations, the subscript r stands for "rated values", and the superscript asterisk (*) represents the corresponding conjugate phasors. It is evident from the equations that the q-axis is used to control the active power while the d-axis controls the reactive power.

A tradeoff is made in [4] in terms of the rated power efficiency and the partial-load efficiency. If the zero reactive power transfer is to be realized, Eq. 3.11 and Eq. 3.12 can be set to zero to derive the following equations:

$$k_{1r} s_r M_r = M_{dr} \tag{3.14}$$

$$k_{2r} M_r = s_r M_{dr} \tag{3.15}$$

$$k_{2r} = k_{1r} s_r^2 \tag{3.16}$$

The ratio of the rms values of the steady-state fault current i_{2acf} and the rated i_{2acr} is also important. According to Eq. 3.2, when v_{2ac}=0, the equation becomes:

$$r = \frac{1}{\sqrt{1 - k_{1r}^2 s_r^2}} \tag{3.17}$$

Then, it is also possible to obtain the relation between r and k_{1r}, which is:

$$k_{1r} = \frac{\sqrt{1 - 1/r^2}}{s_r} \tag{3.18}$$

In order to decrease the power losses under partial-load working conditions, a method is proposed to regulate the capacitor in [10]. After rearranging and substituting Eq. 3.10 and Eq. 3.11 into the condition $M_d^2 + M_q^2 \leq M_r^2$, this inequality becomes:

$$(s_r k_1 M_r)^2 + \left(2P_{part}\omega k_3 / s_r M_r V_{2dc}^2\right) \leq M_r^2 \tag{3.19}$$

In this case, P_{part} refers to a partial load. Afterward, the minimal capacitor can be calculated using Eq. 3.20:

$$\begin{aligned} C_{\min} &= \frac{-b-\sqrt{b^2-4ac}}{2a} \\ a &= 4\omega^6 P_{part}^2 L_1^2 L_2^2 \Big/ s_r^2 M_r^2 V_{2dc}^4 + s_r^2 M_r^2 L_2^2 \omega^4 \\ b &= -2\left[4P_{part}^2\omega^4(L_1+L_2)L_1L_2 \Big/ s_r^2 M_r^2 V_{2dc}^4 + s_r^2 M_r^2 L_2^2\omega^2\right] \\ c &= 4P_{part}^2\omega^2(L_1+L_2)^2 \Big/ s_r^2 M_r^2 V_{2dc}^4 + s_r^2 M_r^2 - M_r^2 \end{aligned} \tag{3.20}$$

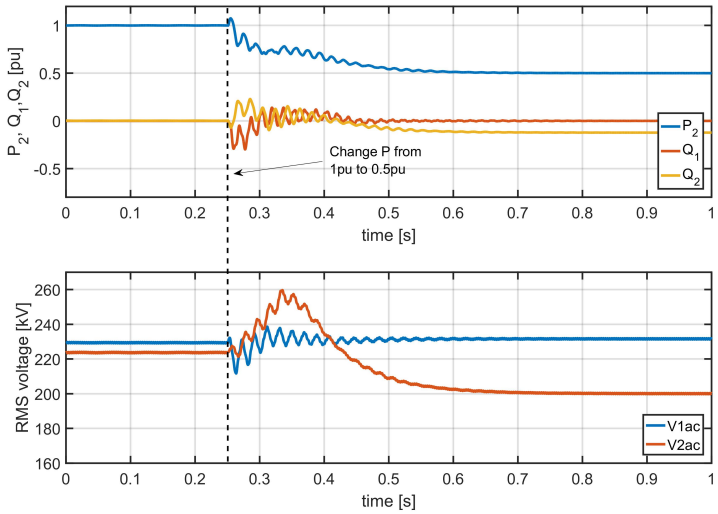

Figure 3.2: The behaviour of converter after decreasing power reference.

3.2.2. REGULATING THE *s* OF THE LCL CIRCUIT UNDER PARTIAL LOADS

REGULATING *s* TO DECREASE ACTIVE POWER LOSSES

Although the capacitance can be decreased, there is still a basic reactive power requirement, whereby the controller automatically readjust M_d to meet this reactive power demand. Figure 3.2 shows the simulated case when P_2=1.0pu changes to 0.5pu at 0.25s. In this case, the Q_2 is no longer zero, as the VSC has begun to absorb reactive power from the LCL circuit. Consequently, the current flowing through the converter bridge is still high which often results in high power losses and is a disadvantage of using the LCL-VSC under partial-load conditions. This is because the voltage V_{2ac} decreases while V_{1ac}

remains, in which case the redundant reactive power from the capacitor C in the LCL circuit is delivered to the VSC.

A solution could be found if the reactive power in the LCL circuit itself is analyzed. In order to ensure that no reactive power is being transferred, one condition must be met within the LCL circuit: the reactive power generated by the capacitor must be completely consumed by the two inductors. This condition can be satisfied before changing the reference of P_2 in Figure 3.2, as the Q_1=Q_2=0. Then the difference between the generated and consumed reactive powers is calculated as follows:

$$Q_{gen.} - Q_{con.} = \frac{\left(CL_2\omega^2 - 1\right) V_{1acd}^2 + \left(CL_1\omega^2 - 1\right) V_{2acm}^2 + 2V_{1acd}V_{2acd}}{\omega\left(L_1 + L_2 - CL_1L_2\omega^2\right)} \tag{3.21}$$

If Eq. 3.21 is made to be equal to zero, and Eq. 3.2, Eq. 3.3 and Eq. 3.5 are substituted in it, the following equation can be obtained:

$$s = f(C) = \sqrt{\frac{CL_1\omega^2 - 1}{CL_2\omega^2 - 1}} \tag{3.22}$$

Eq. 3.22 means that the step ratio is the function of capacitance C and inductances L_1 and L_2. Given that the inductors are connected in series in the AC grid, they cannot be changed; thus, Eq. 3.22 is solely the function of capacitance C. As such, it can be concluded that by using the optimal capacitor C_{min} calculated from Eq. 3.20, a specific refined step ratio $s_{refined}$ can be found. Hence, if the step ratio s can be changed accordingly, Eq. 3.21 will become close to zero, and the power losses will decrease.

RECALIBRATE TAP CONSIDERING THE IMPACT OF TRANSFORMER

Changing s can be mathematically achieved by either tuning the magnitudes V_{1acm} or V_{2acm}. In practice, using a tap-changeable transformer to adjust V_{1acm} is convenient. Although it is possible to ensure Q_2=0 by modulating V_{2acm}, the Q_1 could be momentarily large under partial loads. Then, it still needs to tune the tap of the transformer and capacitor banks to decrease the reactive power.

On the other hand, by interfacing a transformer, the AC system can work at an arbitrary voltage, making it preferable to install the tap changer on the secondary side of the transformer while connecting the primary side to the point of common coupling (PCC). Since a real transformer is not an ideal ratio changer, the impact of windings needs to be considered. The voltage drops on the leakage inductance and winding resistance decrease the output voltage. Consequently, the step ratio of the LCL circuit cannot be kept at the refined value.

The equivalent transformer model for phase A is shown in Figure 3.3. The Γ model is applied due to its simple configuration, where the n of the ideal voltage changer refers th the rated winding ratio, and k represents the position of tap changer. Thus, $k{\cdot}n$ means the ratio after changing the tap, and v_p and v_s indicate the primary and secondary voltage respectively. In addition, L_m and R_m are the magnetizing inductance and resistance respectively, while L_{L_tot} and R_{CuL} define the total leakage inductance and total winding resistance in H and Ω respectively, specified for 100% tap, as seen from the secondary side. According to [12, 13], these data are used to calculate the matrix that represents

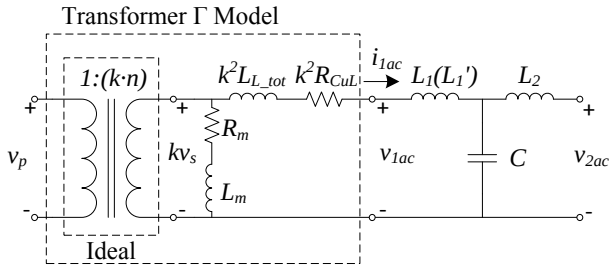

Figure 3.3: LCL circuit connecting transformer (only shows phase A).

a coupled transformer [1]. The coefficient k^2 is due to the secondary base impedance $Z_{base2} = (kV_{s\_rms})^2 / S_{base}$ (V_{s_rms} is set to V_{1acm} as the rms value of the secondary winding voltage).

When considering a more practical situation, k needs to be recalibrated. After applying the KVL in the phasor domain, Eq. 3.23 is obtained in a complex form:

$$k\overline{V_s} = \overline{V_{1ac}} + k^2\left(R_{CuL} + j\omega L_{L\_tot}\right)\cdot\overline{I_{1ac}} \tag{3.23}$$

It is important to note that since the PLL is locked with $\overline{V_{1ac}}$, and the purpose is to obtain zero reactive power. Only then can Eq. 3.24 be derived from Eq. 3.23 [2]:

$$kV_{1acm}\angle\theta = s_{re\_pu}V_{1acm} + \frac{k^2\left(R_{CuL} + j\omega L_{L\_tot}\right)\cdot P_{part}}{s_{re\_pu}V_{1acm}} \tag{3.24}$$

where, the $s_{re\_pu} = s_{refined}/s_r$. Eq. 3.24 informs that the power consumption of the leakage inductance and windings can be compensated by adjusting the amplitude of $\overline{V_s}$, thus the k. After taking the absolute value of Eq. 3.24, the variable k can be expressed as a function:

$$k = \frac{\sqrt{V_{1acm}^2 - \alpha - \sqrt{(V_{1acm}^2-\alpha)^2 - 4\beta^2\gamma^2}}}{\sqrt{2}\beta}$$
$$\begin{cases} \alpha = 2R_{CuL}P_{part} \\ \beta = \sqrt{R_{CuL}^2 + \omega^2 L_{L\_tot}^2}\,P_{part}/\left(s_{re\_pu}V_{1acm}\right) \\ \gamma = s_{re\_pu}V_{1acm} \end{cases} \tag{3.25}$$

The value of γ in Eq. 3.25 is the required secondary voltage after tapping the transformer, and it reflects that $s_{refined} = V_{1acm\_refined}/V_{1acm}$. Eq. 3.20, Eq. 3.22, and Eq. 3.25 clear illustrate that the variables k and $s_{refined}$ are the functions of P_{part}. This means that an LCL-converter-based system is able to work under different load conditions with certain values of $s_{refined}$ and k, such as by having a minimal required capacitor and a transformer tap selection.

[1] In PSCAD, the per-unit leakage reactance and magnetizing currents, specified for 100% tap, are used to calculate admittances for the new voltage rating corresponding to the tap setting [14].

[2] Although, the active power that is delivered from AC to DC side is assumed as positive P_{part} here, similar result can be derived if this active power is assumed as negative P_{part}.

In addition, Eq.3.23 and Eq. 3.24 have been derived under the assumption that only active power is imported from transformer's secondary side. Therefore, the reactive power consumed by the transformer is fully delivered from the primary side, which is the outer AC grid. In order to save the capacity of the AC transmission line system, it is also favorable to use the capacitor banks to provide the transformer's reactive power consumption [11]. Similar to Eq. 3.22, Eq. 3.26 can be obtained if leakage inductance of transformer is considered as a part of the LCL:

$$s_{refined} = s_{re\_pu} \cdot s_r = \sqrt{\frac{C\left(k^2 L_{L\_tot} + L_1{}'\right)\omega^2 - 1}{CL_2\omega^2 - 1}} \tag{3.26}$$

In this solution, the L_1 is divided into two parts: the fixed part L_1' and the changeable part $k^2 L_{L\_tot}$. The L_1' should be $L_1 - L_{L\_tot}$, so under full load where $k = s_{re\_pu} = 1$ (when assuming that the transformer is lossless), and Eq. 3.26 is equal to Eq. 3.24. This mathematical transformation simplifies the design: when the leakage inductance is given, one can use the obtained L_1 to find L_1', and replace it into the LCL circuit in Figure 3.3 to find k:

$$k = \sqrt{\frac{CL_1{}'\omega^2 - 1}{s_r^2\left(CL_2\omega^2 - 1\right) - CL_{L\_tot}\omega^2}} \tag{3.27}$$

This equation is different from Eq. 3.25 only in terms of the source of reactive power that is required by the transformer.

3.2.3. SELECTION OF THE ORIGINAL *s* AND DERATING OF THE CONVERTER

As a design parameter, the step ratio could be selected randomly if the converter is required to work at the rated power. However, the act of disconnecting the capacitor under partial load must be done cautiously. Figure 3.4 shows the relationships between the required capacitor C_{min} and P_{part} with different LCL step ratios. If s is selected below 1, the optimal C_{min} becomes negative when P_{part} is lower than a certain amount, which is physically impossible. Therefore, when the s-parameter must be designed lower than 1, it is best to plot the values and Figure 3.4 before determining the available minimum load. For example, the minimal partial load for $s_r = 0.85$ is around 0.32pu.

However, when a converter operates under a low partial load for a specific purpose, the rated power of a converter should be set to a lower value. This derating actually moves the working point of P_{part} close to 1 on the abscissa. As shown in Figure 3.4, when a converter is rated at 800MW, with an s_r of 0.85, it may not operate at 200MW, because the $P_{part} = 0.25$pu. After derating the converter to 400MW, the P_{part} becomes 0.5pu, and C_{min} reaches 0.25pu.

Upon describing the method that involves refining the s-parameter, the procedures of designing an LCL-based MMC can be outlined:

1. Determine the DC voltage V_{2dc}, M_r, P_r, P_{part} and the fault current ratio r.
2. Calculate the V_{2am} by using Eq. 3.8.
3. Calculate the V_{1am} through Eq. 3.13, by using the selected rated s_r.
4. Calculate the k_{1r} in accordance with Eq. 3.17.
5. Calculate the k_{2r} by using Eq. 3.16.

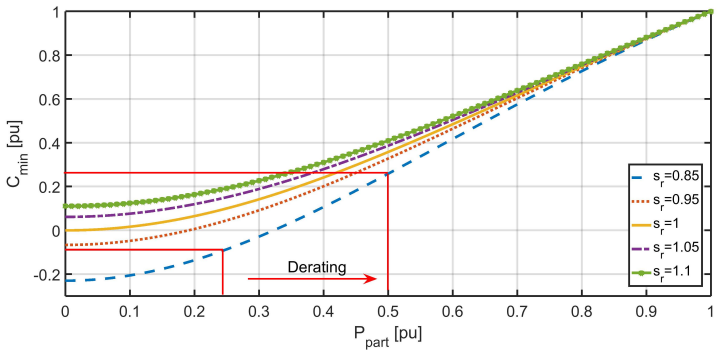

Figure 3.4: The required capacitor versus P_{part} (r=1.02).

6. Calculate the M_{dr} referring to Eq. 3.15 or Eq. 3.14.
7. Calculate the M_{qr} according to Eq. 3.9.
8. Calculate the k_{3r} by using Eq. 3.10.
9. Calculate the L_1 and L_2 through to Eq. 3.3.

Then under partial loads, these procedures should be followed:

10. Find the required C_{min} according to Eq. 3.20 and the P_{part}. Derate a converter when it is necessary.
11. Refine the s by using Eq. 3.22.
12. Find the tap through Eq. 3.25 or Eq. 3.27.
13. Regulate the tap changer and capacitor accordingly.

Figure 3.5 shows the diagrams of $s_{refined}$ and k versus the P_{part} with different s_r values. To obtain the k from Eq. 3.25, the leakage inductance and copper losses are respectively set to 0.18pu and 0.006pu [15]. The black-cross parts on the traces in Figure 3.5 result from the not available (N/A) operation regions under the partial loads of s_r=0.95 and 0.85 in Figure 3.4. Due to the leakage inductance and winding resistance, the value of $s_{refined}$ is slightly lower than k, even when the P_{part}=1pu. The gap reflects the effects of the voltage drop on the winding.

3.2.4. THE EFFECT OF OPTIMIZATION ON FAULT CURRENT RATIO

Because the main purpose of applying the LCL circuit is to limit the fault current, it is important to investigate the effect of changing step ratio s on the fault current.

The relationship between r and s can be obtained according to Eq. 3.17 and Eq. 3.22, which is expressed as:

$$r = \left\{1 - \left[\frac{(L_2 - L_1)\, s}{L_2 s^2 - L_1}\right]^2\right\}^{-\frac{1}{2}} \tag{3.28}$$

and the solution of r in pu are plotted in Figure 3.6.

As mentioned in the previous sections, the $s_{refined}$ is the function of P_{part}, and it is monotonic in Figure 3.5. Furthermore, $s_{refined}$ is monotonic decreasing when s_r<1 and

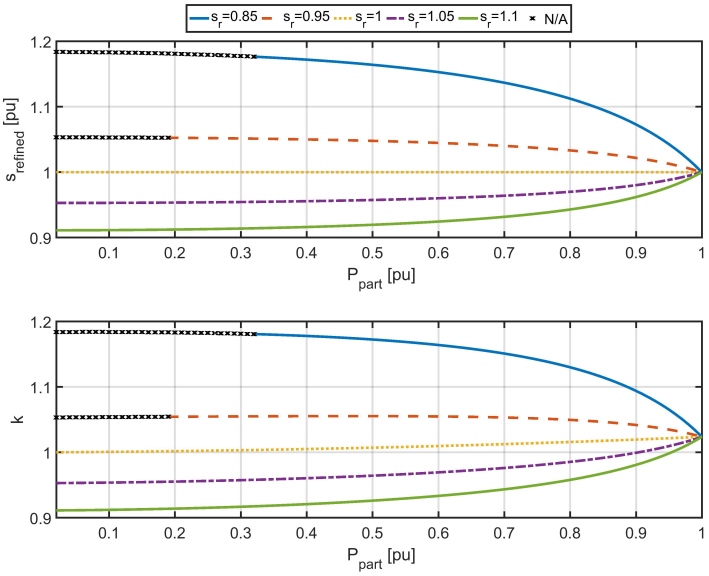

Figure 3.5: The required capacitor versus P_{part} (r=1.02).

is monotonic increasing when s_r>1. In Figure 3.6, the trajectories of r with different s_r also show the same monotonicity which are corresponding to Figure 3.5. Therefore, the domains of Eq. 3.28 are different under each s_r, and their traces all start from $s_{refined}$=1pu but in different directions, which are consistent with the decreasing trend of partial load from P_{part}=1pu. In Figure 3.6, the decrease of P_{part} are categorized by the arrows with different colors and line types.

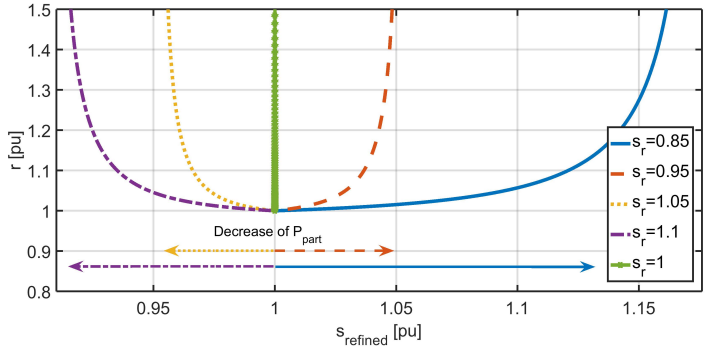

Figure 3.6: Fault current ratio r versus refined s (r=1.02)

Based on the results in Figure 3.6, when the converter works under partial loads, and the tap changer is switched accordingly, the fault current ratio increases, but it remains close to the r_{pu}=1 if P_{part} is kept within a range from 0.3pu to 1.0pu. when the P_{part}

drops out of this range, the solution of Eq. 3.28 will be at least three times higher than the desired fault current ratio, as shown in Figure 3.6. In addition, after solving Eq. 3.28 numerically when s_r=1, the result will become infinite, as shown by the green solid line with diamond in Figure 3.6. Although the fault current cannot be infinite in practice, it will still be quite large when the DC faults occur, and thus it would not be a good working condition.

3.2.5. PERFORMANCE OF THE LCL MODULAR MULTI-LEVEL CONVERTER

In accordance with the proposed design, a simplified HVDC network has been simulated in PSCAD. As previously mentioned, the modular multi-level converter has been modeled by a Type 4 model. The LCL-based test system is shown in Figure 3.7, and the parameters of the LCL HB-MMC are listed in Table 3.2. As a simulating counterpart, a regular HB-MMC without an LCL circuit has also been modeled, and the data are listed in Table 3.2 as well. It has been assumed that the range of the tap changer is ±5% with a step size of 1.25% for each tap [16]. In addition, it should be noted that the voltages tabulated in Table 3.2 are all in line-to-line rms values. As the original s_r is higher than 1, there is no need to derate the converter under partial loads.

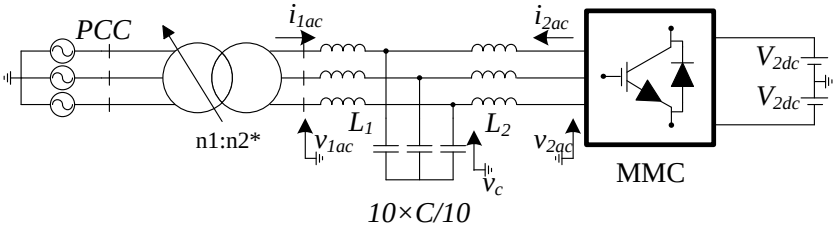

Figure 3.7: The schematic of LCL-based test system.

THE CAPABILITY OF TOLERATING DC FAULT

As the most severe fault, a permanent pole-to-pole fault is applied at 0.02s on the DC sides of the LCL HB-MMC and conventional HB-MMC, which are blocked when the DC current on either one pole is higher than 6kA [15]. It can be observed that the LCL circuit can restrain the fault current at a lower level, with the LCL HB-MMC experiencing a lower fault current which is half of that in the conventional HB-MMC. At the same time, the current in the converter's arms also decreases as evidenced in the middle graph of Figure 3.8, where the current of the LCL HB-MMC in the upper arm of phase A is drastically lower than that in the case of the HB-MMC. Therefore, the overcurrent stress in the converter bridge is limited in an acceptable range by the LCL circuit.

In the case of the LCL-based MMC, the AC voltage at PCC remains close to the rated value, so the DC fault is not transferred to the AC side. The simulation is demonstrated in the graph at the bottom of Figure 3.8, where the small depression in AC voltage is the result of reactive power circulation.

Parameters	LCL HB-MMC	HB-MMC
DC voltage	400kV	
PCC voltage	145kV	
Rated power	800MW	
Original step ratio s	1/0.95	N/A
Fault current ratio r	1.02	
Inductor L_1	0.1639H	
Inductor L_2	0.1681H	
Capacitor C	49uF	
RMS voltage $V1_{ac}$	231.57kV	
RMS voltage $V2_{ac}$	220kV	
Transformer turn ratio	145/231.57*	145/220
Transformer leakage reactance	0.18pu	
Transformer copper losses	0.006pu	
Tap changer	±1.25% × 4	N/A

Table 3.2: The test system's data. The asterisk indicates where the tap changer is located. N/A: not available.

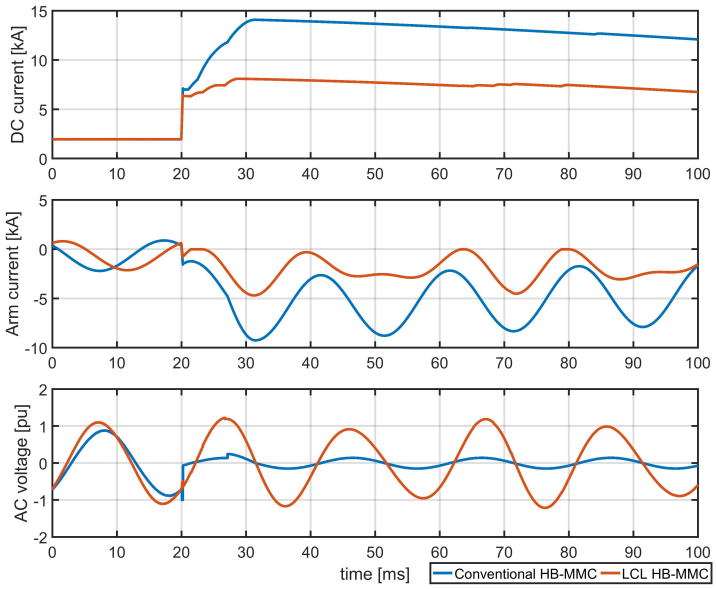

Figure 3.8: The converter response after a DC fault occurs.

THE CAPABILITY OF DECREASING POWER LOSSES

The aim of regulating a transformer is to decrease the reactive power transfer between the LCL circuit and the converter bridge, thus decreasing the power losses. Based on Eq. 3.25, the corresponding taps under each partial load conditions are listed in Table 3.3. It is also assumed that the capacitor is divided into 10 banks and that specific capacitor

banks are disconnected under different partial-load conditions.

Partial load	Connected C	$s_{refined}$	k	Tap changer
0.1pu		1.0011	95.09%	$1-4\times1.25\%$
0.2pu		1.0024	95.19%	$1-4\times1.25\%$
0.3pu		1.0040	95.35%	$1-4\times1.25\%$
0.4pu		1.006	95.60%	$1-4\times1.25\%$
0.5pu		1.0085	95.93%	$1-3\times1.25\%$
0.6pu		1.0118	96.39%	$1-3\times1.25\%$
0.7pu		1.0163	97.01%	$1-2\times1.25\%$
0.8pu		1.0229	97.90%	$1-2\times1.25\%$
0.9pu		1.0333	99.26%	1
1.0pu		1.0526	101.72%	$1+1\times1.25\%$

Table 3.3: Step ratio s and its corresponding tap changer under partial load.

Furthermore, while it is fairly difficult and complex to calculate the exact efficiency of an MMC, the losses can still be approximated [17–19]. The estimation of the power losses in different scenarios can be achieved through the method described in [19], and the adopted IGBT characteristics are those of the Mitsubishi CM1500HC-66R [20]. For comparison purposes, Table 3.4 lists the decreased power losses when converter working in rectifier (left sub-table) and inverter (right sub-table) modes respectively. The results show that the proposed method can reduce power losses, thus increasing the efficiency.

P[pu]	Power Loss [MW]		ΔLoss[%]
	s_r	$s_{refined}$	
0.1	0.2794	0.2778	0.57
0.2	0.7992	0.7872	1.50
0.3	1.4689	1.4314	2.55
0.4	2.2366	2.1542	3.68
0.5	3.0660	2.9414	4.06
0.6	3.9085	3.7160	4.93
0.7	4.7728	4.5848	3.94
0.8	5.6421	5.3873	4.52
0.9	6.6978	6.5218	2.63
1.0	7.4358	7.4358	N/A

P[pu]	Power Loss [MW]		ΔLoss[%]
	s_r	$s_{refined}$	
-0.1	0.3189	0.3183	0.19
-0.2	0.8950	0.8821	1.44
-0.3	1.6328	1.5977	2.15
-0.4	2.4791	2.3998	3.20
-0.5	3.4032	3.2732	3.82
-0.6	4.3421	4.1439	4.56
-0.7	5.2715	5.1139	2.99
-0.8	6.2758	6.0165	4.13
-0.9	7.4481	7.2582	2.55
-1.0	8.3091	8.3091	N/A

Table 3.4: Power losses before and after changing the tap of transformer under different partial loads. Top sub-table: rectifier mode. Bottom sub-table: inverter mode.

Since the unit of power loss is in MW, a small reduction in it can have considerable economic benefits. It is also predictable that this method can achieve a similar or better performance when implemented with two- or three-level converters because they are less efficient than MMC.

The different power losses taking place in the rectifier and inverter modes are caused by the IGBT and diode's different characteristics of resistance. Figure 3.9 depicts the

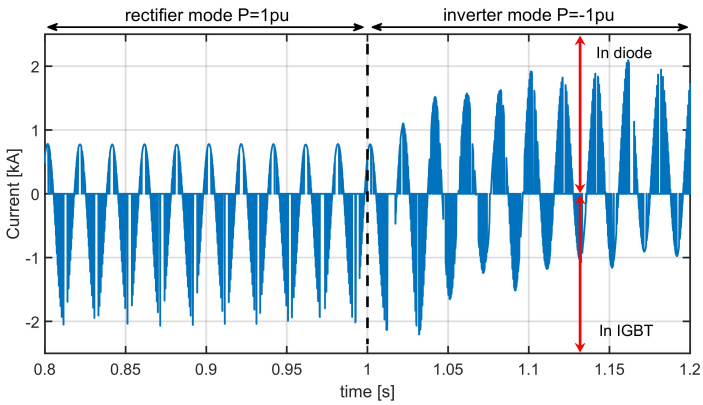

Figure 3.9: The current of one sub-module in the rectifier and inverter modes.

currents in one sub-module when the converter shifts from the rectifier mode (P=1pu) to the inverter mode (P=-1pu) at 1s. It can be understood that the current goes mainly through IGBTs in the rectifier mode but through diodes in the inverter mode.

DYNAMICS OF LCL CONVERTER DURING LOAD CHANGE

This section examines the dynamic behavior of the converter after changing the power reference using the solution based on Eq. 3.25. If it is assumed that the load require-

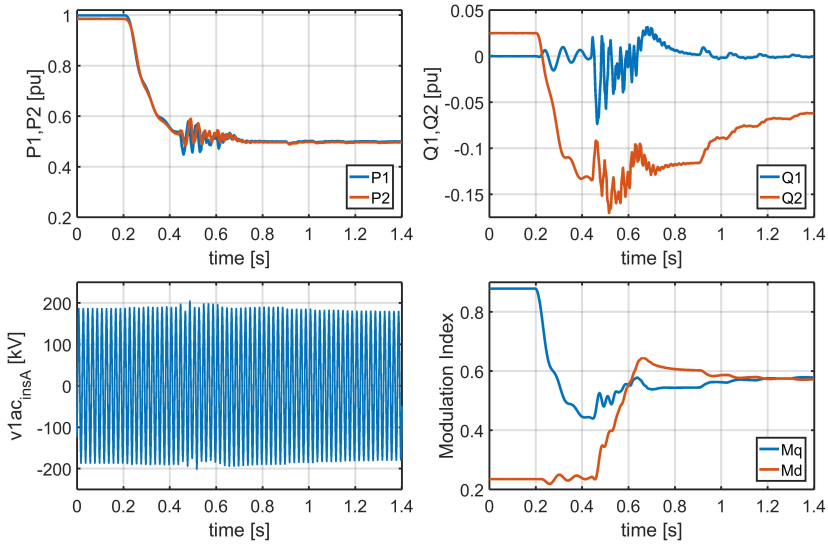

Figure 3.10: The dynamics of an LCL converter after changing the power reference, where only the instantaneous voltage of phase A of v_{1ac} is shown.

ment for a converter is decreased from 1pu to 0.5pu, then the regulation can be achieved through three procedures: 1) changing the power reference of the converter; 2) disconnecting the capacitor banks of the LCL circuit; 3) adjusting the tap of the transformer. In order to verify the effects of these actions respectively, the simulation is additionally divided into three parts: 1) changing the reference from 1pu to 0.5pu at 0.2s; 2) disconnecting the capacitors during the interval from 0.4s to 0.6s, with a 0.04s interval for disconnecting one bank; 3) adjusting the tap from 0.9s to 1.3s.

Figure 3.10 illustrates that the converter can successfully re-stabilize. Although there are some fast transients during the interval from 0.4s to 0.7s, they are not significant. The step-by-step change of tap also arouses dynamic behaviors, yet they are very smooth. Since the transformer links a strong system, tapping the transformer does not cause fast transients in v_{1ac}. The three procedures take place over 1.4s altogether as they are performed separately; however, this time can be shortened if all of them start at the same instant. Therefore, this method has good time response with regard to coping with load change.

3.3. CONCLUSION

This chapter introduces a new type of HB-MMC. Due to the LCL circuit, this type of MMC has higher resistibility against DC fault, when compared to the conventional HB-MMC. In order to ensure a high working efficiency, an optimized design of the LCL VSC under partial-load conditions is proposed as well.

Based on the in-depth analysis of the power balancing equation pertaining to the LCL circuit, the step ratio s can be modified theoretically for partial loads and is easily achieved by using the transformer with a tap changer. The design procedures of the LCL circuit are then proposed based on the theory. This dissertation also proves that the original step ratio should be s>1 and that the converter needs to be derated when s<1 as the converter would otherwise not function in the case of low partial load.

The simulation further shows that in order to achieve the best optimization, the range of the partial load P_{part} of this type of VSC should be between 0.5pu and 0.9pu. The results indicate that refining the step ratio with a tap changeable transformer can improve the working efficiency of the LCL-VSC without sacrificing its capability of limiting fault currents.

The application of the LCL circuit cannot isolate the DC fault feeding from the AC side, but it is able to keep the DC fault current at a low level and thus reduces the requirements of DCCBs. Since applying the proposed method results in lower power losses, the LCL-VSC will be a promising option for the future DC grids in terms of both operation and protection.

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4

SIGNAL PROCESSING TECHNIQUES FOR HVDC PROTECTION

In this chapter, three types of signal processing algorithms are introduced and discussed with regard to their capabilities when processing transient signals after the occurrence of DC-side faults. A fault current is simulated for a four-terminal LCL-MMC-based network, which is derived in Chapter 3. The demonstration shows the worst fault scenario when a permanent pole-to-pole fault takes place in a cable system. As such, the applied signal processing techniques that are discussed include the Fast Fourier Transform (FFT), the discrete and stationary wavelet transform (DWT & SWT) and the median absolute deviation (MAD) method.

4.1. SIGNAL PROCESSING TECHNIQUES

4.1.1. FAST FOURIER TRANSFORM

THE Fourier Transform (FT) is a mathematical method that decomposes a continuous function of time (i.e., $f(t)$) into frequency domain. The equation itself is defined as [1, 2]:

$$F(\omega) = \int_{-\infty}^{+\infty} f(t)\, e^{-i2\pi\omega t}\, dt \tag{4.1}$$

Furthermore, Eq. 4.1 is a complex-valued function of frequency ω which contains information pertaining to the harmonic components that make up the original signal $f(t)$. For the function of one harmonic component, its absolute value represents the amount of this harmonic frequency that is present in the original signal $f(t)$, and its complex argument is the phase of the sinusoid in this harmonic frequency. Hence, by decomposing a signal using the FT, one can identify the harmonic content of the signal.

When applying FT in practice, the signal is always discrete. Therefore, the FT is rewritten in terms of discrete signal samples $f(n)$ and discrete frequency components $F(k)$ [2]. This formulation is known as Discrete Fourier Transform (DFT), which is indicated as:

$$F(k) = \sum_{n=1}^{N-1} f(n)\, e^{-i2\pi kn/N}, k = 0, \ldots, N-1 \tag{4.2}$$

In order to accelerate the calculation of the DFT, the Fast Fourier Transform (FFT) is proposed [3]. This algorithm can decrease the complexity involved with computing the DFT from $O(N^2)$ to $O(NlogN)$ [4], where N is the size of the signal. The most common Cooley–Tukey FFT algorithm is graphically shown in Figure 4.1 [3]. As the most important numerical algorithm [5, 6], this method is considered to process the signal after the fault occurs in the established MTDC network.

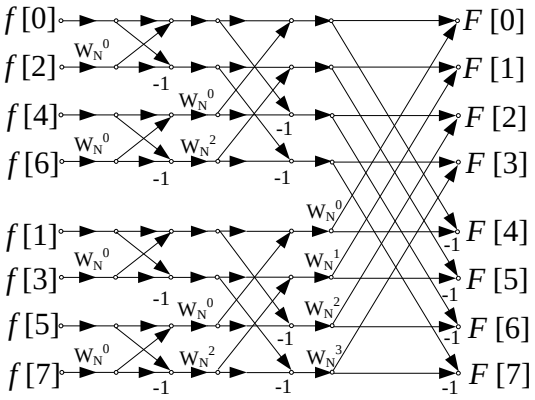

Figure 4.1: The diagram of Cooley-Tuckey FFT algorithm. The signal size is N=8 in the diagram.

4.1.2. WAVELET TRANSFORM

The wavelet transform (WT) is a powerful tool for signal analysis in the "time-scale" domain, which is well suited to detect the local and abrupt changes in a signal, such as the transient process in a power system. The idea behind the WT is that the original signal is to be decomposed into different scales using an analyzing function called "mother wavelet", and the most common ones can be classified into Haar wavelet, Daubechies wavelets, Symlets wavelets, and Coeiflets wavelets. When practically applied, these mother wavelets are scaled and translated to locally match an input signal. The wavelet coefficients that are subsequently calculated represent the correlation between the scaled wavelet and the signal [7].

Upon processing a continuous signal $f(t)$ by using the WT, the relevant equation can be expressed as

$$WT(f,a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{+\infty} f(t)\,\psi^*\left(\frac{t-b}{a}\right) dt \tag{4.3}$$

where the $\psi(t)$ is the selected mother wavelet, the asterisk denotes a complex conjugate, a is the scale parameter, and b is the translation parameter.

When processing a discrete or sampled signal, the DWT is widely used because of its high computational efficiency and data compression capability [8]. For a given discrete signal $f(k)$, its DWT can be expressed as:

$$DWT(f,m,n) = \frac{1}{\sqrt{a_0^m}} \sum_k f(k)\,\psi^*\left(\frac{n - k b_0 a_0^m}{a_0^m}\right) \tag{4.4}$$

It is noticeable that the scale parameter and the translation parameter are a_0^m and $k b_0 a_0^m$ respectively. In a standard DWT, the coefficients are sampled from the continuous WT on a dyadic grid where $a_0 = 2$ and $b_0 = 1$ [8] [9].

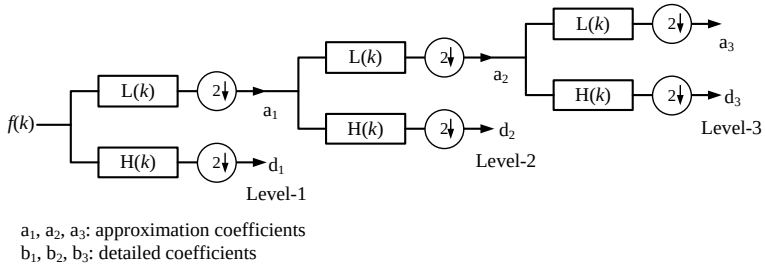

Figure 4.2: The Mallat Tree of DWT.

An actual implementation of the DWT is achieved using the so-called Mallat Tree Algorithm [8, 10, 11], which is depicted in Figure 4.2. The signal $f(k)$ is decomposed by the filter banks $H(k)$ and $L(k)$ where the former denotes a high pass filter, and the latter represents its corresponding dual low pass filter. The circles with the downward arrows denote down sampling by a factor of 2.

In order to overcome the DWT's lack of translation-invariance, which will be discussed in Section 4.2.3, the SWT uses up-sampling at each level of computation, instead

of the down-sampling used in the DWT. Similarly to the DWT, the Mallat Tree of the SWT is shown in Figure 4.3.

Since both the DWT and SWT can be applied to the transient detection, they are considered to be alternative options when processing the signals in HVDC systems after fault occurrence.

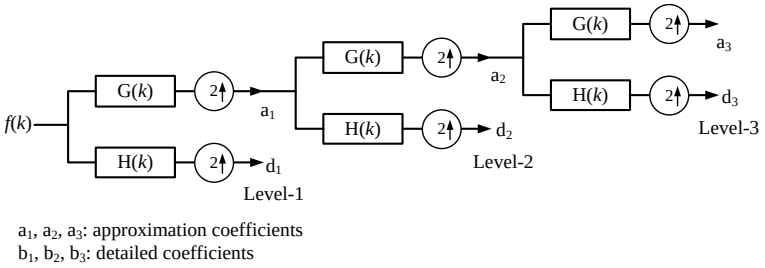

Figure 4.3: The Mallat Tree of SWT.

4.1.3. MEDIAN ABSOLUTE DEVIATION

BASIC CONCEPT OF MAD

The median absolute deviation (MAD) method is a robust statistical method that can locate outliers in a data or signal series [12], such as the most abrupt value in a transient process. If there is a vector S indexed by i that contains the latest m samples of signal X_i within an observation interval:

$$S_i = [X_i(t - m \times \Delta t) \dots X_i(t - 2 \times \Delta t), X_i(t - \Delta t), X_i(t)] \tag{4.5}$$

where Δt represents the sample interval, and the MAD of S_i is defined as:

$$MAD(S_i) = median[|S_i - median(S_i)|] \tag{4.6}$$

Eq. 4.6 demonstrates that the MAD is the median of the absolute deviations of samples from the median of the complete S_i vector. MAD is particularly useful because it has been proven to be able to identify the outliers in a data series, i.e., extreme value or outlying data [13].

Since it is less likely that the S_i has symmetrically distributed sample values, it is prudent to perform MAD_{double} [14, 15] instead, in order to properly identify the high and low outliers of the dataset. The description of MAD_{double} is as follows:

$$MAD_{double}(S_i) = \begin{cases} MAD_{low} = MAD(S_i), S_i \le median(S_i) \\ MAD_{high} = MAD(S_i), S_i \ge median(S_i) \end{cases} \tag{4.7}$$

where the MAD_{low} value corresponds to the median absolute deviation from the median of all samples which are lower than or equal to the median of the complete S_i dataset. On the other hand, MAD_{high} value differs in that it corresponds to the median absolute deviation from the median of all samples which are greater than or equal to that of the

complete S_i dataset. As such, it is then that the MAD denominated samples of S_i can be obtained as follows:

$$S_{iMAD} = [S_i - median(S_i)] / MAD_{double}(S_i) \tag{4.8}$$

According to Eq. 4.8, the S_{iMAD} is dependent on the whole S_i dataset. Therefore, after attributing a moving window function to S_i, it updates automatically at each sampling interval, so that only the most recent samples are taken into account in the calculation.

The MAD's feature of outlier detection depends on the fact that Eq. 4.6 is close to zero when the system is in the steady state. Therefore, when an outlier is recorded in the S_i vector, S_{iMAD} largely varies in accordance with Eq. 4.8 [1].

It also needs to be noted that originally in [13] an absolute value operator for the numerator of Eq. 4.8 existed. However, it has been removed in this thesis so that the polarities of MAD can be used to identify both the positive and the negative outliers. Consequently, MAD becomes far more effective in an HVDC environment when detecting an abrupt change.

MODIFIED MAD

Although the MAD has a good time response for transient signal processing, the information that it provides is limited since the extremely large values gathered through this method are basically impossible to quantify. Although this is not a problem when it is applied to protect a simple point-to-point HVDC system where there is only one DC line, it becomes more problematic in a more complex MTDC network where the MAD does not serve as a sufficient form of protection if there are only unquantifiable outliers. The MAD is also modified accordingly in order to enhance its functionality in an MTDC situation. As such, Eq. 4.6 becomes:

$$MAD(S_i) = median(S_i) \tag{4.9}$$

However, Eq. 4.7 and Eq. 4.8 are kept unchanged throughout this process.

By doing this, the $MAD(S_i)$ can still reflect the steady operation of the system since the median of S_i does not change until the samples of the outliers occupy half of the whole dataset. For the purpose of easily identifying them in the thesis, the algorithm using Eq. 4.6 is referred to as MAD-1, while the one using Eq. 4.9 is referred to as MAD-2. This will be further discussed in the next chapter.

[1] Theoretically, the S_{iMAD} should be infinite when there is an outlier. However, this is impossible because the Eq. 4.6 cannot be strictly zero due to the noise emitted within a system.

4.2. PERFORMANCE OF CONSIDERED TECHNIQUES

4.2.1. COLLECTING FAULT TRANSIENT DATA

In this section, a four-terminal MTDC system is modeled based on the LCL-MMC converter described in Chapter 3, which is used to obtain the transient signal after the fault occurs. The system is depicted in Figure 4.4, and the parameters of this HVDC system are listed in Table 4.1. In Figure 4.4, it is assumed that a small inductor is installed at each port of the bus working as fault current limiter (FCL). The transformer ratios are also adjusted according to the least active power losses, and all the MMCs are set to be blocked when the amplitude of the DC current in either one of six arms is higher than 3kA. In addition, in order to obtain accurate transient information, the underground cables are modeled using the Frequency Dependent (Phase) Model [16, 17] in PSCAD, whose dimensions are shown in Figure 4.5. The cable data are adopted from [18].

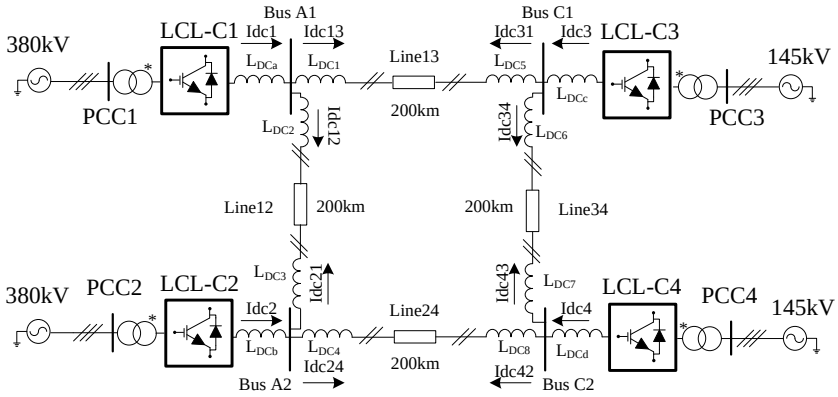

Figure 4.4: A four-terminal LCL-MMC-based HVDC network.

AC system			DC system	
Bus name	RMS voltage	Transformer ratio	Converter name	Control mode and setting points
PCC1	380kV	380×95%/231.58	LCL-MMC-C1	V_{dc}: V_{dcref}=±200kV
				Q: Q_{ref}=0 MVAR
PCC2		380×95%/231.58	LCL-MMC-C2	P/V_{dc}: P_{ref}=-300MW, V_{dcref}=±200kV, droop=0.05
				Q: Q_{ref}=0 MVAR
PCC3	145kV	145×100%/231.58	LCL-MMC-C3	P/V_{dc}: P_{ref}=700MW, V_{dcref}=±200kV, droop=0.05
				Q: Q_{ref}=0 MVAR
PCC4		145×95%/231.58	LCL-MMC-C4	P/V_{dc}: P_{ref}=-300MW, V_{dcref}=±200kV, droop=0.05
				Q: Q_{ref}=0 MVAR

Table 4.1: The converters' operating modes and set points.

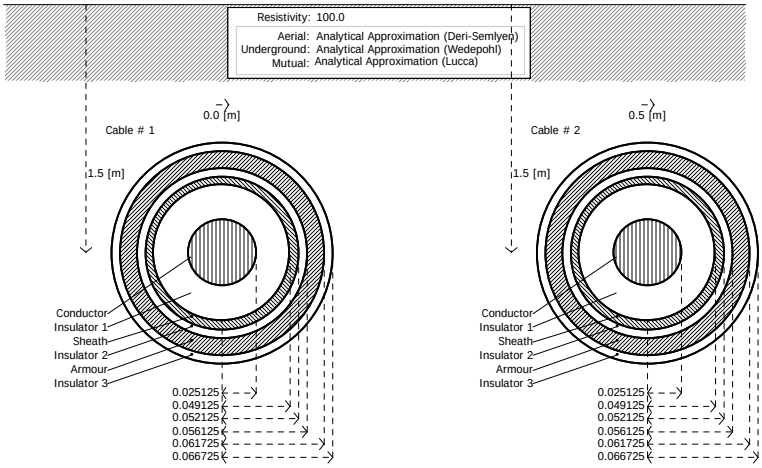

Figure 4.5: The dimensions of XPLE cable.

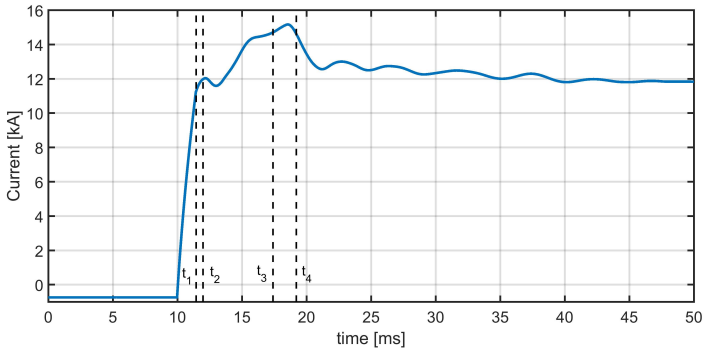

Figure 4.6: The fault current Idc13. The block time of converter is marked: t_1 for LCL-C1, t_2 for LCL-C3, t_3 for LCL-C2, and t_4 for LCL-C4.

The recorded data correspond to a simulated permanent pole-to-pole fault which is applied on Line13 at 10ms. Its location is 0km away from Bus A1, which is at the left end of Line13, and the actual size of the current limiter is neglected. The current Idc13 is shown in Figure 4.6 where all the block instants of the four converters are marked as well. It is noticeable that the fault current rises to a high level in a very short period of time. As such, if the fault is detected and cleared in a quick manner, the system blackout can be avoided.

4.2.2. DECOMPOSING A SIGNAL USING FFT

Based on the simulated current shown in Figure 4.6, the FFT is applied in order to provide the frequency response of the signal between 10ms and 50ms, and the results after decomposition are shown in Figure 4.7. In the code of FFT, the zero padding is used to

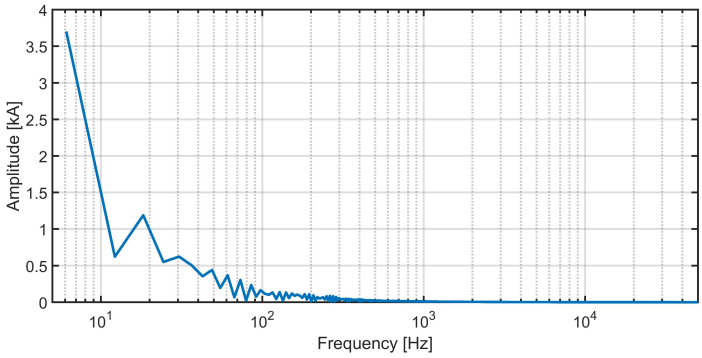

Figure 4.7: The results of FFT.

ensure that the number of sampled signal is a multiple of two. It is clear that the dominant current harmonic components of the signal in Figure 4.6 are located in the low-frequency range from 6Hz to 20Hz. In addition, there are identifiable harmonic components in the high-frequency range between 30Hz and 300Hz. The results show that the FFT is suitable for identifying the harmonic content in the original signal but that it cannot determine the instant when each component occurs. In other words, the FFT cannot distinguish between different transient signals containing the same harmonic components that can appear at different instants in time domain. Therefore, using FFT is not enough for processing the transient information.

In order to resolve this problem, the short-time Fourier Transform (STFT) [19] can be used. Unlike the FFT, the STFT divides the original signal into several segments with respect to time and then decomposes the signal in each segment as illustrated in the top graph of Figure 4.8. This makes it possible to identify the harmonic components in every segment of time so that the occurring instants of the harmonic components can be obtained. In a practical computation, these segments are defined using a certain window function, with the most common types being Hann window, Hamming window, Gaussian window, Blackman window.

Furthermore, it is necessary to consider the resolution when using the STFT. The STFT's resolution can be explained in the two lower graphs of Figure 4.8 where it can be seen that a wider window yields a better resolution of frequency, and a narrower window yields a better resolution of time. In Figure 4.9, the results of using STFT to process the signal in Figure 4.6 are depicted. The top plot uses a Hamming window with a width of 62, while the bottom one uses the same window with a width of 3. Due to the wider window, a certain range of frequencies are separated by different "stripes" in the top plot, and these frequencies are more likely to distribute throughout the whole time interval. Based on the amplitudes in dB/Hz, the more identifiable frequencies are those that are lower than 5Hz. However, the spectrum mixture means that width=62 is still too narrow to identify the low-frequency components. Even if the window width is increased, the spectrum mixture is still inevitable. In fact, the mixture in spectrum follows the Gabor uncertainty principle in time-frequency analysis [20], which states that the exact time

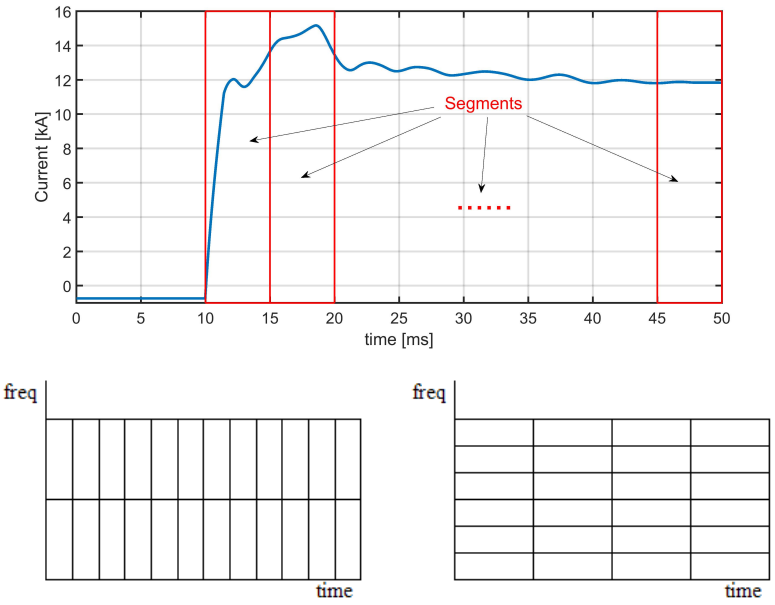

Figure 4.8: The top plot illustrates the concept of STFT, and the bottom plots indicate the resolution of STFT with narrow (left) and wide (right) windows [20].

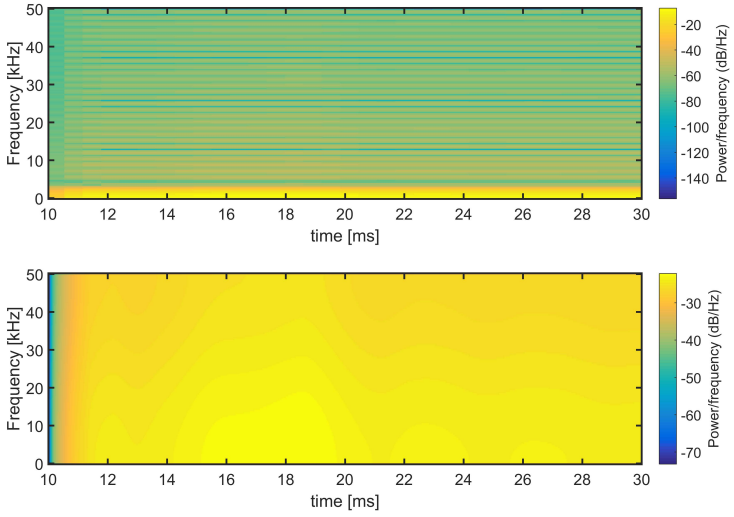

Figure 4.9: The results of the STFT using Hamming window with width=62 (top) and width=3 (bottom).

and frequency of a signal can never be simultaneously known: a signal cannot plot as a point on the time-frequency plane.

In the bottom plot of Figure 4.9 with a narrower window, there are more identifiable areas in the time scale. For example, the area between 15ms and 20ms shows that the frequencies between 0Hz and 20Hz are distinguishable in dB/Hz. Nevertheless, it is challenging to identify the characteristic frequency component in a time interval as the aforementioned interference in the spectrum still occurs. Therefore, determining the fault indicator becomes difficult. In order to find an ideal characteristic frequency component of a signal, the STFT must be implemented repetitively using different window widths.

Although the STFT improves upon the FFT in terms of its ability to process the transient information, it is still insufficient. One reason for this is because the fixed window width cannot meet the flexible requirements when detecting the low- and high-frequency components in a time-varying signal, and the boundary between the wide and narrow windows is ambiguous. Another reason is the high computation burden of this algorithm because the FFT needs to be implemented in each time segment, which means long computation time can delay the process of fault detection.

In this study, only Hamming window is considered; however, the other types of windows would generate similar results. Furthermore, the research of window is also important, but it is not discussed here in detail, as it is beyond the scope of the research.

4.2.3. DECOMPOSING A SIGNAL USING WT

In this section, the original signal is processed by WT with the mother wavelet "Haar". The results of implementing the SWT and DWT in MATLAB are illustrated in Figure 4.10 and Figure 4.11 respectively, where only three levels of detailed coefficients are depicted. More importantly, it can be observed that for both discussed WTs, the most identifiable coefficients are generated in the first 1ms after the fault occurs. Using a prudently selected threshold in accordance with the first crest or valley value, this fast time response makes the WT a good fault-detecting option in a DC grid.

In Figures 4.10 and 4.11, it can be seen that the coefficients d2 and d3 of the SWT and DWT are generated before the fault occurs, which is at 10ms. This is because the MATLAB toolbox carries out the off-line calculation of the WT. If the WT is applied synchronously with the electrical network simulation in EMT software, there will be a certain time delay for each level. However, these delays do not impact the fast time response of the WT. For the purpose of comparison, the DWT results obtained from PSCAD are shown in Figure 4.12 as well. The selection of the simplest "Haar" mother wavelet accounts for the shortest possible time delay, which will unfortunately increase when a more complex mother wavelet is chosen, such as the Daubechies 5 (db5) wavelet. Since have a long time delay is not preferred, "Haar" is the only mother wavelet considered in this thesis.

Although WT favors a fast time response, the DWT is disadvantaged because it lacks translation invariance, meaning that the outputs of the DWT can vary when processing a same signal with different time delays. The main reason for this is the "translation" of the mother wavelet in Eq. 4.3 and Eq. 4.4, which is evident when the sampling frequency of a DWT is low, as shown in Figure 4.13. In this figure, the three plots of the first row trace

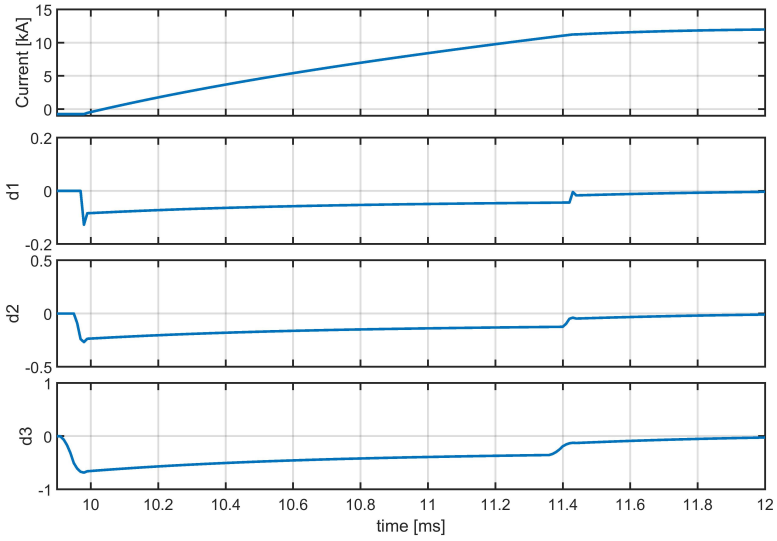

Figure 4.10: The results of SWT.

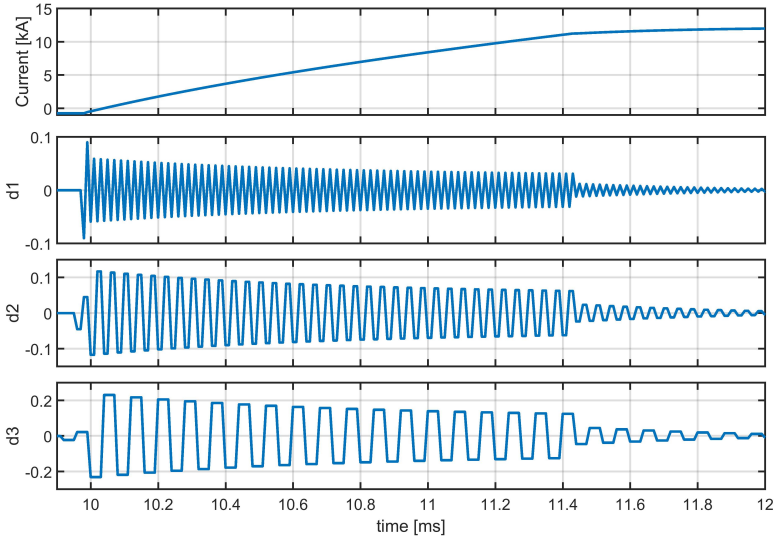

Figure 4.11: The results of DWT.

the DWT results of the original signal from 9ms to 12ms in Figure 4.6. In the meantime, when the original signal is manually delayed by 0.4ms, the DWT with the same sample frequency has different output, which is traced in the three plots of the second row in Figure 4.13.

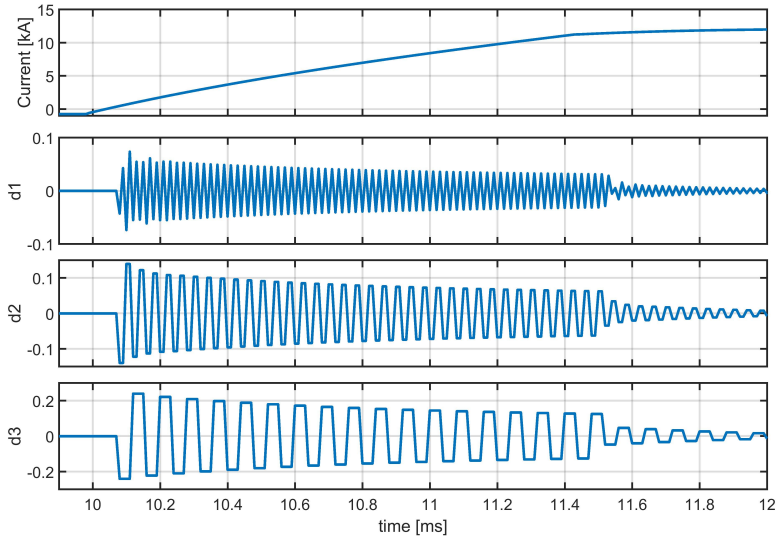

Figure 4.12: The delay of DWT in PSCAD.

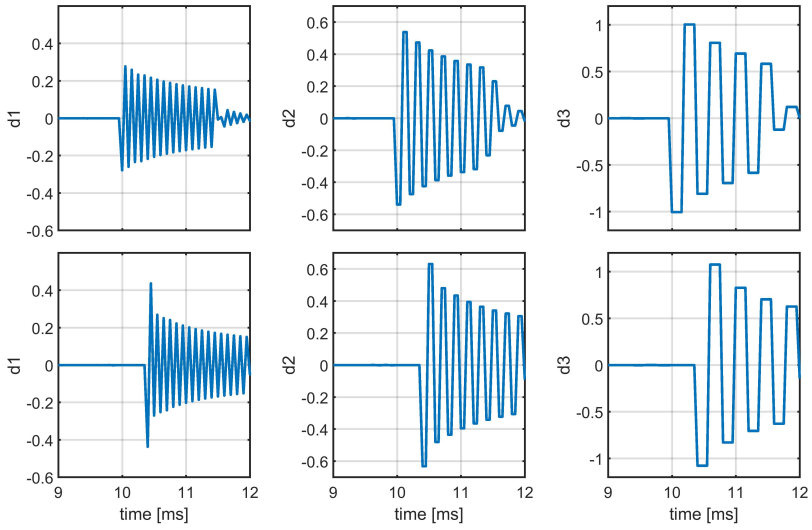

Figure 4.13: The results of the DWT after processing the original (top plot) and manually-delayed (bottom plot) signals. The sample frequency is 20kHz.

Given that there are unavoidable and unpredictable time delays in a real system, the lack of translation invariance can increase the uncertainty in the process of fault detection. Although the predefined threshold might be missed because of this feature of DWT,

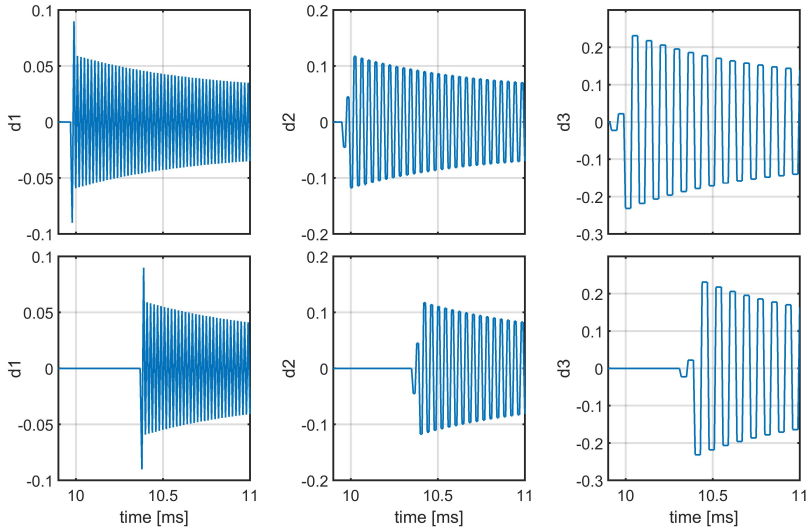

Figure 4.14: The results of the DWT after processing the original (top plot) and manually-delayed (bottom plot) signals. The sample frequency is 100kHz.

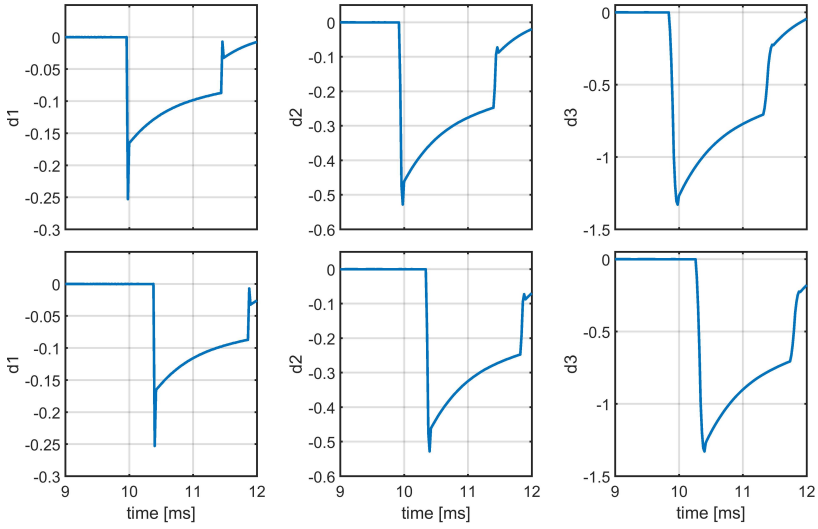

Figure 4.15: The results of the SWT after processing the original (top plot) and manually-delayed (bottom plot) signals. The sample frequency is 20kHz.

there are fortunately two solutions for this possible trouble. The first one is increasing the sampling frequency of the DWT, and the second one is the use of the SWT. By processing the same signal without and with time delay, the DWT and SWT generate the

results in Figures 4.14 and 4.15 respectively. Based on these two figures, it is observable that the time delay no longer has an impact on the results of the WT. As such, either the DWT with the high sampling frequency or the SWT can be used to detect fault signals.

4.2.4. PROCESSING FAULT-CAUSED TRANSIENTS USING MAD

Unlike the discussed FFT and WT, MAD does not transform the original signal into other domains. Instead, it is used to examine whether or not the latest data sampled from a signal are outliers. When there is a fault, it is highly possible that the latest samples of the current or the voltage become disturbed data. Based on the equations provided in Section 4.1.3, the MAD-1 is scripted and implemented, and its performance is illustrated in Figure 4.16. The current signal in the upper plot of this figure, which is same as that in Figure 4.6, is sampled at a frequency of 10kHz, and the latest 50 samples are stored in S_i to compute S_{iMAD}.

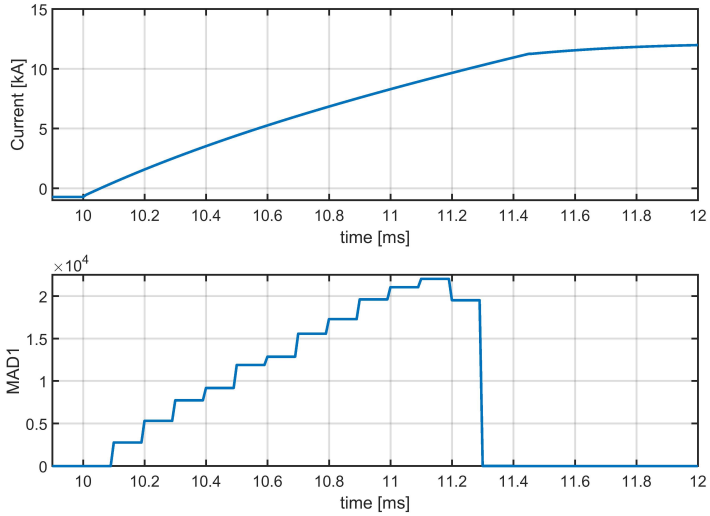

Figure 4.16: Performance of MAD-1 to detect outlier.

Here, it can be seen that the MAD-1 can generate a high distinguishable value at 10.1ms (keeping in mind that the fault is applied at 10ms). Consequently, a command can be initialized at 10.1ms to indicate that a fault has happened. If the sampling frequency is higher, the fault detection can also be faster. In addition, according to the concept of MAD, we can consider that this algorithm is immune to the time delay during the signal transferring. This is because the time delay only affects the recording instant of the abrupt data, but not their statistical feature with regard to the whole dataset.

Although only the MAD-1 detecting post-fault transients is shown here, it is possible that MAD-2 also has a fast response due to the similarities between these two algorithms. In the next chapter, both of these methods will be discussed thoroughly as their different properties and features involve undertaking different tasks.

4.3. CONCLUSION

The state of an electrical system can be indicated after its currents or voltages are processed. Among the discussed processing methods, the STFT can transform the signal into frequency domain within certain time intervals. However, there should be a compromise between the resolutions pertaining to the frequency and the time. As explained in Section 4.2.2, it is quite complicated to identify the most characteristic frequency component in a transient signal as an indicator of faults.

Due to its flexible scaling and translating features, the WT is competitively used to detect faults, as its multiresolution reveals the abrupt signal with respect to time. By performing this procedure, it is convenient to find the arrival instant of a fault surge, thus determining the required threshold as a fault indicator. Nevertheless, the use of the WT requires cautiously considering the sampling frequency, which determines the improvement of DWT's translation-invariance. In the case shown in Figure 4.14, although the impact of the time delay can be avoided, it comes at the cost of using a high sampling frequency. By contrast, while the SWT is immune to a possible time delay, its required signal length must be able to be divided exactly by 2^{Levels}. This means that in order to achieve a 3-level SWT, the input must have at least $2^3 \times k(k = 1,2,3\ldots N)$ samples, and the output of each level contains the same number of samples as the input. Therefore, the redundancy of the SWT can be extremely high if the original signal is sampled at a high frequency. Consequently, before using the SWT to process a signal, a fixed-width data window has to be used to store the signal samples.

Due to the fixed simulation time step, the maximal sampling frequency is also fixed in the EMT applications, which makes the up-sampling of the SWT impossible. Hence, the DWT is more feasible than the SWT in EMT environment. In the next chapter, the DWT is implemented as a key algorithm for a unit protection method. Unlike the SWT, it is evident that the oscillation of the DWT output complicates the detection of a fault transient. Therefore, a simple component of "self-hold" function has been applied additionally to record the first DWT output.

Compared to the FFT and WT, the MAD method is more straight-forward and simple since it statistically evaluates the most recent data used in the whole dataset, unlike the FFT and WT which transform the signal into other domains. Therefore, the processing time required by the MAD is shorter than those of the other two. In addition, unlike the DWT, the high sampling frequency is not a necessity for MAD. In the presented case, it can be seen that the 10kHz sampling frequency is sufficiently high for MAD. Therefore, the next chapter devises a protection method that is based on MAD and does not require communication.

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5

FAULT DETECTING ALGORITHMS BASED ON TRANSIENT ANALYSIS

In this chapter, the transient process after a fault occurs within the modeled MTDC system is discussed and explained first. Using the traveling wave theory, the identifiable characteristic of the incident surge traveling along the faulty line is demonstrated. Then, a DWT-based unit protection is introduced to protect the DC lines, and it is implemented in the MTDC system. Afterward, the sensitivity of this method is analyzed, and the thresholds are determined accordingly. On the other hand, a communication-free protection is proposed based on MAD. This method is a counterpart of the former DWT-based protection which depends on the communication between the relays on the remote ends of the DC lines. In order to ensure the protection's selectivity, a current differential protection is proposed to deal with the bus fault.

5.1. DWT-BASED DC LINE PROTECTION METHOD

5.1.1. TRAVELING-WAVE BASED DC FAULT ANALYSIS

WHEN an electrical system is working in the steady state, the voltage at each converter's DC terminal is relatively stable, which enables the identification of the power flow of one line according to the direction of the current in this line. Furthermore, when a reference direction is predefined, the current direction can be simply represented through its positive and negative signs, which mean in and out of phase in terms of the reference direction respectively. These two current polarities also apply in fault scenario and can provide important information when attempting to determine the fault location. In this thesis, the traveling wave theory [1, 2] is used to explain this feature as it is widely accepted for the transient analysis in electrical power systems, especially when there are long transmission lines or cables involved.

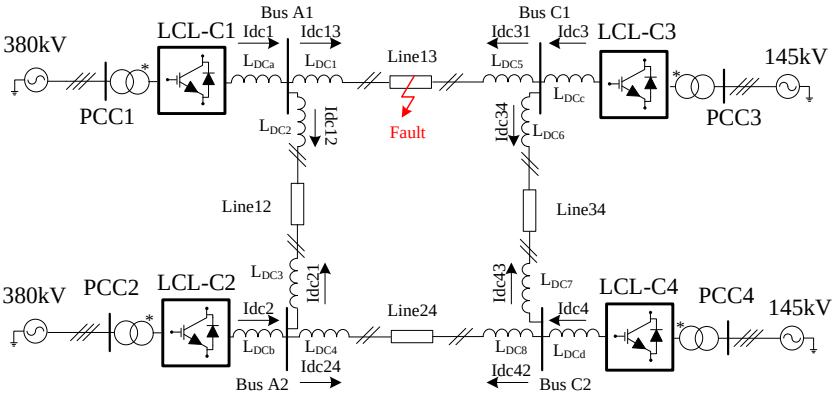

Figure 5.1: A four-terminal LCL-MMC-based HVDC network.

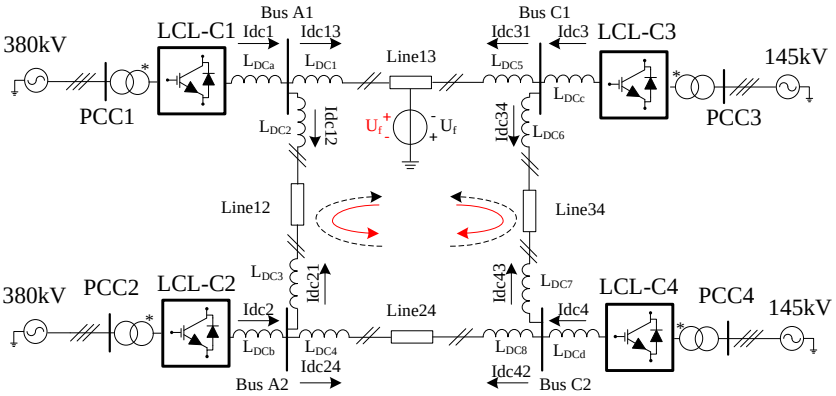

Figure 5.2: A fault-generated traveling wave of current.

When examining Figure 5.1, it can be assumed that a fault may occur on Line13 of the four-terminal HVDC system. For a selective protection, the fault is internal for the

relays protecting the Line13 while external for those that protect the Line12, Line34 and Line24, and the surge U_f generated by fault can be seen in Figure 5.2 [3]. When the fault occurs on the positive pole, the U_f that is designated in black becomes negative, and the current traveling wave caused by the fault flows in the direction indicated by the black dashed arrow on the diagram. When considering the reference directions specified on each line, it becomes clear that the polarities of Idc13 and Idc31 on Line13 in Figure 5.2 are both positive after the fault occurs. By contrast, on healthy Line24, the current polarities of Idc24 and Idc42 are both negative, while for either healthy Line12 or Line34, the polarities of the currents on the two ends of a line are opposite to each other.

On the contrary, when the fault occurs on the negative pole, the U_f in red is positive, and the flowing of the current traveling wave is depicted as the red solid arrow in Figure 5.2. In this situation, the current polarities of Idc13 and Idc31 in the same figure are both negative; however, the current polarities on Line24's two ends are both positive. Similar to the above fault case for either the Line12 or Line34, the polarities of the currents on either line's two ends are opposite to each other.

Therefore, if the polarities of the currents on the two ends of one line are monitored, it is possible to determine whether or not a fault has occurred on this line. More importantly, it is understandable that these features of the current polarities are valid in situations where more than two lines are connected to one bus [4].

5.1.2. FAULT DETECTING CRITERIA

According to the above-mentioned fault characteristic analysis and the DWT's ability to detect the abrupt and local changes in a signal [5, 6], the first value of the DWT is used to determine the internal fault on a transmission line or cable [4, 7]. Suppose that W^+_{ab} and W^+_{ba} are the initial WT outputs obtained respectively on remote ends a and b of Lineab's positive pole, while W^-_{ab} and W^-_{ba} are the corresponding WT outputs of Lineab's negative pole [1]. Based on the reference current directions in Figures 5.1 and 5.2, the relations between the DWT output signs and current polarities are as follows:

On the positive pole, the negative sign of the DWT value (the first valley of the DWT waveform is negative) indicates that a positive current traveling wave is flowing through the end. However, on the negative pole, the positive sign of the DWT value (as the first crest of DWT waveform is positive) means that a negative current traveling wave is flowing through the end. Then, the current polarity criterion [4] is applied for both positive and negative poles, and it is only when there is an internal fault on a line that the following equation can be fulfilled:

$$\begin{cases} sign\left(W^+_{ab}\right) = -1 \wedge sign\left(W^-_{ab}\right) = 1 \\ sign\left(W^+_{ba}\right) = -1 \wedge sign\left(W^-_{ba}\right) = 1 \end{cases} \tag{5.1}$$

As such, it is clear that the protection needs to be achieved by a current polarity information exchange and upon comparing the relays on the two ends of one line.

Even though the simulated MTDC is a symmetrical monopole system, there are weak couplings between the two poles of one DC line. Thus, the WT output of a current traveling wave on a healthy pole would be lower than that on a faulty pole [7]. Therefore, when

[1] Superscripts "+" and "-" stand for the quantities with regard to positive and negative poles respectively.

identifying the pole-to-pole fault and pole-to-ground fault, the following equations can be applied :

$$\begin{cases} |W_{ab}^{+}| > k_1 |W_{ab}^{-}| \\ |W_{ba}^{+}| > k_1 |W_{ba}^{-}| \end{cases} \tag{5.2}$$

$$\begin{cases} |W_{ab}^{-}| > k_2 |W_{ab}^{+}| \\ |W_{ba}^{-}| > k_2 |W_{ba}^{+}| \end{cases} \tag{5.3}$$

$$\begin{cases} |W_{ab}^{+}| - |W_{ab}^{-}| \in (-\varepsilon, \varepsilon) \\ |W_{ba}^{+}| - |W_{ba}^{-}| \in (-\varepsilon, \varepsilon) \end{cases} \tag{5.4}$$

When Eq. 5.2 or Eq. 5.3 is fulfilled, a positive pole-to-ground fault or a negative pole-to-ground fault occurs correspondingly. The coefficients k_1 and k_2 are safety margins as well as thresholds to determine faults. On the other hand, when Eq. 5.4 is fulfilled, a pole-to-pole fault occurs, and the ϵ in Eq. 5.4 should theoretically be zero because the current traveling waves in the positive and negative pole should have the same magnitude in the pole-to-pole fault. Nevertheless, in order to eliminate the impact of noise and guarantee the successful fault detection, a close-to-zero ϵ is implemented.

5

5.1.3. SENSITIVITY ANALYSIS AND THRESHOLD DETERMINATION

The sensitivity of this method must be carefully considered when selecting the threshold. As mentioned earlier in Chapter 4, the DWT lacks translation invariance. Hence, in order to obtain an accurate DWT output in PSCAD, the thesis adopts a sampling frequency of 100kHz. In Figure 5.3, the absolute values of W_{13}^{+} and W_{13}^{-} during a negative pole-to-ground fault on Line13 are calculated as a function of fault distance. In accordance with the explanation provided concerning Eq. 5.3, it is evident that $|W_{13}^{-}|$ is always larger than $|W_{13}^{+}|$, which makes it easier to determine the threshold.

In addition, $|W_{13}^{+}|$ and $|W_{13}^{-}|$ are calculated as a function of fault resistance as shown in Figure 5.4. According to Figures 5.3 and 5.4, for each fault distance, the $|W_{13}^{-}|/|W_{13}^{+}| \in (6.33, 7.06)$, and for each fault resistance, the $|W_{13}^{-}|/|W_{13}^{+}| \in (6.99, 7.06)$. Due to the symmetry of the two poles, the similar results of $|W_{13}^{+}|/|W_{13}^{-}|$ can be obtained through the

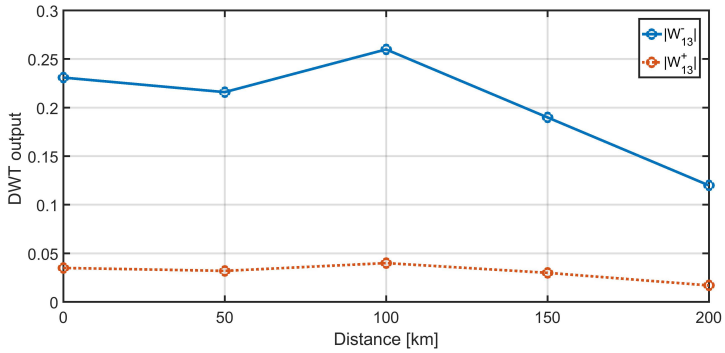

Figure 5.3: The DWT output as a function of fault distance with regard to Bus A1 (Negative pole-to-ground fault).

simulation of positive pole-to-ground faults. Thus, the k_1 and k_2 in Eq. 5.2 and Eq. 5.3 can be set to ***6***. Similarly, the sensitivity of the DWT is performed for the pole-to-pole fault, and the results are displayed in Figures 5.5 and 5.6. As mentioned before, when the pole-to-pole fault occurs, the W_{13}^{+} and W_{13}^{-} should be the same. However, upon considering a safety margin, the ϵ is set to $\boldsymbol{10^{-5}}$ in Eq. 5.4. Furthermore, in order to avoid unnecessary noise, the initial output of the DWT within ±0.002 is filtered out.

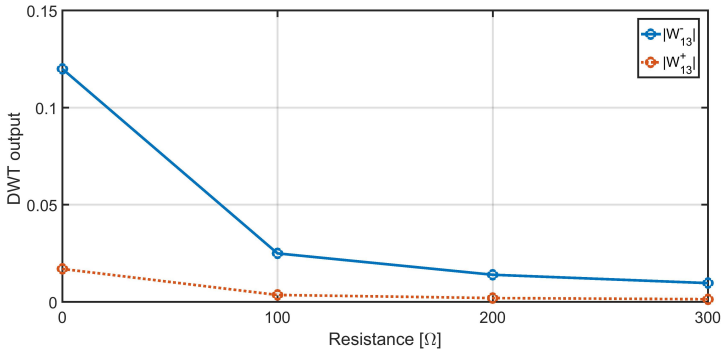

Figure 5.4: The DWT output as a function of fault resistance. Fault distance is 200km with regard to Bus A1 (Negative pole-to-ground fault).

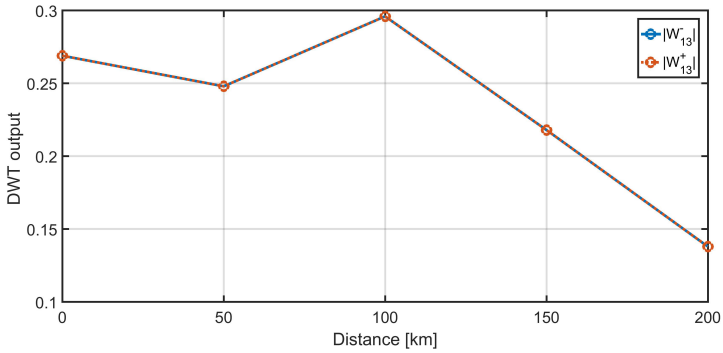

Figure 5.5: The DWT output as a function of fault distance from Bus A1 (Pole-to-pole fault).

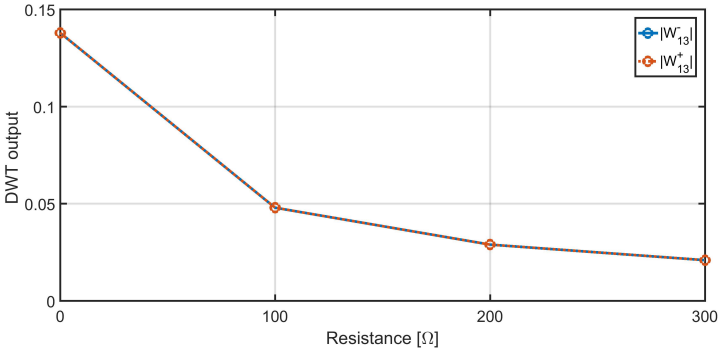

Figure 5.6: The DWT output as a function of fault resistance. The fault distance is 200km from Bus A1 (Pole-to-pole fault).

5.2. MAD-BASED DC LINE PROTECTION METHOD

In order to protect one DC line, the DWT-based method discussed in the previous section requires that there should be communication between the relays on this line. Thus, this method is associated with the concept of unit protection, and the loss of the communication channel can result in the complete protection failure. A delay in communication can also increase the system components' overcurrent stress. Therefore, for the sake of improving the protection's reliability and fast time response, a protection method without communication is proposed in this section.

5.2.1. LOCAL TRANSIENT ANALYSIS

The requirement of having communication in DWT-based protection is determined by the current traveling wave feature on the faulty line. Hence, if the communication is removed, a local fault indicator is needed. When analyzing the traveling wave on one end of a line, it becomes clear that the voltage and current at this end are sensitive to the fault. For example, when examining the solid pole-to-pole fault on Line13 in Figure 5.7, it can be seen that the incident traveling wave first arrives at the end of a faulty line and its neighboring healthy line. In this diagram, the converter is represented by equivalent C_C and L_C [8, 9].

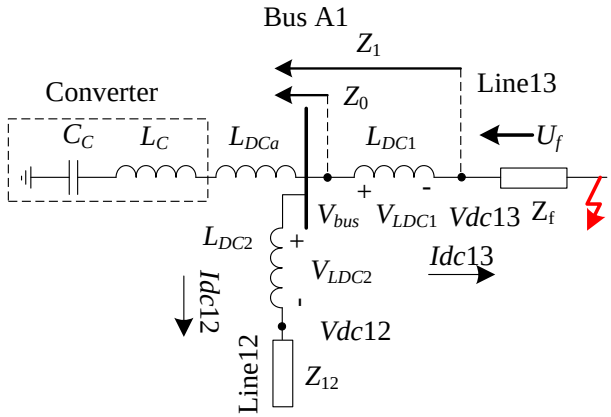

Figure 5.7: A simplified schematic of the traveling wave at the end of Line13.

If it is assumed that $L_{DC1} = L_{DC2} = L_{DCa} = L$, and based on the analysis in [9–11], it is easy to obtain the refracted surge on the positive pole in the Laplace domain that transmits through the current reactor and into the rest of the system as seen below:

$$Vdc13_{surge}(s) = -\frac{2Z_1}{Z_1 + Z_f}\frac{U_f}{s} = -\frac{2(Z_0 + sL)}{Z_0 + sL + Z_f}\frac{U_f}{s} \tag{5.5}$$

where the $U_f(t)$ is assumed to be an infinite step wave with a magnitude of $-U_f$ (negative surge), $Z_1 = Z_0 + sL$ is the equivalent impedance viewed at the line side of the current reactor, the Z_f is the characteristic impedance of the faulty line Line13, and Z_{12} is the characteristic impedance of Line12. The Z_0 represents the equivalent impedance seen

from Bus A1, which is:

$$Z_0 = (Z_C + sL) \,||\, (Z_{12} + sL)$$
$$Z_C = sL_C + 1/(sC_C) \tag{5.6}$$

The subscript "surge" refers to the waveform caused by the fault-incident surge. Then, it is possible to derive the voltage V_{LDC1} on inductor L_{DC1} in Laplace domain:

$$V_{LDC1surge}(s) = \frac{-sL}{Z_0 + sL} Vdc13_{surge}(s) = \frac{2sL}{Z_0 + sL + Z_f} \frac{U_f}{s} \tag{5.7}$$

If Eq. 5.7 is transformed into the time domain, the current *Idc*13's function of time and its first order derivative: *Idc*13′ can be deduced. However, due to the complexity of Eq. 5.6, the orders of numerator and denominator in Eq. 5.5 are high which consequently make it difficult to obtain the explicit solution of Eq. 5.7 in the time domain. Nevertheless, upon checking *Idc*13 and *Idc*12's reference directions in Figure 5.7 and their responses after the faults on Line13 occur in Figure 5.8, it is clear that the current measured on a faulty line would increase while that measured on healthy line would decrease. Therefore, the different trends of change reveal an important prerequisite for the fault detection.

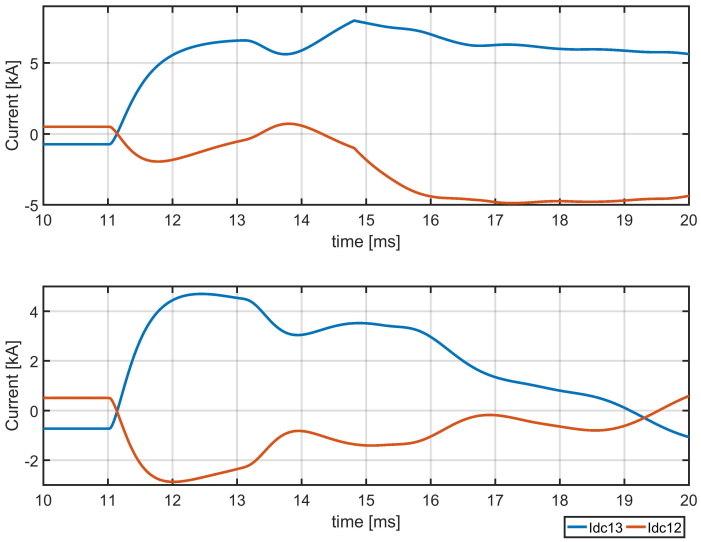

Figure 5.8: The current waveforms of *Idc*13 and *Idc*12 after a pole-to-pole fault (top plot) and a pole-to-ground fault (bottom plot). Faults occur on the middle point of Line13 at 10ms.

According to Chapter 4, when there is an outlier, the output of MAD is theoretically infinite. Therefore, during a simulation or a practical test, the exact value of the MAD output is uncertain. On the other hand, the fault-introduced surge can finally travel throughout the whole network, making it more difficult to use MAD solely for the purpose of establishing the fault detecting criterion.

Besides the current, the DC voltage can be analyzed in a similar way. As the $Vdc13_{surge}$ has been obtained in Laplace domain, $Vdc12_{surge}(s)$ can also be found in the below equation:

$$Vdc12_{surge}(s) = \frac{2Z_0Z_{12}}{(Z_{12}+sL)(Z_0+Z_f+sL)}\frac{U_f}{s} \tag{5.8}$$

Similar to Eq. 5.5, the high order of Eq. 5.8 makes it hard to explicitly calculate their time-domain functions. Nevertheless, their values at the instant when the incident surge arrives (t=0) can be estimated using the numerical method through MATLAB:

$$\begin{cases} Vdc13_{surge}(0) = -\left[(a+b)Z_f + c\right]U_f \\ Vdc12_{surge}(0) = \left[(a+b)Z_{12} - c\right]U_f \end{cases} \tag{5.9}$$

where,

$$\begin{aligned} a &= 6C_CL^2/d \\ b &= 4C_CLL_C/d \\ c &= 2Z_{12}/(Z_{12}+Z_f) \\ d &= (3C_CL^2 + 2C_CL_CL)(Z_{12}+Z_f) \end{aligned} \tag{5.10}$$

As such, it can be easily proved that:

$$Vdc13_{surge}(0) - Vdc12_{surge}(0) = -(a+b)(Z_f+Z_{12})U_f < 0 \tag{5.11}$$

This implies that due to the inductive electromotive forces in the current reactor L_{DC1} and L_{DC2}, the voltage drop at the end of Line12 is delayed. The specific time delay depends on the size of the inductors.

Although the incident surge is assumed as an ideal infinite square wave for easy explanation, it is still instructive. In practice, the waveform is determined by the propagation parameter [12, 13]:

$$A = e^{-\lambda(\omega)l} \tag{5.12}$$

This parameter is characterized by the attenuation and the time delay, which are respectively the real and imaginary parts of $\lambda(\omega)$. The initial magnitude of the incident surge at the fault location should be obtained by using the symmetrical component method [14]. The more realistic waveforms of $Vdc13$ and $Vdc12$ are simulated and demonstrated in Figure 5.9, which clearly illustrate that the voltage on the healthy line drops slower than that on the faulty line. Hence, we can take advantage of this feature as another criterion to detect a fault.

According to the above analysis and discussion, the inductor at each terminal of the line can divide the grid into different zones. The current and voltage measured between the inductor and the DC line's end provide important information regarding fault detection. Therefore, it is reasonable to define a fault in a protection zone when the current is increasing, and the voltage is quickly dropping. In this study, the inductor at each terminal is set as 100mH based on [8, 15].

It is significant to mention here that unlike the bus configuration in Figure 5.7, the bus of an MTDC system may connect more than two cables or transmission lines. However, the analysis is still valid in this case, as the current and voltage features of faulty and healthy lines should be similar to the above discussions.

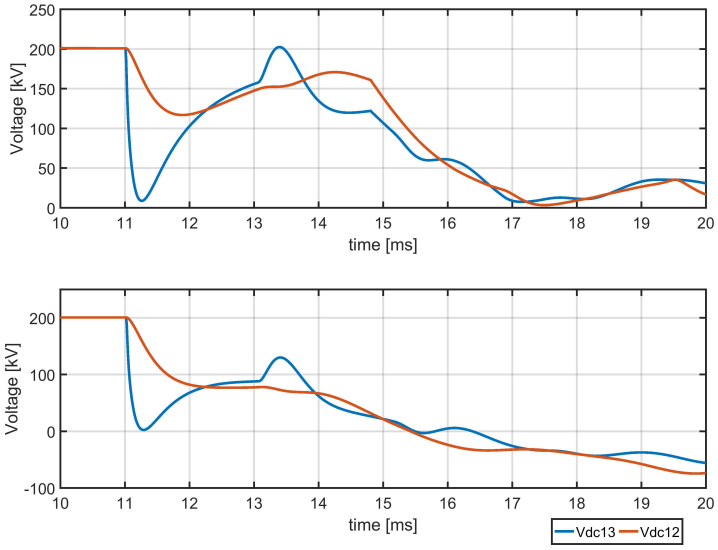

Figure 5.9: The voltage waveforms of *Vdc*13 and *Vdc*12 after a pole-to-pole fault (top plot) and a pole-to-ground fault (bottom plot). Faults occur on the middle point of Line13 at 10ms.

5.2.2. SENSITIVITY AND SELECTIVITY ANALYSIS

In order to ensure the reliability of the fault detection, the sensitivity of the proposed MAD-based method is tested on the MTDC system modeled in PSCAD. Figure 5.10 illustrates the waveforms after using MAD-1 to process the currents *Idc*13 and *Idc*12 after a pole-to-pole fault, i.e. top plot of Figure 5.8. It can be easily determined that a positive MAD-1 output implies a fault and thus a faulty line, while a negative MAD-1 output implies a healthy line. In addition, this negative MAD-1 output can be used to block the protection unit on the healthy line, thus preventing any malfunction of the protection.

Similarly, Figure 5.11 plots the results obtained by using MAD-2 to process the *Vdc*13 and *Vdc*12 after the same pole-to-pole fault, i.e. top plot of Figure 5.9. As indicated in Chapter 4, MAD-2 is sensitive to transient signals, and the results obtained are more quantifiable than those obtained through MAD-1. It can be seen that the output for *Vdc*13 drops to -1 almost immediately after the fault, which is faster than that for *Vdc*12. In addition, since the lowest possible value of MAD-2 is -1, the MAD-2 is more quantifiable than MAD-1; thus, it would be easier when selecting thresholds for MAD-2. Therefore, it is decided that processing DC current and DC voltage respectively using MAD-1 and MAD-2 with cautious thresholds can be an effective fault detecting method in an MTDC system.

Besides this case, MAD-1 and MAD-2 are analyzed with regard to the faults that take place at the boundary as well as outside of the protection zone. For example, a 50Ω pole-to-ground fault on Line13 at 200km from Bus A1, and a 0Ω pole-to-pole fault on Bus C1 have been selected to test MAD-1 and MAD-2 for Bus A1. The reason for this decision is that as in Bus A1, the relay used to protect Line13 must be able to differentiate between

internal and external faults. Although the 50Ω is chosen, in practice, the resistance could be very low since cable faults are usually bolted faults, which have almost zero resistance.

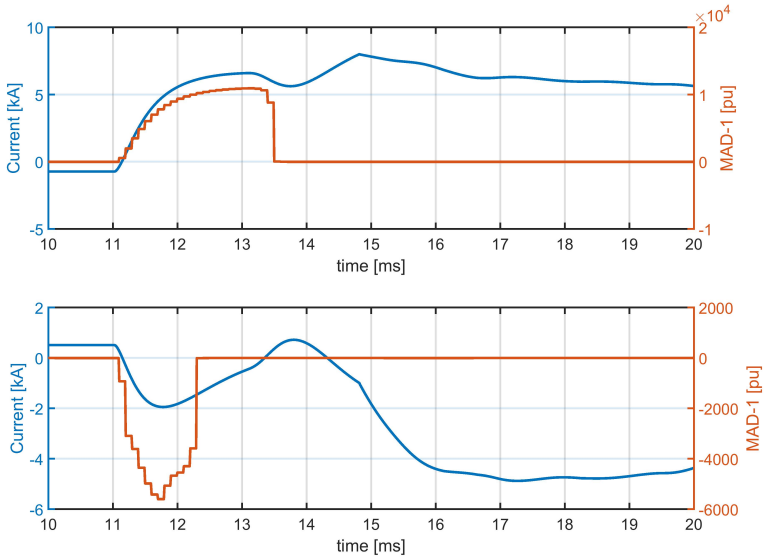

Figure 5.10: The results of using MAD-1 to process currents in Figure 5.8. Top plot: *Idc*13. Bottom plot: *Idc*12.

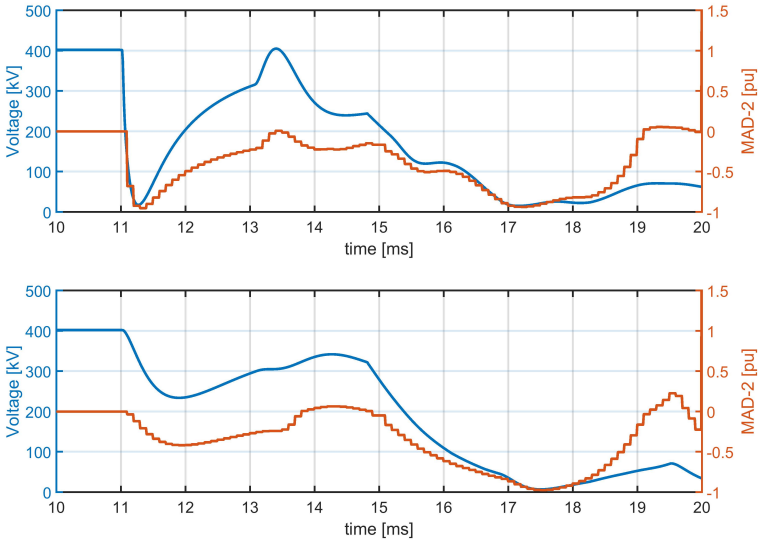

Figure 5.11: The results of using MAD-2 to process voltage in Figure 5.9. Top plot: *Vdc*13. Bottom plot: *Vdc*12.

In Tables 5.1 and 5.2, the currents and voltages on the faulty and healthy poles are monitored, and the "+" and "-" respectively stand for quantities measured on the positive and negative poles of an HVDC system. Comparing the simulation results of the faulty lines (shown in red in Table 5.1) with those of the healthy poles, it can be observed that the faulty pole has the most distinguishable results of MAD-1 and MAD-2, meaning that it would not be difficult to determine the threshold for fault detection.

	Bus A1		Bus A2		Bus C1		Bus C2	
MAD-1	$Idc13^+$	31.43	$Idc21^+$	-2.75	$Idc31^+$	69.25	$Idc43^+$	-7.29
	$Idc13^-$	222.61	$Idc21^-$	7.47	$Idc31^-$	462.99	$Idc43^-$	51.63
	$Idc12^+$	10.2	$Idc24^+$	4.59	$Idc34^+$	106.62	$Idc42^+$	34.02
	$Idc12^-$	-49.07	$Idc24^-$	-7.05	$Idc34^-$	-338.61	$Idc42^-$	-36.73
MAD-2	$Vdc13^+$	0.002	$Vdc21^+$	0.002	$Vdc31^+$	0.042	$Vdc43^+$	0.001
	$Vdc13^-$	-0.23	$Vdc21^-$	-0.01	$Vdc31^-$	-0.36	$Vdc43^-$	-0.006
	$Vdc12^+$	0.001	$Vdc24^+$	0.001	$Vdc34^+$	0.004	$Vdc42^+$	0.001
	$Vdc12^-$	-0.005	$Vdc24^-$	-0.003	$Vdc34^-$	-0.019	$Vdc42^-$	-0.003

Table 5.1: The results under a 50 Ω pole-to-ground fault on Line13 at 200km from Bus A1. Superscripts "+" and "-" respectively stand for quantities measured on the positive and negative poles of an HVDC system.

	Bus A1		Bus A2		Bus C1		Bus C2	
MAD-1	$Idc13^+$	34.02	$Idc21^+$	6.86	$Idc31^+$	-3640	$Idc43^+$	56.59
	$Idc13^-$		$Idc21^-$		$Idc31^-$		$Idc43^-$	
	$Idc12^+$	-52.64	$Idc24^+$	6.06	$Idc34^+$	-1858	$Idc42^+$	-174.14
	$Idc12^-$		$Idc24^-$		$Idc34^-$		$Idc42^-$	
MAD-2	$Vdc13^+$	-0.043	$Vdc21^+$	-0.0078	$Vdc31^+$	-0.13	$Vdc43^+$	-0.043
	$Vdc13^-$		$Vdc21^-$		$Vdc31^-$		$Vdc43^-$	
	$Vdc12^+$	-0.015	$Vdc24^+$	-0.0017	$Vdc34^+$	-0.13	$Vdc42^+$	-0.005
	$Vdc12^-$		$Vdc24^-$		$Vdc34^-$		$Vdc42^-$	

Table 5.2: The results under a 0 Ω pole-to-pole fault on Bus C1. Superscripts "+" and "-" respectively stand for quantities measured on the positive and negative poles of an HVDC system.

5.2.3. CRITERION FOR DC FAULT DETECTION

According to the simulation results in Tables 5.1 and 5.2, distinguishing between internal and external faults requires using MAD-1 to process the current signal. The first corresponding criterion is:

$$Index_I = \begin{cases} 1, S_{iMAD-1}(t) \geq 2S_{iMAD-1}(t-\Delta t) \wedge S_{iMAD-1}(t) \geq 200 \\ 0, else \end{cases} \tag{5.13}$$

This criterion ensures that only the positive outlier will be taken into consideration for a faulty line. As such, a decreasing current would never initialize a protection command, which in return can be used to block the corresponding relay unit. The dynamic threshold is automatically updated by 2 multiplying $S_{iMAD-1}(t-\Delta t)$, which is the MAD-1 output

after the last sampling. Meanwhile, the value 200 is meant to prevent any false operation caused by small load fluctuations and contingencies. According to the discussion in Chapter 4, the output of MAD-1 is hard to quantify. Therefore, it is not straight forward to calculate these two coefficients analytically. Consequently, they are heuristically determined [16] based on the data flow of MAD-1 output during simulations.

Since MAD-2 is similarly used to process the voltage signal, the second criterion is:

$$Index_V = \begin{cases} 1, S_{iMAD-2}(t) \leq S_{iMAD-2}(t-\Delta t) \wedge S_{iMAD-2}(t) \leq -0.2 \\ 0, else \end{cases} \tag{5.14}$$

Then, the fault can be detected when both Eq. 5.13 and Eq. 5.14 are simultaneously equal to 1:

$$Index_{VI} = \begin{cases} 1, Index_I = 1 \wedge Index_V = 1 \\ 0, else \end{cases} \tag{5.15}$$

In order to obtain a reliable fault detecting method, it has been decided that when either Eq. 5.13 or Eq. 5.14 becomes positive, the relay should wait a certain amount of time for the other one to become positive. This set-up is also necessary for the simulation programs and facilities of EMT type, as the solution of the branch current is calculated one time-step later than that of the nodal voltage in Dommel's algorithm [17]. In this thesis, the waiting time has been selected as 50μs.

5.3. PERFORMANCE OF DC LINE PROTECTION METHODS

In this section, the two demonstrated DC line protection methods are tested to verify their performances. The testing objectives pertain to their sensitivities to internal faults, their insensitivity to external faults, and their time responses to the faults. The two fault scenarios are as follows:

- F1: A pole-to-pole fault (fault resistance R_f is 20Ω) is applied at 10ms at the end of Line13, close to Bus C1.
- F2: A negative pole-to-ground fault (fault resistance R_f is 20Ω) is applied at 10ms at the end of Line13, close to Bus C1.

In addition, it is assumed that at both ends of each cable, there is one relay unit installed on each pole, and all the units can perform the protection algorithm. Thus, when both units on two poles pick up, the fault is identified as a pole-to-pole fault; otherwise, it is a pole-to-ground fault. The instants when commands are given based on the two proposed protection methods are summarized in Tables 5.3 and 5.4, with the former table also listing the output values of the DWT at the corresponding instants. In both tables, it is clear that both the DWT- and MAD-based methods can distinguish between internal and external faults, as only the faulty line or pole is identified. In these two tables, the superscripts "+" and "-" also indicate the quantities on the positive and negative poles respectively.

Due to the lack of translation-invariance, the sampling frequency of the DWT-based method is 100kHz, while 10kHz has been selected for the MAD-based method. According to the description of the DWT-based protection method, the relays on the two ends

	F1		
	DWT detection		Command
Bus A1	$W_{13}^{+}=-0.18$	1@11.13ms	1@11.13ms
	$W_{13}^{-}=0.18$		
	$W_{12}^{+}=0.57$	0	0
	$W_{12}^{-}=-0.57$		
Bus A2	$W_{21}^{+}=-0.08$	1@12.26ms	0
	$W_{21}^{-}=0.08$		
	$W_{24}^{+}=0.005$	0	0
	$W_{24}^{-}=-0.005$		
Bus C1	$W_{31}^{+}=-0.24$	1@10.13ms	1@12.13ms
	$W_{31}^{-}=0.24$		
	$W_{34}^{+}=0.15$	0	0
	$W_{34}^{-}=-0.15$		
Bus C2	$W_{43}^{+}=-0.018$	1@11.13ms	0
	$W_{43}^{-}=0.018$		
	$W_{42}^{+}=0.003$	0	0
	$W_{42}^{-}=-0.003$		
	F2		
	DWT detection		Command
Bus A1	$W_{13}^{+}=-0.015$	1@11.13ms	1@11.13ms
	$W_{13}^{-}=0.103$		
	$W_{12}^{+}=-0.016$	0	0
	$W_{12}^{-}=-0.072$		
Bus A2	$W_{21}^{+}=0.001$	0	0
	$W_{21}^{-}=0.01$		
	$W_{24}^{+}=-0.006$	0	0
	$W_{24}^{-}=-0.016$		
Bus C1	$W_{31}^{+}=-0.02$	1@10.13ms	1@12.13ms
	$W_{31}^{-}=0.2$		
	$W_{34}^{+}=-0.02$	0	0
	$W_{34}^{-}=-0.18$		
Bus C2	$W_{43}^{+}=0.0004$	0	0
	$W_{43}^{-}=0.019$		
	$W_{42}^{+}=-0.004$	0	0
	$W_{42}^{-}=-0.015$		

Table 5.3: The performance of the DWT-based protection method. Superscripts "+" and "-" respectively stand for quantities measured on the positive and negative poles of an HVDC system.

of one DC line must communicate with each other. For example, on Line*ij*, the unit generating W_{ij}^{+} is required to communicate with that generating W_{ji}^{+}. Hence, although the fault is close to Bus C1 on Line13 in Table 5.3, the command can only be made when the DWT information from the other end (Bus A1) is received. Consequently, the protection unit at Bus C1 can detect the fault at 10.13ms, but the command is initialized at 12.13ms.

	F1				
	$Index_I$		$Index_V$		Command
BusA1	$Idc13^+$	1@11.1ms	$Vdc13^+$	1@11.1ms	1@11.1ms
	$Idc13^-$		$Vdc13^-$		
	$Idc12^+$	0	$Vdc12^+$	0	0
	$Idc12^-$		$Vdc12^-$		
BusA2	$Idc21^+$	1@12.3ms	$Vdc21^+$	0	0
	$Idc21^-$		$Vdc21^-$		
	$Idc24^+$	0	$Vdc24^+$	0	0
	$Idc24^-$		$Vdc24^-$		
BusC1	$Idc31^+$	1@10.1ms	$Vdc31^+$	1@10.1ms	1@10.1ms
	$Idc31^-$		$Vdc31^-$		
	$Idc34^+$	0	$Vdc34^+$	0	0
	$Idc34^-$		$Vdc34^-$		
BusC2	$Idc43^+$	0	$Vdc43^+$	1@11.6ms	0
	$Idc43^-$		$Vdc43^-$		
	$Idc42^+$	0	$Vdc42^+$	1@13.4ms	0
	$Idc42^-$		$Vdc42^-$		
	F2				
	$Index_I$		$Index_V$		Command
BusA1	$Idc13^+$	0	$Vdc13^+$	0	0
	$Idc13^-$	1@11.2ms	$Vdc13^-$	1@11.2ms	1@11.2ms
	$Idc12^+$	1@11.2ms	$Vdc12^+$	0	0
	$Idc12^-$	0	$Vdc12^-$	0	0
BusA2	$Idc21^+$	0	$Vdc21^+$	0	0
	$Idc21^-$	1@12.3ms	$Vdc21^-$	0	0
	$Idc24^+$	0	$Vdc24^+$	0	0
	$Idc24^-$	0	$Vdc24^-$	1@14.7ms	0
BusC1	$Idc31^+$	0	$Vdc31^+$	0	0
	$Idc31^-$	1@10.1ms	$Vdc31^-$	1@10.1ms	1@10.1ms
	$Idc34^+$	0	$Vdc34^+$	0	0
	$Idc34^-$	0	$Vdc34^-$	1@12.2ms	0
BusC2	$Idc43^+$	0	$Vdc43^+$	0	0
	$Idc43^-$	0	$Vdc43^-$	0	0
	$Idc42^+$	0	$Vdc42^+$	0	0
	$Idc42^-$	0	$Vdc42^-$	0	0

Table 5.4: The performance of the MAD-based protection method. Superscripts "+" and "-" respectively stand for quantities measured on the positive and negative poles of an HVDC system.

Here, it is assumed that the communication delay is 1ms for the 200km cable [18].

It is also evident that the DWT-based protection can detect the fault F1 at Bus A2 and Bus C2, as the W_{21}^+, W_{21}^-, W_{43}^+, and W_{43}^- are all equal to 1 respectively at 12.26ms and 11.13ms. Nevertheless, there are no positive signals from the corresponding W_{12}^+, W_{12}^- and W_{34}^+, W_{34}^-, thus meaning that there are no commands for Line12 and Line34.

By contrast, in Table 5.4, due to the independently working relay unit, the MAD-based protection can respond more quickly to the fault than the DWT-based one. For example, the commands for a faulty line can be made in Bus C1 at around 10.1ms, which is 2ms faster than that when using DWT-based protection. In the meantime, because of the propagation of the traveling wave, some single $Index_I$ or $Index_V$ values of relay units on healthy lines could react to the faults as well. However, since their corresponding $Index_V$ or $Index_I$ values stay unchanged, no commands are given to the healthy lines.

5.4. CURRENT DIFFERENTIAL DC BUS PROTECTION METHOD

In the previous two sections, the protection methods discussed have aimed at protecting the DC lines, which are cables in the MTDC model. Based on the concept of selectivity, they are not designed to protect the DC buses, such as the Bus A1, A2, C1 and C2. According to the bus configuration in Figure 5.1, it is feasible to adopt the current differential protection based on the branch currents flowing through one bus. As such, the theoretical criterion is:

$$\begin{aligned} I_{diffx} &= Idcx - \sum Idcxy(x, y = 1,2,3,4, x \neq y) \\ Index_{diff} &= \begin{cases} 1, I_{diff} \neq 0 \\ 0, I_{diff} = 0 \end{cases} \end{aligned} \tag{5.16}$$

where the x and y stand for the numbers that denote the currents in Figure 5.1.

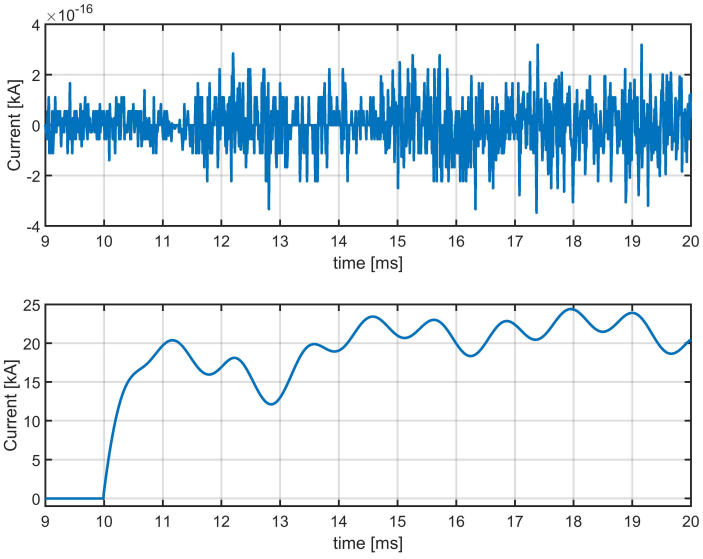

Figure 5.12: I_{diff} for Bus A1 during fault F3 (top plot) and F4 (bottom plot).

Aside from its simplicity, another main reason for the decision to implement the current differential protection is that the three measured currents are "close" to each other,

which means the Kirchhoff's current law (KCL) is always valid without the need to consider the possible time delay and current attenuation caused by a long cable. Figure 5.12 plots the I_{diff1} of Bus A1 under two faults:

- F3: A pole-to-pole fault applied at 10ms at the end of Line13.
- F4: A pole-to-pole fault applied at 10ms at Bus A1.

It is noticeable that I_{diff} is extremely sensitive to the bus fault but immune to other faults. This inherent selectivity is determined by the KCL of currents flowing through a bus. Consequently, it is unnecessary to consider the algorithm as complex as those for the DC line protection. The spikes in the top plot of Figure 5.12 are caused by the numerical computation in EMT type programs. In order to avoid the false activation, the bus protection will be triggered using the below index:

$$Index_{diff} = \begin{cases} 1, I_{diff} = 1kA \\ 0, else \end{cases} \tag{5.17}$$

5.5. LIMITATION

The performances of each protection method are demonstrated by the simulation results. However, since the underground cable system is considered for the MTDC system modeled in the software, the accounted faults are caused by short-circuits between the pole and ground, and between two poles. However, when an overhead line (OHL) system is implemented to the MTDC system, it could be exposed to lightning strokes.

Since the lightning can also cause surge on the transmission line, the proposed WT-based and current differential methods cannot distinguish the lightning-caused traveling wave, and especially, the polarity of impulse voltage resulted from lightning can be either same as or opposite to the DC voltage [19, 20]. Thus, these two methods require more considerations and improvements to solve this problem. Similarly, since the typical lightning surge is a 1.2/50μs waveform, even though the implemented MAD-based protection uses a sampling frequency of 10kHz which means the signal is sampled every 0.1ms, there is a high possibility that the signal of lightning-caused surge would be recorded into the dataset of MAD. When the MAD-based method uses a higher sampling frequency, this possibility would increase.

5.6. CONCLUSION

In Chapter 4, two data processing methods are selected for fault detection: the DWT and MAD. Based on the traveling wave theory, the DWT-based protection method is discussed in this chapter. In order to detect the fault, it uses different polarity features of incident current traveling waves on faulty and healthy lines. Additionally, it uses the quantitative relations of WT outputs $|W^+_{ab}|/|W^-_{ab}|$ and $|W^+_{ba}|/|W^-_{ba}|$ to identity fault types, i.e., pole-to-pole fault and pole-to-ground fault.

Successful fault detection based on the DWT-based method is dependent on obtaining the initial wavelet output as it contains important polarity information. In order to ensure the accuracy of the DWT, a high sampling frequency of 100kHz is adopted. By using a high sampling frequency, the DWT's lack of translation-invariance can be avoided.

However, high sampling frequency could bring extra cost in practice. At the same time, the inevitable noise in the system can affect the results of transformation. Even though the SWT can remove the noise [21], and it is naturally invariant to translation, its relatively high requirement of storing required data samples still makes it "expensive" to use for fault detection.

In practice, because of the communication delay in DWT-based protection, the action units (e.g., DC circuit breakers) installed at the bus must be designed to have a higher rate as they otherwise may not survive the overcurrent. If the realistic communication delay is longer than that assumed in this thesis (i.e., 1ms), the DCCB will suffer high current for a longer period.

In order to remove the protection system's dependence on long-distance communication, a MAD-based method is introduced as well. This method can detect the DC side fault in around 1ms with a limited number of samples of DC voltage and current. More importantly, the voltage and current signals are sampled locally with a low frequency, i.e., 10kHz. Therefore, this novel protection method has high reliability and low requirements. In addition, by eliminating the need for the relays to communicate on the cable's remote ends, the fault detection is much faster, as demonstrated in the simulation results.

This chapter has additionally showed that the proposed MAD-based method becomes less efficient when the fault resistance is higher than 50Ω. The reason for this is that a transient signal is declined because of a high fault resistance which cannot be easily characterized by MAD. On the contrary, the DWT-based method can detect a fault with resistance as high as 300Ω. Thus, if the main protection implements MAD-based protection, then the DWT-based one could be used as a "backup" form of MAD-based protection; however, in the Chapter 7, "backup" protection is referred with other purpose, so the DWT-based protection would be referred to as an ancillary of the main protection. Although the latter has a longer protection time, the system experiences a lower overcurrent stress because of higher fault resistance. Although cables are used in the modeled MTDC system, it is important to acknowledge that usage of the transmission line system is suitable in both of these two methods to detect the considered types of faults.

The demonstrated DC bus protection applies the concept of current differential protection. The condition for this application is the lumped circuit at each bus bar. Therefore, the KCL is always provided without the need to consider any time delay caused by the distributed circuit, i.e., a long cable or an OHL. This concept will be applied in Chapter 7 to establish the entire protection scheme.

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6

DESIGNING AND CALIBRATING THE DC CIRCUIT BREAKER MODEL

The DCCB is the major unit to interrupt the fault current then isolate the fault, and this chapter discusses how to embed the DCCB into an MTDC network. Due to the complex configuration of an MTDC network, a relay unit requires that a certain number of DCCBs protect predefined areas, i.e., protection zones. In an MTDC network, depending on the fault distance and resistance, the fault currents are quite different under transmission line faults and DC bus faults. In addition, the DCCB's performance relies on other factors, such as the mechanical delay, and the critical di/dt of the injecting current. Therefore, the specific requirements for one DCCB must be localized. Although there are different types of DCCBs, the mechanical DCCB is presented, and its design and calibration are discussed comprehensively in this chapter.

6.1. A BASIC UNDERSTANDING OF THE MECHANICAL DCCB

CURRENTLY, one of the most important topics in HVDC research is the reliability of fault current interruption. Although the DC faults in a point-to-point HVDC link can be adequately isolated by the conventional ACCBs installed on the converter's AC side, this is not an option for the MTDC network because it may cause the loss of the whole DC network. Unlike that in AC systems, the fault current in a DC system cannot naturally decrease to zero. In other words, isolating a fault on the DC side necessitates the artificial creation of zero-crossing points in the fault currents, which additionally gives rise to the idea behind the conceptual design of the DCCB. Besides the zero-crossings in the current, the successful fault interruption also requires a DCCB to be capable of dissipating the magnetic energy stored in DC system's inductors and withstanding the electrical strength of the transient interruption voltage (TIV) [1].

Although there are DCCBs available for low- and medium-voltage applications, only transfer and load current switches are in use for the HVDC application [2]. The CBs that are used for HVDC fault current interruption are not commonly available, or they have limited ranges. There are different types of CBs for the HVDC systems, such as the mechanical DCCB [3] and the hybrid DCCB [4, 5]. Although they belong to different categories, they are similarly configured as both contain a switching element in the nominal path to build the voltage withstand capability, a commutation path to create the current zero which is usually an inductor-capacitor (LC) oscillating circuit, and an absorber path to dissipate the stored energy [6]. As a large number of semiconductors in hybrid DCCBs require considerable investment, this chapter only discusses the mechanical DCCB. Its configuration is shown in Figure 6.1 [3], which highlights the above-mentioned three paths.

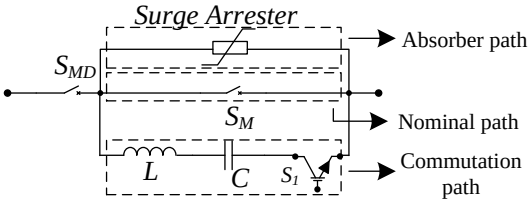

Figure 6.1: The typical configuration of a mechanical DCCB.

6.2. OPERATING PRINCIPLE OF MECHANICAL DCCB

For a general understanding, Figure 6.2 illustrates the operation of a mechanical DCCB during fault current interruption. The figure also specifies the major components of a DCCB including a high speed mechanical vacuum interrupter (S_M), a paralleled resonant branch (L, C, S_1) with a surge arrester, and a residual current circuit breaker (S_{MD}).

The procedure in which the DCCB interrupts the short-circuit current begins when the switch S_M is activated after receiving a trip signal from the relay unit. When its contacts have separated from one another by a sufficient distance to withstand the applied transient voltage during interruption, the resonant circuit injects a counter-current by

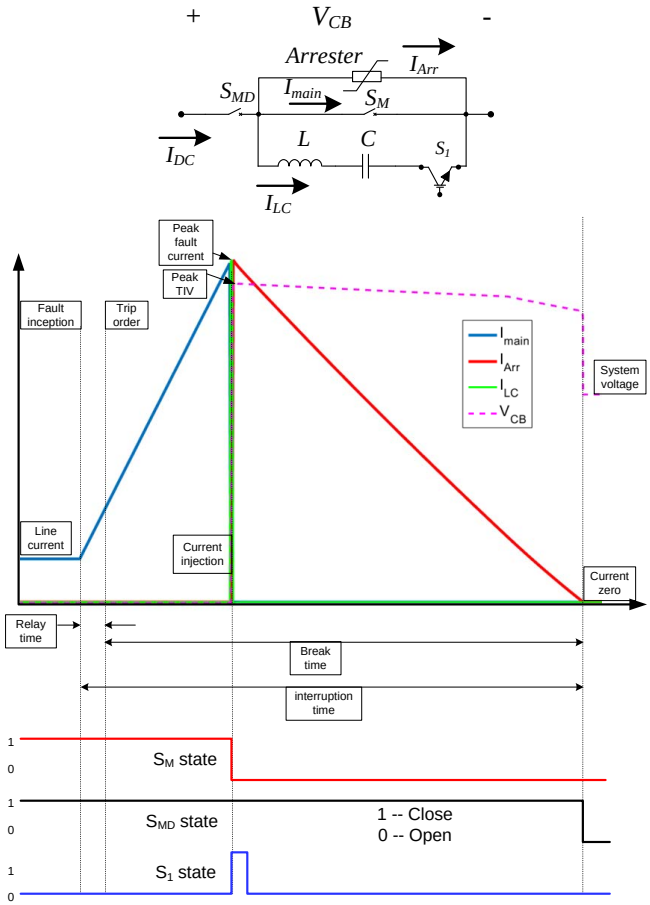

Figure 6.2: The operating principle of the mechanical DCCB.

turning on switch S_1. This generates a current of zero within the interrupter S_M, and all the current now flows through the resonant branch, which results in the V_{CB} first rises negatively with a very steep rate and then increases in the opposite direction with $du/dt = I/C$. As Figure 6.2 is an illustration showing instants and the variation of the current during the interruption process, this negative spike has not been the point of discussion. When the clamping voltage of arrester is reached, the current flowing through the circuit breaker begins to decrease rapidly.

Then, the energy stored in the system dissipates in the arrester over a period of time which depends on the system conditions. When the DC breaker current passes through zero, the residual current circuit breaker S_{MD} becomes an open circuit, providing galvanic isolation of the circuit breaker from the rest of the network.

6.3. FACTORS INFLUENCING THE DCCB

Since the DCCB is composed of different components, its function is determined by these components' features. Hence, it is necessary to take them into account in the process of designing and modeling a DCCB.

6.3.1. THE INJECTED CURRENT SLOPE

The injected current slope or gradient (*di/dt*) plays an important role in the functioning of the ACCB, during the quenching of the high-frequency current at its zero-crossings. The limit between the interruption and reignition of the high-frequency current has been expressed as a critical *di/dt* value, beyond which the interruption cannot occur [7–10]. The same phenomenon can also happen during the interruption of the DC fault current [7], even though the zero-crossing has been artificially created by the commutation path of the DCCB.

Figure 6.3 demonstrates the injected currents of one DCCB when it interrupts two DC fault currents with the amplitudes of 5kA and 15kA. The *di/dt* of the injected current at the zero-crossing point in each case is also marked in Figure 6.3, where it is observable that the *di/dt* in the 5kA-scenario is higher than that in the 15kA-scenario. In practice, the critical *di/dt* value of a vacuum switch is 150-1000A/µs [11].

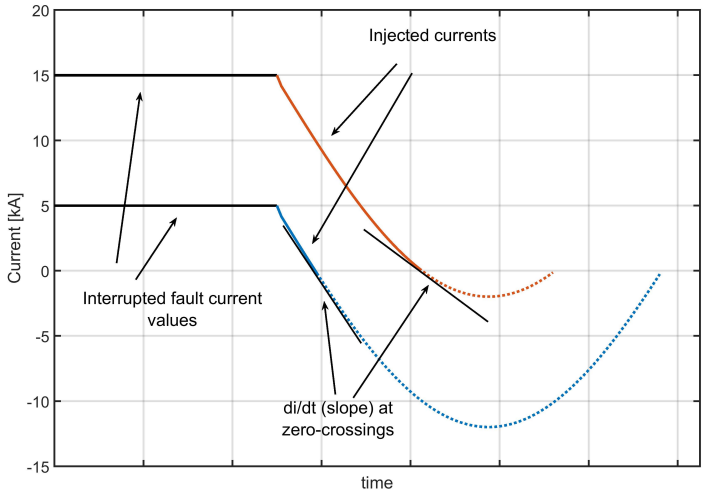

Figure 6.3: The DCCB interrupting different fault currents.

In an MTDC system, the range of the fault current amplitude can be very large depending on the system configuration in terms of the number of terminals and the topology of the transmission system. Therefore, in order to design a reliable DCCB, the applied LC circuit must be calibrated to meet the vacuum switch limits of *di/dt* for all the possible fault currents in the DCCB's protection zone.

In addition, one can also use the DCCB to disconnect an OHL or a cable during its

normal operation for the purpose of maintenance. However, an LC circuit is always designed to interrupt the fault current so that it can fail to interrupt the load current. Since the load current can be ten times lower than the fault current, the gradient at the instant of interrupting the load current may possibly exceed the mentioned critical range. Hence, avoiding this problem necessitates considering an auxiliary LC circuit for the maintenance of the DC line.

6.3.2. THE CHOPPING CURRENT

The chopping current is an important feature of a vacuum switch. The arc in a vacuum can be extinguished directly when the current is lower than the chopping current, and its value can be roughly approximated in AC systems [7]. In this chapter, the considered chopping current is obtained from experiments with the contact material CuCr55 [12], which is the most common contact material used in a high voltage vacuum interrupter. The chosen values are demonstrated and discussed in a later section.

6.3.3. THE DELAY OF SWITCH OPENING

Once a signal is sent to trip a DCCB, there is always a time delay before the mechanical devices are activated. However, due to the aging and the DCCB's physical system, the duration of this time delay can be random, albeit within a range of several milliseconds in practice. Since the DC fault current can increase in a very short period, this time delay can influence the actual current interrupted by the DCCB. In this chapter, it is assumed that the actual activating time is randomly between the range of 5.5ms and 6ms based on [3]. In addition, the delay is set to follow the normal distribution.

6.4. OPTIMIZED ALGORITHM FOR DESIGNING AN LC CIRCUIT

When considering the aforementioned factors, it is possible to obtain the ideal boundary of an injected current gradient when the DCCB successfully interrupts the DC fault current at instant T_i, whose values are represented as follows:

$$0 \leq \frac{di_{LC}(T_i)}{dt} = \frac{U_C}{L}\cos\left(\frac{1}{\sqrt{LC}}T_i\right) \leq S_{\max} \tag{6.1}$$

$$0 < T_i \leq \frac{\pi\sqrt{LC}}{2} \tag{6.2}$$

where, respectively, the $i_{LC}(t)$ represents the function of the injected current in the time domain, the U_C and S_{max} stand for the voltage of the capacitor and the desired di/dt at the instant of injection, and the L and C are the inductance and capacitance of resonant branch.

It is also important to note that the interruption should always take place within the i_{LC}'s first quarter of a cycle during which the function of di_{LC}/dt is monotonically decreasing. Then the maximal value of C becomes:

$$\frac{T_i^2}{L} < C \leq \frac{T_i^2}{L\arccos^2\left(LS_{\max}/U_C\right)} \tag{6.3}$$

In practice, Eq. 6.1 cannot be equal to 0 to guarantee successful interruption before i_{LC} reaches its maximum I_{max}. If the assumption is that the inductance L, S_{max}, and U_C are predefined constants (U_C is always the system voltage), then the capacitor size is the function of the instant of interruption. However, the inductance and the capacitance can influence the interrupting instant T_i in return, making it difficult to find the specific required capacitor value. As such, an iteration process is necessary, and it is proposed in the following steps:

1. First, according to Eq. 6.1,the minimum inductance L_{min} of LC circuit can be assumed to be:
$$L = \frac{U_C}{S_{\max}} = L_{\min} \tag{6.4}$$
This equation is derived from Eq. 6.1 based on the critical condition shown by the following inequality:
$$\cos\left(\frac{1}{\sqrt{LC}} T_i\right) \leq \frac{LS_{\max}}{U_C} \leq 1 \tag{6.5}$$

2. Then, based on the maximum current I_{max} of a transmission line or a cable end, and a certain safety margin K, the range of capacitance C of the LC circuit can be obtained:
$$C = \frac{(KI_{\max})^2 L}{U_C^2} \tag{6.6}$$
In Eq. 6.6, the L is a fixed value, making C proportional to KI_{max}. The coefficient K determines the peak current that the LC circuit can achieve. It could be set as 2 for a 100% margin [13], in which case the circuit breaker is more than capable of coping with an unexpected situation, such as a time delay in the functioning of the main switch.

3. Thereafter, with a given fault current I_{fault}, the instant of interruption T_i and gradient S at this instant can be obtained respectively from Eq. 6.7 and Eq. 6.8:
$$T_i = \sqrt{LC} \arcsin\left(\frac{I_{fault}\sqrt{L/C}}{U_C}\right) \tag{6.7}$$
$$S = \frac{U_C}{L} \cos\left(\frac{1}{\sqrt{LC}} T_i\right) \tag{6.8}$$

4. When S from Eq. 6.8 is lower than S_{max} or the predefined limit, the range of the LC circuit's natural frequency is obtainable according to Eq. 6.4 and Eq. 6.6 in the following equation:
$$f = \frac{1}{2\pi\sqrt{LC}} \tag{6.9}$$

5. Lastly, if the frequency is found to be within a defined range, the calculated inductance and capacitance meet the requirements pertaining to the preferred *di/dt*. Otherwise, it would be prudent to repeat all the previous steps from beginning with a new minimum inductance.

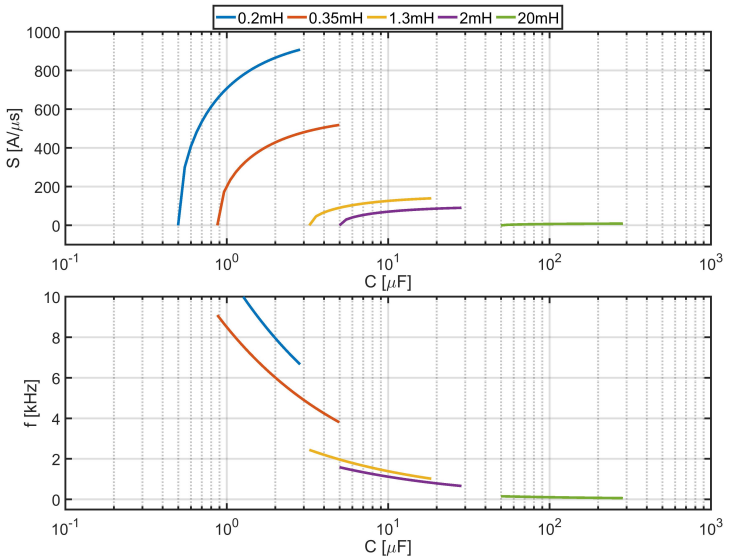

Figure 6.4: The results of the optimized algorithm with regard to the capacitances under different L_{min} values.

Figure 6.4 shows five sets of results obtained from the applied algorithm, which is assumed to interrupt a 10kA fault current in a ±200kV system. In addition, the KI_{max} of the LC circuit is selected as 2×12kA, which leaves the margin coefficient as K=2. Derived from Eq. 6.6, the largest chosen C is $(24^2 L_{min}/200^2)\mu$F. At the same time, the smallest C is $(10^2 L_{min}/200^2)\mu$F, which ensures that the arcsine function in Eq. 6.7 is within the domain (0,1], otherwise Eq. 6.8 will have complex solutions, and it physically means the C is too small to generate high enough current for fault interruption.

Figure 6.4 clearly shows the *di/dt* at the instant of interruption for different values of L and C. It is evident that defining L_{min} in Eq. 6.4 can set a hard limit on the *di/dt* at the interruption instant. It is also important to note here that when the KI_{max} is higher than 64kA, the selected minimal inductances in Figure 6.4 would respectively result in the mathematical upper limits of S_{max}: 1000A/μs, 571A/μs, 154A/μs, 100A/μs, and 10A/μs. Since another boundary of this algorithm is the natural frequency of the LC circuit, only the frequencies between the range of 3kHz to 6.5kHz are chosen in this chapter.

6.5. FAULT CURRENT RANGES

The estimated maximum and minimum current values are two crucial inputs of the optimization algorithms as they determine the LC circuit of a DCCB. In this thesis, this range of the fault current is obtained using DC-side fault simulations on a cable in a 4-terminal DC grid. In order to evaluate the critical pressure of the DCCB, the MTDC system adopts the topology similar to the one in [14], and the load flow is determined based on the test system DCS2 in [15].

6.5.1. DESCRIPTION OF THE STUDIED SYSTEM

The configuration of the studied MTDC system is shown in Figure 6.5, which is a 4-terminal symmetric monopole HVDC system (±200kV). The converter Cm-F1 connects the offshore wind power plant, and Cm-E1 connects the offshore oil and gas platform, with the rest of the onshore systems modeled as infinite buses. The system is modeled in PSCAD environment, and the data of this system are provided in Table 6.1.

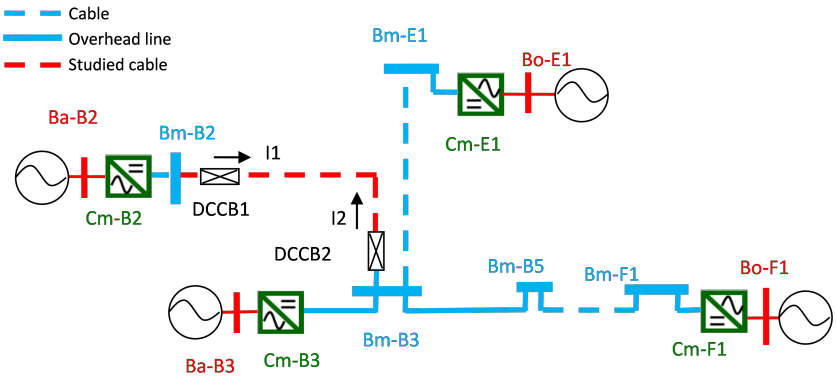

Figure 6.5: The configuration of the studied MTDC system.

AC system		DC system	
Bus name	RMS voltage	Converter name	Control mode and setting points
Ba-B2	380kV	Cm-B2	P/V_{dc}: P_{ref}=400MW, V_{dcref}=±200kV, droop=0.2
			Q: Q_{ref}=0MVAR
Ba-B3		Cm-B3	P/V_{dc}: P_{ref}=-800MW, V_{dcref}=±200kV, droop=0.2
			Q: Q_{ref}=0MVAR
Bo-E1	145kV	Cm-E1	P/V_{dc}: P_{ref}=-100MW, V_{dcref}=±200kV, droop=0.2
			Q: Q_{ref}=0MVAR
Bo-F1		Cm-F1	P: P_{ref}=500MW
			Q: Q_{ref}=0MVAR

Table 6.1: The data of the studied system.

The fault is applied on the 200km XLPE cable between DC buses Bm-B2 and Bm-B3. Two CBs are installed respectively on this cable's two ends: DCCB1 and DCCB2 [1]. More importantly, the directions of the LC injected currents for DCCB1 and DCCB2 are respectively aligned with the directions of I1 and I2 in Figure 6.5. The parameters of the studied cable are same as those in Figure 4.5, which is derived from [16]. This cable has

[1] In this thesis, the locations of the DCCBs are chosen in order to show its model's performance and may not related to a actual situation.

been chosen because the fault current would be contributed to only by the converter Cm-B2 at the terminal of Bm-B2, while it would be contributed to by three feeders from the terminal of Bm-B3. The multiple contributions are the representative feature of an MTDC grid, and when a fault occurs on the studied cable the three healthy feeders at Bm-B3 may increase the fault current experienced by DCCB2.

6.5.2. SIMULATION OF FAULTS AT DIFFERENT LOCATIONS

A series of fault scenarios are simulated on the studied cable, and the fault is a permanent metallic pole-to-pole fault that is applied at different locations at 10ms. Additional details are listed in Table 6.2 below.

Fault scenario	Description
Fault A	0km away from Bm-B2.
Fault B	20km away from Bm-B2.
Fault C	80km away from Bm-B2.
Fault D	120km away from Bm-B2.
Fault E	180km away from Bm-B2.
Fault F	200km away from Bm-B2.

Table 6.2: The simulated fault cases.

The I1 and I2 are the currents flowing through DCCB1 and DCCB2 respectively, and their simulation results are demonstrated in Figure 6.6. It is noticeable that the fault location influences the amplitudes of fault currents I1 and I2 as the closer the fault is to one end of the DC line, the larger the measured current is at that end. On the other hand, the three healthy feeders on Bm-B3 clearly contribute to the I2 as the highest value of I2 is almost twice that of I1. Therefore, the rating of the prospective DCCB2 should be higher than that of the prospective DCCB1.

Assuming the fault can be detected instantly by the MAD-based method when the incident surge arrives at the cable end, one can find the fault current that needs to be interrupted by the DCCB, depending on the random mechanical time delay and the time delay caused by the traveling wave. The estimated interruption time intervals are tabulated in Table 6.3 for the most and least severe fault cases: for the DCCB1, they are respectively Fault A and Fault F, while vice versa for the DCCB2. The table also shows the range of fault currents in the corresponding time intervals. The time interval in this table accounts the mechanical time delay defined previously and the time delay caused by traveling wave in the studied cable is around 1.015ms, which is computed by the Line Constants Program (LCP) in PSCAD.

Interrupting time interval		Interrupting current interval
DCCB1	[0.0155s 0.017015s]	[5.870kA 12.52kA]
DCCB2	[0.0155s 0.017015s]	[7.873kA 21.36kA]

Table 6.3: An estimation of fault current ranges.

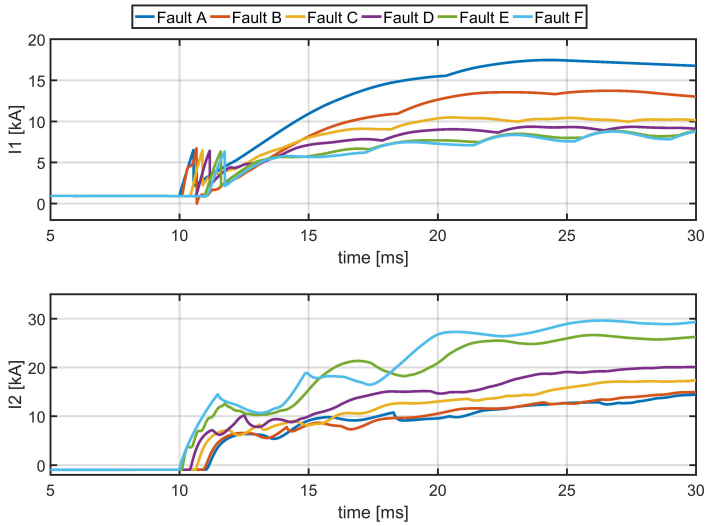

Figure 6.6: The simulation results of the fault currents at two ends of the studied cable.

6.6. PERFORMANCE OF THE DCCBS

6.6.1. DESIGNING THE LC CIRCUIT WITHOUT CONSIDERING *di/dt*

In accordance with the fault current ranges in Table 6.3, the LC circuits of DCCB1 and DCCB2 are shown in Table 6.4. The configuration of the circuit breakers is as shown in Figure 6.2, where an IGBT S_1 is used to control the current injection through the commutation path. It is assumed that the vacuum switch S_M cannot open when *di/dt* is higher than a critical value, which is set to 650A/μs. The arrester's data are obtained from [17]: the rated voltage is 243kV, and the maximum continuous operating voltage (MCOV) is 175kV. The chopping currents of S_M and S_{MD} are defined as 32A [12] and 10A [3] respectively, and the control loop and logic of the DCCB are designed based on [3] and [18].

Parameter	DCCB1	DCCB2
Capacitor	7μF	
Inductor	0.2mH	
Frequency	3.97kHz	
U_C	200kV	
I_{max}	37.42kA	

Table 6.4: The configurations of the two DCCBs.

The performance of DCCB2 in scenario Fault E is shown in Figure 6.7, where it is evident that the injected current cannot interrupt the fault due to the high *di/dt*. In practice, the arc in the vacuum switch cannot vanish, and it is quite likely that it will actually reignite instead. As a result, the main current flowing through the vacuum interrupter

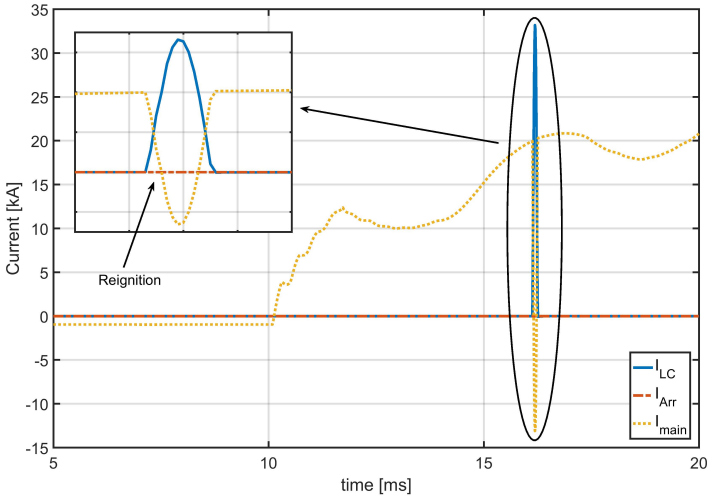

Figure 6.7: The performance of the DCCB2 before optimizing.

cannot commute into the energy absorption branch. In order to avoid this kind of failure, the design of the LC circuit must take its *di/dt* into account.

6.6.2. OPTIMIZING THE LC CIRCUIT CONSIDERING *di/dt*

Similarly, according to Table 6.3 and a pre-assumed maximal di/dt=571A/μs, the DCCB1 and DCCB2 are calibrated optimally. The results are shown in Table 6.5, where the "main" LC circuit references in the title is to be distinguished from the "auxiliary" LC circuit discussed in the next paragraph. On the other hand, the maximum injected current I_{max} of the LC circuit is higher than the estimated maximum fault current, which is around a 54% margin for both DCCB1 and DCCB2. Although making a 100% margin is recommended in [13], the margins used for the optimized DCCBs suffice.

Parameter	DCCB1	DCCB2
Capacitor	5μF	9μF
Inductor	0.35mH	
Frequency	3.8kHz	2.8kHz
U_C	200kV	
I_{max}	23.9kA	32.1kA
di/dt_{max}	571A/μs	

Table 6.5: The DCCBs after optimization: the main LC circuits.

As mentioned previously, a DCCB can also be used to disconnect an OHL or a cable for purpose of the maintenance during its nominal operation. Therefore, the auxiliary LC circuits are calibrated for this aim in Table 6.6. As the nominal power (±200kV×0.95kA=380MW)

Parameter	DCCB1	DCCB2
Capacitor	0.2μF	
Inductor	0.35mH	
Frequency	19kHz	
U_C	200kV	
I_{max}	4.78kA	
di/dt_{max}	571A/μs	

Table 6.6: The DCCBs after optimization: the auxiliary LC circuits.

flows from Bm-B2 to Bm-B3, the auxiliary LC circuits of DCCB1 and DCCB2 are chosen to inject current that aligns with the direction of I1, which means that DCCB2 needs to be bidirectional to interrupt the currents that are directionally opposite to each other under the faulty and normal conditions [2]. In fact, having DCCBs with bidirectional interruption capability is necessary for an MTDC network [19]. However, it is not discussed in detail here because it is beyond the scope of this chapter.

6.6.3. PERFORMANCE OF THE OPTIMIZED DCCBS

The optimized configuration of the DCCB is shown in Figure 6.8. The main and auxiliary LC circuits have been combined and thus share one inductor. Therefore, when the switch S_C is closed, the capacitance will be C_1+C_2, and they are used to interrupt the fault current. However, when S_C is opened, the capacitance will only be C_2, and it is used to interrupt the load current. As C_2=0.2μF, the C_1 of DCCB1 and DCCB2 is 4.8μF and 8.8μF respectively. The switch S_C can be controlled using another independent signal, e.g., a maintenance signal given by the system operator. Similar functionality is also provided by the hybrid DCCB [20].

For the clear explanation and demonstration, one more IGBT (S_2) is anti-paralleled with S_1 in DCCB2 so that it can also interrupt the current that flows oppositely to the reference direction.

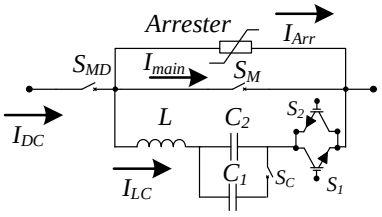

Figure 6.8: The configuration of the optimized DCCB.

INTERRUPTING FAULT CURRENTS

Figures 6.9 and 6.10 demonstrate the successful fault interruption concerning the two circuit breakers. For the sake of consistency, the fault is located with respect to Bm-B2 as

[2] By contrast, if it is chosen to align with the direction of I2, then DCCB1 has to be bidirectional.

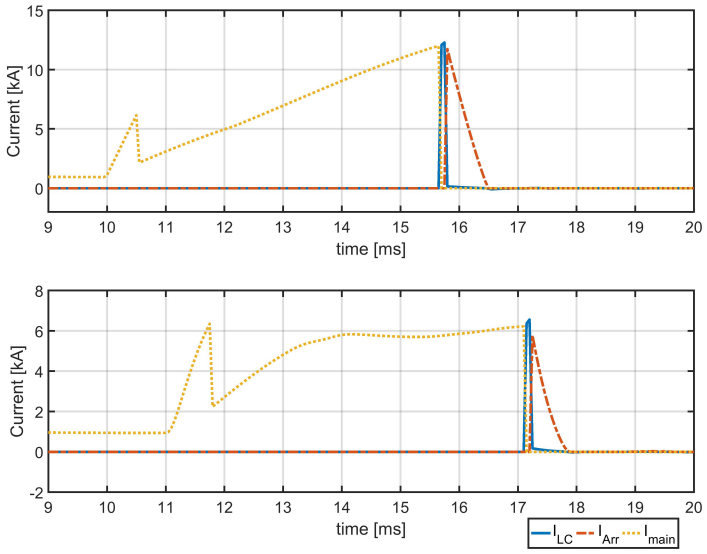

Figure 6.9: The performance of DCCB1 after optimizing. Top plot shows DCCB clearing Fault A. Bottom plot shows DCCB clears Fault F.

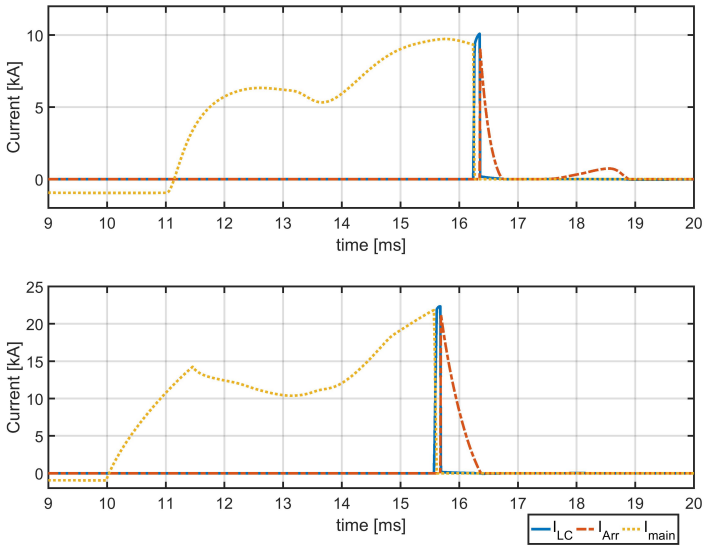

Figure 6.10: The performance of DCCB2 after optimizing. Top plot shows DCCB clearing Fault A. Bottom plot shows DCCB clears Fault F.

in Section 6.5.2. In these two figures, only Fault A and Fault F are simulated here, as Fault A is the most and least severe fault scenario for DCCB1 and DCCB2 respectively, and the opposite holds true Fault F. It is also noticeable that the considered faults can be cleared within 10ms.

INTERRUPTING LOAD CURRENTS

Figure 6.11 depicts the successful load current (0.95kA) interruption by DCCB1 and DCCB2: they both received the signal at 10ms and interrupted the currents at around 15ms and 15.03ms respectively. It is clear that the load current flowing though DCCB2 is opposite to its reference direction, which causes the interruption to be delayed. However, the interruption still occurs when I_{LC}=I_{main}=-0.95kA. The current can be neutralized in 0.03ms due to its low value and the high natural frequency of the LC circuit.

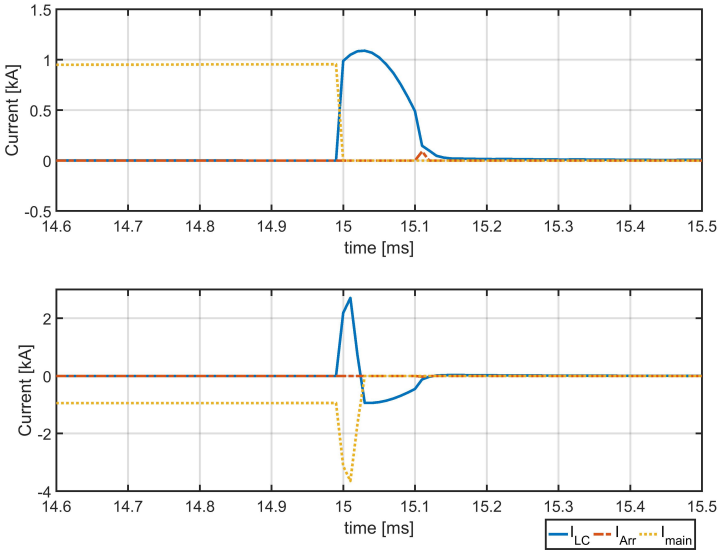

Figure 6.11: The performance of circuit breaker interrupting load currents. Top plot shows DCCB1 clearing load current. Bottom plot shows DCCB2 clearing load current.

The simulation also demonstrates the DCCBs' functionality in terms of interrupting the load current after optimized calibration. In practice, the LC circuit is pre-charged by the system voltage [21], and this charging procedure can cause transient phenomena that impact the operation of an MTDC network. Therefore, a transmission line or cable can be disconnected by first opening either DCCB linked on the line and then opening the other one after the current has decreased to zero. Through this way, only one LC circuit needs to be recharged after re-closing the line.

6.6.4. DISCUSSION

Besides the scenarios shown in Table 6.2, other fault situations with different fault distances are simulated as well. Figure 6.12 displays and records the *di/dt* of the two studied

DCCBs at the current zero instant under each situation, and the fault distance is also calculated from Bm-B2 to the fault location. Upon analyzing the results, it can be observed that they are well below the set critical value 650A/μs, which can ensure the operation of the vacuum switch and thus successful fault isolation. The simulation shows the effectiveness of the optimized DCCBs: after optimization, the *di/dt* value at the current zero instant can be limited to an acceptable level.

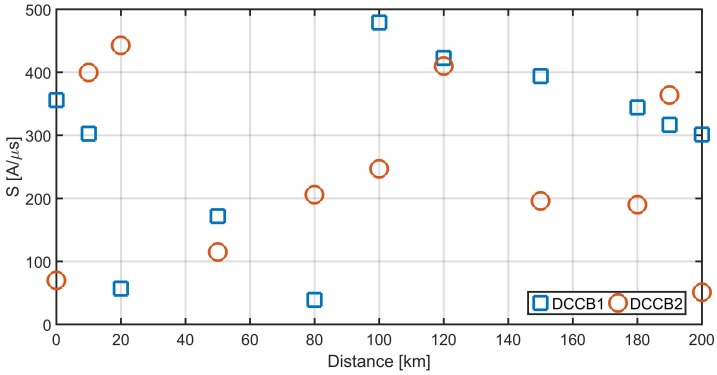

Figure 6.12: *di/dt* at the interrupting instant under different located faults.

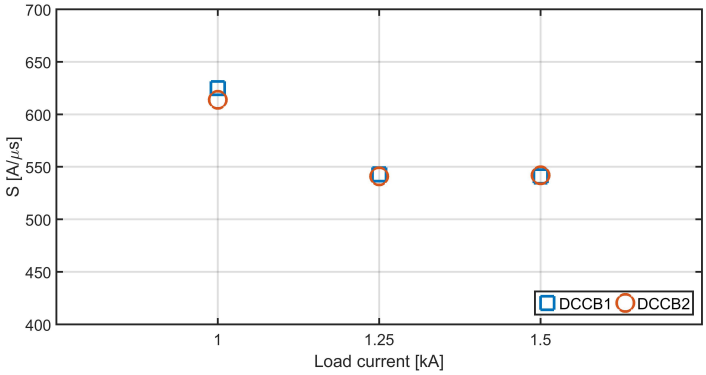

Figure 6.13: *di/dt* at the interrupting instant under different load currents.

In addition, the slopes are also calculated and recorded in Figure 6.13 when the load currents are interrupted, whereby it is evident that *di/dt* is close to the critical value (650A/μs). In practice, when designing and testing an LC circuit, it is better to consider a safe margin for the slope based on the critical *di/dt* of a vacuum switch and to choose a suitable inductor in Eq. 6.4. Otherwise, the vacuum switch will always work at its maximal limit when interrupting a fault current.

6.6.5. LIMITATION

In a real circuit breaker, the vacuum interrupter's maximum quenching capability of *di/dt* depends on the characteristics of the vacuum bottle. Although the maximum value range is described as 150-1000 A/μs in [11], this value is influenced by many factors such as the interruption current and the gap distance. In this chapter, the maximum quenching capability of *di/dt* for a vacuum interrupter under a different fault current magnitude is neglected, and a fixed 650 A/μs is considered. In practice, the higher the interruption current is, the denser the residual plasma will be after current zero. This means that vacuum contact can withstand a lower *di/dt* as a result [22]. In addition, the gap distance and the separating dynamic of the contacts also influence the maximum *di/dt* quenching capability because the vacuum bottle can survive a higher *di/dt* when the gap distance between contacts is larger [22]. If the dynamic of the gap distance during operating contacts were to be provided, the results could be more realistic.

6.7. CONCLUSION

This chapter discusses a significant physical feature that can influence the functionality of a vacuum switch: the *di/dt* of the injected current from the LC circuit at the interrupting instant. As the vacuum switch can extinguish an arc only when the *di/dt* is lower than a critical value, the *di/dt* must be considered when designing and calibrating a DCCB. As such, an algorithm is proposed to optimize a DCCB with the given critical *di/dt*.

Due to the internal correlation between the inductance, capacitance, and interrupting instant, the optimal parameters should be obtained iteratively. Besides the algorithm, the configuration of the DCCB has also been modified accordingly so that the current can be interrupted in both fault and nominal conditions. The simulation performed in the PSCAD environment shows that the algorithm can guarantee that the *di/dt* is within a safe limit during the interruption. On the other hand, the results of the *di/dt* when interrupting load currents indicate that it is advisable to choose a safe margin for the *di/dt* when an LC circuit is being designed. The same design concept is implemented in the next chapter for the protection scheme.

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7

DETERMINING AND TESTING THE PROTECTION SCHEME

In this chapter, the findings of previous chapters are gathered, and the protection scheme is determined accordingly. As discussed in Chapter 2, solid grounding is chosen as the reference grounding method for the sake of calibrating the protection scheme. Meanwhile, other grounding methods are additionally considered to test the calibrated scheme. The MMC-based HVDC system established in Chapter 3 is also adopted as a testing platform.

7.1. PROTECTION SCHEME SET-UP

A complete protection scheme is supposed to contain primary protection and backup protection. In this thesis, the primary protection consists of DC line protection and DC bus protection. More specifically, the DC lines are protected by the MAD-based protection method. Furthermore, as discussed in Chapter 5, in case of high fault impedance, the DWT-based protection is also implemented in the DC line protection. Although it works as "backup" for the MAD-based protection, the DWT-based protection is referred to as ancillary for the MAD-based protection.

On the other hand, in order to guarantee the security of the network, having backup protection is crucial since it serves as the solution when the DC line protection or DC bus protection fail. Hence, it helps to minimize the affected areas of faults when the primary protection fails. For the sake of simplicity and since different protections would command different DCCBs, the DCCB linking the DC bus and the DC line is called a "line DCCB", and the one linking the DC bus and the converter is referred to as a "bus DCCB".

7.1.1. PRIMARY PROTECTION

DC LINE PROTECTION

The structure of the DC line protection is shown in Figure 7.1. Since both the MAD-based and DWT-based methods contribute to the DC line protection, it is understandable that the command (opening signal) for the CBs is generated by inputting the commands from the MAD- and DWT-based protections through an "OR" gate. Due to the faster time response, the MAD-based method is responsible more often for initializing the command, and when there is a high-impedance fault, the DWT-based method's command can be the remedy if MAD-based method fails.

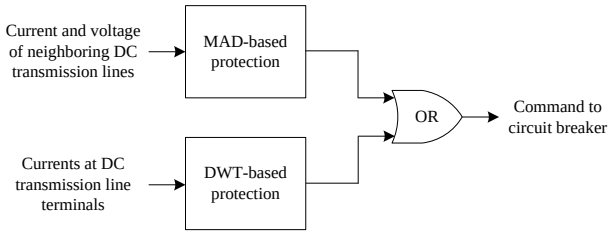

Figure 7.1: The proposed DC line protection scheme.

DC BUS PROTECTION

According to the simulation cases in Chapter 5, the current differential protection is appropriate for the bus protection. More importantly, due to its simplicity and selectivity, it is high feasible in practice. The protection scheme for the bus is shown in Figure 7.2.

It is necessary to clarify that in case of high-resistance faults in HVDC networks, the DWT-based protection actually works as "backup" for the MAD-based protection. This is because the latter functions as the "main" protection since the low-resistance fault is much more hazardous to the HVDC network. However, in the thesis, these two cases are considered to be the primary protection components, since the backup protection, which is discussed in the following section, has other purposes.

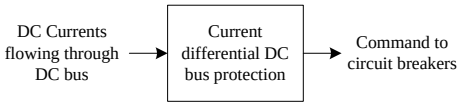

Figure 7.2: The proposed DC bus protection scheme.

7.1.2. BACKUP PROTECTION

Due to the matters related to the aging and manufacturing of the products, failures are inevitable and unpredictable; it implies that having backup protection is necessary in order to prevent an HVDC system from being jeopardized by protection failures. In this section, it is assumed that two types of failures might occur in a protection system [1]:

1. Signal failure
   A signal failure occurs when a breaker cannot receive the trip signal because of the loss or malfunction of signal channel, even though the protection unit has made the right decision and sent the signal to open this breaker. In order to ensure that fast fault clearing takes place, after the primary protection sends the signal, the backup protection is set to send an auxiliary signal 0.1ms later to the breaker through another channel, so as to avoid major disturbances in the HVDC grid [2]. This characteristic must be provided by the mutual monitoring amongst the primary protection, backup protection, and circuit breakers.
2. Device failure
   This failure is defined as the mechanical failure of breakers. Given that the outage of an entire DC network is undesirable, the backup protection has to isolate the fault by tripping the DCCBs closest to the breaker on which the device failure occurs. Hence, it is possible to minimize the adverse impact that any potential mechanical failure might have. The criterion for disconnecting these DCCBs is determined as follows: when the primary protection or auxiliary protection sends the command, but the circuit breaker continues to closing for 6ms, which is the applied DCCB's maximal latency, the backup protection must initiate tripping signals.

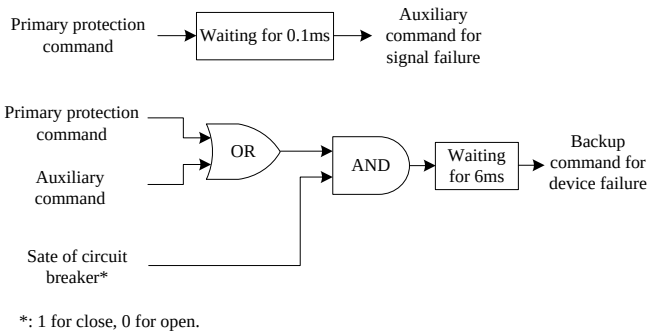

Figure 7.3: The proposed backup protection scheme.

The scheme of backup protection is shown in Figure 7.3. The "OR" gate ensures

that the backup protection can work when the circuit breaker experiences both signal and device failures. Corresponding to the random time delay of the DCCB between 5ms and 6ms assumed in Chapter 6, the 6ms waiting time is necessary, and the "waiting" component will be reset when the circuit breaker is closed. Otherwise, there is no distinction between the primary protection and the backup protection.

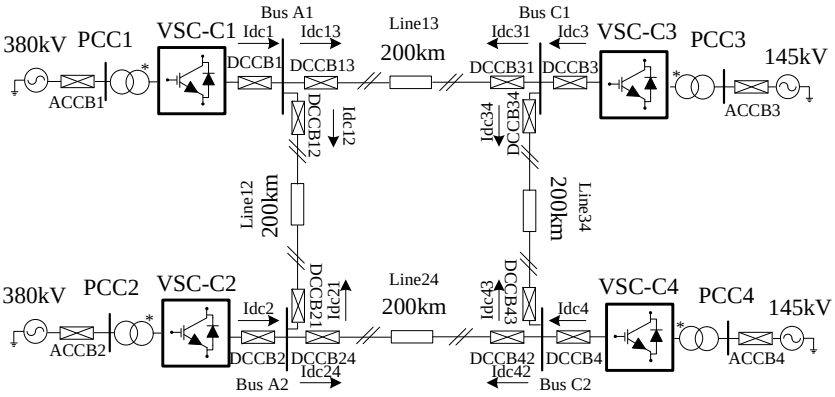

Figure 7.4: The installation of circuit breakers in the studied system

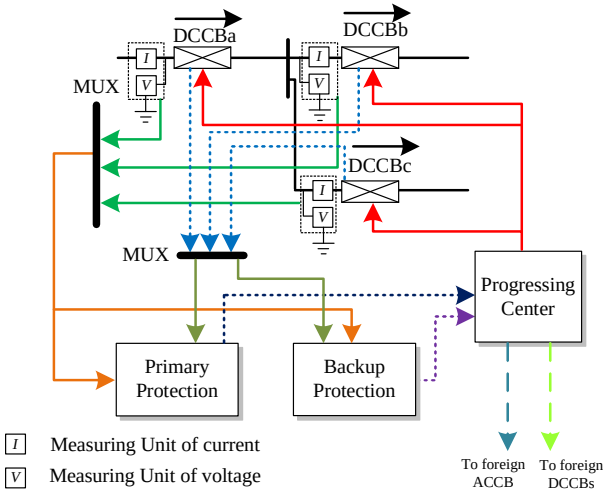

Figure 7.5: The implementation of the protection scheme in one bus.

In Figure 7.4, for example, if a relay send command to DCCB13 after a fault is successfully detected but DCCB13 fails to open, the backup protection should work according to the fault type. If the fault occurs on Bus A1, then the nearest line DCCB on the other end of Line13 must be opened, such as DCCB31. On the other hand, if the fault occurs

on Line13, then all the other DCCBs linked to Bus A1 will be tripped, such as DCCB1 and DCCB12. Another possibility is that DCCB1 cannot be opened, in which case the converter must then be isolated from the AC network by opening the AC circuit breaker. It is understandable that when the backup protection is activated to prevent device failure, the protection's selectivity has been sacrificed, since a part of the healthy section is isolated together with the faulty section.

According to the configuration of the modeled MTDC system, the circuit breakers are installed near buses as shown in Figure 7.4. Therefore, the full protection scheme is arranged in one bus as depicted in Figure 7.5, where "DCCBa" represents the bus DCCB while "DCCBb" and "DCCBc" represent line DCCBs. The black arrows are the currents' reference directions for the circuit breakers.

In Figure 7.5, each protection shares the measured currents or voltages and possesses its own calculation unit. Additionally, the states of all DC circuit breakers are monitored and shared by two protections, as the dashed blue arrows indicate. The "Protection logic" is a logic control loop that initializes signals for certain circuit breakers, which includes the external DCCBs and ACCB that are linked to different buses. Since these external circuit breakers could be remotely located, the time delay concerning communication must be accounted. Similar to the assumption made in Chapter 5, optic fiber is used as the signal channel, and the time delay would be 1ms for a transmitting distance of 200km (the speed of light is 200km/ms in an optic fiber [3]).

7.1.3. CALIBRATING THE PROTECTION THRESHOLDS AND CIRCUIT BREAKERS SETTINGS

DETERMINING THE PROTECTION THRESHOLDS

As explained in Chapter 1, the solid grounding is chosen as a reference for the protection scheme calibration. In Chapter 5, the thresholds have been decided based on the system without grounding and DC capacitors. According to the analysis of solid grounding in Chapter 2, the highest peak current would be generated when a fault occurs. Therefore, the thresholds for DC line protection identified in Chapter 5 are considered to be appropriate for the solid grounding as well and are thus kept for this type. At the same time, since the KCL can be always provided at each bus, it is not necessary to modify the current differential protection for the DC bus.

The settings of the three protection methods are summarized as follows:

1. MAD-based protection
   Criterion 1:

$$Index_I = \begin{cases} 1, S_{iMAD-1}(t) \geq 2S_{iMAD-1}(t-1) \wedge S_{iMAD-1}(t) \geq 200 \\ 0, else \end{cases} \tag{7.1}$$

   Criterion 2:

$$Index_V = \begin{cases} 1, S_{iMAD-2}(t) \leq S_{iMAD-2}(t-1) \wedge S_{iMAD-2}(t) \leq -0.2 \\ 0, else \end{cases} \tag{7.2}$$

2. DWT-based protection

Fault detection:

$$\begin{cases} sign\left(W_{ab}^{+}\right) = -1 \wedge sign\left(W_{ab}^{-}\right) = 1 \\ sign\left(W_{ba}^{+}\right) = -1 \wedge sign\left(W_{ba}^{-}\right) = 1 \end{cases} \tag{7.3}$$

Positive pole to ground fault:

$$\begin{cases} \left|W_{ab}^{+}\right| > 6\left|W_{ab}^{-}\right| \\ \left|W_{ba}^{+}\right| > 6\left|W_{ba}^{-}\right| \end{cases} \tag{7.4}$$

Negative pole to ground fault:

$$\begin{cases} \left|W_{ab}^{-}\right| > 6\left|W_{ab}^{+}\right| \\ \left|W_{ba}^{-}\right| > 6\left|W_{ba}^{+}\right| \end{cases} \tag{7.5}$$

Pole-to-pole fault:

$$\begin{cases} \left|W_{ab}^{+}\right| - \left|W_{ab}^{-}\right| \in \left(-10^{-5}, 10^{-5}\right) \\ \left|W_{ba}^{+}\right| - \left|W_{ba}^{-}\right| \in \left(-10^{-5}, 10^{-5}\right) \end{cases} \tag{7.6}$$

3. Current differential DC bus protection

$$\begin{aligned} I_{diffx} &= Idcx - \sum Idcxy (x, y = 1,2,3,4, x \neq y) \\ Index_{diff} &= \begin{cases} 1, I_{diff} = 1kA \\ 0, I_{diff} = 0 \end{cases} \end{aligned} \tag{7.7}$$

where the x and y stand for the numbers that denote the currents in Figure 7.5

DC CIRCUIT BREAKER DESIGNING

Based on the same methodology identified in Chapter 6 [4], the parameters for DCCBs connecting to the same bus are calculated and listed in Table 7.1. The design also considers backup protection. Aside from its own protection zone, either one of the DCCBs is responsible for its neighboring protection zone. For example, in Figure 7.5, when DCCBb is obliged to open but fails to do so, DCCBa and DCCBc must be opened. The design of the auxiliary LC circuit is not considered, as the demonstrations only show the interruption of the fault current.

Parameter	DCCB
Capacitor	1.06μF
Inductor	0.35mH
Frequency	8.27kHz
U_C	200kV
I_{max}	11kA
di/dt_{max}	571A/μs

Table 7.1: Parameters of the DCCBs used in the modeled MTDC system [4]

According to the discussion in Chapter 3, while the DC capacitor can discharge during the fault, it mainly contributes to the first peak of the fault current. Since the clearing time of the DCCB is taken into account in this thesis, its performance when interrupting the fault current is not influenced by the DC capacitor.

7.2. TESTING SCENARIOS

The protection scheme is to be tested using different scenarios. More importantly, the protection scheme are to be tested with and without the aforementioned failures, thus enabling the verification of both primary and backup protections. The considered fault scenarios are listed in Table 7.2.

Fault scenarios	Description
FSA	PtP fault applied at 10ms at the end of Line13. R_f=20Ω.
FSB	Negative PtG fault applied at 10ms at the end of Line13. R_f=20Ω.
FSC	PtP bus fault applied at 10ms on Bus A1. R_f=20Ω.
FSD	PtP fault applied at 10ms at the end of Line13. R_f=100Ω.
FSE	FSA with a signal failure on DCCB13.
FSF	FSA with a device failure on DCCB13.

Table 7.2: The considered fault scenarios. PtP refers to pole-to-pole, and PtG stands for pole-to-ground.

The scenarios **FSA** to **FSD** aim to test a normally operating protection scheme. In order to specifically examine the cooperation of the DWT-based and MAD-based protections, the fault resistance in **FSD** is set to 100Ω. The **FSE** and **FSF** are also set to evaluate the backup protection.

7.3. PERFORMANCE OF THE PROTECTION SCHEME

7.3.1. PRIMARY PROTECTION

SCENARIO: FSA

The simulation results of scenario **FSA** are summarized in this section. The command to the DCCBs can be generated using both MAD- and DWT-based protection methods. However, as discussed in Chapter 5, when the DWT-based protection is functioning, the communication can cause a delay of approximately 2ms during the process of protection in the Bus C1 protection scheme. This time difference can be observed in Figure 7.6, where the top and bottom plots are the commands generated by the primary protection in Bus A1 and Bus C1 respectively.

As there is an "OR" gate in the primary protection (such as that shown in Figure 7.1), DCCB13 and DCCB31 are activated when the commands from the MAD-based protection are delivered. When using MAD-based protection, the impact of a fault is smaller than that occurring with the DWT-based protection. The performances of DCCB13 and DCCB31 are demonstrated in Figure 7.7. In this figure, it is evident that the surges of fault currents arrive at DCCB13 and DCCB31 respectively at around 11ms and 10ms, which are depicted by the yellow dotted lines. Due to the fast response of the DC line protection shown in Figure 7.6, the LC circuits of these two DCCBs began to interrupt the fault currents at around 16.4ms and 15.4ms respectively as demonstrated by the blue solid lines. After the energy is successfully commutated to the surge arrester, such as the red dash dotted lines, the fault current is completely cleared at 16.7ms by DCCB13 while at 15.75ms by DCCB31.

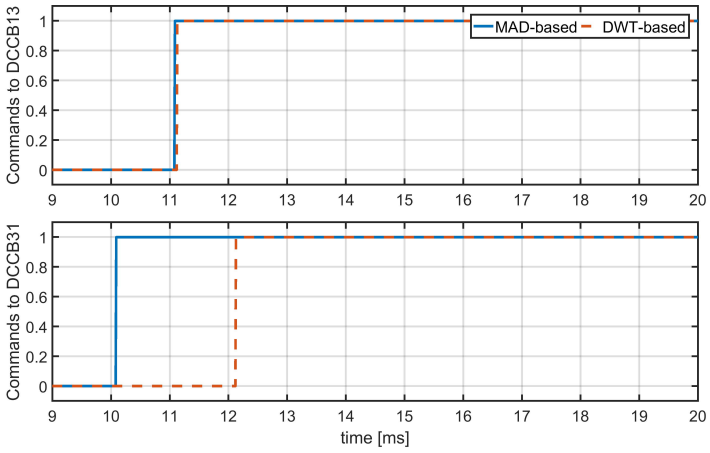

Figure 7.6: The responses of the primary protection in Bus A1 (top) and Bus C1 (bottom). Scenario **FSA**.

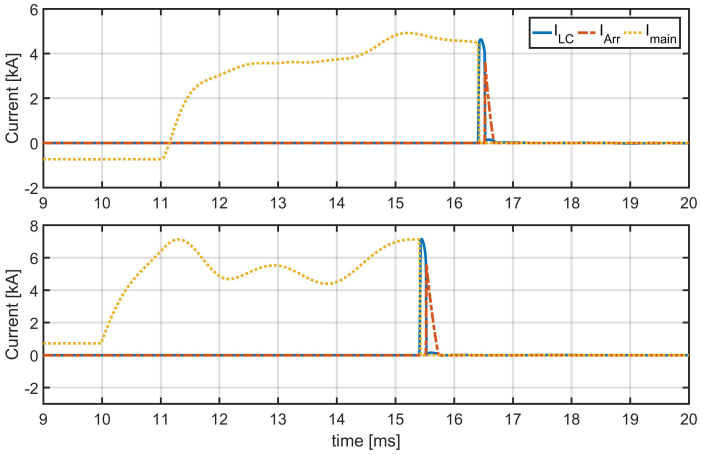

Figure 7.7: The performances of DCCB13 (top) and DCCB31 (bottom) with corresponding zoom-in at the instant of current interruption. Scenario **FSA**.

SCENARIO: FSB

Similarly, the performances of the protection scheme and circuit breakers in scenario **FSB** are demonstrated in Figure 7.8. Similarly to scenario **FSA**, the 2ms time delay is inevitable in scenario **FSB**. The hyphen sign used in the Y-axis of Figure 7.8 stands for the DCCBs on the negative pole. The current waveforms in two DCCBs are depicted in Figure 7.9, and same as the fault clearance procedure that is explained in the case **FSA**, the fault is cleared at 16.6ms by DCCB13- and at 15.65ms by DCCB31-.

It is observable that the fault currents in Figure 7.9 are different from those in Figure 7.7. The reason is the different circuits for the traveling waves under pole-to-pole fault and pole-to-ground fault; because of the asymmetrical circuit under the pole-to-ground

fault, the contribution of AC system is less severe when compared to that under the pole-to-pole fault.

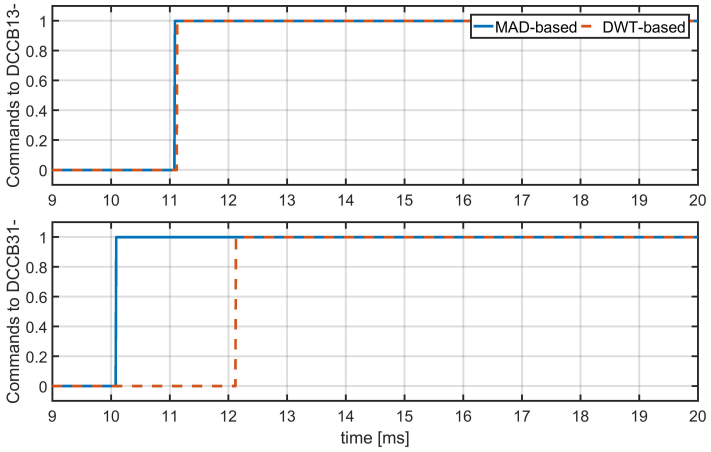

Figure 7.8: Responses of primary protection in Bus A1 (top) and Bus C1 (bottom). Scenario **FSB**.

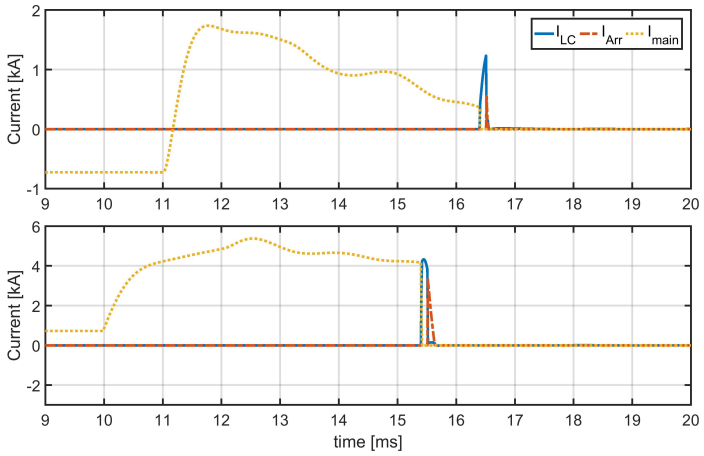

Figure 7.9: DCCB performances of DCCB13- (top) and DCCB31- (bottom) with corresponding zoom-in at the instant of current interruption. Scenario **FSB**.

SCENARIO: FSC

This scenario shows the performance of the bus protection. According to Figure 7.10, the command can be generated immediately by the current differential algorithm after the fault happens. This command is sent to all three circuit breakers, as opposed to the DC line protection which would not send any command.

In Figure 7.11, the performances of DCCB1, DCCB12 and DCCB13 are plotted, together with the zoom-in from 15.85ms to 16.1ms. Unlike DCCB1, DCCB 12 and DCCB

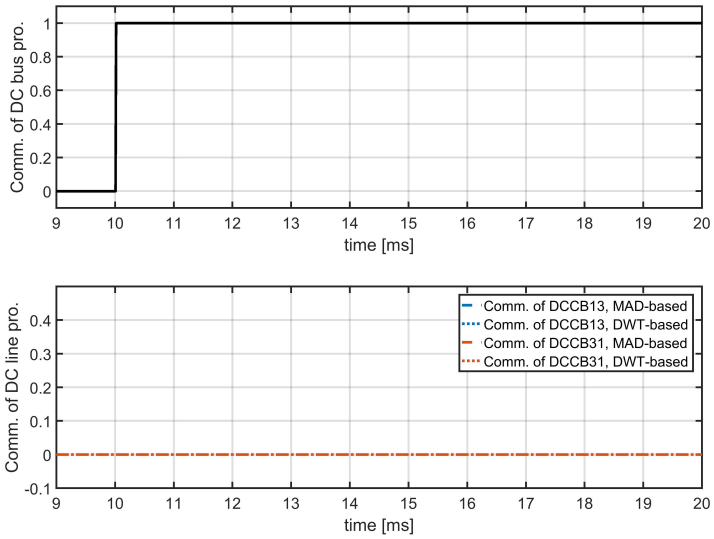

Figure 7.10: The responses of the DC bus protection and DC line protection. Scenario **FSC**.

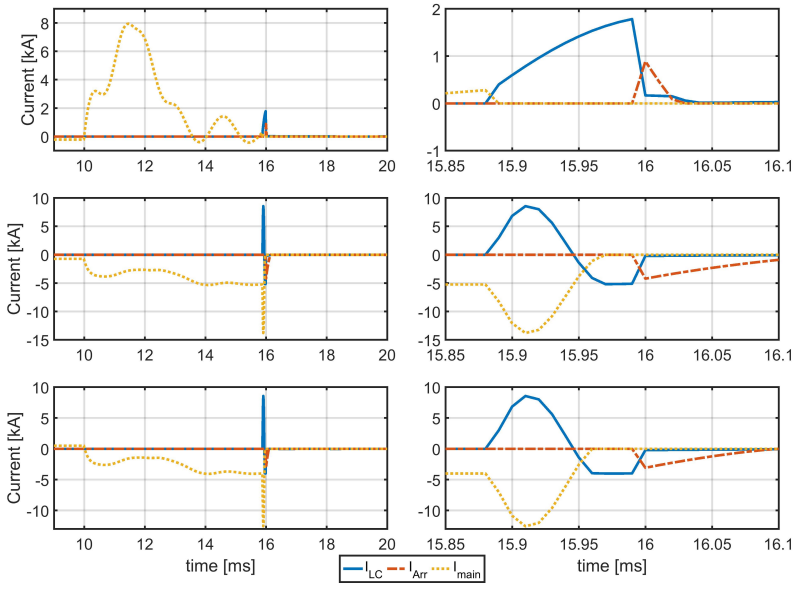

Figure 7.11: The performances of DCCB1 (top row), DCCB13 (middle row) and DCCB12 (bottom row) with corresponding zoom-in at the instant of current interruption. Scenario **FSC**.

13 interrupt the currents which are opposite to the reference direction. On the other

hand, if the zoomed-in area in Figure 7.11 is examined, the fault current is shown to be almost zero when DCCB1 begins to interrupt the current. This is because converter VSC-C1 blocks itself when the DC current flowing through one of its six arms exceeds 3kA, as described in Section 4.2.1, consequently limiting the fault current. This situation is inevitable due to the DC circuit breaker's mechanical latency and the fault's proximity to the VSC-C1.

SCENARIO: FSD

In this scenario, the fault resistance is set to 100Ω in the pole-to-pole fault, and the response of protection scheme is shown in Figure 7.12. Although the MAD-based method can detect the fault in Bus C1 that is directly exposed to the fault, it fails to do so in Bus A1 due to the high fault resistance. Even though the fault current is quite low because of the large fault resistance as shown in Figure 7.13, it still needs to be isolated.

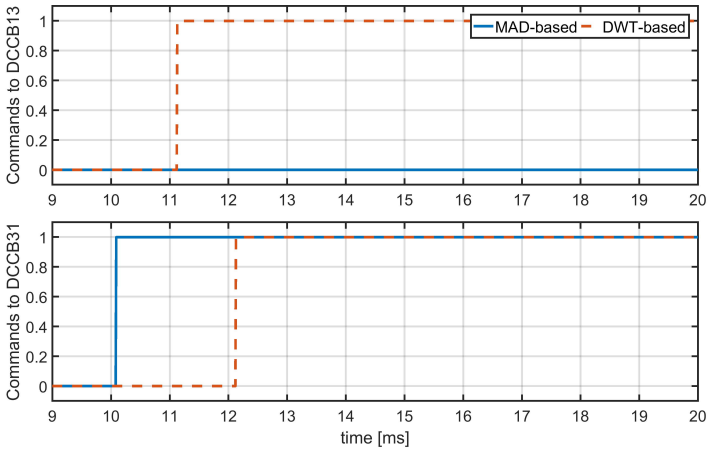

Figure 7.12: The responses of the primary protection in Bus A1 (top) and Bus C1 (bottom). Scenario **FSD**.

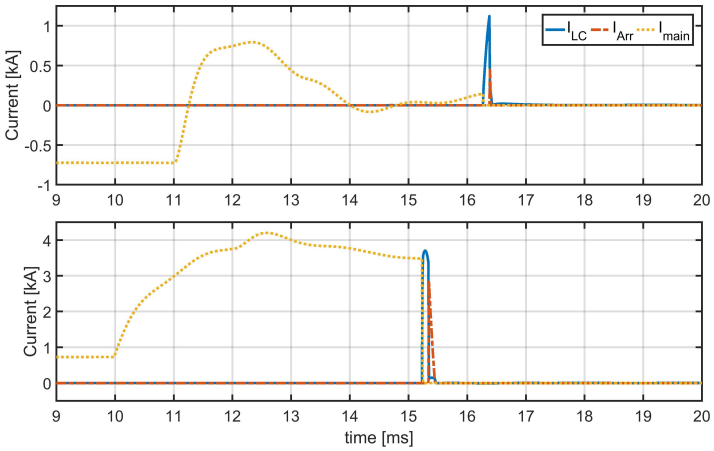

Figure 7.13: The performances of DCCB13 (top) and DCCB31 (bottom) with corresponding zoom-in at the instant of current interruption. Scenario **FSD**.

Based on the analysis in Chapter 5, the DWT-based method can theoretically detect the fault with resistance as high as 300Ω; therefore the protection installed in Bus A1 can recognize the simulated high-resistance fault, consequently the DCCB13 can still

function. The performances of DCCB13 and DCCB31 are illustrated in Figure 7.13, which shows that the LC circuits inject currents at respectively at 16.3ms and 15.25ms, and the fault can be cleared respectively at 16.4ms and 15.45ms.

7.3.2. BACKUP PROTECTION

SCENARIO: FSE AND FSF

In testing scenario **FSE**, the channel of the primary protection command is manually disabled. However, the auxiliary command can still guarantee that circuit breaker DCCB13 can clear the fault in 6ms. Since the protection algorithm works normally in Bus C1, the DCCB31 can clear the fault successfully, and its performance shown in Figure 7.14 is similar to that in Figure 7.7 of **FSA**.

In scenario **FSF**, the channel of primary protection is assumed to be functioning as usual, which is why the auxiliary command is not shown. On the other hand, since DCCB13 is set to experience device failure, DCCB1 and DCCB12, which are linked to the same bus as DCCB13 does, must open.

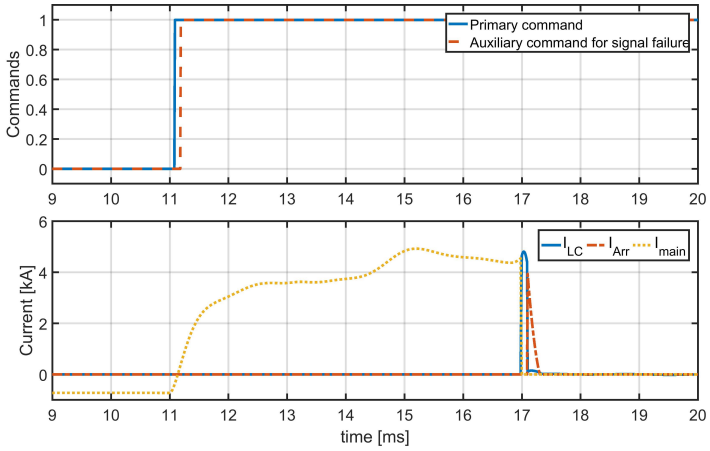

Figure 7.14: Top plot: the response of the backup protection in Bus A1. Bottom plot: the currents in DCCB13. Scenario **FSE**.

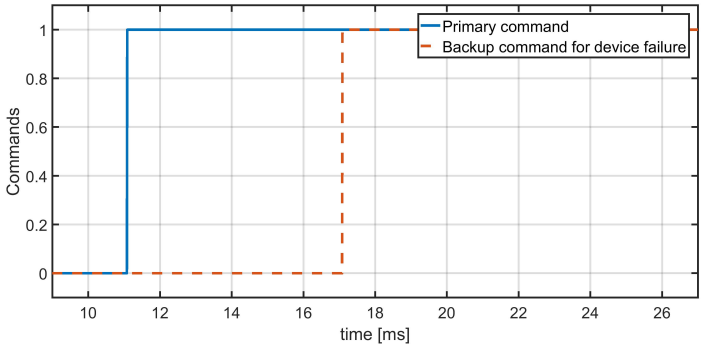

Figure 7.15: The response of the backup protection in Bus A1. Scenario **FSF**.

Due to the fact that in the case of device failure, the backup protection must wait

6ms after the primary protection's command is given (as explained in Section 7.1.2), and the DCCB has its own mechanical delay which has been set up to 6ms in Chapter 6, the total fault clearance time has been increased to around 12ms. In Figure 7.16, the performances of DCCB1 and DCCB12 are shown, where it is clear that the DCCB1 must interrupt the fault current of 4kA, while the DCCB12 interrupts the fault current that is opposite to the reference direction. Unlike that in scenario **FSC**, since DCCB1 is opened before converter VSC-C1 blocks itself, the fault current cleared by DCCB1 in higher than that in scenario **FSC**.

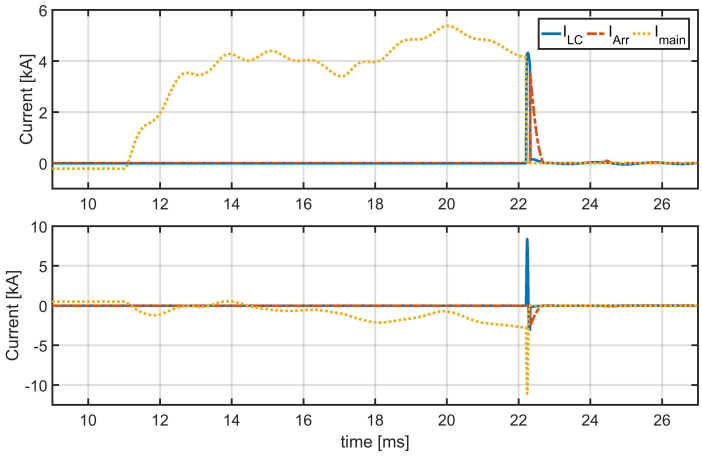

Figure 7.16: The performances of DCCB1 (Top) and DCCB12 (bottom). Scenario **FSF**.

7.4. PROTECTION SCHEME WORKING UNDER DIFFERENT GROUNDING METHODS

In order to verify the generality of the protection scheme, especially the primary protection, it is tested by using other grounding methods, which are grounding through an inductor, a resistor, and a capacitor respectively. According to the discussion in Chapter 2, these types have more effect on the pole-to-ground fault due to the path through the soil. Hence, scenario **FSB** is used in all the tests. From Figure 7.17 to Figure 7.19, the responses of the protection scheme are plotted. As the thresholds in the protection scheme are determined based on the floating method and have already been tested using sensitivity analysis in Chapter 5, this type is not considered in this section.

According to Figures 7.17 and 7.18, it is evident that the primary protection functions smoothly when the system is grounded through a capacitor and resistor, since both the MAD-based and DWT-based protection methods can function well, similarly to the responses described in Section 7.3.1. However, when the system is grounded through an inductor, the MAD-based method cannot detect the fault in Bus A1. Fortunately, the DWT-based method can remedy this issue, as shown in Figure 7.19.

The failure of the MAD-based method lies in the fact that the thresholds in Eq. 7.1 cannot identify the fault current in the case of grounding through an inductor. Nevertheless, it does not change this method's sensitivity. If the outputs of MAD-1 are examined for three considered grounding methods, it is clear that all of them can respond quickly and noticeably. Their responses are depicted in Figure 7.20, where the first output of MAD-1 in three grounding methods are zoomed out in the top plot.

From the simulation discussed in Chapter 2, it is known that in the cases of all the considered grounding elements (i.e., resistor, capacitor, inductor), the fault currents increase, albeit with different gradients. As the results of MAD rely on the discrete data series, the gradient determines the first sample recorded by MAD, which consequently

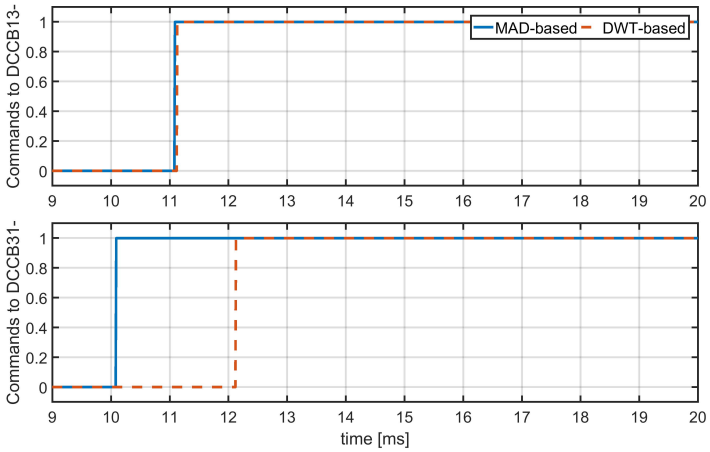

Figure 7.17: Responses of the primary protection in Bus A1 (top) and Bus C1 (bottom). Case: grounding through a capacitor

causes the MAD-based protection to be affected by the sampling frequency. After decreasing the sampling frequency from 10kHz to 6.67kHz, the results of MAD-1 change drastically, as shown in the bottom plot of Figure 7.20. Thereafter, the defined thresholds can work in all three considered cases.

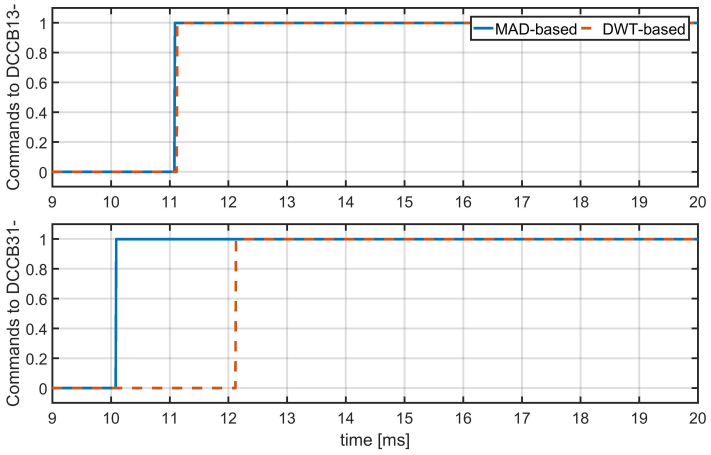

Figure 7.18: Responses of the primary protection in Bus A1 (top) and Bus C1 (bottom). Case: grounding through a resistor.

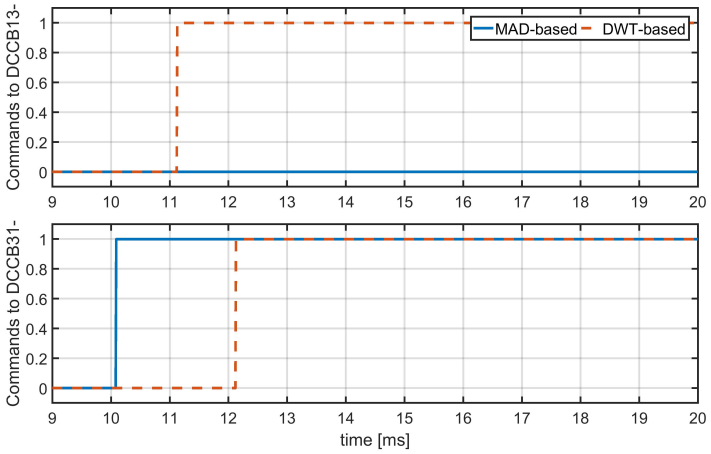

Figure 7.19: Responses of the primary protection in Bus A1 (top) and Bus C1 (bottom). Case: grounding through an inductor.

It reveals that when a lower sampling frequency is applied, a sample with a higher value is recorded from the fault current signal to calculate the first MAD output. On the other hand, because sampling frequency is reduced, the calculation of MAD-1 is subsequently delayed by around 50μs. Figure 7.21 shows the performances of DCCB13 in-

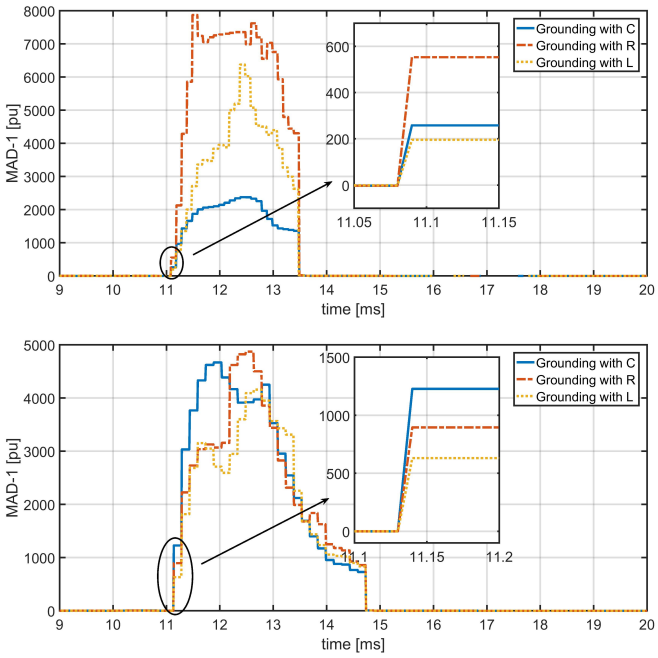

Figure 7.20: Outputs of MAD-1 in three grounding methods. Top plot: sampling frequency=10kHz. Bottom plot: sampling frequency=6.67kHz.

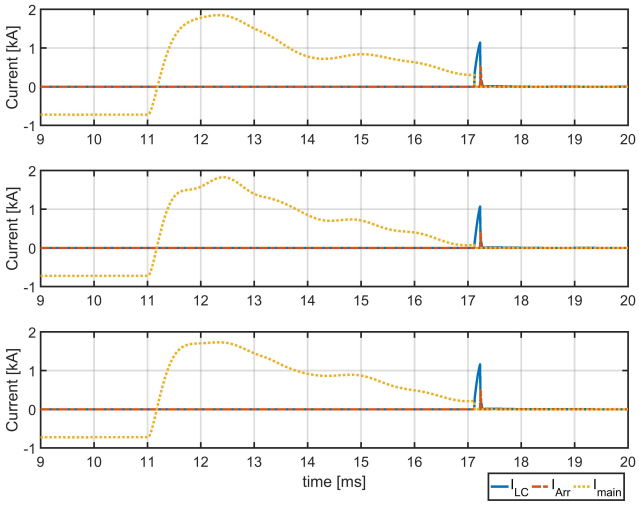

Figure 7.21: Performances of DCCB13 in the cases of: grounding through a capacitor (top plot), through a resistor (middle plot), and through an inductor(bottom plot).

stalled at Bus A1 in the three discussed cases.

7.5. REAL-TIME PERFORMANCE OF MAD-BASED PROTECTION

So far, the proposed protection scheme has been implemented and demonstrated in PSCAD, which is an off-line application. Due to the features of this type of application, the proposed protection algorithms are performed simultaneously with the network solution in each time step. This means that the latency of protection is covered by the simulation time cost in each time step. Therefore, the more realistic latency introduced by the protection cannot be revealed in an off-line simulation, seeing as the protection system works in tandem with the power system in reality.

Aside from the time consuming practice involved with performing the key algorithm, the latency also includes the time required for data sampling and information transmitting. These three time-related features depend on the specific protection unit, the adopted standard, and the condition of the information network. In order to demonstrate the performance capabilities of the proposed protective algorithm, the cyber-physical simulation platform is utilized, as a co-simulation between the electrical power system model and information and communication technology (ICT) infrastructure based on the standard IEC61850 in real-time.

This section explains a shown case of MAD-based protection which has been chosen because its algorithm is feasible to the program in RSCAD environment using standard C. On the other hand, the DWT-based protection must be supported by a physical relay unit or a virtual one (e.g., a PC that can run MATLAB), which was not feasible by the time of this study.

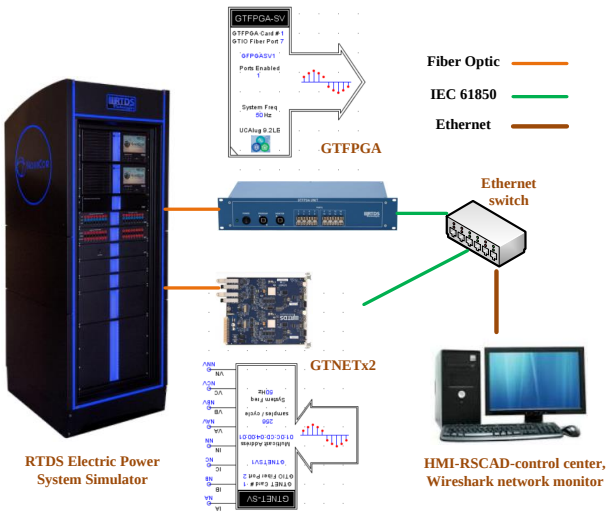

Figure 7.22: A real-time simulation platform and IEC61850 based ICT infrastructure.

7.5.1. REAL TIME SIMULATION PLATFORM

The real-time cyber-physical simulation platform is illustrated in Figure 7.22. The test MTDC system and protection logic was firstly coded in C language and then simulated in real time using RTDS [5]. Four RTDS racks, including 16 PB5 processor cards, are used to provide the AC system in the environment of large time step 75μs and Type-5 models of HB-MMC converters [6] in addition to the realistic mechanical DCCBs [7] in the environment of small time step 3.124μs. Furthermore, using the the hardware (i.e. GTFPGA and GTNETx2 in Figure 7.22), the sample value (SV) messaging is conducted and can be interpolated. Although these two units can support both IEC61869-9 and IEC61850-9-2LE standards, the proposed protection method only requires a sampling frequency of 10kHz. Therefore, the IEC61850-9-2LE is considered, as it provides a sampling frequency of 12.8 kHz that is sufficient for the proposed method. The SVs from the critical measuring points in the MTDC system will be sent (published) to the local Ethernet network by GTFPGA. Whilst, the GTNETx2 is configured to subscribe to the SV data stream that feeds the measurements to the protection logic established in RTDS. The corresponding data flows can be observed and analyzed by using the Wireshark network analyzer installed on the PC that is connected to the local Ethernet switch, as shown in Figure 7.23.

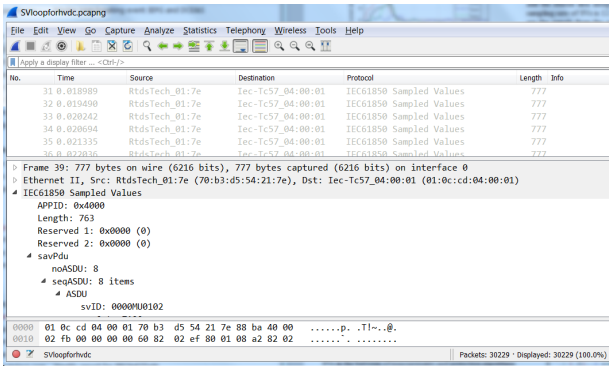

Figure 7.23: Monitoring of SVs in Wireshark.

7.5.2. VERIFICATION OF THE ALGORITHM

The runtime sib-file in RSCAD that provides a center control platform to run the fault cases in real time can be seen in Figure 7.24. The fault **FSA** is considered here as an example to demonstrate the implementation of the proposed protection algorithm on the real-time simulation platform. The DCCB models have been implemented at each end of the DC lines. Four critical relays and breakers are selected as the observed objects (shown as red circles in Figure 7.24) experiencing positive fault currents. If there is no time delay in the communication links, the simulation results can be seen from Figure 7.25 to Figure 7.27. The voltage and current waveforms that are seen by four critical relays and breakers are depicted in Figure 7.25. The fault is applied at 100ms, and the arrival timings of the traveling waves to the four points are different. The subscripts

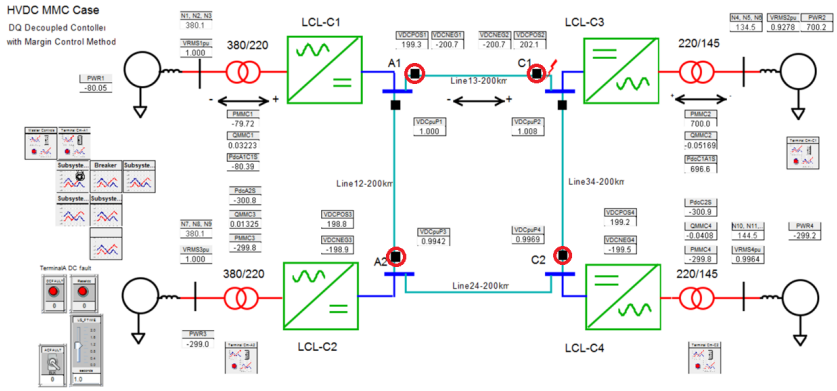

Figure 7.24: The runtime platform for protection scheme testing.

A1C1, C1A1, A2A1, and C2C1 represent the measurement points close to Bus A1, C1, A2, and C2 on related lines.

Based on the related analysis, proposed algorithms, and the criteria in the previous section, the MAD-based indices are shown in Figure 7.26. It is evident that the sensitivity of the current index is higher than that of the voltage index, as all four relays detect the current derivations, whilst only the two relays installed on the faulty line can detect the voltage derivations. Then, the combined $Index_{VI}$ can be generated, which is depicted in the bottom plot of Figure 7.26. Hence, the protection system, in this case, is able to successfully detect and locate fault on Line13, between Bus A1 and Bus C1.

When the corresponding trip signals are generated, the performances of DCCBs (DCCB1 and DCCB2 in Figure 7.24) can be observed from the simulation results of the related currents in Figure 7.27. Due to different distances between the relays and fault **FSA**, the fault

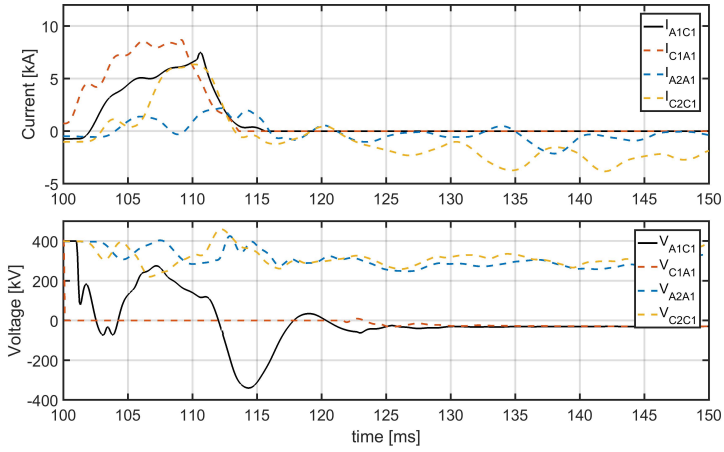

Figure 7.25: Currents and voltages measured by critical relays.

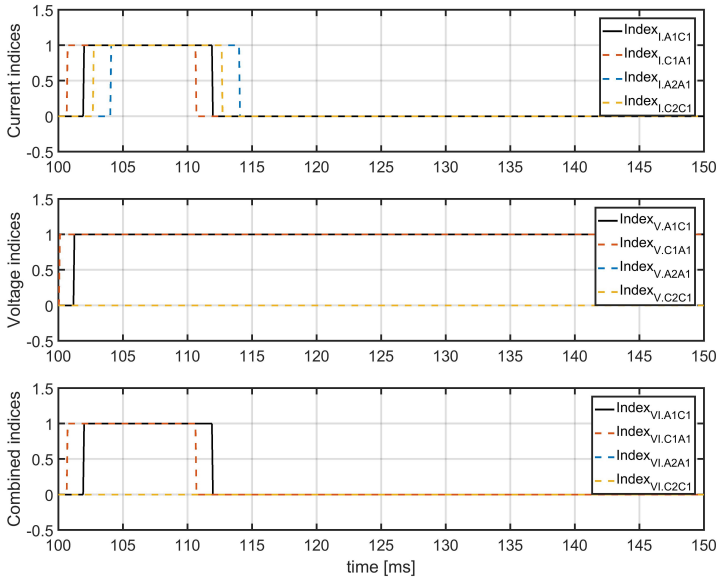

Figure 7.26: The protection indices of the critical relays.

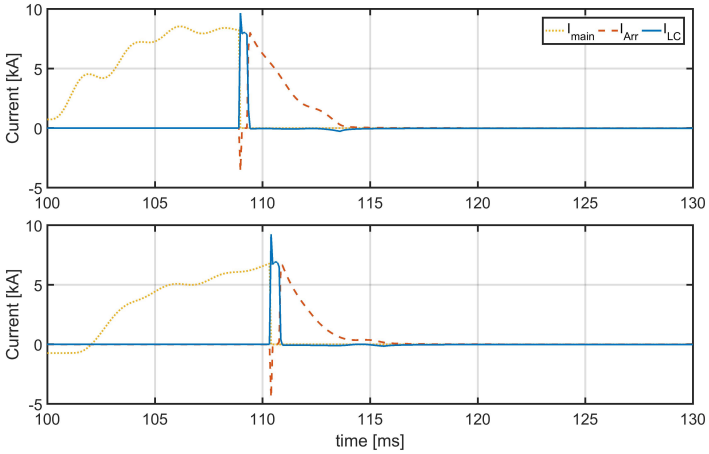

Figure 7.27: The currents of the DCCBs. Top plot: DCCB1. Bottom plot: DCCB2.

is detected and interrupted at different instants. Since the operation delay of all DCCB interrupters is set as 8ms [7], the current interruption time is considered to be different in two DCCBs: the interruption time is around 0.109s in DCCB1 and approximately 0.1103s in the DCCB2.

If there is a time delay in the communication links, then the simulation results can be seen from Figure 7.28 to Figure 7.30. The time delay is produced by the communication links of SVs, which are the communication interfaces and the related data interpolation

algorithm. The default sampling period of the SVs is around 0.078ms (i.e., a sampling frequency of 12.8kHz), and DCCB1 is chosen an example in this particular case.

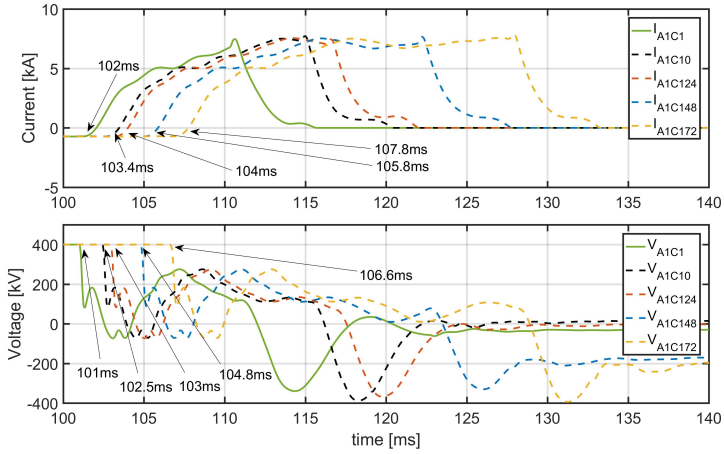

Figure 7.28: The currents and voltages measured at DCCB1.

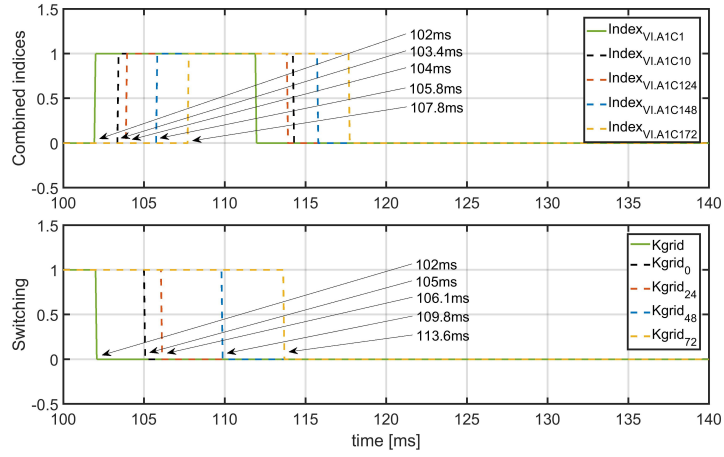

Figure 7.29: The combined indices and tripping signals for DCCB1.

In the figures ranging from Figure 7.28 to 7.30, the solid green traces are the signals from the case **FSA** without any communication delays, and they are marked in the legend with an extra subscript 0. In addition, when the interpolation algorithm is implemented, the corresponding current waveforms upon different settings of interpolation algorithm delays are simulated and marked by legends with subscripts 24, 48 and 72 respectively, which indicate the delay time in terms of sample periods (s.p.). In this case, the required voltages and currents are collected through the SV links, and the grid tripping signal Kgrid (initiated by $Index_{VI}$) is sent through the SV links as well. It is evident in Figure

7.30 and Table 7.3 that when the interpolation algorithm delay setting increases, along with the increase of communication delays, the fault detection requires longer time. The critical timings and delays are shown in these figures and in Table 7.3, in which the mechanical delay of the DCCB (i.e., 8ms) is not considered as part of the communication delay.

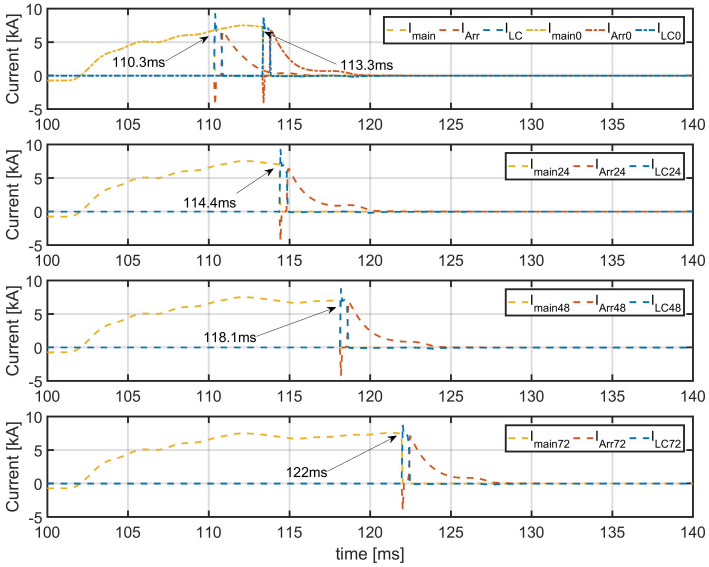

Figure 7.30: The currents of DCCB1 with different delays.

Interpolation delay time	Timings			Comm. delays
	Detection	Tripping	Interruption	
No communication	102ms	102ms	110.3ms	0ms
0 s.p.	103.4ms	105ms	113.3ms	1.6ms
24 s.p.	104ms	106.1ms	114.4ms	2.1ms
48 s.p.	105.8ms	109.8ms	118.1ms	4ms
72 s.p.	107.8ms	113.6ms	122ms	5.8ms

Table 7.3: The critical timings and delays of DCCB1 and the related protection. N/A: not available.

It should be noted that although the time delays according to IEC61850-9-2LE are long, the DCCB can sustain currents during this time delay since the fault current has been limited by the LCL converter [8]. Therefore, the DCCB can be designed with a low interrupting capability, as the fault current would not increase significantly during the time delay. Since the protection should operate within 2ms from the fault occurrence [7], upgraded hardware is required for the communication.

7.6. CONCLUSION

This chapter proposes and demonstrates a protection scheme that combines the DWT-based and SWT-based methods to strengthen the DC line protection. In addition, the current differential protection is in charge of the DC bus protection. Due to the possible signal and device failures, the backup has been considered in this chapter as well.

Taking into account the protection thresholds from Chapter 5, the simulation cases show that the protection scheme can function well to clear the faults when the system uses solid grounding. The analysis discussed in Chapter 5 and the findings of this chapter further reveals that the MAD-based protection has a higher sensitivity, seeing as it can generate a command to trip the DCCB faster than the DWT-based protection by approximately 2ms. However, if the fault resistance is higher than 50Ω, the MAD-based protection becomes less effective. Fortunately, the DWT-based method can ensure the functionality of the whole scheme at this point in time. The simulation also shows the importance of backup protection, as failures are inevitable and unpredictable.

The proposed protection scheme is also tested using different grounding methods, even though there is not a defined grounding method for the VSC-based MTDC network. Based on the thresholds determined through sensitivity analysis in Chapter 5, the protection scheme has a good time response concerning the grounding through a capacitor, a resistor, and an inductor. However, the exception is that the MAD-based method cannot fully work under grounding with an inductor, although it can nonetheless be improved after decreasing its sampling frequency.

The proposed protection method was verified using a cyber-physical simulation platform developed on the RTDS platform. At the same time, an SV-based protocol was adopted to provide the required sampling frequency and communication interfaces. The real-time simulation cases demonstrate that the MAD-based method is highly robust and considers the latency introduced by hardware interfacing, data communication and processing when implementing SV protocols. Even though the implemented SV messaging link may not be suitable for DC protection applications, the proposed method can be realized effectively with future technologies, due to its low requirements. Since the protection method needs local signal processing at a DC bus station, more improvements and implementation of information communication technologies are necessary. Then, the proposed protection method will be a valuable addition to the concept of the digital substation.

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8

CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

This chapter summarizes the conclusions of the thesis and reiterates the answers to the research questions as well. In addition, a few suggestions for future research are also discussed.

8.1. ANSWERS TO THE RESEARCH QUESTIONS

THE main research question of this thesis is ***"How to protect an MTDC system in a reliable manner?"*** In order to answer it, the five sub-questions have been comprehensively discussed and addressed.

1. What is an appropriate AC/DC converter configuration needed to establish an MTDC network?

   Chapter 3 introduces a new configuration of the HB-MMC, which is the LCL MMC. The added LCL circuit on the AC side makes the VSC more capable of withstanding DC faults. The simulation results show that the MMC's stress caused by a fault current can be halved after implementing the LCL circuit, whereby the impact of the DC fault on an AC system is ignorable. In addition, a controlling method of transformer' tap for optimizing the LCL circuit's capacitor banks is proposed in order to decrease the LCL-based HB-MMC's power losses, especially during partial-load operations. Since implementing an LCL circuit does not require the reconfiguration of the converter bridge, it has been concluded that this tap controlling method is compatible with different VSC techniques. Therefore, the LCL MMC should become more widespread in the future MTDC grids. This is largely due to their affordability, resilience, continuous power-transferring efficiency, and their high DC fault tolerability.

2. How to detect DC faults in a fast and accurate way?

   It has been found that the signal processing algorithms DWT and MAD function more efficiently than the FFT and STFT when processing the fault-caused signals. More specifically, the ability of the DWT to accurately detect faults is provided by sampling the signal with a high frequency, which is 100kHz in this thesis, since its lack of translation-invariance under low sampling frequency may result in maloperation. By contrast, the MAD method reliably detects faults using only a limited number of samples. In fact, the analysis has shown that the latest 50 samples are enough, and a high sampling frequency is not necessary when using MAD. The thesis also shows that sampling with 10kHz provides an adequate and fast time response.

   By applying the DWT, the time-vary signals can be processed using a multiscale analysis, whereby the signal is decomposed into different ranges of frequencies. Through the use of the MAD algorithm, which is explicit and straightforward, the abrupt data change within a discrete signal series can be easily found. The simulations in Section 4.2.3 and 4.2.4 show that the WT and MAD can detect the fault-caused transient signal more quickly and accurately.

3. How to ensure the protection's selectivity?

   In order to ensure the selective protection of the DC line, Chapter 5 introduces DWT-based and MAD-based methods. As a type of unit protection, the selectivity of DWT-based method is provided by making use of the communication between the relays located at the two ends of each DC line, which is applicable for MTDC lines.

Unlike the DWT-based method, the MAD-based method does not require remote communication, and its selectivity is provided by the fault current and voltage characteristics of the neighboring faulty and healthy lines that are linked to the same bus. By carefully selecting threshold values, this method enables the identification of the internal and external faults for a defined protection zone.

The proposed protection scheme combines the MAD and DWT-based protection methods. Due to the reason that the low-resistance faults are more severe to HVDC systems, and MAD-based protection is more efficient to detect them, the protection scheme adopts it as the main protection. Since DWT-based protection is more sensitive to high-resistance faults, it can detect them smoothly if MAD fails to do so. Even though the communication delay in the DWT-based method is not preferred, its impact on fault clearance is irrelevant, as the high-resistance fault always causes less severe situation than the low-resistance fault does.

In order to protect the DC bus from faults, a current differential protection algorithm has been applied. This method depends on the fact that the KCL is valid without consideration of time delay for the bus as current measuring points on a bus are close to each other. The simulation cases provided in Section 5.4 show that it is an appropriate method to protect the DC bus because it proves good selectivity and sensitivity to DC bus faults.

4. How to embed the DCCB into the protection scheme?

   In order to ensure successful fault clearance, Chapter 6 discusses the design of the DCCB with an active current injection circuit. The results of the analysis show that a more practical design of DCCB must consider two factors: the first is the limits of DCCB's elements, and the second is the rate of DCCB. The critical *di/dt* of the vacuum switch, the chopping current of each switch, and the mechanical delays determine the DCCB's features and prospective working conditions. A detailed optimizing procedure regarding the DCCB's LC discharging circuit is proposed. Generally, the DCCB's operating delay defines its own current range of interruption, which influences the design of LC discharging circuit in return together with the element limits of the DCCB.

   Since the protection scheme is composed of different protection methods, their time responses must be accounted in order to successfully calibrate the DCCBs. The set-up in Chapter 7 shows that when the primary protection implements MAD-based and DWT-based methods, it is better to consider the DCCB's operating time frame as its own mechanical latency plus the time delay introduced by the MAD-based method. This is because DWT-based protection is set to work as ancillary protection in order to deal with high-resistance faults, which cause lower fault current. Therefore, even if DWT-based protection has a longer time delay, the DCCB would not experience higher overcurrent stress than that in the case of low-resistance faults, which are taken care by the MAD-based protection. For the DC bus protection, the simulation shows that the similar operating time frame of DCCBs is acceptable, because the current differential protection can respond as fast as the MAD-based protection.

The findings also reveal that the cooperation between DCCBs and different protection mechanisms must be taken into consideration. The reason is that the faults in different protection zones may need to be interrupted by the same DCCB, such as the line DCCBs, which must be bidirectional to isolate the bus faults and DC line faults.

5. What is the impact of grounding methods?

   The simulation cases of pole-to-ground faults show that the amplitude of the first peak current depends on the DC capacitor's discharge and the grounding options. Among the grounding methods considered in this thesis, the solid grounding results in the highest peak current amplitude compared to other types of grounding, because it has the lowest soil resistance. Since the fault current rises promptly and the frequency is high, the grounding impedance also has a capacitive and inductive component which makes the influence of the grounding very important for the fault current characteristics.

   The results in Section 7.4 clarify that the grounding methods do not influence the fast responses of the DWT and MAD algorithms. It has been proved that the protection thresholds determined based on an ungrounded HVDC system can be also used for solid grounding, grounding through a resistor, and grounding through a capacitor, but not for grounding through an inductor. The reason for this is that the inductor limits the increasing of the fault current, and thus, the low-value data are recorded when a high sampling frequency is applied. This problem can be resolved by decreasing the sampling frequency, whereby the transient fault current samples with higher values can be recorded for MAD-1 calculation.

Knowing the answers of the five sub-questions, we can understand that the reliable protection of MTDC system lies in the coordination between the fault-limit HVDC converter, the reliable protection methods, and the properly designed DCCB: the protection method must detect the fault reliably and fast, followed by the DCCB interrupting the fault successfully, and most importantly, the HVDC converter must restrain the overcurrent stress caused by the fault for the whole system; therefore, the requirements for the protection and DCCB are less stringent.

8.2. RECOMMENDATIONS FOR FUTURE RESEARCH

1. Field tests for tuning tap-changer and switching capacitor banks.

   The proposed controlling method of LCL-based converter lies in the tuning of an on-load transformer's tap-changer, and the switching of an LCL circuit's capacitor banks. However, since the physical configurations of the tap-changers and switches can be complex, these operations may introduce some electromagnetic phenomena that cannot be modeled in the EMT software, especially when the tuning of the tap-changer and the switching of the capacitor banks are executed simultaneously. Therefore, it is quite necessary to test the time responses when the transformer tap is changed and the capacitor banks are switched.

   Afterwards, the more detailed tap-changer model and switch model can be developed. More importantly, they can be implemented in order to conduct research

beyond the control of LCL-based converter.

2. Ancillary service exploitation of VSC

   The ancillary services, such as reactive power control, voltage control, and black start service, provided to the system operators are important for the system stability. In the thesis, the AC system is modeled as ideal voltage source that does not have stability problems. However, when a practical AC system is considered for the HVDC studies, the ancillary services must be accounted as the stability of AC system can impact the DC network.

   Although the definition of ancillary services varies among different countries, as a part of the transmission system, HVDC grids are subjected to the frameworks of ancillary services. Typically, the aforementioned services concern more for the AC systems; however, acting as the interface between AC and DC grids, the VSCs should at least take part of the responsibility for providing ancillary services for the both AC and DC sides.

   Since the energy buffered in the DC systems reacts similarly to the inertia in AC systems, the AC side's requirement of frequency regulation can be feasibly conducted by the VSC, for example the technique of virtual synchronous generators. Furthermore, if the DC system evolves into a more complex configuration, it would also need some new grid-forming ancillary services, such as DC voltage stabilization and DC-side fault ride through.

3. Implementation of practical units and standards.

   Practical transducers and other equipment can introduce certain time delays during the process of measuring a signal. These devices' bandwidths can also influence the output of the measuring as some important information might be filtered out. Consequently, the signal processing may generate unexpected results.

   At the same time, since the modern protection is usually based on personal computers (PCs), intelligent electronic devices (IEDs), and Ethernet, the delays occurring during the transmission of digital information also need to be discussed. With regards to the DWT-based protection specifically, the thesis considers an ideal transmitting speed of signals in fiber optic, although the practical speed can be lower than this value. This means that the protection scheme needs to be readjusted.

   On the other hand, the protection methods proposed in the thesis adopt high sampling frequencies, i.e., 100kHz and 10kHz for DWT-based and MAD-based protections respectively. Although the frequency of SV messaging can be as high as 96kHz in IEC61869-9, these two frequencies can barely be supported by all the IEDs, especially the frequency of 100kHz. Since the proposed protection method is based on the signal and data processing within and between DC buses, it aligns with the concept of "digital substation". Therefore, it is valuable to conduct the research on the non-conventional instrument transformers (NCIT) and corresponding merging units that can be embedded with the latest standards for HVDC system.

4. Real-time simulations and hardware-in-the-loop.

Carrying out a hardware-in-the-loop (HIL) simulation considers the parallel modeling of MMC-based HVDC systems and physical relay systems. More importantly, the detailed MMC model with firing control is feasible in real-time simulation facilities. Therefore, the most accurate time responses of an MMC-based system can be obtained.

In addition, corresponding to the second suggestion concerning future research, the control-loop can be established by an independent PC running Matlab, which allows the effects of communication channels to be considered. Similarly, the HIL enables the connection of practical transducers. Furthermore, as described in the thesis, the DWT and SWT are both supported in Matlab, and the latter can remove the noise without having strict requirements concerning the sampling frequency. Therefore, it is worth of testing the performance of the SWT when there is sufficient memory for data storing to see if it can provide a more reliable and easily-implementable protection method.

5. Quantitative analysis of the grounding and the modeling of the underground mesh.

   As the grounding elements influence the gradients of fault currents, it is important to obtain the quantitative relations between fault currents and the sizes of different grounding elements. In fact, it has been found that when using discrete algorithms like MAD, its sampling frequency must be coordinated with the grounding methods. As such, the results can guide the determination of the protection scheme.

   When discussing grounding methods, the only variable considered in the thesis is the element connecting the DC-side mid-point and the soil. However, a more practical case is that the elements connect the ports of a metal mesh that is buried underground. Due to the electrical coupling between the ports and the segments of mesh, the frequency-domain responses at a grounding point are complex. Although the vector fitting can be successfully adopted to find the impedance matrix to represent the frequency responses, some applications only use the admittance matrix for the same purpose, and the vector fitting of admittance matrix cannot generate stable simulation due to the numerical compatibility issue. Therefore, using this method in certain software needs to be researched.

6. The dynamic study of the vacuum bottle.

   The di/dt is considered in the thesis for the successful fault interruption. However, the TIV of a DCCB, especially the d(TIV)/dt, also has an impact on the fault interruption. In order to accurately obtain results, the theory must begin by experimenting on practical devices.

   Additionally, the resistance of the vacuum bottle is a non-linear function of the opening time and gap distance, which is much more complex than the switch represented by a two-state resistor in EMT software. Aside from this, the non-linear function of the resistance is also relevant to the opening history of the vacuum bottle, since the plasma generated during each opening in the bottle makes it even less of a vacuum than it was originally. In order to have a more convincing model, these factors should be considered, and the model must be numerically compatible with other components when it is used in a software environment.

7. HVDC system based on both underground cable and overhead line.

   In this thesis, although the underground cable is considered for the DC line system, the OHL is another option for it. More importantly, due to the different physical features, the OHL system usually has higher reactance and lower capacitance than the underground cable. Therefore, the reflection and refraction of the traveling wave on a faulty overhead line would be different from those on a faulty underground cable, especially when there is a hybrid DC line system where the OHL and the cable are connected directly in series. Given by these different properties with regard to traveling wave, the protection method must be readjusted accordingly or re-determined.

   On the other hand, a more frequent fault type in the OHL system is the high-impedance fault, such as when a tree falls down and touches the line. Since the high impedance of the fault can attenuate the transient phenomena, it is important to theoretically analyze the fault responses of the OHL-based HVDC system.

   In the years to come, there are ideas that DC and AC line circuits are installed on the same tower. This type of "mixed" line system can introduce unprecedented challenges for the power system operator: aside of the complex electromagnetic coupling between AC and DC lines, there might be short circuit occurs between the AC and DC lines, and the subsequent system responses can be profound. Thus, this can be an interesting topic for the power system research.

8. Protection methods that can distinguish lightning strokes.

   The main concerns in this thesis are the pole-to-pole and pole-to-ground faults that can occur in an underground cable system. Consequently, the lightning strokes are not considered when designing the protection methods. Therefore, it is necessary to find solutions to this problem when the proposed methods are implemented for an OHL system.

   Since the wave front of lightning-caused surge usually lasts for 1.2μs, whilst that of fault-caused surge usually lasts for 100μs, the fast sampling technique and advanced algorithm are necessary to identify different wave fronts. On the other hand, because the investigation of lightning is in the scope of several microseconds, the high frequency model of HVDC converter is critical for this study.

GLOSSARY

AC alternating current.

ACCB AC circuit breaker.

CBs circuit breakers.

CCSCs circulating current suppression controllers.

CIGRE International Council on Large Electric Systems.

DC direct current.

DCCB DC circuit breaker.

DWT discrete wavelet transform.

EMT electromagnetic transient.

FB full-H bridge.

FCL fault current limiter.

FFT Fast Fourier Transform.

FIRs finite impulse response filters.

GTO gate turn-off thyristor.

HB half-H bridge.

HIL hardware-in-the-loop.

HVDC high voltage DC.

ICT information and communication technology.

IEDs intelligent electronic devices.

IEEE Institute of Electrical and Electronics Engineers.

IGBT insulated-gate bipolar transistor.

KCL Kirchhoff's current law.

KVL Kirchhoff's voltage law.

LC inductor-capacitor.

LCC line-commutated converter.

LCL inductor-capacitor-inductor.

LCP Line Constants Program.

MAD median absolute deviation.

MCOV maximum continuous operating voltage.

MMC modular multilevel converter.

MTDC multi-terminal HVDC.

NCIT non-conventional instrument transformers.

OHL overhead line.

PCC point of common coupling.

PI proportional integral.

PLL phase-lock loop.

pu per unit.

PWM pulse width modulation.

rms root mean square.

ROCOV rate of change of voltage.

RTDS Real Time Digital Simulator.

SM sub-module.

STFT short-time Fourier Transform.

SV sample value.

SWT stationary wavelet transform.

TIV transient interruption voltage.

UHVDC ultra-high-voltage DC.

VSC voltage source converter.

WT wavelet transform.

ACKNOWLEDGMENT

FIRSTLY, I would like to express my sincere gratitude to my promotors Prof. Mart van der Meijden and Dr. Marjan Popov for the continuous support of my Ph.D study and related research, for your patience, motivation, and immense knowledge. Your guidance and feedback helped me in all the time of research and writing of this thesis. I could not have imagined having a better advisor and mentor for my Ph.D study.

Besides my supervisors, I would like to thank my thesis committee: Prof. Dong, Prof. Chen, Mr. Drobnjak, Prof. Palensky and Prof. Vaessen for their insightful comments which inspired me to widen my research from various perspectives.

I would also acknowledge my friend Dr. Romain Thomas, you were the first guy I met in the group, and I really appreciate that you showed me around in the IEPG, even though your French-accent English drove me mad from the very beginning. Furthermore, I must admit that the muffin and pie you baked tasted so good.

My time at Delft was made enjoyable in large part due to the many friends and groups that became a part of my life. I am grateful for time spent with Hossein, Swasti, Martija, Tina, Rishabh, Jose and Catalina, for Martija and Tina's hospitality when we were participating your wedding ceremony, for our unforgettable trips in Slovenia and Croatia, and for many other people and memories. And, Nakisa, Viney, Arcadio, and Isidora, it was great to work and have dinner with you.

I am grateful to the Chinese Mafia (unofficial) in the IEPG group. Kaikai, Siyuan, Zhou, Chenguang, Aihui, you are all terrific friends to me; I would miss the amusing talks we had, and the time we spent together playing UNO was so amazing.

I appreciate Dr. Bart Tuinema for translating the summary and propositions of my thesis into Dutch. Also, it was a good cooperation with you in TSO2020. Ilya, Arun, Claudio, Digvijay and all the other IEPG colleagues, thank you so much for the fantastic working environment.

I gratefully acknowledge the funding sources that made my Ph.D. work possible. I was funded by the scholarship of China Scholarship Council for my four-year PhD study. From October 2017 to October 2018, I was financed by the TSO2020 project to work as a Research Associate, and I must appreciate this opportunity that Jose gave me.

Lastly, I would like to thank my family for all their love and encouragement. For my parents who raised me with a love of science and supported me in all my pursuits. And most of all for my loving, supportive, encouraging, and patient girlfriend Yuhan whose faithful support during the whole process of this Ph.D. is so appreciated. Thank you.

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Lian Liu was born in Wuhan, China in 1987. He received both his Bachelor and Master degrees from Wuhan University, Wuhan, China, respectively in 2010 and 2013. Since October 2013, he started his PhD project in Delft University of Technology, Delft, The Netherlands, where he studied the transient behavior in MTDC system. The project is funded by China Scholarship Council (CSC). From October 2017 to October 2018, he worked as Research Associate in Activity 2 of project TSO2020. The task of Activity 2 is to exploiting the ancillary services of electrical network in northern Netherlands.

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