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Graphene Nanoribbon-Based Analog-to-Digital Conversion

Pim Verton[1] and Sorin Coțofană[2]

Abstract— This paper introduces a novel approach towards Analog-to-Digital Converter (ADC) implementation that combines Graphene Nanoribbon (GNR) devices capabilities to provide augmented (more complex than a switch) functionality with the fact that each output bit $b_i, i \in [0, n-1]$ of an n-bit ADC is defined as a periodic symmetric function $F_i(V_{\text{in}})$ with period $\frac{V_{\text{max}}}{2^i}$, of the ADC input $V_{\text{in}} \in [0, V_{\text{max}}]$. As such, by making use of the Boolean function implementation methodology with two complementary GNRs, the implementation of an n-bit ADC requires $2n$ GNR devices. To demonstrate our approach we present the implementation of a 4-bit ADC and the evolutionary algorithm that identifies the GNR topologies required for $F_i(V_{\text{in}}), i \in [0, 3]$ evaluation when $V_{\text{in}} \in [0, 200\text{ mV}]$. We demonstrate the correct functionality of our proposal by means of SPICE simulations and compare it with state-of-the-art counterparts. The comparison indicates that our approach exhibits around five orders of magnitude lower power consumption, is operating at four orders of magnitude larger sample frequency, requires nine orders of magnitude lower real estate, and, in terms of Walden's figures of merit, scores three orders of magnitude better in time per conversion step and nine in energy per conversion step. The required GNR device topologies are identified by means of an evolutionary algorithm, allowing a design space of many trillions of possible devices to be searched by evaluating the behaviour of only a few hundred thousand different topologies.

I. INTRODUCTION

Graphene is a novel material with many interesting properties, e.g., atomic thinness and 2D structure, ballistic transport, ultrahigh intrinsic carrier mobility, outstanding thermal properties, ability to sustain very high current densities [1], [2], [3], [4]. These properties opened roads towards its utilization in, e.g., electronics, spintronics, photonics and optoelectronics, sensing, energy storage and conversion, flexible electronics, and biomedical applications.

In particular, its unique electronic properties fostered research towards replacing conventional CMOS circuits by, or augmenting them with graphene-based counterparts [5]. Initially, the community followed the idea of making use of graphene nanoribbons (GNRs) as a FET conduction channel to obtain better switches, which are foundational for Boolean gate implementations. To this end Lemme et al. [6] introduced graphene FETs (GFETs), which exhibit better mobility than conventional CMOS transistors, which were followed by numerous GNR FET proposals, (e.g., [7], [8], [9]) and tunneling GNR FETs, (e.g., [10], [11], [12], [13]).

Jiang et al. [14] went beyond replacing FETs with graphene-based counterparts and introduced augmented functionality graphene devices and proposed Boolean gate implementations by means of complementary GNR pairs. They demonstrated that by changing the GNR topology, more complex behaviour than a simple on-off switch can be obtained and that two devices with complementary behaviour can be combined in a CMOS-alike style. As such they proposed and validated by means of simulation [15] GNR-based implementations of, e.g., (N)AND, (N)OR, X(N)OR, gates that substantially outperform CMOS counterparts [16]. Wang et al. [17] and Dumitru et al. [18] then went another step further by designing artificial synapses and digital-to-analog converters consisting of GNR devices, respectively. Thus, they proved that analog, complex behaviour can be obtained by means of functional complementary GNR circuit pairs.

In this paper we continue the same line of thinking and propose GNR-based Analog-to-Digital Converter (ADC) circuits. Our proposal builds upon the fact that the behaviour of each ADC output bit (b_i) can be described as a periodic symmetric function on the ADC input $V_{\text{in}} \in [0, V_{\text{max}}]$, with a period $\frac{V_{\text{max}}}{2^i}$ [19], as graphically depicted in Fig. 3 for a 4-bit ADC of V_{in} between 0 and 200 mV. Thus, the implementation of an n-bit ADC requires n GNR pairs, each of them evaluating $b_i, i \in [0, n-1]$ as a periodic symmetric function of V_{in}, with a period $\frac{V_{\text{max}}}{2^i}$.

As a result of utilizing GNR devices with complex, analog, behaviour, the proposed ADC consists of only a handful of devices, $2n$ GNRs for an n-bit ADC. Thus, our proposal results in ADC circuits which substantially outperform state-of-the-art CMOS ADC circuits in terms of circuit area, latency, power consumption, and composite metrics such as transition energy and Walden's figures of merit [20].

The rest of this paper is organised as follows. In Section II, we briefly discuss graphene related background and the simulation model we utilize to determine expected GNR device behaviours. In Section III, we introduce the ADC circuit architecture and the required behaviour of its constituent GNR devices. In Section IV, we introduce the evolutionary algorithm utilized to identify GNR devices able to provide the requested functionality. Afterwards, in Section V, we present SPICE simulation results for a 4-bit ADC circuit and compare its per-

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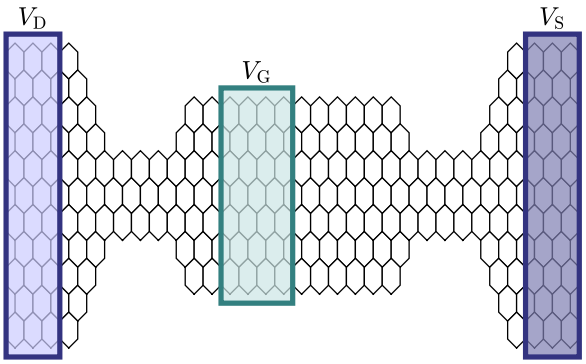

Fig. 1. Generic GNR device topology.

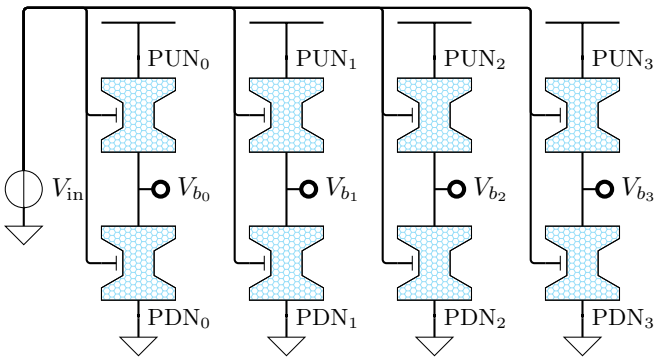

Fig. 2. 4-bit ADC circuit schematics.

formance to that of similar conventional CMOS ADCs. Finally, Section VI presents some conclusions.

II. Background and GNR Simulation

Fig. 1 presents a GNR device example. It consists of a shaped piece of graphene, the graphene nanoribbon, on a substrate and biased via two terminal contacts, drain and source, by V_D and V_S, respectively. The GNR acts as a conduction channel between these terminals, the conductance of which is controlled by a dynamic bias V_G applied at a gate contact positioned somewhere along the channel. A static biasing voltage V_{Back} can be also applied to a back gate to further adjust the channel conduction range.

The GNR device behaviour strongly depends on its specific topology, i.e., the GNR shape and the location, size, and biasing of each contact. We note that, to date, no predictive model to relate GNR topology to its electrical behaviour has been proposed and as such, the behaviour can be only derived by means of atomistic simulations. In this paper we make use of the simulation model described earlier by Wang et al. [21] and Jiang et al. [22], which employs the non-equilibrium Green function model of quantum transport, where the system Hamiltonian is obtained using semi-empirical tight binding computations, and the Landauer-Büttiker formalism is utilized to derive the conduction and current through the GNR device. This simulation produces a so-called conduction map that captures the relation between the modulating potential V_G and the conductance of the GNR channel between the terminal contacts. From this conduction map, a lookup table-based Verilog-A model is created, which is utilized to perform circuit level SPICE simulations of graphene circuits.

III. GNR-based Analog-to-Digital Converter

Due to the nature of positional number representation, each output bit $b_i, i \in [0, n-1]$ of an n-bit Analog to Digital Converter (ADC) is defined as a periodic symmetric function $F_i(V_{in})$ with period $\frac{V_{max}}{2^i}$, of the ADC input $V_{in} \in [0, V_{max}]$ [19]. Thus, a GNR-based n-bit ADC implementation requires n complementary GNR pairs, each of them evaluating $b_i = F_i(V_{in})$. While this structure is generic, for the sake of discussion simplicity we make use from here on of a 4-bit ADC as a discussion vehicle. Fig. 2 presents the 4-bit ADC circuit built with 8 GNR devices, making up 4 complementary pairs evaluating $V_{b_i} = F_i(V_{in}), i \in [0, 3]$ as described in Fig. 3 for V_{in} values between 0 and 200 mV.

To correctly evaluate $F_i(V_{in})$, the topologies of GNR devices pairs have to be properly chosen such that together each pair implements its own transfer function, mapping the input voltage V_{in} to the correct V_{b_i} value in concordance with the logic value "low" (logic 0) or "high" (logic 1) in Fig. 3. Such a transfer function maps alternating sections of the input signal's range to either a low or a high voltage, corresponding to the required bit b_i of the 4-bit digital symbol representing the value of V_{in}. The required conduction map of each GNR device can be derived from these transfer functions as follows. For each V_{in} value, if V_{b_i} needs to be low, the conductance G_{PDN_i} of the corresponding Pull-Down Network (PDN) GNR device should be high, whereas the conductance G_{PUN_i} of the respective Pull-Up Network (PUN) GNR device should be low. Similarly, when V_{b_i} needs to be high, G_{PDN_i} should be low and G_{PUN_i} high.

Given that the V_{in} range is from 0 mV to 200 mV, and we are concerned with a 4-bit ADC, each 12.5 mV segment of this range corresponds to a different 4-bit digital symbol. Therefore, the required transfer functions for each complementary pair are plotted in Fig. 3 with respect to V_{in}, and in Fig. 4 and Fig. 5 the required conduction maps for all the GNR devices in the circuit are plotted. One can easily observe in Fig. 4 and Fig. 5 that the key attribute to look for in the GNR devices conduction maps is periodicity; GNR devices involved into the b_i evaluation should exhibit periodic conduction maps with a period proportional to $\frac{1}{2}^i$.

As no formal method exists to deduce the GNR topology for a given conduction map, the identification of appropriate GNR topologies requires many very time consuming atomistic simulations. To alleviate this is-

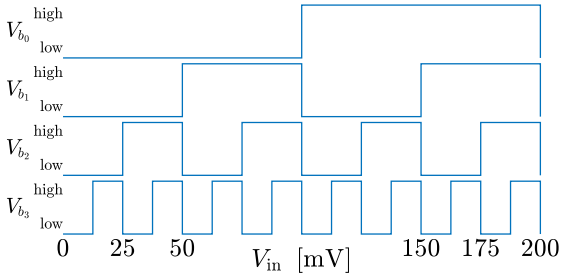

Fig. 3. Complementary GNR pair required transfer function qualitatively plotted with respect to V_{in} value.

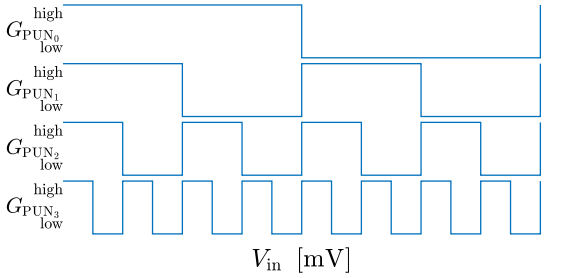

Fig. 4. Required PUN GNR devices behaviour.

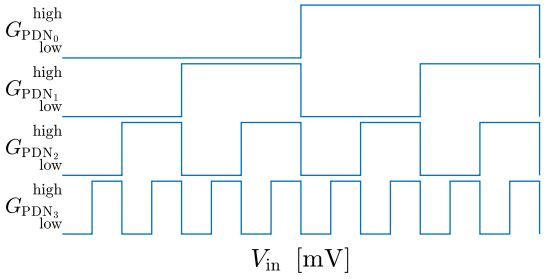

Fig. 5. Required PDN GNR devices behaviour.

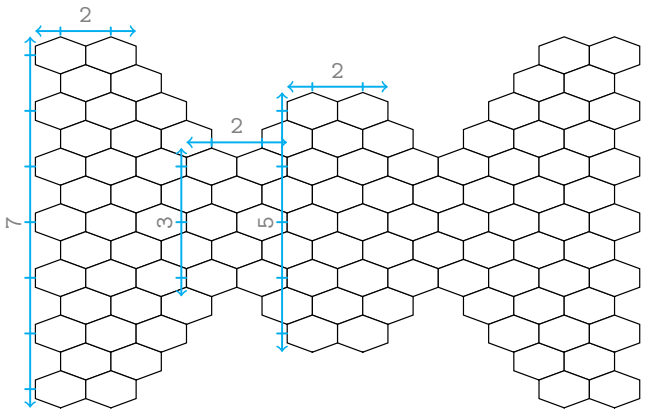

Fig. 6. A mutable specification for a GNR device topology. The features' dimensions are measured in hexagonal unit cells, which are also indicated with small marks along the arrows.

sue, in the next section, we introduce an evolutionary algorithm that we make use of to find suitable GNR geometries for the 4-bit ADC implementation.

IV. Evolutionary Algorithm for GNR Topology Identification

To be able to utilize an evolutionary algorithm to find GNR device topologies we need to: (i) propose a method of generating random GNR devices and mutating them incrementally and (ii) define a fitness function which evaluates candidate GNR devices by their suitability in the context of the ADC circuit.

For the first requirement, we propose a simple way of specifying GNR device topologies based on Jiang et al.'s work in [23]. Rather than limiting us to classes like "camel"- or "butterfly"-shaped devices, we specify devices as symmetric arbitrary-length series of alternating "constrictions" and "bumps". Fig. 6 presents such a device, which consists of a bump with a length of 2 hexagonal unit cells and height of 5 unit cells, surrounded by 2-unit long constrictions with a height of 3 units, and finally bumps at the ends of length 2 and height 7.

These dimensions, i.e., lengths and heights of bumps and constrictions, can easily be randomly generated to create aleatory GNR topologies and can also be incremented or decremented to mutate these topologies. In addition to the GNR shape, gate contact position and size, terminal contacts size, and back gate biasing are also randomly generated and mutable. Together, these parameters account for a design space with a size on the order of 10^{14} different device topologies.

The second requirement, the fitness function, should evaluate a GNR device topology and assign it a score based on how well it conforms to the required behaviour defined in Section III. To this end we first utilize the simulation method in Section II to calculate a low-resolution (2 mV steps) conduction map that associates V_{in} to the drain-source device conductance G. Subsequently, we treat this conduction map as a waveform with respect to V_{in} and evaluate its dominant frequency, phase, amplitude, and the correctness of the digitized signal with respect to the expected behaviour. The signal digitization requires some clarification. Each value of the conduction map can be classified as being "high" or "low" conductance, either relative to the range of the conduction map itself, or to some absolute threshold. For the former, we compare each conductance value to the 40^{th} and 60^{th} percentile values of the conduction

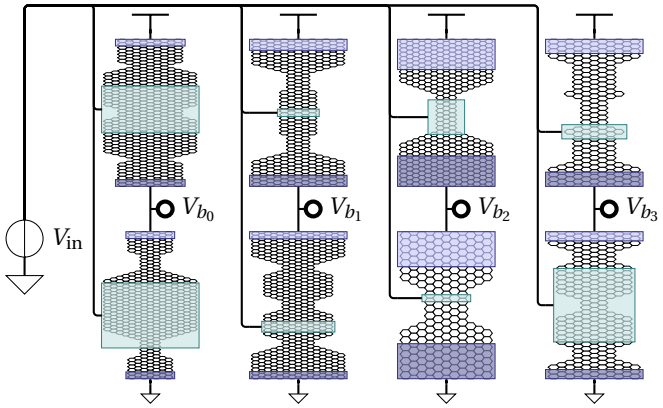

Fig. 7. 4-bit ADC circuit GNR device geometries.

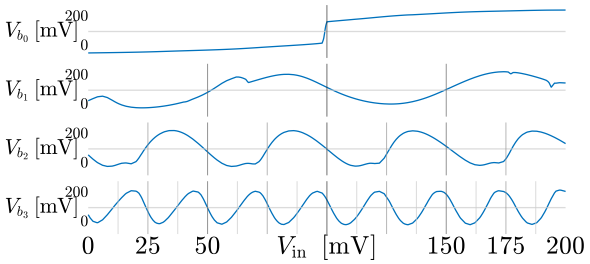

Fig. 8. 4-bit ADC SPICE simulation results.

map. For the latter, we compare the conductance value to the 40^{th} and 60^{th} percentiles of all conductance values of a large dataset of GNR devices, respectively, 0.74 µS and 2.8 µS. In both cases, conductance values above the upper threshold we call "high" values, conductance values below the lower threshold are "low", and everything in between is "intermediate". This results in a discrete-valued signal which can be compared to the required qualitative conduction map as presented in Fig. 4 and Fig. 5.

We finally combine all these metrics into a single one-dimensional fitness score that indicates the appropriateness of the current GNR candidate as PDN_i or PUN_i device. This combined score is calculated using a weighted mean. This fitness function is different for each GNR device in the ADC circuit according to their required conduction map. Similarly, this fitness function could also easily be replaced according to some other set of requirements to identify the topology of a GNR device for some arbitrary other purpose.

By executing the evolutionary algorithm for all the 8 devices we identify a suitable candidate for each component. The evolutionary algorithm searches for one GNR device geometry at a time, evaluating a pool of 120 different configurations at a time in parallel according to this fitness function. For each generation, the top ten fittest devices get selected, as well as two random ones to avoid some early convergence on a local optimum. Each of these devices is mutated into ten new configurations each to create the next generation. After the evaluation of 15 generations the process starts over with a fresh pool of devices, while remembering the configurations which resulted in devices with the highest fitness. This again repeats 15 times, such that a total of $15 \cdot 15 \cdot 120$ different device configurations are evaluated to find the best geometry for a given ADC circuit component.

V. Simulation Results

Having evaluated the fitness of in total a few hundred thousand devices out of a potential design space of many trillions of possible GNR device topologies, Fig. 7 displays the 4-bit ADC circuit consisting of the eight found GNR device topologies. Table I presents the topology of each ADC's GNR devices. The GNR shape is defined as a sequence of segments, each with a length and a height in hexagonal unit cells, just as how they're indicated in Fig. 6. The Table also specifies the terminal and gate contact length, gate contacts position as an offset from the drain contact, and the back gate biasing voltage.

Fig. 8 presents the 4-bit ADC SPICE simulation results for $V_{\text{in}} \in [0, 200\ \text{mV}]$. A horizontal line is drawn on each plot at $V_{b_i} = 100$ mV, which is the threshold value to determine the digital value b_i of each output signal V_{b_i}. Vertical lines indicate V_{in} values for which b_i's value should change.

Note that the V_{b_i} digital values—and therefore the transfer functions of the ADC—follow the required values quite closely. Specifically, the most significant bit, b_0 is the most accurate, having the correct value for 99.6 % of V_{in} values, whereas the least significant bit b_3 has the correct value in 83.4 % of the circumstances.

From these transfer functions, we can determine the 4-bit output of the ADC circuit for each $V_{\text{in}} \in [0, 200\ \text{mV}]$ value. Knowing the expected output value we can then determine the error as a function of V_{in}. As such we obtain a Root Mean Square (RMS) error value, when integrated over the entire input range, of around 1.1 times the LSB value. This translates to a Signal-to-Noise Ratio (SNR) of around 14 dB, which in turn corresponds to an effective resolution of 3.1 bits.

To determine the conversion delay (τ_{p}) and power consumption (P) we make use of a simple circuit model [24], consisting of a contact resistance (R_{C}), a GNR channel resistance (R_{GNR}), and a gate capacitance (C_{G}). R_{C} and C_{G} are both determined from the GNR dimensions, while R_{GNR} follows from the conductance simulation. From (τ_{p}) and (P) values we calculate the transition energy (E_{t}) and Walden's figures of merit (P_{Walden} and F_{Walden}). To determine the circuit area we assume a rectangular footprint the size of the outer dimensions of each GNR

GNR Device	Segment lengths [unit cells]	Segment heights [unit cells]	Terminal length [unit cells]	Gate length [unit cells]	Gate position [unit cells]	Back gate bias [V]
PUN_0	[4, 7, 1, 7, 1, 7, 4]	[6, 3, 4, 2, 4, 3, 6]	3	3	19	-0.05
PDN_0	[3, 4, 6, 4, 6, 4, 3]	[6, 3, 5, 2, 5, 3, 6]	2	16	9	0.05
PUN_1	[10, 10, 10]	[8, 2, 8]	7	8	15	-0.10
PDN_1	[7, 6, 7]	[6, 3, 6]	5	1	10	0.20
PUN_2	[7, 6, 12, 6, 7]	[7, 2, 3, 2, 7]	3	2	20	0.10
PDN_2	[7, 3, 6, 4, 6, 3, 7]	[8, 3, 6, 3, 6, 3, 8]	2	3	26	0.00
PUN_3	[7, 2, 10, 4, 10, 2, 7]	[5, 3, 7, 5, 7, 3, 5]	2	14	15	0.20
PDN_3	[6, 6, 15, 6, 6]	[4, 2, 8, 2, 4]	2	19	16	0.15

TABLE I

4-bit ADC GNRs topology specifications.

device.

Table II presents a comparison of the 4-bit GNR ADC circuit in terms of several key metrics with a selection of conventional low-resolution CMOS ADC circuits, as collected by [32]. Note that the comparison is skewed in a few ways. First, the metrics describing the GNR ADC performance are very simplistically estimated, not taking into account any interconnect, overhead, noise, or quantum capacitance.

Apart from that, the ADC circuits in the Table have a higher than 4-bit resolution, and it is well known that ADC circuits generally scale quite dramatically with resolution in terms of circuit complexity and conversion cost.

In the case of this GNR ADC circuit, increasing the resolution would entail finding GNR device topologies to implement additional bits in the same way as was done for these four bits. These additional GNR devices would contribute roughly a linear increase in terms of power cost and circuit area. Further research [33] suggests that further bits of resolution would yield gradually diminishing returns in terms of accuracy and require physically larger GNR devices. This suggests that it would be possible to increase the resolution of this ADC circuit, but not to an arbitrary degree. Apart from or on top of that, more conventional ADC design techniques such as successive approximation could also be applied to yield a higher resolution.

In spite of this circuit's low resolution, the Table suggests that our proposal has the potential to substantially outperform state-of-the-art counterparts. More specifically: by having around five orders of magnitude lower power consumption, operating at four orders of magnitude larger sample frequency, and requiring a nine orders of magnitude lower real estate. In terms of Walden's figures of merit, the GNR ADC circuit scores three orders of magnitude better in time per conversion step and nine in energy per conversion step. These improvements can be attributed to the GNR ADC circuit simplicity, i.e., consists of only a handful of components, whereas conventional ADC circuits are rather complex [34], which induces substantial power consumption and delay overheads.

VI. Conclusions

We introduced a novel approach towards Analog-to-Digital Converter (ADC) implementation that builds upon Graphene Nanoribbon (GNR) devices capabilities to provide augmented (more complex than a switch) functionality and the fact that each output bit $b_i, i \in [0, n-1]$ of an n-bit ADC is defined as a periodic symmetric function $F_i(V_{\text{in}})$ with period $\frac{V_{\max}}{2^i}$, of the ADC input $V_{in} \in [0, V_{max}]$. As such, by making use of the Boolean function implementation methodology with two complementary GNRs, an n-bit ADC requires $2n$ GNR-based devices. We assumed that $V_{\text{in}} \in [0, 200\text{ mV}]$ and demonstrated our approach by implemented a 4-bit ADC. We demonstrated the correct functionality of our proposal by means of SPICE simulations and compared it with state-of-the-art counterparts. The comparison indicated that our approach exhibits around five orders of magnitude lower power consumption, is operating at four orders of magnitude larger sample frequency, requires nine orders of magnitude lower real estate, and, in terms of Walden's figures of merit, scores three orders of magnitude better in time per conversion step and nine in energy per conversion step.

Furthermore, the methodology of using an evolutionary algorithm to identify suitable GNR device topologies could be utilized for many other applications by simply altering the algorithm's fitness function. This could improve the efficiency of identifying such topologies by many orders of magnitude, similar to how in this case a design space of trillions of possible GNR devices is searched by only evaluating several hundred thousand topologies.

References

[1] A. K. Geim and K. S. Novoselov, "The rise of graphene," Nature Materials, vol. 6, pp. 183–191, Mar. 2007.

[2] E. J. Duplock, M. Scheffler, and P. J. D. Lindan, "Hallmark of Perfect Graphene," Physical Review Letters, vol. 92, p. 225502, June 2004.

[3] A. E. Galashev and O. R. Rakhmanova, "Mechanical and thermal stability of graphene and graphene-based materials," Physics-Uspekhi, vol. 57, p. 970, Oct. 2014.

[4] C. Lee, X. Wei, J. W. Kysar, and J. Hone, "Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene," Science, vol. 321, pp. 385–388, July 2008.

ADC Type	$R_{\text{eff.}}$ [bit]	P [mW]	F_{s} $\left[\frac{\text{Gsample}}{\text{s}}\right]$	P_{Walden} $\left[\frac{\text{ps}}{\text{step}}\right]$	F_{Walden} $\left[\frac{\text{pJ}}{\text{step}}\right]$	A $\left[\text{mm}^2\right]$
GNR	3.07	$0.80 \cdot 10^{-3}$	$0.23 \cdot 10^{6}$	$0.53 \cdot 10^{-3}$	$0.42 \cdot 10^{-9}$	$0.2 \cdot 10^{-9}$
32 nm 6-bit TI Flash [25]	4.81	70	20	1.78	0.12	0.25
65 nm 6-bit TI MBS [26]	4.62	88	25	1.63	0.14	0.24
16 nm 8-bit TI SAR [27]	4.9	280	28	1.20	0.33	2.80
28 nm 6-bit TI SAR-TDC [28]	4.51	23	24	1.83	0.04	0.03
7 nm 8-bit TI SAR [29]	4.6	150	29	1.42	0.21	0.09
16 nm 8-bit TI Flash-TDC [30]	5.6	175	20	1.03	0.18	0.10
65 nm 8-bit TI TD [31]	6.15	130	20	0.70	0.09	0.22
40 nm 6-bit TI 2S Flash [32]	4.71	56	20	1.91	0.11	0.10

TABLE II

GNR ADC vs conventional low-resolution ADC circuits.

[5] A. S. Mayorov et al., "Micrometer-scale ballistic transport in encapsulated graphene at room temperature," Nano letters, vol. 11, no. 6, pp. 2396–2399, 2011.

[6] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A Graphene Field-Effect Device," IEEE Electron Device Letters, vol. 28, pp. 282–284, Apr. 2007.

[7] Y.-Y. Chen, A. Sangai, M. Gholipour, and D. Chen, "Schottky-barrier-type Graphene Nano-Ribbon Field-Effect Transistors: A study on compact modeling, process variation, and circuit performance," in 2013 IEEE/ACM International Symposium on Nanoscale Architectures, pp. 82–88, July 2013.

[8] Y.-Y. Chen, A. Rogachev, A. Sangai, G. Iannaccone, G. Fiori, and D. Chen, "A SPICE-compatible model of Graphene Nano-Ribbon Field-Effect Transistors enabling circuit-level delay and power analysis under process variation," in 2013 Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 1789–1794, Mar. 2013.

[9] L.-T. Tung and E. C. Kan, "Sharp Switching by Field-Effect Bandgap Modulation in All-Graphene Side-Gate Transistors," IEEE Journal of the Electron Devices Society, vol. 3, pp. 144–148, May 2015.

[10] H. Mohamadpour and A. Asgari, "Graphene nanoribbon tunneling field effect transistors," Physica E: Low-dimensional Systems and Nanostructures, vol. 46, pp. 270–273, Sept. 2012.

[11] W. Mehr et al., "Vertical Graphene Base Transistor," IEEE Electron Device Letters, vol. 33, pp. 691–693, May 2012.

[12] L. Britnell et al., "Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures," Science, vol. 335, pp. 947–950, Feb. 2012.

[13] P. Zhao, R. M. Feenstra, G. Gu, and D. Jena, "SymFET: A Proposed Symmetric Graphene Tunneling Field-Effect Transistor," IEEE Transactions on Electron Devices, vol. 60, pp. 951–957, Mar. 2013.

[14] Y. Jiang, N. C. Laurenciu, and S. D. Cotofana, "On Carving Basic Boolean Functions on Graphene Nanoribbons Conduction Maps," in 2018 IEEE International Symposium on Circuits and Systems (ISCAS), (Florence), pp. 1–5, IEEE, May 2018.

[15] S. Datta, Quantum Transport: Atom to Transistor. Cambridge: Cambridge University Press, 2005.

[16] Y. Jiang, N. C. Laurenciu, H. Wang, and S. D. Cotofana, "Graphene Nanoribbon Based Complementary Logic Gates and Circuits," IEEE Transactions on Nanotechnology, vol. 18, pp. 287–298, 2019.

[17] H. Wang, N. C. Laurenciu, Y. Jiang, and S. Cotofana, "Graphene Nanoribbon-based Synapses with Versatile Plasticity," in 2019 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), pp. 1–6, July 2019.

[18] F.-S. Dumitru, N. Cucu-Laurenciu, A. Matei, and M. Enachescu, "Graphene Nanoribbons Based 5-Bit Digital-to-Analog Converter," IEEE Transactions on Nanotechnology, vol. 20, pp. 248–254, 2021.

[19] S. Cotofana and S. Vassiliadis, "Periodic symmetric functions, serial addition, and multiplication with neural networks," IEEE Transactions on Neural Networks, vol. 9, pp. 1118–1128, Nov. 1998.

[20] R. Walden, "Analog-to-digital converter survey and analysis," IEEE Journal on Selected Areas in Communications, vol. 17, pp. 539–550, Apr. 1999.

[21] H. Wang, N. C. Laurenciu, Y. Jiang, and S. D. Cotofana, "Atomistic-Level Hysteresis-Aware Graphene Structures Electron Transport Model," in 2019 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1–5, May 2019.

[22] Y. Jiang, N. C. Laurenciu, and S. Cotofana, "Non-Equilibrium Green Function-based Verilog-A Graphene Nanoribbon Model," in 2018 IEEE 18th International Conference on Nanotechnology (IEEE-NANO), pp. 1–4, July 2018.

[23] Y. Jiang, N. C. Laurenciu, and S. Cotofana, "Complementary Arranged Graphene Nanoribbon-based Boolean Gates," in 2018 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), pp. 1–7, July 2018.

[24] Y. Jiang, N. Cucu Laurenciu, and S. D. Cotofana, "On Basic Boolean Function Graphene Nanoribbon Conductance Mapping," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, pp. 1948–1959, May 2019.

[25] V. H.-C. Chen and L. Pileggi, "A 69.5 mW 20 GS/s 6b Time-Interleaved ADC With Embedded Time-to-Digital Calibration in 32 nm CMOS SOI," IEEE Journal of Solid-State Circuits, vol. 49, pp. 2891–2901, Dec. 2014.

[26] S. Cai, E. Zhian Tabasy, A. Shafik, S. Kiran, S. Hoyos, and S. Palermo, "A 25 GS/s 6b TI Two-Stage Multi-Bit Search ADC With Soft-Decision Selection Algorithm in 65 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 52, pp. 2168–2179, Aug. 2017.

[27] Y. Frans et al., "A 56-Gb/s PAM4 Wireline Transceiver Using a 32-Way Time-Interleaved SAR ADC in 16-nm FinFET," IEEE Journal of Solid-State Circuits, vol. 52, pp. 1101–1110, Apr. 2017.

[28] B. Xu, Y. Zhou, and Y. Chiu, "A 23-mW 24-GS/s 6-bit Voltage-Time Hybrid Time-Interleaved ADC in 28-nm CMOS," IEEE Journal of Solid-State Circuits, vol. 52, pp. 1091–1100, Apr. 2017.

[29] D. Pfaff et al., "A 56-Gb/s Long-Reach Fully Adaptive Wireline PAM-4 Transceiver in 7-nm FinFET," IEEE Solid-State Circuits Letters, vol. 2, pp. 285–288, Dec. 2019.

[30] S.-J. Kim, Z. Myers, S. Herbst, B. Lim, and M. Horowitz, "20-GS/s 8-bit Analog-to-Digital Converter and 5-GHz Phase Interpolator for Open-Source Synthesizable High-Speed Link Applications," IEEE Solid-State Circuits Letters, vol. 3, pp. 518–521, 2020.

[31] M. Zhang, Y. Zhu, C.-H. Chan, and R. P. Martins, "A 20GS/s 8b Time-Interleaved Time-Domain ADC with Input-Independent Background Timing Skew Calibration," in 2021 Symposium on VLSI Circuits, pp. 1–2, June 2021.

[32] D.-R. Oh, "A 6-Bit 20 GS/s Time-Interleaved Two-Step Flash ADC in 40 nm CMOS," Electronics, vol. 11, p. 3052, Jan. 2022.

[33] P. Verton, "Graphene Genetics: Designing an Analog-to-Digital Converter in Graphene Utilizing an Evolutionary Algorithm," Master's thesis, Delft University of Technology, Delft, Apr. 2024. Available at http://resolver.tudelft.nl/uuid:492066af-8f83-40c0-84ed-ef31ba77833c.

[34] S. Park, Y. Palaskas, and M. P. Flynn, "A 4-GS/s 4-bit Flash ADC in 0.18-µm CMOS," IEEE Journal of Solid-State Circuits, vol. 42, pp. 1865–1872, Sept. 2007.