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An Auto-Zero Stabilized Voltage Buffer with a Trimmed Input Current of 0.2pA

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***Abstract*—This paper presents an input-current trimming scheme for auto-zero amplifiers. Since their input current is mainly due to charge injection, the scheme operates by trimming the clock swing, and hence the charge injection, of two dummy input switches. At room temperature, the trimming scheme reduces the maximum input current of an auto-zero stabilized voltage buffer from 1pA to 0.2pA (13 samples) over its full input voltage range (0 to 1.3V). This increases to 0.4pA over temperature (0 to 85°C), which is well below the leakage of typical ESD diodes, and is the lowest input current ever reported for an auto-zero amplifier.**

I. Introduction

The readout of high impedance sensors and sampled voltage references [1] requires amplifiers with a combination of low offset, low voltage noise and low input current. To achieve the former, dynamic offset compensation techniques, such as chopping and auto-zeroing, are often used. However, the associated switching activity gives rise to significant input current, which is often in the order of several tens of pAs [2,3]. Furthermore, it also causes output spikes, making it more difficult to interface such amplifiers with subsequent circuitry.

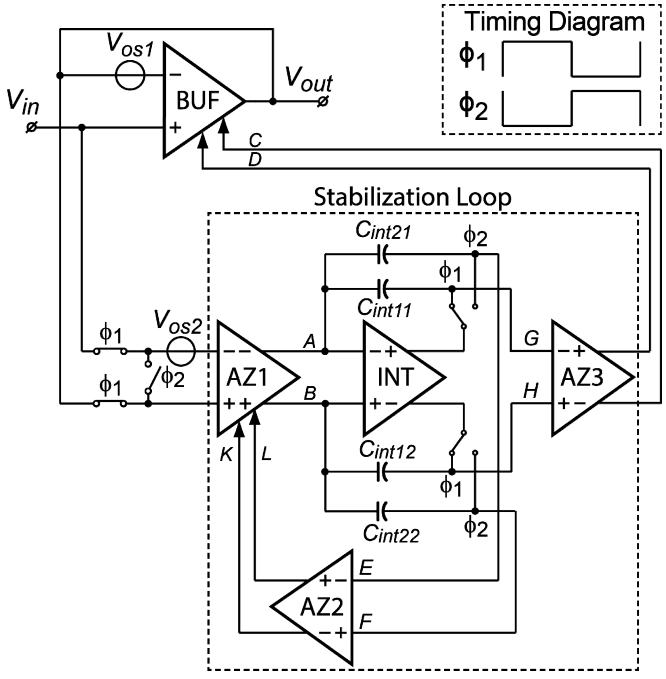

Fig. 1. Simplified block diagram of an auto-zero stabilized voltage buffer

Recently, an auto-zero (AZ) stabilized buffer has been proposed [4,5]. As shown in Fig. 1, it consists of a buffer (BUF), whose offset (V_{os1}) and 1/*f* noise are periodically cancelled by an AZ stabilization loop. The latter consists of an OTA (AZ1), an integrator (INT and $C_{int11\text{-}int12}$, 10pF each) and a second OTA (AZ3) [4]. AZ1 is itself auto-zeroed by a second AZ loop, which consists of an integrator (INT and $C_{int21\text{-}int22}$, 10pF each) and another OTA (AZ2).

This design achieves state-of-the-art offset (< 1μV) and low-frequency noise performance (only √2× higher than the buffer's own thermal noise floor). However, the charge injection of its input switches gives rise to significant input current: up to 0.8pA [5]. Since this current is relatively independent of input voltage, however, it can be effectively trimmed at a single input voltage.

In [6], the input current of a chopper amplifier is also trimmed. To ensure that switching artefacts can be easily filtered out, the amplifier employs a relatively high chopping frequency (1.2MHz). As a result, even after trimming, its input current is still quite high (90pA). Since the architecture of the proposed AZ stabilized buffer ensures that it produces no measurable switching artefacts [4,5], its input switches can be switched at a much lower frequency (f_{AZ} = 15kHz). This, in turn, results in much lower input current (0.2pA) after trimming.

The rest of the paper is organized as follows. Details of the trimming scheme are described in Section II. Measurement results are shown and discussed in Section III, and the paper ends with conclusions.

II. Input Current Trimming Scheme

The input network of the AZ stabilized buffer is shown in Fig. 2. The two main sources of offset are the offset of the buffer V_{os1}, and the offset of the stabilization loop V_{os2}. By appropriately configuring the three input switches, either V_{os1} can be sensed and auto-zeroed by the stabilization loop (phase Φ_1), or V_{os2} can be auto-zeroed by shorting the input of the stabilization loop (phase Φ_2). At the end of Φ_1, the Φ_1 switches turn off, while the Φ_2 switch turns on. As a result, most of the channel charge of the Φ_1 switches (q_1 and q_2) is absorbed by the Φ_2 switch. The charge injection mismatch of the Φ_1 switches, however, will divide equally between V_{in} and V_{out}, resulting in an input current $I = f_{AZ}(q_1\text{-}q_2)/2$.

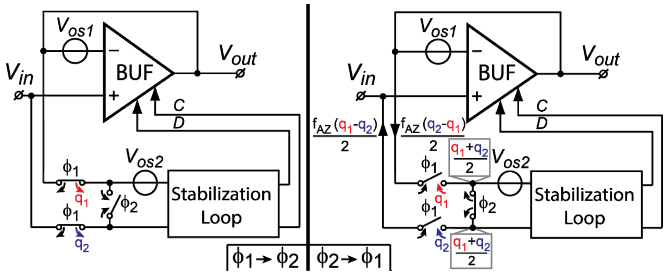

Fig. 2. Input current caused by charge injection mismatch of the AZ switches

In order to absorb this charge injection mismatch, dummy Φ_2 switches can be placed in series with the Φ_1 switches (Fig. 3). In this work, the charge these switches absorb (q_3 & q_4), and hence the input current, is made trimmable by including a circuit that adjusts the amplitude of the clock signals (V_{trim1} and V_{trim2}) applied to their gates.

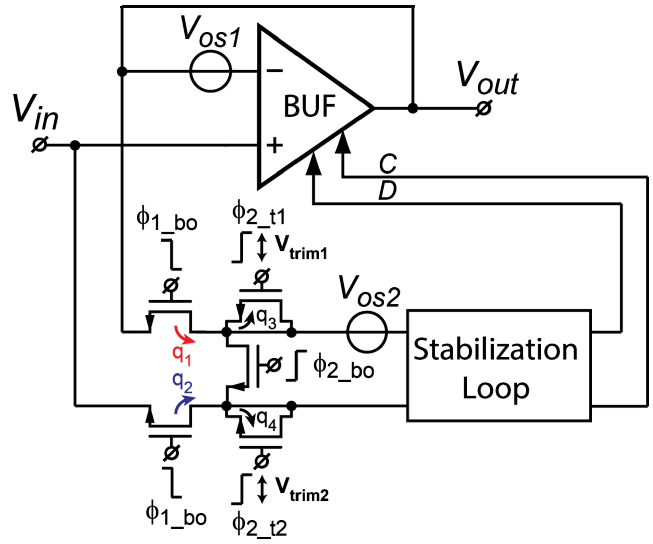

Fig. 3. Input current trimming using dummy switches with trimmed clock amplitudes

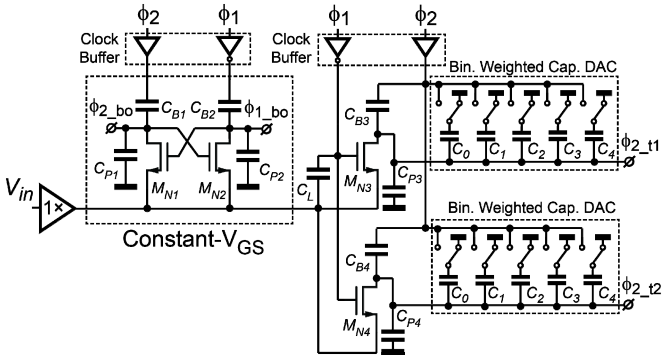

Fig. 4. Constant-V_{GS} drive with the trimming circuit for the clock amplitudes of the dummy switches.

The main switches are driven by capacitively-coupled constant-V_{GS} drive circuits (Fig. 4), which effectively add a fraction of a 1.8V clock signal to a buffered version of V_{in} [5]. The amplitude of the resulting clock signal $\Phi_{1,2\_bo}$ is determined by the ratio of the boosting capacitor ($C_{B1\text{-}B2}$) to the parasitic capacitance to ground ($C_{P1\text{-}P2}$). By adjusting this ratio via a capacitive DAC, a similar circuit can be used to adjust the amplitude of the clock signals $\Phi_{2\_t1,2}$ applied to the dummy switches. The DAC capacitors are always in parallel to either the boosting capacitor or the parasitic capacitor and thus are never floating.

The result is a very linear trimming characteristic, as can be seen from the measured input current vs trimming code (Fig. 5). From previous work [5], the buffer's maximum input current is expected to be less than 1pA, and to vary by about 0.2pA over the buffer's input voltage range. A 4-bit binary weighted DAC with a 0.1pA LSB would then be sufficient to trim the input current. For near-minimum size dummy switches, this LSB corresponds to a 30mV change in clock amplitude, which can be achieved with a 40fF (minimum-size) LSB capacitor and a 1.1pF boosting capacitor. To ensure robustness to process spread, a 5-bit DAC was actually implemented.

To minimize power-supply spikes, the dummy switches are driven by Φ_1 and Φ_2 clock signals provided by a current-mode logic (CML) buffer. From Fig. 4, however, it can be seen that the trim DACs only load the CML buffer's Φ_2 output. To avoid generating asymmetric Φ_1 and Φ_2 clock signals, which would also cause current spikes in the buffered V_{in}, a dummy load capacitor (C_L) is also used on the Φ_1 side. Its value is roughly equal to the trim DAC capacitance at the mid-range DAC code.

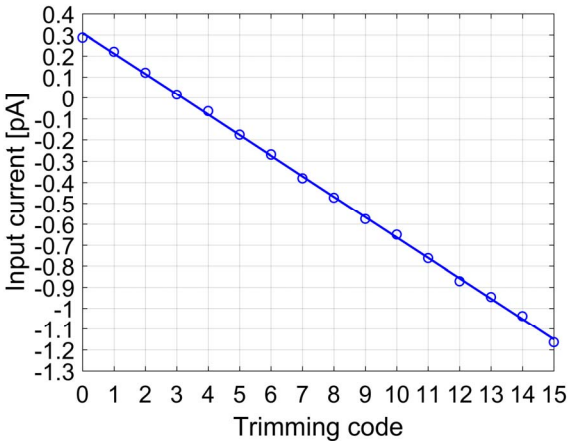

Fig. 5. Measured Input current vs Trimming code (4 bits) for a typical sample

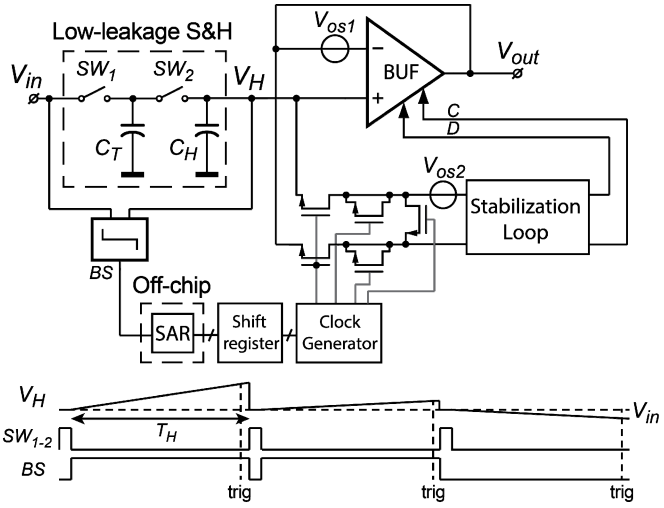

Fig. 6. Automatic input current trimming loop

As in [4,5], the input current can be measured by observing the voltage drift of an on-chip hold capacitor C_H (= 36pF) connected to a S&H circuit. The leakage of the S&H circuit is minimized by using an additional hold capacitors to bootstrap the critical junctions of the sampling switches $SW_{1,2}$. One of these capacitors (C_T = 3pF) ensures that the channel of SW_2 is bootstrapped, minimizing its leakage. In this work, this drift is used as the sensing mechanism of an automated trimming scheme (Fig. 6).

Initially the voltage across C_H is reset by sampling the input voltage V_{in}. After a hold time T_H, a dynamic comparator senses the difference between V_{in} and the voltage on C_H. Its output (BS) then indicates the polarity of the input current. This is fed to off-chip SAR logic, which applies different trial codes to the trim DACs. To ensure that the voltage drift associated with the 0.1pA LSB current is significantly larger than the comparator's offset (< 5mV) and noise, the automatic trimming scheme employs a smaller hold capacitor (1pF) and a hold time (T_H) of 100ms.

III. Measurement Results

The proposed buffer is realized in a 0.18µm CMOS process (Fig. 7). It draws 210µA from a 1.8V supply, and has an active area of 0.55mm^2, 0.12mm^2 of which is occupied by the S&H circuit. Compared to [5], the main change is the addition of the trim DACs, which occupy 0.012 mm^2, i.e. about 2% of the total active area.

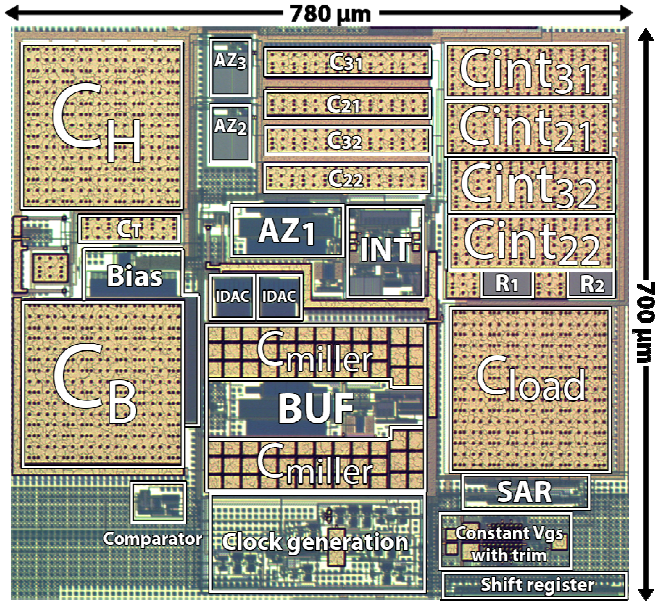

Fig. 7. Chip micrograph of the active area.

The input current of 13 samples was measured over the buffer's full input voltage range (0 to 1.3V). Before trimming, the measured input current is limited to ±1pA (Fig. 8). Trimming the input current manually (Vin = 0.7V), reduces this to ±0.2pA (Fig. 9). Good agreement can be seen between the manually and automatically trimmed samples (Fig. 9), proving the effectiveness of the automatic trimming scheme. This low input current was achieved while also keeping the same low low-frequency noise density (20 nV/√Hz) and offset (< 1µV) as in [5].

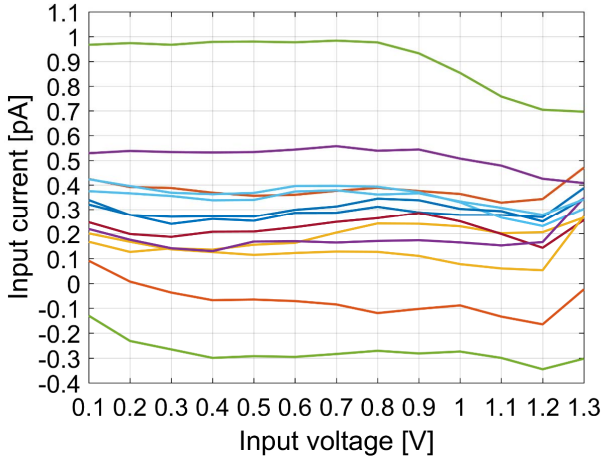

Fig. 8. Measured input current vs input voltage before trimming

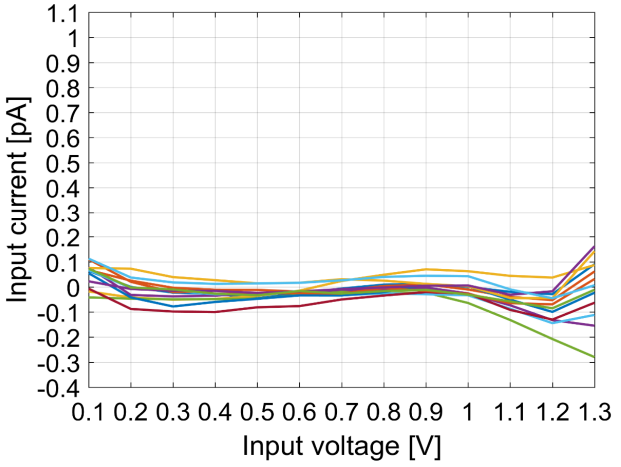

Fig. 9. Measured input current vs input voltage after a manual trim at 0.7V

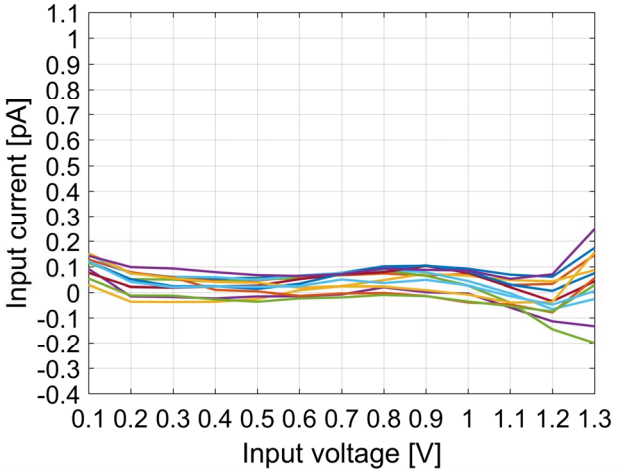

Fig. 10. Measured input current vs input voltage after automatic trimming at 0.7V

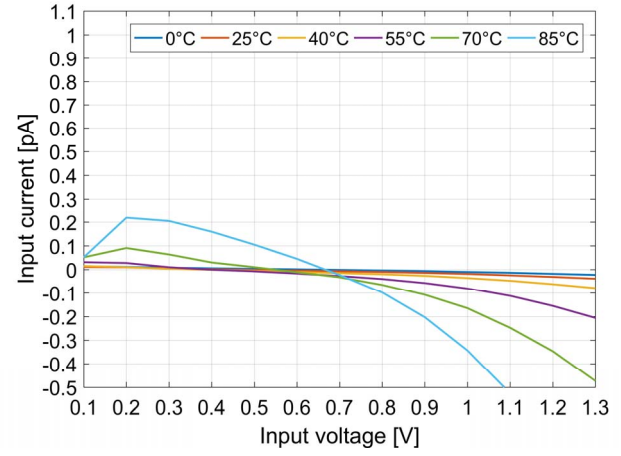

Fig. 11. Measured input current vs input voltage over temperature with auto-zeroing disabled

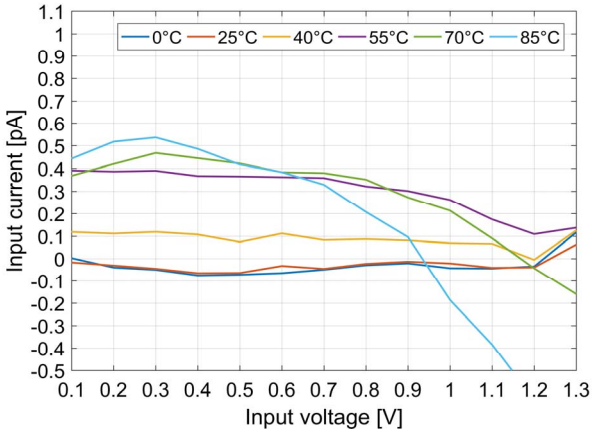

Fig. 12. Input current vs input voltage over temperatures with AZ enabled for a typical sample

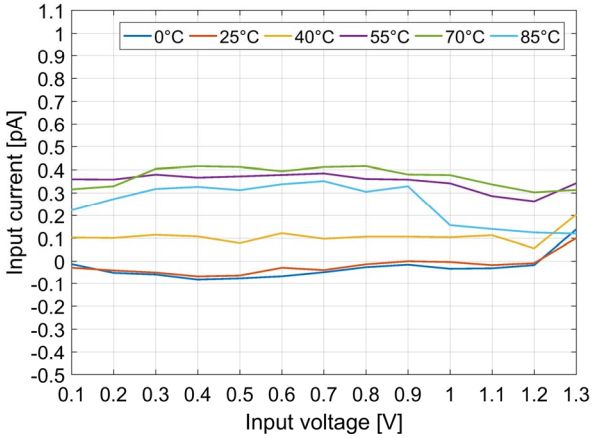

Fig. 13. Input current vs input voltage over temperatures for a typical sample with the S&H leakage subtracted

The input current of a typical sample was also measured over temperature (0 to 85°C). First, AZ was disabled and the input current vs input voltage was observed via the low-leakage S&H (Fig. 11). At higher temperatures, an apparent increase in the measured input current can be seen near the extremes of the buffer's input voltage range, probably because the passive bootstrapping of SW_2 does not perfectly suppress its parasitic junction leakage. With AZ enabled, a similar trend is observed (Fig. 12). To examine the behavior of the charge-injection related input current, the difference between the two measurements was also plotted (Fig. 13). It can be seen that the charge-injection related input current change is quite stable, only drifting by about 0.4pA over temperature. Simulations show that this drift is related to changes in the rise and fall time of the Φ_1 and Φ_2 clock signals, which, in turn, is related to the temperature-dependent bias current of the CML buffers.

In a general purpose application, the inputs of the buffer would be connected to pads, which would be protected by ESD diodes. To investigate the effect of these diodes, their leakage current was measured in a separate experiment. At room temperature, the variation in their leakage current with input voltage exceeds 0.5pA. Since diode leakage increases exponentially at higher temperatures, low-leakage (bootstrapped) ESD diodes will be needed to preserve the low input currents of the proposed amplifier [7].

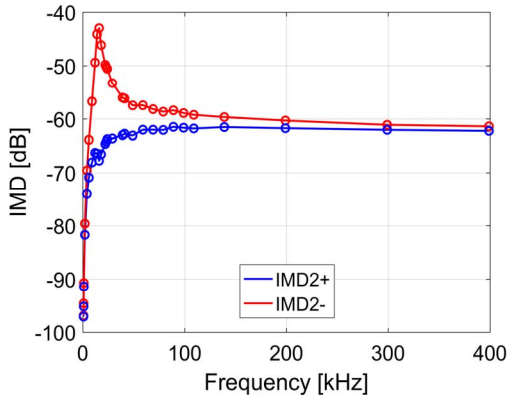

Fig. 14. Measured Intermodulation distortion with varying input frequency for a $100mV_{rms}$ input signal and a typical sample

Another switching artefact observed in auto-zero and chopper amplifiers, especially around their switching frequencies, is intermodulation distortion (IMD). The IMD of the buffer was measured by sweeping the frequency f_{in} of a $100mV_{rms}$ input signal and observing the amplitude of the second order products ($f_{AZ} \pm f_{in}$ & $f_{in} - f_{AZ}$). The second order products above and below f_{in} were measured separately, denoted by IMD2+ and IMD2-, respectively, in Fig. 14. At low frequencies, the IMD2 is about 100dB, but it is only 44dB (IMD2-) around the AZ frequency (15kHz). For even higher frequencies a relatively constant IMD of around 60dB was measured.

IV. Conclusions

An Auto-Zero Stabilized Voltage Buffer with a trimming scheme to minimize its input current is presented. To the authors' knowledge, this is the first time such a trimming scheme has been presented. The scheme operates by trimming the clock swing, and hence the charge injection, of two dummy input switches. Thanks to this scheme, the maximum input current can be lowered from 1pA to 0.2pA, which represents a 4× improvement on the state-of-the art [5], while only requiring 2% of the total area. Over temperature (0 to 85°C) the input current stays below 0.4pA, which is still well below the ESD leakage.

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