Condition Monitoring of MMC Submodule Semiconductors

Jeroen J.C. van Ammers

TU Delft
Delft University of Technology

IEPG Intelligent Electrical Power Grids

Condition Monitoring of MMC Submodule Semiconductors

by

Jeroen J.C. van Ammers

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Thursday August 31, 2023 at 1:00 PM.

Student number:	4818369	
Project duration:	December 1, 2022 – August 31, 2023	
Thesis committee:	Prof. Dr. M. Popov,	TU Delft, responsible professor
	Dr. Ir. A. Lekić,	TU Delft, daily supervisor
	Dr. Ir. M. Ghaffarian,	TU Delft
	Dr. Ir. G. Ye,	TenneT TSO
	Ir. B. Mihić,	TenneT TSO

This thesis is confidential and cannot be made public until August 31, 2024.

TU Delft

Abstract

Submodules are the building blocks for MMC-type HVDC converters and therefore of utmost importance for converter reliability. In order to unlock smarter maintenance strategies for submodule semiconductors, the technical condition of the semiconductors needs to be estimated to form a health index. Besides the non-project-specific traditional health index methods, a complete practical implementable data-driven lifetime estimation approach for individual converters is needed to determine the exact remaining useful lifetime of all submodule semiconductors. The methodologies should finally explore a new research direction in the optimization of the converter lifetime considering maintenance intervals.

This thesis presents a health index methodology applicable to submodule semiconductors in modern MMC-type HVDC converters. The ON-state collector-emitter voltage is used as a condition indicator and external influences are neglected with electrical and thermal models. These models are needed to estimate the junction temperature in the submodule semiconductors due to the temperature-dependent ON-state collector-emitter voltage.

A novel lifetime optimization methodology is presented that determines the submodule that is near its end-of-lifetime and should be replaced in the next maintenance interval. In order to optimize the converter lifetime, the selected submodule is switched more frequently based on a selection window generated from the submodule insertion vector. Switching this submodule more frequently can ensure that it fails exactly at a determined time instant and allows other submodules to be switched less frequently extending their remaining useful lifetime.

Finally, a complete data-driven lifetime estimation methodology has been described that uses available measurements in existing MMC-type HVDC converters. Based on the converter load profile and the semiconductor specifications, estimations are made on the submodule semiconductors' lifetime. Simulations show the significant influence of the DC-current based on different voltage class semiconductors and their limitations considering obtaining the minimum required lifetime.

Preface

During my Master's in Electrical Power Engineering at the Delft University of Technology, I have learned a lot and gained a lot of experience. This thesis marks the end of a very special chapter in my life in which I enjoyed the entire journey. It is challenging to summarize those two years and thereby complete my studies with a single master's thesis.

Before the Master's program started, I was introduced to the world of Electrical Power Engineering and Power System Protection by Prof. Dr. Marjan Popov with invitations to attend several workshops organized by his Power System Protection Centre. This opened a whole new direction of interest in my professional career and with only the basic knowledge I had at this time, I discovered what I wanted most: tackling climate change by assuring a stable and reliable electrical power supply for everyone and for always. This eventually made the decision to apply for the Electrical Power Engineering Master's program from where I chose specialisation courses provided by the Intelligent Electrical Power Grids group. Already in the beginning, the genuine desire of the staff sparked my interest and I followed courses related to Electrical Power System Analysis, Transients in Power Systems, and Power System Protection. These courses given by Prof. Dr. Marjan Popov and his genuine passion for teaching eventually made me decide on the final phase of my Master's program and started the discussions of the thesis that would come later. I am sincerely grateful he took the role of responsible professor. His outstanding support and guidance made the entire following journey amazing.

During the master's thesis research, I was introduced to Dr. Aleksandra Lekić who became my daily supervisor. Her comprehensive knowledge of converters and specialisation in intelligent control of power electronic systems opened new directions in the research and I learned a lot during all conversations we had. Her persistent support, patience, and encouragement have made this research into innovations in nowadays converters. I am sincerely thankful for her unwavering support and guidance leading to these results. From TSO TenneT, I was supervised by Gu Ye. During that time we had many conversations where I enjoyed his constant persistence and guidance on top of the research itself a lot. I learned many things about a wide variety of topics which helped me become a better researcher and understand practical necessities. On top of this, I specifically enjoyed our fruitful discussions and travel together for meetings and the time we spent there.

A significant part of my Master's program was spent learning about technical aspects of the electrical power system that were not directly covered during my personal study program. Already during my Bachelor's degree, I joined TSO TenneT as a part-time trainee next to my regular studies to learn more how to apply the theory taught in university to practice. My personal mentor at TSO TenneT was Bojana Mihić with whom I had many memorable conversations and enjoyed her enormous patience. Bojana was always there when I needed her and helped me define my personal career path such that I eventually stayed at TSO TenneT under her guidance for almost the entire duration of my master's. I am sincerely indebted for her guidance specifically related to personal development.

Another special period during my master's program was my internship in Mannheim where I researched novel techniques for transient testing of HVDC cable systems under the supervision of Dr. Mohamad Ghaffarian Niasar. This marks the excessive variety in my study program where I learned from developing cable test techniques to understanding transient phenomena in power systems to power system protection, and finally condition monitoring of semiconductors in MMC-type HVDC converters. I sincerely thank my family, friends, and people I met during those years for their constant support.

Jeroen J.C. van Ammers
Delft, August 2023

Contents

1 Introduction

The energy transition poses many different challenges to the electrical transmission system. While previously the electrical network was built to connect centrally located generation units to customers, nowadays renewable energy sources are being installed depending on the energy source availability. The energy resource usable for geographic areas depends on the local climate, where e.g. hydro-powered energy is preferred for mountainous areas while photovoltaic plants can be used for a desert landscape. Although many different energy resources are needed to produce constant renewable energy, the distance between those locational preferred energy resources is large. Long-distance bulk energy transport is therefore even more relevant in the future. The technology used is a High-Voltage Direct Current (HVDC) transmission system consisting of two converters and conductors.

This development emphasizes the importance of HVDC transmission systems in the modern energy system as these will form the backbone of the existing Alternating Current (AC) transport system. The reliability of those transmission systems is therefore of utmost importance and should be carefully considered. Unexpected outages of critical nodes in the system can cause large-scale blackouts.

In the last years, Modular-Multilevel Converters (MMC) have replaced line-commutated converters as a preferred technology for transferring renewable energy due to benefits, e.g., fully active and reactive power control, grid forming capabilities, and reduced harmonic distortion.

1.1. Problem Statement

TenneT TSO is a transmission system operator responsible for the Netherlands and a large part of Germany. A remarkable cost difference in maintenance costs is observed by TenneT TSO between onshore- and offshore-located HVDC converters. Maintenance to onshore converters is cheaper because the stations can be accessed more easily compared to budget-wise expensive maintenance offshore converters. These offshore converters are placed on platforms and preferably designed to be operated unmanned to reduce the platform size. Most of the maintenance expenses are due to physical inspections verifying the condition of converter components. Condition monitoring systems can reduce the number of required physical inspections and thus reduce subsequent costs. These systems should be accessible from the mainland - preferably from an office workplace.

TenneT TSO is planning to install at least 14 large-scale offshore MMCs with its 2 GW program and specifications for all condition monitoring systems should be determined before those converters are built. Adjustments to converters (extra sensor installations, data requests) are almost impossible after hand-over. Although previous progress has been made with health estimation and condition monitoring of some converter auxiliary systems, the understanding of the degradation mechanisms of the most critical elements, the submodule semiconductors, is lacking. Condition indicators for these systems should be found whereafter a condition monitoring strategy should be developed.

1.2. Existing Framework

Condition monitoring of the submodule semiconductors in MMC belongs to a wider portfolio of health indexing applied in TSO TenneT. This refers to the estimation of the technical condition of an asset to enable a data-driven maintenance strategy. It has been decided to change the existing time-based maintenance strategy, with fixed time intervals, to a more intelligent condition-based maintenance strategy. Information about the asset, such as its operational conditions and operational lifetime, is used in mathematical formulation to estimate the health of the component. This health is divided into ten levels indicating the condition of an element as shown in Table 1.1.

Table 1.1: Health index applied in TSO TenneT.

Level	Color	Definition
1	Purple	Within 3 years, 80% chance that the component is irreparably damaged
2	Purple	Within 3 years, 50% chance that the component is irreparably damaged
3	Purple	Within 3 years, 20% chance that the component is irreparably damaged
4	Red	Within 7 years, 80% chance that the component is irreparably damaged
5	Red	Within 7 years, 50% chance that the component is irreparably damaged
6	Red	Within 7 years, 20% chance that the component is irreparably damaged
7	Orange	The component is older than 75% of the average lifetime
8	Orange	The component is between 60% and 75% of the average lifetime
9	Green	The component is more than 5 years old and less than 60% of the average lifetime
10	Green	The component is less than 5 years old

The condition indicators for most existing components are their age and failure rate. These are weighted in a mathematical summation producing a number representing its health level. TSO TenneT aims to improve the health framework more intelligently, also taking operational conditions and asset-specific factors into account. This is an important step since none of the components is identical; a circuit breaker frequently switching will experience faster deterioration than a circuit breaker less frequently switching [1].

Although these operational conditions improve the health indexing slightly, taking more indicators into the mathematical summation is still only applicable for components where lots of historical data are available. Technical improvements in components over time can alter the determined average lifetimes and other indicators of similar components already in operation. Discrepancies will occur as the health index will only be applicable for certain versions of specific components.

In particular, this a is major concern for submodule semiconductors applied in MMC. It is observed that none of the HVDC converters in TSO TenneT are identical; different manufacturers and sub-manufacturers are used and technical improvements between the projects are rapid. Sometimes control system software updates during operation already have a significant influence on the failure rate of the submodules. A more intelligent condition monitoring methodology should be studied in parallel to determine the feasibility of project-specific health indexing of submodule semiconductors.

1.3. Scope of the Research

The overall goal of this research is to develop a data-driven health index for MMC submodule semiconductors. This health index shall be used to estimate the remaining lifetime of the semiconductors and improve submodule maintenance and inspection planning. Besides, the condition indicators compatible with the current way of working in the health index framework, the feasibility of a project-specific condition monitoring method for submodule semiconductors shall be studied. The method shall be developed and tested with existing converters if applicable.

Since the developments of MMC and HVDC systems are rapid and difficult to predict, it shall be determined which submodule semiconductors shows the most potential to be used in future projects. Based on this the health indexing can be aimed at the most promising technology making it compatible with futuristic projects that are still under development, but it is preferred that the methodology also works with all existing converters.

These requirements can be briefly elaborated within the following research questions:

1. Which are the failure mechanisms for the most promising submodule semiconductors?
2. What is the most suitable condition indicator to measure the degradation of the submodule semiconductors?
3. How can the technical condition of the submodule semiconductors be estimated with the esteemed condition indicator?
4. How can the lifetime of the submodule semiconductors be prolonged or how to utilize this lifetime more efficiently?

5. How can a project-specific condition monitoring strategy for submodule semiconductors in MMC-type HVDC converters be developed?

1.4. Main Results and Thesis Outline

In this thesis, a new health index for MMC submodule semiconductors is presented. Since required sensors are not installed in existing converters, these can be requested for future projects. A converter control system update is proposed to optimize the maintenance windows. Lastly, a method to calculate the remaining lifetime of all individual MMC submodule semiconductors with existing available data is presented. These outcomes are divided into the following chapters:

Semiconductor Monitoring is the first chapter in which the different HVDC system topologies and submodule configurations in MMC are discussed. The half-bridge submodule configuration is selected after comparison with the full-bridge submodule configuration. This is followed by a thorough analysis of different semiconductors and their housings. Failure modes and observations during degradation are carefully outlined. A condition monitoring methodology is presented where it is shown that the ON-state collector-emitter voltage should be measured. An estimation model for this condition indicator is presented such that external influences are excluded.

Semiconductor Power Losses continues from the condition indicator estimation model to minimize external influences. The first step is to estimate the average power losses in the IGBT and Free-Wheeling Diode (FWD) semiconductors. For the IGBT switching losses, a comparison is made between a linear and non-linear approximation, where the latter is difficult to estimate from available data in practice. It is shown that the component losses of conventional IGBTs in half-bridge configurated submodules are different in the rectifier- and inverter mode. For Reverse Conducting (RC) IGBT devices], these losses are more homogeneous for both operation modes.

Converter Thermodynamics is the last step in the condition indicator estimation model to minimize external influences. The junction temperature steady-state temperature and its fluctuation over the half-wave AC-cycle is estimated. The steady-state value is explicitly modelled from the heat-sink coolant inlet temperature since the coolant temperature is measured at specific locations in real converters. It is shown that bypass FWD experiences the highest overall junction temperature fluctuation, meaning it degrades fastest without modifications in the gate-driver circuits or over-dimensioning.

Lifetime Optimization outlines a novel MMC inner-control methodology to optimize maintenance interval utilization. Conventional presented MMC inner-controllers only ensure capacitor voltage balance while this novel controller also switches the least-healthy submodule more frequently such that it breaks exactly when the maintenance interval starts. As a result, other submodules are switched less frequently and therefore have a prolonged remaining useful lifetime.

Reliability Centered Maintenance is the last part where a method is presented to estimate the remaining useful lifetime of all semiconductors in an MMC with available measurements provided by real converters. The model is finally tested on an actual converter where historical data was available. It is shown that currently, the submodule semiconductors are not the critical element in the converter considering the designed lifetime.

2
Semiconductor Monitoring

As discussed in Chapter 1, the first step of this research is defining the current state-of-the-art for MMC and HVDC systems. A condition indicator to estimate the health of submodule semiconductors in MMC should be found applicable for the most promising semiconductor.

This chapter first discusses the HVDC system configurations applied in practice. After this, the MMC and its characteristics are outlined in more detail followed by a comparison between the most utilised submodule topologies, the half-bridge and full-bridge circuits. The semiconductors used in these circuits are compared whereafter the three different housings together with their failure mechanisms and observations are thoroughly analyzed. Finally, the most suitable condition indicator is determined and an estimation methodology is presented.

2.1. Converter Station Topologies

Different HVDC system configurations have been used in practice. These can be categorized into monopolar and bipolar configurations. Both systems are further explained in the following sections.

2.1.1. Monopolar configuration

The monopolar configuration has only one converter unit between the DC terminals and the converter-transformer. Only one high-voltage insulated conductor is needed as the earth surface or a low-voltage insulated neutral conductor can be used for the return path. A low voltage insulated conductor is usually more cost-effective compared to a high voltage insulated conductor because the latter weighs significantly in the total transmission system costs [2]. A disadvantage of this configuration is the loss of a single system element requires the system to be shut down because there is only one converter unit. The current return path distinguishes the system into a symmetrical monopole or an asymmetrical monopole.

Symmetrical Monopole A symmetrical monopole has a metallic neutral return low-voltage insulated conductor. The neutral return conductor operates on zero potential which makes its design more straightforward. The system thus has two conductors insulated for the complete DC voltage with its converter-transformer connected to the mid-point between the positive and neutral DC conductor. There is no DC voltage stress on the converter-transformer and this allows therefore more flexibility in the step-up transformer design.

Assymmetrical monopole Contrary to the symmetrical monopole, only one conductor, rated to the full DC potential, is required for an asymmetrical monopolar system. The return path consists of the earth's surface and is connected to the converters with big electrodes. However, the current through the physical ground gives often complications with existing infrastructure and environmental constraints such as the maximum permissible ground current and the eco-system. This monopolar system configuration is therefore not a preferred option in practice [3].

2.1.2. Bipolar Configuration

A parallel connection of two monopolar systems results in a bipolar HVDC transmission system configuration. It has two converter units between the two DC high-voltage insulated conductors and the converter transformer. One DC conductor is rated for positive polarity while the other is negative polarity. In case a converter unit or DC conductor is disrupted, the system is still able to transport a

significant part of the rated power, depending on factors such as the designed overload capacity [3]. Since both conductors must be rated for the full DC potential, and the cable costs are a significant part of the total transmission system costs, a bipolar configuration is more expensive compared to a monopolar configuration [4].

A return conductor connected between the converter units can be used in case the system is unbalanced. This classifies the configuration into a symmetrical or asymmetrical system.

Symmetrical bipolar The symmetrical bipolar configuration has a return conductor between the positive and negative DC terminals. This return conductor can be either the physical ground or a metallic return conductor and is normally grounded at one end of the transmission system [5].

Assymmetrical bipolar An asymmetrical bipolar configuration does not have a current return path and has a disadvantage when the loads are unbalanced. The two poles do not operate in a balanced mode [5].

2.2. Modular Multilevel Converter

Each converter unit consists of six arms connected to the three phases of the AC system. The upper arms connect the highest DC potential terminal to the phases while the lower arms connect the lowest DC potential terminal to the phases. The arms have DC storage capacitors in series which can be switched in or bypassed between the AC phase and DC terminal such that a desired waveform can be generated. A modular multi-level converter consists of many submodules with DC storage capacitors and semiconductor switches that can be controlled individually to create a smoother AC voltage waveform over the submodules. This results in less harmonic distortion and allows for the use of lower switching frequencies reducing the switching losses [6]. Other advantages of modular multi-level converters are [7]:

- The modularity assures easy scalability in the design process.
- Each submodule offers a simple structure reducing manufacturing costs.
- The output voltage and current ripple are very low due to the many switching devices in series, this also reduces the total harmonic distortion.
- The high number of series modules allows for many steps thus a lower submodule switching frequency can be used.
- Extra submodules can be placed in series to increase redundancy when some submodules fail.

2.2.1. Submodule topology

Commonly used submodule configurations are the half-bridge and full-bridge topology [8]. These are further outlined in the following paragraphs.

Half-bridge The half-bridge configuration has two semiconductor switches and one DC storage capacitor for temporary energy storage. The semiconductors can be switched in conducting ON-state $S_x = 1$ or blocking OFF-state $S_x = 0$ using a control signal generated in two gate-driving modules integrated into each submodule. An anti-parallel diode prevents damage in the reverse blocking direction during DC-system faults and can conduct during reverse conducting conditions. If e.g. the arm current is negative ($i_{\mathrm{xy}} < 0$), the submodule can be bypassed with the anti-parallel diode.

Each submodule semiconductor should be operated such that the voltage over the capacitor remains constant at the desired value. Both semiconductors are operated in a contrary manner such that the capacitor can not be short-circuited; if *S1* is switched in ON-state, *S2* is switched in OFF-state. When *S1* is in ON-state for duration τ, the capacitor conducts AC-current $\mathrm{i_{xy}}$ and the DC-storage capacitor voltage $\mathrm{V_c}$ rises,

$$V_c\left(t+\tau\right) = \frac{1}{C}\int_t^{t+\tau} i_{xy}\left(t\right) S_1 dt + V_c\left(t\right), \tag{2.1}$$

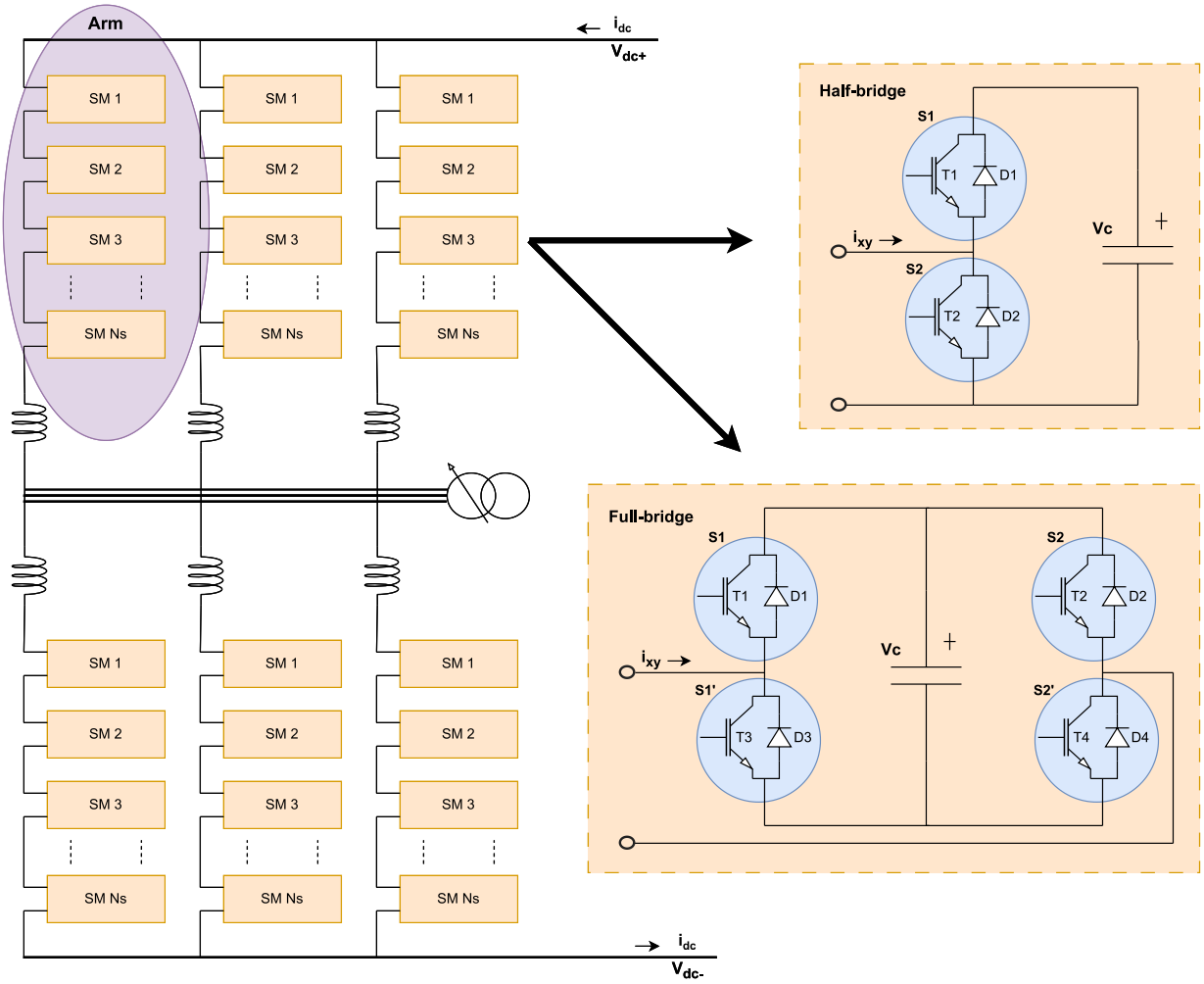


Figure 2.1: Overview of an MMC with two different submodule configurations depicted. The half-bridge submodule has two switches and the full-bridge submodule has four switches.

under the condition i_{xy} is positive (entering the top terminal in Figure 2.1) while V_c decreases if i_{xy} is negative and the submodule is enabled (*S1* in ON-state).

This configuration can produce two different submodule voltages, acting as a two-level converter. Depending on the AC current i_{xy} direction to the capacitor positive terminal, the submodule voltage thus subsequently charges or discharges. The effect of the possible switching states and current direction in half-bridge submodules is summarized in Table 2.1.

Table 2.1: Switching states of the half-bridge submodule [8].

Switching State	S_1	S_2	V_{SM}	$i_{xy}>0$	$i_{xy}<0$
1	1	0	V_c	$V_c \uparrow$	$V_c \downarrow$
2	0	1	0	$V_c \approx$	$V_c \approx$

$\uparrow$ = Increasing, $\approx$ = No change, $\downarrow$ = Decreasing

Full bridge The full-bridge submodule configuration has four semiconductors composed of two parallel half-bridge legs. A capacitor between these legs serves for temporary energy storage. Each semiconductor has anti-parallel diodes to generate the desired voltage during both AC-current i_{xy} directions, meaning the submodule can be bypassed and inserted. Both switches in the legs are operated in a complementary manner such that the capacitor cannot be short-circuited. This implies if the top

switch in a leg is in ON-state ($S_x = 1$), the bottom switch in this leg shall be in OFF-state ($S_x = 0$) where the latter is referred to as $\overline{S_x}$. The voltage over the submodule capacitor can be written,

$$V_c\left(t+\tau\right) = \frac{1}{C}\int_t^{t+\tau}\left(S_1\overline{S_2} - \overline{S_1}S_2\right) i_{xy}\left(t\right) dt + V_c\left(t\right), \tag{2.2}$$

as a function of these switching states and AC-current i_{xy}. If both are in the complementary state, the capacitor will charge or discharge depending on which switch is enabled and the direction of i_{xy}.

Using the complementary operation of both switches in the legs with S_x representing the upper switch and $\overline{S_x}$ the lower switch makes it a three-level converter. An additional blocking mode is possible where all four switches are switched to OFF-state ($S_x = 0, \overline{S_x} = 0$) which can be used to suppress DC-fault currents with a negative i_{xy}. The possible submodule output voltages are shown in Table 2.2.

Table 2.2: Switching states of the full-bridge submodule.

Switching state	S_1	$\overline{S_1}$	S_2	$\overline{S_2}$	V_{SM}	$i_{xy}>0$	$i_{xy}<0$
1	1	0	1	0	0	$V_c \approx$	$V_c \approx$
2	1	0	0	1	V_c	$V_c \uparrow$	$V_c \downarrow$
3	0	1	1	0	$-V_c$	$V_c \downarrow$	$V_c \uparrow$
4	0	1	0	1	0	$V_c \approx$	$V_c \approx$
BM	0	0	0	0	$-V_c$	N/A	$V_c \downarrow$

$\uparrow$ = Increasing, $\approx$ = No change, $\downarrow$ = Decreasing
BM = Blocking mode

Comparison The differences between half-bridge and full-bridge submodule configurations should be studied to determine the most suitable configuration for future MMC projects. While the half-bridge configuration operates as a two-quadrant converter, the full-bridge operates as a four-quadrant converter and is able to generate a negative submodule voltage. This is particularly useful in the case of temporary DC-faults, by inserting a series of negative voltages in between the AC-system voltage and the faulted DC terminal, the fault impedance approaches zero such that the current stops flowing. After DC-fault removal, the converter can resume nominal operation by inserting the submodules in a normal way. This DC-fault blocking capability is a significant advantage from full-bridge submodules to half-bridge submodules. A comparison between all metrics is shown in Table 2.3.

Table 2.3: Comparison between the two submodule configurations in MMC used in practice. The major performance metrics are mentioned [8].

Metric	Half-bridge SM	Full-bridge SM
Output voltage levels	2	3
Max. blocking voltage	V_c	V_c
IGBT devices	2	4
DC capacitors	1	1
Power losses	Low	Moderate
DC fault suppression	No	Yes

While the blocking voltage capability is similar for both submodule configurations, the semiconductor power losses are higher for full-bridge submodules. This is because the currents pass two semiconductors compared to a single semiconductor in half-bridge configured submodules. On top of this, double the amount of semiconductors is needed for the full-bridge submodules which increases the converter capital expenditures.

The half-bridge submodule is nowadays most suitable for offshore applications according to Siemens Energy [9]. The higher reliability due to the reduced amount of semiconductors compared to the full-bridge submodule is essential for remote locations. The full-bridge configuration is primarily used for HVDC systems comprising overhead lines as the fault can be cleared by shortly reversing the line polarity thus di-ionizing the arc. As the Multi-Terminal HVDC grids are emerging, these already comprise

HVDC circuit breakers which makes full-bridge configuration not necessary. This thesis will focus on the half-bridge configured submodules because of the aforementioned reasons.

2.3. Semiconductor Study

A voltage source converter requires submodule semiconductors that are able to both conduct ($S_x = 1$) the arm current and block ($S_x = 0$) the DC-storage capacitor voltage as controlled by the applied gate-signal send by the two submodule control modules. These fully-controllable semiconductors are nowadays in rapid development. The developments and state-of-the-art are briefly summarized in the following paragraphs.

Gate Turn-off Thyristor The Gate Turn-Off Thyristor (GTO) is a three-terminal semiconductor device and has been developed in the 1970s [10]. The device can be turned on with a small current pulse while for turning it off, a large negative current pulse is required. A disadvantage of GTOs is their large turn-off time limiting the use of high switching frequencies in the modules to 1 kHz. Higher turn-off times also lead to an increase in switching losses. Moreover, a switching stress reduction network is needed to decrease dv/dt and di/dt transients and is implemented in the form of a snubber.

As improvement to the GTO, the Integrated Gate-Commutated Thyristor (IGCT) was developed. An IGCT has its gate integrated next to the thyristor minimizing the parasitic gate inductance [11]. This reduces undesired induced gate currents and increases the withstand rate of voltage rise (dv/dt) thus omitting the need for a gate snubber network. The homogeneous switching across the semiconductor chip area reduces the switching losses compared to a GTO.

Insulated Gate Bipolar Transistor The IGBT is widely used in the industry for voltage source converters and in particular for MMC-type converters. The device is a combination of a bipolar junction transistor and a field effect transistor, combining the advantages of both devices. This gives the device a high input impedance at the control gate thus neglecting the need for a high power supply [10]. Whereas the high switching speed from the field effect transistor allows the usage of high switching frequencies in the IGBT. The bipolar transistor structure further marks withstanding capability against high voltages and currents. An IGBT device structure allows for easy semiconductor chip paralleling to increase the current rating of the device.

A promising development is a Reverse-Conducting IGBT (RC-IGBT) developed by Hitachi Energy [12]. This variant has its anti-parallel diode semiconductor chips merged together with the IGBT semiconductor chips and shows smoother switching waveforms and reduced losses. This device is expected to be used in future projects. This thesis will focus on the conventional IGBT and the RC-IGBT variant for the aforementioned advantages and the future outlook.

2.4. Device Structure

The IGBT and FWD semiconductor chips can be positioned in parallel to increase the submodule current rating. Stacking devices in series chains increases the voltage withstand capability. The amount of devices in series and parallel is a trade-off between reliability and costs. Stacking many chips in series increases the module voltage withstand capability such that the submodule can operate with a higher voltage. This will reduce the number of needed submodules to reach the arm voltage and significantly reduces the converter capital expenditures. On the other hand, the more semiconductor chips are stacked in series, the higher the impact of a single failed semiconductor chip; if a single semiconductor in the chain fails, the whole submodule will be out of service.

There are three semiconductor housing structures used in the industry. These are the wire-bonded, rigid press-pack, and compliant press-pack structures. Their properties are further explained below together with their degradation mechanisms [13].

2.4.1. Wire-bonded device

The IGBT semiconductor chips are soldered on directly bonded copper substrates and connected to the case terminals by wire bonds. Silicon gel is applied to keep the bond wires in place and improve heat dissipation from the bond wires to the case. The device is cooled from the base plate as cooling from the top side is not possible due to the placement of the terminals. Wire-bonded devices are older

and have the disadvantage that they fall into an open-circuit failure mode. This means that a whole series chain of modules is out of operation in case of failure. A cross-section view of a wire-bonded IGBT device is shown in Figure 2.2.

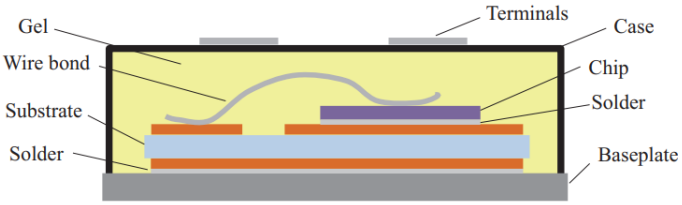


Figure 2.2: Side-view of a wire bonded housing structure for IGBT and anti-parallel diode semiconductor chips [13].

The main failure mechanisms for wire-bonded devices are bond-wire degradation and solder layer degradation [14], [15]. These failure mechanisms are further discussed below together with the physical process during the degradation till device failure.

Bond-wire degradation Bond-wire degradation can be categorized into complete bond-wire lift-off and bond-wire heel cracks. When the semiconductor chip heats up during operation, it will expand according to the Coefficient of Thermal Expansion (CTE). As the aluminum bond wires have a different CTE than the semiconductor chips, the interface between the bond wire and the semiconductor chips experiences mechanical stress. This results in small cracks and after many repetitions eventually lead to a bond wire cut off or heal crack. The electrical resistance of the semiconductor chips will increase and further result in more heat dissipation in the semiconductor chips. This will increase the semiconductor chip temperature and the IGBT ON-state collector-emitter voltage.

An experiment was performed on a $1200\,\mathrm{V}/\ 50\,\mathrm{A}$ bond-wire IGBT module by Chen et al. including two IGBT semiconductor chips and two anti-parallel diode semiconductor chips [16]. The chips were connected by four bond wires, connected to the chips each in two locations subsequently. The total collector-emitter voltage drop was determined to be over the IGBT chip and package materials. These package materials are further divided into terminal resistance, copper layer resistance (between terminal and bond-wire), bond wire resistance, and chip solder layer resistance (below Chip in Figure 2.2). This proves the ON-state collector-emitter voltage drop incline in case the bond wire resistance increases as a result of degradation. To mimic the bond-wire degradation, different cuts were made in the bond-wires. The ON-state collector-emitter voltage of the healthy module was measured to be $2164\,\mathrm{mV}$, while it increased to $2172\,\mathrm{mV}$ after one bond wire was cut resulting in one connection left for this bond wire. The ON-state collector-emitter voltage increased to $2201\,\mathrm{mV}$ after this bond-wire was completely cut-off, and increased further to $2213\,\mathrm{mV}$ after the second bond-wire was also partially cut, and finally to $2249\,\mathrm{mV}$ after all four bond-wire feet were cut off. The bond-wire electrical resistance increased subsequently from $1.37\,\mathrm{m\Omega}$ for the healthy module, to $1.49\,\mathrm{m\Omega}$ after the first cut, to $1.87\,\mathrm{m\Omega}$ after the second cut, and $2.01\,\mathrm{m\Omega}$ after the third cut and $2.49\,\mathrm{m\Omega}$ after the last cut.

Solder layer degradation The expansion due to the difference in material CTE parameters results in an increase in heat dissipation. With the solder layer being the most crucial part in the heat conduction path, it is the layer dominantly to degradation as a result of thermal cycling. Cracks will start to form in this layer and reduce the heat dissipation capability further. This will lead to a positive feedback process and eventually to the device's failure. There are two solder layers, where the solder layer between direct copper bonded and baseplate is the most prone to failure due to the higher CTE mismatch compared to the layer between the silicon IGBT chip and direct copper bonded substrate [15].

The study performed by Jia et al. revealed that the solder layer degradation mechanism of bond-wire IGBTs modules is similar for press-pack IGBTs [17]. It is common that an $5\,\%$ increase in on-state collector-emitter voltage and a junction thermal resistance increase of $20\,\%$ indicate solder-layer degradation [18].

2.4.2. Rigid press-pack device

A rigid press-pack device uses contact pressure technology to connect the rigid electrodes with the IGBT semiconductor chips. Electrode pillars are used for mechanical support and are typically made of annealed copper with high elastic properties. The housing is hermetically sealed and made from ceramic material [13]. Pressure is applied externally from the top and bottom side by clamps.

The rigid press-pack devices were developed to improve the open-circuit failure mode. If one of the IGBT chips fails, a conductive intermetallic consisting of aluminum from adjacent components is formed, creating a short circuit. In case a press-pack IGBT fails, it falls into a short-circuit failure mode due to the contact pressure on the device's top and bottom. An additional submodule bypass switch is not needed with this failure-mode property. Another advantage of the structure is the possibility of applying cooling plates both on top and at the bottom of the device.

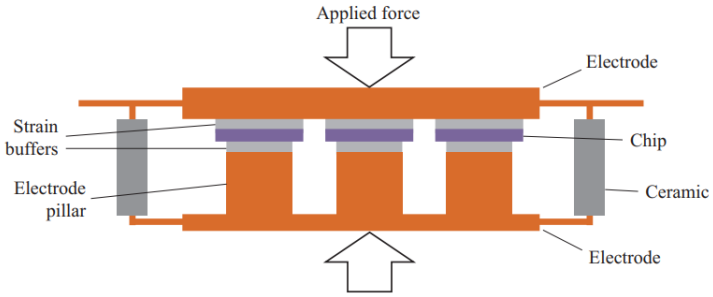


Figure 2.3: Side-view of a rigid press pack device [13].

During manufacturing, it is almost impossible to have all element dimensions inside the rigid-press pack device exactly equal. A small difference in the semiconductor chip size or electrode pillar height contributes to pressure non-uniformity. The external clamping pressure non-ideality adds to this effect and results in some IGBT chips suspected to have higher clamping pressure and thus take more current during ON-state. This will eventually result in device degradation. The exact degradation mechanisms are assumed to be similar to compliant press-pack devices (both are press-pack devices) and are summarized in the following section.

2.4.3. Compliant press-pack device

As development to the rigid press-pack devices, compliant devices are made of non-hermetic plastic housing and have disc springs with higher elastic properties compared to electrode pillars inside the package [13]. This improves the pressure distribution more evenly over the semiconductor chips and thus has a better current density rating per IGBT chip and is less susceptible to overpressure on the semiconductor chips in the centre of the module. External clamping pressure is also applied but is limited. Those disc springs are bigger in size compared to the electrode pillars used in rigid press-pack devices, which makes the available area for the IGBT chips smaller thus limiting the package's total current conduction capability. The devices are single-sided cooled at the bottom plate due to the spring connection between top plate and IGBT chip.

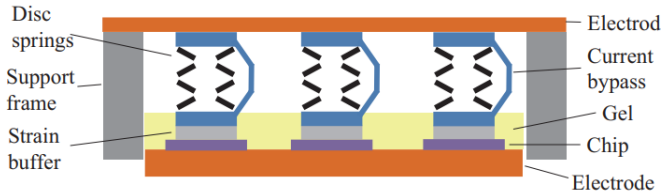


Figure 2.4: Side-view of a compliant press pack device [13].

Four degradation mechanisms for press-pack packages are described in more detail. These are fretting wear degradation, gate-oxide degradation, spring degradation, and lid warping degradation [19].

Fretting wear degradation Fretting wear degradation is the dominant degradation mechanism of press-pack devices and is caused by the difference in CTE in the package materials similar to the main degradation mechanism for wire-bonded devices. However, for press-pack devices, the contact surfaces between the layers will undergo fretting wear. During power cycling, the internal pressure will fluctuate which stresses the internal package layers and is amplified specifically for rigid press-pack devices due to the decreased elastic properties of the electrode pillars compared to the disc springs used in compliant press-pack devices. This pressure cycling eventually leads to increased contact layer roughness and thus a higher electrical and thermal contact resistance. The higher thermal contact resistance will reduce the package's cooling ability and causes the junction temperature to increase. This process could eventually lead to thermal runaway of the module.

Jia et al. studied a 1200 V/ 50 A rigid press-pack IGBT module with two IGBT semiconductor chips and two FWD semiconductor chips configured as half-bridge [17]. The chips are welded on a directly bonded copper layer through die-attach solder layers, further welded to a copper baseplate. It is noted that a 20 % increase in junction-to-case thermal resistance and 5 % increase in collector-emitter voltage usually indicates thermal failure due to solder degradation. The experiment showed that the collector-emitter voltage increased by 4.42 % while the junction-to-case thermal resistance increased by roughly 31 %.

Huang et al. modeled and did practical accelerated ageing experiments with six IGBT modules rated 1700 V/ 3600 A [20]. Solder cracks were observed in the die-attach layer in between the semiconductor chip and the directly bonded copper layer during power cycling. While one IGBT chip observed an 33 % increase in junction-to-case thermal resistance, the other only experienced an 15 % increase. The observed incline in ON-state collector-emitter voltage was respectively 1.8 % and 2 %.

The effect of fretting damage on a single IGBT chip has less effect on the complete module ON-state collector-emitter voltage compared to the voltage of the single IGBT chip ON-state collector-emitter voltage due to the parallel structure. This could explain the variations found by the different researchers and emphasizes the accuracy requirements.

Gate-oxide degradation Besides fretting damage, gate-oxide degradation is another major failure mechanism for press-pack IGBT devices. Due to the extrusion of the emitter layer under cyclic stress, the oxide layer between the gate and the emitter will start deteriorating. This reduces the gate-emitter electrical resistance causing a leakage current to flow from the gate to the emitter. This process continues till the gate is not able to supply the current resulting in a gate-emitter voltage decline. The conductive channel between the gate and emitter will narrow as a result which further increases the on-state voltage between the collector and emitter. Eventually, this overstress will result in device failure.

Tinschert et al. did practical experiments with 4.5 kV/ 1600 A press-pack IGBT devices [21]. These devices consisted of many individual IGBT chips and contained anti-parallel diode chips. Eight of the ten tested devices failed because of gate-oxide degradation and micro arcing during power cycling tests. Multiple parameter observations were made during the degradation process and moment of failure. First, a sudden step in ON-state collector-emitter saturation voltage was measured of roughly 4 % for a device while multiple steps were observed for another device of varying magnitude (same order as the first device) with the last step roughly 30 %. Secondly, a significant increase of gate-emitter current was observed and a decrease of gate-emitter resistance to 80–500 kΩ was seen. Lastly, a reduced blocking capability was measured where the devices were not able to block the rated voltage anymore. It was noted that the reduction of gate-emitter resistance will increase the collector-emitter saturation voltage in all parallel chips inside a module.

Another experiment was performed by Liu et al. in which three 3300 V/ 50 A press-pack IGBTs were exposed to power cycling tests [22]. It was observed that the gate surface changed from smooth and flat before the test, to rough after the test. Also, the gate-emitter resistances drastically decreased and leakage current increased during the degradation process pointing to the gate-oxide degradation mechanism. The devices' gate-emitter resistances were measured 1000 MΩ before the test. After failure, the first device measured a device gate-emitter resistance of $8.7\,\Omega$, second $314.6\,\Omega$, and third 6.9 kΩ. During the process of degradation, the collector-emitter voltage increased in many small steps to approximately 30 % at the moment of failure, where a high incline of 67–97 % in collector-emitter voltage was observed as the gate driver was not able to supply the required leakage current and the increase of gate resistance.

Spring degradation Each IGBT semiconductor chip in press-pack IGBT devices has its gate terminal connected to one of the module gate driver modules by a special spring construction. This construction consists of a pin head, pin tube, and a spring where the spring is most susceptible to degradation. Spring fatigue leads to an increased electric contact resistance between gate terminal and gate driver module thus increasing the power losses and the temperature at the IGBT chip gate. This temperature incline results in a higher gate-emitter leakage current [23]. The contact resistance can increase in the range of 10^2 to 10^3 times the initial contact resistance [19]. The higher gate resistance affects the IGBT switching: the switching time will be longer resulting in higher switching losses and thus a temperature increase while the higher resistance damps the ringing: smaller collector-emitter voltage gradients and collector current gradients will be observed. The larger switching time will further increase the switching losses of the device. The switching performance degradation of a single IGBT semiconductor chip has little effect on the performance of the whole multi-chip device.

Lid warping degradation The applied external clamping pressure should be extremely uniform for both press-pack device categories. This holds also for the internal pressure from the springs for compliant press-pack devices. Multi-chip IGBT modules experience lid-warping degradation due to the temperature gradient inside the module during thermal cycling. This temperature gradient is caused by the heat conduction parameter that differs horizontally from the inner side of the module to the outer side. Thermal expansion, therefore, is more significant for the IGBT chips on the inner side compared to the outer side. This leads to a reduced contact surface and increased electrical contact resistance for the semiconductor chips on the outer side, thus a reduced current through the outer semiconductor chips and an increased current through the inner semiconductor chips is experienced. The thermal resistance for the outer modules will incline as a result of the reduced contact area, which causes a temperature increase in those semiconductor chips if the power dissipation in those chips decreases slower than the thermal resistance increases.

A practical experiment together with simulations was performed by Lai et al. on two press-pack IGBTs rated 3300 V/ 1500 A [24]. Each device consisted of 30 IGBT chips and 14 FWD chips. All FWD chips were placed around the square IGBT chip configuration, resulting in 4 IGBT chips positioned in the corners. By applying an unbalanced external clamping force, lid warping degradation was mimicked and the expected physical processes were observed. The junction temperature difference between cells in the centre and the outer ring was measured to be 23 degC with an outer chip surface roughness of 1.27 µm with the inner chips being colder. Using finite-element-modelling, a current difference of 15.6 A ampere was measured between inner IGBT chips and the 4 corner IGBT chips, with the inner chips conducting 58.1 A and outer chips conducting 42.5 A. An accelerated-aging experiment showed a temperature difference after 6060 cycles of 53.6 degC between inner and outer chips with the inner semiconductor chips being colder. The conduction current density difference was 20.8 A, with inner conducting 58.9 A and outer conducting 38.1 A. It was observed that the main chip degradation mechanism is sliding between chips, which refers to fretting wear damage. However, the main degradation mechanism is different, it was shown that lid warping degradation significantly contributes to the complete degradation, and because of this, the centre chips are more prone to fretting wear damage as those withstand higher temperature cycling stress. This process was also observed by Tinschert et al. with a test performed on 4.5 kV/ 1600 A multi-chip press-pack IGBTs but referred to as arcing failure mechanism [21]. The assessed degradation mechanism was identical and therefore in this research categorized as lid-warping degradation. A temperature difference of roughly 35 degC was determined from a comparative simulation between inner and outer chips, where the outer chip layer was warmer.

2.5. Monitoring Methodology

It was shown that several degradation mechanisms are observed in the literature. While only wire-bonded devices suffer from bond-wire degradation, all of them suffer from solder layer degradation. Besides this, both the press-pack devices additionally endure fretting wear degradation, gate-oxide degradation, spring degradation, and lid-warping degradation. These damage processes affect several device parameters which need to be studied to select a suitable condition indicator for condition monitoring. This condition indicator should be used to assess the health of the different IGBT devices used in practice and is further discussed in the following sections.

2.5.1. Parameter selection

Observed parameter fluctuations due to the discussed degradation mechanisms were experimentally verified by several researchers. Bond-wire degradation mainly results in a change of ON-state collector-emitter voltage and a semiconductor chip junction temperature increase. This phenomenon was similar for solder layer degradation in both press-pack device types. The dominant fretting-wear degradation in press-pack devices mainly causes a semiconductor junction temperature increase. This further affected the ON-state collector-emitter voltage to incline. Gate-oxide degradation was determined to have its main effect on the device switching behaviour: turn-on time and gate-emitter resistance are mainly altered but also an increase in ON-state collector-emitter voltage can be measured.

The press-pack device failure modes spring degradation and lid warping degradation were not primarily related to ON-state collector-emitter voltage increase. While spring degradation mainly affects the switching behaviour and so the device temperature, the increase in ON-state collector-emitter voltage is only a secondary consequence. Lid warping degradation was determined as a side-effect of other degradation mechanisms such as fretting wear. Lid warping degradation was shown to affect the individual semiconductor chip junction temperatures and currents in multi-chip devices.

Since the most dominant failure modes affect the ON-state collector-emitter voltage, this is the most suitable parameter to monitor. Another reason is that from an operational perspective, it is only important to know the condition of the device and its remaining lifetime, whereas the exact degradation mechanism is irrelevant as IGBT devices can only be replaced per device and not per internal semiconductor chip due to their complex and tight structure.

2.5.2. External influence

With the condition indicator determined to be the ON-state collector-emitter voltage, external influences on this condition indicator need to be studied. It is important that deviations in measurements are solely due to device degradation. First, the theoretical equation will be given followed by a practical approach using available parameters. Lastly, a methodology is presented to exclude external influences on the selected condition indicator. The ON-state collector-emitter voltage $V_{ce,on}$ can be written according to the device geometry and characteristics. In general, this involves many parameters [25],

$$V_{ce,on} = \frac{2k_B T}{q} \ln\left[\frac{J_c W_n}{4qD_a n_i F\left(\frac{W_N}{2L_a}\right)}\right] + \frac{\rho L_{CH} J_{CH}}{\mu_{ni} C_{ox}\left(V_G - V_{TH}\right)}, \tag{2.3}$$

where k_b is the Boltzmann constant, T the junction temperature, W_N width of the N+ region, J_c collector-current density, n_i intrinsic carrier concentration, D_a ambipolar diffusion coefficient, L_a ambipolar diffusion length, L_{ch} ambipolar diffusion length, C_{ox} channel length, ρ indicated cell pitch, V_G applied gate voltage, V_{th} the gate threshold voltage, and μ_{ni} the inverse layer mobility [26].

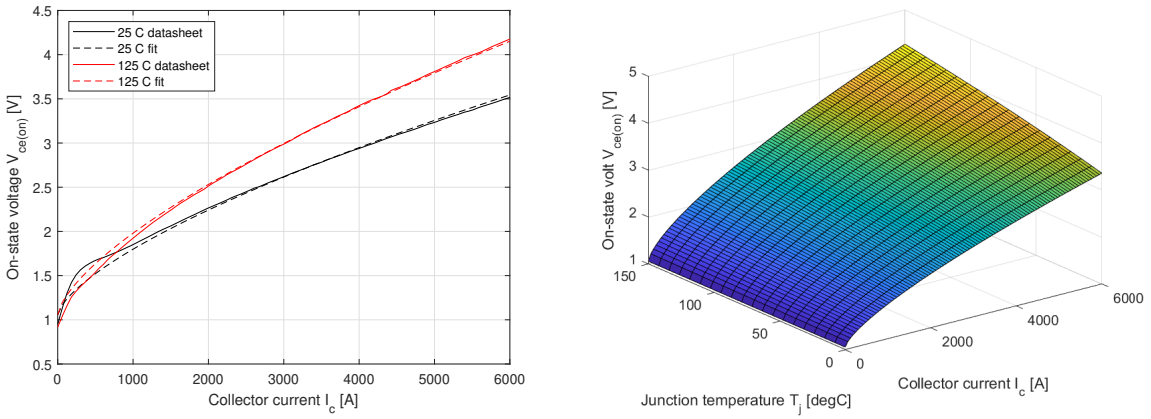
It is obvious that $V_{ce,on}$ depends on many parameters subject to the IGBT design which are prone to intellectual property. In order to establish a generalized mathematical methodology for IGBT condition assessment that is manufacturer-independent, it is needed to eliminate all operational independent device design parameters. Although datasheets usually show $V_{ce,on}$ against i_c curves for two or three junction temperatures, a continuous temperature range is needed for operational independent condition assessment. Using unknown parameter vector $x = [x_1\ x_2\ x_3\ x_4]$, curve fitting on

$$V_{ce,on} = x_1 \times I_c^{x_2} \times log_{10}\left(x_3 \times T\right) + x_4, \tag{2.4}$$

has shown to be accurate to obtain the current dependency with extrapolation to a continuous temperature range. The results as shown in Figure 2.5 are obtained for the Hitachi Energy *5SJA 3000L520300* RC-IGBT device.

These datasets can be used as references representing a healthy device. During operation, i_c and T_j should be obtained and the measured $V_{ce,on}$ can be compared to the device reference dataset. If deviation to ranges specified in section 2.4 are recognized, the device undergoes degradation and the deviations between different IGBTs in an MMC can be compared to estimate the relative health.

The advantage of using this methodology is that only a junction temperature estimation is needed instead of accurate computation. The junction temperature estimation methodology is explained in the following section.



(a) Model validation using the two given temperatures.

(b) Model over the continuous temperature range.

Figure 2.5: Extracted reference model for a healthy *5SJA 3000L520300* RC-IGBT module with a continuous junction temperature T_j range based on the datasheet with two given temperatures.

2.6. Estimation Model

Obviously, the junction temperature in all submodule semiconductors in an MMC should be estimated during condition monitoring. If a measured $V_{ce,on}$ is compared to its reference value both should be computed at the same junction temperature T_j and collector current i_c. Since the arm current, if a semiconductor switch is enabled ($S_x = 1$) equal to the collector current, can be easily measured, the focus will be on the junction temperature estimation. The junction temperature is a result of semiconductor power losses which are dissipated into heat [27]. This causes a temperature drop over the semiconductor housing between the chip and the module case. These power losses should be estimated based on the submodule arm-current i_{xy} and the device characteristics. The semiconductor housing's absolute temperature is affected by the cooling system: the more heat energy is removed from the module case, the lower the junction temperature will be. The cooling system thermodynamic performance is therefore the last step in the junction temperature determination process.

The complete methodology for junction temperature T_j estimation in all submodule semiconductors is presented in Figure 2.6.

The estimation methodology is divided into two chapters, each focusing on a different aspect of the methodology.

Semiconductor power losses describes the power loss estimation in each semiconductor. These losses depend on the current through each semiconductor device and its loss characteristics. Since the current through each semiconductor is not measured, this should be estimated from the converter's set points. The focus in this chapter has been on set points that are available in higher levels of the converter control system, implying that the methodology can be used in real projects.

Converter thermodynamics specifies the semiconductor junction temperature estimation as a result of the semiconductor power losses. The steady-state temperature and a ripple due to the half-wave AC cycles are examined. The steady-state value depends on the heat-sink performance connected to the submodule semiconductor. As there are only temperature sensors at each converter tower, the heat-sink temperatures have to be estimated. The focus here is on a general methodology where the cooling system configuration can be different.

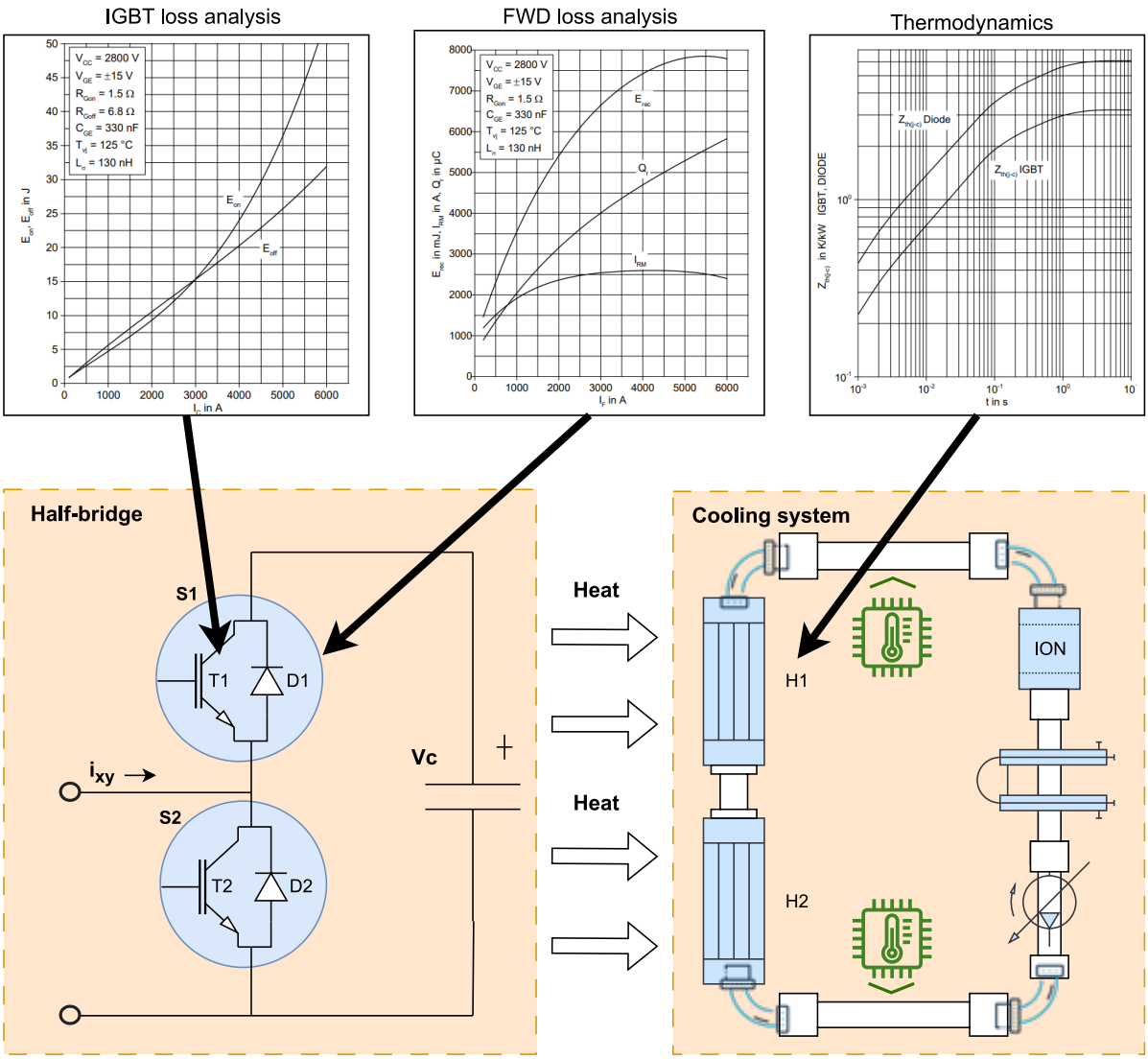


Figure 2.6: Methodology to estimate the junction temperature of each submodule semiconductor.

3
Semiconductor Power Losses

In this chapter, the power losses in all submodule semiconductors are estimated. These power losses depend on the device's current and the device's loss characteristics. Since there are no current sensors installed directly to the semiconductors, the estimation is based on higher level parameters that are widely available in converter control systems such as the DC-pole current. Analysis is performed between a linear- and non-linear computation of the switching losses, where the feasibility of obtaining necessary parameters with real components is assessed. This is particularly useful to assure a general estimation process applicable to different converter vendors and semiconductor manufacturers. Finally, the semiconductor power losses in half-bridge submodules are compared for a converter operating in rectifier mode and a converter operating in inverter mode where the differences are discussed.

3.1. Submodule Analysis

The first step in the power loss estimation process is the computation of the current through each submodule semiconductor. Average and RMS currents through each semiconductors in half-bridge configuration can be calculated using the operational conditions of the converter, also referred to as mission profile in literature [28], [29]. A symmetrical monopolar system is assumed for the analysis for simplicity. The results can be easily adjusted for a symmetrical bipolar system under steady-state operation. Here, the DC-pole voltage will be half of the value for a symmetrical bipolar system. With the three AC phases being symmetrical, only one of them has been used (v_a, i_a). First, the voltage and current for a single phase in the AC system can be written as:

$$\begin{aligned} v_a\left(t\right) =& E_m \sin\left(\omega_n t\right) \\ i_a\left(t\right) =& I_m \sin\left(\omega_n t + \theta\right) \end{aligned} \tag{3.1}$$

with E_m and I_m representing the respective amplitude. Supposing inverter operation, where the DC current I_{dc} flows into the positive terminal of the upper arm and out of the negative terminal of the lower arm, the currents through the upper arm i_{au} and lower arm i_{ial},

$$\begin{aligned} i_{au}\left(t\right) =& \frac{I_{dc}}{3} + \frac{i_a\left(t\right)}{2} \\ i_{al}\left(t\right) =& \frac{I_{dc}}{3} - \frac{i_a\left(t\right)}{2}, \end{aligned} \tag{3.2}$$

both contain a DC- and an AC component. By substituting $i_a\left(t\right)$ from (3.1) into (3.5) and using current ratio $k = 3I_m/2I_{dc}$, the arm currents can we written as function of variables ω_n, θ, and I_{dc},

$$\begin{aligned} i_{au}\left(t\right) &= \left[1 + k \sin\left(\omega_n t + \theta\right)\right] \frac{I_{dc}}{3} \\ i_{al}\left(t\right) &= \left[1 - k \sin\left(\omega_n t + \theta\right)\right] \frac{I_{dc}}{3}, \end{aligned} \tag{3.3}$$

which can be measured at the converter terminals and assures the methodology can be applied in practice since these are widely available in converter control systems. In order to generate a sinusoidal waveform on the AC side from constant DC voltage, the arm voltages should be sinusoidal with the upper and lower arm voltages 180 out of phase. These upper $u_{au}\left(t\right)$ and lower arm $u_{al}\left(t\right)$ voltages,

$$\begin{aligned} u_{au}\left(t\right) =& \frac{U_{dc}}{2} - v_a\left(t\right) \\ u_{al}\left(t\right) =& \frac{U_{dc}}{2} + v_a\left(t\right), \end{aligned} \tag{3.4}$$

also contain a DC- and AC component but are perpendicular to the respective arm-current AC component. Assuming that the number of submodules per arm is sufficient to neglect non-fundamental harmonics in the sinusoidal waveforms, $v_{\mathsf{a}}(t)$ from (3.1) can be substituted into (3.5), and by using modulation index $m = 2E_m/U_{dc}$, the arm voltages can be rewritten to:

$$\begin{aligned} u_{au}(t) &= [1 - m\sin(\omega_n t)]\frac{U_{dc}}{2} \\ u_{al}(t) &= [1 + m\sin(\omega_n t)]\frac{U_{dc}}{2} \end{aligned} \tag{3.5}$$

In order to generate a sinusoidal arm voltage, half-bridge submodules can be enabled giving $V_{\mathsf{SM}} = V_{\mathsf{c}}$ or bypassed resulting in $V_{\mathsf{SM}} = 0$. The number of modules enabled in the upper arm $n_{\mathsf{au}}(t)$ and lower arm $n_{\mathsf{al}}(t)$ depends on the sinusoidal arm voltage amplitudes $u_{\mathsf{au}}(t)$ and $u_{\mathsf{al}}(t)$,

$$\begin{aligned} n_{au}(t) &= \frac{u_{au}(t)}{U_c} = n[1 - m\sin(\omega_n t)] \\ n_{al}(t) &= \frac{u_{al}(t)}{U_c} = n[1 + m\sin(\omega_n t)], \end{aligned} \tag{3.6}$$

and can further be written as a function of the number of submodules $2n$ in an arm. This number should be large enough to neglect non-fundamental harmonics in the arm voltages and rounded to an integer value. Multiple submodule insertion strategies exist so that an expression for the current through an individual submodule is complex. Under the reasonable assumption that all submodules are inserted evenly over time, the probability of an enabled submodule $p_{\mathsf{au}}(t)$ in the upper arm and $p_{\mathsf{al}}(t)$ in the lower arm can be calculated with the average number of submodules enabled in an arm $n_{\mathsf{au}}(t)$, $n_{\mathsf{al}}(t)$ and the total number of modules in this arm $2n$,

$$\begin{aligned} p_{au}(t) &= \frac{n_{au}(t)}{2n} = \frac{1 - m\sin(\omega_n t)}{2} \\ p_{al}(t) &= \frac{n_{al}(t)}{2n} = \frac{1 + m\sin(\omega_n t)}{2}, \end{aligned} \tag{3.7}$$

which can be seen as depending on the modulation index m and AC-system angular frequency ω_n. From the energy conservation relationship neglecting the losses in MMC,

$$\frac{U_{dc}I_{dc}}{3} = \frac{I_m E_m \cos(\theta)}{2}, \tag{3.8}$$

which describes the power balance between the AC- and DC-side of the converter and modulation index, it is possible to write current-ratio k,

$$k = \frac{2}{m\cos(\theta)}, \tag{3.9}$$

from the converter set points available in the control system. Each semiconductor (IGBT or FWD) in a half-bridge configuration conducts in a half-wave AC period depending on the AC-current direction and the submodule voltage state V_{SM} (enabled or bypassed). When the submodule is bypassed, T_2 is conducting when $i_{xy} > 0$ while D_2 conducts when $i_{xy} < 0$. The other semiconductors (T_1 and D_1) follow a similar methodology depending on the submodule insertion state and AC-current i_{xy} direction. Trigonometric formulae can be used to solve the arm current zero crossings $i_{au}(t) = 0$ and $i_{al}(t) = 0$ from (3.3). If the converter operates in inverter mode, the arm-current zero crossings are calculated using,

$$\begin{aligned} \omega_n t_1 &= -\theta - \arcsin\frac{1}{k} \\ \omega_n t_2 &= -\theta + \pi + \arcsin\frac{1}{k}, \end{aligned} \tag{3.10}$$

while in the same operational mode these arm-current zero crossings are in the lower arm:

$$\begin{aligned} \omega_n t_1 &= -\theta + \arcsin\frac{1}{k} \\ \omega_n t_2 &= -\theta + \pi - \arcsin\frac{1}{k} \end{aligned} \tag{3.11}$$

If the converter operates in rectifier mode, these zero-crosings in the upper-arm are,

$$\begin{aligned}\omega_n t_1 &= -\theta + \arcsin\frac{1}{k}\\ \omega_n t_2 &= -\theta + \pi - \arcsin\frac{1}{k},\end{aligned} \tag{3.12}$$

while in the lower arm these are computed using:

$$\begin{aligned}\omega_n t_1 &= -\theta - \arcsin\frac{1}{k}\\ \omega_n t_2 &= -\theta + \pi + \arcsin\frac{1}{k}\end{aligned} \tag{3.13}$$

The resulting average and RMS-squared currents can be calculated by multiplying the current through the module (3.3) with the semiconductor conduction probability (3.7) and integrating over the time-period determined previously. In this example only the inverter operation and the upper arm is elaborated since the other modes can be computed using the same methodology. The average current through each submodule semiconductor can be computed here:

$$\begin{aligned}I_{T1,av} &= \frac{1}{2\pi}\int_{\omega_n t_2}^{\omega_n t_1+2\pi}\frac{I_{dc}}{3}\left[1+k\sin\left(\omega_n t+\theta\right)\right]\frac{1-m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\\ I_{T2,av} &= \frac{1}{2\pi}\int_{\omega_n t_1}^{\omega_n t_2}\frac{I_{dc}}{3}\left[1+k\sin\left(\omega_n t+\theta\right)\right]\frac{1+m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\\ I_{D1,av} &= \frac{1}{2\pi}\int_{\omega_n t_1}^{\omega_n t_2}\frac{I_{dc}}{3}\left[1+k\sin\left(\omega_n t+\theta\right)\right]\frac{1-m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\\ I_{D2,av} &= \frac{1}{2\pi}\int_{\omega_n t_2}^{\omega_n t_1+2\pi}\frac{I_{dc}}{3}\left[1+k\sin\left(\omega_n t+\theta\right)\right]\frac{1+m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\end{aligned} \tag{3.14}$$

While finally the RMS-squared current through each submodule semiconductor can be computed using:

$$\begin{aligned}I^2_{T1,rms} &= \frac{1}{2\pi}\int_{\omega_n t_2}^{\omega_n t_1+2\pi}\frac{I^2_{dc}}{9}\left[1+k\sin\left(\omega_n t+\theta\right)\right]^2\frac{1-m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\\ I^2_{T2,rms} &= \frac{1}{2\pi}\int_{\omega_n t_1}^{\omega_n t_2}\frac{I^2_{dc}}{9}\left[1+k\sin\left(\omega_n t+\theta\right)\right]^2\frac{1+m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\\ I^2_{D1,rms} &= \frac{1}{2\pi}\int_{\omega_n t_1}^{\omega_n t_2}\frac{I^2_{dc}}{9}\left[1+k\sin\left(\omega_n t+\theta\right)\right]^2\frac{1-m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\\ I^2_{D2,rms} &= \frac{1}{2\pi}\int_{\omega_n t_2}^{\omega_n t_1+2\pi}\frac{I^2_{dc}}{9}\left[1+k\sin\left(\omega_n t+\theta\right)\right]^2\frac{1+m\sin\left(\omega_n t\right)}{2}\,d\omega_n t\end{aligned} \tag{3.15}$$

3.2. Device Losses

With the average and RMS-squared currents determined through each submodule semiconductor, the power losses can be calculated. These power losses are dissipated into heat and propagate from the semiconductor chip junctions to the device case. There are four types of power losses in IGBT and FWD semiconductors:

- Conduction losses: During ON-state, both IGBT and FWD semiconductors dissipate power due to a small voltage drop over the non-ideal devices causing conduction losses.
- Blocking losses: In OFF-state, both IGBT and FWD semiconductors suffer from a small leakage current through the devices which causes blocking losses.
- Switching losses: During the transition between both states, the IGBT experiences switching losses as a result of a non-ideal transition.
- Reverse recovery losses: When switching from ON-state to OFF-state, the FWD experiences reverse recovery losses as a result of a non-ideal transition.

Because of the very-short on-time (time duration of the transition from OFF-state to ON-state) and the very small FWD reverse blocking current, the turn-on losses, as of switching from OFF-state to ON-state, and blocking losses for the FWD can be neglected [30]. Similarly, the blocking losses for the IGBT are very small such that these can also be neglected. For both devices, the drive losses (from the gate signal) have been excluded since this does not directly affect the junction temperature. Besides, these losses can be neglected due to their low contribution to the total losses [30]. The computation for the conduction losses, switching losses, and reverse-recovery (FWD switching) losses is further explained in the following sections.

3.2.1. Conduction losses

The conduction losses for IGBT and FWD semiconductors are caused by a small voltage drop over the devices during the device ON-state. This voltage drop is represented by the non-linear voltage-current characteristics. This dependency can be approximated using first-, second-, or higher-order polynomials. For an *5SNA 1200G450300* Hitachi Energy IGBT device it was shown that a first-order polynomial approximation is sufficient to match real datasheet curves [31], while in section 2.5.2 a different order approximation with temperature dependency was used for the *5SJA 3000L520300* Hitachi Energy RC-IGBT module. For a first-order approximation, the IGBT ON-state collector-emitter voltage $V_{ce,on}$ and the FWD forward voltage V_F can be written as:

$$\begin{aligned} V_{ce,on} &= V_{ce,on,0} + R_c i_c \\ V_F &= V_{F,0} + R_F i_F \end{aligned} \tag{3.16}$$

with $V_{ce,on,0}$ and $V_{F,0}$ representing the conduction state zero-current forward voltage drop of the respective semiconductor, while R_c and R_F are the conduction state resistances. The temperature dependency of these resistances is neglected in this first-order approximation. The instantaneous power dissipation equals the convolution of current and voltage while the average conduction power loss for the IGBT and FWD semiconductors during one AC fundamental frequency cycle,

$$P_{\text{c,T/D}} = \frac{1}{2\pi} \int_0^{2\pi} V_{ce,on,0} i_c + R_c i_c^2 \, d\omega t, \tag{3.17}$$

is calculated by the multiplication of (3.16) with the collector-current i_c. The resulting average conduction losses for the IGBT and FWD semiconductors (device *x*) is therefore:

$$P_{c,T/D} = |I_{av,x}| \, V_{0,x} + R_{0,x} I_{rms,x}^2 \tag{3.18}$$

with $I_{av,x}$ representing the average current through the device, $V_{0,x}$ the forward device voltage, $R_{0,x}$ the conduction state resistance, and $I_{rms,x}$ the RMS current through the device.

3.2.2. Switching losses

An IGBT semiconductor suffers from switching losses when the device switches between the conduction ($S_x = 1$) and blocking state ($S_x = 0$) due to a non-ideal transition; voltage over the device and current through the device do not change instantly.

Switching process A general illustration of the voltage and current of an IGBT device during switching from OFF-state to ON-state is shown in Figure 3.1

The analytical evaluation of the switching process is adopted from Tu et al. in [33]. An IGBT operates in its cut-off region when it is in a blocking state. In order to switch the IGBT to a conduction state, a positive voltage V_{GG} is applied to the gate, with respect to the emitter. This voltage charges non-linear parasitic gate-collector C_{gc} (Miller) and gate-emitter C_{ge} capacitances, seen in parallel from the gate as C_{ies} and rises until it reaches gate-threshold voltage V_{th}. Under the assumption that the impedance effect from the parasitic gate inductance L_g is much smaller compared to the gate resistance R_g, the gate-emitter voltage rise,

$$V_{ge}(t) = (V_{g,0} - V_M) \, e^{\frac{-t}{R_g C_{ies}}}, \tag{3.19}$$

is exponential and depends on the gate resistance R_g, C_{ies}, and the Miller plateau voltage V_M. When V_{th} has been reached, the MOS channel has been built, and collector current I_c starts to flow. At first,

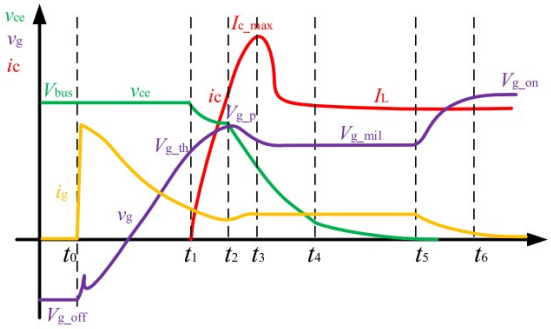


Figure 3.1: IGBT voltage and current during switching from OFF-state to ON-state [32].

V_{ce} is much bigger than V_{ge} such that the MOS channel is saturated and the IGBT operates in the active region. The collector current rise can be expressed as the time-derivative of the current in the active region,

$$\begin{aligned} I_c &= K\left(V_{ge} - V_{th}\right)^2 \\ \frac{di_c}{dt} &= 2K\left(V_{ge} - V_{th}\right)\frac{dV_{ge}}{dt}, \end{aligned} \tag{3.20}$$

with *K* representing the specific transconductance depending on the device geometry and electrophysical parameters. The current flowing through the gate thus charges C_{ies}. This current can be expressed as,

$$I_g = C_{ies}\frac{dV_{ge}}{dt} = \frac{V_{GG} - V_{ge}}{R_g}, \tag{3.21}$$

and results in a voltage drop (V_{GG} - V_{ge}) over the gate-resistor R_g. Substituting dV_{ge}/dt from (3.21) into (3.20) gives the expression of the collector current rise when V_{th} has been reached,

$$\frac{di_c}{dt} = \frac{2K\left(V_{ge} - V_{th}\right)\left(V_{GG} - V_{ge}\right)}{R_g C_{ies}} \tag{3.22}$$

indicating that the rise of collector-current depends on the applied gate-voltage V_{GG} resulting in gate-emitter voltage V_{ge}, V_{th}, R_g, and C_{ies}. The lower the gate resistance, the higher the rise in collector current, thus the faster the IGBT turns on. Meanwhile, V_{ce} has a slight drop as a result of this rising I_c through the stray series inductance L_s:

$$\Delta V_{ce,1} = L_s\frac{di_c}{dt} \tag{3.23}$$

The energy loss in this turn-on region can be approximated using,

$$E_{on,1} = \int_{t_1}^{t_3}\left(V_{ce} - \Delta V_{ce}\right)i_c dt \tag{3.24}$$

and thus significantly depends on the gate-resistor R_g and parasitic capacitance C_{ies}.

With the FWD parallel to the IGBT, implying (I_L = I_c + I_d), a rise in collector-current results in a similar decline in forward diode current for inductive current switching. This means the FWD turns off with $di_F/dt = -di_c/dt$ and enters reverse recovery with a reverse peak current of I_{rr}. The reverse-recovery charge,

$$Q_r = \frac{I_{rr}\left(t_a + t_b\right)}{2} = \frac{I_{rr}t_a\left(1 + S\right)}{2}, \tag{3.25}$$

is the average loss between reaching the reverse-recovery peak current at time t_a and leaving the reverse-recovery region after time t_b. Snappiness factor ($S = t_b/t_a$) is defined as the ratio between these time instants. A higher Snappiness factor means the total reverse-recovery time (t_a + t_b) is longer such that the diode has more time to leave the reverse-conducting region and gradient stress

on the device is lower. As di_F/dt is assumed constant, the reverse-current peak amplitude I_{rr} can be approximated at t_a,

$$I_{rr} = t_a \frac{di_F}{dt} = \sqrt{\frac{2}{1+S} Q_r \frac{di_F}{dt}}, \tag{3.26}$$

and further be written as a function of Snappiness factor S, Q_r, and di_F/dt by the substitution of t_a from (3.25). Here it is seen that a high Snappiness factor will result in a lower I_{rr} for a constant reverse-recovery charge while this effect is contrary to di_F/dt. Since di_F/dt is equal to $-di_c/dt$, the speed is also highly affected by the IGBT gate resistance and C_{ies}.

Meanwhile, the IGBT still operates in the active region. If the collector-current overshoot is low, the gate-emitter voltage can be approximated as nearly constant. The incline of collector-emitter voltage,

$$\frac{dv_{ce}}{dt} = \frac{d}{dt}\left(v_{cg} + v_{ge}\right) \approx \frac{dv_{cg}}{dt} = \frac{i_g}{C_{gc}} = \frac{V_{GG} - V_{GE}}{R_g C_{ies}} \tag{3.27}$$

now can be simplified depending solely on the gate-collector voltage gradient [34]. As this decrease is due to the charging of C_{gc} with the gate-current, it can be simplified by the current through the gate resistance. This is again due to the voltage drop ($V_{GG} - V_{ge}$) over this resistance. Obviously, the rate-of-change of voltage depends highly on the gate-resistor and C_{ies}. The decline in collector-emitter voltage in this period equals,

$$\Delta V_{ce,2} = t_b \frac{dv_{ce}}{dt}, \tag{3.28}$$

and can be used in order to approximate the total energy loss for the FWD for entering a reverse-conduction region [34]:

$$E_{rec} = \frac{S \Delta V_{ce,2} Q_r}{3\left(1+S\right)} \tag{3.29}$$

Similarly, the energy loss for the IGBT in this period can be written [34]:

$$E_{on,2} = \left(\left(V_{DC} - \Delta V_{ce,1}\right) \left(I_L + \frac{I_{RR}}{2} \right) - t_b \frac{dV_{ce}}{dt} \frac{3I_L + I_{RR}}{6} \right) t_b \tag{3.30}$$

After the IGBT reaches its peak overshoot current, it decreases to the constant load current represented by I_L. The gate-emitter voltage is clamped at the Miller-plateau V_M. The increase of non-linear capacitance C_{ge} as a result of the declining collector-emitter voltage causes the gradient to decrease,

$$\frac{dv_{ce}}{dt} = -\frac{V_{GG} - V_M}{R_g C_{ies}}, \tag{3.31}$$

such that the final IGBT losses in this region can be approximated:

$$E_{on,3} = \frac{V_{DC} - \Delta V_{ce,1} - \Delta V_{ce,2} - V_{ce,on}}{2\frac{dv_{ce}}{dt}} \tag{3.32}$$

as defined by the voltage where the IGBT is considered in ON-state $V_{ce,on}$. The total losses for turning the IGBT on can now be computed by summing all losses in the different regions:

$$E_{on} = E_{on,1} + E_{on,2} + E_{on,3} \tag{3.33}$$

Similarly, the turn-off losses can be derived. This procedure is similar and can be computed using the reverse of the described process. However, during IGBT semiconductor switching from ON-state to OFF-state, the overshoot is in the collector-emitter voltage instead of the collector-current. This emphasizes the lower reverse-recovery losses in the parallel FWD.

Practical approach Device datasheets generally indicate E_{on}, E_{off}, and E_{rec} measurements for a single reference blocking voltage and a continuous operating current range. Required parameters to estimate the switching losses completely analytically, with the previously described process, are not provided. The analytical description of the switching losses however can be used to understand effects from reference measurement changes; such as the gate-resistor R_g.

According to [29], [35], [36], and [37], the average switching losses can be obtained by multiplying the loss of one switching action with the switching frequency. Here, the losses of a switching action are scaled linearly from the datasheet measurement reference voltage $v_{ref,T/D}$ and reference current $i_{ref,T/D}$ to the current and blocking voltage in the converter application:

$$\begin{aligned} P_{sw} &= (E_{on} + E_{off}) \frac{v_{cx} \left| i_{Tx,av} \right| f_{sw}}{v_{ref,T} i_{ref,T}} \\ P_{rec} &= E_{rec} \frac{v_{cx} \left| i_{Dx,av} \right| f_{sw}}{v_{ref,D} i_{ref,D}} \end{aligned} \tag{3.34}$$

However, in [38] a different approximation was used. Here, it was mentioned that these losses have a non-linear correlation with the blocking voltage for transistor switching losses and non-linear scaling for both current and voltage for reverse recovery losses. Also, a temperature scaling factor $c_{T,sw}$ $c_{T,rr}$ to the reference temperature condition should be taken into account:

$$\begin{aligned} P_{sw,I} &= f_{sw} \left(E_{on} + E_{off} \right) \frac{\sqrt{2}}{\pi} \frac{i_c}{i_{c,ref}} \left(\frac{v_{dc}}{v_{ref}} \right)^{K_v} \times \left(1 + c_{T,sw} \left(T_{j,T} - T_{j,T,ref} \right) \right) \\ P_{sw,D} &= f_{sw} E_{rr} \left(\frac{\sqrt{2}}{\pi} \frac{i_f}{i_{ref}} \right)^{K_i} \left(\frac{v_f}{v} \right)^{K_v} \times \left(1 + c_{T,rr} \left(T_{j,D} - T_{j,D,ref} \right) \right) \end{aligned} \tag{3.35}$$

Next to the single-term non-linear scaling factors, in [39] the current loss-term in $P_{sw,T}$ and in [40] both $P_{sw,T}$ and $P_{sw,D}$ from (3.35) were approximated using a second order polynomial of the collector-current:

$$\begin{aligned} \frac{i_c}{i_{c,ref}} &= a_0 + a_1 i_c + a_2 i_c^2 \\ \left(\frac{\sqrt{2}}{\pi} \frac{i_f}{i_{ref}} \right)^{K_i} &= b_0 + b_1 i_c + b_2 i_c^2 \end{aligned} \tag{3.36}$$

This is almost similar since all coefficients can be obtained using curve-fitting in both methods. According to SEMIKRON [41], the single-term scaling factors can be approximated for IGBT and FWD semiconductors with the parameters depicted in Table 3.1.

Table 3.1: Approximated scaling parameters for non-linear losses according to [41].

Semiconductor	K_v	K_i	$C_{T,sw}$ [K^{-1}]
IGBT	1.3–1.4	1.0	0.003
FWD	0.60	0.60	0.006

To develop a generalized mathematical methodology for semiconductor health assessment it is important that the power loss estimations hold for general IGBT devices and this should be verified.

Analysis Analysis has been performed on the E_{on}, E_{off}, and E_{rec} measurements from the Hitachi Energy *5SNA 3000K452300* and *5SJA 3000L520300* IGBT devices. The first device has separate IGBT and FWD semiconductor chips, representing a conventional IGBT device, whereas the latter has its IGBT and FWD semiconductors integrated into the same chip, being an RC-IGBT. Using different IGBT technologies indicates if the approximations for the switching losses including the reverse-recovery losses are IGBT technology independent as assessed on conventional used IGBTs and RC-IGBT devices. On top of that, the assessment of Hitachi Energy devices with SEMIKRON parameters indicates the applicability between two different vendors of the factors given in Table 3.1. The subsequent IGBT-device specifications are shown in Table 3.2.

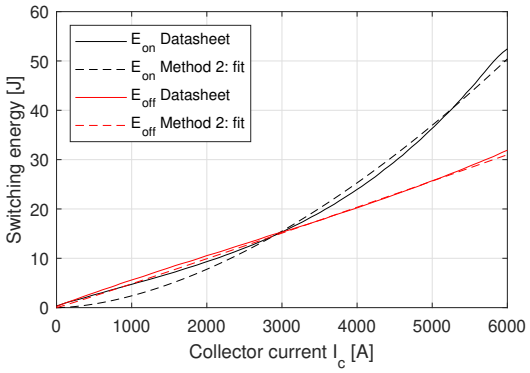
First, the *5SNA 3000K452300* IGBT switching losses $P_{sw,I}$ as a function of the collector-current are studied. These losses should scale linearly according to the approaches method 1 (3.34) and method 2 (3.35), while method 3 (3.36) suggests it is polynomial. However, the curve-fitting requirement from

Table 3.2: Semiconductor parameters used in the analysis.

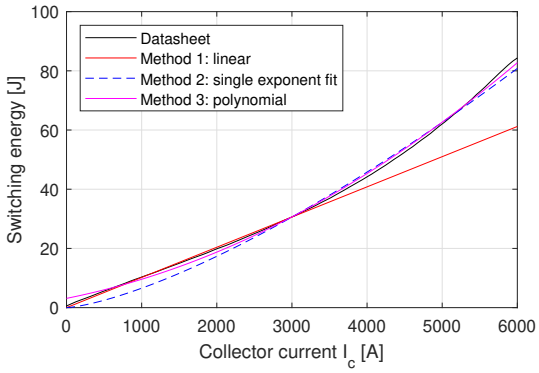
Device	Blocking voltage [kV]	DC-collector current [kA]	Peak collector-current [kA]
5SNA 3000K452300	4.5	3.0	6.0[a]
5SJA 3000L520300	5.2	3.0	6.0[a]

[a] Maximum time-duration 1 ms

this method opens to possibility for linear scaling if the second-order term is neglected. Figure 3.2a shows the energy losses for a single switching action. Switching the device to ON-state is depicted apart from switching the device to OFF-state due to the difference in overshoot. In Figure 3.2b the summation of these individual switching actions is depicted.



(a) Single switching action: K_i = 1.7 for E_{on} and 1.0 for E_{off}.



(b) Complete switching action: K_i = 1.4, a_0 = 3.1, a_1 = 5.1×10^{-3}, and a_2 = 1.4×10^{-6}.

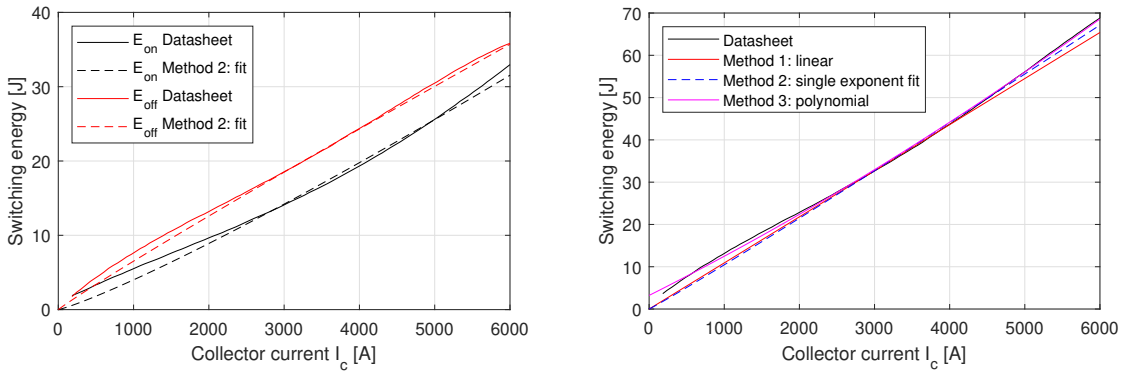
Figure 3.2: Switching energy losses for the IGBT semiconductor chips in the *5SNA 3000K452300* IGBT device.

The losses of both individual switching actions and subsequent summation are shown to scale approximately linearly for a current 0–3 kA in Figure 3.2a. This proves the switching loss computation according to the first two approaches. For the higher current range, 3–6 kA, the switching losses start to differ from the linear estimation method and are only accurately estimated using the third method. As seen in Figure 3.2b, this is a result of the losses due to switching to ON-state. Since the device is rated for continuous a DC-current of 3 kA, the device can handle this current only for a shorter time period (with 6 kA maximum 1 ms). During a pole-to-ground fault, the pole current will increase fast until the fault has been cleared by the protection. During the rise in pole current, the arm current will likewise increase while the switching losses will increase even faster. This stresses the importance of terminating the switching process during faults preventing losses from scaling faster and jeopardizing the semiconductor's maximum permittable junction temperature. Normally this is 150 degC while the semiconductors are operated at 70–90 degC.

A curve-fit for both curves depicted in dashed lines confirms the linear scaling for a current 0–3 kA and a higher order if a larger current range 0–6 kA has been taking into account as the scaling factors obtained are $K_i = 1.7$ for E_{on} and $K_i = 1.0$ for E_{off}. The summation of both gives a current scaling of $K_i = 1.4$ for 0–6 kA. The accuracy of this value is clearly seen to be more accurate for a collector current above 3 kA while the converters of interest are below 2 kA. This means that the current scaling factor of $K_i = 1.0$ according to Table 3.1 holds for this IGBT device.

A similar analysis has been done for the RC-IGBT *5SJA 3000L520300* device. The results are shown in Figure 3.3.

For the RC-IGBT device, E_{on} and E_{off} are estimated for a collector-current of 0–6 kA to scale with $K_i = 1.15$ and $K_i = 0.95$ respectively. This is near to linear especially compared to the conventional IGBT device. Less effect from increased switching losses due to a collector current above the rated continuous DC-operating current can be seen at this device. This means switching this IGBT device has less contributing to overheating the semiconductor junctions during DC-faults compared to the



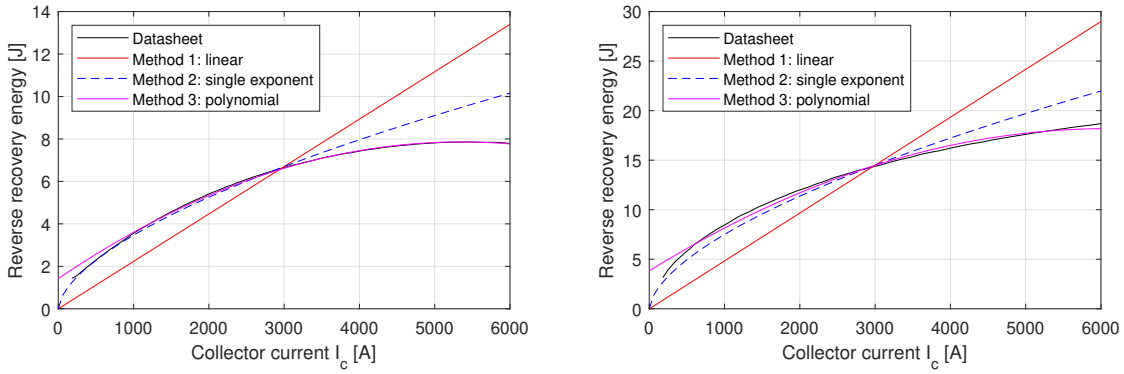
(a) Single switching action: K_i = 1.15 for E_{on} and 0.95 for E_{off}.

(b) Complete switching action: K_i = 1.04, a_0 = 3.2, a_1 = 8.9$\times 10^{-3}$, and a_2 = 3.3$\times 10^{-7}$.

Figure 3.3: Switching energy losses for the IGBT semiconductor chips in the *5SJA 3000L520300* RC-IGBT device.

conventional studied IGBT device. Adding both individual switching losses together shows a fit of $K_i = 1.0$ with a tight approximation for 3–6 kA. Due to the linear behaviour over the entire collector current range, the third approximation does not give additional benefits for this RC-IGBT device.

The analysis for the E_{rr} losses for both devices is depicted in Figure 3.4.



(a) IGBT device: K_i = 0.60, b_0 = 1.4, b_1 = 2.4$\times 10^{-3}$, and b_2 = -2.3$\times 10^{-7}$.

(b) RC-IGBT device: K_i = 0.60, b_0 = 3.8, b_1 = 4.7$\times 10^{-3}$, and b_2 = -3.9$\times 10^{-7}$.

Figure 3.4: Reverse-recovery losses for the FWD semiconductors in the *5SNA 3000K452300* IGBT and the *5SJA 3000L520300* RC-IGBT device.

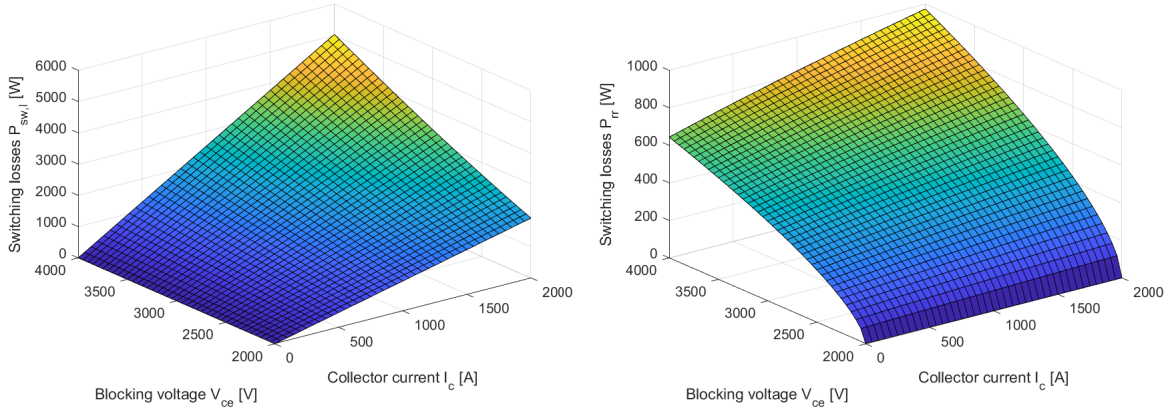
According to the figures, the scaling factor of $K_i = 0.6$ is matching for a collector-current 0–3 kA and therefore matches with the SEMIKRON parameters. The approximation for a collector current of 3–6 kA seems to match better for the third method with the polynomial. Obviously, the linear approximation is not accurate.

For the voltage scaling losses, no comparison is possible since loss measurements as function of the blocking voltage are not provided for the studied IGBT devices, nor for any regular IGBT device. If the voltage scaling factor $K_v = 1.4$ is assumed, the IGBT semiconductor switching losses are as shown in Figure 3.5a and the FWD reverse recovery losses in Figure 3.5b for the *5SNA 3000K452300* IGBT device.

3.3. Total Average Losses

All loss components can be added together to compute the average power losses for IGBT and FWD:

$$\begin{aligned} P_{T,av} &= P_{c,T,av} + P_{sw,av} \\ P_{D,av} &= P_{c,D,av} + P_{rec,av} \end{aligned} \tag{3.37}$$



(a) IGBT semiconductor: K_i = 1.0 and K_v = 1.4.

(b) FWD semiconductor: K_i = 0.6 and K_v = 0.6.

Figure 3.5: Switching and reverse-recovery losses for the *5SNA 3000K452300* IGBT device with method 2 and SEMIKRON parameters.

Since the RC-IGBT has a shared junction between IGBT and FWD parts, the steady-state model will become time-dependent and thus more complex. Rather, the average power loss across the shared semiconductor chip should be computed,

$$P_{av,RC-IGBT} = \frac{1}{2\pi}\int_{t_1}^{t_2} \pi P_{av,Tx} \sin(\omega_0 t)\ dt + \frac{1}{2\pi}\int_{t_2}^{t_3} \pi P_{av,Dx} \sin(\omega_0 t)\ dt, \tag{3.38}$$

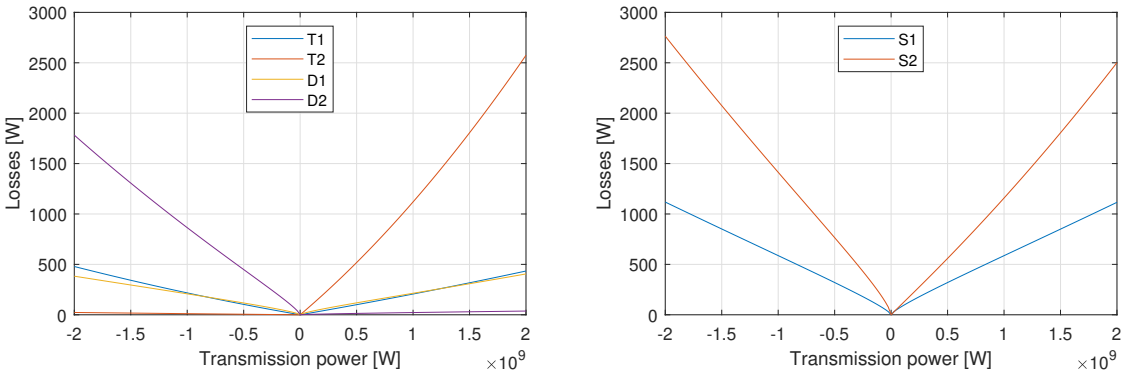
such that the power loss is time-independent and the same methodology as with conventional IGBT devices can be used. This assures a generalized mathematical methodology for IGBT/RC-IGBT condition assessment. Since the average loss computation for RC-IGBT devices is a complex process where a comparison is needed between the conventional model in (3.37) and a practical experiment required to determine the best estimation, for simplicity (3.37) has also been used for the RC-IGBT device in this research. Both $P_{T,av}$ and $P_{D,av}$ are added together forming the losses of the top IGBT device S_1 and the lower IGBT device S_2 in the half-bridge configured submodules.

Case-study A 525 kV monopolar MMC rated 2 GW consisting of half-bridge configured submodules rated 3 kV has been used to study the submodule device losses. The converter operates in a steady state with modulation index $m = 1$, meaning arm current-ratio $k = 2$. The switching frequency is assumed 150 Hz and the power angle θ at the AC-side is selected as 0 degrees. Semiconductor parameters used are depicted in Table 3.3.

Table 3.3: Semiconductor parameters used in the analysis. Eon, Eoff, Err, reference measurements made at 2800 V, 3000 A.

Device		$V_{0,cx}$ [V]	$R_{c/f}$ [mΩ]	E_{on} [J]	E_{off} [J]	E_{rr} [J]
5SNA 3000K452300	IGBT	1.6	66.7	15.5	15.1	
5SNA 3000K452300	FWD	1.7	33.3			6.7
5SJA 3000L520300	IGBT	1.7	40.0	14.2	18.5	
5SJA 3000L520300	FWD	2.5	36.4			14.5

Both devices have been modelled with the determined loss scaling coefficients. This means the IGBT switching losses are calculated with the linear scaling method. Even though the polynomial from the third method shows a better approximation, the losses are here non-zero if there is no collector current. For the reverse recovery losses of the FWD, the single exponent from the second method has been used. The SEMIKRON scaling factor $K_i = 0.6$ has been used for both devices. For the conventional IGBT device, the device losses as a function of the converter loading are shown in Figure 3.6a while for the RC-IGBT these results are demonstrated in Figure 3.6b.



(a) IGBT Device *5SNA 3000K452300*.

(b) RC-IGBT Device *5SJA 3000L520300*.

Figure 3.6: Total semiconductor power losses in 3 kV rated half-bridge configured submodules for conventional IGBT and RC-IGBT devices. A negative transported power means the converter operates in rectifier mode while a positive value indicates it operates in inverter mode.

From the figures, multiple things can be concluded:

- The total average power losses are highest in FWD *D2* in a converter operating in rectifier mode as a result of the predominantly negative AC arm-current $i_{xy}(t)$ from the DC-offset in this operation mode.
- Contrary, the total average power losses are highest in IGBT *T2* for inverter mode due to the predominantly positive AC arm-current. This indicates the total average device power losses are highest for bypass switch *S2* in the half-bridge configuration as seen for the RC-IGBT.
- The power loss component summation gives nearly equal switch losses between the inverter and rectifier operation mode for the RC-IGBT. This does not mean the device is more usable irrespective of operation mode; the significant loss contribution from IGBT or FWD is comparable to the conventional IGBT.
- The least losses are generated in IGBT *T2* in rectifier mode. This means semiconductors with more losses can be installed at this position in order to reduce costs.
- FWD *D1* experiences low losses in both inverter and rectifier operation modes. Next to the de-rated IGBT *T1*, the whole switching device *S1* can be optimized on costs and other factors.

4
Converter Thermodynamics

The estimation model to exclude external influences from the condition indicator estimation consisted of two aspects: the power loss estimation of the semiconductors and the estimation of the absolute junction temperature. The power loss estimation in the previous chapter revealed the power loss dependency on temperature. This chapter aims to estimate the junction temperature of all four semiconductors in half-bridge submodules depending on the converter operational conditions. First, the cooling system configurations in modern MMC are outlined and the temperature components are analysed. A model considering realistic estimations and available measurements is presented. This is followed by simulations for the steady-state and ripple component. Finally, a complete simulation model is developed to verify the analytical computations.

4.1. Cooling System Structure

The submodule device cases are connected to one or more heat sinks which are subsequently cooled by a closed-loop liquid cooling system. Di-ionized water is often used as a coolant to prevent pipe erosion and current loops between devices. The coolant is mixed with glycol such that the coolant has a low freezing point and excellent heat transfer properties. Heat exchangers are used to keep the coolant within temperature boundaries assuring all semiconductors are operated at a preferred temperature. These heat exchangers transfer the excess heat energy to an outer closed-loop cooling system with a different coolant optimized for heat dissipation outside the converter hall (e.g. without di-ionized water). For offshore converter stations, this outer loop can be configured to either dissipate the heat energy into the seawater or the open air. TenneT $2\,$GW offshore converter stations are required to dissipate the excess heat energy in the open air. An overview of a closed-loop inner-cooling system is depicted in Figure 4.1.

The system is shown to cool two submodules in series (N_s) and three submodules in parallel (N_p). Normally, the maximum amount of submodules in parallel is determined by the converter tower arrangement as series cooling between converter towers is impractical. The number of modules in series and parallel is project and device-specific, making these preferred model parameters for the temperature estimation. The cooling system further consists of the di-ionizer, heat exchanger to an outer cooling loop, and cooling pump. There are two temperature sensors depicted at the cooling system inlet and outlet valves. Inside the half-bridge submodules, the IGBTs and FWDs can also be cooled in series or parallel combination but is not depicted in this example.

Assumptional remark A reference temperature measurement in these cooling systems is needed to estimate the absolute junction temperature of each semiconductor. Most researchers assume there is a thermocouple installed at each individual heat sink connected to the semiconductors (e.g. [42]–[44]). Although this assumption will make the estimation process straightforward with less thermodynamic analysis involved, it is very impractical in real converters considering the number of thermocouples needed. While each thermocouple has a low failure probability, the hundreds of submodules with double the amount of heat sinks in a modern MMC will introduce new uncertainties; if an erroneous semiconductor is detected, how to be sure this is not due to a thermocouple failure?

In this work, it is therefore assumed there are no thermocouples available at each heat sink connected to a semiconductor. Instead, there are coolant temperature sensors installed in the inner di-ionized water cooling system at each converter tower coolant inlet and outlet pipe, implying each parallel combination of cooled submodules has an inlet and outlet temperature measurement available.

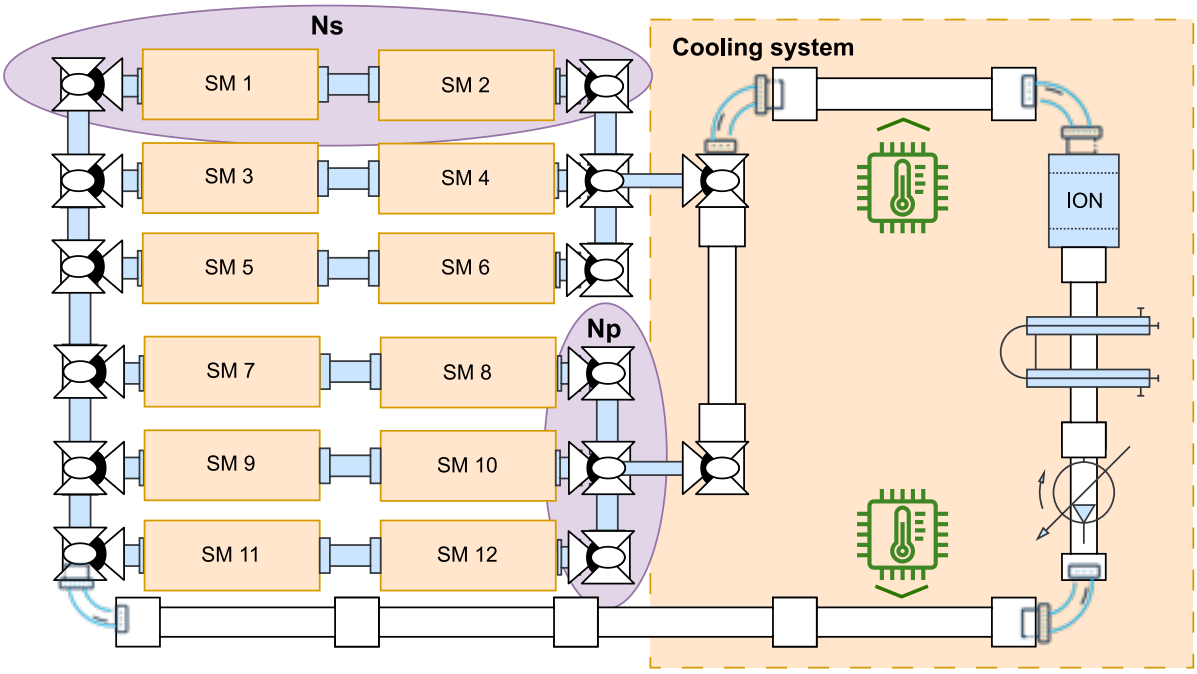


Figure 4.1: Converter cooling system illustration. In this configuration there are two submodules cooled in series and three submodules cooled in parallel. Temperature sensors are here installed at the cooling system inlet and outlet valves.

Since the complete heating process in between these inlet and outlet pipes is primarily due to semiconductor losses in this tower [45], the semiconductor power loss models from Chapter 3 can be used in thermodynamic modelling from the parallel combination inlet and outlet temperature to the semiconductor junctions. The following section first illustrates the temperature components where each component estimation process is outlined.

4.2. Temperature Components

The fluctuation of the IGBT junction temperature is mainly determined by the load-current [46]. If the converter is varying load conditions (e.g. I_{dc} or the circulating current between the arms), or the cooling system changes states (e.g. increasing flow rate) the junction temperature enters a transient state till a new power balance has been established. After several fundamental $50\,\text{Hz}$ AC cycles, the average junction temperature reaches steady-state [47]. A power balance between dissipated and absorbed heat is formed and only a small fluctuation ΔT_j is seen over the semiconductor junctions. This means the junction temperature estimation can be split into three parts:

- Steady-state: average junction temperature as a result of the power losses and cooling system dissipated heat being balanced.
- Transient: varying junction temperature if the arm current makes a change due to varying load conditions or the cooling system power dissipation changing its set-points.
- Ripple: temperature fluctuation over static steady-state or transient temperature component due to the fundamental $50\,\text{Hz}$ AC cycles.

Steady-state converter operation semiconductor loss estimations were made for each individual submodule (e.g. (3.14) and (3.15)). The submodule-enabled probability used here omits the need for the exact control scheme implementation but is only possible for average losses under steady-state operation. With the complex control mechanisms applied in real MMC, it is problematic to estimate the losses in a transient state. These controls are project and manufacturer specific; meaning each project requires a specific approach for semiconductor condition monitoring. This means that the losses only hold under constant converter loading conditions. These conditions should be constant for at least several fundamental $50\,\text{Hz}$ cycles determined by the thermal inertia. If the cooling system is

changing set points to keep a power dissipation balance, its time constant is slower than the electrical time constants. After the converter settles to a steady-state loss component, it takes more time for the cooling system temperature to settle. There is thus no need to consider the junction temperature transient component. The estimation of the steady-state junction temperature and the overlaying ripple is explained in the following sections.

4.2.1. Steady-state

For conventional IGBT devices with both IGBT and FWD semiconductor chips soldered to the base plate apart from each other, the junction temperatures are different. The heat losses produced by the devices are first released in the respective semiconductor chip junction layer and dissipated through the other device layers to the module case. This case could be single- or double-sided cooled. By using the thermal impedance from junction to device case $Z_{th,JC}$, the junction temperatures,

$$\begin{aligned} T_{j,T} =& P_{T,av} Z_{th,JC} + T_C \\ T_{j,D} =& P_{D,av} Z_{th,JC} + T_C, \end{aligned} \tag{4.1}$$

are given by the average device power losses $P_{T/D,av}$ and the module case temperature T_c. The thermal impedance $Z_{th,JC}$ is in general represented as a fourth-order Foster or Cauer network as shown in Figure 4.2. Manufacturers normally provide Foster network thermal resistance R_n and thermal capacitances C_n parameters in datasheets [48]. The Foster network could be translated to a Cauer network using curve-fitting. In these networks only the junction and case nodes do have physical meaning, all intermediate nodes can not be used to estimate temperatures or heat flows.

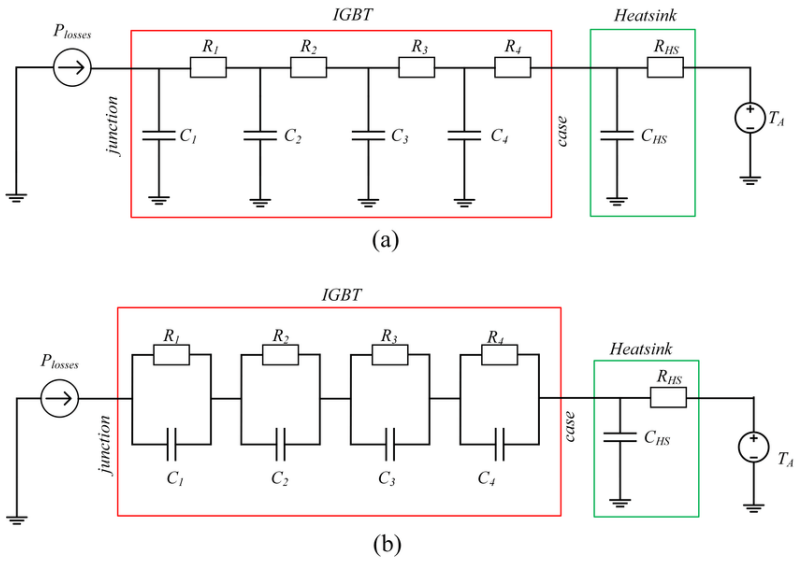


Figure 4.2: Thermal Cauer (a) and Foster (b) electrical circuits used to estimate the junction temperature from the power losses. A heat sink with outer temperature T_a is connected to the IGBT device. Figure is taken from [48].

All heat sinks are cooled by a flowing liquid in MMC-type HVDC converters. A single-sided heat sink module has a thermal resistance $R_{th,hs}$ between the heat-sink coolant inlet and the heat-sink top layer connected to the device case. This thermal resistance,

$$R_{th,hs} = R_{th,0} + \frac{K_w}{f_w}, \tag{4.2}$$

depends on the coolant flow rate f_w and contact resistance K_w [49]. The higher the coolant flow rate, the lower the thermal resistance and thus the less the heat sink itself heats up. In case double-sided cooling is used, there is also a temperature coupling between both sides. This coupling through the heat-sink side walls is represented using first-order Cauer model parameters,

$$\begin{aligned} R_{sw} =& \frac{l_s}{A_s k_{AIN}} \\ C_{sw} =& m_s c_{AIN}, \end{aligned} \tag{4.3}$$

depending on the side-wall height l_s, area A_s, mass m_s, thermal conductivity k_{AlN}, and heat capacity c_{AlN} [50]. The first law of thermodynamics formulates the conservation of energy. The energy losses dissipated by the IGBT devices are transferred to the liquid coolant. The temperature in the heat-sink pipe section will rise from inlet T_{in}^{liq} to T_{out}^{liq}. Further, the time-derivative of the heat-gain in the liquid coolant,

$$\begin{aligned} E =& m_c c_p \left(T_{out}^{liq} - T_{in}^{liq}\right) \\ \frac{dE}{dt} =& c_p \frac{dm_c}{dt} \left(T_{out}^{liq} - T_{in}^{liq}\right) + c_p m_c \frac{d}{dt} \left(T_{out}^{liq} - T_{in}^{liq}\right), \end{aligned} \tag{4.4}$$

indicates that the rate of change of energy dE/dt supplied to a fluid with specific heat capacity c_p, mass m_c, is configurable by the mass-flow rate dm_c/dt which can be obtained by multiplying the volumetric flow rate by the fluid density. The higher the mass flow rate in the inner cooling system as set by the pump, the faster the temperatures over the heat sinks will settle to a steady-state value after an alteration in dissipated heat energy. It is important to note dE/dt represents the power losses dissipated in all semiconductors in the half-bridge submodules where it can generally be assumed $95\,\%$ of the power losses are transferred to the liquid coolant [45]. Under steady-state the heating of the coolant simplifies to:

$$\frac{dE}{dt} = c_p \frac{dm_c}{dt} \left(T_{out}^{liq} - T_{in}^{liq}\right) \tag{4.5}$$

The steady-state coolant inlet temperatures of any heat sink in a chain of series-connected heat sinks can be calculated using (4.5) whereafter (4.2) can be used to estimate the device case temperature T_c. If N_p heat-sinks are cooled in a parallel configuration, the mass flow rate decreases by $1/N_p$.

There is often a selective variety of data available in practical applications and it varies between projects. If the thermal resistance from heat-sink coolant inlet to surface $R_{th,hs}$ in (4.2) is unavailable, another method can be used to estimate the heat sink surface temperature T_{hs}. Herewith, the heat-sink coolant outlet temperature T_{out} can be written as a differential equation [51],

$$c_p \rho V_p \frac{dT_{out}^{liq}}{dt} = c_p \frac{dm_c}{dt} \left(T_{in}^{liq} - T_{out}^{liq}\right) + h_c \left(T_{hs} - T_{out}^{liq}\right), \tag{4.6}$$

with parameters the plate volume V_p, heat-transfer coefficient h_c of the heat-sink, and its surface temperature T_{hs}. For all pipe sections in between the heat sinks and valve tower inlet and outlet, the temperature change can be written [51],

$$c_p \rho V_p \frac{dT_{out}^{liq}}{dt} = c_p \frac{dm_c}{dt} \left(T_{in}^{liq} - T_{out}^{liq}\right) \tag{4.7}$$

as a function of the section pipe volume V_p and the mass flow rate. It again emphasizes the higher the mass-flow rate in the pipe section, the faster the temperature settles to a steady-state value. This means that for fast dynamics in the load current, the cooling system should have a sufficient mass-flow rate such that the heat exchanger is able to transfer all heat energy from the di-ionized water cooling loop.

In [52] analysis was performed to solve the temperature distribution between the pipe surface connected to the heat-sink, and the coolant inside the pipe. This implies solving the presented differential equations adjusted to the temperature difference along the pipe surface and liquid coolant. First, using the temperature difference between the heat sink and outlet,

$$c_p \rho V_p \frac{d\left(T_{hs} - T_{out}^{liq}\right)}{dt} = h_c A_p \left(T_{hs} - T_{out}^{liq}\right), \tag{4.8}$$

a differential equation is formed with the heat-sink heat transfer rate and its surface area equal to the perimeter for a cylindric pipe. The solution of this differential equation gives the heat transfer between the heat sink surface temperature and the heat sink coolant inlet temperature,

$$\begin{aligned} T_{out}^{liq} =& T_{hs} - \left(T_{hs} - T_{in}^{liq}\right) e^{-\frac{t}{\tau}} \\ \tau =& \frac{c_p \frac{dm_c}{dt}}{h_c A_p}, \end{aligned} \tag{4.9}$$

indicates the time constant τ is defined by the heat-sink liquid pipe perimeter A_p, the heat-transfer coefficient, mass flow rate, and specific heat of the liquid coolant. In laminar flow, the heat transfer coefficient h_c can be calculated from the Nusselt number *Nu*, fluid average thermal conductivity k_{av}, and the pipe diameter d_p:

$$h_c = Nu\frac{k_{av}}{d_p} \tag{4.10}$$

A model for a liquid pipe heat sink is available in MATLAB/Simulink. Its fundamental equations are formed based on the outlined heat transfer properties. First, the solution of the convective heat flow term $h_c\left(T_{hs} - T_{out}^{liq}\right)$ from the presented differential equation in (4.6) is specified as:

$$\frac{dE}{dt} = \frac{dm_c}{dt}c_p\left(T_{hs} - T_{in}^{liq}\right)\left(1 - e^{\frac{-t}{\tau}}\right) \tag{4.11}$$

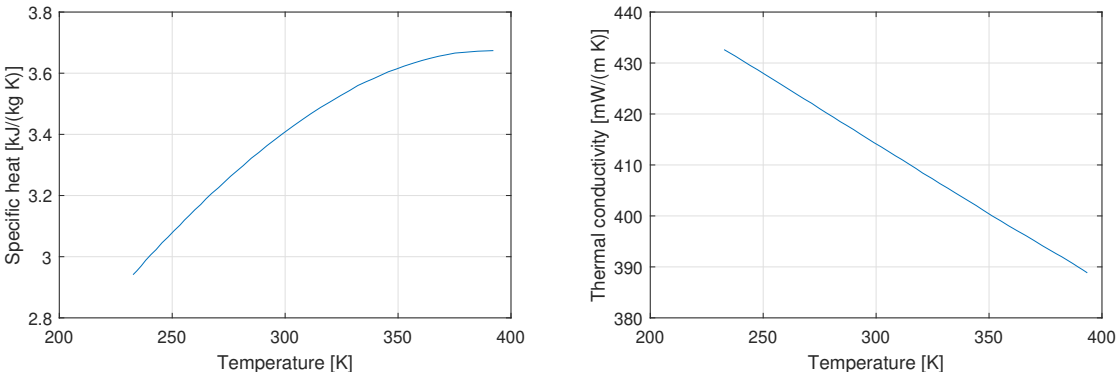
while the conductive heat transfer, which was neglected in [52], is given:

$$\frac{dE}{dt} = \frac{k_a v S_h}{d_p}\left(T_{hs} - T_x^{liq}\right), \tag{4.12}$$

with T_x^{liq} representing the liquid coolant temperature in between the inlet and outlet. This temperature varies according to the number of parameterized sections inside the heat sink. Since the heat flow from the heat sink to liquid coolant depends on the temperature difference, this heat flow is generally not similar over the whole length of the liquid pipe inside the heatsink, implying the more sections considered, the higher the computation accuracy. By solving (4.11) and (4.12) for steady-state conditions, the heat-sink temperature T_{hs} can be approximated:

$$\begin{aligned} T_{hs} =& \frac{d_p}{k_a S_h + D\frac{dm_c}{dt}c_p\kappa}\left(c_p\frac{dm_c}{dt}\left(\Delta T^{liq} + T_{av}^{liq}\frac{k_{av}S_h}{d_p}\right) + T_{in}^{liq}\frac{dm_c}{dt}c_p\kappa\right) \\ \kappa =& 1 - exp\left(\frac{-Nuk_{av}S_h}{d_p m_c c_{p,av}}\right) \end{aligned} \tag{4.13}$$

For water coolant with $50\,\%$ ethylene glycol volume mixture, specific heat and the average thermal conductivity obtained from MATLAB/Simulink database are depicted in Figure 4.3a.



(a) Specific heat.

(b) Average thermal conductivity.

Figure 4.3: Thermal properties of a $50\,\%$ Volume ethylene glycol and water mixture under constant pressure. Results obtained from MATLAB/Simulink thermal fluids database.

The thermal property temperate dependency shows that a higher temperature drop over the heat-sink inlet and outlet valves not only affects the heat flow but also the coolant heating. A higher temperature drop means more heat energy is required to raise the outlet valve temperature compared to the inlet valve temperature. Besides, an average value for specific heat and thermal conductivity can only be taken if the temperature drop is low, otherwise, optimization is needed to find the average temperature in the heat sink or the heat sink model should be divided into multiple sections.

Simulation A simulation with six half-bridge configured submodules is made in MATLAB/Simulink. Each submodule contains two *5SJA 3000L520300* Hitachi Energy RC-IGBT devices both connected to a single-sided liquid-cooled heat sink. The converter is assumed to operate in rectifier mode with approximately 2 GW power transmission. This means the average power loss in device *S1* is 1 kW while the average power losses in *S2* is 2.5 kW as was illustrated in Figure 3.6b. Inside the submodule, *S1* and *S2* are cooled in series. There are three rows ($N_\text{p} = 3$) of parallel cooled submodules. The coolant mass-flow equals 6 kg/s for the valve tower inlet, meaning the flow through each series string is 2 kg/s. An overview of the cooling configuration is depicted in Figure 4.4.

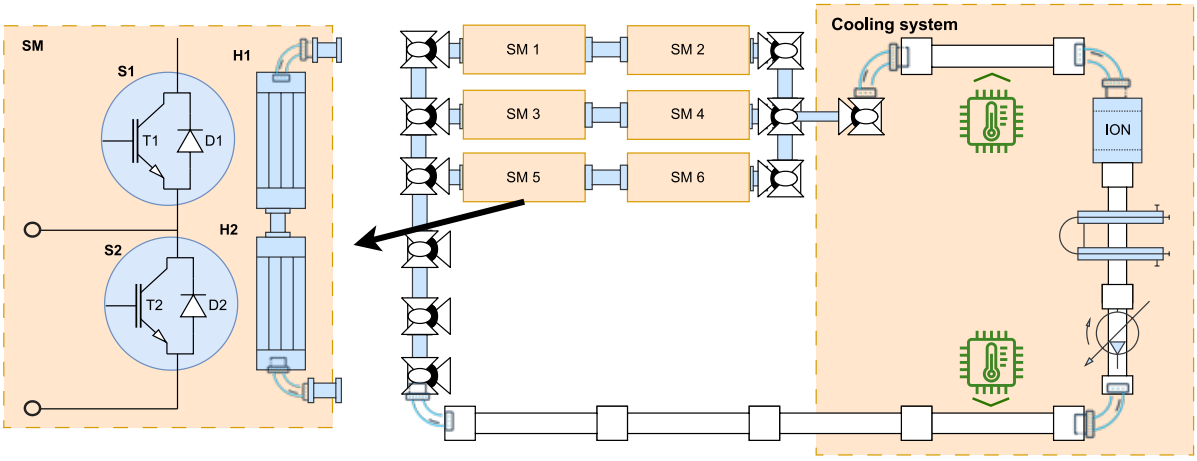


Figure 4.4: Illustration of the simulated cooling system. There are three submodules configured in parallel representing a converter tower. Each parallel string consists of two series of cooled submodules. Both IGBT devices in a single submodule are cooled in series.

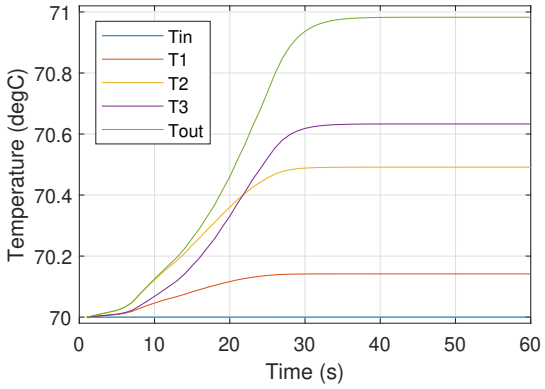
In the presented analytical computations multiple things can be noticed. First, in (4.7), it was shown that the mass flow is a main parameter in the heating liquid coolant inside pipe sections. This parameter thus should keep the liquid temperature in between a threshold in order to control the heat sink temperature at a preferred temperature. This temperature is the main parameter influencing the IGBT device temperatures and should generally be around 80 degC in practical application. In (4.8) it was shown that the pipe section area in the heat sink is a main control parameter for the heat sink temperature if those liquid temperatures are controlled. As a result, two case studies have been considered:

- First, all heat-sinks have length 20 m and diameter 2 cm. This represents a straightforward design where heat sinks can be implemented in a modular way.

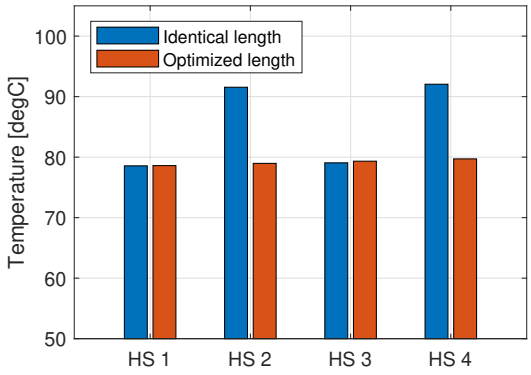
- Second, the heat-sinks connected to *S1* have length 20 m and the heat-sinks connected to *S2* have length 50 m. The ratio between these lengths is optimized to the average power losses ratio and should therefore result in a more equal temperature distribution over the heat sinks.

The resulting liquid temperatures of one string of heat sinks are shown in Figure 4.5a. There are five temperatures shown, the first is the inlet temperature of the cooling system. This is followed by the temperature drop over the heat sink connected to *S1*, and subsequently the temperature over the heat sink over *S2*. After this, the second series connected submodule with a similar configuration is shown. Lastly, the output temperature is shown, equal to the temperature drop over the heat sink connected to *S2* of the second heat sink. The heat sinks temperatures of both study cases is depicted in Figure 4.5.

First, it can be seen that the temperature drop over the liquid in a series string of two cooled submodules is below 2 degC with 2 GW converter operation. As expected, the higher the power loss in an IGBT device, the higher the temperature drop over the liquid inside a heat sink. This is within the temperature range specified for the IGBT and indicates the mass flow rate is sufficient. If needed even more submodules can be cooled in a series configuration. Next, the heat-sink temperatures are shown to be more equal to the preferred 80 degC for the optimized length case. There is a large temperature variation seen over the different heat sinks for the identical length case. This means the IGBT devices are not operated at a similar temperature which should be avoided.



(a) Temperatures of the liquid coolant with all heat sinks having identical length.



(b) Temperatures of the heat sinks with two considered heat sinks parameterizations.

Figure 4.5: Temperatures inside the series connection of heat sinks. There are four heat sinks meaning five liquid coolant temperature measurements.

4.2.2. Ripple

The junction temperature ripple is a result of the AC-system fundamental frequency cycles. As the module thermal impedance time constant is much lower compared to the heat-sink time constant, this fluctuation can only be observed inside the IGBT or FWD semiconductors. The IGBT and FWD average power losses over one switching cycle were computed in Chapter 3. To estimate the junction temperature ripple, these should be divided into smaller parts as the loss scales with the arm current and is thus sinusoidal. Each half-wave cycle can be divided into several blocks, as long as its time length equals at least the minimum device thermal impedance time constant. It was shown in [47] that by dividing the losses over a half-wave period into four instants,

$$\begin{aligned} P_{1,4} =& 8 f_0 \int_0^{\frac{1}{8 f_o}} \pi P_{T/D,av} \sin\left(\omega_n t\right)\, dt = P_{T/D,av}\left(4 - 2\sqrt{2}\right) \\ P_{2,3} =& 8 f_0 \int_{\frac{3}{8 f_o}}^{\frac{1}{8 f_o}} \pi P_{T/D,av} \sin\left(\omega_n t\right)\, dt = P_{T/D,av} 2\sqrt{2}, \end{aligned} \tag{4.14}$$

the maximum junction temperature occurs after the third instant and the minimum at the instant of switching in which is at the initial of the first part. Using the fact that for steady-state operation, the minimum junction temperature of a cycle is equal to the minimum of the next cycle and for the maximum junction temperature the contrary holds, the steady-state minimum $T_{j,k'}$ and maximum junction temperature $T_{j,k}$ can be written:

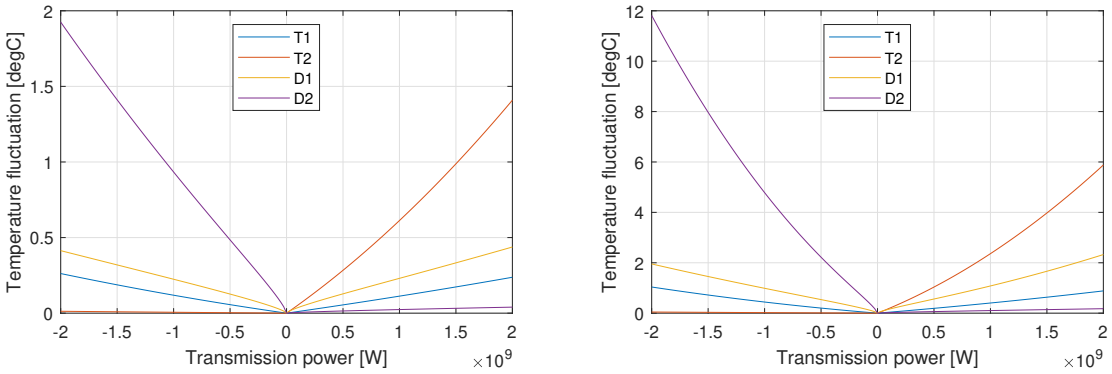
$$\begin{aligned} T_{j,k'} =& \frac{P_1 Z_{th}\left(3\Delta t\right) e^{\frac{-5\Delta t}{\tau}} + \left(P_2 - P_1\right) Z_{th}\left(2\Delta t\right) e^{\frac{-5\Delta t}{\tau}} + P_1 Z_{th}\left(\Delta t\right) e^{\frac{-4\Delta t}{\tau}}}{1 - e^{\frac{-8\Delta t}{\tau}}} \\ T_{j,k} =& \frac{P_1 Z_{th}\left(\Delta t\right) e^{\frac{-7\Delta t}{\tau}} + P_1 Z_{th}\left(3\Delta t\right) + \left(P_2 - P_1\right) Z_{th}\left(2\Delta t\right)}{1 - e^{\frac{-8\Delta t}{\tau}}} \end{aligned} \tag{4.15}$$

Substraction of the maximum and minimum junction temperature during a steady state gives the expression for the temperature ripple:

$$T_{jk} - T_{jk'} = \frac{P_1 Z_{th}\left(\Delta t\right)\left[e^{\frac{-7\Delta t}{\tau}} - e^{\frac{-4\Delta t}{\tau}}\right] + P_1 Z_{th}\left(3\Delta t\right)\left[1 - e^{\frac{-5\Delta t}{\tau}}\right] + \left(P_2 - P_1\right) Z_{th}\left(2\Delta t\right)\left[1 - e^{\frac{-5\Delta t}{\tau}}\right]}{1 - e^{\frac{-8\Delta t}{\tau}}} \tag{4.16}$$

For RC-IGBT devices the estimation is impossible because it is unknown when the maximum and minimum temperature values will occur. This depends on all operational conditions and device specifications, and is therefore excluded in this research. First practical experiments should be performed to develop a simplified analytical junction temperature ripple model for these devices. Since RC-IGBT devices have a more homogeneous temperature ripple profile compared to the conventional IGBT devices

due to the shared junction, the ripple is lower and causes less degradation. Therefore conventional IGBT devices can be taken as worse-case scenario. The results for the junction temperature ripple for the semiconductors in half-bridge configured submodules is shown in Figure 4.6.



(a) Hitachi Energy *5SNA 3000K452300* IGBT.

(b) Infineon *FZ1200R45HL3* IGBT.

Figure 4.6: Semiconductorr junction temperature swing in 2.5 kV rated half-bridge configured submodules for conventional IGBT and RC-IGBT devices. A negative transported power means the converter operates in rectifier mode while a positive value indicates it operates in inverter mode.

In the figures, it is seen that the junction temperature ripple is very device-specific. While for the Hitachi Energy IGBT this is generally below 2 degC, the Infineon IGBT shows a higher junction temperature ripple. It is important to note manufacturers can not be compared based on these results. Both devices could differ in price or be used in different converters. While the specific Hitachi Energy IGBT performs better regarding junction temperature ripple, Infineon could prefer another IGBT device for 2 GW converters.

4.3. Simulation

A simulation model has been developed in MATLAB/Simulink to verify the analytical analysis. Both temperature components have been included in the model and the losses are simulated with an electrical model of the IGBT devices. The model is further outlined in the following paragraphs.

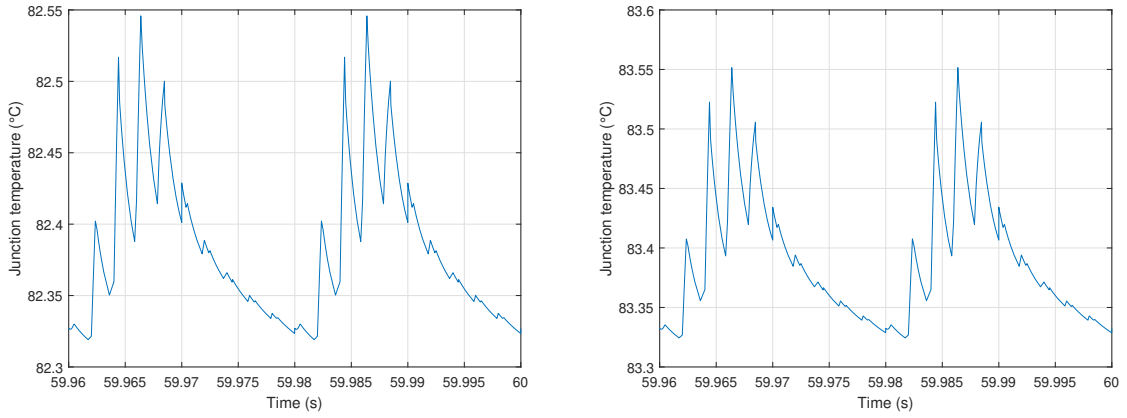
IGBT Electrical An MMC arm has been modelled with two submodules. In these submodules, both semiconductors from *S1* are represented with the average loss models while both IGBTs semiconductors from *S2* are modelled with a detailed model. With the converter operating in inverter mode, the detailed modelled semiconductors have the highest power losses and thus are most relevant to study. This means the ON-state characteristics are non-linear, causing non-linear conduction losses, and the switching losses are tabularized and junction temperature dependent. This junction temperature dependency factor could be seen in (3.35) with parameters $c_{T,sw}$ and $c_{T,rr}$. Since these factors are not provided in datasheets nor are impossible to estimate according to the available data, temperature dependency was excluded in the power loss estimation methodology. The Hitachi Energy *5SNA 3000K452300* IGBT device has been imported in MATLAB/Simulink with its datasheet parameters which use a linear extrapolation for $c_{T,sw}$ and $c_{T,rr}$ based on the two provided energy loss reference values at 25 degC and 125 degC. It is important to understand this dependency is only an approximation and not particularly representing reality. In order to estimate the real temperature dependency factors, the losses from a physical IGBT device should be measured during practical experiments.

Both submodules have a peak-current of 2 kA which represents the DC-pole current. As a result, the submodule capacitor voltage is also periodic with a peak voltage of 2 kV. Each semiconductor device has a switching frequency of 500 Hz. Each time the devices switch, switching loss power is dissipated instantly, meaning the semiconductor switching waveform is modelled ideally and linearly, while the dissipated power losses are internally calculated as non-linear with respect to the collector-current as given in the datasheets. Differences between these linear and non-linear models were elaborated in Chapter 3. Because of the linear power dissipation representation, it is not possible to graphically study the switching waveforms of the IGBT devices.

IGBT Thermal The detailed IGBT device models have temperature-dependent losses. Fourth-order Cauer thermal network models as provided in the datasheets are imported according to their Foster equivalent network. Both final nodes in the Cauer networks are connected to the liquid-cooled heat sinks similar to the heat sinks studied in section 4.2.1, where the coolant pipe through the heat sink is adjusted to a length of $10\,\mathrm{m}$ and a diameter of $15\,\mathrm{cm}$ for optimal device junction temperature at approximately $80\,\mathrm{degC}$. While the IGBT device switching process is modelled linearly, the junction temperature swing is not completely bypassed. Internally calculated non-linear losses are dissipated instantly at a switching action, meaning at the time of switching the junction temperature is not very accurate and makes a step. Due to the smaller time scale of each switching action compared to the half-wave AC fundamental frequency, the junction temperature ripple is still present with a minimum and maximum value.

Cooling system A closed-loop inner cooling system with a $50\,\%$ water volume mixture of ethylene glycol is used. A pump and a pressurized tank in this loop are used to regulate the coolant mass flow and the coolant pressure at constant values. This pressure regulation further ensures the specific heat and the thermal conductivity of the coolant, as explained in section 4.2.1, are kept at a determined value such that an analytical approximation can be used to estimate the temperature component. The outer cooling loop is modelled ideal and the heat exchanger between is modeled with a thermal resistance. This assures realistic operating conditions and keeps the temperature of the liquid coolant in the inner cooling loop at a desired temperature such that the junction temperatures are operated around $80\,\mathrm{degC}$ to mimic realistic converter operational conditions.

Results The resulting junction temperatures are depicted in Figure 4.7 after steady-state converter operating conditions have been reached.



(a) Junction temperature of the first submodule IGBT device *T2*.

(b) Junction temperature of the second submodule IGBT device *T2*.

Figure 4.7: Junction temperatures of two IGBT devices *T2* from two subsequent submodules that are cooled in series. The coolant enters the first submodule andreturns to the heat exchanger after the second submodule.

Steps in junction temperature can clearly be seen in the plots as a result of the instantly dissipated switching losses when an IGBT device switches between ON and OFF states. This dictates the limitation of the available data on the simulation accuracy; for a more precise simulated junction temperature, the non-linear switching process should not only be internally calculated but also be used for heat dissipation. The junction temperature ripple component was estimated to be approximately $0.6\,\mathrm{degC}$ for both devices in section 4.2.2 for a roughly similar operating condition. Here, the submodule capacitor voltage was constant and slightly higher but the switching frequency was lower. Representing a model accuracy in all parameters and domains simultaneously is impossible on this scale. The junction temperature ripple in both simulated cases can be seen as approximately $0.2\,\mathrm{degC}$ where the difference can be mainly accounted to the inclusion of the temperature-dependent loss scale parameters in the Hitachi Energy IGBT model. While the junction temperature ripple was calculated based on a worse case operating junction temperature of $125\,\mathrm{degC}$, in the complete simulation these losses are calcu-

lated based on the real-time junction temperature and are thus lower. This further results in a lower junction temperature ripple.

5
Lifetime Optimization

A condition monitoring algorithm for multi-vendor and multi-technology IGBT devices applicable to different MMC generations based on the ON-state collector-emitter voltage measurement was presented in the previous chapters. This methodology can be used for the current Health Index used in TenneT TSO which is based on condition indicators.

The next step in MMC reliability research and development can be taken with the power loss and thermal models for the IGBT devices in half-bridge configured submodules. This Chapter will present a novel control methodology such that the converter operates more efficiently regarding the submodule's remaining lifetime. Since the controller operates on arm level, first the existing control processes on the converter-arm level are discussed. This is followed by the introduction of the lifetime balancing recommendation and the adjustments needed to the control philosophy. After this, the modulation techniques used in modern MMCs are examined and a methodology is presented to improve the suggested controller compatible with these modulation methods. Finally, an analytical approach is outlined to study the effect of the suggested control approach and a final simulation model is built to show the effect of the presented controller.

5.1. Submodule Energy Balancing

The MMC arms consist of a series connection of submodules with DC storage capacitors and semiconductors. Each submodule is constantly switched between enabled and disabled mode such that a desired arm voltage waveform is generated. The number of needed submodules per period depends on the arm voltage modulation index and varies depending on the converter reference settings. This is for the two arms connecting the AC A-phase to the DC poles, $u_{\mathrm{au}}(t)$ in the upper arm and $u_{\mathrm{al}}(t)$ in the lower arm as derived in (3.5).

Voltages in the DC-storage capacitors should be kept at the desired value (u_{sm}) with a ripple (Δu_{sm}) below a specified maximum to prevent the capacitor from charging to an overvoltage causing damage to the capacitor or discharging below a threshold where it can not effectively contribute to $u_{\mathrm{a}}(t)$. If the capacitor voltage is below a threshold (u_{sm}-$\Delta u_{sm}/2$), the converter arm is not able to reach $u_{\mathrm{au}}(t)$ or $u_{\mathrm{al}}(t)$, meaning the apparent modulation index ($m = 2E_m/U_{dc}$) is lower than anticipated. The allowed capacitor voltage ripple is generally assumed to be 10 % of its mean voltage level but varies according to project requirements [53]. Due to the modularity of the converter, the capacitor voltage fluctuation is split into two parts [54]:

- Entire submodule strings (arms) can be charged to different voltages.
- Within a converter arm the submodule capacitors can be charged to different voltages.

The capacitor voltage is determined by the capacitance, the current through the arm in which the capacitor is located, and the time instants when the subsequent submodule is enabled as outlined in (2.1). Since the capacitances are generally equal in each arm, only the average enabled probability (3.7) and the difference between the current through converter arms cause energy exchange between converter arms.

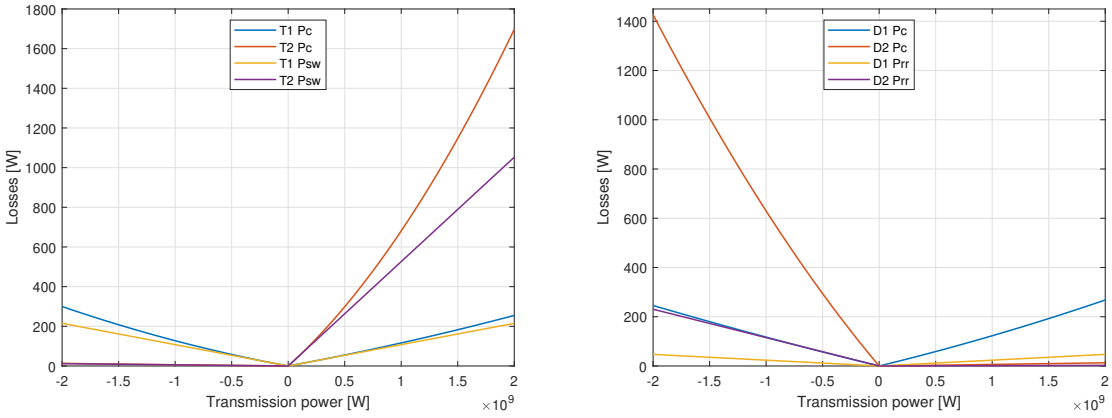
For the capacitor voltage variations within the arm, mainly the enabled probability over time causes differences between capacitor voltages. If one submodule is enabled when the arm current is positive, and another submodule is enabled when the arm current is negative, there will be a difference in u_{sm} between those submodules.

In order to keep a balance in voltage between different converter arms, the outer controller adjusts $u_{\mathrm{au}}(t)$ and $u_{\mathrm{al}}(t)$ for each converter leg with feedback loops. For the balance in voltages between

different submodules within a converter arm, an inner control mechanism is needed that translates $u_{\text{au}}(t)$ and $u_{\text{au}}(t)$ for each converter leg into submodule gate pulses. If a capacitor should be charged to a higher voltage, the corresponding submodule should be inserted when the current is entering from the submodule positive terminal while the contrary should happen when the current direction is opposed.

5.2. Lifetime Balancing

The remaining useful lifetime of an IGBT device depends largely on junction-temperature cycling in both the IGBT and FWD semiconductor chips as described in section 2.4. The larger the junction-temperature fluctuations in those semiconductors, the shorter the device's remaining useful lifetime will be. These fluctuations are caused by the semiconductor switching losses, reverse-recovery losses, and conduction losses which further depend on the converter operational conditions as shown in Figure 5.1 for a $525\,\text{kV}$ symmetrical monopolar MMC rated $2\,\text{GW}$. All submodules are configured in half-bridge configurations and do have *5SNA 3000K452300* Hitachi Energy IGBT devices.



(a) IGBT Semiconductor.

(b) FWD Semiconductor.

Figure 5.1: Semiconductor conduction (Pc), switching (Psw), and reverse-recovery (Prr) loss components in $150\,\text{Hz}$ switched half-bridge configured submodules equipped with a conventional IGBT device. A negative transported power means the converter operates in rectifier mode while a positive value indicates it operates in inverter mode.

The figure illustrates the IGBT semiconductor losses (predominantly *T2* conduction losses) are highest in inverter mode while *D2* conduction losses are highest in the rectifier mode. Since *D2* has low reverse recovery losses in inverter mode, the overall effect on remaining useful lifetime is limited. Contrary, it is clear that *T2* suffers both high switching and high conduction losses in inverter mode. This illustrates the ratio of how frequently a submodule is enabled (switching losses in *T2*) compared to disabled (conduction losses in *T2*) over time, mainly determines the submodule remaining useful lifetime.

Due to the desired sinusoidal arm voltage, as shown in (3.5), a specific amount of submodules $n_{\text{ins}}(t)$ in an arm should be enabled at a time instant depending on the sinusoidal reference waveform $u_{\text{au}}(t)$. The higher the sinusoidal reference waveform amplitude, the more submodules should be switched to the enabled mode by firing respective gate signals $GS_{SM,N}$. Which exact submodules that should be switched from disabled to the enabled mode in the arm can be determined by the converter inner controller and is nowadays mainly determined in literature by the converter voltage balancing controllers and the amount of submodules that should be inserted and the voltage of each submodule v_{sm}:

$$GS\left(SM_1, SM_2, ..., SM_N\right) = f\left(n_{ins}, v_{sm,1}, v_{sm,2}, ..., v_{sm,N}\right) \tag{5.1}$$

With the condition monitoring algorithms presented in the previous chapters, the remaining useful lifetime of all IGBT devices in every submodule can be estimated. This allows the extension of the arm inner controllers with lifetime optimization controllers utilizing maintenance window availability. Due to the large-scale offshore deployment of MMC and the over-stressed electricity grid as a result of the energy transition, these maintenance windows are becoming shorter and should be considered in the

converter control methodology. If a submodule in a converter operating in inverter mode has an IGBT device with reduced remaining useful lifetime and a maintenance window is available, it could be beneficial to bypass this submodule more frequently (increasing P_{sw} at *T2*) such that it breaks exactly when the maintenance team arrives. By bypassing the specific submodule more frequently, other submodules need to be inserted less frequently (decreasing P_{sw} at *T2*) and therefore have a longer estimated remaining useful lifetime. To make sure that the submodule breaks at the start of the maintenance window, the insertion frequency difference is an important element of this control aspect. Hereby, the individual submodule gate signals change to a function of both the submodule voltages and the IGBT condition indicators $v_{ce,on}$:

$$GS\left(SM_1, SM_2, ..., SM_N\right) = f\left(n_{ins}, v_{sm,1}, v_{ce,on,1}, v_{sm,2}, v_{ce,on,2}, ..., v_{sm,N}, v_{ce,on,N}\right) \tag{5.2}$$

The novel inner control structure considering lifetime optimization and single-arm capacitor voltage balancing processes is outlined in the following sections. First, the gate-pulse generation mechanisms used in a conventional MMC is outlined such that the proposed controller is compatible with preferred modulation techniques used in practice.

5.3. Gate-Signal Generation

A MMC is not able to exactly follow $u_{ref}\left(t\right)$ as the modular capacitors limit the AC output to discrete voltage levels. Pulse Width Modulation (PWM) is used to select the switching of individual devices such that a short-time average of the discrete voltage levels coincides with the short-time average of u_{ref} [54]. The most suitable modulation methods in MMC can be classified into carrier-less and carrier-based PWM [55]. The carrier-based modulation is mainly segregated into level-shifted PWM and phase-shifted PWM.

Nearest Level Control Carrier-less has its most straightforward modulation method with nearest level control which does not use any carrier modulation signal. A reference sinusoidal waveform is divided by the DC link voltage and rounded to an integer that determines how many submodules should be inserted,

$$n_{ins} = \text{round}\left(\frac{V_{ref}}{V_{DC}}\right) \tag{5.3}$$

$$\text{round}\left(x\right) = \begin{cases} \text{floor}\left(x\right), & x < \text{floor}\left(x\right) + 0.5 \\ \text{ceil}\left(x\right), & x \geq \text{floor}\left(x\right) + 0.5 \end{cases} \tag{5.4}$$

with $floor\left(x\right)$ determining the largest integer lower than x and $ceil\left(x\right)$ indicating the lowest integer higher than x [54]. This two-sided rounding improves sinusoidal reference tracking compared to single-sided rounding. Subvariants of this method are random NLC, where it is randomly chosen which specific submodule to insert, and flat-topped modulation. The triplen-series is used in flat-toppled modulation to fully utilize the DC voltage [56]. This reduces the zero-sequence component of the converter-side current and is critical for converter-transformer earthed systems. In order to balance the individual submodule voltages, a balancing algorithm is needed.

The conventional capacitor voltage balancing algorithm usually sorts the capacitor voltages based on unbalance factor γ at different voltages [57],

$$\gamma = \frac{\Delta U_{c,max}}{U_{c,rated}} = \frac{U_{c,i} - U_{c,rated}}{U_{c,rated}}, \tag{5.5}$$

in which sorting algorithms such as quick-sort and bubble-sort can be used. The capacitor voltage balance sorting method results in a switching frequency difference between submodules in an arm and therefore different strategies can be used. The sorting algorithm requires a centralized voltage balancing control system sending the gate pulses which could be computationally expensive for a large-scale MMC with hundreds of submodules. In practice, capacitor voltages are obtained using individual voltage sensors, called capacitor position voltage sensors, at each submodule. If the arm current is positive, meaning the current will flow into the positive capacitor terminal of an enabled submodule, the submodules with a low capacitor voltage $(\min\left(\gamma\right))$ will be inserted first while for a negative current, the submodule with the highest capacitor voltage $(\max\left(\gamma\right))$ will be inserted first.

The switching frequency significantly affects the efficiency of this algorithm. A higher switching frequency allows for more precise capacitor charging and discharging, while on the other hand, the converter power losses increase for a higher switching frequency.

Level Shifted-PWM The rounding used by carrier-less methods causes an output voltage mismatch resulting in carrier-based modulation being the preferred modulation technique in traditional MMC. All submodules are controlled individually in Level Shifted-PWM by a modulator that compares a carrier waveform (e.g. triangular) to the arm reference voltage u_{ref}.

Level-Shifted PWM has its carrier signals belonging to the submodules in an arm shifted in height, meaning there is an amplitude offset between the carriers. The individual carrier signals are compared to the arm voltage reference signal and a firing gate-pulse is generated if the carrier is e.g. higher in amplitude than the reference signal. The converter arm current (3.3) is out-of-phase with θ from the converter arm voltage (3.5), and every submodule is inserted repeatedly at different time instants, resulting in submodules exposed to different operating conditions. This means the vertical offset between individual submodule carrier signals causes submodules to degrade unequally.

Phase-Shifted PWM In Phase-Shifted PWM the carrier signals that belong to submodules in one arm are all shifted $2\pi/N$ in phase to each other and have amplitude V_{dc}/N. Gate pulses are generated by comparing the carrier signals with the arm voltage reference signal. If the carrier signal amplitude is e.g. lower, the gate-pulse of the subsequent submodule top-level IGBT *T1* is fired. This method allows for evenly distributed switching losses between the submodules and balanced capacitor voltages in the arms if the switching frequency is not equal to a harmonic of the AC system frequency [58].

In order to balance the capacitor voltages, a carrier rotation balancing strategy was proposed by Bai et al. that does not need an external sorting algorithm and thus reduces the computational burden [59]. Here, carriers are periodically interchanged between submodules such that each submodule conducts an even current over a larger time interval. Although the carrier-based insertion algorithm is decentralized, a rotary balancing algorithm requires a centralized controller or extra control signals from the distributed gate control units. An example of two submodules controlled with Phase-Shifted PWM is shown in Figure 5.2, where it is clearly shown both submodules switch two times to enabled mode in a 50 Hz fundamental AC-system period.

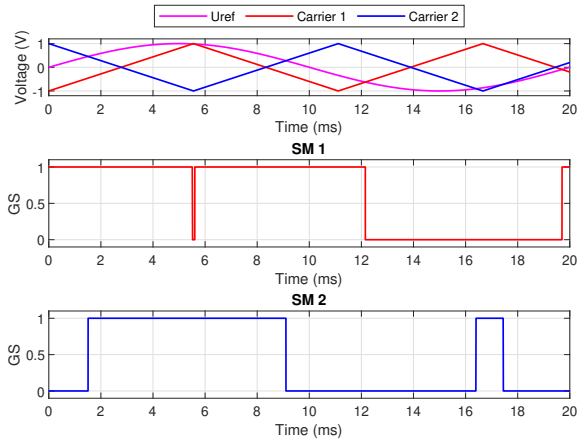


Figure 5.2: Illustration of two submodules controlled with PS-PWM in converter connected to an 50 Hz AC-system.

5.4. Methodology

The proposed lifetime-optimization controller should take the next available maintenance window into consideration and reconfigure the submodule insertion indices to switch the submodule with the least healthy IGBT device more frequently to enabled mode such that this affected component in the submodule breaks at the start of the next maintenance window. This ensures the submodule is replaced with

the least possible remaining useful lifetime resulting in other submodules being inserted less frequently. Other submodule semiconductor devices therefore have lower power losses, experience less mechanical stress, and their remaining useful lifetime is longer. The methodology should be compatible with the existing gate-signal generation techniques nearest-level control, level-shifted PWM, and phase-shifted PWM. First, the ON-state collector-emitter voltage measurement aggregation is discussed whereafter two possible lifetime optimization insertion techniques are compared.

5.4.1. Signal processing

The ON-state collector-emitter voltage of each IGBT device can be measured, implying there are two measurements per half-bridge configured submodule and N_s measurements in a converter arm. Signal processing is needed to determine which measurement to consider in a submodule and subsequently to estimate the relative ageing between the submodules in an arm. First, the aggregation on submodule level is explained whereafter the arm aggregation is outlined.

Submodule aggregation The condition monitoring methodology for IGBTs was described in the previous chapters. This algorithm uses the ON-state collector-emitter voltage of the IGBTs. In every submodule there are two IGBT devices in a half-bridge configuration while individual devices can not be replaced; if a single IGBT device fails, the whole submodule is faulted. This means the highest IGBT ON-state collector-emitter voltage determines the remaining useful lifetime of a submodule. This can be either the highest predicted ON-state collector-emitter voltage of these devices $\max\left(v_{ce,on}\right)$ at the time-to-maintenance t_m,

$$v_{ce,on} = \max\left(v_{ce,on}\left(t_m\right), f_{C1}\left(t_m\right)\right), \tag{5.6}$$

or taken as the highest voltage at the time instant of assessment t_x;

$$v_{ce,on} = \max\left(v_{ce,on}\left(t_x\right), f_{C1}\left(t_x\right)\right). \tag{5.7}$$

As it was shown in section 3.2 that the operational conditions of the MMC have a significant influence on the power losses of the individual devices and so the component's degradation rate, estimation of the remaining useful-lifetime of any device including operational conditions (5.6) is extremely hard and requires accurate converter operation estimations, further depending on external factors such as weather data if the converter is connected to a renewable energy resource. The MMC lifetime should be at least forty years as specified by TSO TenneT which requires the operational estimations to be of the same time span. Because precise operational condition estimations are extremely difficult for multiple years, it is considered to be unrealistic. As a result, the IGBT device with the highest ON-state collector-emitter voltage in a submodule at the time instant of assessment (5.7) is determined to indicate the submodule remaining useful lifetime.

In Figure 5.1, it was shown that *T2* and *D2* experience the highest power losses in a half-bridge submodule configuration during both inverter and rectifier operation mode. The significant difference with *T1* and *D1*, and the fact that replacement of individual IGBTs inside submodules is not possible, means that only *T2* shall be monitored implying that *T2* inside a submodule determines the complete submodule remaining useful-lifetime at the time-of-assessment $v_{ce,on}\left(t_x\right)$.

Arm aggregation After the ON-state collector-emitter condition indicators at specific time instants are generated in *T2*, the measurements should be aggregated between every submodule in the converter arm for all devices being equal and fail at the same threshold for ON-state collector-emitter voltage deviation. This assumption is justified by the fact that manufacturers only start the IGBT production process after the production line is calibrated and sample devices show characteristics in between extremely tight boundaries. This indicates the relative ageing between submodules and is computed using,

$$v_{ce,on,av} = \frac{1}{N_{SM}} \sum_{i=1}^{N_{SM}} v_{ce,on}\left(i\right), \tag{5.8}$$

and depends on the total number of submodules in an arm N_{SM}. It is important to consider the total number of submodules in the arm as the lifetime optimization controller should operate on arm level because the controller is determined to act within the internal energy exchange controller in a single

converter arm process. The submodule condition indicators in an arm can now be sorted using a new vector,

$$\delta = \frac{\Delta V_{ce,on}}{V_{ce,on,av}} = \frac{V_{ce,on,i} - V_{ce,on,av}}{V_{ce,on,av}}, \tag{5.9}$$

such that the condition indicators are based on the relative submodule condition in an arm. Similar to the arm voltage deviation vector γ, vector δ can be sorted using algorithms such as quick-sort or bubble sort. This allows MMC manufacturers to use existing software building blocks in the control system for simplified extendability and reduced costs in implementing a lifetime optimization control approach.

During the arm level aggregation process, *T2* ON-state collector-emitter voltage measurements could differ between submodules while the internal devices are exactly equal and have identical health. This is a result of the sinusoidal arm current and the difference in insertion time instants; if a submodule is inserted during peak current, it will have a lower ON-state collector-emitter voltage measurement compared to a submodule that is bypassed during the peak current while the *T2* devices are exactly equal. This generally occurs if the modulation index is lower than one as is illustrated in Figure 5.3

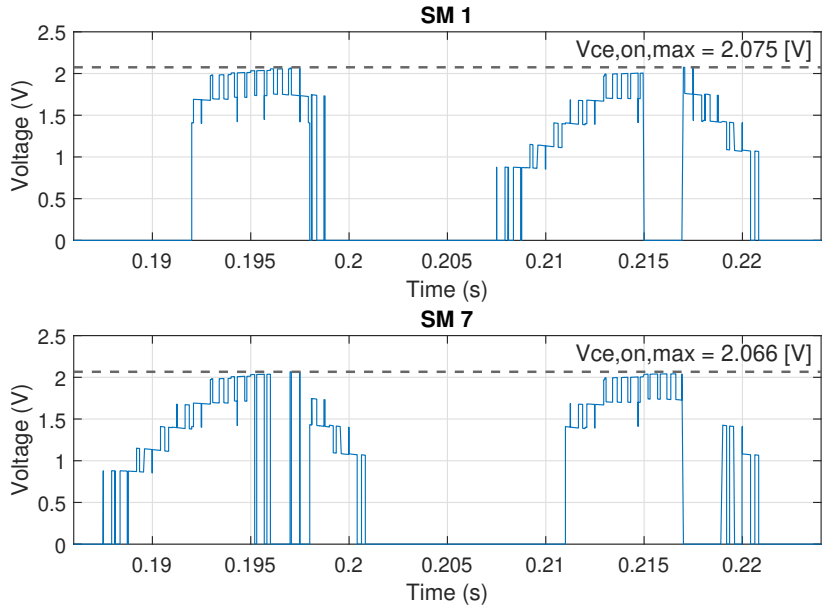


Figure 5.3: Illustration of the $v_{ce,on}$ measurements of two submodules in the same converter arm. The arm consists of 8 submodules and the modulation index is 0.8.

Here submodule 1 is seen with a higher measured ON-state collector-emitter voltage compared to submodule 7. The first submodule is bypassed during the peak of the arm current, meaning there is an ON-state collector-emitter voltage measurement at *T2*, while the other submodule is enabled during this time instant, meaning there is no ON-state collector-emitter voltage measurement at *T2*. Therefore, it is necessary to approximate the complete non-linear ON-state collector-emitter voltage over multiple AC fundamental frequency cycles before vector δ can be created, where the accuracy is determined by the approximation window size. A measurement approximation for the simulated converter arm with 8 submodules is illustrated in Figure 5.4.

The single-term non-linear approximation method has been used in the example. Obviously, if only measurements from an estimation window size of $50\,\mathrm{s}$ have been used, emphasis is on the lower and higher collector-current samples, such that the curve is not representing the real ON-state collector-emitter voltage of this device. When the estimation window size is prolonged to $150\,\mathrm{s}$, more measurements are available over the complete collector-current range, and the accuracy is assumed sufficient since all measurements coincide with the approximated non-linear characteristic. More research is needed to determine the effect of the estimation window length and to study different techniques such as moving minimum or maximum windows. It is important to note the junction temperature effect adds a third dimension to the estimation approach which will require even larger estimation windows. Research to the estimation window is considered out of scope and the exact behaviour is excluded in this

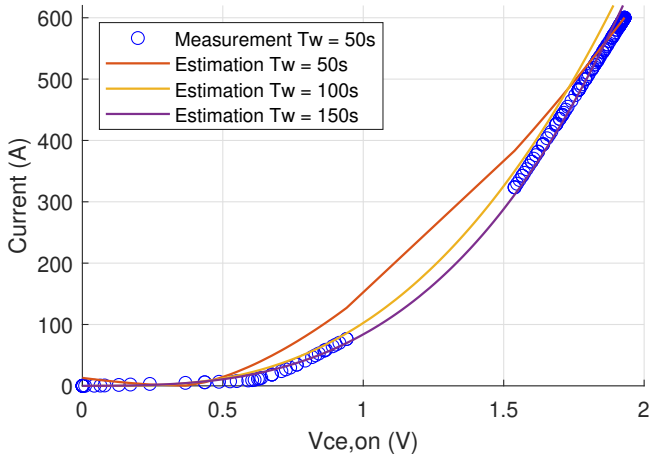


Figure 5.4: Dynamic estimation curve-fitting analysis for the ON-state collector-emitter voltage of a submodule.

research. From the example illustration it can only be concluded that the estimation window should be multiple orders higher compared to the fundamental AC-frequency period and real-time estimations are thus not possible. The lifetime controller should rely on inputs that are delayed.

5.4.2. Insertion techniques

There are in general two approaches to include lifetime optimization in the submodule insertion algorithm based on *T2* ON-state collector-emitter voltage measurements. The first makes use of the rotational carrier method while the second adjusts the sorting vector generated in the arm capacitor voltage balancing controller.

Rotational carrier Level-shifted PWM has its carriers shifted with a vertical offset, causing the submodules to be switched with an unequal average insertion time. The submodule level shift affects the ageing of submodules relative to each other and is therefore useful for a lifetime-optimization controller. Depending on the submodule degradation condition indicator, a rotational carrier algorithm can be used to rotate the level-shift of the individual submodules. If a submodule should be inserted more frequently, a carrier signal with more frequent insertion can be appointed to this submodule. This requires the need of a rotational ON-state collector-emitter voltage-dependent submodule balancing strategy compared to existing methods applicable for the voltage balancing process. A possible implementation of the rotational LS-PWM method is depicted in Figure 5.5. Each submodule sends the ON-state collector-emitter voltage of *T2* to the data-processing unit which aggregates the measurements to arm-level and creates vector δ. This vector is sent to the carrier rotation mechanism together with the voltage balancing vector β whereafter the individual carrier offset is determined for each submodule. The modulator finally generates the gate signals for each submodules based on the comparators with the reference voltage for each arm.

Extended sorting Similar to the conventional capacitor sorting algorithm presented, it would be possible to implement a sorting algorithm based on δ after sorting is performed on γ. This means the sorting process is extended and now based on two parameters where both are decoupled such that parallel sorting is possible. Because the capacitor voltages are also sorted but on a different metric, extending the sorting with remaining useful lifetime can imbalance capacitor voltages and disrupt normal operation. Therefore, the starting point shall be sorting the capacitor voltages in subsequent order depending on the arm current. The submodules at the far ends in the resulting vector have either the highest priority to be inserted or to be bypassed. The submodules in the middle of the resulting sorted vector have relatively more freedom to be re-assigned in priority before they exceed their allowed voltage tolerance $u_{sm} \pm \Delta U_{sm}/2$. A selection window can be used that takes a number of selected submodules in the middle of γ and re-arranges them in subsequent order according to sorting of the ON-state collector-emitter voltages.

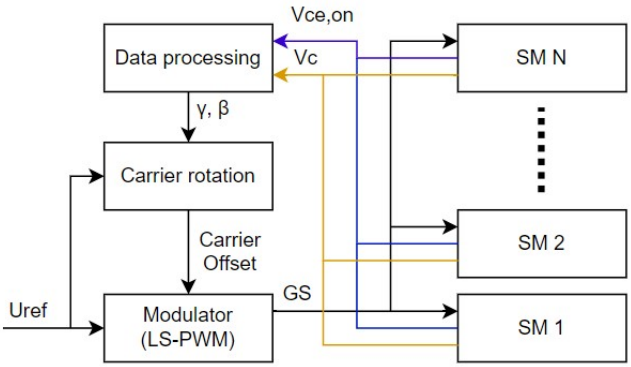


Figure 5.5: Block diagram of the rotational carrier method including capacitor voltage balancing and lifetime optimization control methodology.

An implementation diagram of the extended sorting methodology is depicted in Figure 5.6. First, each submodule sends the measurements of $v_{ce,on}$ and v_c to the data processing unit where γ and δ are formed. A selection window is subsequently determined in a selector unit wherein part of the gate signal vector is formed based on γ. This vector has a size of the selection window boundaries while the remaining part is directly taken from δ for capacitor voltage prioritization.

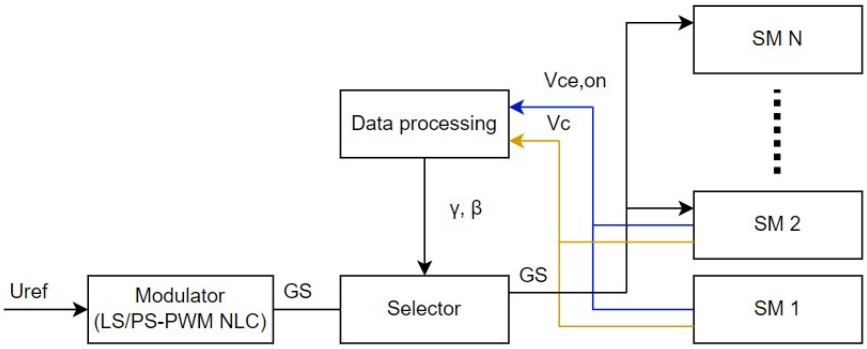


Figure 5.6: Block diagram of the extended sorting method including capacitor voltage balancing and lifetime optimization control methodology.

Selection Two methods were presented where both use the sorted vectors γ and δ as specified in the sorting function. The rotational carrier method is relatively straightforward to implement since the methodology has already been described in the literature but for a different purpose. A significant disadvantage here however is the method is only applicable for level shifted PWM controlled submodules. The extended sorting method is more complex to implement since there are no references available yet. The advantage of this method is its applicability to all three mentioned modulation techniques. As a result, the extended sorting methodology has been chosen as the insertion technique used for including lifetime optimization in the arm energy exchange balancing process. The implementation and analytical selection window setting is outlined in the following section.

5.5. Analytical Approach

A generic flow diagram of the extended sorting algorithm applied on a converter arm with eight submodules and a selection window of four submodules is depicted in Figure 5.7.

It can be seen in the present arm current direction, submodule 4 has the highest priority to be inserted according to assure capacitor voltage balance over the submodules. The selection window is set to length four, such that submodule 3, 1, 6, and 2 can be re-appointed according to which submodule has the most priority according to the ON-state collector-emitter voltage balancing. Here, submodule 3 has the highest priority to be inserted more frequently. After re-arranging the submodule priority inside

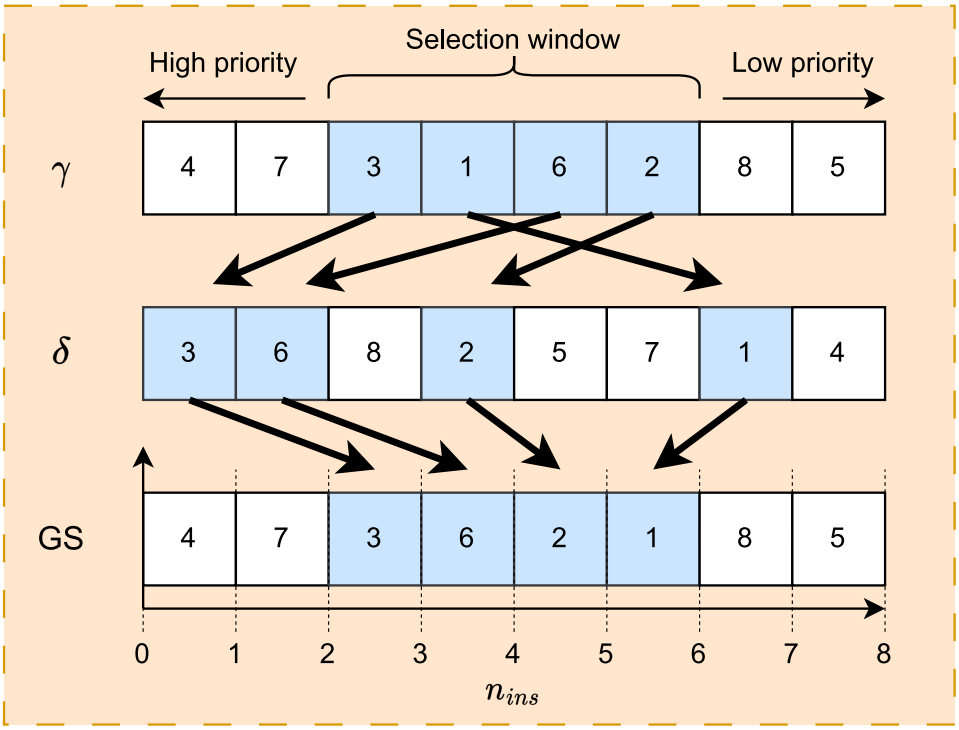


Figure 5.7: Extended sorting methodology with capacitor voltage balance vector γ and ON-state collector-emitter vector δ. Based on the selection window, the final gate signal (GS) vector is generated and based on n_{ins}, a number of submodules are switched to enabled mode.

the selection window, the resulting gate signal vector indicates from left to right which submodule should be inserted first.

In order to insert these submodules according to the reference waveform and modulation strategy, first the number of submodules that should be switched to enabled mode are obtained at each time instant independently of the modulation strategy. This can be done by comparing the reference with the modulation strategy used for each submodule and adding the result together forming n_{ins}. Sorting this vector in the same order as the insertion priority vector, element-wise multiplication can be used to generate the gate pulses for the submodules.

5.5.1. Selection window determination

The objective of the improved sorting methodology in inverter mode is to increase ΔT_j by generating higher losses in *T2* for a selected submodule under the condition that these losses are reduced in other submodules. This implies the selected submodule is bypassed as long as possible (increasing P_c) and switched as much as possible (increasing P_{sw}) such that other submodules do not need to be bypassed or switched in order to generate the desired arm voltage.

In section 4.2.2 it was outlined that the junction temperature T_j of a semiconductor in MMC increases from the instant when this semiconductor starts conducting in a half-wave current cycle till the instant 75 % of the half-wave cycle has passed; the last 25 % of the half-wave current cycle the junction temperature will decrease. For *T2* in inverter mode, the semiconductor conducts if the arm current is positive such that these time instants can be determined,

$$\begin{aligned} t_{a,i} &= \frac{1}{\omega_N}\left[-\theta - \sin^{-1}\left(\frac{1}{k}\right) + 2\pi\left(1+K\right)\right] \\ t_{b,i} &= \frac{1}{\omega_N}\left[-\theta + \sin^{-1}\left(\frac{1}{k}\right) + \pi\left(1+2K\right)\right], \end{aligned} \tag{5.10}$$

as a function of the angular fundamental AC frequency ω_N, phase angle θ, and current index k. The

$75\,\%$ boundary where the maximum T_j occurs can thus be written:

$$t_{b,max} = \frac{t_{a,i} + 3t_{b,i}}{4} \tag{5.11}$$

If the respective submodule is bypassed this entire period, conduction energy losses E_c are generated in *T2* and can be calculated by the instantaneous value,

$$E_c = \int_{t_a}^{t_{b,max}} V_{ce,on}[1 + k\sin(\omega_N t + \theta)]\frac{I_{DC}}{3}dt, \tag{5.12}$$

in case $v_{ce,on}$ is treated as constant. Another approach is to multiply the average conduction power losses of *T2* with the time of conduction $\Delta t = t_{b,max} - t_{a,i}$. Here, $v_{ce,on}$ can be approached as being linear with current as used in (3.18).

The reference arm voltage determines how many submodules should be enabled. For the upper-arm $u_{au}(t)$ as example, the number of submodules enabled in this arm,

$$N_{su}(t) = \frac{N_s}{2} - \frac{mN_s}{2}\sin(\omega_N t) \tag{5.13}$$

is a function of the modulation index m, the total number of submodules N_s in this arm (even number), and the angular fundamental system frequency ω_N. It is important to note N_{su} is the short-time average value of n_{ins} which is further explained using Figure 5.9; there is a ripple seen over N_{su} which is represented by n_{ins}. The selection window boundaries are integers significantly in between $\{0, N_s\}$ such that the highest priority is given to the capacitor voltage balancing process. Because the arm current $i_{au}(t)$ is $180\,$deg out-of-phase with the number of submodules that should be enabled in an arm $N_{su}(t)$, the selection window starts when the arm-current is increasing and $N_{su}(t)$ is decreasing as illustrated in Figure 5.8.

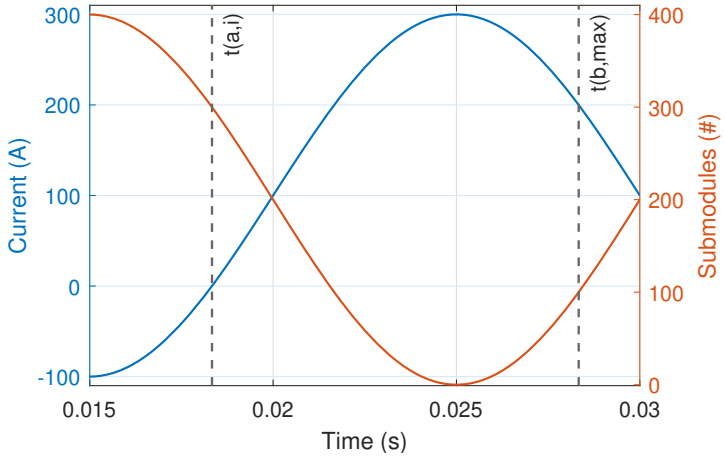


Figure 5.8: Illustration of arm current and N_{su} during the selection window with a converter arm consisting of 400 submodules and modulation index unity. It should be noted there is no ripple (n_{ins}) shown over N_{su}.

In the illustration, it is shown in between $t_{a,i}$ and $t_{b,max}$ the inner controller should change the insertion vector such that the most losses occur in the selected submodule *T2* device causing increased ΔT_j such that other submodules have reduced losses and a lower ΔT_j in their *T2* device.

The insertion vector $\{0, N_s\}$ has a selection window with lower boundary B_l and upper boundary B_u where it holds that $(0 < B_l < B_u < N_s)$. Both B_l and B_u could be even or odd integers. The ratio J_L given $(B_u - B_l)/N_s$ defines the freedom the controller has to move losses from any submodule to the selected submodule, whereas the ratio $(N_s - B_u + B_l)/N_s$ defines the remaining freedom for the inner arm capacitor voltage balancing. Both boundaries also define at which time instant the controller can

start with interchanging insertion indices and when it stops. These time instants can be calculated as:

$$\begin{aligned} t_{a,W} =& \frac{1}{\omega_N}\left[-\sin^{-1}\left(\frac{N_s-2B_l}{mN_s}\right)+\pi\left(1+2K\right)\right] \\ t_{b,W} =& \frac{1}{\omega_N}\left[-\sin^{-1}\left(\frac{N_s-2B_u}{mN_s}\right)+\pi\left(1+2K\right)\right] \end{aligned} \tag{5.14}$$

From here it can be directly noticed that $t_{b,W} < t_{b,i}$, meaning $t_{b,W}$ defines the end of the selection window in time domain. The start of the selection window in time domain is defined by the maximum of $t_{a,W}$ and $t_{a,i}$. With the boundaries set, the ripple over N_{su} can be studied. The decreasing part of $n_{ins}(t)$ as resulting from phase shifted-PWM modulation, thus including the ripple, together with the increasing arm current $i_{au}(t)$ is shown in Figure 5.9.

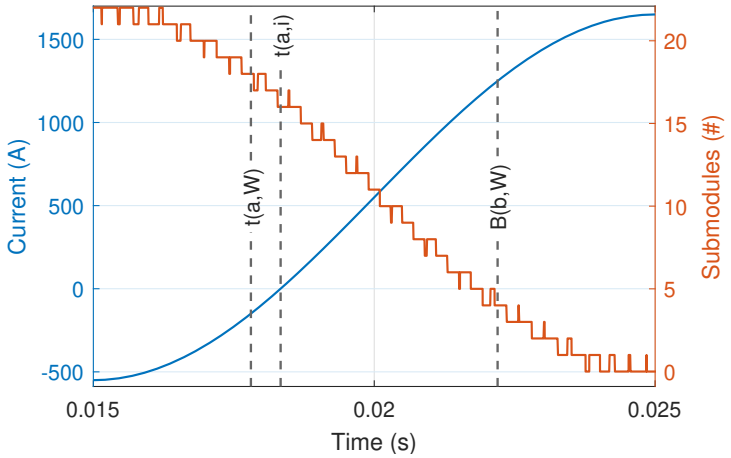


Figure 5.9: Illustration of arm current and n_{ins} with time boundaries equal to the selection window. The arm has 22 submodules, B_l is 4, B_u is 18, I_{dc} is 1.65 kA, theta is assumed zero, and the submodule switching frequency is 150 Hz.

The time window where the controller can act for interchanging vector indices is shown to be $t_{a,i}$ - $t_{b,W}$ in this example. If the arm current $i_{au}(t)$ would horizontally offset by at least $t_{a,i}$ - $t_{a,W}$ seconds (phase-shift θ), the lower boundary is determined by $t_{a,i}$. The fluctuations of N_s over the plane staircase function in this time window determine how many times the selected submodule can be switched from disabled mode to enabled mode. There are seven switching actions possible during the selected time window in the illustration.

5.5.2. Loss component optimization

When a submodule is switched to enabled mode during a ripple instant over the plane staircase function, the conduction losses P_c in *T2* decrease as only *D1* conducts if the submodule is enabled and the arm current is positive. This means that the higher the submodule switching frequency, the lower the conduction losses in *T2*. In order to calculate the reduction in conduction losses, the carrier waves should be studied as no plane function could be found in literature describing the time duration of the ripple as a function of the switching frequency and the number of submodules.

The triangular carriers in phase shifted PWM can be written as periodical linear functions,

$$\begin{aligned} C_u\left(t\right) =& 2N_s f_{sw}\left(t-\frac{K}{f_{sw}}-\frac{i}{f_{sw}N_s}\right) \\ C_d\left(t\right) =& N_s - 2N_s f_{sw}\left(t-\frac{K}{f_{sw}}-\frac{i}{f_{sw}N_s}\right), \end{aligned} \tag{5.15}$$

where integer *K* indicates the switching frequency period number and integer *i* represents the submodule phase shift number ($0 < i < N_s$). The carrier belonging to the first submodule has no phase-shift ($i = 0$), whereas the carrier belonging to the second submodule is phase shifted with $1/(f_{sw}N_s)$, meaning $i = 1$. This process repeats itself till the carrier of submodule N_s is phased shifted with $i = N_s - 1$.

For the next period, $K = 1$ and $i = 0$ again. For simplicity, $(K/f_{sw} - i/(f_{sw}N_s))$ can thus be altered to $i/(f_{sw}N_s)$ due to these periodical properties.

If the submodule switching frequency is at least twice an integer multiple of the fundamental system frequency, two important things can be noticed in the selection window $\{B_l, B_u\}$:

- The intersection of an upwards carrier waveform $c_u(t)$ with the short-time average arm voltage reference waveform $N_{su}(t)$ causes n_{ins} to drop by exactly one submodule.
- The intersection of a downwards carrier waveform $c_d(t)$ with the short-time average arm voltage reference waveform $N_{su}(t)$ causes n_{ins} to rise by exactly one submodule.

This means that during the decreasing N_{su} in the operating window time frame ($t_{a,W/i}$ - $t_{b,W}$), the intersection with downward periodical carriers initiates a ripple over the plane decreasing staircase function. The intersection time instant defining the start of the ripple,

$$\frac{N_s}{2} - \frac{mN_s}{2}\sin\left(w_n t_{start}\right) = N_s - 2N_s f_{sw}\left(t_{start} - \frac{i}{f_{sw}N_s}\right), \tag{5.16}$$

cannot be solved algebraically and should therefore be solved numerically. The first subsequent intersection of an upwards carrier waveform $c_u(t)$ defines the end of this ripple over the plane decreasing staircase function:

$$\frac{N_s}{2} - \frac{mN_s}{2}\sin\left(w_n t_{end}\right) = 2N_s f_{sw}\left(t_{end} - \frac{i}{f_{sw}N_s}\right) \tag{5.17}$$

However, the periodic properties of the linear carrier notation give infinite intersections while only the intersections in between ($t_{a,W/i}$ - $t_{b,W}$) are of necessity for interchanging insertion indices. Therefore, *i* should be a vector with a length of the number of intersections starting from the first carrier with horizontal offset i_s till the last crossing carrier with horizontal offset i_e. For the downward carriers, these instances can be calculated using,

$$\begin{aligned} i_{d,s} &= \left\lceil N_s f_{sw}\left(t_{a,W/i} - \frac{N_s + N_s m\sin\left(w_n t_{a,W/i}\right)}{4N_s f_{sw}}\right)\right\rceil \\ i_{d,e} &= \left\lfloor N_s f_{sw}\left(t_{b,W} - \frac{N_s + N_s m\sin\left(w_n t_{b,W}\right)}{4N_s f_{sw}}\right)\right\rfloor, \end{aligned} \tag{5.18}$$

while for the upwards carriers, these instances can be computed in a similar way but by replacing the c_d function part with the function from c_u in (5.18).

Comparison A comparison between the estimated ripple time-instantons using the presented analytical approach and a MATLAB/Simulink simulation has been made. The number of submodules in the arm is 22, with a selection window lower boundary B_L of 7 and a selection window upper boundary B_u of 15. This means the lifetime optimization loss transfer freedom coefficient J_L equals $(15-7)/22 = 0.4$ while the remaining capacitor voltage balancing coefficient J_c equals $(22-15+7)/22 = 0.6$. The modulation index *m* is 1, while the DC-current I_{dc} is set 1.5 kA. These instants define the submodule selection window instants as explained in section 5.5.1. The submodule switching frequency f_{sw} is set 150 kHz and the AC phase-shift θ is assumed to be zero. The results are depicted in Figure 5.10.

It is clearly seen that the estimated ripple initiation and ending time instants are very accurate to the MATLAB/Simulink simulation. This means the ripple estimation methodology functions sufficiently and could further be used to estimate the loss difference and finally analyse the effect of all parameters to the *T2* junction temperature fluctuation.

5.5.3. Energy loss transfer

The difference between each pair of (t_{end} - t_{start}) defines exactly the time duration that conduction losses are dissipated in *D1* instead of in *T2* for the selected submodule. In between these pairs, *T2* experiences conduction losses. In order to calculate those conduction losses, the average and RMS-squared

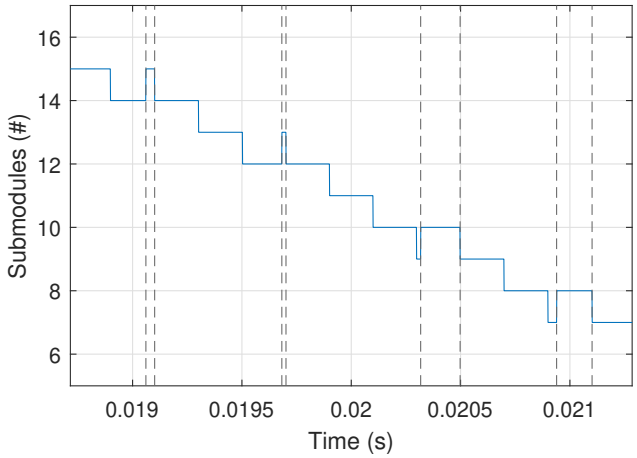


Figure 5.10: Comparison of the analytical estimation of the ripple instants in dotted lines with the MATLAB/Simulink n_{ins} simulation during the complete submodule indice interchanging interval, implying the selection window in the time domain.

currents through *T2* in those time windows can be computed,

$$\begin{aligned} I_{T2,av} &= \frac{1}{t_{start,i+1} - t_{end,i}} \int_{t_{end,i}}^{t_{start,i+1}} \left[1 + k \sin\left(\omega_n t + \theta\right)\right] \frac{I_{dc}}{3}\, dt \\ I_{T2,rms}^2 &= \frac{1}{t_{start,i+1} - t_{end,i}} \int_{t_{end,i}}^{t_{start,i+1}} \left[1 + k \sin\left(\omega_n t + \theta\right)\right] \frac{I_{dc}}{3}\, dt, \end{aligned} \tag{5.19}$$

with which the conduction losses in these periods ($t_{end,i}$ - $t_{start,i+1}$) can be solved using (3.18). Another approach is to subtract the average conduction losses in (3.18) with average current boundaries ($t_{start,i}$ till $t_{end,i}$) in (5.19) from the conduction losses computed in (5.12) where it is assumed no switching action takes place.

For the switching energy losses in the time window the controller should interchange insertion indices ($t_{a,W/i}$ - $t_{b,W}$), the average current through *T2* during each switching action should be estimated. In this case the time boundaries for $I_{T2,av}$ in (5.19) should be adjusted to $t_{start,i}$ and $t_{end,i}$ as a single ripple duration over the plane staircase function is normally very small and the average current through *T2* during switching from disabled to enabled mode can be assumed to be identical to the average current through *T2* during switching to disabled mode again. The resulting switching energy losses in the time window can finally be calculated using a discrete summation:

$$E_{sw} = \left(E_{on} + E_{off}\right) \frac{U_{cx}}{U_{ref,T}} \sum_{j=1}^{length(i_{d,s})} \frac{\left|I_{T2,av}\left(j\right)\right|}{I_{ref,T}} \tag{5.20}$$

The trade-off between switching as much as possible and completely bypassing the selected submodule in order to generate more losses in the selected submodule can now be examined. For the analysis, the *5SNA 1500E330305* and the *5SNA 3000K452300* Hitachi Energy IGBT devices are studied. The subsequent characteristics of those devices are indicated in Table 5.1.

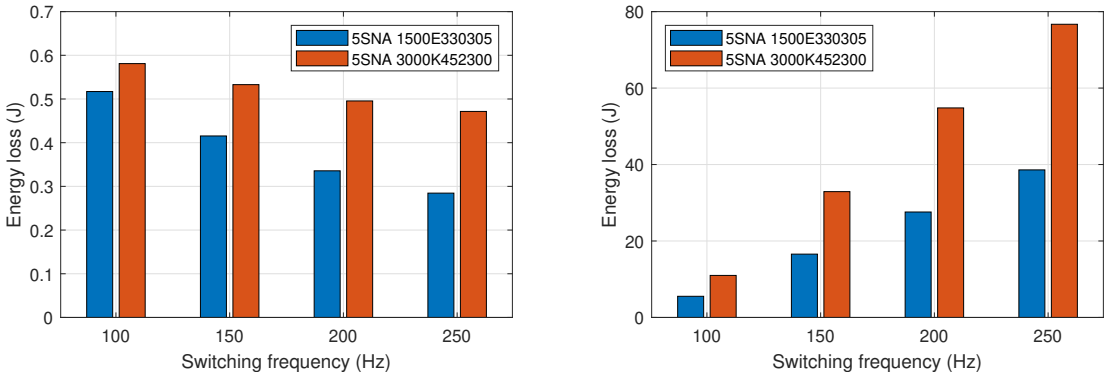
Table 5.1: Relevant specifications of the IGBT devices used in the analysis.

IGBT Device	U_0 [V]	$r_{0,t}$ [mΩ]	E_{on} [J]	E_{off} [J]	$U_{ref,T}$ [kV]	$I_{ref,T}$ [kA]
5SNA 1500E330305	3.1	2.0	2.15	2.80	1.8	1.5
5SNA 3000K452300	1.6	0.67	15.5	15.1	2.8	3.0

It is important to note that the two studied devices differ significantly in characteristics. While the *5SNA 1500E330305* IGBT device has switching losses (E_{on} + E_{off}) equal to 15.4 J, with the loss measurement references linearly scaled to $U_{ref,T}$ is 2.8 kV and $I_{ref,T}$ equal to 3.0 kA, these energy losses

are a factor of two higher (30.6 J) for the *5SNA 3000K452300* IGBT device. The reason is the *5SNA 1500E330305* IGBT device is an older technology and was developed when the switching frequency applied in VSC was relatively higher. Nowadays the switching frequency has decreased significantly, making the switching losses less relevant and the conduction losses dominating. This means the IGBT semiconductor design is now focused on optimization for different characteristics such as the conduction losses. This can further be seen in the characteristic differences of U_0 and $r_{0,t}$, both are namely significantly lower for the *5SNA 3000K45230* IGBT device.

Both IGBT devices are used in an MMC operating in inverter mode with submodules in half-bridge configuration. There are 200 submodules per arm (N_s) whereas each submodule capacitor is rated 2 kV. The DC-current I_{dc} equals 1.5 kA, defined by the upper limit of the older *5SNA 1500E330305* IGBT device conduction current rating and the converter is assumed to be operating in steady-state. The lifetime optimization controller selection lower limit B_l is set to 90 while the upper limit B_u is set to 110. This means the loss transfer freedom coefficient J_l equals $(110-90)/200 = 0.1$ while the remaining inner arm capacitor voltage balancing freedom coefficient J_C equals $(200 - 110 + 90)/200 = 0.9$. The resulting energy losses are shown in Figure 5.11.



(a) Conduction losses.

(b) Switching losses.

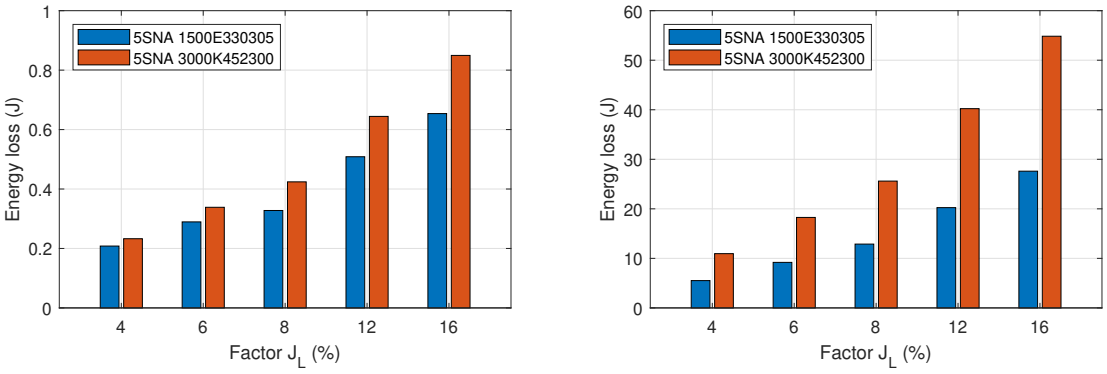
Figure 5.11: Comparison between the energy losses in *T2* during the lifetime optimization controller selection window for a converter arm with 200 submodules, B_l is 90, and B_u is 110 and 2 kV rated submodules.

It is obvious from the results that the conduction energy losses (Fig. 5.11a) are only a fraction of the switching energy losses (Fig 5.11b) for both IGBT devices during the lifetime optimization controller selection window $\{B_l, B_u\}$. This seems to contradict the semiconductor power loss estimations made in Chapter 3, where it was determined that the conduction power losses are higher compared to the switching power losses for *T2* configured in half-bridge with the MMC operating in inverter mode. However, this difference can be explained with the following arguments:

- During average power loss estimations, it was assumed *T2* switches exactly one time during each submodule switching frequency cycle. For the lifetime optimization controller, *T2* switches multiple times during each submodule switching frequency cycle increasing the switching energy losses.
- In the computation for the average power losses, the total energy loss during a switching action (E_{on} + E_{off}) was multiplied with the time period $1/f_{sw}$ of the submodule switching frequency. Since the activation time-period ($t_{a,W/i}$ - $t_{b,W}$) of the lifetime optimization controller is much shorter than $1/f_{sw}$, the switching energy losses contribute much more to the total energy loss in *T2*.

Further, it can be seen that a higher submodule switching frequency results in lower conduction energy losses in *T2*. This confirms the assumption that when a submodule is switched from disabled to enabled mode and the arm current $i_{au}(t)$ is positive, *D1* conducts instead of *T2* subsequently reducing conduction losses in *T2*. The more this process repeats itself (higher submodule switching frequency), the lower the conduction energy losses in *T2* will be. Since the submodule needs to be bypassed after every switching action to enabled mode, these losses will never drop to zero. An obvious opposite phenomenon can be seen for the switching energy losses; the higher the submodule switching frequency, the higher the switching energy losses in *T2*.

The effect of the selection window width (B_u - B_l), as defined in intersection freedom parameter J_L (%) as a function of the total number of submodules in an arm N_s and the selection boundaries has been studied. Here it is assumed the submodule switching frequency is fixed at 150 Hz and further converter and device parameters are identical to the previous study. The results for the generated energy losses in selected submodule IGBT *T2* are shown in Figure 5.12.



(a) Conduction losses.

(b) Switching losses.

Figure 5.12: Comparison between the energy losses in *T2* during the lifetime optimization controller selection window for a converter arm with 200 submodules, submodule switching frequency 150 Hz, and 2 kV rated submodules.

Here it is seen that the higher the freedom factor J_L, the more energy losses can be generated in the selected submodule IGBT *T2*. The most significant losses are in the switching energy losses, as also was emphasized in Figure 5.11.

5.5.4. Junction temperature effect

For the selected submodule where more losses have to be generated, the junction temperature fluctuation ΔT_j in *T2* should be estimated to assess the effect on the submodule remaining useful lifetime. The analysis will follow the thermodynamics expressions for temperature ripple as presented in Chapter 4. These formulations require the average power losses for *T2* in the selected submodule, which computation methodology was presented in Chapter 3. However, slight modifications have to be made to the average power loss computation since it was assumed that *T2* switches exactly one time during each submodule switching frequency cycle, whereas it switches multiple times during each cycle with a lifetime optimization controller.

This means the average switching power losses can not be estimated based on the energy losses during one switching cycle $(E_{on} + E_{off})$, scaled to the average current and blocking voltage through-of the IGBT device, divided by the time period of one switching cycle $1/t_{sw}$. Now, the device is assumed to switch one time due to its own carrier wave, and an amount of the total ripple n_r during the interchanging indices window (e.g. in Fig 5.10 n_r equals 4). As a result, the average switching power losses,

$$P_{sw} = (E_{on} + E_{off}) \frac{U_{cx} \left| I_{Tx,av} \right| f_{sw} (1 + n_r)}{U_{ref,T} I_{ref,T}}, \tag{5.21}$$

increase by the factor (1 + n_r). The total power losses in the selected submodule can similarly to Chapter 3 be computed using linear summation of average power switching losses and average power conduction losses (P_c + P_{sw}) in the device. A specific amount of submodule (n_r) does not switch in this time period as the selected submodule is used to execute these switching actions. In order to calculate the average power losses for these submodules, a very rough estimation can be made that these only consist of submodule conduction losses. In reality, there will be some switching losses as well since the lifetime optimization controller has a selection window that is shorter than the heating period of the device ($t_{a,i}$ - $t_{b,imax}$). The remaining submodules in the arm (N_s - n_r), are not affected by and thus have power losses as computed in Chapter 3.

Analysis has been done on an MMC configured with 200 half-bridge submodules per arm. The DC-current equals 1.5 kA whereas the modulation index is unity, submodule switching frequency is 150 Hz, and AC phase-angle is zero. The device used in the analysis is the *5SNA 3000K452300* Hitachi Energy

IGBT. The resulting average power losses and junction temperature swings for the selected submodule, remaining selection window submodules, and the rest of the submodules in the converter arm for three different loss coefficients are shown in the Table below.

Number of submodules	P_{av} [kW]	ΔT_j [K]	
1	7.34	4.01	$J_L = 6\%$
5	1.82	0.99	
194	2.74	1.50	
1	9.19	5.02	$J_L = 8\%$
7	1.82	0.99	
192	2.74	1.50	
1	10.1	6.03	$J_L = 10\%$
9	1.82	0.99	
190	2.74	1.50	

The selected submodule experiences the highest junction temperature ripple for all three J_L factors. The higher J_L is, the larger the selection window and thus the more submodules have a reduced junction temperature ripple. Whereas for J_L is $6\,\%$ only 5 submodules have a reduced junction temperature ripple, for J_L equal to $10\,\%$, already 9 submodules have a reduced junction temperature ripple and proves the initial assumptions of the influence of the selection window width of the number of switching actions that can be transferred.

5.6. Control System Implementation

The lifetime optimization controller can be implemented using control system blocks. A general overview of the control system is shown in Figure 5.13.

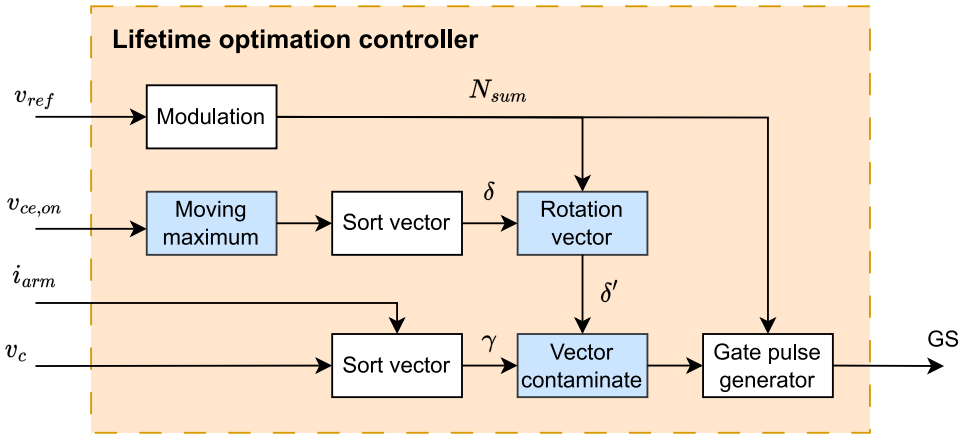


Figure 5.13: Control system implementation of the lifetime optimization controller with capacitor voltage balancing. Inputs are the condition indicators $v_{ce,on}$, arm current for sorting i_{arm}, capacitor voltages v_c, and arm reference voltage v_{ref}. The coloured blocks are further outlined in detail.

There are four inputs in the system. First, the ON-state collector-emitter voltages of *T2* from each submodule in the respective arm is needed are condition indicator. The arm-current is send to the vector sorting algorithm to determine the order of sorting. A positive arm current means the capacitor voltages should be sorted from the lowest voltage to the highest voltage, respectively from highest priority to lowest priority in γ. A negative arm current implies the sorting should be in opposite order; from highest capacitor voltage to lowest capacity voltage. The capacitor voltages are directly send the the capacitor voltage balance sorting process. Finally, the arm-voltage reference voltage v_{ref} is needed in the selected modulation technique whereafter the amount of submodules inserted N_{sum} can be either taken as n_{ins} are using the analytical estimation methodolgy as N_{su} as explained in section 5.5. the From the gate-pulse generator, the gate signals (GS) are generated. The highlighted blocks are further outlined:

- Moving maximum: In section 5.4.1 the ideology of measurement aggregation techniques were discussed. The implications of the non-periodic insertion showed a curve-fit or moving maximum can be used whereas this was considered out of scope of the current research. In order to show general purpose of the lifetime optimization insertion indices, a moving maximum has been used for the measurement aggregation between the submodules. The time-interval is set 20 ms such that one period is covered in the 50 Hz AC-system. This short time window is justified by the fact the modulation index is unity and all submodules are used in the arm.
- Rotation vector: After δ is formed, the selected submodule indice where more losses have to be generated, is always located on the high-priority side of the selection window. This is only effective when B_L submodules have to be inserted. A rotation algorithm is applied based on N_{sum} that relocated the selected submodule indice to the indice of N_{sum} in δ'. The selected submodule indice is thus always on the position where the ripple over the plane staircase function occurs over n_{ins} in the selection window.
- Vector contaminate: The selection window from δ' is contaminated with the remaining part of the capacitor voltage balance process γ before the gate pulse can be generated.

Simulation The presented control system has been implemented in MATLAB/Simulink together with a single leg of an MMC to validate the working of the proposed controller including capacitor voltage balancing and lifetime optimization. Both arms in the leg consist of eight half-bridge configured submodules and only the upper-arm is modeled including *T2* deterioration. The DC-poles are rated 8 kV whereas each submodule is 2 kV. The arm current is measured at the DC poles and each submodule is built with capacitor voltage sensors and IGBT collector-emitter voltage sensors. As the converter works in inverter mode, these sensors are only installed at *T2* due to their dominating losses and high deterioration. A mechanism assures the measurements are only performed when the respective gate signal is fired such that OFF-state measurements are filtered.

In order to mimic the effect of increasing ON-state collector-emitter voltage during deterioration, a resistor is placed in series with *T2* which increases according to the number of instances the respective device has been switched between ON-state and OFF-state. This respective resistance R_s is modeled according,

$$R_s = \alpha \left(N_{sw}\right)^{\beta}, \tag{5.22}$$

where N_{sw} represent the number of times the corresponding series *T2* device has switched, α is the deterioration offset factor and β the deterioration scaling factor. The parameters per series resistor in the upper arm are listed in Table 5.2.

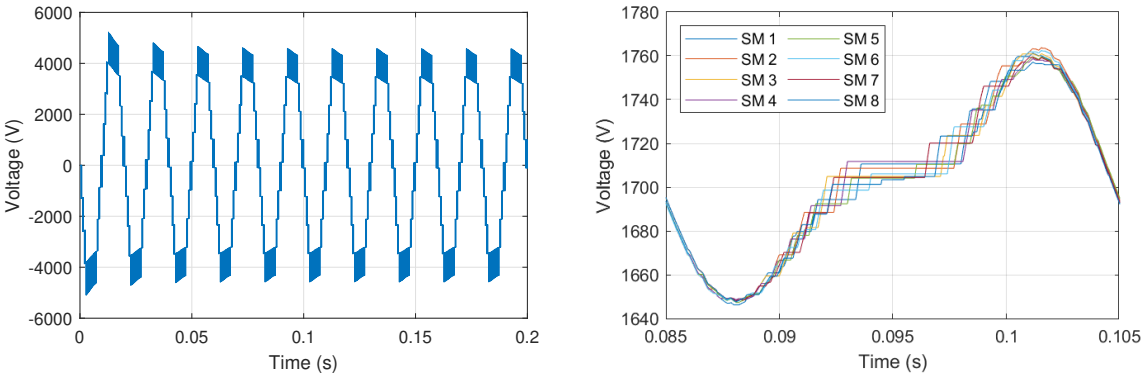
Table 5.2: Lifetime deterioration parameter settings α and β per submodule in the upper arm.

Submodule number	α	β
1	1×10^{-6}	1.40
2	1×10^{-6}	1.00
3	1×10^{-6}	1.05
4	1×10^{-6}	1.10
5	1×10^{-6}	1.08
6	1×10^{-6}	1.10
7	1×10^{-6}	1.00
8	1×10^{-6}	1.20

With these parameter settings, submodule 1 should deteriorate the fastest under the same submodule switching frequency due to the highest offset factor β. Oppositely, submodules 2 and 7 should deteriorate the slowest.

First, the capacitor voltage balancing and the generation of the AC-phase voltage is simulated. These simulation results can be seen in Figure 5.14.

In the figure, the generated AC voltage can be seen in a block shape. Due to the absence of arm reactors, this waveform is not completely sinusoidal. These reactors are not modelled because of the



(a) Generated AC phase voltage.

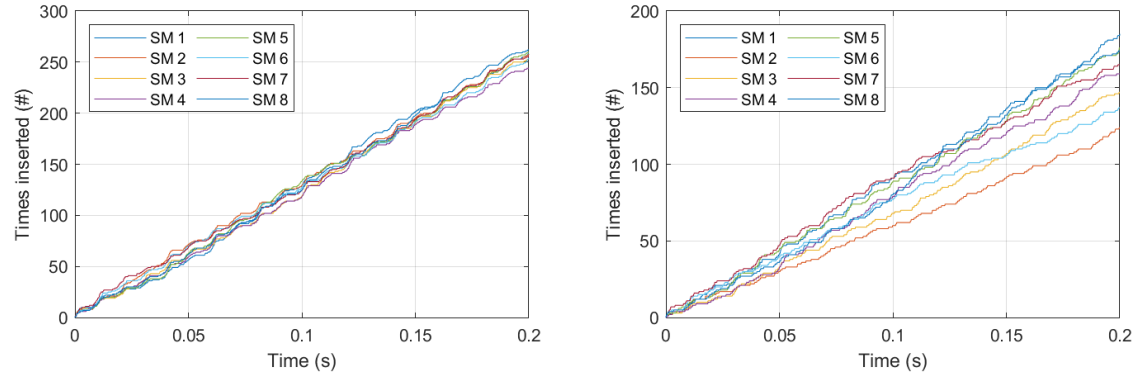
(b) Capacitor voltages during a single 50 Hz period.

Figure 5.14: Generation of the AC-phase voltage and the capacitor voltage balancing between the eight submodules.

increased computational burden due to the higher differential equation order these components bring. Since the focus is on the control methodology of the insertion indices, there is no need to have pure sinusoidal waveforms in the simulation. The average capacitor voltage of 1.7 kV is reduced compared to the initial value of 2 kV due to the capacitance and DC-pole current. The capacitance and capacitor voltage balancing process shall be tuned to keep the capacitor average voltages at a preferred value compared to only balancing the voltages. Further, it can be seen the peak AC-phase voltage is lower at around 5 kV than expected (8 kV - 8×1.7 kV). This is because of the ratio between the AC-phase impedance and the arm resistors. For more sophisticated simulation behaviour, other simulation tools such as RSCAD shall be used but require adjustments in order to simulate the deterioration effect of *T2*.

Besides, the capacitor voltages are seen to be balanced and follow a sinusoidal pattern with block steps. This balancing process confirms the working of the intended capacitor voltage balancing algorithm. The increasing half of the sinusoidal waveform has a more block shape compared to the decreasing half of the sinusoidal waveform because in the first half, the arm current is strongly positive such that the capacitors are charging fast while in the second half, the arm current is only slightly negative and the capacitors are discharging slowly. In conclusion, the capacitor voltage balancing process performs as intended but another controller is needed to keep the average voltage values at the intended voltage in order to generate the desired AC-phase voltage.

Secondly, the performance of the selection window control aspect has been verified using the MATLAB/Simulink model. Two scenarios are considered; disabling the selection window such that only the capacitor voltage balancing controller is active and enabling both controllers implying the complete presented control methodology is simulated. The number of times a submodule is inserted using both strategies is depicted in Figure 5.15. According to the scenario with only the capacitor voltage bal-



(a) Capacitor voltage balancing control.

(b) Lifetime optimization and capacitor voltage balancing control.

Figure 5.15: Number of times a submodule has been inserted with two scenarios considered.

ancing controller active, the submodules are seen to be inserted evenly over time. This confirms the explanation of the capacitor voltage balancing controller evenly inserting submodules over time in order to balance the voltage (energy) between each submodule. When the lifetime optimization controller is also activated, the insertion frequency between the submodules starts to differ over time. It can be seen submodule 1 is inserted most while submodule 2 is inserted least as expected. Interestingly, submodule 6 is inserted less than submodule 7. This could be a result of the capacitor voltage having more influence on the insertion indices of submodule 7 so that the indice of submodule 7 is often outside the selection window. Another reason is the lifetime optimization controller works with a selected submodule, namely submodule 1 in this example, while the remaining submodules are used to switch less in a more random matter.

Finally, a simulation has been made with first only the capacitor voltage balancing controller active whereafter the lifetime optimization controller is also activated. These results are shown in Figure 5.16.

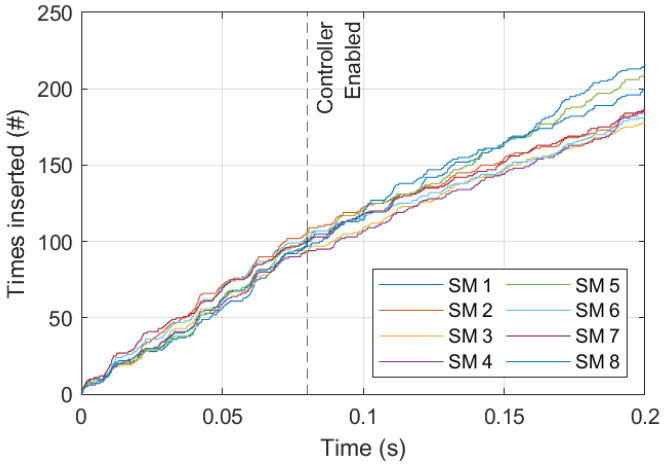


Figure 5.16: Capacitor voltage balancing control whereafter the lifetime optimization controller is activated at roughly $80\,\mathrm{ms}$.

From here it can be seen the submodules are first inserted evenly over time whereafter also the lifetime optimization controller is activated and the submodule insertion frequency starts to differ between the submodules. A similar pattern as the previous simulation can be observed where the differences are mainly caused by the shorter activation time of the lifetime optimization controller. The longer the lifetime optimization controller is active, the larger the difference in insertion frequency between the selected submodule and the remaining submodule will be. This selected submodule can clearly be seen as the submodule with the highest ON-state collector-emitter voltage (difference in β) and thus represent the fastest degradation.

6
Reliability Centered Maintenance

In Chapter 2 the IGBT device structures applied in modern MMC and their subsequent failure modes were analyzed. It was found that the junction temperature is the main reason for IGBT degradation. In order to estimate the junction temperature, it was explained in Chapter 3 that the power losses in the IGBT devices should be estimated based on the MMC operational conditions. A comprehensive model with linear- and non-linear loss estimation was discussed and presented. Based on these power losses, in Chapter 4 an absolute junction temperature estimation model for each IGBT was developed. This makes it possible to estimate the absolute junction temperature of each IGBT in an MMC depending on the converter operational conditions and the location of the submodule.

This chapter aims to estimate the absolute remaining lifetime of each submodule in an MMC. This implies that the absolute junction temperature of each IGBT should be modelled towards the remaining lifetime of the submodule in which it is located. The resulting technical condition of the IGBT devices and thus the submodules are of utmost important for a reliability centered maintenance strategy.

6.1. Reliability Analysis

Reliability is defined as the ability of a system to fulfil its function for a given time period and under certain conditions. The reliability of a single submodule is of substantial significance for the reliability of the complete converter and a HVDC link. Power losses in the four semiconductors in the half-bridge configured submodules were seen to be different between the semiconductors but generally identical for all submodules. This means if one of the hundreds submodules in modern MMC approaches its end-of-life, nearly all of them will be at their end of life and have a high failure probability. The general time-dependent reliability lifetime of a component is characterised by the bath-tub curve as shown in Figure 6.1.

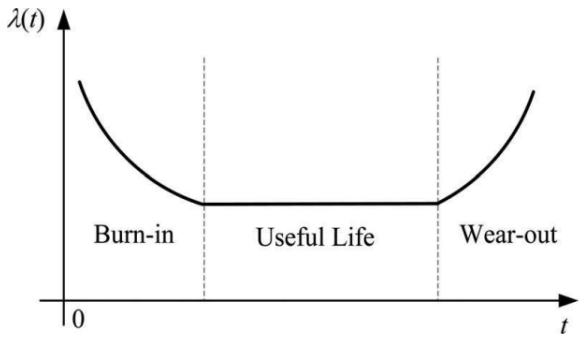


Figure 6.1: Example illustration of a bathtub failure rate curve with the three regions and general failure rate behaviour [60].

Generally, the failure rate of a component, mentioned further as a submodule, is first high and burn-in failures are experienced which are due to abnormalities in the design and fabrication process. These failures are hard to predict and generally taken for granted. After a certain time period, the submodules with manufacturing deviations are faulted and replaced whereafter the failure rate of the remaining submodules will decrease and these will enter their useful life phase. The failure rate is non-zero and a low number of failures is seen. Manufacturers are required to design the MMC such that the product of the failure rate per submodule and the number of submodules in the MMC is below the redundancy limit for yearly operation. The failure rate in this phase is hard to determine and unusable for health indexing

due to the project-specific designs and the high development rate of semiconductors in MMC. After the useful lifetime, semiconductors will enter their end-of-lifetime and the failure rate of the submodules will start to increase. Especially in MMC, it can be expected that the incline will be very steep due to the uniform stresses of semiconductors between all submodules. This research will therefore focus on the estimation of the start of the end-of-life phase.

6.2. Damage Model

The estimation of the useful remaining lifetime of an IGBT device is complex. These remaining lifetime models are device-specific and manufacturers normally only provide needed accelerated ageing measurements under strict non-disclosure agreements. Nevertheless, a fundamental lifetime estimation model can be developed, where parameters can be easily adjusted based on the provided information by the manufacturer.

There are in general different models indicating the damage done by a single thermal junction temperature cycle as published in the literature. These models are briefly discussed in the following paragraphs.

Coffin-Manson The Coffin-Manson model describes the remaining number of thermal cycles N_f of junction temperature swing amplitude ΔT_j as a function of scaling parameters *A* and *n*,

$$N_f = A\left(\Delta T_j\right)^{-n}, \tag{6.1}$$

where *A* is determined by the size of the solder joint, the coefficient of thermal expansion mismatch between the material layers, the solder thickness, and the ductility factor of the solder joint [61].

Several curve-fits were performed on accelerated ageing test data in [62]. The device under test was a $3.3\,$kV, $1.0\,$kA rated IGBT where *A* was estimated to be 5.23×10^{15} and *n* approximated as -5.34. However, it was also found that the Coffin-Manson model alone was not sufficient to estimate the remaining lifetime for the device under test. Another research focusing on bond-wire lift-off, the main degradation mechanism for bond-wire IGBT devices, reported parameter *A* as 1.4×10^{11} and *n* to be -3.597 [63]. The semiconductor used was fabricated by Dynex High Power Semiconductors.

LESIT model An Arrhenius factor including the average junction temperature $T_{j,av}$ was added to the Coffin-Manson model resulting in the LESIT model [64]. This includes effect of the average junction temperature $T_{j,av}$ on the remaining cycles to failure,

$$N_f = A\left(\Delta T_j\right)^{-B} e^{\frac{Q}{RT_{j,av}}}, \tag{6.2}$$

with *Q* representing the activation energy and *R* the gas constant. It holds that the higher the average junction $T_{j,av}$ temperature, the lower the number of cycles to failure. Parameter *C* is a constant that should be derived from curve-fitting accelerated ageing test data.

Extremely contradicting model parameters were given in [65]. First, an additional factor was added to include the junction temperature cycling frequency, effectively changing the model to a Lorris-Landzberg model with the Arrhenius term as a function of the maximum junction temperature $T_{j,max}$ and the gas constant with Boltzmann constant k_B,

$$N_f = Af^{-\alpha}\left(\Delta T_j\right)^{-B} e^{\frac{Q}{k_B T_{j,max}}}, \tag{6.3}$$

whereafter the cycle frequency *f* was taken as one, and the total cycles were counted with the Miner damage theorem, effectively making the model a LESIT model with different parameters in the Arrhenius term. Most contradicting is model parameter *C* was given 0.42 and k_b as 1.38×10^{-23} (Boltzmann constant). This means the Arrhenius term results in infinity for all reasonable operating semiconductor junction temperatures (30–$125\,$degC) in MMC-type HVDC converters applied in practice.

Bayerer model A sophisticated model has been developed by Bayerer et al in [66]. Compared to the LESIT model, more factors are affecting the remaining cycles to failure are included,

$$N_f = K_1\left(\Delta T_j\right)^{-\beta_1} e^{\frac{\beta_2}{T_{j,min}+273}} t_{on}^{\beta_3} I^{\beta_4} V_B^{\beta_5} d_b^{\beta_6}, \tag{6.4}$$

with t_{on} indicating the heating time, I the current through the IGBT device, V_B the device blocking voltage, and d_b the bond-wire thickness.

The accelerated ageing test data of the 3.3 kV, 1.0 kA rated IGBT in [62] was also curve-fitted on a modified version of the Bayerer model. Here, ($KV_B^{\beta_5} d_b^{\beta_6}$) and the Arrhenius term, were included in a new constant K_2:

$$N_f = K_2 \left(\Delta T_j\right)^{-\beta_1} t_{on}^{\beta_3} I^{\beta_4} \tag{6.5}$$

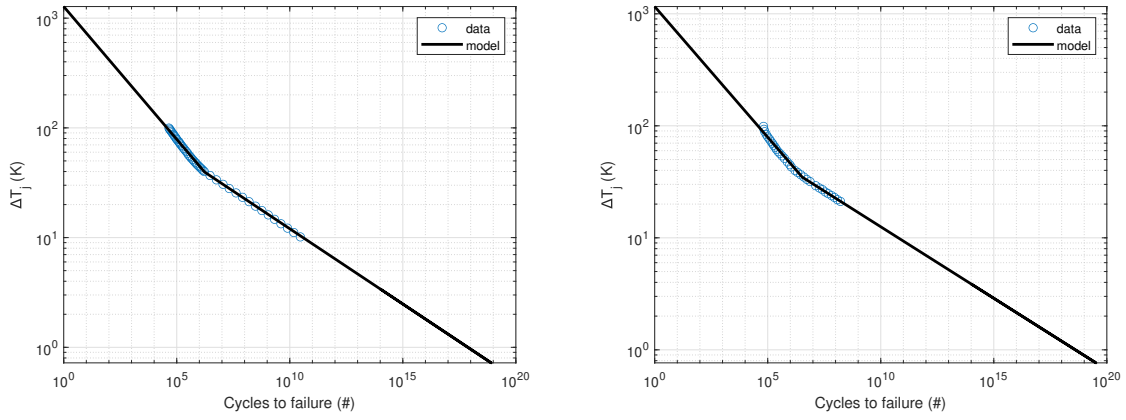
The resulting fitting parameters obtained for both models are depicted in Table 6.1.

Table 6.1: Resulting coefficients Bayerer model test data comparison between two publications.

Model	K_1	K_2	β_1	β_2	β_3	β_4	β_5	β_6
[62]		5.23×10^{15}	-2.07		-1.42	-4.1		
[66]	N/A		-3.483	1.917×10^3	-0.438	-0.717	-0.751	-0.564

A comparison was made for the obtained parameters in [62] with the original Bayerer model in [66]. These models were not matching, with a justification that the studied IGBT devices possibly differ too much. Different manufacturing techniques and technological advancements in the devices could result in different estimation methods for remaining cycles to failure.

Selection The Bayerer model is the most sophisticated model but requires many input parameters making the lifetime consumption calculation for an MMC more difficult. Besides this, the bond-wire thickness d_b is often not specified in open-source IGBT datasheets and could therefore not be used in practice. Therefore, this model has been excluded further. While the LESIT model is the more sophisticated version of the Coffin-Manson model, no parameters were found to make a reasonable estimate of the remaining cycles to failure. In contrast, the Coffin-Manson model was reported to lack the addition of extra necessary parameters for an accurate estimation of the remaining cycles to failure. Most importantly, for identical models applied to different IGBT devices, different fitting parameters were obtained which emphasizes the need to perform accelerated ageing test data per IGBT device. From here it can be concluded that TSO TenneT shall request subsequent damage models for each converter individually to the manufacturers and currently no general damage model applicable to all semiconductors exists. For the remaining part of this research, the exemplary numerical damage models from application manuals are used as depicted in Figure 6.2.



(a) Infineon Technologies application manual.

(b) Fujij Electric application manual.

Figure 6.2: Generated models using curve-fit from two remaining cycles to failure estimation curves given in manufacturer application manuals.

6.3. Temperature Damage Components

The thermodynamic models are used to calculate the absolute junction temperature of each device based on converter operational conditions. Historical data can now be used to calculate these junction

temperatures over time and estimate the remaining useful lifetime of the devices based on the failure curves. Two different forms of thermal cycles can be examined over the semiconductor junctions:

- High-frequency cycles: the temperature ripple component over the semiconductor junctions due to the half-wave conducting characteristics over the fundamental frequency AC-waveform.
- Low-frequency cycles: converter load-changes and cooling system setpoint adjustments result in absolute junction temperature differences.

The high-frequency cycle amplitude is normally small whereas low-frequency temperatures could be higher. On the other hand, these high-frequency temperature cycles occur very frequently such that the resulting total damage to the device is of more significance. The influence of these temperature components should be examined based on historical operational data and compared between different converters to understand the effects between constant loads and highly fluctuating loads.

6.3.1. Cycle counting

The amount of high-frequency temperature components can be easily calculated based on the time constant, which is 20 ms for 50 Hz AC systems, and the converter operational conditions. The computation of the ripple amplitude was explained in section 4.2.2.

For the low-frequency temperature cycle counting a more sophisticated approach has to be used. From the computed absolute junction temperatures over time, it could be harder to assess when the junction temperature makes a full cycle with which respective amplitude. In the most optimum scenario, the required historical data has a high sampling rate such that the estimations are very accurate and no temperature fluctuations are seen as a result of the sample rate. However, the sampling frequency from the required operational data is in the range of mHz in practice so that temperature fluctuations could be seen which are only a result of the low data sampling rate. Therefore, the lowest temperature fluctuations are first filtered out such that only the higher fluctuations determine the low-frequency temperature components. In order to illustrate the methodology to estimate the remaining lifetime based on cycle counting, an example case study is used. For the analysis, an MMC-type HVDC converter operating in inverter mode with half-bridge configured submodules is used. The focus is on the submodule *T2* device implying the most stressed component is the submodule. First, the filtering process is applied. An illustration of the filtering method applied for the IGBT device over a time period of two days is shown in Figure 6.3.

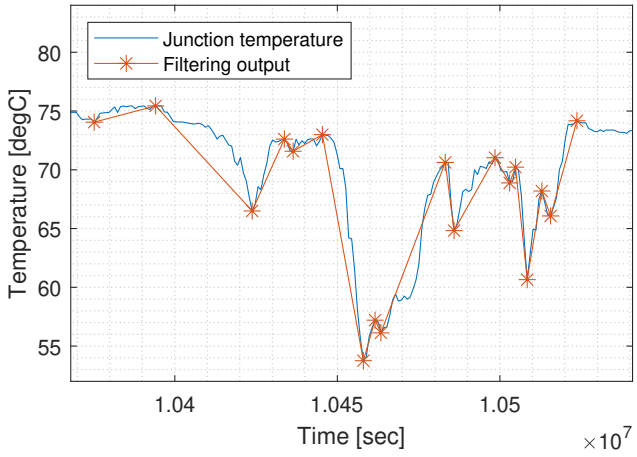


Figure 6.3: Illustration of the filtering process to exclude high variations due to the data low sample rate.

The IGBT device can be seen suffering several low-frequency junction temperature cycles. Obviously, the amount of cycles experienced over a two-day period is low because of the converter load profile. After the filtering process, the temperature cycles have to be counted and an approach called rain flow counting is applied. Based on each absolute junction temperature and the next subsequent junction temperature, it is assessed whether a full temperature cycle is made. This can be graphically

explained using Figure 6.3. Multiple short-temperature components can be seen after the filtering process. These are during other longer-temperature components and therefore disrupt the total amplitude of other cycles. The methodology used in rain flow counting assures all full-range temperature components are added together and smaller fluctuations do not disrupt these full cycles. Since the rain flow counting algorithm is also able to compute the average value of the junction temperature per cycle, is it often used in literature [67]. An automated rain flow counting function is integrated into MATLAB that performs according to the *ASTM E 1049* technical standard focused on standard practices for cycle counting in fatigue analysis. This function will be used further in this research. An example of the rain flow counting method based on a yearly time span of the studied *T2* device is depicted in Figure 6.4.

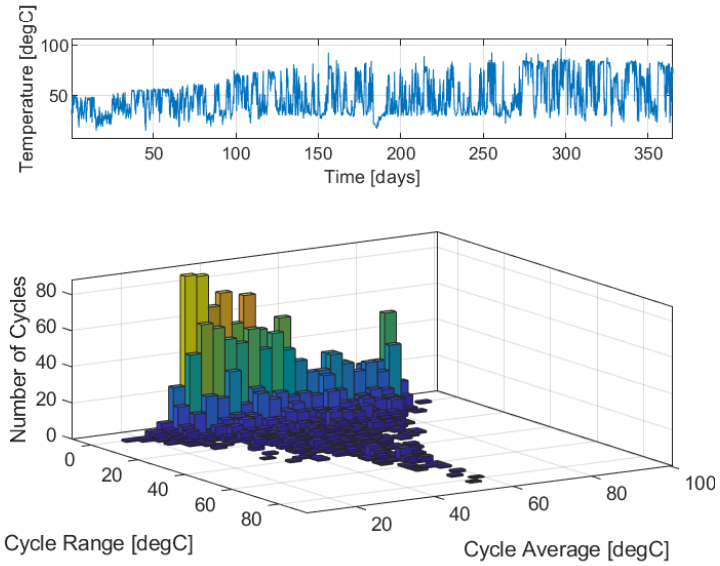


Figure 6.4: Rain flow counting results for a yearly mission profile of an *T2* device in a converter operating in inverter mode.

In the figure, the historical annual calculated temperature from the filtering process is seen on top. The temperature first makes low-frequency cycles about 50 degC and later rises to approximately 75 degC. First, the average temperature is rather low, and this could represent a period with less converter loading. The loading could be caused due to the wind speed in the area if the converter is connected to a wind farm via the DC-link. In the bottom figure, the number of counted cycles using the rain flow methodology can be seen. The lower the cycle range, the more cycles are counted. These lower average temperature cycles are just above the filter limitation and cause less damage to the IGBT. Surprisingly, many low temperatures (about 20 degC) cycle averages can be seen. This indicates the IGBT operates at a lower temperature than expected during a significant part of the annual operational profile. The heat-sink optimization from Chapter 4 could be a good solution to raise the cycle average temperature for more efficient converter operation.

6.3.2. Accumulated damage

After temperature component counting, the damage done from each temperature cycle can be computed using the lifetime curve. In order to assess the total damage done from all temperature segments, the low-frequency and the high-frequency components, Miner's linear fatigue accumulation theorem can be used [68]. This theorem is widely accepted as a universal standard in fatigue analysis, and is based on the assumption that fatigue damage is equal to the accumulated cycle ratio [69],

$$D = \sum \frac{n_i}{N_i}, \tag{6.6}$$

where D ($0 < D < 1$) represents the cumulative damage of the device and n_i the number of respective cycles of damage N_i. A device can be considered faulty when D equals 1. For e.g. a time-duration of 1 s in a 50 Hz switched system, every 20 ms there are 50 high-frequency temperature components. If the cycles-to-failure from each of those high-frequency temperature components is 10^8, n_i equals 50

and N_i is 10^8. An illustration of the cummulative damage done to the IGBT in the annual mission profile estimated from the rain-flow counting method is shown in Figure 6.5.

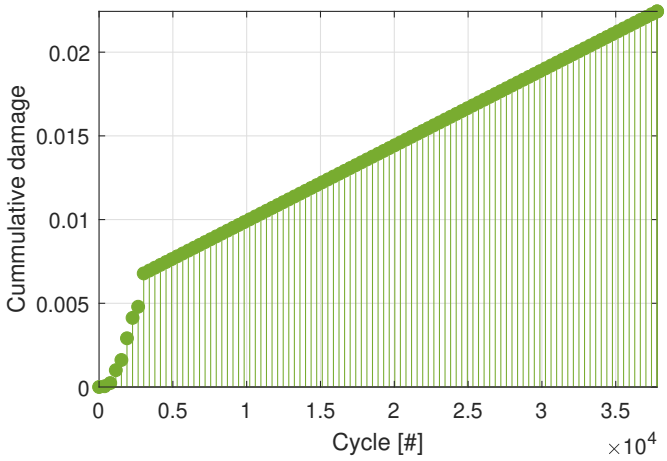


Figure 6.5: Annual cummulative damage of a *T2* device in a converter operating in inverter mode.

From the cumulative damage plot of *T2* it is shown roughly $2\,\%$ of the lifetime is consumed on an annual basis. A small portion of the cycles is seen to consume $0.5\,\%$ of the lifetime while the rest is shown to increase linearly due to the low significance of the cycle amplitudes. Based on these results and the assumptions used, it can be concluded the expected lifetime of the *T2* device is much longer compared to the minimum lifetime of 40 years as specified by TSO TenneT.

6.4. Lifetime Assessment

A case study should determine the effect of the load profile and the amplitude of the DC-pole current on the lifetime of the IGBT devices in the submodules. This summarizes all previous analyses into the final computation of the remaining useful lifetime. This section is devidided into a medium scenario load profile and a heavy scenario load profile representing higher converter loading.

There are many different loadings possible. To include low-frequency junction temperature cycles and study the effect of high-frequency junction temperature cycles, there are two scenarios considered:

- Medium scenario: The DC-pole current is $500\,\text{A}$ and increases daily once to $1\,\text{kA}$ whereafter it returns to $500\,\text{A}$ at the end of the day. The ratio of full-load with $1\,\text{kA}$ compared to low-load with $500\,\text{A}$ determines the capacity (1–$99\,\%$) of the converter.
- Heavy scenario: The DC-pole current is $1\,\text{kA}$ and increases daily once to $2\,\text{kA}$ whereafter it returns to $1\,\text{kA}$ at the end of the day. The capacity factor is calculated similarly to the medium scenario.

The difference between these scenarios shows the effect of mainly the high-frequency junction temperature cycles due to the major dependency on the DC-pole current. Daily, the DC-pole current is twice the current from the medium scenario for an identical converter capacity factor. The transported power is thus higher and this will increase the power losses and the semiconductor junction temperature ripple as determined in the previous Chapters.

6.4.1. Medium scenario

In this scenario, the DC-pole current is assumed to be $500\,\text{A}$ and maximum $1\,\text{kA}$ such that it represents a $900\,\text{MW}$ symmetrical MMC-type HVDC converter rated $320\,\text{kV}$. The IGBT device used is a $4.5\,\text{kV}$ rated device designed by Infineon Technologies and referred to as *FZ1200R45HL3*. This voltage class is often used in practice for these converter power ratings. The relevant IGBT specifications are shown in Table 6.2.

It is seen the switching energy losses are rather low compared to the previously assessed IGBT devices. Similar comparison as previously, identifying if the device is older since it is optimization in switching loss optimization, is not possible since the reference measurements are here based on a

Table 6.2: Semiconductor electrical parameters used in the analysis. E_{on}, E_{off}, and E_{rr} reference measurements are made at 2800 V and 1200 A.

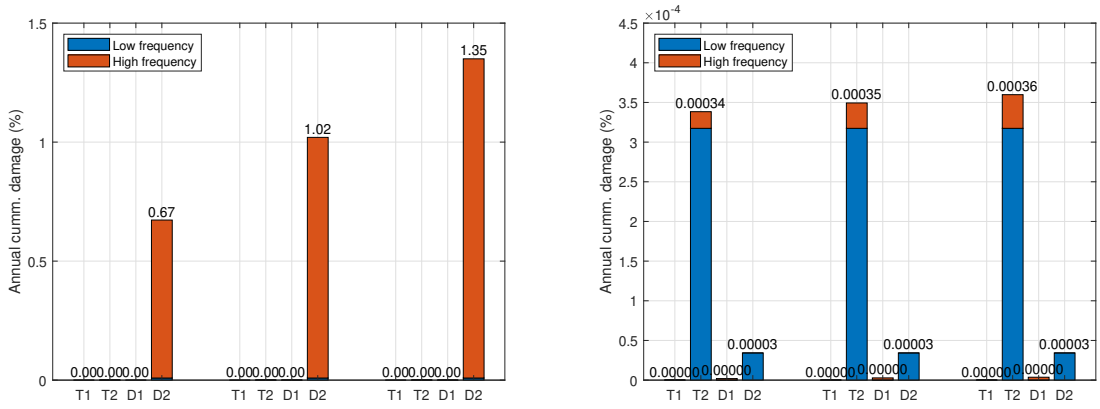
Device		$V_{0,cx}$ [V]	$R_{c/f}$ [mΩ]	E_{on} [J]	E_{off} [J]	E_{rr} [J]
FZ1200R45HL3	IGBT	1.50	1.11	5.3	5.3	
FZ1200R45HL3	FWD	1.25	0.972			3.2

collector-current of 1.2 kA compared to the Hitachi Energy reference measurements at 3.0 kA. The thermal characteristics of the IGBT device are shown in Table 6.3.

Table 6.3: Semiconductor thermal parameters used in the analysis.

Device		R_{jc} [mΩ]	R_{ch} [mΩ]	$R_{jc,1}$ [mΩ]	$R_{jc,2}$ [mΩ]	$R_{jc,3}$ [mΩ]	R_{jc4} [mΩ]	$\tau_{jc,1}$ [s]	$\tau_{jc,2}$ [s]	$\tau_{jc,3}$ [s]	τ_{jc4} [s]
FZ1200R45HL3	IGBT	8.20	10.0	1.23	4.91	1.28	0.734	0.0050	0.053	0.63	5.59
FZ1200R45HL3	FWD	13.8	10.5	3.47	7.48	2.01	0.834	0.0050	0.050	0.47	5.93

For the heat sink, the simplified thermal model has been used where the heat sink represented by a single thermal impedance equal to $14\,\mathrm{K/kW}$. The submodule switching frequency is 150 Hz and each submodule is rated 2.5 kV with the AC-phase angle 0 deg and the modulation index unity. For the cycles to failure damage model, the estimations from Figure 6.2b are used. The resulting annual cumulative damage (%) for the four semiconductors in the half-bridge configured submodules under three different converter capacities is seen in Figure 6.6.



(a) Rectifier mode.

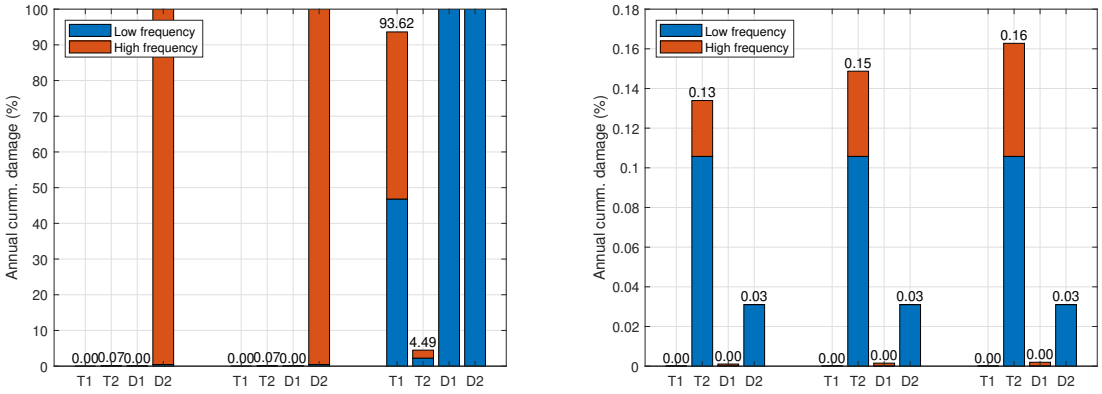
(b) Inverter mode.

Figure 6.6: Annual cumulative damage to the four semiconductors in half-bridge configured submodules with the medium scenario. Three converter capacity factors are studied with from left to right; 70 %, 80 %, and 90 % rated power.

According to the annual cumulative damage, it is clear in rectifier operation mode, most damage is caused to the *D2* device under all three converter capacity factors. While for a capacity factor of 70 % this annual damage is 0.67 %, this increases to 1.35 % damage if the capacity factor is 90 %. The high-frequency damage component is the most significant for this device due to the high junction temperature ripple in the FWD. Obviously, in inverter operation mode device *T2* suffers the highest annual damage. Compared to the rectifier mode, here the low-frequency damage component is the main contributor to the total damage instead of the high-frequency damage component. This can be explained using the semiconductor thermal parameters as given in Table 6.3. Here it can be seen while the Foster thermal time constants are almost equal for both semiconductor devices, the thermal resistance is higher for the FWD semiconductor in network orders compared to the IGBT semiconductor. This causes the junction temperature ripple to be higher and the high-frequency damage more significant for the *D2* device.

6.4.2. Heavy scenario

During the heavy scenario, the DC-pole current is assumed to be 1 kA and increases to 2 kA on a daily basis. The ratio between the peak-current of 2 kA and 1 kA defines the converter capacity factor. This heavy scenario represents a symmetrical monopolar 2 GW MMC-type HVDC converter rated 525 kV. A similar IGBT as in the medium scenario has been used and the half-bridge configured submodules are rated 2.5 kV. The submodule switching frequency is 150 Hz and the power factor unity. For the cycles to failure damage model, the estimations from Figure 6.2b are used. It should be noted that a higher voltage class IGBT device is going to be used for the future 2 GW converters for TSO TenneT. Instead of the studied IGBT device with a blocking voltage of 4.5 kV, 6.5 kV rated IGBT devices will be used due to the higher current that causes a higher voltage ripple over the submodule capacitors. This can be counteracted by reducing the submodule capacitor capacitance such that the heavy scenario is still possible in practice but not preferred. The resulting annual cumulative damage (%) for the four semiconductors in the half-bridge configured submodules under three different converter capacities is seen in Figure 6.7.



(a) Rectifier mode.

(b) Inverter mode.

Figure 6.7: Annual cumulative damage to the four semiconductors in half-bridge configured submodules with the heavy scenario. Three converter capacity factors are studied with from left to right; 70 %, 80 %, and 90 % rated power.

The cumulative annual damage is much higher for the heavy scenario compared to the medium scenario. First, in the rectifier mode, it can be seen that device *D2* already suffers more than 100 % cumulative damage only according to the high-frequency damage component for a capacity factor of 70 %. The DC-pole current causes many losses in *D2* whereafter the thermal Foster constants of the FWD amplify the effect and generate a high junction temperature ripple with significant damage to the semiconductor. As a result, this IGBT device can not be implemented in a 2 GW converter operating in rectifier mode with a reduced submodule capacitor capacitance to lower the subsequent voltage ripple. On the other hand, if this IGBT device is installed a similar converter operating in inverter mode, the annual cumulative damage is lower and an expected lifetime of 40 years can be reached with the linear cumulative damage model. This emphasizes the difference between the thermal time constants of the device IGBT and FWD semiconductors. As expected, the higher the capacity factor, the higher the high-frequency component damage will be. This is because the capacity factor influences the time duration the DC-pole current equals its peak-current of 2 kA thus increasing the power losses and the junction temperature ripple.

7
Conclusion

To assess the technical condition of submodules in MMC-type HVDC converters, a data-driven condition monitoring strategy using the existing TenneT Health Index framework for the semiconductor devices in the submodules had to be developed. With significant developments in the converter technology, practical knowledge was minimal and the failure mechanisms had to be studied. In particular, the developed methodology needed to be applicable to real projects and compatible with the diverse MMC-type HVDC converter implementations while the expected future outlook on the developments shall be incorporated in the model. Sophisticated research has been performed in this thesis which led to many new insights into the implementation of condition monitoring and lifetime optimization to unlock smarter maintenance strategies for these converters. Conclusions drawn throughout the thesis and recommendations for future research are outlined in this Chapter.

7.1. Conclusion

Semiconductor devices were discussed in Chapter 2 in order to predict which devices will be used in future MMC projects and are therefore relevant for condition monitoring. The relevant devices were described to be the conventional IGBT and the RC-IGBT. Whereas the conventional IGBT is now applied mostly in practice, the RC-IGBT is expected to be used more in future projects. Both devices can be surrounded by three different housing structures, the wire-bonded housing, rigid-press pack surrounding using external force, and the compliant-press pack housing with springs added inside the device. While the bond-wire structure mainly suffers from bond-wire degradation, all three devices experience solder degradation. From the extensive literature study, thermal cycling was determined to be the main cause for most failure mechanisms. This thermal cycling is a result of the device semiconductor junction temperature that fluctuates during operation.

The most suitable condition indicator to estimate the cumulative damage to the semiconductors was determined to be the ON-state collector-emitter voltage. During degradation, cracks will form between the semiconductor chip junctions and the device case. These cracks are in the middle of the heat propagation path from the semiconductor junction to heat sink meaning the thermal impedance will increase. This thermal impedance causes the device to operate on a higher absolute junction temperature increasing the ON-state collector-emitter voltage. Since the absolute junction temperature is near impossible to estimate, the ON-state collector-emitter voltage is determined to be the most suitable condition indicator.

The ON-state collector-emitter voltage was outlined in Chapter 2 and is influenced by the arm-current, which could be measured, and the junction temperature for which a complex estimation model had to be developed. The estimation of the technical condition of the submodule semiconductor was thus an extensive process consisting of two parts. First, in Chapter 3 the semiconductor power loss computation was presented using available converter operational conditions such as the DC-pole current and the submodule switching frequency. Based on the available specifications, the conduction, switching, and reverse-recovery losses were estimated and three different estimation methods were compared. The power losses were seen to differ significantly between the converter inverter and rectifier operation modes for the four semiconductors in half-bridge configured submodules. The second part in the estimation of the technical condition of the semiconductors was explained in Chapter 4 where the junction temperature components were computed with the device power losses and the device thermal characteristics. The temperature was explained to consist of the fundamental AC-frequency period ripple over a steady-state value. The steady-state temperature estimation was presented based on two possible approaches such that it can be computed in different projects and data availabilities. The AC-

fundamental frequency temperature ripple was shown to be highly dependent on the device's thermal impedance but generally assumed to be low. These thermal models made it possible to estimate the junction temperature within the ripple boundaries and finally assess the technical condition of the submodule semiconductors based on the ON-state collector-emitter voltage.

The differences between the four semiconductor power losses in half-bridge configured submodules were explained to cause differences in ageing depending on the converter operational mode. A novel lifetime-optimization approach was presented in Chapter 5 that allocates submodule insertion indices based on a selection window. The presented control philosophy was designed to be compatible with existing converter controllers and easily adopted in control systems as it uses available control system building blocks. The philosophy has not been seen in literature and it is expected to open a new direction in HVDC converter research and development. An analytical method was presented to estimate the effect of the controller on the semiconductor junction temperature fluctuations where it was seen a selected submodule can be degradated to prolong the remaining lifetime of other submodules. A practical control system implementation was shown in MATLAB/Simulink to be compatible with the capacitor voltage balancing process and the insertion sum performs as expected.

A project-specific lifetime estimation model for all four semiconductors has been developed in Chapter 6. Particular focus was on the available parameters such that the model can be verified using existing historical operational measurements. Different damage models were outlined whereafter exemplary failure curves were used further. Depending on the manufacturer of the converters it would be possible to use any damage model in the lifetime assessment methodology. The two damage components were determined to be the low-frequency and high-frequency cycles. The most contributing damage component was shown to be converter specific, with a determination between the converter loading; either connecting a heavy-loaded wind farm or a medium-loaded wind farm.

7.2. Recommendations for Future Research

Inclusive research has opened many new directions for future research. These are outlined according to the Chapter categories in the following paragraphs.

Power loss estimation Estimation models for the power losses in the four semiconductors in half-bridge configured submodules were outlined in Chapter 3. These models revealed the differences between the semiconductor power losses and showed that *D2* power losses are highest in rectifier mode and *T2* power losses are dominant in inverter mode. Since these losses were seen the be of significant relevance in the semiconductor deterioration in Chapter 6, further research is needed to reduce the losses in the dominating power loss device. This means that an optimum must be studied on the submodule level instead of the component level. The total power losses per submodule could thus be higher such that the power losses in the dominating device are lower. This will finally result in a prolonged lifetime of the respective submodule.

Converter thermodynamics In Chapter 4 the converter thermodynamics were studied. Here it was shown that the length of the liquid pipe through a liquid-cooled heat sink can be optimized to operate all four semiconductors in the half-bridge configured submodules at the same temperature. Operating these devices at a similar temperature is useful for higher efficiency and equally distributed resistances over the converter arms. More research on the length of the heat sink is needed to find an optimum based on the operational conditions and the cooling system limitations. Important aspects here are the modularity of the submodules since in practice manufacturers prefer to use interchangeable components irrespective of the position and the function of the semiconductor stack.

Further, it was shown that all four orders of the Foster thermal network are higher for the FWD semiconductors compared to the IGBT semiconductors. This means that even though the power losses are higher for the IGBT semiconductors, the junction temperature ripple is higher for the FWD semiconductors causing more degradation to the devices. This should be resolved and future research is needed on the reduction of the thermal resistances of the fourth-order Foster network of FWD semiconductors.

Another interesting aspect for future research is the estimation of the junction temperature ripple in RC-IGBT devices. For conventional IGBT devices practical experiments were performed and showed how the ripple can be estimated based on the operational conditions. For RC-IGBT devices an analytical approach still needs to be developed and is useful for the remaining useful lifetime estimation of

the devices.

Lifetime optimization The lifetime optimization methodology was presented in Chapter 5. For control system implementation a sliding maximum window was used to form vector δ representing the aggregation on arm-level. It was specifically noted this technique was used as a simplified representation because further research is first needed to find how those measurements can be aggregated and a maximum voltage can be found to determine the selected submodule. Finding the maximum ON-state collector-emitter voltage in a converter arm under dynamic operating conditions where submodules have different temperatures and are switched with a dynamic submodule switching frequency is an important topic.

Besides, the presented lifetime optimization control methodology was based on a single selected submodule in an arm. It would be interesting to study the effect if multiple submodules are used where the junction temperature ripple is increased. Potentially, the junction temperature ripple will decrease over the selected submodules such that the deterioration and failure moment can be prolonged depending on the time to maintenance. This is consistent with another research direction left open in this chapter, namely the lifetime optimization controller activation. It would be very interesting to study when the controller should be activated if maintenance to the converter has to be performed and the subsequent limitations.

Relability centered maintenance Finally the estimation of the IGBT devices remaining useful lifetime based on available operational measurements was presented in Chapter 6. Damage models were briefly discussed and compared and it was determined no general model for all IGBT devices is currently existing. Future research in the direction of the development of a general damage model for different IGBT devices and manufacturers would be interesting. Another approach could be the usage of damage models provided by IGBT manufacturers and verify if those match the lifetime expectations. It is important to consider the applicability since those models are normally only provided under strict non-disclose agreements.

For the cycle counting, a low-temperature fluctuation threshold had been used to filter out the effect of the low measurement sampling rate. It would be interesting to study this threshold in more detail and the corresponding effects on accuracy. While in literature the measurements are often at preferred sampling rates, in practice needed measurements have low sampling rates or sometimes no measurements are available at all during specific time windows.

Bibliography

[1] J. V. Dunné, "A data-driven health index for high-voltage sf 6 circuit breakers cover: Siemens 3av1 fg blue 145 kv live tank circuit breaker [1] style: Tu delft report style, with modifications by daan zwaneveld."

[2] G. Asplund, K. Lindén, C. Barker, *et al.*, "Hvdc grid feasibility study."

[3] M. H. Okba, M. H. Saied, M. Z. Mostafa, and T. M. Abdel- Moneim, "High voltage direct current transmission - a review, part i," in *2012 IEEE Energytech*, 2012, pp. 1–7. DOI: 10.1109/EnergyTech.2012.6304650.

[4] G. Kamalapur and K. Arakeri, *A comparative study of monopolar and bipolar hvdc transmission systems*, Oct. 2020.

[5] N. Macleod, G. J. Liang, G. H. Hillborg, *et al.*, *Members DESIGNING HVDC GRIDS FOR OPTIMAL RELIABILITY AND AVAILABILITY PERFORMANCE*. 2017, ISBN: 978-2-85873-415-3.

[6] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015. DOI: 10.1109/TPEL.2014.2327641.

[7] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, 2015. DOI: 10.1109/TPEL.2014.2310127.

[8] "Fundamentals of modular multilevel converter," in *Modular Multilevel Converters*. John Wiley & Sons, Ltd, 2017, ch. 2, pp. 37–78, ISBN: 9781119367291. DOI: https://doi.org/10.1002/9781119367291.ch2. eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/9781119367291.ch2. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119367291.ch2.

[9] S. E. G. GmbH, in *HVDC PLUS – the decisive step ahead*, 2022.

[10] M. Eremia, C.-C. Liu, and A.-A. Edris, "Power semiconductor devices for hvdc and facts systems," in *Advanced Solutions in Power Systems: HVDC, FACTS, and Artificial Intelligence*. 2016, pp. 11–34. DOI: 10.1002/9781119175391.ch2.

[11] G. Falahi, "Design, modeling and control of modular multilevel converter based hvdc systems," Ph.D. dissertation, Dec. 2014.

[12] L. Storasta, A. Kopta, C. P. Munaf Rahimo, S. Geissmann, and R. Schnell, in *The Next Generation 6500V BIGT HiPak Modules*, 2013.

[13] R. Simpson, A. Plumpton, M. Varley, C. Tonner, P. Taylor, and X. Dai, "Press-pack igbts for hvdc and facts," *CSEE Journal of Power and Energy Systems*, vol. 3, no. 3, pp. 302–310, 2017. DOI: 10.17775/CSEEJPES.2016.01740.

[14] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Study and handling methods of power igbt module failures in power electronic converter systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2517–2533, 2015. DOI: 10.1109/TPEL.2014.2373390.

[15] C. Busca, R. Teodorescu, F. Blaabjerg, *et al.*, "An overview of the reliability prediction related aspects of high power igbts in wind power applications," *Microelectronics Reliability*, vol. 51, no. 9, pp. 1903–1907, 2011, Proceedings of the 22th European Symposium on the RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2011.06.053. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271411002526.

[16] H. Chen, W. Cao, P. Bordignon, R. Yi, H. Zhang, and W. Shi, "Design and testing of the world's first single-level press-pack igbt based submodule for mmc vsc hvdc applications," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 3359–3366. DOI: 10.1109/ECCE.2015.7310134.

[17] Y. Jia, Y. Huang, F. Xiao, H. Deng, Y. Duan, and F. Iannuzzo, “Impact of solder degradation on vce of igbt module: Experiments and modeling,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 4, pp. 4536–4545, 2022. DOI: 10.1109/JESTPE.2019.2928478.

[18] M. Bayer, S. Hartmann, M. Berg, R. Moody, and G. Paques, “Interpretation of power cycling data derived from transient cooling curves,” in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–6.

[19] R. Liu, H. Li, R. Yao, W. Lai, W. Xiao, and H. Tan, “Overview of monitoring methods of press-pack insulated gate bipolar transistor modules under different package failure modes,” *IET Power Electronics*, vol. n/a, no. n/a, DOI: https://doi.org/10.1049/pel2.12407. eprint: https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/pel2.12407. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/pel2.12407.

[20] Y. Huang, Y. Luo, F. Xiao, B. Liu, and X. Tang, “Evaluation of the degradation in electrothermal characteristics of igbts during thermal cycling cocaused by solder cracking and al-wires lifting-off based on iterative looping,” *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 1768–1778, 2023. DOI: 10.1109/TPEL.2022.3209331.

[21] L. Tinschert, A. R. Årdal, T. Poller, M. Bohlländer, M. Hernes, and J. Lutz, “Possible failure modes in press-pack igbts,” *Microelectronics Reliability*, vol. 55, no. 6, pp. 903–911, 2015, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2015.02.019. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271415000451.

[22] R. Liu, H. Li, R. Yao, *et al.*, “Research on long-term reliability of silver sintered press-pack igbt modules,” *Power Electronic Devices and Components*, vol. 3, p. 100 012, 2022, ISSN: 2772-3704. DOI: https://doi.org/10.1016/j.pedc.2022.100012. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2772370422000098.

[23] E. Deng, Z. Zhao, Q. Xin, J. Zhang, and Y. Huang, “Analysis on the difference of the characteristic between high power igbt modules and press pack igbts,” *Microelectronics Reliability*, vol. 78, pp. 25–37, 2017, ISSN: 0026-2714. DOI: https://doi.org/10.1016/j.microrel.2017.07.095. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271417303876.

[24] W. Lai, H. Li, M. Chen, *et al.*, “Investigation on the effects of unbalanced clamping force on multichip press pack igbt modules,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2314–2322, 2019. DOI: 10.1109/JESTPE.2018.2876768.

[25] B. J. Baliga, “Insulated gate bipolar transistors,” in *Fundamentals of Power Semiconductor Devices*. Cham: Springer International Publishing, 2019, pp. 755–1044, ISBN: 978-3-319-93988-9. DOI: 10.1007/978-3-319-93988-9_9. [Online]. Available: https://doi.org/10.1007/978-3-319-93988-9_9.

[26] Q. Kong, M. Du, Z. Ouyang, K. Wei, and W. G. Hurley, “A model of the on-state voltage across igbt modules based on physical structure and conduction mechanisms,” *Energies*, vol. 12, no. 5, 2019, ISSN: 1996-1073. [Online]. Available: https://www.mdpi.com/1996-1073/12/5/851.

[27] X. Han, Q. Hao, D. Li, and S. Wang, “Junction temperature analysis of press-pack ig-bts of modular multilevel converter based on electro-thermal coupling model,” in *2019 4th IEEE Workshop on the Electronic Grid (eGRID)*, 2019, pp. 1–6. DOI: 10.1109/eGRID48402.2019.9092643.

[28] Y. Zhang, D. Xiang, G. Xu, L. Yin, and Y. Liu, “On gate oxide degradation mechanism and chip-related failure precursors of igbt,” in *2019 Chinese Control Conference (CCC)*, 2019, pp. 4878–4884. DOI: 10.23919/ChiCC.2019.8866596.

[29] “Analytical approximate calculation of losses for modular multilevel converters,” *IET Generation, Transmission & Distribution*, vol. 9, 2455–2465(10), 16 Dec. 2015. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/iet-gtd.2015.0228.

[30] R. Wu, J. Wen, J. Wu, Z. Chen, C. Peng, and Y. Wang, “Analysis of power losses in voltage source converter with new generation igbts,” in *2012 IEEE International Conference on Computer Science and Automation Engineering (CSAE)*, vol. 1, 2012, pp. 674–678. DOI: 10.1109/CSAE.2012.6272683.

[31] A. K. Sadigh, V. Dargahi, and K. A. Corzine, “Analytical determination of conduction and switching power losses in flying-capacitor-based active neutral-point-clamped multilevel converter,” *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5473–5494, 2016. DOI: 10.1109/TPEL.2015.2498107.

[32] Y. Yang and P. Zhang, “A novel bond wire fault detection method for igbt modules based on turn-on gate voltage overshoot,” *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7501–7512, 2021. DOI: 10.1109/TPEL.2020.3047135.

[33] P. Tu, P. Wang, X. Hu, C. Qi, S. Yin, and M. A. Zagrodnik, “Analytical evaluation of igbt turn-on loss with double pulse testing,” in *2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA)*, 2016, pp. 963–968. DOI: 10.1109/ICIEA.2016.7603721.

[34] V. K. Khanna, “Igbt fundamentals and status review,” in *Insulated Gate Bipolar Transistor IGBT Theory and Design*. 2003, pp. 35–100. DOI: 10.1002/047172291X.ch2.

[35] K. Yu, F. Gu, L. Zhang, and W. Ruan, “Comparative analysis of power loss for mmc rectifiers with nlm and cps modulation schemes,” in *2020 12th IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2020, pp. 1–5. DOI: 10.1109/APPEEC48164.2020.9220554.

[36] Z. Chen, L. Yuan, Z. Zhao, and X. Sun, “Power losses in two- and three-level three phase photovoltaic inverters equipped with igbts,” in *2012 15th International Conference on Electrical Machines and Systems (ICEMS)*, 2012, pp. 1–6.

[37] M. Aydin and E. Beşer, “Power loss and thermal temperature calculation of igbt module by mathematical equations,” in *2023 International Conference on Power Energy Systems and Applications (ICoPESA)*, 2023, pp. 862–867. DOI: 10.1109/ICoPESA56898.2023.10141374.

[38] J. Falck, M. Andresen, and M. Liserre, “Active thermal control of igbt power electronic converters,” Nov. 2015, pp. 000 001–000 006. DOI: 10.1109/IECON.2015.7392925.

[39] Z. Wang, H. Wang, Y. Zhang, and F. Blaabjerg, “Submodule level power loss balancing control for modular multilevel converters,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 5731–5736. DOI: 10.1109/ECCE.2018.8557496.

[40] J. Liu, J. Yao, S. Yang, and K. Wang, “Loss analysis of two kinds of flexible hvdc converters,” in *Proceedings of The 7th International Power Electronics and Motion Control Conference*, vol. 3, 2012, pp. 1669–1674. DOI: 10.1109/IPEMC.2012.6259086.

[41] Wintrich, Nicolai, Tursky, and Reimann, “Application manual power semiconductors,” SEMIKRON International GmbH, 2015, pp. 41–42.

[42] Z. Wang, B. Tian, W. Qiao, and L. Qu, “Real-time aging monitoring for igbt modules using case temperature,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1168–1178, 2016. DOI: 10.1109/TIE.2015.2497665.

[43] Y. Liu, J. Sheng, Y. Dong, *et al.*, “Thermal analysis of modular multilevel converters under subsynchronous oscillation,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 5190–5195. DOI: 10.1109/ECCE.2018.8558414.

[44] H. Ding, F. Ma, R. Han, L. Lin, Q. Xu, and Y. Kuang, “A junction temperature balance control among sub-modules for modular multilevel converter,” in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–6. DOI: 10.1109/IECON48115.2021.9589962.

[45] S. B. C. RATHKE, J. L. J. DORN, Z. S. C. PLET, C. D. Y. FU, R. O. Q. LI, and Y. Z. B. SHENG, “Feasibility study for assessment of lab losses measurement of vsc valves,” Sep. 2021. DOI: 844.

[46] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, “Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter,” *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590–602, 2015. DOI: 10.1109/TPEL.2014.2312335.

[47] X. Wang, Z. Li, F. Yao, and S. Tang, “Simplified estimation of junction temperature fluctuation at the fundamental frequency for igbt modules considering mission profile,” *IEEE Access*, vol. 7, pp. 149 308–149 317, 2019. DOI: 10.1109/ACCESS.2019.2947346.

[48] A. Giannakis and D. Peftitsis, “Electro-thermal design of a solid-state mvdc circuit breaker,” in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019, pp. 1–8. DOI: 10.23919/ICPE2019-ECCEAsia42246.2019.8797031.

[49] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, “Converter structure-based power loss and static thermal modeling of the press-pack igbt three-level anpc vsc applied to multi-mw wind turbines,” *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2505–2515, 2011. DOI: 10.1109/TIA.2011.2168557.

[50] O. Senturk, “High power density power electronic converters for large wind turbines,” English, Ph.D. dissertation, 2011, ISBN: 978-87-92846-00-6.

[51] K. Murashko, H. Wu, J. Pyrhönen, and L. Laurila, “Modelling of the battery pack thermal management system for hybrid electric vehicles,” Aug. 2014. DOI: 10.1109/EPE.2014.6910774.

[52] R. Gupta, “A simulink model for an engine cooling system and its application for fault detection in vehicles,” 2015.

[53] D. W. Spier, E. Prieto□Araujo, O. Gomis□Bellmunt, and J. López-Mestre, “Analytic estimation of the mmc sub-module capacitor voltage ripple for balanced and unbalanced ac grid conditions,” *ArXiv*, vol. abs/2109.00310, 2021.

[54] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, “Modulation and submodule energy balancing,” in *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. 2016, pp. 232–271. DOI: 10.1002/9781118851555.ch5.

[55] A. Marquez, J. I. Leon, S. Vazquez, L. G. Franquelo, and M. Perez, “A comprehensive comparison of modulation methods for mmc converters,” in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 4459–4464. DOI: 10.1109/IECON.2017.8216768.

[56] R. Li, J. E. Fletcher, L. Xu, and B. W. Williams, “Enhanced flat-topped modulation for mmc control in hvdc transmission systems,” *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 152–161, 2017. DOI: 10.1109/TPWRD.2016.2561929.

[57] Z. Yang, J. Zhao, S. Wang, and C. Zhang, “A capacitors voltage balancing control strategy of mmc sub-modules based on dynamic threshold for pv system,” in *2021 40th Chinese Control Conference (CCC)*, 2021, pp. 5965–5970. DOI: 10.23919/CCC52363.2021.9550115.

[58] L. Mathe, P. D. Burlacu, and R. Teodorescu, “Control of a modular multilevel converter with reduced internal data exchange,” *IEEE Transactions on Industrial Informatics*, vol. 13, no. 1, pp. 248–257, 2017. DOI: 10.1109/TII.2016.2598494.

[59] Z. Bai, H. Xia, H. Ma, and J. Wang, “Mmc capacitor voltage balancing strategy based on carrier rotation,” in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, 2018, pp. 1–5. DOI: 10.1109/PEAC.2018.8590333.

[60] C.-K. Kim, J.-W. Kang, and Y.-B. Yoon, “Margin calculation of vsc hvdc modules based on mmc,” in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 2544–2550. DOI: 10.1109/IECON.2016.7793317.

[61] M. Ciappa, “Selected failure mechanisms of modern power modules,” *Microelectronics Reliability*, vol. 42, no. 4, pp. 653–667, 2002, ISSN: 0026-2714. DOI: https://doi.org/10.1016/S0026-2714(02)00042-2. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271402000422.

[62] M. Hernes, S. D’Arco, A. Antonopoulos, and D. Peftitsis, “Failure analysis and lifetime assessment of igbt power modules at low temperature stress cycles,” *IET Power Electronics*, vol. 14, no. 7, pp. 1271–1283, 2021. DOI: https://doi.org/10.1049/pel2.12083. eprint: https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/pel2.12083. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/pel2.12083.

[63] M. Musallam, C. M. Johnson, C. Yin, C. Bailey, and M. Mermet-Guyennet, “Real-time life consumption power modules prognosis using on-line rainflow algorithm in metro applications,” in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 970–977. DOI: 10.1109/ECCE.2010.5617883.

[64] M. Hernes, S. D'Arco, A. Antonopoulos, and D. Peftitsis, "Failure analysis and lifetime assessment of igbt power modules at low temperature stress cycles," *IET Power Electronics*, vol. 14, no. 7, pp. 1271–1283, 2021. DOI: https://doi.org/10.1049/pel2.12083. eprint: https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/pel2.12083. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/pel2.12083.

[65] H. Liu, K. Ma, P. C. Loh, and F. Blaabjerg, "Lifetime estimation of mmc for offshore wind power hvdc application," in *2014 International Power Electronics and Application Conference and Exposition*, 2014, pp. 35–40. DOI: 10.1109/PEAC.2014.7037825.

[66] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of igbt modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, 2008, pp. 1–6.

[67] L. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Lifetime prediction of igbt in a statcom using modified-graphical rainflow counting algorithm," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 3425–3430. DOI: 10.1109/IECON.2012.6389349.

[68] Z. Chen, F. Gao, C. Yang, T. Peng, L. Zhou, and C. Yang, "Converter lifetime modeling based on online rainflow counting algorithm," in *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, 2019, pp. 1743–1748. DOI: 10.1109/ISIE.2019.8781196.

[69] K. Hectors and W. De Waele, "Cumulative damage and life prediction models for high-cycle fatigue of metals: A review," *Metals*, vol. 11, Jan. 2021. DOI: 10.3390/met11020204.