Wafer scale fabrication of Josephson junctions

by

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Abstract

In this thesis variations in the Josephson junction conductance across a 100 mm wafer are studied. For this study junctions fabricated with a Dolan bridge and with the Manhattan layout are used. These junctions are fabricated on a planar and a non-planar NbTiN base layer to characterise the uniformity. On a planar base junctions fabricated with a Dolan bridge showed higher uniformity and yield than junctions with the Manhattan layout. On a non-planer base junctions fabricated with a Manhattan layout showed a higher uniformity than the Dolan bridge junctions. This can be attributed to the through silicon vias, which affect the resist spinning required for the Dolan bridge.

Manhattan style junctions are fabricated on a Si base layer in an attempt to improve the uniformity across a 100 mm wafer. By fabricating junctions on Si overall fabrication complexity is reduced, while also reducing the fabrication time. These junctions are used to investigate the role of oxygen ashing prior to the junction deposition. We find that the ashing increase the uniformity of the junctions, however, further attempts to improve the uniformity using different ashing steps did not how any additional improvements.

Finally, to explain the variations in Manhattan style junctions a geometric model is introduced. This model is based on the thickness of the top resist stack, which could potentially affect the width of the junction electrodes. The model is compared with SEM images and with the coefficient of variation. The model shows correspondence with the SEM data, but overestimates the variations when compared with the coefficient of variation.

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1 Introduction

This chapter gives an introduction on why there is an interest in the field of quantum mechanics followed by the objective of this thesis. Finally an overview of the chapters in this work is given.

1.1. Motivation

In the last few decades the field of quantum mechanics has received a lot of attention. Governments and companies such as Google, Amazon, IBM and Microsoft are investing heavily in the field in order to speed up the progress. But why is this field of such interest and why are companies investing in the field as well?
It turns out that quantum mechanics can be used to create a quantum computer. Where a classical computer uses bits that can either be a 0 or a 1, a quantum computer uses quantum bits, also known as qubits. These qubits obey the laws of quantum mechanics and can therefore be in a superposition of 0 and 1 at the same time. Due to this unique property a quantum computer is able to solve certain problems faster than a classical computer. A textbook example of this is Shor's algorithm [1], which uses prime factorization to break the RSA encryption which is used for secure data transmission.
The problem with quantum computers is that it is still unknown how to build a large quantum computer that is able to solve non-trivial problems. This is also the reason that governments and companies are investing in the field, every party wants to be the first to build a quantum computer. While there are multiple platforms to build a quantum computer, such as nitrogen-vacancies in diamond, trapped ions, quantum dots and Majorana zero modes, most companies focus on the same platform, superconducting qubits. This platform has the advantage that it is compatible with current CMOS and microwave control technology.
In this thesis the emphasis lies on the *transmission line shunted plasma oscillation qubit* [2], also known as the transmon qubit. The transmon is a form of a superconducting qubit, which uses a capacitor in parallel with a Josephson junction to create an an-harmonic oscillator. By confining the computational subspace to the lowest two energy levels of the oscillator it is possible to create a qubit. This qubit operates at a certain frequency, which is determined by the capacitance and the inductance of the electrical circuit. This frequency is an important parameter for the performance of a chip with multiple qubits, also known as a superconducting quantum processor. In such a processor the qubits are divided into three frequency groups, in which ideally all qubits of the same group have the same frequency. If the qubit frequencies within a certain group differ too much from each other the processor will not function properly.
As the number of physical qubits on a superconducting quantum processor increases, it becomes more difficult to connect all the wires required for the control of the qubits. In order to overcome this problem through silicon vias are introduced, these vias can be used as 3D interconnects to allow for the control of all the qubits on a chip. The downside of these vias is that they affect the resist spinning, which results in a non-uniform thickness. Currently a critical piece of the superconducting qubit, called the Josephson junction, requires a uniform resist thickness, which poses a problem for the fabrication of superconducting qubits. In order to solve this problem a different type of Josephson junction that is less sensitive to resist thickness variations is currently investigated in the field.

1.2. Objective

This thesis focuses on characterising and improving the frequency targeting of superconducting qubits during wafer-scale fabrication. This goal is investigated by studying a critical feature of the qubit, the Josephson junction. The Josephson junction conductance obtained from room temperature measurements is directly related to the qubit frequency according to the Ambegaokar-Baratoff relation [3]. Therefore, the objective of this thesis is to quantify and improve the uniformity of the Josephson junction conductance across a 100 mm wafer.

1.3. Outline

This thesis is structures into five different chapters.
Chapter 2 (Theory) provides a brief introduction on Josephson junctions and the physics behind the transmon qubit that is of interest for this thesis. Such as the relation between the frequency targeting of a qubit and the room temperature resistance measurements.
Chapter 3 (Junction Characterisation) determines the variations in the Josephson junction conductance using the current fabrication recipe on a NbTiN base layer.
Chapter 4 (All Aluminum Junctions) describes the experiments performed to study the junction uniformity using a simplified fabrication process. This process reduces the number of fabrication steps and thus variables.
Chapter 5 (Model) discusses a geometric model that could explain the variations in the Josephson junction conductance.
Chapter 6 (Conclusions and Outlook) summarizes the results of this thesis and gives an outlook on further research that is relevant for the fabrication of transmon qubits.

2

Theory

This chapter gives a brief introduction on the concept of superconductivity and how this phenomena can be used to create a Josephson junction. This junction is used to create a superconducting qubit. Building on this the surface code and its importance is introduced and discussed. Lastly, the fabrication steps required to create Josephson junctions on a wafer are discussed.

2.1. Superconductivity

A concept that is important for the fabrication of superconducting qubits is superconductivity itself. In 1911 H. Kamerlingh Onnes discovered that the resistance of a solid mercury vanishes if the wire is cooled below 4.2 K [4]. Later he discovered that the resistance of other materials such as lead and tin also vanishes below a certain critical temperature T_c. This is the first hallmark of a superconductor, perfect conductivity. Later in 1933 Meissner and Ochsenfeld discovered another hallmark, perfect diamagnetism [5], in which a magnetic field is excluded from entering a superconductor up to some critical magnetic field known as the Meissner effect. Applying a magnetic field stronger than the critical magnetic field will break superconductivity. Similarly, applying a current above the critical current will break this superconductivity as well. The cause of these properties of a superconductor were unclear for quite some time, until 1950 when Ginzburg and Landau proposed the macroscopic theory of superconductivity [6]. While this theory gives a description of superconductivity, the microscopic behaviour of superconductivity remained elusive, until 1957 when John Bardeen, Leon Cooper and John Robert Schrieffer proposed a microscopic theory of superconductivity [7–10], now known as BCS-theory.

2.1.1. BCS Theory

The Bardeen-Cooper-Schrieffer theory explains superconductivity based on the formation of Cooper pairs by an attractive interaction between two electrons. Under normal circumstances electrons repel each other due to the Coulomb interaction. However, it is possible to overcome the Coulomb interaction, which allows the electrons to bond and form a Cooper pair. An example of this pairing can be given using a simple lattice of a metal. In this case the electron moves through the metal, where it is repelled by other electrons due to their negative charge and it is attracted to ions in the lattice that have a positive charge. This attractive force is able to create a small displacement in the lattice in the form of a phonon. In this case the charge density will be locally increased, which attracts another electron. The force at which both electrons are attracted is large enough to overcome the Coulomb interaction, thus allowing the electrons to bond and form a Cooper pair. The bonding of the electrons is quite weak and is therefore easily broken if the thermal energy is too high. If the thermal energy decreases it becomes more difficult to split the Cooper pairs into electrons, at some point the thermal energy is too low and the Cooper pairs are not split into electrons anymore. The temperature corresponding to this thermal energy is called the critical temperature. Below this temperature the fermionic electrons in the metal will form bosonic Cooper pairs. The Cooper pairs obey Bose-Einstein statistics and are therefore able to occupy only the ground state of the system. If all the electrons in the material form Cooper pairs and occupy the ground state the resistance of the material vanishes. This can be explained by the fact that the electrons normally cause the resistivity in a material, but when all the electrons form Cooper pairs, there are no electrons left to create the resistivity.

2.1.2. Superconducting Materials

There is a wide array of materials that become superconducting below a certain temperature, T_c, also known as the critical temperature. However, only a small number of these materials are used in circuit quantum electrodynamics (cQED). In cQED, the superconducting materials are used for the coherent transport of signals throughout the superconducting circuit. The choice of the superconducting material depends on various factors, such as material properties and compatibility with fabrication processes. For the material properties such as the critical current, dielectric losses and the magnetic field tolerance are important. In this section, a number of materials and compounds explored in cQED are discussed, in general elemental materials are more popular because film depositions are relatively simple and stable [11]. The downside of pure materials is that these often form a thin oxide layer at the surface, which can house two-level systems (TLS), which are identified to be a dominant source of losses. For each material, the critical temperature is given, whereas for the compounds a range is given, as the critical temperature depends on the composition of each element in the compound.

- Aluminum (Al): $T_c \approx 1.2$ K
  The material of choice for the fabrication of Josephson junctions, however it can also be used as the superconducting base layer. Al has a small superconducting band gap of 0.3 meV, a low critical temperature of $T_c = 1.2$ K and a relative long quasi particle life time [12], which can affect the performance of the transmon qubits. Al oxidises when exposed to air, which allows for TLS to form on top of the base. Even though that Al has some disadvantage properties it has been used in high performance superconducting quantum processors, such as Google's Sycamore processor, used to demonstrate quantum supremacy [13].

- Niobium (Nb): $T_c \approx 9.3$ K
  At first glance pure Nb appears to be a suitable choice of superconducting material, it has a high T_c and a large superconducting band gap. However, it turns out that Nb has a few downsides. The first is the complex stoichiometry of Nb forms with O_2 (NbO, NbO_2, Nb_2O_5), which are able to house TLS and thus losses. Secondly, Nb is observed to have a larger density of sub-gap states than materials with a lower T_c, such as Al, which corresponds to more thermally excited quasi-particles and shorter coherence times [14, 15]. In order to overcome these problems, compounds of Nb and other materials are explored for superconducting base layers, such as NbN and NbTiN. In another study, deposited Nb was exposed with nitrogen in order to replace the formation of surface oxides with nitrides, however measurements showed that there were still oxides present on the film, indicating that this is not a feasible solution [16].

- Niobium Nitride (NbN): $T_c \approx 8 - 16$ K
  Adding N to Nb allows for a high T_c and high critical magnetic field, while potentially reducing losses due to TLS by removing surface oxides. The downside of NbN is the short superconducting coherence length, which causes problems for the fabrication of high-quality tunnel junctions, and the long magnetic penetration depth which limits its application in high frequency superconducting circuits [17].

- Titanium Nitride (TiN): $T_c \approx 0 - 6$ K
  TiN is used in superconducting microwave kinetic inductance detectors [18] and has also been used in superconducting qubits [19]. This compound is very hard and robust and has been used to create high quality resonators ($Q_i > 10^7$) while having a long quasi-particle lifetime ranging from 10-200 µs [18]. The nitrogen is added to increase the T_c of the compound, where the highest T_c and lowest film resistivity is measured for films where the stoichiometry was correct i.e. 1:1 Ti:N. It is hypothesized that the N at the surface would prevent the oxidation of the film and would thus reduce the TLS population. However, it is found that TiN also form a thin oxidation layer on top of the film, thus still allowing for the presence of TLS. [15, 20–22].

- Niobium Titanium Nitride (NbTiN): $T_c \approx 15 - 18$ K
  NbTiN is a compound with a high critical temperature, large superconducting band gap, little microwave phase noise and microwave loss. NbTiN is heavily used in the field of astronomy due to its ability to operate in a large frequency range. It has similar applications and properties as NbN, but the addition of Ti to the compound allows for the metallic and structural benefits of TiN. In this compound, the N allows for a high T_c and stability in air. The addition of N should also prevent the formation of surface oxides and thus reduce losses due to TLS. [23, 24].

- Tantalum (Ta): $T_c \approx 4.5$ K
  Ta is a relatively new material in the field of cQED, but one that attracts a lot of attention. Using a Ta base layer on a sapphire substrate transmon qubits with a relaxation time (T_1) exceeding 0.3 ms [25] and 0.5 ms [11] have been fabricated. The current hypothesis is that the insulating oxide layer that forms on the Ta allows for a better metal air interface and it thus allows for lower losses when compared to Nb, that has a more complicated stoichiometry [11, 25].

2.2. Josephson Junction

In 1962 B.D. Josephson predicted the mathematical relation between the current and the voltage between two superconductors separated by an insulator [26], also known as a weak link. This type of junction is known as a superconductor-insulator-superconductor (SIS) junction. It is also possible to fabricate a junction using a normal metal between the two superconductors, which is known as a superconductor-normal metal-superconductor (SNS) junction. The requirement on the insulator separating the two superconductors is that it should be thin enough, such that Cooper pairs can quantum mechanically tunnel through the barrier. A schematic representation of a Josephson junction can be seen in figure 2.1. Here two superconducting materials with phase ϕ_L and ϕ_R are separated by an inductive layer with a current I_J going through the junction. In a Josephson junction, the current and voltage are described by the Josephson equations

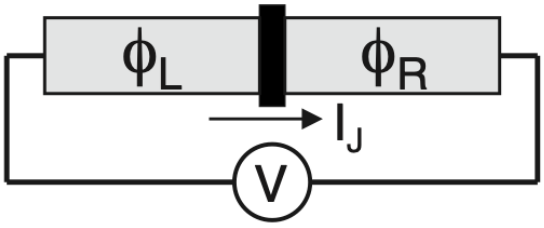


Figure 2.1: Schematic representation of a Josephson junction connected to a bias voltage V. Two superconducting materials with phase ϕ_L and ϕ_R respectively are separated by an insulating barrier. Figure taken from [27].

$$I_J = I_C \sin(\varphi) \tag{2.1}$$

$$V = \frac{\Phi_0}{2\pi}\frac{d\varphi}{dt} \tag{2.2}$$

where I_J is the current through the Josephson junction, I_C is the critical current, $\varphi = \phi_L - \phi_R$ is the superconducting phase difference, V is the current over the junction and $\Phi_0 = h/2e$ is the superconducting flux quantum, with h Planck's constant and e the electron charge. The critical current I_C can be determined according to

$$I_C = \frac{\Delta_1(T)}{R_N} K\left(\left(1 - \frac{\Delta_1^2(T)}{\Delta_1^2(T)}\right)^{1/2}\right) \tag{2.3}$$

where $\Delta_1(T)$ is the smallest of the two temperature dependent superconducting band gaps and $\Delta_2(T)$ is the larger one, $K()$ is the complete elliptical integral of the first kind and R_N is the normal junction resistance [3]. In case that the same material is used for both electrodes of the Josephson junction i.e. $\Delta_1(T) = \Delta_2(T)$ and thus $K(0) = \frac{1}{2}\pi$ equation (2.3) reduces to

$$I_C = \frac{\pi\Delta(T)}{2R_N} \tag{2.4}$$

This simplified equation can be used to determine the critical current of a Josephson junction from room temperature resistance measurements, which will be discussed in further detail later on.
Another important property of the Josephson junction is the inductance. Using equations (2.1) and (2.2) the inductance, L_J, can be calculated

$$L_J = \frac{V}{dI_J/dt} = \frac{\Phi_0}{2\pi I_0 \cos(\varphi)} \tag{2.5}$$

here we used the fact equation (2.1) can be rewritten as $\frac{\partial I_J}{\partial \varphi} = I_0 \cos\varphi$ and the property $\frac{dI}{dt} = \frac{\partial I}{\partial \phi}\frac{\partial \phi}{\partial t}$. From equation (2.5) it becomes clear that the inductance is non-linear due to the $\cos(\varphi)$ dependence. The inductance has an oscillating behaviour and reaches a maximum at $\varphi \to \pi/2$ and becomes negative for $\pi/2 < \varphi < 3\pi/2$.

This non-linear behaviour of the Josephson junction is important for the fabrication of a superconducting qubit, which is discussed later on [28].

2.2.1. SQUID

Superconducting qubits often use two Josephson junctions in parallel to form a superconducting quantum interference device (SQUID). SQUID's are used as they allow for the tuning of the Josephson coupling energy [2]. In a SQUID the superconducting phase φ becomes important as the phase can be different for both Josephson junctions. The Josephson current through the SQUID is simply the sum of the individual Josephson junctions

$$I_{J,SQUID} = I_{C,1}\sin(\varphi_1) + I_{C,2}\sin(\varphi_2) \tag{2.6}$$

where $I_{C,n}$ is the critical current and φ_n is the superconducting phase for each Josephson junction respectively [28]. These parameters $I_{C,n}$ and φ_n depend on the physical properties of the Josephson junction such as the size and materials. In case that a symmetric SQUID is used equation (2.6) can be written as

$$I_{J,SQUID} = 2I_C\cos\left(\frac{\varphi_1-\varphi_2}{2}\right)\sin\left(\frac{\varphi_1+\varphi_2}{2}\right) \tag{2.7}$$

in the case that an asymmetric SQUID is used the critical current through each junction in the SQUID becomes different and the equation becomes more complicated. In this work only symmetric SQUID's are used and therefore the asymmetric case is not considered. When a magnetic field is applied perpendicular to the plane of the SQUID, the superconducting phase is shifted. The phase shift in the SQUID obeys the relation $\varphi_1 - \varphi_2 = -2\pi\frac{\Phi}{\Phi_0}$, where Φ is the magnetic flux through the SQUID [29]. In this case the Josephson current can be written as

$$I_J = 2I_C\cos\left(\pi\frac{\Phi}{\Phi_0}\right)\sin\left(\varphi_2+\pi\frac{\Phi}{\Phi_0}\right) \tag{2.8}$$

From which we find that the Josephson current depends on the magnetic flux through the SQUID. It is important to note that this equation only holds when the Josephson current does not exceed the critical current. For the SQUID the critical current can be expressed as

$$I_{C,SQUID} = 2I_C\left|\cos\left(\pi\frac{\Phi}{\Phi_0}\right)\right| \tag{2.9}$$

Finally the inductance of the SQUID can be determined using $L_J = \frac{V}{dI_J/dt}$, the way as for the single Josephson junction. From this we find

$$L_{SQUID} = \frac{\Phi_0}{2I_C\cos\left(\pi\frac{\Phi}{\Phi_0}\right)\cos\left(\varphi_2+\frac{\Phi}{\Phi_0}\right)} \tag{2.10}$$

From which we find that similar to the Josephson current through the SQUID the inductance also depends on the magnetic flux through the SQUID. This allows for the flux tunability of the qubit frequency, which is discussed later on.

2.2.2. Al/AlO_x Properties

The most common material used for the fabrication of Josephson junctions in superconducting qubits is aluminum. Al has the advantage that it oxidizes when exposed to O_2, resulting in the formation of a thin layer ($\approx 2-3$ nm) of AlO_x on top of the Al. This property allows for the fabrication of a Josephson junction in a single electron beam step by using a double angle evaporator and thus Al is compatible with methods such as a Dolan-bridge and the Manhattan layout. Al has a superconducting band gap of 0.3 meV, which allows for small junctions. The problem with this material is that two-level defects in the amorphous AlO_x tunnel barrier are identified to limit the performance of the superconducting qubit [30, 31]. A study by Zeng et al. [32] showed that due to non-uniformities in the bottom electrode and the formation of the tunnel-barrier less than 10% of the junction area dominates in the electron tunneling. The roughness of the substrate on which the electrodes are deposited directly affects the roughness of the electrode and thus the tunnel-barrier. In order to reduce this effect it is important to create a smooth surface for the deposition of the electrodes.

A study on the influence of the deposition method used on the AlO_x barrier is conducted by Fritz et al. [33]. This study involved three different deposition machines with different operating settings. One of these machines is a Plassys-MEB550, which is the same machine used at the DiCarlo lab to fabricate Josephson

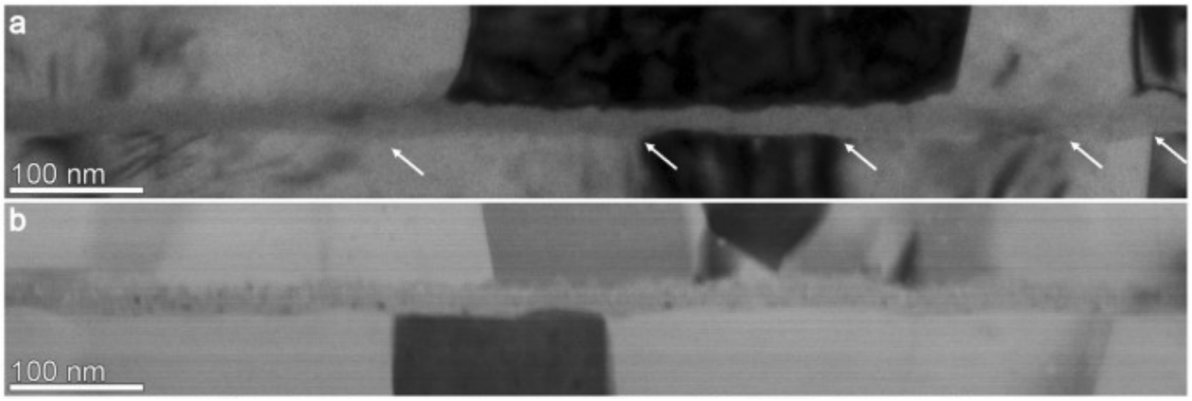


Figure 2.2: TEM images of a Al/AlO_x/Al junction fabricated. In figure a the AlO_x barrier is formed with dynamic oxidation using pure O_2. The white arrow points to grain boundaries. In figure b the AlO_x barrier is formed with dynamic oxidation using pure O_2 in the presence of UV-illumination to enhance dynamic oxidation. Figure taken from [33].

junctions. This study used transmission electron microscopy (TEM) to study the transition between the Al/AlO_x/Al layers. Two TEM images of a Al/AlO_x/Al barrier fabricated using the Plassys can be seen in figure 2.2. The Al layers are present at the top and bottom of the image and are separated by a 20-30 nm AlO_x layer and are obtained by multiple deposition and oxidation steps. The top figure corresponds to Al/AlO_x/Al junction formed using dynamic oxidation in pure oxygen and the bottom figure corresponds to Al/AlO_x/Al junction formed using dynamic oxidation in pure oxygen in the presence of UV-illumination to enhance dynamic oxidation. When the top and bottom are compared we find that the Al/AlO_x/Al formed in the presence of UV shows a smoother interface with less grain boundaries.

It is important to note that AlO_x tunnel barriers suffer from a process called aging. Aging refers to the instability of the AlO_x tunnel barrier over time. This instability is attributed to the diffusion of oxygen atoms from the oxide barrier to the electrode and the change of the chemical composition of the barrier [34, 35]. This aging is able to increase or decrease the conductance of the Josephson junction. This can be exploited to change the conductance post fabrication in order to obtain the desired frequency value [36, 37]. Aging of the junctions can be suppressed by nitridation of the electrodes, nitrides are chemically more stable therefore show less signs of aging. It has been shown that aging is affected by contaminations around the area where the electrodes are deposited. By cleaning the substrate with ethanol and isopropylalcohol (IPA) or isotropic reactive ion etching (RIE) the effect of aging can be reduced, where junction fabricated on the RIE cleaned surface showed no aging. Isotopic etching is required since areas with a large undercut need to be cleaned [34].

Koppinen et al. [38] showed that junctions annealed at 200 °C and 400 °C showed an increase in the resistance of 50% and 300% respectively. During this process the junction area was not cleaned. Pop et al. [34] showed that junction fabricated on an area cleaned with RIE are stable when annealed at 200 °C. In this same study, junctions are annealed at 200 °C with a layer of polymethyl methacrylate (PMMA) resist on top of it. In this case, a decrease in the junction resistance is observed. This change is attributed to hydrates (-OH) from the resist, which combine with the oxides on the aluminum. The resistance was measured a week later, which showed an increase in the junction resistance. When the junctions are again annealed at 200 °C with PMMA resist on it, the resistance decreased again. A measurement four weeks later again showed an increase in the resistance. The increase/relaxation behaviour can be explained by the hydrates that are absorbed during the annealing process and are desorbed during the storage of the junctions.

2.2.3. Josephson Junction Types

In this work two methods to fabricate Josephson junctions are used, the first method utilizes a Dolan bridge [39, 40] and the second method is based on the Manhattan design [41]. Here Josephson junctions fabricated using one of these techniques will be referred to as Dolan bridge junctions and Manhattan junctions.
A Dolan bridge is a connection between two parts of a resist layer between two exposed parts on top of another over exposed resist layer. A schematic representation of the cross section of a Dolan bridge can be seen in figure 2.3. In this design, metal is deposited from direction 1 under a tilt θ, followed by an oxidation step to create the oxide layer. The second layer of metal is deposited from direction 2 under the same tilt θ, thus by rotating the sample 180°. The overlap area between the top and bottom electrode can be defined by determining the amount of material deposited under the bridge, which can be calculated for the bottom electrode as

$$L_{Bottom} = R_H / \tan(\theta) \tag{2.11}$$

where L_{Bottom} is the length of the bottom electrode under the Dolan bridge, R_H is the height of the bottom resist and θ is the angle of the incident material. The same calculation can be used for the top electrode, but with the thickness of the bottom electrode being subtracted from the height.

$$L_{Top} = (R_H - T_{Bottom}) / \tan(\theta) \tag{2.12}$$

where L_{Top} is the length of the bottom electrode under the Dolan bridge and T_{Bottom} is the thickness of the bottom electrode. In this case the overlap area can be determined by the length of the top and bottom electrode overlap multiplied by the width of the top electrode

$$A_{Dolan,top} = (L_{Top} + L_{Bottom} - L_{Bridge}) W_{Top} \tag{2.13}$$

where $A_{Dolan,top}$ is the overlap area of the Dolan bridge junction, L_{Bridge} is the length of the Dolan bridge and W_{Top} is the width of the top electrode. In a typical Dolan bridge junction the top electrode has a smaller width than the bottom electrode, therefore only the width of the top electrode is relevant. In the Dolan bridge junction, the contribution of the sidewall between the top and bottom electrode can also be taken into account, which would add a contribution of

$$A_{Dolan,side} = T_{Bottom} W_{Top} \tag{2.14}$$

where $A_{Dolan,side}$ is the contributions of the sidewall to the overlap area. In this case the total overlap is defined as

$$A_{Dolan} = A_{Dolan,top} + A_{Dolan,side} \tag{2.15}$$

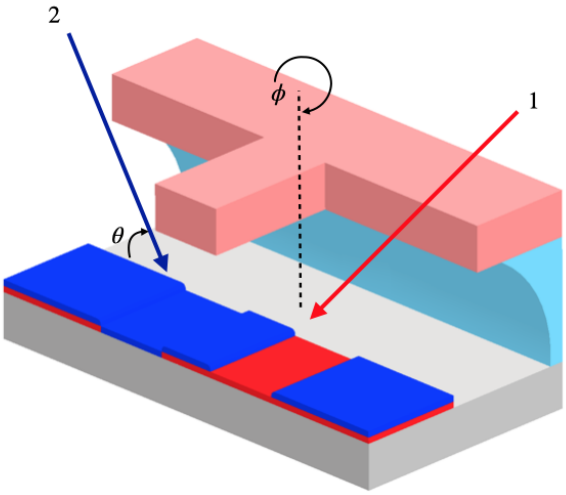


Figure 2.3: Schematic representation of the resist stack used for the fabrication of Dolan bridge junctions. The top resist layer is used to create a Dolan bridge. The color correspond to: Red - first metal deposition, Blue - second metal deposition, Grey - Si, Light Blue - PMGI, Light Red - PMMA.

The advantage of Dolan bridge junctions is that spinning resist allows for an uniform layer, thus allowing uniform fabrication of junctions across a sample. The downside of Dolan bridge junctions is that the resist spinning requires a relatively flat substrate in order to spin an uniform layer. In the case of through silicon vias (TSV) this requirement is not met, which results in variations in the Dolan bridge junction fabrication process.

The Manhattan junction is a bridgeless junction that is less sensitive to resist height variations than the Dolan bridge. A schematic representation of the layout used to fabricated Manhattan style junctions can be seen in figure 2.4. Here a thick top resist layer is used to create the pattern for the deposited material, while a thin bottom resist layer is used to promote lift-off. The metal is deposited from direction 1 under a tilt θ, followed by an oxidation step to create the oxide layer. Then the substrate is rotated around the φ axis by 90° followed by another deposition under a tilt θ. For this process it is important that the resist stack thickness T_{resist}, junction width W and the tilt θ obey the following relation.

$$T_{resist} > W / \tan(\theta) \tag{2.16}$$

If this relation is not satisfied, material of the first deposition is deposited in the opening for the second deposition, resulting in problems in the Josephson junction. In case that there is a misalignment α between the axis of rotation and the width of the junction, the relation becomes:

$$T_{resist} > W / (\tan(\theta)\cos(\alpha)) \tag{2.17}$$

The overlap area of the Manhattan style junctions can be calculated by multiplying the width to the top and bottom electrode

$$A_{Top} = W_{Bottom} W_{Top} \tag{2.18}$$

Where A_{Top} is the overlap area, W_{bottom} is the width of the bottom electrode and W_{Top} is the width of the top electrode. For the Manhattan junctions the area on the side of the bottom electrode can also be taken into account, these add a contribution of

$$A_{Side} = 2 W_{Top} T_{Bottom} \tag{2.19}$$

here the factor of 2 is added, since there is a sidewall on both sides of the junction. The advantage of the Manhattan style junction is that it is less sensitive to resist height variations. This advantage becomes important as the number of physical qubits on a processor increases. In order to connect all the wires to the processor 3D interconnects are necessary, which will affect the uniformity of resist spinning. Figure 2.5 shows scanning electron microscope (SEM) images of both type of Josephson junction fabricated on a NbTiN base.

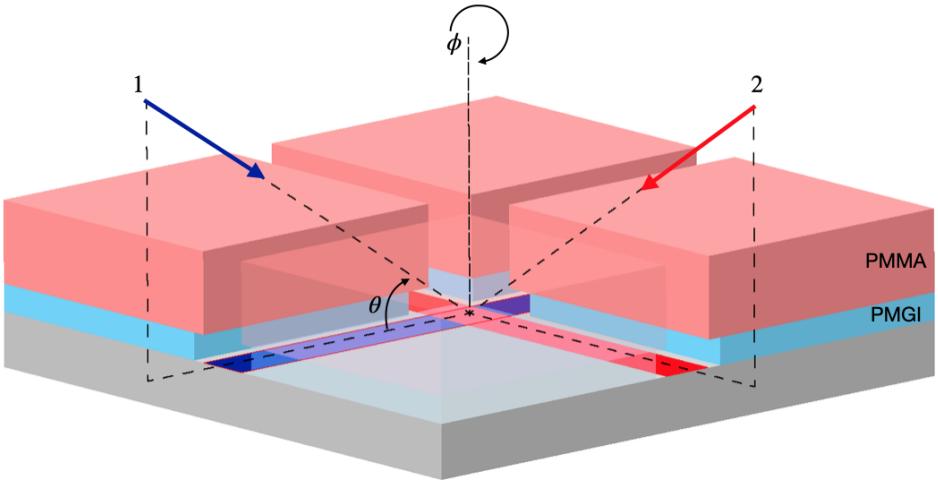
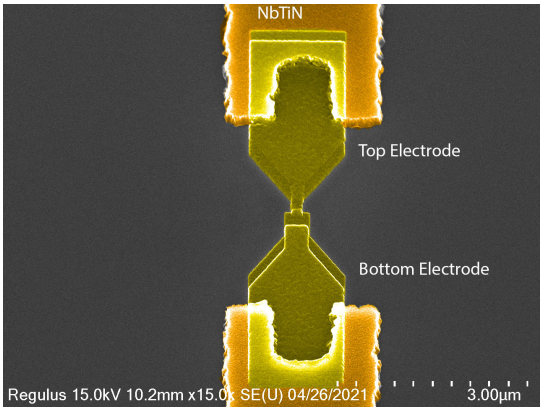
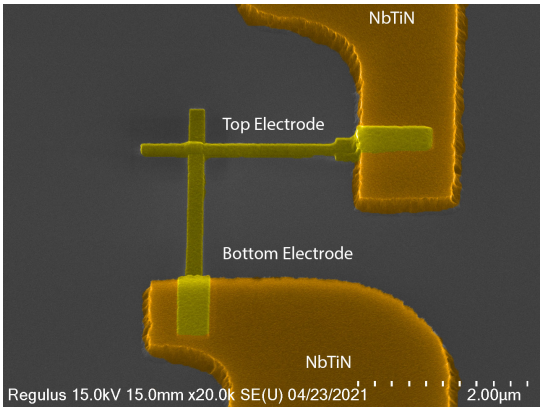


Figure 2.4: Schematic representation of the resist stack used for the fabrication of Manhattan junctions. The color correspond to: Red - first metal deposition, Blue - second metal deposition, Grey - Si, Light Blue - PMGI, Light Red - PMMA.



(a) False colored SEM image of a Dolan bridge junction at 15k magnification.



(b) False colored SEM image of a Manhattan junction at 20k magnification.

Figure 2.5: False colored SEM images of both Josephson junctions types at a 45° tilt. The aluminum electrodes are yellow and the NbTiN base layer is orange.

2.3. Harmonic Oscillator

This non-linear inductance of the Josephson junction can be used in a LC-circuit to form an anharmonic quantum oscillator, opposed to the normally used harmonic quantum oscillator, which uses a normal inductor. Figure 2.6 shows both of these oscillators. Note that in the case of the harmonic oscillator the energy levels are degenerate and thus it is not possible to confine the lowest two energy levels. In the case of the anharmonic oscillator this degeneracy is broken by the Josephson junction, in this case the lowest two energy levels can be used as the computational subspace of the qubit. We also note that in the anharmonic oscillator it becomes apparent that the energy spacing between each consecutive level decreases. This is an important consideration as the higher energy levels become a source of leakage for the transmon qubits, thus the transition to these levels should be suppressed sufficiently.

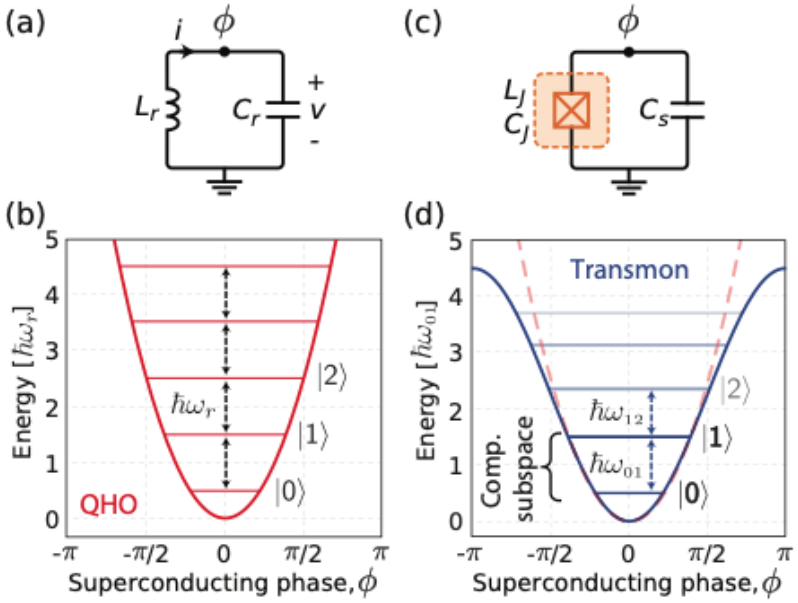


Figure 2.6: Comparison between a harmonic oscillator and an anharmonic oscillator. The harmonic oscillator is constructed by using a LC-circuit, whereas the anharmonic oscillator uses a Josephson junction instead of an inductor in the LC-circuit, to create an anharmonicity. In the anharmonic oscillator the energy spacing's between each level is different, which allows for the confinement of the computational subspace to the lowest two energy levels. Figure taken from [42].

2.4. Superconducting Qubits

Superconducting qubits are a promising platform to build a quantum computer in the future. Superconducting qubits have the advantage that they are highly designable, scalable, easy to couple to each other and relatively easy to control in comparison to other platforms [43]. The downside of these qubits is that they are not true 2-level systems, they are quite large and they require dilution refrigerators for operation.
In general, superconducting qubits use a Josephson junction to obtain an anharmonic oscillator. There are two main categories of superconducting qubits, namely the charge qubit and the flux qubit. These categories can be distinguished from each other by looking at the ratio of E_J/E_C in which they operate. The charge qubit operates in the regime of $E_J \ll E_C$. The flux qubit operates at around $1 \ll E_J/E_C \ll 100$. During the evolution of superconducting qubits new categories have arised, such as fluxonium [44] and the transmon [2] which is used in our lab.

2.4.1. Charge Qubit

The first superconducting qubit was proposed in 1998 by Bouchiat et al. [45], which was called the Cooper-pair box. This design consists of a single superconducting island connected to a superconducting electron reservoir by a Josephson junction. By designing the qubit such that it operates in the $E_J \ll E_C$ regime it is possible to determine the qubit state by the presence or absence of an extra Cooper pair on the superconducting island. The Hamiltonian of this system is given by

$$\hat{H} = 4E_{\mathrm{C}}\left(\hat{n} - n_{\mathrm{g}}\right)^2 - E_{\mathrm{J}}\cos\left(\hat{\phi}\right) \tag{2.20}$$

where $\hat{n}$ is the Cooper pair number operator, n_g is the offset, $\hat{\phi}$ is the phase difference operator E_J is the Josephson energy and E_C is the charging energy, which is defined as $E_C = \frac{e^2}{C}$, where C is the junction capacitance. Charge qubits have a large anharmonicity (> 10 GHz), but suffer from short dephasing times due to environmental charge noise. An adaptation of the charge qubit is the transmon, which uses a shunted capacitor in order to reduce the sensitivity to noise and improve the performance [46].

2.4.2. Flux Qubit

The flux qubit was proposed in 1999 by Mooij et al. [47]. The design consists of a superconducting loop with Josephson junctions in it. The Josephson junction can be used to remove or add a magnetic fluxon to the loop. The removal of addition of a fluxon results in a change in the direction of the current in the superconducting loop, which is used to define the qubit state. The direction of the current can be determined by measuring the flux generated by the loop with a DC SQUID [46, 47].

2.4.3. Transmon

The *transmission line shunted plasma oscillation qubit* or transmon qubit was first proposed by Koch et al. [2]. The transmon is a charge qubit with a shunted capacitor that operates in the regime where the charging energy is smaller than the Josephson energy, thus $E_J \gg E_C$. This suppresses the charge dispersion exponentially at the cost of decreasing the anharmonicity. Unlike the Cooper pair box, the transmon uses a DC-SQUID loop, thus consisting of two Josephson junctions. This allows the Josephson energy E_J to be tuned by using an external magnetic field. The effective Hamiltonian of the transmon is identical to that of the Cooper pair box system,

$$\hat{H} = 4E_C\hat{n}^2 - E_J\cos(\hat{\phi}) \tag{2.21}$$

where E_C is the charging energy, which is defined as $E_C = \frac{e^2}{C_\Sigma}$. The total capacitance C_Σ is the sum of the junction capacitance C_J and the shunt capacitance C_S. The Josephson energy for the transmon qubit is $E_J = E_{Jmax}|\cos(\pi\frac{\Phi}{\Phi_0})| = \frac{\Phi_0 I_C}{2\pi}|\cos(\pi\frac{\Phi}{\Phi_0})|$, where I_C is the critical current. Equation (2.21) can be expressed in terms of the creation ($\hat{a}^\dagger$) and annihilation ($\hat{a}$) operators and the zero-point fluctuations of charge and phase $\hat{n} = i\left(\frac{E_J}{32E_C}\right)^{\frac{1}{4}}(\hat{a} - \hat{a}^\dagger)$ and $\hat{\phi} = \left(\frac{2E_C}{E_J}^{\frac{1}{4}}\right)(\hat{a} + \hat{a}^\dagger)$ [2, 42, 48]. Transmon qubits operate in the regime $E_J/E_C \gg 1$, thus $\hat{\phi} \ll 1$. Therefore, we can take a Taylor expansion of $\cos\hat{\phi}$, which will results in

$$H = \sqrt{8E_CE_J}(\hat{a}^\dagger\hat{a} + \frac{1}{2}) - E_J - \frac{E_C}{12}(\hat{a} + \hat{a}^\dagger)^4 + \ldots \tag{2.22}$$

here the commutation relation $[\hat{a}\hat{a}^\dagger - \hat{a}^\dagger\hat{a} = 1]$ is used for the transmon operators.

This equation can be further simplified by neglecting the constant contributions to the Hamiltonian and by rewriting the term $(\hat{a}+\hat{a}^{\dagger})^4$ and by dropping the fast rotating terms. This will result in equation:

$$H \approx \sqrt{8E_C E_J}\hat{a}^{\dagger}\hat{a} - \frac{E_C}{2}\hat{a}^{\dagger}\hat{a} - \frac{E_C}{2}(\hat{a}^{\dagger}\hat{a})^2 \tag{2.23}$$

In this equation $\hat{a}^{\dagger}\hat{a}$ is the counting operation of the energy level. Thus using this approximated form of the Hamiltonian, the qubit frequency and the difference between the qubit frequency levels can be determined. The qubit frequency of energy level i can be written as

$$\omega h = \left(\sqrt{8E_C E_J} - \frac{E_C}{2}\right)i - \frac{E_C}{2}i^2 \tag{2.24}$$

where ω is the qubit frequency, $h = 6.626 \times 10^{-34}$ Js, is the Planck constant. The difference between two energy levels can be written as:

$$\Delta\omega h = \sqrt{8E_C E_J} - E_C(j+1) \tag{2.25}$$

where j is energy level. From equation (2.25) we see that the spacing between the energy levels for higher levels becomes smaller. Which can also be seen in the figure for the anharmonic quantum oscillator.

2.4.4. Starmon

The DiCarlo lab uses a transmon qubit in the shape of a star, named the starmon. The layout of the starmon can be seen in figure 2.7, it has seven-port connectivity of which four are coupling busses to the nearest-neighbor qubits, one is a readout resonator, one is a microwave driveline for qubit control and finally a flux-bias line for frequency tuning. The connectivity is achieved by using co-planar waveguides, which consists of a conductor used to transport the signal surrounded by a grounded plane, separated by a gap. At the DiCarlo lab the conductor and grounded plane are fabricated from NbTiN. The co-planar waveguides and the starmon are surrounded by a holey ground. The holey ground is added to reduce the dissipation due to magnetic vortices [49]. The qubit frequency of the starmon can be changed by altering E_J by means of the overlap area of the Josephson junction or by changing E_C by means of changing the size of the capacitor used in the starmon design.

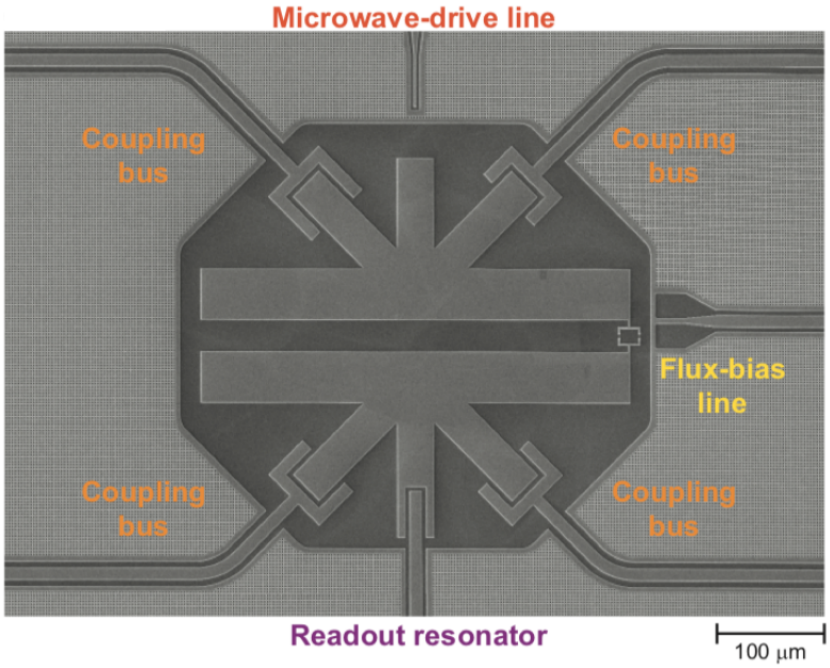


Figure 2.7: SEM image of the starmon design. Figure taken from [50].

2.5. Surface Code

Qubits are susceptible to losses and therefore the performance of a single qubit will decrease over time. In order to increase the performance the logical qubit is introduced, a logical qubit is a qubit that is created by entangling multiple physical qubits. In this logical qubit there are ancilla and data qubits present, by using indirect measurements on the ancilla qubit it is possible to perform error corrections, which allows for a logical qubit that performs better than a single physical qubit. To create a logical qubit, a surface code is required, which is an error correcting code defined in a 2D lattice of qubits. If there are enough physical qubits in the 2D lattice it is possible to create multiple logical qubits with the surface code. These logical qubits can then be used to perform operations with less errors than the physical qubits.

The DiCarlo lab uses a scalable surface code, consisting of a 8 qubit unit cell, incorporating data and ancilla qubits operating in 3 frequency groups to enable easier fabrication and measurement. The current state-of-the-art in superconducting quantum processor complexity is Surface-17, comprising 6 low frequency data qubits operating at a frequency of 4.9 GHz, 8 middle frequency ancilla qubits operating at a frequency of 6.0 GHz and 3 high frequency data qubits operating at a frequency of 6.7 GHz. The data qubits are used to perform calculations, while the ancilla qubits are used for error detection. The 8 ancilla qubits are divided into 4 Z-parity check qubits and 4 X-parity check qubits. Here the Z-parity check is used to detect phase flip errors, while the X-parity check is used to detect bit flip errors. Using multiple frequency groups it is possible to read out multiple qubits at the same time using frequency multiplexing [51]. An overview of the Surface-17 layout can be seen in figure 2.8 within the area denoted by the black line. The area outside of the black line represents how the surface code fabric can be extended to include more qubits to eventually scale up to a surface code that uses 49 qubits, also known as Surface-49. As the number of physical qubits increases on a superconducting quantum processor is becomes more difficult to connect all the required cables to the processor. To solve the problem through silicon vias (TSV) are introduced, which can be used as interconnects to create 3D circuits. At the same time these vias create isolation between components on the chip and suppress substrate modes which could affect the performance of the superconducting quantum processor [52, 53].

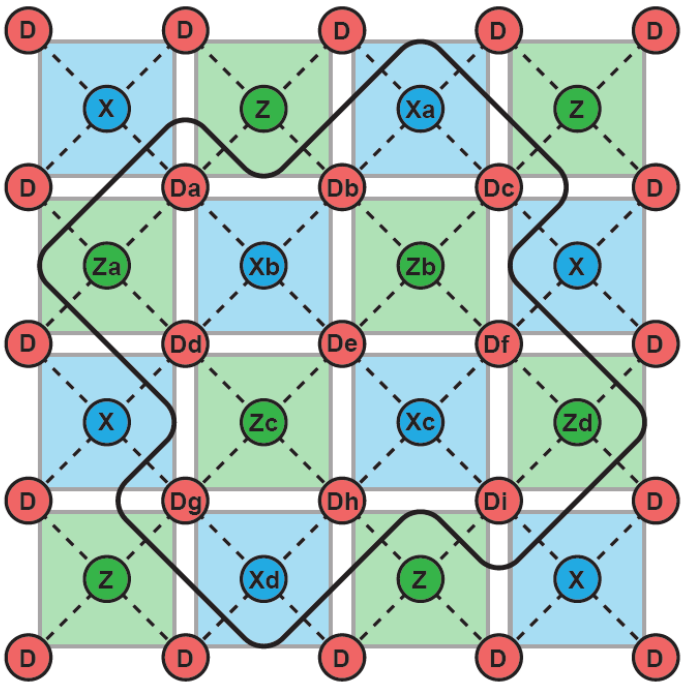


Figure 2.8: Layout of the surface-code fabric. The black line encloses the Surface-17 layout, which consists of 8 data qubits and 9 ancilla qubits. The red circles represent the data qubits and the blue (green) circles represent the ancilla qubits used for performing X-type (Z-type) parity checks on the nearest-neighbor data qubits. Figure taken from [50].

2.5.1. Importance Of Frequency Targeting

Frequency targeting refers to the process of reducing mismatch between the designed and the measured qubit frequency during fabrication. If there is a good frequency targeting the designed and actual qubit frequency should be the same, which allows for the optimal operation of the processor. The frequencies of the qubits are designed such that crosstalk is mitigated as much as possible. Crosstalk is identified as a dominant source of gate errors [54, 55] and can be described as unwanted interaction between coupled qubits on a processor. For superconducting qubits this crosstalk occurs via resonance of qubit frequency between two qubits. There are currently two methods used to avoid accidental resonance of qubits. The first method is to tune the qubit frequency using tunable qubit and the second is to temporarily disable connections between qubits using tunable couplers [56]. Both of these methods can be applied at the same time in order to reduce crosstalk even further.

Using tunable qubits and tunable couplers allows for more suppression of crosstalk and thus for the optimal performance of a processor. The problem with using both tunable qubits and tunable couplers is that such an architecture generally has a shorter coherence time than simpler systems and that it is susceptible to noise. This is why IBM Q works with fixed frequency qubits and fixed couplers, which allow for long coherence times and noise immunity. They report a two-qubit gate error approaching 0.01 using this architecture. The downside of this architecture is that crosstalk cannot be mitigated and therefore the frequency targeting becomes more important. This is why IBM invests in the tuning of qubit frequencies using laser-annealing [57–59]

Our group uses an architecture with tunable qubits and fixed couplers, in this case the performance of a single qubit is affected by its sweetspot frequency. If the qubit operates at the sweetspot there will be minimal dephasing from $1/f$ noise, which decreases the qubit dephasing and relaxation [60]. The frequency difference between the operating frequency and the park frequency depends on the residual interaction during single-qubit gates. The smaller the frequency difference, the larger the single-qubit gate error will be. Versluis et al. [50] discussed that a 400 MHz difference between the sweetspot frequency and the park frequency results in a 0.01 single-qubit error rate, while a difference of 1.2 GHz results in a 0.001 error rate. [50].

Lastly, the architecture using both tunable qubits and tunable couplers is investigated by Google [13]. This architecture is susceptible to $1/f$ noise if the qubit is not operating at the sweetspot, however this architecture allows for the highest reduction in errors introduced by crosstalk by flux tuning the qubit frequencies and disabling the connection between two qubits. This allows for an average gate error of 0.067% for single qubit gates and 0.08% for two-qubit gates. Using this architecture Google claimed quantum supremacy in 2020 [13].

2.5.2. Frequency Targeting Estimation

The qubit frequency can be estimated from room temperature resistance measurements. As discusses earlier the energy levels of a transmon qubit can be calculated using equation (2.24). Using $i = 1$, the ground state of the transmon can be calculated

$$\omega h = \sqrt{8E_C E_J} - E_C \tag{2.26}$$

Recall that the Josephson energy is defined as $E_J = \frac{\Phi_0 I_C}{2\pi}$, where I_C is the critical current. As discussed earlier the critical current can be estimated from room temperature resistance measurements using the Ambegaokar-Baratoff relation [3], which is given by

$$I_C = \frac{\Delta_1(T)}{R_N} K\left(\left(1 - \frac{\Delta_1^2(T)}{\Delta_1^2(T)}\right)^{1/2}\right) \tag{2.27}$$

which can be simplified to $I_c = \frac{\pi\Delta(T)}{2R_N}$ since the same materials are used for both junction electrodes. In the case of the SQUID this relation still holds. This expression can be related to the Josephson energy to make the relation between the room temperature resistance measurements and the frequency of the qubit apparent. This relation is

$$E_J = \frac{\Phi I_C}{2\pi} = \frac{\Phi\Delta(T)}{4R_N} = \frac{M_\#}{R_N} = M_\# G_N \tag{2.28}$$

where $M_\#$ is known the magic number and G_N is the conductance obtained from room temperature measurements. In the DiCarlo lab the magic number is typically 120-145 GHzkΩ, the variation in the magic number is caused by variations in the fabrication process. The magic number depends on the critical current and is thus material dependent, by using different materials for the Josephson junctions the qubit frequency can be

changed. Resistance and conductance are related according to $R = 1/G$, therefore the Josephson energy can also be expressed as the product of the magic number and the conductance. In figure 2.9 the relation between the transmon qubit frequency and the conductance of the Josephson junction is represented. In this plot the $E_c = 0.3\,\text{GHz}$ and the $M_\# = 130\,\text{GHz}\,\text{k}\Omega$.

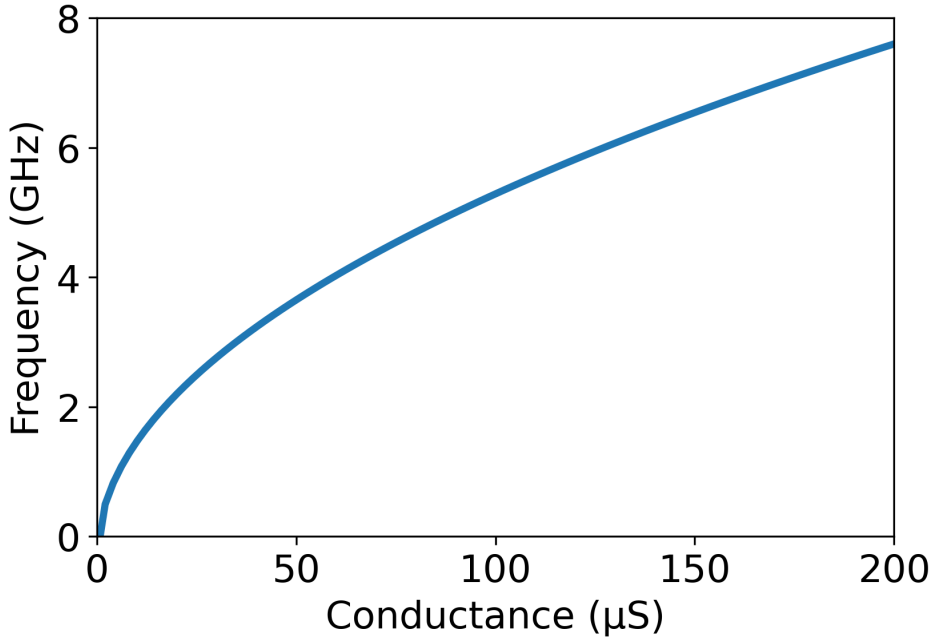


Figure 2.9: The transmon qubit frequency as a function of the Josephson junction conductance. These two parameters are related to each other by the Ambegaokar-Baratoff relation. For this figure the following values are used for the $E_c = 0.3\,\text{GHz}$ and $M_\# = 130\,\text{GHz}\,\text{k}\Omega$.

2.5.3. Room Temperature Resistance Measurements

The normal junction resistance is measured at room temperature via two-probe resistance measurements. A direct current is applied on the Josephson junction using two tungsten probe needles, the voltage drop across the junction is measured to determine the junction resistance. Since the Josephson junction is a nano-structure the current of a normal multi-meter would be too large and short the junction. Therefore, a custom-built junction measurement box is used to get a lower current that is suitable for the junction. The electrical circuit of the junction measurement box can be seen in figure 2.10. In the schematic the resistance R can be varied between 1 kΩ, 100 kΩ and 10 MΩ. Changing the resistance R changes the current send through the junction. The tungsten needles are attached to micro manipulators for accurate control. The sample position can be fixed using a weak vacuum.

Currently the DiCarlo lab is working on an automatic probe-station that is able to use four-probe measurements, instead of two-probe measurements. These measurements are more accurate since the voltage drop through the measurement cables and the series resistance contribution from the NbTiN SQUID stem are not excluded in two-probe measurements. Some datasets in this work are obtained by using the automatic probe-station, however with two-probe measurements, since the four-probe measurements are yet to be implemented.

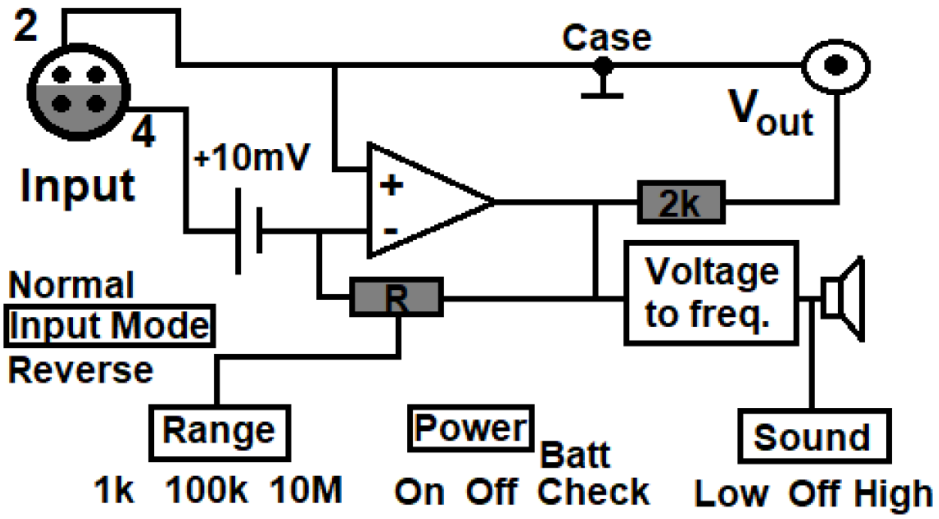


Figure 2.10: Electrical circuit of the junction measurement box.

2.6. Nanofabrication Processes

In this section some of the processes used during the fabrication of superconducting quantum processors are highlighted. Specifically, this section focuses on reactive ion etching and double angle evaporation.

2.6.1. Magnetron Sputter Deposition

Sputter deposition is a form of physical vapor deposition (PVD), which is used to deposition a thin film on a substrate. In this process argon ions from a glow discharge plasma are attracted to the negatively biased target and collide with it. During this collision atoms from the target material are dislocated and are transported to the substrate on which they are deposited under ultra high vacuum conditions. By using a metal target such as Nb it is possible to deposit a thin Nb film on a substrate. If during the process N is added to the process chamber it is possible to create a film of NbN.

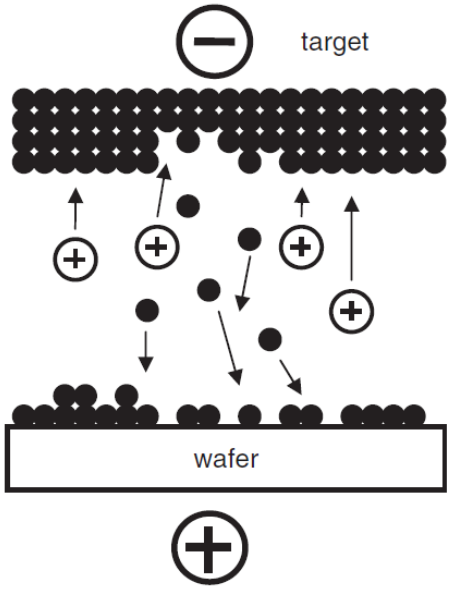


Figure 2.11: Schematic representation of a sputtering process. The Ar ions are attracted to the target material and will dislocate atoms from it. These atoms fly through the chamber, before being deposited on the wafer.

2.6.2. Electron beam Lithography

Electron beam lithography (EBL) is a technique that uses electrons to pattern structures on a substrate. In EBL a resist layer that is sensitive to the electron beam is spun on a substrate. A typical resist used is polymethyl methacrylate (PMMA), which consist of long carbon chains. The substrate is loaded into an electron beam pattern generator (EBPG), which is used for the EBL. In the EBPG the resist is exposed to the electron beam, which breaks the carbon chains into smaller chains. After the exposure the exposed parts of the resist can be removed by immersing the substrate in a solvent. The exposed parts dissolve in the solvent, whereas the non-exposed parts are not affected. EBL has a few advantages over commonly used optical lithography. EBL is able to directly write a pattern on the resist layer without the need of a mask, which is typically used for optical lithography. Furthermore, the electrons used have a smaller wavelength than photons used for optical lithography. This smaller wavelength allows for a higher resolution, which is critical for the fabrication of nano-scopic features.

2.6.3. Reactive Ion Etching

Reachtive ion etching (RIE) is an anisotopic form of dry etching that uses a plasma to create vertical walls in a material. There are two forms of plasma reactors typically used, the capacitively coupled plasma (CCP) reactor and the inductively coupled plasma (ICP) reactor. In this work only CCP is used and therefore ICP is not discussed. In a CCP reactor gas is injected between two parallel plates, a top and bottom electrode. Gases typically used in these systems are fluorine (CF_4, SF_6, CHF_3, NF_3, C_2F_6, C_4F_8, XeF_2), chlorine (Cl_2, BCl_3, $SiCl_4$, $CHCl_3$) and bromine (HBr) based. After the gas is injected into the chamber and a steady pressure is reached a radio frequency voltage is applied between the electrodes in order to ionize the gas and obtain a plasma. The ions in the plasma are attracted to the negative potential of the electrode, which can be used to etch a substrate by positioning it on the bottom electrode. Figure 2.12 shows a schematic representation of a RIE chamber.

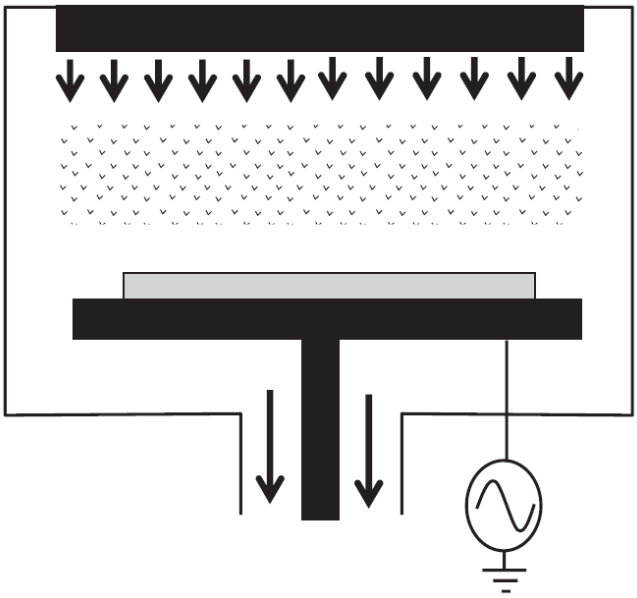


Figure 2.12: Schematic representation of the chamber of a RIE system. The gas is injected at the top of the chamber. The RF voltage ignites a plasma which splits the gas into ions and excited neutrals. The ions are accelerated towards the bottom electrode and etch the substrate by physically bombarding it, while the excited neutrals chemically react with the substrate to form a volatile product that is removed from the substrate.

In the case of RIE not only the ions but also the excited neutrals play a role in the etching process. An example of this is the etching of Si with CF_4. When the plasma is ignited CF_4 will split up into $CF_4 \longleftrightarrow CF_3 + F$, in this reaction fluor is released. This fluor can react with the silicon according to $Si + 4F \longrightarrow SiF_4$, here the SiF_4 is volatile at room temperature and will therefore be removed from the sample. This process in combination with the bombardment of the ions results in an anistropic etch profile [61, 62].

2.6.4. Double Angle Evaporation

Josephson junctions are typically fabricated using a double angle evaporator. Such a system is capable of depositing material from different tilt angles and rotation angles without breaking vacuum, which is important for the fabrication of junctions. The most common material for the fabrication of Josephson junction is aluminum. Aluminum oxidises when it comes in contact with O_2 to form a layer of 1-3 nm AlO_x, this layer can be used as the insulating layer in a SIS junction. Note that the oxidized aluminum is written as AlO_x, this indicates that there are defects during the formation of the tunnel barrier. In the ideal case the aluminum and oxygen would form Al_2O_3. Using this oxidizing property it is possible to deposit aluminum and oxidize it in a consecutive step. After the oxidation a second layer of aluminum can be deposited to form the SIS junction. There are two types of oxidation processes typically used, static and dynamic oxidation. In static oxidation the chamber is filled with oxygen until a certain pressure is reached and after a certain waiting time the oxygen is removed from the processing chamber. In dynamic oxidation there is a continuous flow of oxygen. The oxygen is added to the chamber until a certain pressure is reached, where after the oxygen is pumped away at the same rate that fresh oxygen is added to the system. This will result in a flow of oxygen entering and leaving the system. During the deposition of the Al for the Josephson junctions it is important to choose an appropriate tilt and rotation for each deposition step in order to prevent the fabrication of a shorted or open circuit.

There are two type of evaporator sources, a thermal source and an electron beam source. In a thermal source the material is put in a crucible which is wrapped in a resistive wire. By applying a current to the wire the the crucible and material heat up. If the material becomes warm enough it will start to evaporate from the crucible towards the substrate. The problem with this method is that it is possible that the crucible will also start to evaporate resulting in contaminations. Using a thermal source low deposition rate are possible, which range between $1-20$Å/s.

The electron beam source consists of a cathode filaments that releases electrons. This electron bundle is first focused with an aperture and then deflected onto the material using a magnetic field. The material is positioned in a crucible, which is cooled from the outside. Using the electron beam it is possible to warm up a small spot on the material within the crucible, therefore the spot scans across the material to obtain a more uniform evaporation. Once the material is warmed up by the electron beam it will start to evaporate from the crucible and it will eventually be deposited on the substrate. The advantage of electron beam evaporation is that it is possible to evaporate more material than the thermal source and has less impurities. The deposition rate of the electron beam is typically between $10-100$Å/s, which is higher than the thermal source. The downside of the electron beam evaporator is that it is more expensive than an evaporate with a thermal source.

An evaporator typically first deposits a thin layer of titanium (Ti) prior to the Al deposition. The Ti is used as a getter material, a getter is a reactive material that is introduced to the vacuum to remove unwanted contaminations. The contaminations chemically react with the Ti or are adsorbed by it and are thus removed from the environment. Both of these evaporation machines typically use a piezoelectric material (often quartz) to monitor the rate and the amount of material deposited. This piezoelectric material oscillates when it is electrically driven, when material is deposited on the piezoelectric material is will induce a frequency shift, which can be used to determine the rate at which the material is being deposited [63].

2.7. Fabrication

In this section the fabrication process used to fabricated Josephson junctions on a superconducting base layer is described. The fabrication is separated into a few subsections to indicate the different phases of the process. First the choice of the superconducting material is discussed, followed by how this base layer is patterned. The electron beam lithography used is briefly discussed followed by the reactive ion etching used for etching of the was layer and ashing of the resist stack. Finally the fabrication of Josephson junctions is discussed using a double angle evaporator. An overview of the used fabrication recipe, with the relevant parameters, can be found in appendix B.

2.7.1. Wafer Metallization

For the fabrication of superconducting quantum processors the lab uses high resistivity (ρ = 150 kΩcm), <100> silicon (Si) wafers with a thickness of 525 µm. The high resistivity is required, since the fabricated structures should be separated from the ground plane. The <100> orientation allows for dicing of the wafer, while reducing the risk of breaking it along the crystal orientation. Silicon is used since it has a low dielectric loss, furthermore transmon qubits on silicon have coherence times and gate fidelity's similar or exceeding their sapphire counterparts [64].

2.7.2. Base Patterning

For the patterning of the superconducting base layer there are two options: additive and subtractive patterning. In additive patterning the material is deposited on the substrate such that it has the correct form. This can be done by using a resist and exposing the pattern corresponding to the base layer. After developing, the material can be deposited in the openings, while the rest of the materials is deposited on the resist. The material on the resist can then be removed using lift-off to obtain the desired pattern. In subtractive patterning the material is deposited all over the film. By spinning a resist on top of the materials and exposing it, the desired pattern can be obtained. Using etching chemistry it is possible to remove parts of the deposited material and obtain the desired form of the base layer. While both of these patterning methods will result in a base layer with the same pattern, there are differences between them. When using additive patterning there is less control over the interface between the substrate and the metal, however it does allow for a smooth substrate. When using subtractive patterning there is control over the substrate metal interface, since it is possible to use surface treatments prior to deposition [65]. The downside of subtractive patterning is that the etching chemistry used can also affect the substrate, resulting in an increase in roughness. Since the substrate metal interface is identified as an important parameter that affects the dielectric losses [66–69] subtractive patterning is used for the fabrication of the base layer. The downside of this method is that the Si becomes rough during the etching process of NbTiN, which affects the performance of Josephson junctions. The method to circumvent this problem will be discusses later on.

2.7.3. Base Layer Deposition

For the superconducting film NbTiN is chosen because of its high quality vacuum-metal interface and high T_c. In order to create a high quality substrate-metal interface the substrate is cleaned before the deposition of the NbTiN. First organic contaminants are removed by subjecting the substrate to a 5 min ultra-violet (UV) treatment, as it has been shown that UV is capable of depolymerizing organics [70]. Then a clean with acetone and isopropyl alcohol (IPA) is used to further clean the sample. The inorganic contaminants and the SiO_x that forms on top of the Si are removed using a buffered oxide etch (BOE) mixed 1:1 with H_2O. BOE is a mixture of ammonium fluoride (NH_4F) and hydrofluoric acid (HF). HF removes SiO_x according to the reaction $SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O$ forming fluorosilicic acid H_2SiF_6 and H_2O. Here the H_2SiF_6 is soluble in wafer and is thus removed from the substrate. The problem with this reaction is that is removes the HF, which is necessary for the removal of SiO_x. Therefore the NH_4F is added which replenishes the HF concentration according to $NH_4F \longleftrightarrow NH_3 + HF$, which results in an even concentration throughout the process and thus allows for a constant etch rate.

Besides the substrate cleaning used in our lab there are other methods to clean the substrate, of which the most well known is the Radio Corporation of America Standard Clean, or just RCA clean. The RCA clean consists of three steps, an organic clean, an oxide strip and an ionic clean. The organic clean consist of a 1:1:5 mixture of 28% ammonium hydroxide (NH_4OH: 40% hydrogen peroxide (H_2O_2):H_2O. This mixture is heated up to 75 °C in order to increase the reactivity of the solution. The organic clean removes organics and metals,

but does not affect the SiO_x. The SiO_x layer can be removed using HF. The procedure for the oxide strip in the RCA process is the same as the procedure the lab currently uses to remove the oxide layer. Finally an ionic clean is applied, which is used to regrow the SiO_x layer. This clean is a mixture of 1:1:6 hydrochloric acid (HCl):H_2O_2:H_2O, which is heated to 75 °C to increase the reactivity. This clean removes the traces of metallic contaminants and will also form a new layer of SiO_x. It is important to note that the RCA process requires high-purity chemicals and clean glassware in order to clean the the Si surface and regrow the SiO_x layer. If low quality chemicals or dirty glassware is used it can contaminate the Si surface and the regrown SiO_x barrier [71, 72]. Another well known organic clean is Piranha, which is a mixture of sulfuric acid (H_2SO_4) and H_2O_2 where the ratio's between the two constituents usually vary. The Piranha clean can be used to remove large organic contaminants prior to a RCA clean.

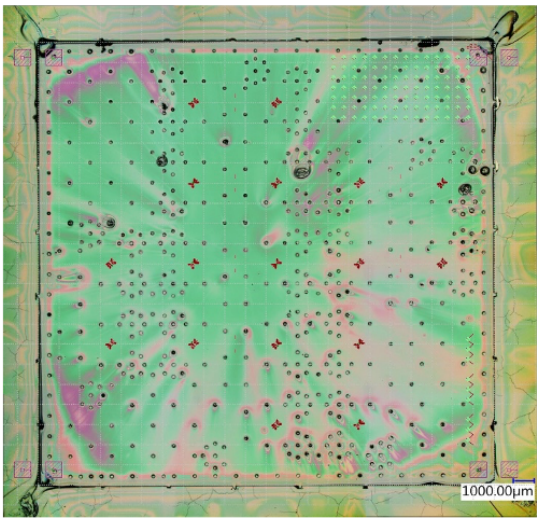
After cleaning the substrate is subjected to a hexamethyldisilazane (HMDS) vapor treatment in a nitrogen atmosphere in order retard the formation of SiO_x [65]. This procedure has been shown to yield an increase in the intrinsic quality factor [73]. After this treatment the superconducting base material can be deposited. The NbTiN is deposited using reactive magnetron sputtering, in this process a NbTi target with concentration 59:39 Nb:Ti is etched using Ar^+ ions. The etched Nb and Ti particles are released into the chamber and end up on the substrate. By filling the process chamber with nitrogen it is possible to obtain a NbTiN film. During this process it is possible for Ar and N atoms to get trapped in the film. The contribution of Ar in the film can be neglected, as it is a non-reactive noble gas. The deposited NbTiN has a lattice constant of 4.39 Å, which is relatively close to the lattice constant of 5.43 Å from the Si substrate, allowing for a smooth interface. After the deposition the sheet resistance of the film is measured using a four point probe measurement. Using this process a NbTiN film of 200 nm is deposited with a critical temperature T_c of 13-14 K, a resistivity of 85-105 μΩcm and a sheet resistance of 0.9-1 Ω/sq is obtained. The advantage of sputtered NbTiN is that it has a fast deposition cycle and produces high quality films with $< 10^2$ particles/wafer. The downside of the sputtering process is that it process a non-uniform film, with 10% thickness variations across a 100 mm wafer. Besides sputtering it is also possible to use Atomic Layer Deposition (ALD) to grow a NbTiN film on the substrate. ALD is capable of producing highly uniform films, with thickness variations of 2% across a 200 mm wafer. The downside of ALD films is that there is a longer deposition cycle and the contaminations introduced in the film. The contaminations are introduced, since the NbTiN recipe is not optimized which results in $> 10^3$ particles/wafer. Due to this large number of contaminations the ALD process is not used in this work.

2.7.4. TSV

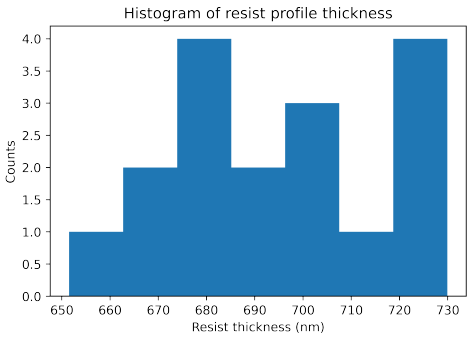
Trough Silicon Vias (TSV) are holes in the silicon substrate fabricated using a highly anisotropic deep reactive ion etching process (DRIE). These holes can be used as interconnects to create 3D circuit, to engineer isolation between components on the chip and to suppress substrate modes which could affect the performance of the superconducting quantum processor [52, 53]. In this work substrates with TSV are referred to as non-planar bases, whereas substrates without TSV are referred to as planar bases. This distinction is important as the TSV will affect the performance of resist spinning in later fabrication steps. To create the TSV a protective layer of SiO_2 with a thickness of 600 nm is deposited on top of the NbTiN base, whose role will become apparent later on. The substrate gets a HMDS treatment to improve the adhesion of the MX5050 negative dry resist which is rolled on both the front and back side. The resist is also applied on the back side of the wafer in order to prevent damage at the back side of the wafer during the DRIE of the TSV. The resist has a thickness of 50 μm and is exposed using a 350 W Hg lamp, with a wavelength of 320-365 nm at a dose of 13 mW/cm^2 for 12 s. The front size is exposed using a mask, whereas the back side is flooded. Since the TSV are microscopic features it is possible to use optical lithography instead of electron beam lithography. After development the TSV are etched using a highly anisotropic Bosch process, with SF_6 as etchant and C_4F_8 as passivation layer. After the DRIE the resist is removed from the substrate. Figure 2.13 shows an optical image of a sample with TSV on it. On this particular sample the resist layer for the base patterning is spun. From the color alterations it can be seen that there are height variations in the resist across the sample, which result from the TSV. After the fabrication of the TSV a 90 nm layer of TiN is deposited using ALD in order to connect cables through the TSV.

2.7.5. Base Layer Patterning

As discussed earlier subtractive patterning is used for the fabrication of the superconducting base layer. The problem with this process is that after the NbTiN base is etched the Si substrate will be etched, which will



(a) Optical image of a sample after the fabrication of through silicon vias. On this sample the electron beam resist for the base patterning step is spun. The color alterations make it clear that there are variations in the height of the resist across the sample. These variations are caused by the TSV.



(b) Histogram of the variations in the resist height of a Surface-17 device.

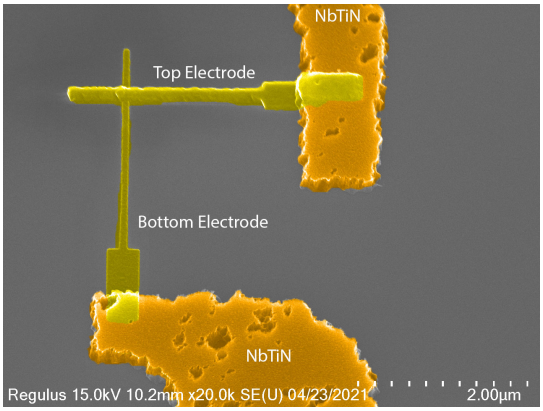
Figure 2.13: Optical image of a 13 × 13 mm chips with through silicon vias on in. The image shows color alterations, which correspond to height variations in the resist as seen in figure 2.13b. This figure shows the resist height off 17 points corresponding to the positions of the qubits on a Surface-17 device.

increase the Si roughness. Since the Josephson junctions are fabricated on the Si the Si should be as smooth as possible, as the roughness of the Al electrodes is affected by the roughness of the substrate on which it is deposited [33]. The Al electrons should ideally be smooth, because a rough electrode will create a rough AlO_x layer. In the case of a rough tunnel barrier it is possible that most of the tunneling will happen in a small area where the tunnel barrier is the thinnest, instead of uniform tunneling across the barrier. In order to create a smooth Si surface after the etching of the NbTiN base a combination of dry etching and wet etching is employed. The dry etching is performed using sulfur hexafluoride (SF_6), whereas the wet etch uses a slightly modified RCA-1.

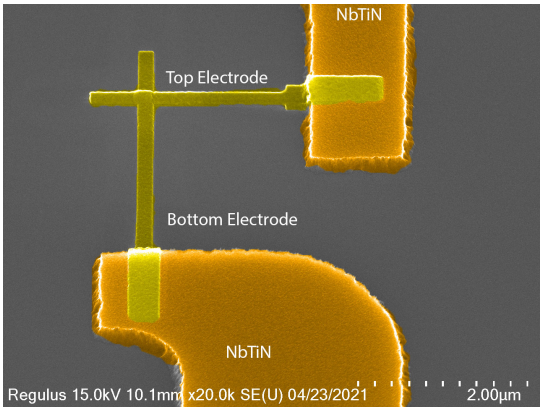
Before the base patterning an inorganic sacrificial layer of Si_3N_4 is deposited on top of the NbTiN using Physical Vapor Deposition (PVD), the layer will protect the top of the NbTiN layer during the wet etch process. First the positive electron beam lithography resist ARP.6200-18, also known as CSAR-18, is spun on top of the sacrificial layer at 1500 rpm and baked for 3 min at 150 °C to obtain a thickness of 1.3 µm. The CSAR is exposed using EBL, this is preferred over optical lithography, since it is capable of writing the desired pattern into the resist, whereas optical lithography requires a mask for exposure. The layout is continuously altered, which would require a new mask for each new alteration. Another option would be to use a direct laser writer for the base layer, however this option is not investigated.

The CSAR is exposed with a 100 kV beam with a spotsize of 63 nm and a stepsize of 0.04 µm at at dose of 360 $\mu C/cm^2$. The resist stack is developed by immersing the sample in pentyl acetate for 1 min followed by a dip in IPA to stop the development. Post development the Si_3N_4 mask and the NbTiN are dry etched using Reactive Ion Etching (RIE) with SF_6. RIE is used since it is an anisotropic process, which allows for uniform etching across the sample. The NbTiN is etched until there is only a thin layer left on top of the Si. The dry etch increases the roughness of the Si if etched completely through the NbTiN, therefore the final layer of NbTiN is etched using a mixture of 1:1:5 hydrogen peroxide:ammonia:H_2O, also known as RCA-1. This mixture etches the NbTiN while leaving the Si intact, thus allowing for smooth surfaces. The mixture is heated up till 33 °C to increase the etch rate of the NbTiN, the mixture can be heated even further for higher etch rates, however this also creates a process that is more difficult to control. The problem with wet etching is that it is isotropic, thus the NbTiN will be etched from all sides, resulting in increases roughness on the top of the NbTiN. This is where the inorganic mask becomes important, this mask protects the top of the NbTiN during wet etch, thus only the openings created during the dry etch and the sidewalls are affect during the wet etch. To determine

if the wet etch has removed the NbTiN on top of the Si the conductance can be measured on the etched areas using two-probe conductance measurements. If a measurements results in a short circuit this indicates that there is still NbTiN present to conduct the current. If the circuit is open the NbTiN is removed and the wet etch does not have to be repeated. If the wet etch is used too long this will cause holes in the sidewalls of the NbTiN, which look like mouse bites, or it will affect to top of the NbTiN as well, resulting in holes in the base, as seen in figure 2.14. It is important to note that between the dry etch and the wet etch the electron beam resist is stripped from the sample using NMP, to prevent the resist from ending up in the RCA-1 mixture. After the wet etch the Si_3N_4 mask is removed using a 1:1 mixture of hydrofluoric acid (HF) and H_2O. The process of patterning NbTiN starting from the bare Si wafer is represented in figure 2.15.

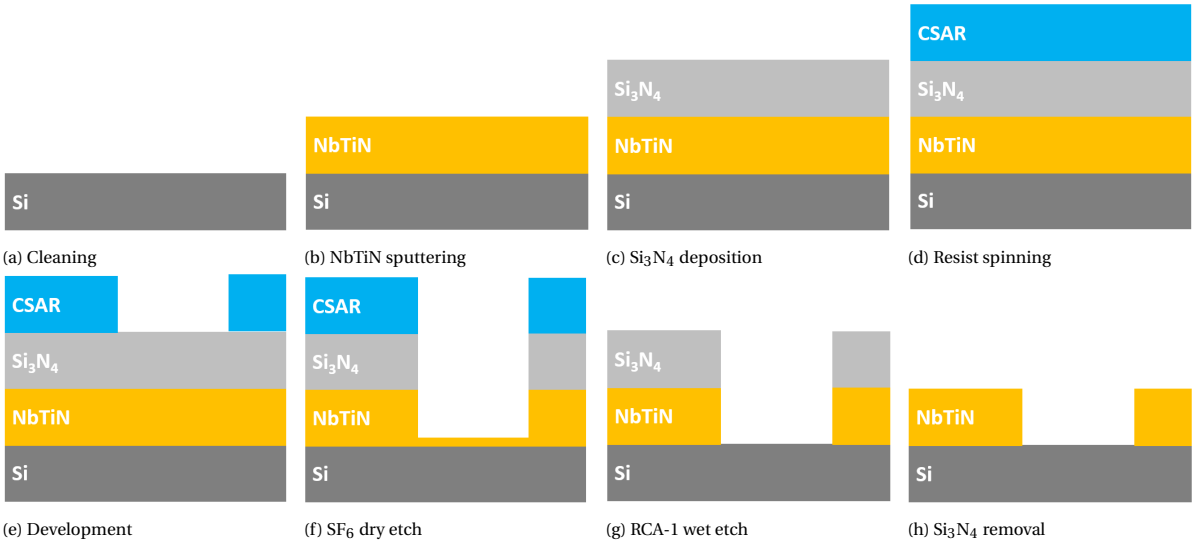


(a) SEM image of over etched NbTiN. The sidewalls are rough and there are holes in the NbTiN indicating that the Si_3N_4 was removed and thus did not protect the NbTiN.



(b) False colored SEM image of properly etched NbTiN. Here the sidewalls seem smooth and there are no holes on the top indicating that the Si_3N_4 protected the NbTiN.

Figure 2.14: False colored SEM images of an over etched and 2.14a and a properly etched 2.14b etched NbTiN base. These SEM images are taken after the deposition of the Josephson junctions.



(a) Cleaning (b) NbTiN sputtering (c) Si_3N_4 deposition (d) Resist spinning

(e) Development (f) SF_6 dry etch (g) RCA-1 wet etch (h) Si_3N_4 removal

Figure 2.15: Graphical representation of the fabrication procedure to obtain NbTiN with the desired patterns on the wafer. First the wafer is cleaned with BOE to remove SiO_x present on the wafer 2.15a, followed by the sputtering of NbTiN 2.15b and PECVD of Si_3N_4 2.15c. The electron beam resist ARP.6200-18 (CSAR) is spun on top 2.15d and exposed using a EBPG. The resist is developed using pentyl acetate 2.15e. The Si_3N_4 and NbTiN are etched using RIE with SF_6 while keeping a thin layer of NbTiN on the substrate 2.15e. The CSAR is removed using NMP followed by a wet etch using the constituents of RCA-1 at 33 °C to remove the thin layer of NbTiN 2.15g. Finally the Si_3N_4 is removed using HF 2.15h.

2.7.6. Josephson Junction Fabrication

After the patterning of the base layer the Josephson junctions can be fabricated. As discussed earlier Josephson junctions consist of two superconducting materials separated by a thin insulating layer, such that the electrons can tunnel through the barrier. In this work two methods to fabricated Josephson junctions are used, the first method utilizes a Niemeyer-Dolan bridge [39, 40] and the second method is based on the Manhattan design [41]. Here Josephson junctions fabricated using one of these techniques will be referred to as Dolan bridge junctions and Manhattan junctions. In this section the methods used to fabricated both type of these Josephson junctions are discussed.

2.7.7. Dolan Bridge junctions

As the name implies, this Josephson junction is fabricated using a bilayer resist stack in which the top resist layer is used to fabricated a Dolan bridge [39, 40]. For the junctions PMGI SF7 is spun at 2000 rpm and baked for 5 min at 180 °C to obtain a thick layer of ≈ 400 nm. On top of this stack 950 PMMA A3 is spun at 2000 rpm to obtain a layer of ≈ 150 nm thick, this layer is also baked for 5 min at 180 °C this top layer will be used to create the Dolan bridge.

The resist is exposed using a 100 kV electron beam with a spotsize of 19 nm and a BSS of 0.01 µm to create the Josephson junction pattern. The development procedure is the same for both junction types, the PMMA is developed for 1 min using a mixture of 1:3 MIBK:IPA as this results in the highest possible resolution, the development is stopped in two steps. First the sample is immersed in a 1:3 mixture of acetone:IPA for 20 s, followed 20 s in IPA. The intermediate step of acetone:IPA is used to create a smoother transition between the developer and the stopper. Before the PMGI is developed the sample is immersed in H_2O to make it hydrophilic, since it is hydrophobic from the previous development step. The PMGI is developed using a 20 s dip in MF321, followed by immersing it back into H_2O to stop the development. After development the wafer is subjected to an O_2 plasma to ash the resist. This removes residual resist in the developed area and has been shown to improve sidewall uniformity. This O_2 plasma introduces O_2 that will react with the Si substrate, creating SiO_x. This layer of SiO_x is removed using BOE diluted 1:1 with H_2O. It is important to load the wafer into the deposition machine within 15 min of removing the SiO_x, otherwise a new layer of SiO_x will form on the substrate.

Figure 2.3 shows a schematic representation of how the resist stack and the deposition angles. The first layer of metal is deposited from direction 1 under an angle of $\theta = 75°$, followed by an oxidation step. Here the chamber is filled with O_2 until the chamber reaches a pressure of 1.3 mbar. This will create a layer of aluminum oxide (AlO_x) on top of the aluminum electrode, which will act as the insulator for our SIS junction. The second layer of metal is also deposited under an angle of $\theta = 75°$, but the sample is rotated 180° around the ϕ axis. After this deposition the aluminum is oxidized again by filling the chamber with O_2. It is important to note that the resist opening for the top electrode is smaller than the bottom electrode. This causes a relatively small overlap area between the top and bottom electrode.

2.7.8. Manhattan junctions

The Manhattan [41] Josephson junction uses a bilayer resist stack for the fabrication of the Josephson junctions. It uses a thin bottom resist layer (≈ 200 nm) of PMGI SF7 diluted 1:1 with cyclopentane, which is spun at 1500 rpm and baked for 3 min at 180 °C. This thin layer is used to promote lift off. On top of this layer a thick resist (≈ 600 nm) of 950 PMMA A6 is spun at 1500 rpm and baked for 5 min at 180 °C. The exposure and the development of the Manhattan junction resist stack is the same as the procedure for the Dolan bridge junctions. However, it should be noted that when using the diluted PMGI there is no limiting reaction when it is developed using MF321.

Figure 2.4 shows a schematic representation of the resist stack and the deposition angles. The first layer of metal is deposited from direction 1 under an 55°, this 35 nm layer forms the bottom electrode. After this the chamber is filled with O_2 until it reaches a pressure of 1.3 mbar. This pressure is maintained for 11 min to form a layer of aluminum oxide (AlO_x) on top of the bottom electrode. The top electrode is then deposited from direction 2 under the same angle. The top electrode consists of 75 nm aluminum, the top electrode must be thicker than the bottom electrode, otherwise the bottom electrode with create a shadow during the second deposition causing the aluminum to not connect, resulting in an open junction. For this method it is important that the rotation axis ϕ, the angle θ, the thickness of the top resist t, and the feature size w are

properly chosen. To be more specific for a perpendicular double angle deposition these parameters should obey the relation: $t > w/\tan\theta$. In the case that there is a misalignment α between the axis of rotation and the width of the feature, the relation becomes $t > w/(\cos\alpha\tan\theta)$ [41]. If these relations are not obeyed, spurious metal from each deposition will end up in the other junction finger, resulting in a shorted Josephson junction.

The main advantages of the Manhattan junction is that it is less sensitive to resist height variations than the Dolan junction. This allows the Manhattan junction to be used on a non-planar base, whereas the Dolan bridge junctions are not suitable in this case, since these junctions require a uniform resist to form the Dolan bridge. Through silicon vias become more important as superconducting quantum processors scale up to designs with more qubits, therefore it is necessary to start using Josephson junctions that can be fabricated on a base with TSV. After the deposition of the Josephson junction the remaining aluminum is removed using lift-off in NMP at 88 °C.

2.7.9. Airbridges

The final step in the fabrication process are the airbridges. Airbridges are microwave components that are used to equalize the electromagnetic ground plane across the superconducting quantum processor. The airbridges can also be used to cross a co-planar wave guide over another co-planar waver guide. These crossovers are necessary as the layout of superconducting quantum processors becomes more complex as the number of qubits on them increase [74].

The airbridges have a height of about 5.5 µm, therefore a thick resist stack is required. For this purpose PMGI SF15 is spun at 2500 rpm and baked for 5 min at 190 °C, this layer is spun two times to obtain the desired thickness. The resist is exposed using e-beam and developed using a mixture of AZ400:H_2O, 1:4. After development the sample is baked for 5 min 200 °C to reflow the resist. This reflow allows the square resist to obtain a circular shape. This reflow process affects the Josephson junction conductance, it has been hypothesised that this is caused by hydrates that bind to the oxides on the junction to form hydroxides [34]. After the reflow a second round of resist spinning and electron beam lithography is used to create in connects on both side of the airbridge. The airbridges are fabricated by depositing Al on top of the resist. The remaining aluminum is then removed using lift-off to obtain an airbridge. Figure 2.16 shows a SEM image of an airbridge that crosses a co-planar wave guide and connects two sides of the ground plane.

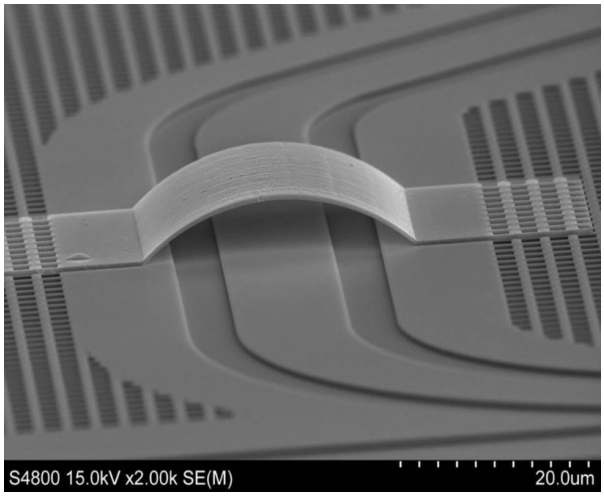


Figure 2.16: SEM image of an airbridge over a co-planer waveguide. The airbridge is used to connect the ground plane on both sides of the co-planer waveguide.

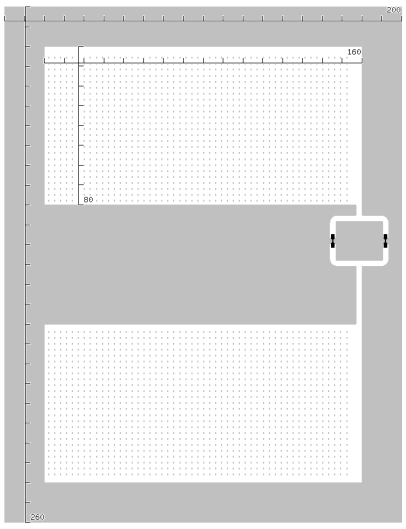
3

Junction Characterisation

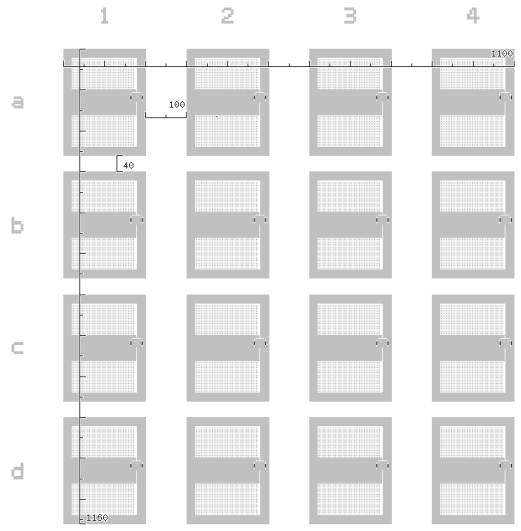
This chapter studies the uniformity of the Josephson junction conductance on a planar base of NbTiN. This is used to quantify the coefficient of variation for the current fabrication process. For the first part of this study a similar layout as the actual Surface-17 devices is used, where the qubits are replaced by junction test pads. In the second part the test pads are used in a large array across the sample.

3.1. Surface-17 Test Pads

To study the variations in the junction uniformity we use a Josephson junction test pad. Figure 3.1a shows the design of such a pad. It consists of two contact pads of 80 × 160µm, at the top and bottom, that are connected by a SQUID loop on the right. The SQUID loop itself has a gap in the middle for deposition of the Josephson junction, which completes the circuit. The contact pads have a holey ground plane which improves contact between the tungsten probes and NbTiN. The addition of holey ground in general, surrounding the device components such as qubits and tranmission lines are typically used to prevent dissipation due to vortices created by the magnetic flux [49]. These pads are positioned in a 4x4 configuration as seen in figure 3.1b, for each pad the overlap area of the junction is increased from left to right, top to bottom. This allows us to study the uniformity of the junctions across the wafer, but also the influence of the junction size on the coefficient of variation and the yield.



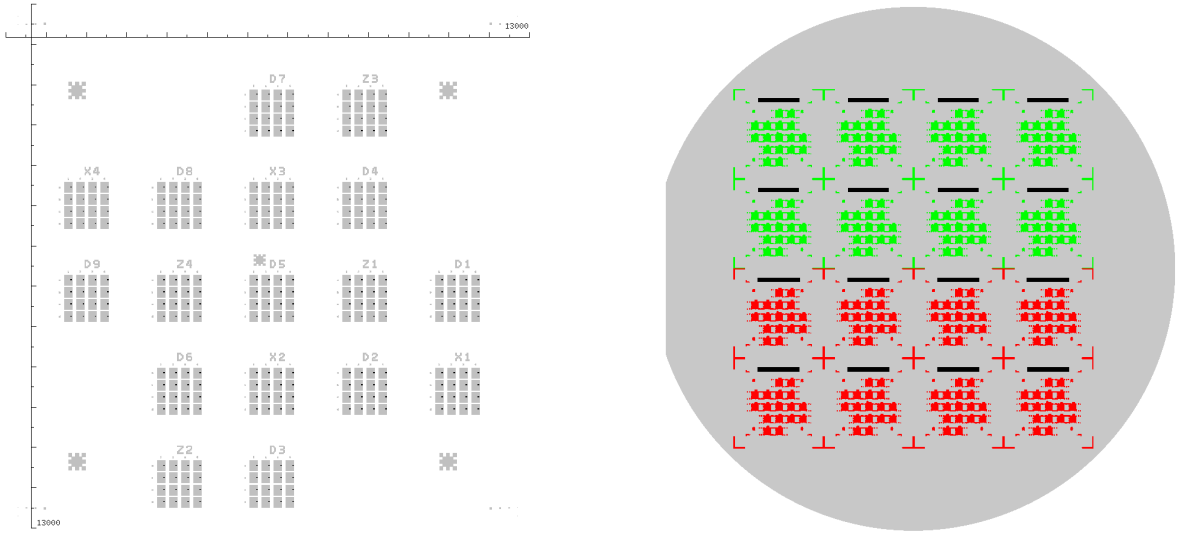
(a) Test pad design consisting of a SQUID loop in the middle and two pads used to measure the SQUID loop on the top and bottom. The total layout of the test pad is 200 × 260µm.



(b) Test array design consisting of 16 test pads. The width of the variable electrode is varied over the pads. The total layout of the test array is 1100 × 1160µm.

Figure 3.1: Schematic representation of the design used for the test pads and test array. The grey area corresponds to Si, the white area to NbTiN and the black are corresponds to the position of the Josephson junctions.

The test array is positioned in a pattern such that it resembles the layout of a Surface-17 device [75], as can be seen in figure 3.2a. The test array is of the same size as the Surface-17 device, which is 13x13 mm. In the real Surface-17 devices the qubits are divided into three frequency groups: low, mid and high. For the test design the same principle is used, thus the test arrays are also divided into three groups. The frequency of the test pads is determined by the overlap area between the top and bottom electrode, if the overlap is larger the frequency increases. For the Dolan bridge junctions the width of the top electrode is variable, while the bottom electrode is 200 nm larger than the top electrode. In this case the overlap area is determined by the width of the top electrode. For the Manhattan style junction the top electrode has a fixed width of 160 nm, while the bottom electrode has a variable width. The pads that correspond to the low frequency (data) qubits (D1, D2, D3, D7, D8, D9) have a variable electrode width that sweeps from 0.060 µm till 0.120 µm. The pads that correspond to the mid frequency (ancilla) qubits (X1, X2, X3, X4, Z1, Z2, Z3, Z4) have a variable electrode width that sweeps from 0.112 µm till 0.172 µm. The pads that correspond to the high frequency (data) qubits (D4, D5, D6) have a variable electrode width that sweeps from 0.168 µm till 0.228 µm, per step the bottom electrode width is increase by 0.004 µm.



(a) Test design. The design is chosen such that it resembles the design of a Surface-17 device. The arrays are divided intro three frequency groups. The total layout of the test design is 13000x13000µm.

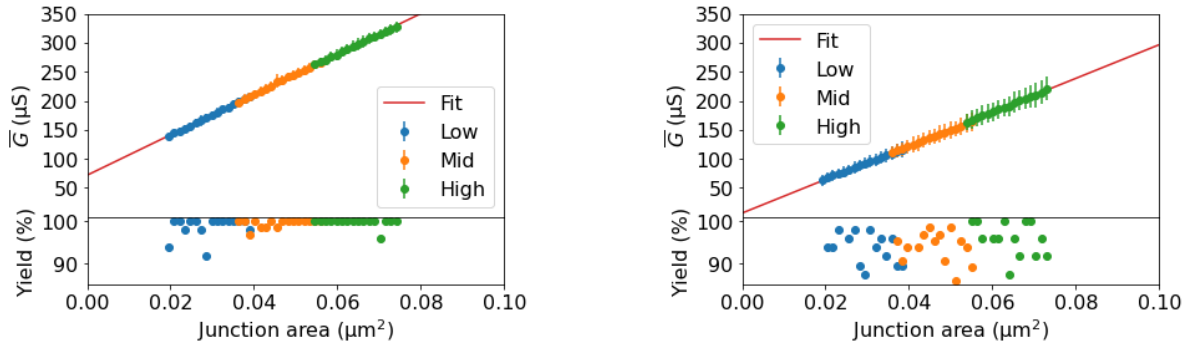
(b) Layout of the wafer used to study the variations in the conductance. The green top pads correspond to Dolan bridge junctions and the red bottom pads correspond to Manhattan junctions.

Figure 3.2: Schematic representation of the Surface-17 test design and the layout of the wafer.

On a 100 mm wafer, there is room for 16 test layouts, spanning an area of 64x64 mm. Figure 3.2b shows the layout of the wafer, it consists of 8 test designs that use Dolan bridge junctions (green) and 8 test designs that use Manhattan junctions (red). Once the junctions are fabricated and measured we can determine the Josephson junction conductance and yield as a function of the junction overlap area as seen in figure 3.3. A linear fit is applied to the conductance as a function of the overlap area, from which we find that the fit for the Dolan bridge junctions have a slope of $(3.5 \pm 0.1) \cdot 10^3$ µS/µm^2 and an offset of 71.9 ± 0.2 µS. The same is done for the Manhattan style junctions, which gives a slope of $(2.9 \pm 0.2) \cdot 10^3$ µS/µm^2 and an offset of 6.6 ± 0.4 µS. The slope for both junction types slightly different, which could indicate that there are differences in the fabrication of the tunnel barrier. The offset for the Manhattan style junctions is close to zero, which indicates that there would be no conductance when the overlap area goes to zero. This makes sense from a physics point of view, where the small offset from zero is probably caused by the contact of the Al with the NbTiN. However for the Dolan bridge junctions the offset does not go to zero when the overlap area decreases. There is currently no explanation for the behaviour of the Dolan bridge junctions.

It is important to note that the number of data points for the low, mid and high test pads are different. The junction yield can also be calculated, the yield is defined as the ratio between the number of functional Josephson junctions divided by the total number of fabricated junctions. For this wafer we find that the junction yield is higher for Dolan bridge junctions than for Manhattan junctions. The yield as a function of Josephson junction overlap area is represented in the bottom part of figure 3.3.

Smaller structures are more prone to fabrication errors, therefore it could be expected that the yield is lower for these junctions. However, the data does not show such variations. To determine the yield a filter is applied to the data to remove data points that correspond to shorted, open or half-open junctions. With a half open junction we refer to a SQUID loop in which one junction is open and one is functional, resulting in a conductance that is half of the normal SQUID loop conductance. The filtering of the data is detailed in appendix A.



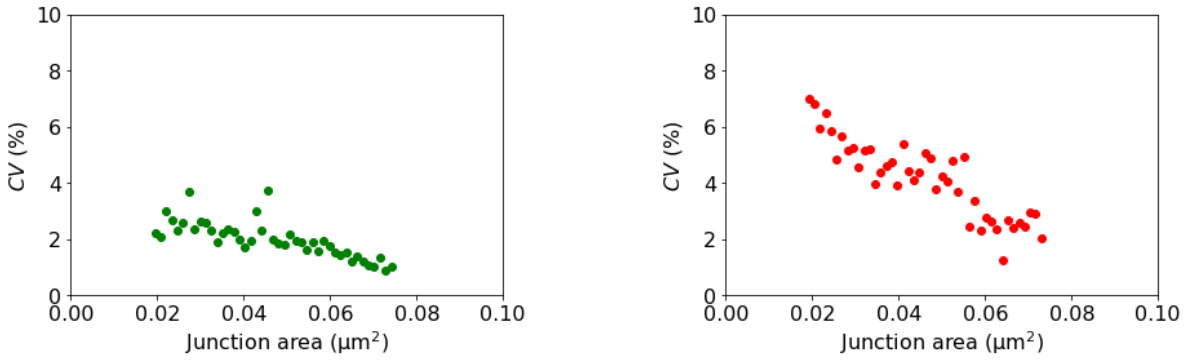
(a) Dolan bridge junctions

(b) Manhattan junctions

Figure 3.3: (top) Mean conductance value of G as a function of designed junction overlap area of the SQUID loop. (bottom) Fabrication yield as a function of designed junction overlap area of the SQUID loop.

3.1.1. Coefficient of Variation

The Coefficient of Variation (CV) is a metric to study the variation of a certain parameter. In this case the CV is used to study the variation in the Josephson junction conductance. The CV of the conductance is defined as the standard deviation divided by the mean, thus $CV_G = \frac{\sigma_G}{\overline{G}}$. In figure 3.4 the CV for the Dolan bridge and Manhattan junctions are plotted as a function of the designed junction overlap area of the SQUID loop. From this figure we see that the CV increases for smaller junction areas. This corresponds with Osman et al. [76] where a similar behaviour of the CV as a function of the designed Josephson junction area for the Manhattan junction is shown. Furthermore, it should be noted that the CV for Manhattan junctions is larger than for the Dolan bridge junctions. This can be explained by the fact that the overlap area of the Manhattan style junction is determined by the width of both electrodes, whereas for the Dolan bridge junction only the top electrode plays an important role. By depending on both electrodes, the Manhattan style junction is more sensitive to variations.



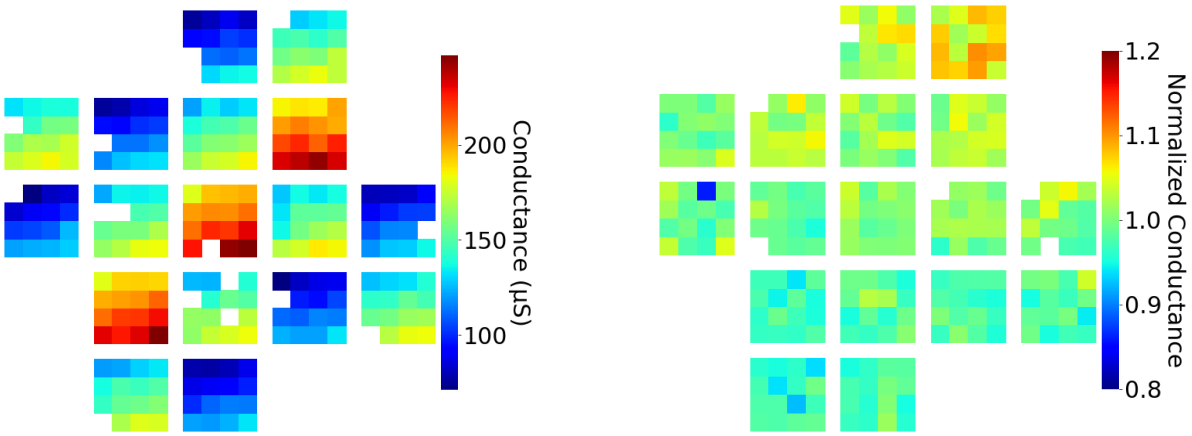
(a) CV for Dolan bridge junctions.

(b) CV for Manhattan junctions.

Figure 3.4: CV of the Josephson junction conductance as a function of the designed junction area of the SQUID loop. The CV for Dolan bridge junctions is lower than for the Manhattan junctions.

3.1.2. Heatmap

The mean conductance, fabrication yield and the coefficient of variation can be used to show the dependence of these parameters on the designed junction area. However, these metrics do not show the variations across the wafer. To determine if the position of the Josephson junction on the wafer is important a heatmap is used. The heatmap shows the measured conductance as a function of the X and Y coordinate and thus allows for a visual interpretation of the data. An example of the heatmap of a single die can be seen in figure 3.5a, using the same layout as figure 3.2a. From this figure the three frequency groups can clearly be seen as well as the sweep from left to right, top to bottom per array. The problem with this heatmap is that is becomes difficult to compare values to each other, due to the difference in width of the variable electrode. Therefore, the heatmap is normalized by dividing the conductance of a Josephson junction width a certain width by the average of all the junction with the same width. This normalized heatmap can be seen in figure 3.5b.



(a) Heatmap for a single die.

(b) Normalized heatmap for a single die.

Figure 3.5: Heatmap for a single die. The white spaces correspond to shorted, open or half-open junctions.

This normalized heatmap shows that there are some variations in the Josephson junction conductance, but nothing significant yet. The normalization of the heatmap becomes more interesting when it is done for all the dies on the wafer, as seen in figure 3.6. Here the D (M) stands for Dolan (Manhattan) and the number for the die position from left to right and the c (e) for center (edge). This figure shows that the variation in the conductance of Josephson junction fabricated using a Dolan bridge is much lower than for junctions fabricated with the Manhattan layout. In both cases there seem to be a dependency on the wafer position, where junctions towards the center of the wafer have a higher conductance than junctions towards the edges. For Dolan bridge junctions these variations may be attributed to the resist thickness, which is approximately 20 nm thinner at the edges than at the center. The variations in the Manhattan style junctions are hypothesised to be caused by the non-uniform NbTiN base layer. Another possible cause of the variation is discussed in chapter 5.

3.1.3. Single Die Deposition

To study the influence of the NbtiN base layer another wafer such as figure 3.2b is fabricated, but instead of doing a single deposition to fabricate the Josephson junctions on each die a different procedure is used. After the fabrication of the base layer the wafer is diced into eight dies. These dies follow the same procedure to fabricate Josephson junctions as used on the half wafer. Using these single dies it is possible to create a similar figure as the bottom half of figure 3.6. If the NbTiN base layer causes the variations of the Manhattan style junctions across the half wafer, the single die depositions should yield a similar result as the half wafer. The conductance as a function of the position on the wafer for the single die depositions can be seen in figure 3.7a and the normalized conductance in figure 3.7b.

The heatmap of the Manhattan style junctions for the single die and wafer-scale deposition show a similar behaviour, which could indicate that the uniformity of the NbTiN base layer plays a role in the fabrication of this junction type. The single die depositions did show larger variations in the overall conductance per die than the wafer-scale deposition. This could also indicate that there are difference in the formation of the tunnel barrier during the oxidation process, which cause these variations.

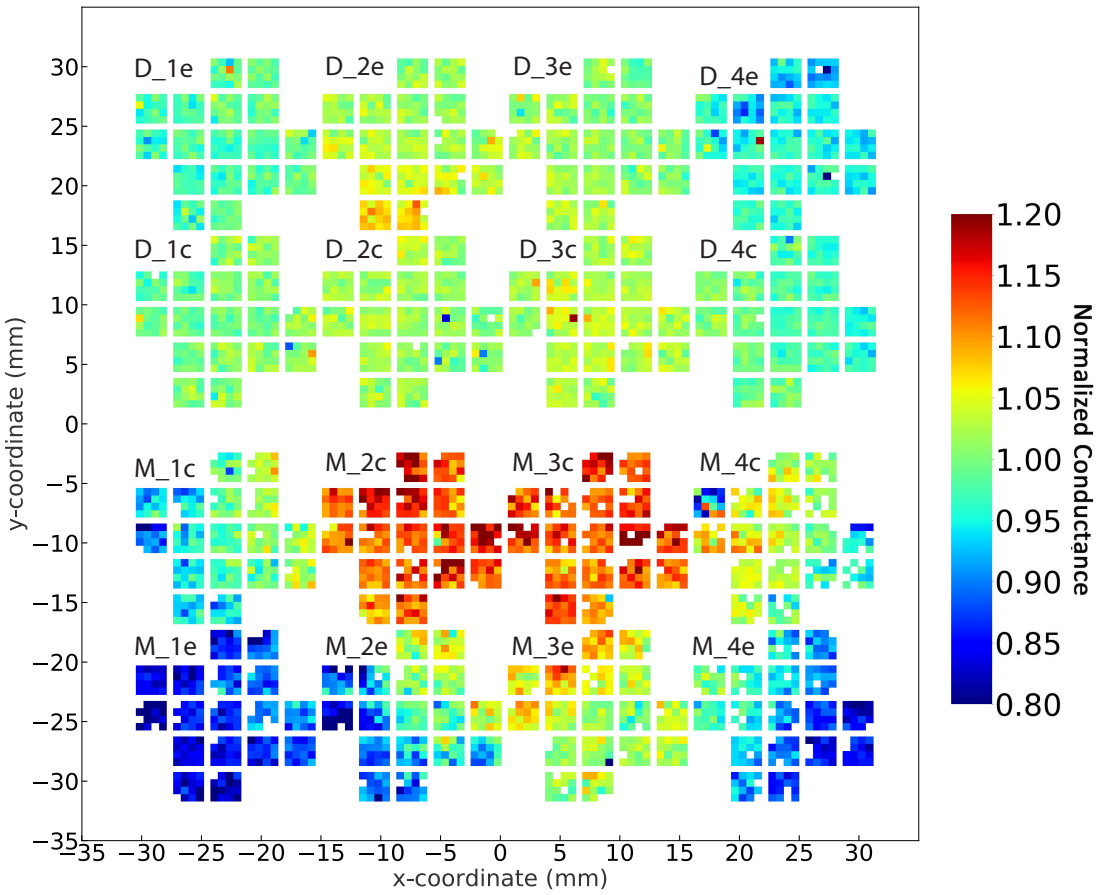
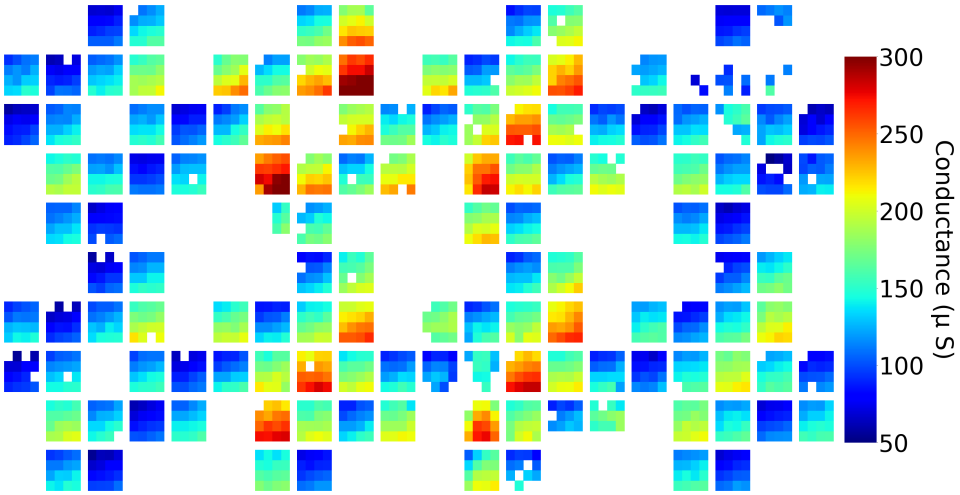
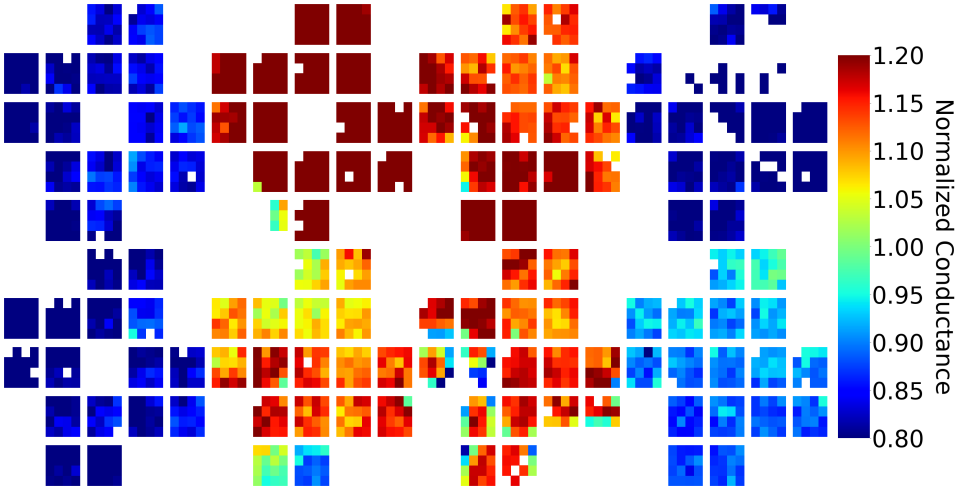


Figure 3.6: Normalized heatmap of the wafer used to study the variations in Josephson junction conductance. The normalization for Dolan bridge junctions and Manhattan junctions is done separately. Dolan bridge junctions seem to show some variations from center to edge, whereas Manhattan junctions show much larger variations.



(a) Conductance as a function of the position on the wafer for single die depositions. Due to a design problem the center pad of die 1c, 2c and 1e are missing.



(b) Normalized conductance as a function of the position on the wafer for single die depositions. Due to a design problem the center pad of die 1c, 2c and 1e are missing.

Figure 3.7: Heatmap of the conductance of Manhattan style Josephson junctions as a function of the position on the wafer. Figure 3.7a shows the heatmap for the single die depositions and figure 3.7b shows the normalized heatmap. This figure shows that there is still an increase in the conductance for the four samples in the middle of the figure. However the normalized heatmap shows that there are large variations in the conductance per die deposition.

3.1.4. Pearson Coefficient

To study the variations between the single die depositions and the wafer-scale deposition the Pearson coefficient is used. The Pearson coefficient can be used to see if two variables are related to each other. The coefficient will be between -1 and 1, where ± 1 corresponds to a perfect positive or negative correlation and 0 means that there is no correlation between the two variables. The coefficient is defined as:

$$r_{xy} = \frac{\sum_{i=1}^{n} (x_i - \bar{x})\left(y_i - \bar{y}\right)}{\sqrt{\sum_{i=1}^{n} (x_i - \bar{x})^2}\sqrt{\sum_{i=1}^{n} \left(y_i - \bar{y}\right)^2}} \tag{3.1}$$

where r_{xy} is the Pearson coefficient and x and y are the two variables that are related to each other. The two variables that we are comparing are the offset and the slope of the line fitted trough the data per die. The entire data set and the filtering are discussed in appendix A. Calculating the Pearson coefficient for the wafer scale deposition we find $r_{wafer} = 0.272$, which indicated that there is a weak correlation between the offset and the slope of this data set. Calculating the Pearson coefficient for the die scale deposition we find $r_{die} = 0.943$, which indicates a strong correlation between the two parameters. This correlation can be explained by the variations in the formation of the tunnel-barrier during the oxidation of the aluminum. During wafer-scale fabrication, this process is the same for each Josephson junction and thus there will be small random fluctuations in the offset and slope. For the single-die depositions the oxidation of the aluminum is different for each die and therefore there will result in differences in the offset and slope. Here the offset and the slope are correlated, since a thinner tunnel-barrier will increase the offset, but also the conductance of all the junctions on the sample. Since we expect that there are variations in the formation of the tunnel barrier for each fabrication round it is more useful to use larger samples.

Besides correlation the wafer scale and die scale depositions to each other, the coefficient can also be used to study the relation between the overlap area of the top and bottom electrode of the Josephson junction and the conductance measured at room temperature. For this purpose SEM images are taken of three SQUID loops, one from each frequency group, on all dies of the wafer scale deposition and the single die deposition. The position of the SQUID loops used for these SEM images can be seen in figure 3.8. For some of the single die depositions the pad corresponding to the high frequency was not fabricated. Therefore, for the single die depositions another high frequency pad was measured. In this case the pad left from the middle of the highlighted area is used.

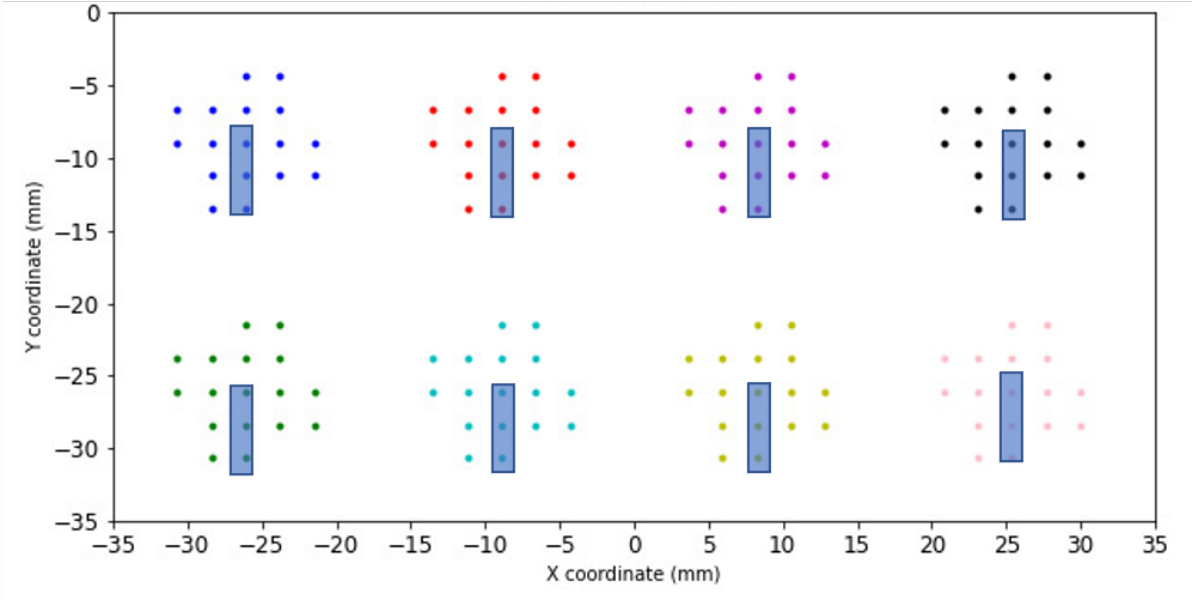


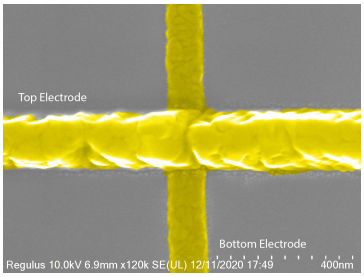
Figure 3.8: Schematic representation of the positions of the Josephson junctions used for the SEM analysis. The Y coordinates are negative to represent that this set corresponds to the bottom half of the wafer.

An example of the SEM images used for this analysis can be seen in figure 3.9. The overlap area is extracted by

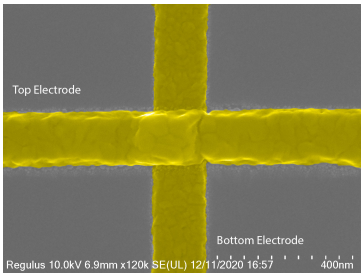
Table 3.1: Pearson coefficient of the overlap area and conductance measurements of Josephson junctions for three frequency groups.

Frequency Range	Wafer scale	Single die
Low	0.697	0.350
Middle	0.744	0.747
High	0.853	0.404

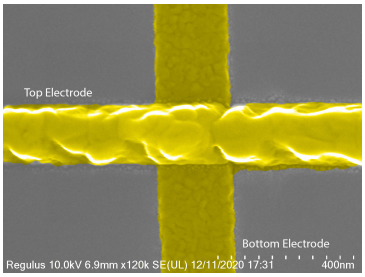
drawing a polygon around the overlap area of the top and bottom electrode using ImageJ. As seen from the figures the overlap area of Josephson junctions with a larger bottom electrode can be extracted with greater accuracy.



(a) False colored SEM image of a Josephson junction with a small bottom electrode, corresponding to a low frequency.



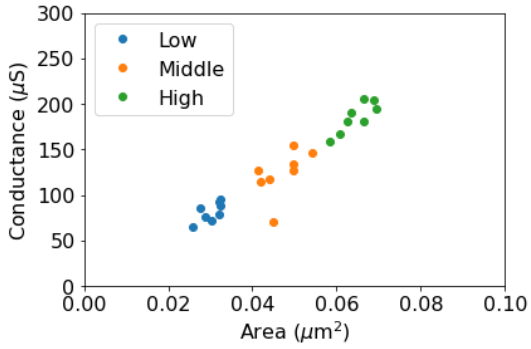
(b) False colored SEM image of a Josephson junction with a medium bottom electrode, corresponding to a middle frequency.



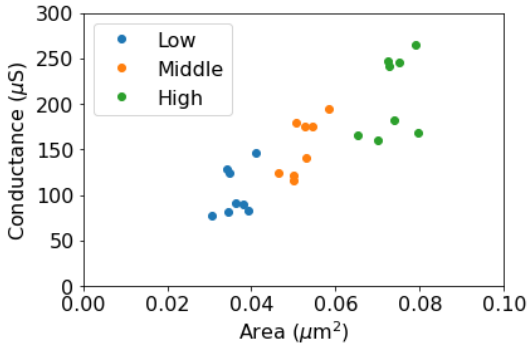
(c) False colored SEM image of a Josephson junction with a large bottom electrode, corresponding to a high frequency.

Figure 3.9: SEM images of three Josephson junction with different bottom electrode widths at a 120k magnification.

The correlation of the low, middle and high frequency SQUID loops for both deposition types are summarized in table 3.1. The table shows that for the wafer-scale fabrication the Pearson coefficient increases as the frequency increases and thus the overlap area. This increase can be explained by taking the sidewall contributions of the Josephson junction into account. The SEM image can only be used to determine the overlap area between the top and bottom electrode, but not the sidewalls. These sidewalls will have a constant contribution to the overlap area since it depends on the top electrode which has fixed width. This can be used to explain why the coefficient increases for larger bottom electrodes, because in this case the contribution is relatively less when compared with smaller bottom electrodes.
For the single die depositions there seem to be a weak correlation for both the low and high frequency junctions. This weak correlation indicates that for the single die depositions the overlap area is less dominant and that in these depositions the variations in the tunnel barrier per die are dominant. It is interesting to note that for the middle frequency junction there seems to be a strong correlation.
The graphical overview of the data used to determine the Pearson coefficient can be seen in figure 3.10. This figure shows that there is a larger spread for the single die depositions than the wafer-scale deposition.



(a) Correlation between the measured conductance and the junction overlap area for the wafer-scale deposition.



(b) Correlation between the measured conductance and the junction overlap area for the single die deposition.

Figure 3.10: Correlation between the measured conductance and the junction overlap area for both the wafer-scale and single die deposition. These figures show that the wafer-scale deposition has a smaller spread than the single die depositions.

Table 3.2: Average CV and yield for all fabricated dies. The position of each die can be seen in figure 3.6.

	Wafer scale				Single die	
	Dolan Bridge		Manhattan		Manhattan	
	CV (%)	Yield (%)	CV	Yield (%)	CV	Yield (%)
1c	2.173	99.3	4.813	94.5	4.449	92.6
2c	2.191	99.3	2.998	94.1	5.823	86.8
3c	2.019	99.3	3.355	87.9	4.169	96.3
4c	2.182	99.6	5.333	86.4	8.125	77.2
1e	2.284	100	4.385	92.6	4.244	90.1
2e	2.456	98.2	7.936	97.1	6.288	98.5
3e	1.928	99.3	3.294	94.1	7.575	90.1
4e	3.334	99.3	5.563	89.7	3.397	97.8

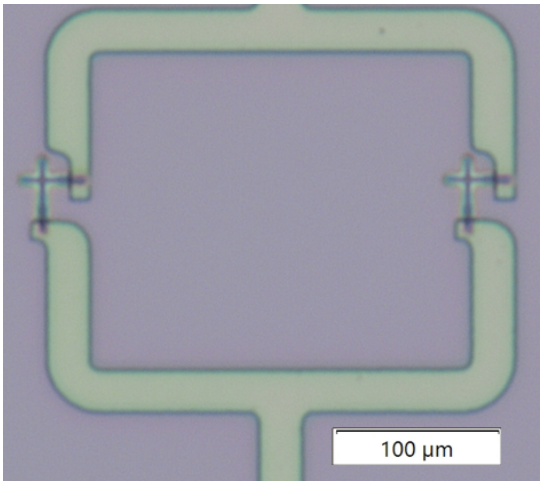
To summarize the results of the Surface-17 test designs, the coefficient of variation and the junction fabrication yield is given for both junction types in table 3.2.

3.2. NbTiN Base Comparison

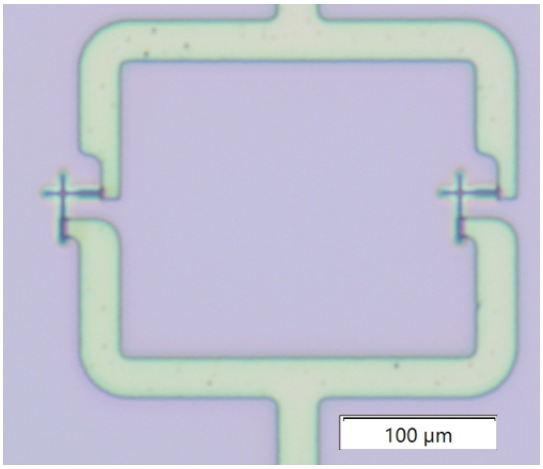
This section gives a short comparison between the planar and non-planar NbTiN base layer. The non-planar base is referred to as a base that has TSV in it. These TSV will affect the spinning of the resist, which will result in a non-uniform layer. A uniform resist layer is required for the fabrication of a Dolan-bridge, therefore the hypothesis is that the Dolan-bridge junction will perform worse than the Manhattan style junctions, which are less sensitive to resist height variations.

3.2.1. Planar Base

For the experiment on the planar base a 35×35 array of Josephson junctions is used. In each pad two Josephson junctions in a SQUID formation are fabricated with a top and bottom electrode width of 0.2 µm, resulting in an overlap area of 0.04 μm^2, or 0.08 μm^2 if both the junctions in the SQUID loop are taken into account. An optical image of the test pad and the SQUID post development of the junction pattern can be seen in figure 3.11a. After development a misalignment in the position of the Josephson junctions is observed as seen in figure 3.11b. This misalignment is caused by a drift in the EBPG system. In the corner the EBPG start writing the junction is properly aligned, however over time the drift results in a misalignment of the junctions.



(a) Properly aligned junctions.



(b) Misaligned junctions.

Figure 3.11: Optical images of the NbTiN base layer and the pattern used for the fabrication of Josephson junctions after development.

Despite the misalignment of the Josephson junctions openings, the sample is still used to fabricated Josephson junctions as for the junctions to work there does not have to be a large contact to the NbTiN base layer. After measuring the Josephson junctions using two-point probe conductance measurements and removing shorted and open junctions, conductance below 20 µS and above 500 µS, we find a junction yield of 98.3%, which is a normal value for the yield. However, the coefficient of variation is quite high for this wafer, 14.64%. A reason for this increase in the CV is the SQUID loop used for this experiment, in a SQUID loop it is possible for one junction to function properly, while the other junction is open, resulting in a half-open junction. The half-open junctions are filtered by removing junctions that have a conductance lower than 70% of the mean of the entire sample. In this case the yield reduces to 93.4%, which is the lowest yield reported in this work. Furthermore, the CV reduces to 10.6%, which shows more similarity to all aluminum junctions. The CV is still larger than the typically values reported in this work. We hypothesise that this increase is caused by the NbTiN base layer, however the mechanism is unclear at this point. The mean normalized conductance as a function of the X and Y coordinate is represented in figure 3.12. This figure again shows an increase in the conductance towards the middle right of the wafer, this is logical as this behaviour was already observed for junctions fabricated on a bare Si wafer. Lastly we report an average conductance of $(25 \pm 3) \cdot 10^1$ µS across the entire wafer, which is inline with the other junctions fabricated on a planar die. Due to time limitations Dolan bridge junctions are not fabricated on a planar base.

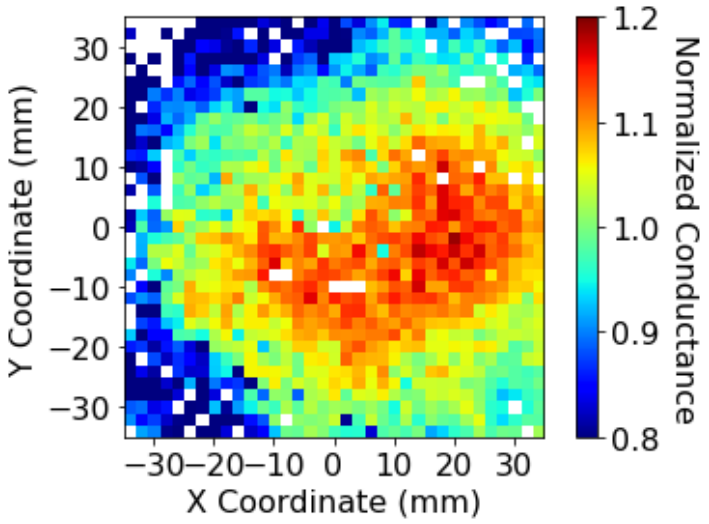


Figure 3.12: Mean normalized conductance as a function of the X and Y coordinate for Manhattan style Josephson junctions fabricated on a planar NbTiN base layer.

3.2.2. Non-Planar Base

Both Manhattan style junctions and Dolan bridge junctions are fabricated on a non-planar base. Instead of a 100 mm wafer, these samples are fabricated a sample with an effective area of 13 × 13 mm, which is the same as a Surface-17 device. For both junction types a unit cell of 5 × 5 test pads is used. In this unit cell the junction overlap area is increased from left to right, top to bottom. Here the opening in the resist for the top electrode of the Dolan bridge junction and the bottom electrode for Manhattan style junctions have a width ranging from 0.052 µm to 0.244 µm in steps of 0.008 µm. There are a total of 25 unit cells on a chip, in a 5 × 5 configuration, which in total gives an array of 25 × 25 junction test pads.

The layout used to fabricated junctions on the non-planar base can be seen in figure 3.13. On the top there are eight chips that have the same size as a Surface-17 device and on the bottom twelve chips that have the same size as a Surface-7 device. In this work only the larger chips on the top are used. From the eight chips, three are used to fabricated Dolan bridge junctions on. Another three are used for Manhattan style junctions and the remaining two are a mix of both junction types. The circles in the figure indicate the position of through silicon vias. The junctions on the device are measured using two-probe conductance measurements. The Josephson junction conductance as a function of the overlap area of both junction types is reported in figure 3.14. In this figure only the best chip is taken into account. This figure shows that there is a larger spread in the conductance of Josephson junctions fabricated with a Dolan bridge than those with a Manhattan layout. In both cases there is a large spread, which is also represented by the accuracy of the linear fit.

For the Dolan bridge junctions there is an offset of $(1 \pm 2) \cdot 10^1$ µS and a slope of $(2 \pm 9) \cdot 10^3$ µS/µm^2. In both cases the uncertainty is larger than the value, which corresponds with the large spread in the data. For the Manhattan style junctions there is an offset of $(3 \pm 1) \cdot 10^1$ µS and a slope of $(4 \pm 5) \cdot 10^3$ µS/µm^2. Again there is a large uncertainty in both fit parameters, which corresponds with the data. The measured conductance can be used to predict the qubit frequency, which is seen in the right panels of figure 3.14. To calculate the qubit frequency a magic number of 135 GHz kΩ and an $E_C = 0.3$ GHz.

In order to study the large variations in the measured conductance the residual standard deviation is plotted, as seen in figure 3.15. This residual standard deviation is the difference in the predicted frequency from the fit through the data. The figure shows that for the Dolan bride junctions there is a larger spread in the residuals than for the Manhattan junctions.

Figure 3.16 shows the heatmap for the normalized conductance measurements. In both figures there are white spots, which normally correspond to open or shorted junctions. In the case of a non-planar base it is possible that the junctions where fabricated on the position of via and that they therefore could not be

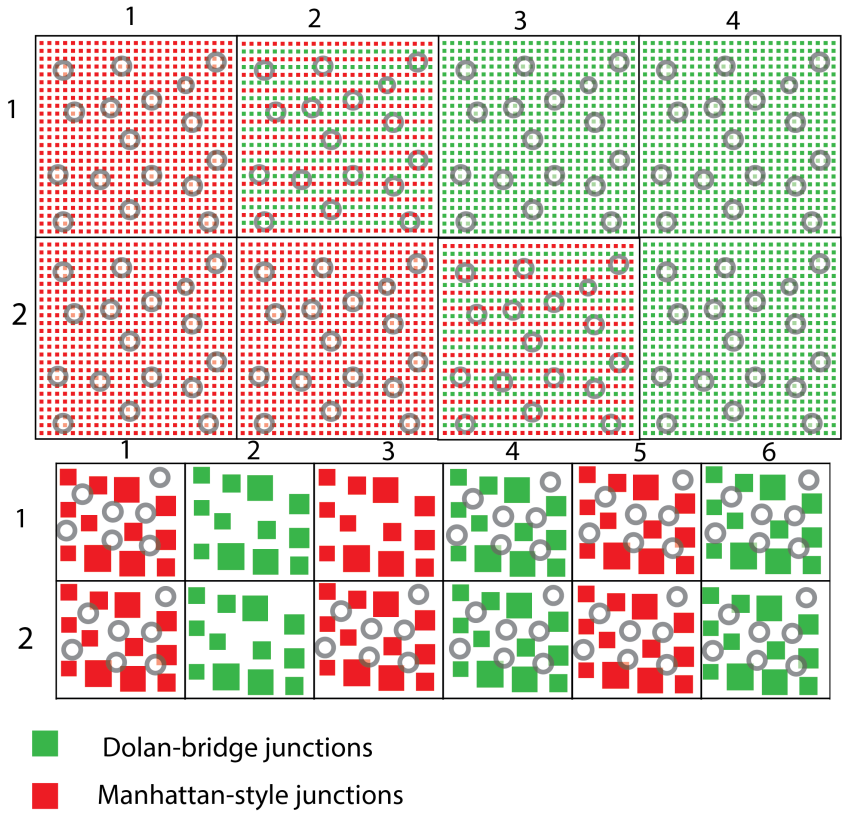
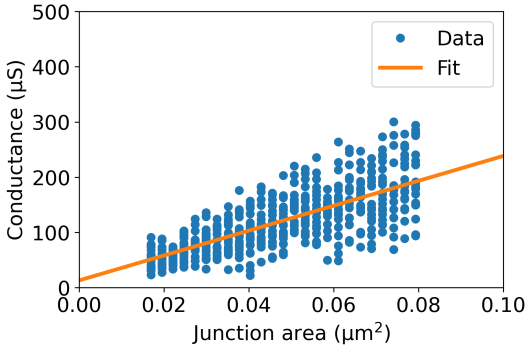
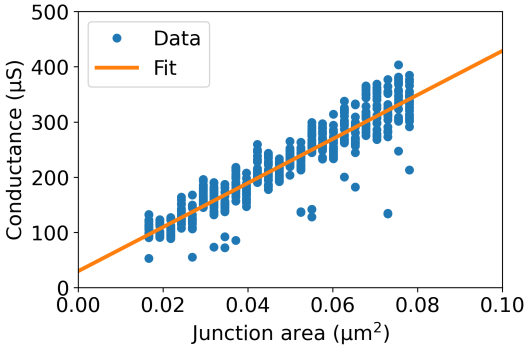


Figure 3.13: Schematic overview of wafer used to fabricat junctions on a non-planar base. The green (red) squares correspond to Dolan bridge (Manhattan style) junctions. The top eight chips consists of three complete Dolan chips, three complete Manhattan chips and two chips on which both junction types are fabricated. The circles in this layout correspond to the position of through silicon vias. In this work only the top chips are used, which have the same size as a Surface-17 device. The bottom chips have the same size as a Surface-7 device, which arrays of Dolan bridge and Manhattan junctions fabricated on it.

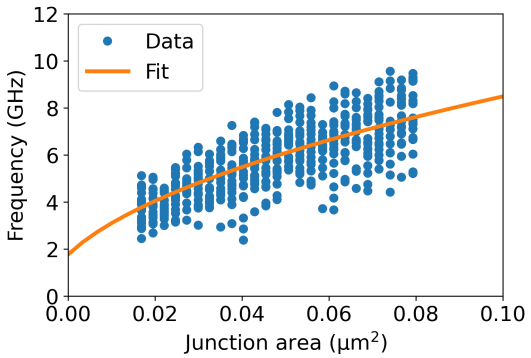
measured. This figure shows that the Manhattan style junctions are relatively uniform when compared to the Dolan bridge junctions. Finally, the coefficient of variation as a function of the overlap area is plotted in figure 3.17. This figures again shows that the Dolan bridge junctions suffer from much larger variations than the Manhattan style junctions.



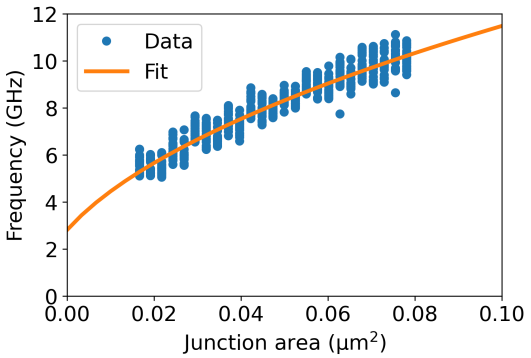
(a) Conductance as a function of the overlap area for Dolan bridge junctions.



(b) Conductance as a function of the overlap area for Manhattan style junctions.

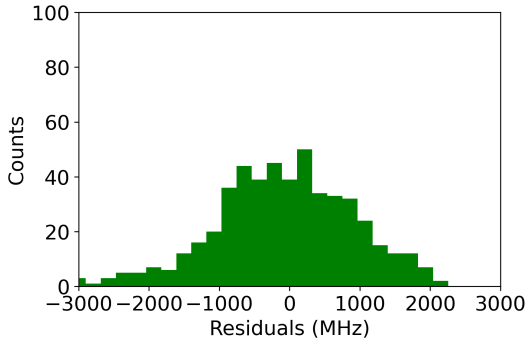


(c) Predicted qubit frequency as a function of the overlap area for Dolan bridge junctions.

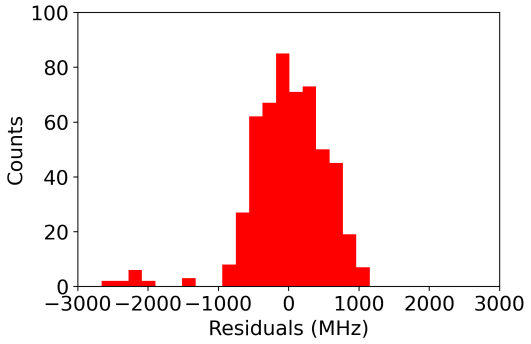


(d) Predicted qubit frequency as a function of the overlap area for Manhattan style junctions.

Figure 3.14: Conductance and predicted qubit frequency as a function of the overlap area for both Josephson junction types.

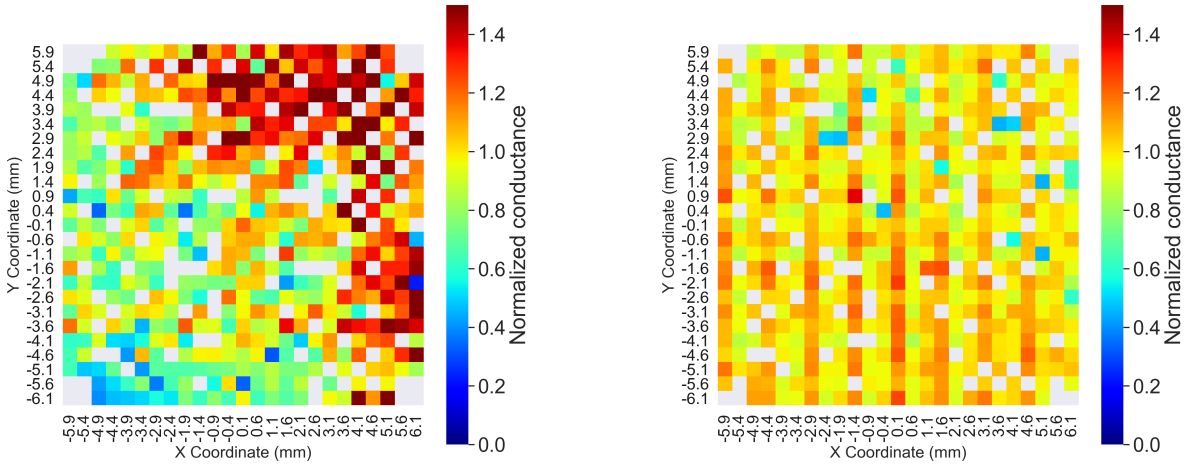


(a) Residual standard deviation for Dolan bridge junctions.



(b) Residual standard deviation for Manhattan style junctions.

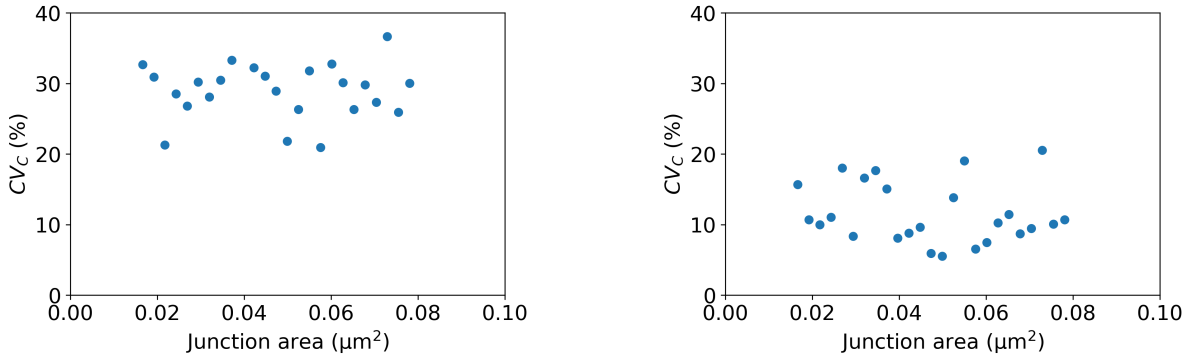
Figure 3.15: Conductance and predicted qubit frequency as a function of the overlap area for both Josephson junction types.



(a) Dolan bridge junctions.

(b) Manhattan style junctions.

Figure 3.16: Normalized conductance as a function of the X and Y coordinate for both junction types.



(a) Dolan bridge junctions.

(b) Manhattan style junctions.

Figure 3.17: Coefficient of variation as a function of the overlap area for a non-planar base.

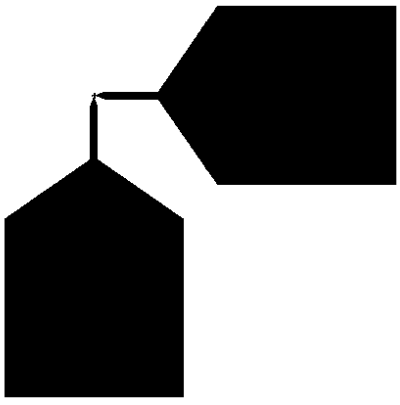
4

All Aluminum Junctions

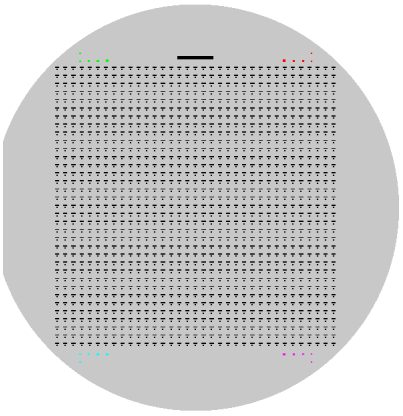
In this chapter the uniformity of the Manhattan Josephson junctions is studied by changing the fabrication recipe to determine the influence of certain steps. For this study a simplified fabrication procedure is used. Instead of using a base of NbTiN the junctions are fabricated on a plain Si wafer. This change in base allows for a shorter test cycle, since fabricating junctions on a plain Si wafer takes approximately two days, whereas junction on a NbTiN base take five days. Additionally, since the fabrication procedure requires less steps, this also removes the dependency of some fabrication steps. The fabrication procedure for the all aluminum junctions is described in Appendix C.

4.1. Design

The all aluminum junctions consists of two measurements pads that are perpendicular to each other and are connected via a Josephson junction. The design is fabricated in a single electron beam lithography step, which patterns both the pads and the junctions. The design of the fabricated aluminum junctions differs from the junctions fabricated on the NbTiN base in two ways. First, the junctions fabricated on a NbTiN base are placed in a SQUID loop, hence per measurement two junctions were measured. For the all Al junctions single Josephson junctions are used. Second, the junctions on the NbTiN base can be measured using the NbTiN pads, whereas for the aluminum junctions these are not present. Therefore, the pads are fabricated in the same deposition step as the junctions. By using this fabrication procedure, spurious junctions are created on both the measurement pads. However, since the pads are significantly larger than the junction overlap area (100×100 µm opposed to 200×200 nm) these contributions can be ignored. The layout of these junctions can be seen in figure 4.1a. In these junctions both the electrodes have a width of 200 nm. These junctions are fabricated on a 100 mm wafer in an array of 35x35, as seen in figure 4.1b.



(a) Layout of the all aluminum junction. Both electrodes have a width of 200 nm.



(b) Layout of the array used for the all aluminum junctions on a 100 mm wafer.

Figure 4.1: Schematic representation of the design used to study the variations in the conductance on a bare Si wafer.

4.2. Ashing

For these experiments the parameters in the ashing step are changed. The ashing step uses reactive ion etching with an O_2 plasma to remove resist residuals in the developed areas. The hypothesis is that the reactive ion etch process is not completely anisotropic. This will result in a non-uniform etch pattern of the top resist layer across the sample. This will unevenly open the resist causing variations in the overlap area.

4.2.1. Baseline

Before the ashing step is changed we require a baseline on the performance of all aluminum junctions with the standard fabrication recipe. For this baseline we use a unit cell consisting of four junctions in a 2x2 formation in the same 35x35 array. This allows us to take the average of each cell, thus filtering the outliers. Obvious shorts and opens are removed from the dataset prior to the filtering. For the baseline two experiments are performed. The first baseline (Wafer 1) consists of a junction deposition without junction pre-treatment procedure and the second baseline (Wafer 2) consist of a junction deposition with the standard fabrication procedure. With pre-treatment procedure we refer to the resist ashing using an O_2 plasma and the removal of SiO_x using BOE before junction deposition. For the resist ashing a RIE process is used at a pressure of 10 µbar. The results of these experiments are summarized in figure 4.3 and table 4.1/ The figure shows a heatmap of the conductance as a function of the X and Y coordinate. For this figure junctions with a conductance below 20 µS and above 500 µS are removed, since these correspond to open and shorted junctions.

From these figures we can see that the conductance pattern of the baseline test with pre-junction treatment is more uniform than the baseline without the treatment. While a heatmap allows for an intuitive analysis of the data, it is still subjective. A better metric to quantify the spread would be the CV, which is therefore used to analyse these results. The CV for the wafer without pre-treatment is 14.26%, which is significantly higher than the CV for the wafer with pre-treatment is 8.73%. From this baseline experiment we can conclude that the pre-junction treatment allows for the fabrication of more uniform junction across the wafer. Furthermore, it is interesting to note that for wafer 2 the conductance seems to increase towards the middle right.

The increase of the conductance towards the middle right seems to indicate that there is a process in our recipe that is not uniform. The primary suspects that could introduce such non-uniformities are the resist ashing and the deposition of the Josephson junction, since these are the most directional processes in the fabrication recipe. The ashing step shows an increase in uniformity, therefore the role of this step is investigated further. The design is changed to a 35x35 grid of single junctions, instead of the unit cell of four junctions, in order to speed up the measurements.

First, a wafer is fabricated with the standard recipe (Wafer 3), to establish a baseline for the new design and to determine if there is still an increase in junction conductivity towards the middle right. For the second test (Wafer 4) a Si wafer with <111> orientation is used, while positioning the wafer with a 180° rotation with respect to the normal procedure. This allows us to determine if the crystal orientation of the wafer influences the process, as well as changing the orientation. The results of these tests are again represented in figure 4.3 and table 4.1. The heatmap of wafer 3 is not shown as this displays a similar dependence as wafer 2. For wafer 3 the yield is similar to that of wafer 2, which makes sense as the same procedure is used. Furthermore we note that the CV is decreased while the average conductance is increased, which we attribute to random variations. For the wafer 4 there are large variations in the conductance, this is also reflected in the CV, which has increased to 12.50%. The yield for both wafers remains similar.

4.2.2. Rotated Ashing

The paper by Kriekebaum et al. [77], reports that non-radially symmetric gradients are reduced and made more radially symmetric by splitting the ashing step into multiple shorter ashing steps, while rotating the substrate between these steps. This paper uses a Plasma Etch PE-50 that is able to create an oxygen plasma at ≈ 500 mbar, which is a much higher pressure than our fabrication process which operates at ≈ 10 μbar. In an attempt to reduce the variations in the measured conductance across the wafer the same procedure as Kriekebaum et al. is followed.

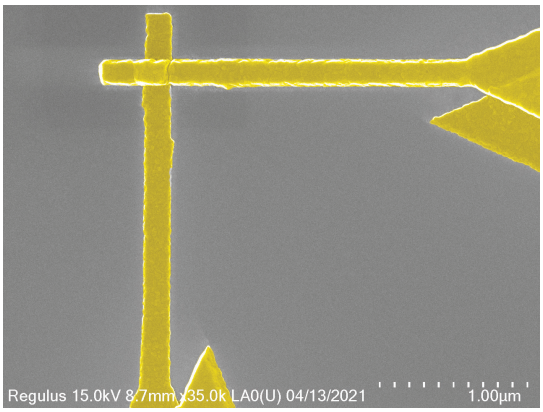
The first experiment (Wafer 5) consists of breaking the 45 s ashing step into four ashing steps of 12 s each. The wafer is positioned at the center of the chamber and rotated by 90° after each ashing step. From the

data we find that rotating the wafer four times during ashing does not remove the increase in conductance towards the center right, while introducing some spots with a much lower conductance. These variations are reflected in the CV, which increases to 10.94%.

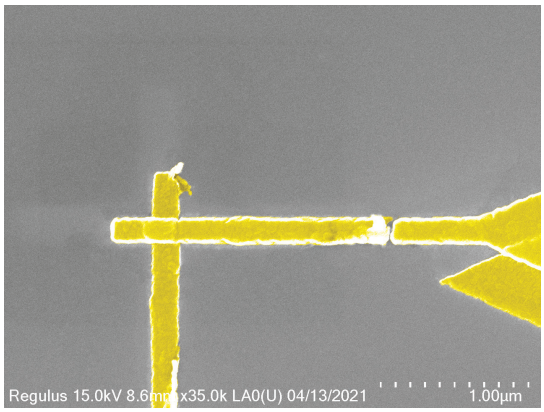
The second experiment (Wafer 6) consists of rotating the substrate sixteen times, four rotations of 90° in four corners of the chamber. Since the wafer is rotated a total of sixteen times the ashing time has to be decreased, otherwise this sample would be ashed for a much longer time. Therefore the time of each ash step is 5 seconds. From this test we find that the conductance again increases towards the middle right. The CV is reduced to 7.51%, which is the lowest measured value for the all aluminum junctions. From these tests we find that rotating the wafer between ashing steps does not seem to yield a significant improvement in the uniformity with the current fabrication process. The problem that arises with rotating the substrate is that it becomes difficult to reproduce, while rotating the substrate four times in the center of the chamber is still manageable, the sixteen times rotation is difficult to reproduce and is therefore not recommended for further experiments.

4.2.3. Tepla

The final test (Wafer 7) consists of using a different plasma etching system, the PVA Tepla 300, that is able to operate at a higher pressure (≈ 1 mbar). This higher pressure allows for an isotropic plasma. The idea is that while it is difficult to create a highly an-isotropic plasma it might be easier to create a highly isotropic plasma. If the isotropic plasma removes oxide everywhere, it might allow for uniform fabrication of Josephson junctions. In this test the system was set to a flow of 170 SSCM O_2, a power of 100 W which resulted in an intensity of 76 and a pressure of ≈ 0.6 mbar. The sample was etched for 2 minutes under these conditions. The results of these tests are again represented in figure 4.3 and table 4.1. From this figure we see that the conductance seems to be randomly distributed across the wafer, as expected. However, the CV has increased to 10.75%. The non-normalized conductance values for this sample were also significantly lower when compared to other wafers. This could indicate that the Tepla did not remove enough resist residuals, which would affect the Josephson junction. To further investigate this hypotheses a SEM analysis is performed, from this we find that most junctions show no defects, figure 4.2a, however some junctions show obvious defects such as figure 4.2b. These defects seem to indicate that resist residuals were present during the junction deposition. During lift-off these residuals are removed, resulting in the lift-off of some of the junctions fingers. The presence of resist residuals indicate that the oxygen plasma etching was not applied long enough to remove all of the residuals.



(a) False colored SEM image of an all aluminum junction.



(b) False colored SEM image of an open all aluminum junction.

Figure 4.2: False colored SEM images of all aluminum junctions at a magnification of 35k. The right figure shows a gap in the aluminum resulting in an open junction. The blue corresponds to aluminum.

The yield and coefficient of variations are summarized in table 4.1. From these tests we can conclude that the ashing and removal of SiO_x post development and pre deposition result in a reduction of the coefficient of variations and thus improve the uniformity of Josephson junctions across a 100 mm wafer, while slightly reducing the yield. Furthermore the ashing and BOE seem to increase the average conductance across the wafer. This could be attributed to the O_2 plasma, that etches the resist and opens the developed area, which is used as the mask for the junction deposition. Thus the etching could increase the overlap area of the junc-

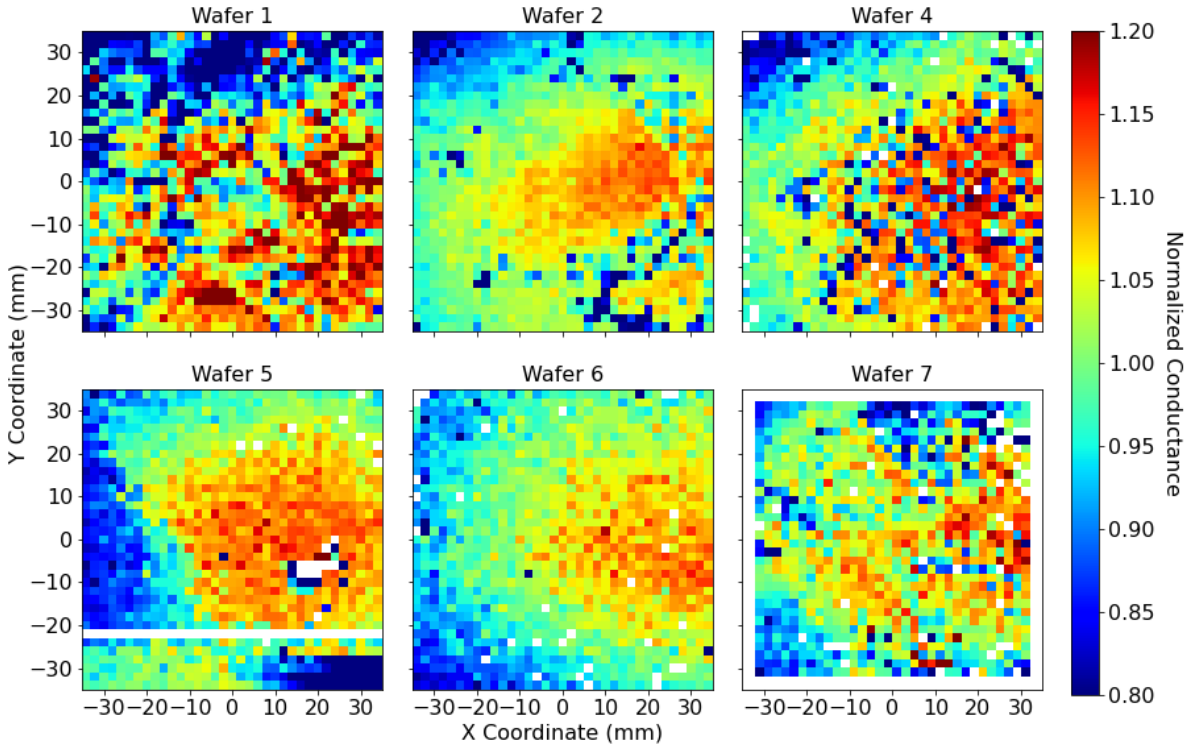


Figure 4.3: Mean normalized conductance as a function of X and Y coordinate of the wafers used to test the influence of ashing on the uniformity of Josephson junctions across a 100 mm wafer. Wafer 1 is fabricated without an ashing step. Wafer 2 is fabricated with the standard ashing procedure. Wafer 4 is fabricated on a <111> substrate while ashed with 180° rotation compared to the other samples. For wafer 5 the ashing step is divided into 4 steps, which combined have a similar ash time as the normal recipe. The wafer is rotated 90° between each ashing step. Wafer 6 is fabricated by dividing the ashing step into 16 separate steps while rotating the wafer 90° four times in four corners of the system chamber. Wafer 7 is fabricated using an ashing step in another system.

tion. Another explanation for the variations in the average conductance could be variations in the formation of the tunnel barrier used for the junction. The cause of these variations is not investigated. The average conductance of all the Josephson junctions without junction pre-treatment is lower than for the junctions with the treatment, which is inline with Kriekebaum et al. [77]. The experiments used for the investigation of the ashing step did not show a significant decrease in the coefficient of variation. This indicates that there is another limiting factor that causes these variations. The primary suspect for these variations is the deposition machine used for the Josephson junctions. Further research is required in order to determine if this is the cause for the variations.

To conclude the CV of these samples can be compared with papers from Osman et al. [76] and Kreikebaum et al. [77]. The design used for the aluminum junctions have an overlap area of 0.04 µm, across a 3.5x3.5 cm area. Osman et al. fabricates junctions with the same size on an area of 2x2 cm. This paper reports a CV of ≈ 3.8, which is comparable with the results we report. Kreikebaum et al. report a CV of 3.5 % across a 100 mm wafer for single Josephson junctions, which is significantly lower than the values reported by us. Furthermore this paper reports an average CV of dies with a size of 1x1 cm on the best wafer of 1.7%, with some dies < 1.0% variations. This is again a lower then our fabrication process as we report a variation of 1.82 % for a 1x1 cm area. This indicates that changes in our current fabrication recipe allows for a higher fabrication of Josephson junctions on a 100 mm wafer.

Table 4.1: Overview of the wafers used to determine the influence of the ashing on the Josephson junction uniformity. The table list the system used for the ashing step, the number of rotations used during each ashing step, the Josephson junctions yield, the coefficient of variation, the coefficient of variation for a smaller area, the average conductance, the standard deviation and the number of Josephson junctions on each sample.

Wafer	Ash system	Rotations	Yield (%)	CV (%)	$CV_{2x2\ cm}$ (%)	$CV_{1x1\ cm}$ (%)	$\overline{G}(\mu S \cdot 10^1)$	# of JJ's
Wafer 1	-	-	98.0	14.26	8.57	6.56	9 ± 1	4900
Wafer 2	F1	-	97.2	8.73	4.16	1.82	14 ± 1	4900
Wafer 3	F1	-	97.6	7.10	3.07	2.10	18 ± 1	1225
Wafer 4	F1	-	97.5	12.50	9.97	4.47	13 ± 2	1225
Wafer 5	F1	4	95.5	10.94	5.69	2.10	20 ± 2	1225
Wafer 6	F1	16	97.2	7.51	3.45	3.47	17 ± 1	1225
Wafer 7	Tepla	-	96.0	10.75	6.22	3.84	13 ± 1	1024

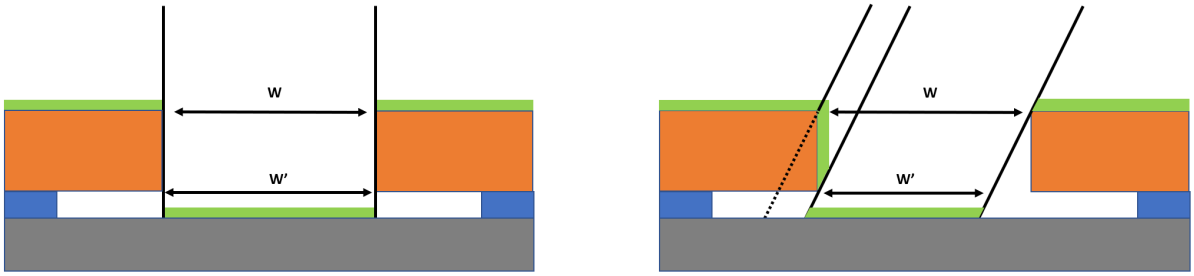
5

Geometric Model

To explain the variations in the conductance of Manhattan junctions we propose a geometric model [78], which is in line with Kriekebaum et al. [79]. In this model, the variation in the width of the junction finger is related to the thickness of the top resist which acts as a shadow mask during junction deposition. This shadowing effect causes the width of the fingers of the junction to become thinner towards the edges of the wafer. The model uses the assumption that the crucible of the deposition machine is a point source, which is a valid approximation for our deposition machine the Plassys MEB550. The model is later on expanded to take the sidewall contributions and variations due to the tilt into account.

5.1. Resist Shadowing

First the model is introduced as a one-dimension problem, which serves as the basis to expand it later on. The one-dimensional problem is described in figure 5.1. During the deposition of both the top and bottom electrode the actual deposited width. W', will be different than the designed width W. This difference is caused by the top resist layer, which will prevent material from reaching the silicon. The junction openings in the middle of the wafer are perpendicular to the deposition source, therefore the designed and deposited junction width will be the same, as seen in figure 5.1a. However, the junction openings at the edge of the wafer are further away and thus the incidence of the deposited material will have an angle θ with respect to the wafer. This angle causes material to be deposited on the top resist layer, instead of the silicon, as seen in figure 5.1b. This variation between the designed and actual width $\Delta = W - W'$, can be calculated according



(a) Deposition geometry when the junction opening is perpendicular to the metal source.

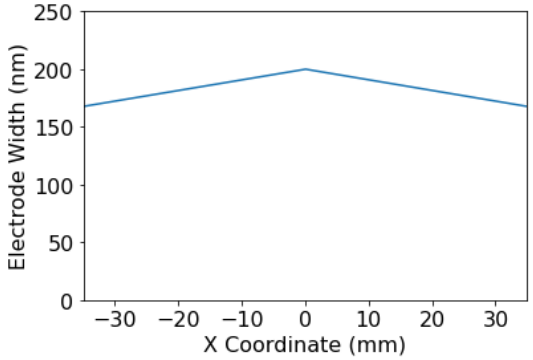
(b) Deposition geometry when the junction opening is tilted with respect to the source.

Figure 5.1: Schematic representation of the one dimensional view of the model. The black lines represent the direction of the deposited metal. The colors corresponds to: Green - Al, Orange - PMMA, Blue - PMGI, Grey - Si.

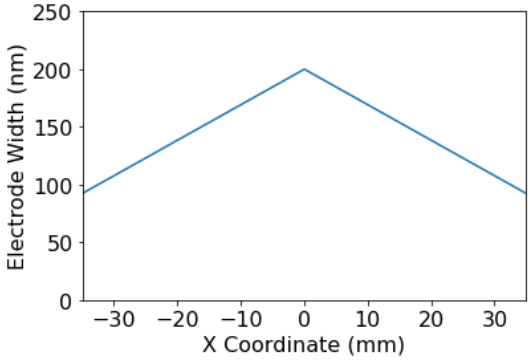
to $\Delta = H/\tan(\theta)$, where H is the height of the top resist and θ is the incident angle of the deposited metal. The angle $\theta = \arctan(D/x)$ depends on the distance from the crucible to the wafer, D, and the position on the junction opening on the wafer, x. Thus the total variation can be expressed as:

$$W' = W - H\frac{|x|}{D} \tag{5.1}$$

Here we take the absolute value of x, since the variation should be symmetric along the x-axis. The result of the change in width for a single electrode can be seen in figure 5.2. It shows that the width of the electrode is equal to the designed width at the center of the wafer and decreases linearly as it moves towards the edges. It also shows a dependence on the height of the top resist layer. The X coordinate is plotted from −35 mm till 35 mm, since this is the maximum width that can be used when a square is cut from a 100 mm wafer.



(a) Electrode width as a function of the X coordinate with a designed electrode width of 200 nm and a 600 nm top resist thickness.



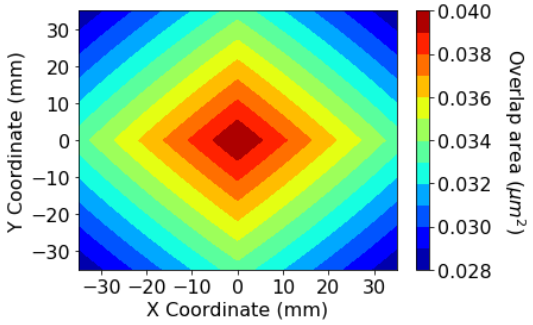
(b) Electrode width as a function of the X coordinate with a designed electrode width of 200 nm and a 2000 nm top resist thickness.

Figure 5.2: Electrode width as a function of the X coordinate according to equation 5.1. The designed width, W, is 200 nm and the distance from the wafer to crucible, D is 650 mm. The height of the top resist is changed, to show the dependence on this parameter. In figure 5.2a the top resist has a height of 600 nm and in figure 5.2b a height of 2000 nm. These figures show that the width is the largest at the center and linearly decreases towards the edges, where an increase in the top resist height results in a larger change as a function of the X coordinate.

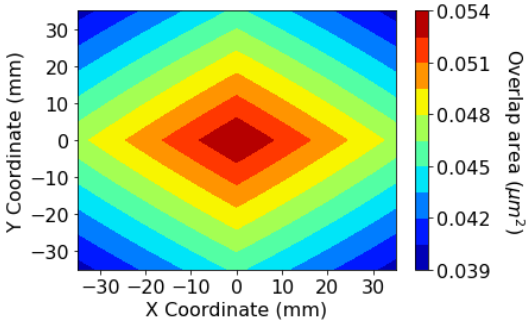
This one-dimensional principle holds for both the junction fingers, thus we can expand it to a two-dimensional model and calculate the difference in width for both the top and bottom electrode. This allows us to study the variations in the overlap area of the top and bottom electrode, which is an important parameter that influences the conductance of the Josephson junction. The expression for the overlap area, $A_{overlap}$, is found by simply taking equation (5.1) for both the x- and y-direction. Thus we obtain:

$$A_{overlap} = \left(W_B - H\frac{|x|}{D}\right)\left(W_T - H\frac{|y|}{D}\right) \tag{5.2}$$

Here it is important to note that the top and bottom electrode do not have the same width, therefore W_B represents the width of the bottom electrode and W_T the width of the top electrode. The overlap area as a function of the x- and y-coordinate can be plotted, as seen in in figure 5.3a.



(a) Overlap area as a function of the X and Y coordinate without the inclusion of any effects.



(b) Overlap area as a function of the X and Y coordinate with the inclusion of sidewall contributions.

Figure 5.3: Schematic representation of the two dimensional model. Figure 5.3a is based on the overlap of the top and bottom electrode, according to equation 5.2. Figure 5.3b is based on the overlap area of the top and bottom electrode and adds an extra contributions due to the overlap area, according to equation 5.3. The contributions of the sidewalls result in an elongated effect along the X axis. The designed width for the top and bottom electrode is 200 nm.

From this we find that the overlap area is the largest at the center of the wafer and decreases towards the edges. This current model only takes the overlap area into account, which is defined by the width of both the

electrodes. However, there is another contribution to the overlap area of both electrodes. The sidewalls of the bottom electrode will also form a tunnel barrier with the top electrode and should therefore also be taken into account. This contribution to the tunnel barrier can be calculated by multiply the thickness of the bottom electrode T_B by the width of the top electrode W_T. Thus the area of the sidewalls $A_{sidewall}$ is expressed as:

$$A_{sidewall} = 2T_B W_T \tag{5.3}$$

here a factor of 2 is added to account for the fact that there are two sidewalls, one on each side of the junction. One could argue that the bottom electrode will act as a shadow during the top electrode deposition, resulting in only one sidewall. This shadowing effect would cause a variation of approximately $(35 \tan(55) \approx)$ 50 nm. However, from SEM images, such as figure 5.4, this was not observed and thus the factor of 2 is applied for the model.

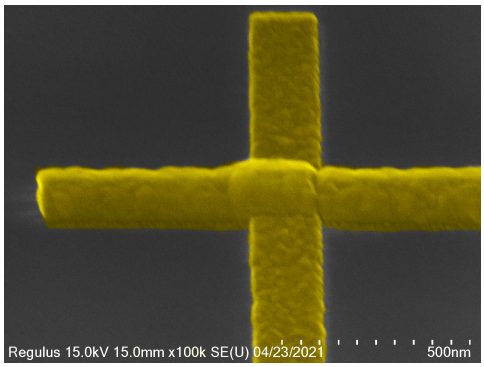


Figure 5.4: False colored SEM image of a Josephson junction at a 45° tilt. The yellow corresponds to the Al junction and the blue corresponds to the surrounding Si.

By summing the overlap area and the sidewall area we get the total area of the tunnel barrier, $A_{total} = A_{overlap} + A_{sidewall}$. The total area is plotted in figure 5.3b, this figure shows that the addition of the sidewall result in an elongated effect along the x-axis. This can be explained by the fact that the width of the top electrode decreases along the y-axis, thus the contributions of the sidewall become less apparent. This model can be expanded further by taking into account that the thickness of the bottom electrode depends on the incident angle of the deposited material. The relation between the thicknesses can be express as

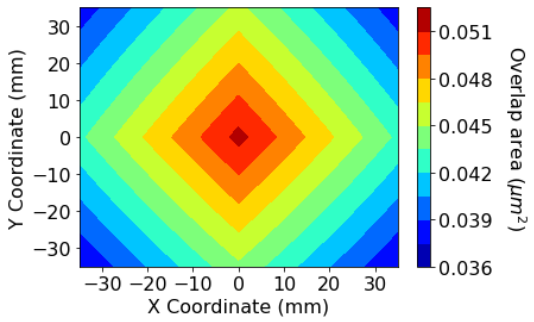
$$T_{real} = T_{design} \sin(\theta) \tag{5.4}$$

where T_{real} is the thickness of the deposited material, T_{design} is the thickness of the material during perpendicular incidence. From this we find that the thicknesses are equal to each other when $\theta = 90°$, which makes sense. Figure 5.5a shows the model when this effect is incorporated. The final addition to the model is the inclusion of the metal deposited on the resist sidewall, described earlier by Zhang et al. [80]. During the deposition of the bottom electrode, metal is deposited on the side of the resist of the opening for the top electrode. This metal will cause the width of the opening to decrease, thus decreasing the width of the top electrode. The result of this simulation can be seen in figure 5.5b.

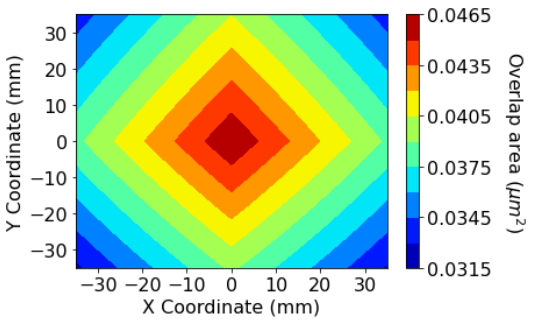
Table 5.1: Parameters used for the model.

Variable	Symbol	Value
Top resist height	H	600 nm
Thickness bottom electrode	T_B	35 nm
Thickness to electrode	T_T	75 nm
Width bottom electrode	W_B	100 nm
Width top electrode	W_T	160 nm
Tilt	θ	35°

This model is applied on the layout used for the production of superconducting quantum processors used in the lab as seen in figure 5.6. This layout consists of 20 Surface-17 devices.



(a) Graphical representation of the model with angle dependent thickness.



(b) Graphical representation of the model with angle dependent thickness and material deposited on the resist sidewall.

Figure 5.5: Schematic representation of the two dimensional view of the model.

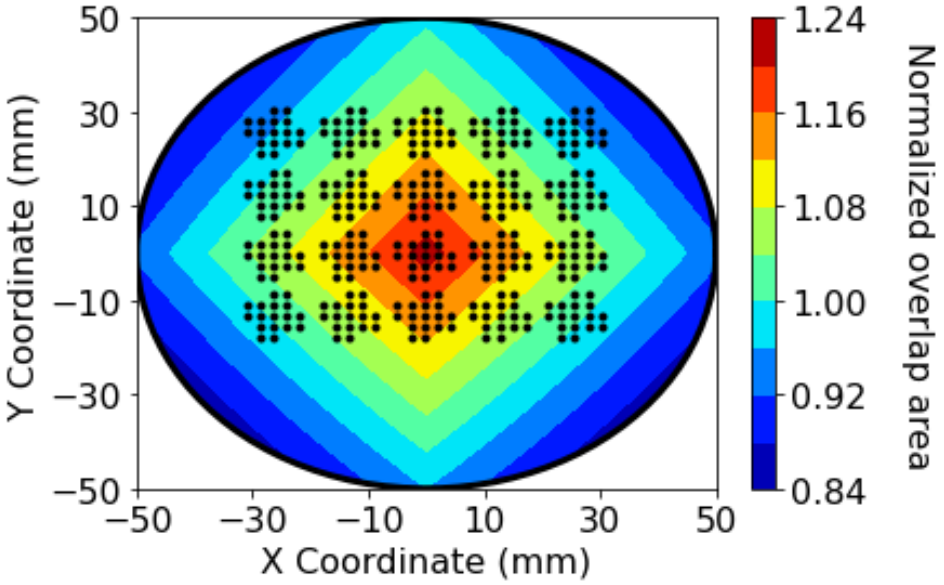


Figure 5.6: Overlap area as a function of the X and Y coordinate applied on a 100 mm wafer for the production of superconducting quantum processors.

Finally the coefficient of variation can be calculated with the model and be compared with the half wafer depositions. The CV as a function of the junction overlap area can be seen in figure 5.7. From this we see that the model shows poor correspondence to the acquired data for the Manhattan style junctions. An explanation could be the low sampling rate used to determine the CV from the data in combination with the spacing of the data points.

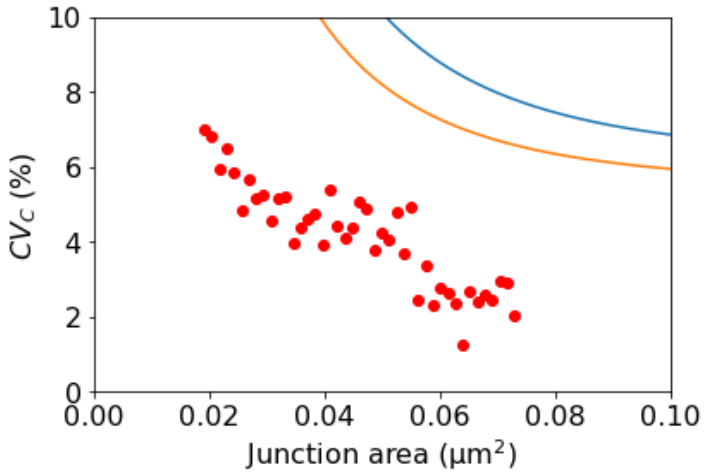
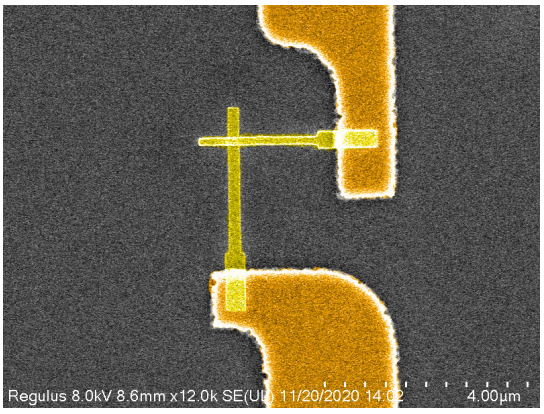


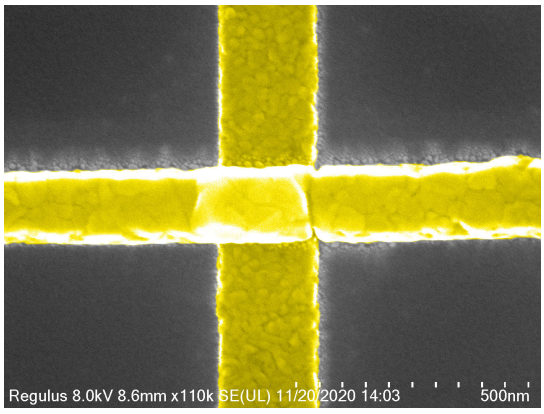
Figure 5.7: Coefficient of variation of Manhattan style junctions as a function of junction overlap area.

5.2. SEM Analysis

An SEM analysis is performed to related the electrodes widths and overlap area to the model. For this analysis the Manhattan style junctions on the half-wafer described in chapter 3 are used. For this analysis, three SQUID loops on each die on the half-wafer are imaged, these three SQUID loops correspond to a low, middle and high frequency range. The positions on the wafer can be seen in figure 3.8. From the SEM images the overlap area of the Josephson junction can be extracted using the software ProSEM.
Figure 5.8 shows SEM images of Manhattan style Josephson junction, used to extract the overlap area. Figure 5.8a shows the position of the junction with respect to the NbTiN bay and how it is connected to it and figure 5.8b is a zoom in of the same junction around the overlap area.



(a) False colored SEM image of a Manhattan style Josephson junction and the surrounding NbTiN bay at a 12k magnification.



(b) False colored SEM image of the overlap area of a Manhattan style Josephson junction at a 110k magnification.

Figure 5.8: Scanning electron micrographs of a Manhattan style Josephson junction around the NbTiN bay (5.8a) and a close up on the overlap area of which the width of the top and bottom electrode can be extracted (5.8b)

By measuring the width of the top and bottom electrode of the junction it is possible to determine the dependence on the X and Y coordinate. The model predicts that the width of the bottom electrode depends on the the X-coordinate, thus the width of the bottom electrode as a function of the X-coordinate are plotted in figure 5.9. In this figure the data is fitted according to equation (5.1), the first number in the fit represents the predicted width W and the second number represents the factor H/D. The designed width of the bottom electrodes are 84, 136 and 192 nm for the low, middle and high frequency junctions respectively. When the designed and predicted width are compared to each other we find that the fit overestimates the width of the bottom electrode. The predicted ratio of H/D is smaller than the designed value of $H/D(= 600/650) = 0.923\,\mathrm{nm/mm}$.
Using the width of the top electrode it is possible to study it's dependence as a function of the X-coordinate.

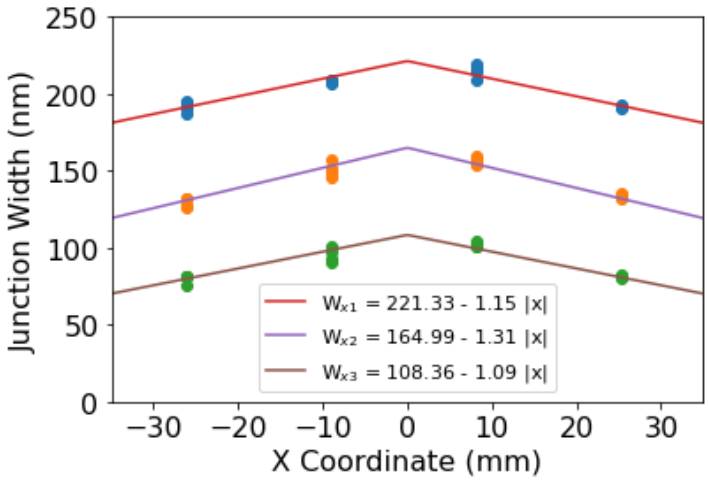
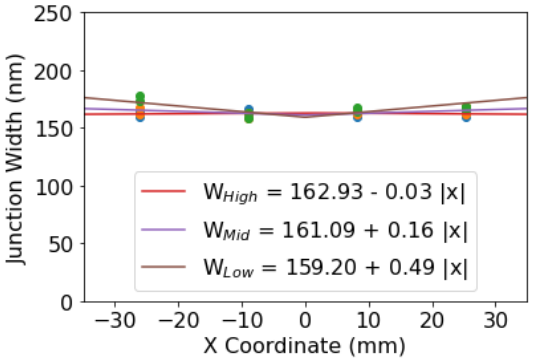
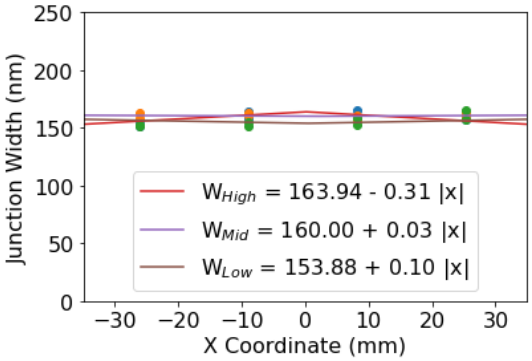


Figure 5.9: Measured junction width of the bottom electrode of the center dies as a function of the X-coordinate.

The model predicts that the width of this electrode should not depend on the X coordinate. The width of the top electrode as a function of the X-coordinate is plotted in figure 5.10. In this case, we find that the predicted width from the model corresponds well to the designed width of 160 nm for almost all fit lines. Furthermore, the coefficient before the $|x|$ should be zero, since there should be no dependence on the x-axis. While this coefficient is indeed small, it is still present. This indicates that there might be another effect which is not considered in this model.



(a) Measured junction width of the top electrode of the center dies as a function of the X-coordinate.



(b) Measured junction width of the top electrode of the edge dies as a function of the X-coordinate.

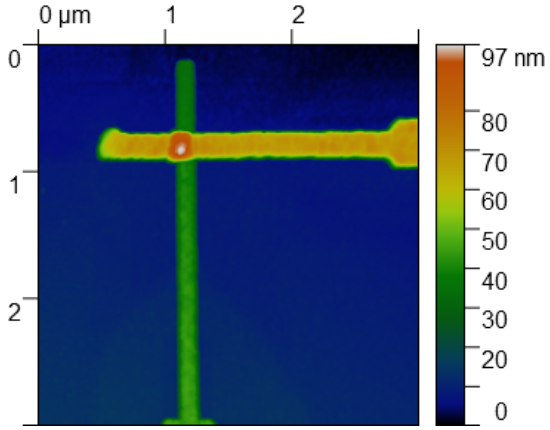
Figure 5.10: Comparison of the variations in center and edge dies. The data is fitted according to equation (5.1). W_{High} shows the data for the junction corresponding to a high frequency, W_{Middle} shows the data for the junction corresponding to a middle frequency and W_{Low} shows the data for the junction corresponding to a low frequency.

The SEM analysis shows that for the top electrode the data and the geometric model shows correspondence with each other. The fits through the data show that the slope is close to zero and that the offset is close to 160 nm, which is as expected. For the bottom electrode the data and the geometric model show poor correspondence, as the fits through the data give a large offset than the designed junction width and the slope is also larger than the predicted value of 0.93 nm/mm.
Besides determining the coefficient of variation for the junctions fabricated on a NbTiN base layer, the model can also be used to determine the correspondence to the all aluminum junctions. For a top and bottom electrode with a 200 µm width the model predicts a CV of 6.40% if the tilt is taken into account and a CV of 6.83% if the metal that is deposited on the sidewall is taken into account. This value is in correspondence with the CV's of the all aluminum wafers, where the lowest reported CV is 7.1%.

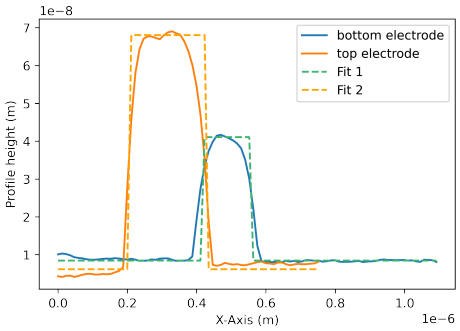
5.3. AFM Analysis

To study the variations in the thickness of the electrodes an atomic force microscope (AFM) analysis is performed. The variations in the thickness are introduced by the tilt of the substrate during the electrode deposition. For this analysis the Manhattan style junctions on the half-wafer from chapter 3 are used.

From each die on the half wafer a Josephson junction is used for the AFM analysis. The positions of each die on the half-wafer can be seen in figure .... The dies are labeled with a number, representing the position from left to right, and a c or e, which stands for center or edge. An AFM measurement can be seen in figure 5.11a, it is clear that there are two electrodes which both have a different thickness. As expected the overlap between both electrodes shows an increase in the height. A single line can be drawn across an electrode to accurately measure the height profile as seen in figure 5.11b. In this figure the data for both electrodes are taken into account, together with the fit used to determine the electrode height. These measurements are taken for a single Josephson junction on each die on the half wafer. The results of these measurements can be seen in table 5.2.



(a) Graphical representation of the area scanned during an AFM measurement to determine the junction thickness.



(b) One dimensional plot of the electrode thickness as a function of the scan length.

Figure 5.11: Overview of the method used to extract the thickness of the junction electrodes using an AFM measurement.

The geometric model predict that the height of the bottom electrode should change along the Y axis from from top to bottom. Electrodes at the top of the wafer should be thicker than electrodes at the bottom of the wafer. Since the Josephson junctions are only fabricated on a half wafer there is not enough data to study this effect and is therefore not discussed. For the top electrode the model predicts variations along the X axis, from left to right. In this case electrodes at the left of the wafer should be thicker than electrodes on the right. Specifically across a line of 70 mm across the wafer there should be a change in the angle of incidence between 57.6° and 52.5° for a tilt of 35°. These incident angle variations give a height difference between 63.3 nm and 59.5 nm if the deposited thickness under perpendicular incidence is 75 nm. In the case of the AFM measurements the distance is 52 mm, resulting in a thickness between 62.8 nm and 60 nm.

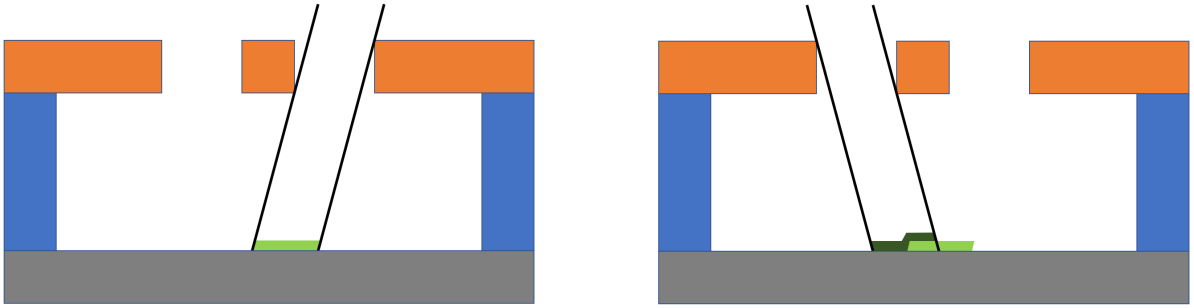
To summarize, the model and measurement data correspond with each other, in both cases a decrease in top electrode thickness is observed from left to right. The measurement data does show larger variations than predicted by the model. In order to further study these variations AFM measurements over a longer distance are required. From these measurements are expected to show larger variations in the electrode thickness, as predicted by the model. Finally the thickness of the bottom electrode does not show significant variations, which is in line with the model.

Table 5.2: Height of the top and bottom electrode for different positions on a wafer.

Die Position	1c	2c	3c	4c	1e	2e	3e	4e
Top contact thickness (nm)	65 ± 1	62 ± 2	62 ± 1	61 ± 1	66 ± 1	64 ± 1	63 ± 1	60 ± 1
Bottom contact thickness (nm)	32 ± 1	30 ± 1	33 ± 1	32 ± 1	33 ± 1	31 ± 1	31 ± 1	31 ± 1

5.4. Dolan Bridge Junctions

The variations in Dolan bridge junctions are significantly less than the variations in Manhattan junction, however it would still be worthwhile to determine if it is possible to create a model that captures the variations in the Dolan bridge style junctions. In the case of Dolan bridge junctions, the overlap area can be calculated by determining how much material is deposited under the Dolan bridge for the bottom electrode, according to: $L_{bottom} = H_{bottom} \sin(\theta_1)$, where L_{bottom} is the length under the bridge, H_{bottom} is the height of the bottom resist stack and θ_1 is the angle under which the material is deposited. The same holds for the deposition of the top electrode, but now the thickness of the bottom electrode needs to be taken into account. Thus the equation becomes $L_{top} = (H_{bottom} - T_{bottom}) \sin(\theta_2)$, where T_{bottom} is the thickness of the bottom electrode and θ_2 is the angle under which the material is deposited. The resist thickness is the highest at the center of the wafer and the lowest at the edges, therefore the thickness H_{bottom} is calculated as: $H_{bottom} = H_{center} - (H_{center} - H_{edge}) \cos(\varphi)$, where H_{center} is the resist height at the center, H_{edge} is the resist height at the edge and φ changes from 0 at the center to 0.5π at the edge. Figure 5.12 shows a schematic representation of the overlap area for a Dolan bridge junction.



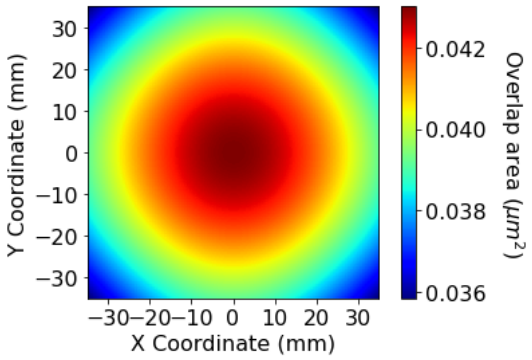
(a) Schematic representation of the first deposition for the fabrication of Dolan bridge junctions.

(b) Schematic representation of the first deposition for the fabrication of Dolan bridge junctions.

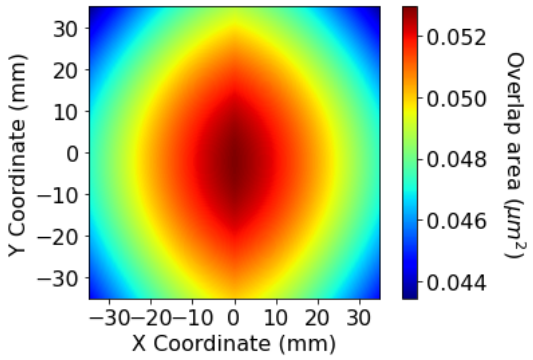
Figure 5.12: Schematic representation of the deposition for Dolan bridge junctions. The black lines represent the direction of the deposited metal. The colors corresponds to: (dark)Green - Al, Orange - PMMA, Blue - PMGI, Grey - Si. The light green corresponds to the first Al deposition and the dark green to the second Al deposition.

The fabricated Dolan bridge junctions were produced on a 200 nm base layer of NbTiN, this means that the Dolan bridge is actually 200 nm higher than when only a bilayer resist stack is used. For the previously described equations this 200 nm can simply be added to the height of the bottom resist H_{bottom}, where the height of the NbTiN base layer also gradually decreases towards the edge of the substrate. This is modelled in the same way as for the resist. The overlap area of the Dolan bridge junction can be calculated according to $A_{top} = (L_{bottom} + L_{top} - L_{Dolan}) W_{top}$, where A_{top} is the overlap area on the top, L_{Dolan} is the length of the Dolan bridge and W_{top} is the width of the top electrode.
Besides the overlap area on the top, the overlap area of the sidewall should also be taken into account. This contribution can be calculated according to $A_{side} = T_{bottom} W_{top}$. Finally the entire overlap area of the Dolan bridge junction is the sum of these two contributions $A_{total} = A_{top} + A_{side}$. Using these simple equations a plot of the overlap area as a function of the position on the wafer can be created, similar to the ones created for Manhattan style junctions. The model is represented in figure 5.13.

To expand this model, the tilt of the wafer, the real thickness of the bottom electrode and the variations in the width W_{top} are taken into account. The tilt plays a role since the it will affect the angle θ under which the material is deposited during both deposition rounds and it will affect the thickness of the bottom electrode, since the incident angle changes throughout the wafer. We find that the angle θ varies between 71° and 79° across the wafer, which is a 4° degree variation in both direction from the 75° angle at the center. This variation in



(a) Overlap area as a function of the X and Y coordinate for Dolan bridge Josephson junctions. This model is based on the variation in the resist height across the wafer.



(b) Overlap area as a function of the X and Y coordinate for the Dolan bridge Josepshon junction. The variations due due to the tilt and shadowing are taken into account.

Figure 5.13: Graphical representation of the model used to determine to overlap area between the top and bottom electrode for the Dolan bridge Josephson junction. Figure 5.13a shows that if only the variation in resist height are taken into account the overlap area becomes radial dependent. If other contributions are taken into account such as the tilt, thickness variations and width variations a elliptic pattern appears.

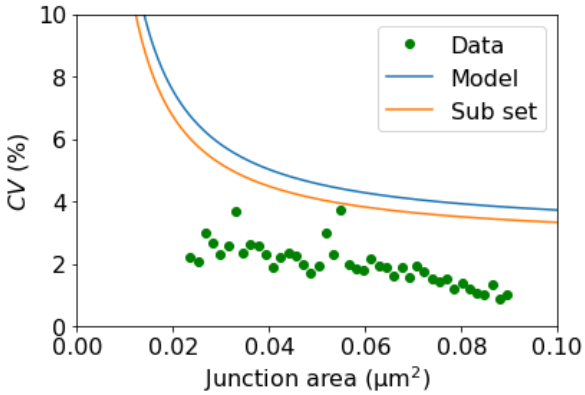


Figure 5.14: Coefficient of variation as a function of the overlap area for the Dolan bridge Josephson junctions. The experimental data is plotted

angle results in a variation in the thickness of the bottom electrode from 34.4 nm to 33.1 nm. Similar to the model for the Manhattan style junctions the effect of the top resist layer on the electrode width is taken into account. For the Dolan bridge junctions the bottom electrode is much wider than the top electrode, therefore this effect is only relevant for the top electrode.
From the model, the coefficient of variation for different junction width can be determined, as seen in figure 5.14. This figure shows that the CV is the largest for small overlap areas. This can be explained by the variations in the junction width due to the shadowing of the top resist layer. This effect will be more dominant for small electrodes than for larger junctions. As the overlap area increases this effect becomes less dominant and the CV decreases. The most important result is that the model overestimates the CV for all overlap areas. However, the over estimation can be reduced by taking the sample size into account. The CV of the model is based on a square of 70 mm by 70 mm, as seen in figure 5.13. In this case a large area is taken into account, which will result in a larger CV. It is also possible to take a subset from the modeled data taking only the area of the dies into account. From this the CV can also be determined as seen in the figure. While the data from the sub set still over estimates the CV, it is reduced. The CV from the subset data could probably be further reduced by taking the exact position and number of the datapoints into account.

6

Conclusion and Outlook

This chapter will summarize the results of this thesis. To conclude this chapter will give an outlook to relevant work for the future.

6.1. Conclusion

The objective of this thesis was to improve the yield of Josephson junction in the wafer-scale fabrication of superconducting quantum processors. To achieve this, the variation in the Josephson junction conductance across a 100 mm Si wafer is investigated for two types of Josephson junctions, the Dolan bridge junction and the Manhattan style junction.

First the performance of both junction types on a planar NbTiN base is studied by using different overlap areas in a Surface-17 configuration. From this we find that the fabrication yield of Dolan bridge junctions is higher, while also having a lower coefficient of variation than the Manhattan style junctions. The problem with Dolan bridge junctions is that these are not compatible with trough silicon vias used for superconducting qubits as these TSV affect the spinning of the resist. Manhattan style junctions are compatible with TSV and thus the field is converging to this junction type. In this work the Manhattan style Josephson junction is investigated further for the same reason.

The influence of the resist ashing is investigated using Manhattan style Josephson junctions that are fabricated on a base Si wafer using Al for the junction and the measurement pad. From these tests we conclude that the ashing decreases the coefficient of variation from 14.26% to 8.73% from across a 100 mm wafer and thus improves the uniformity across the wafer. Using the same procedure the highest uniformity is reported, with a CV of 7.10%. Since the ashing is an important parameter to fabricate junction uniformly across a 100 mm wafer additional tests are performed in order to improve the uniformity even further by rotating the sample in between ashing steps and using a different plasma system. However these additional tests did not yield an improvement in the CV.

Manhattan style junctions are fabricated on 100 mm Si wafer with a planar NbTiN base. This wafer shows an increase in the coefficient of variation in comparison to the all aluminum Manhattan style Josephson junction fabricated on a bare Si wafer. The coefficient of variation increases by 10.60%, which indicates that the NbTiN base layer plays a role to uniformly fabricated Josephson junctions as the best aluminum wafer had a CV of 7.10%.

Dolan bridge and Manhattan style Josephson junctions are fabricated on a non-planar NbTiN base layer on a 13x13 sample. The coefficient of variation as a function of the overlap area is calculated for both types. We find that the coefficient increases significantly for both junction types. While in both cases there are larger variations, the Manhattan style junctions perform better than the Dolan bridge junctions.

We propose a geometric model to explain the variations in Manhattan style Josephson junctions across a 100 mm wafer based on the shadowing of the top resist layer during junction deposition. This model over

predicts the coefficient of variation when compared to the data from Chapter 3. This over estimation is attributed to the sparseness of the data in this set. For Josephson junctions with a overlap area of 0.04 μm^2 the model predicts a CV of 6.7%, which is slightly lower than the CV for the best wafer with all aluminum junctions, which is 7.10%. This is logical as the model assumes an ideal situation, i.e. no fabrication errors, and should thus give a lower bound on the CV. For the Manhattan style junctions fabricated on a NbTiN base layer a CV of 10.60% is found, which is higher than what the model predicts. This could indicate that the NbTiN base layer plays a role in the fabrication of the Josephson junctions that is currently not included in the model.

6.2. Outlook

There are a few things that would be interesting to be investigated further.

It would be interesting to make a comparison of Dolan bridge and Manhattan style Josephson junctions on different base layers. In this case, a base Si, a planar NbTiN and a non-planar NbTiN base layer could be compared. By using different junction overlap areas across the sample it would be possible to determine the coefficient of variation as a function of the overlap area for different base layers. This can be used to compare the geometric model for both junction types and study the influence of the base layer.

In order to improve the performance of superconducting quantum processors the variations across a 100 mm wafer need to be reduced. Further tests could explore the cause of these variations and possibly give a solution. It would be interesting to see the performance of the Josephson junctions when the ashing is performed using an optimized isotropic etch. Another option would be to study the effect of the deposition machine and determine if the recipe can be optimized. The junctions can also be fabricated using a different deposition machine to determine the impact it has. These tests can be conducted using all aluminum junctions on a Si wafer and then be expanded to a planar and non-planar NbTiN base layer.

A

Filtering of data

In this appendix the raw data and the filtered data from the conductance measurements from chapter 3 are represented. First all data points with a conductance above 500 µS and below 20 µS are removed, since these points correspond to shorted or open Josephson junctions. The Josephson junctions are positioned in a SQUID loop, therefore it is possible that one Josephson junction operates properly while another is open. These half open junctions are removed by using a linear fit through the raw data, without the open en shored junctions. If a data points is smaller than $fit \cdot 0.7$ or larger than $fit/0.7$, the point is removed. This allows for the removal of half open junctions and outliers with a high conductance. In the figures A.1 A.2 A.3 the raw data of each measurement can be seen on the left, the filtered data is represented in the middle and the left shows the number of points removed, which electrode width it corresponded to and if the removed point was an open, shorted or half open junction.

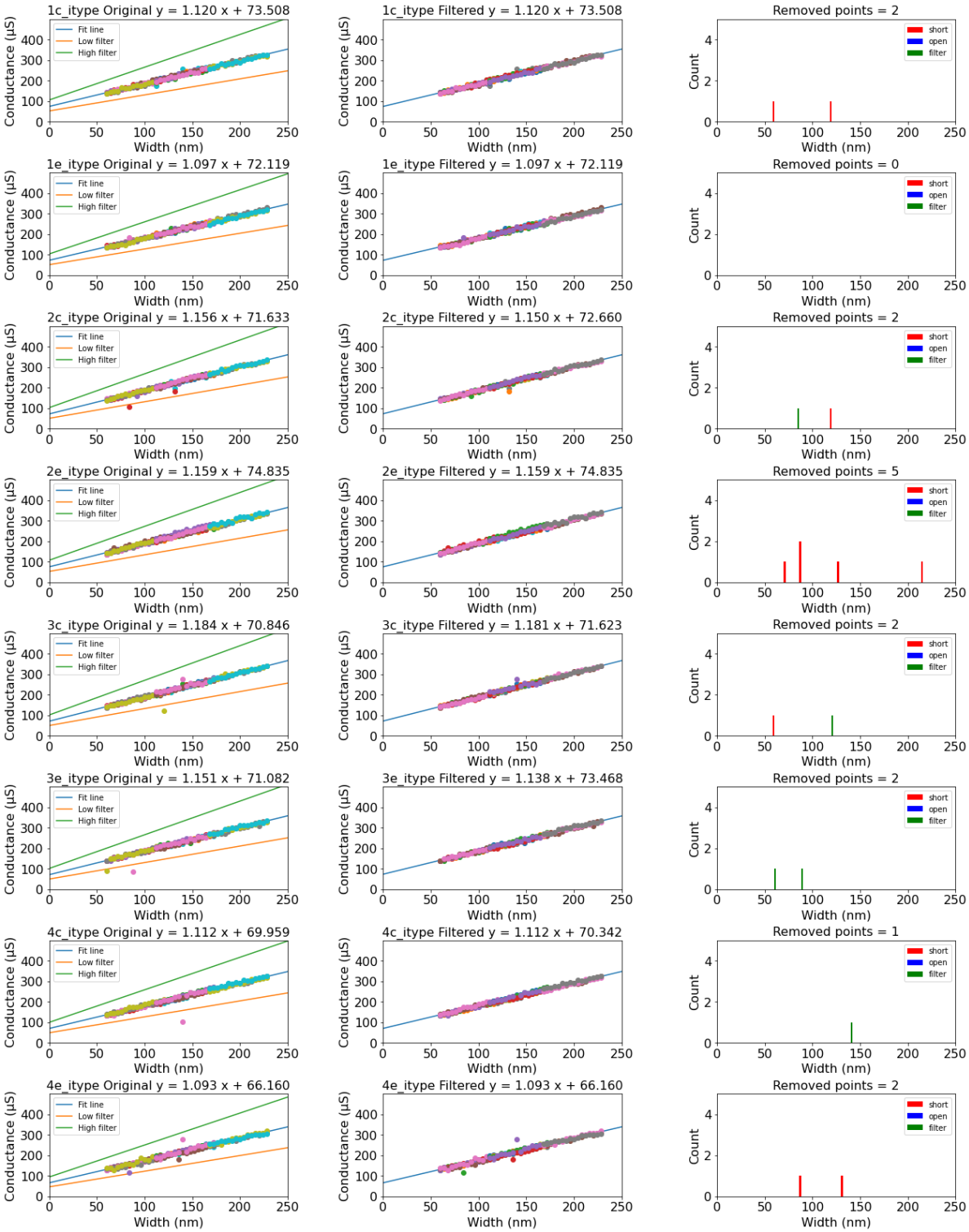


Figure A.1: Filtering of the data from Blackbird 2 Dolan bridge Style. The left column corresponds to the original data, with a fit through this data. The fit line is used to filter outliers, the middle columns shows the images after filtering. The right column shows the number of points filtered for a certain junction width, it also shows if the filtered points where open, short or half-open.

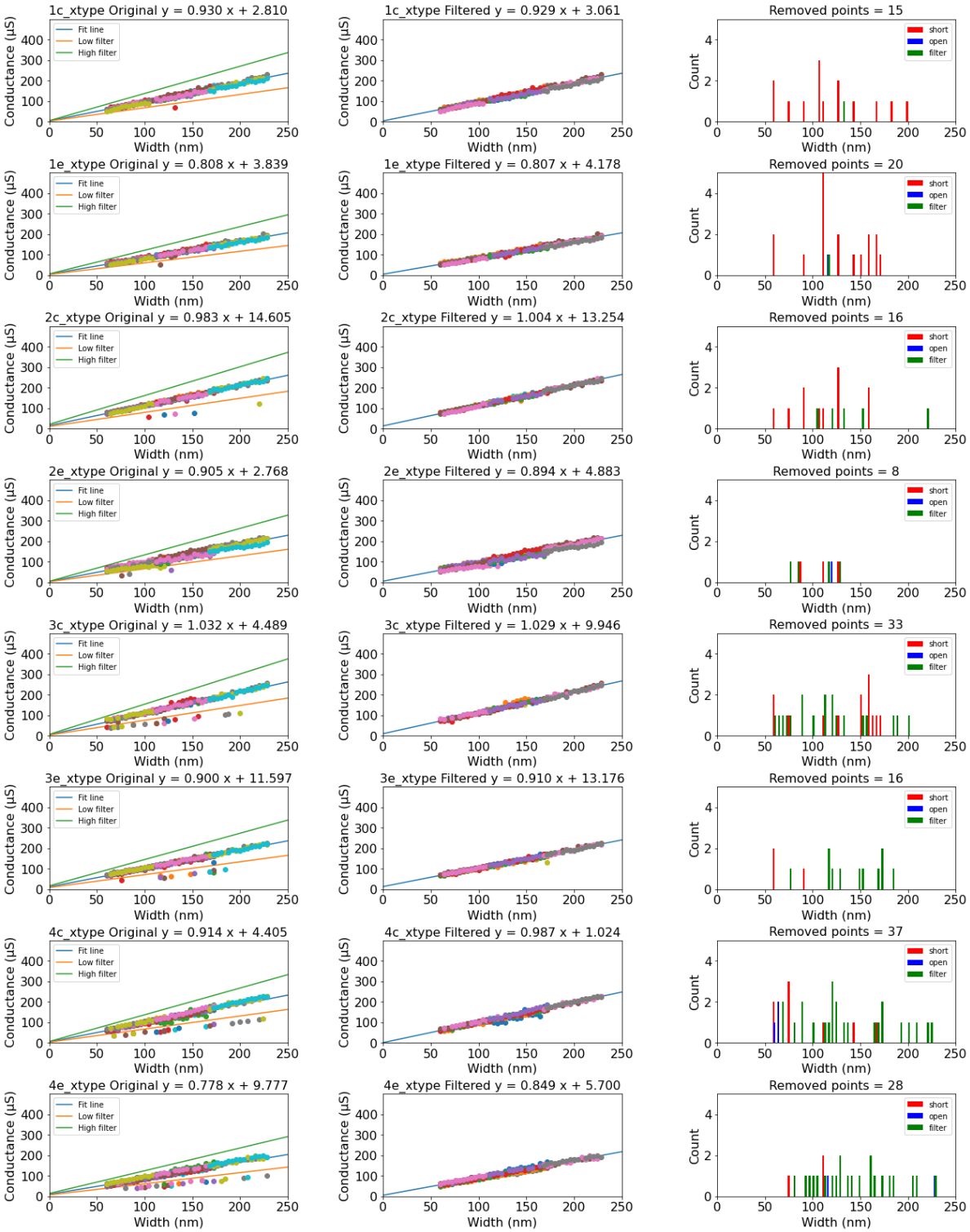


Figure A.2: Filtering of the data from Blackbird 2 Manhattan Style. The left column corresponds to the original data, with a fit through this data. The fit line is used to filter outliers, the middle columns shows the images after filtering. The right column shows the number of points filtered for a certain junction width, it also shows if the filtered points where open, short or half-open.

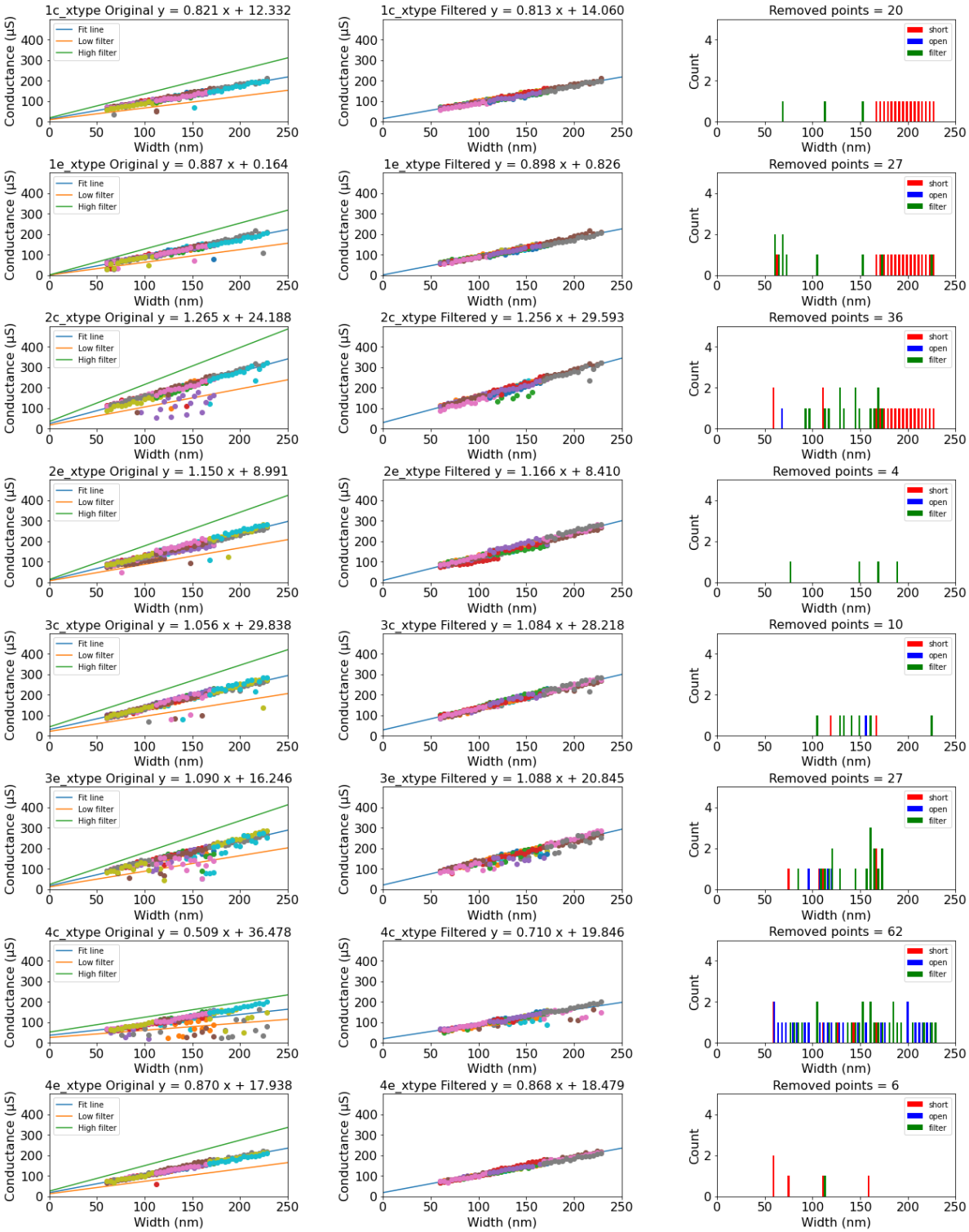


Figure A.3: Filtering of the data from Blackbird 1 Manhattan Style. The left column corresponds to the original data, with a fit through this data. The fit line is used to filter outliers, the middle columns shows the images after filtering. The right column shows the number of points filtered for a certain junction width, it also shows if the filtered points where open, short or half-open.

B

Fabrication Recipe: Junctions on NbTiN

In this appendix the recipe used for the fabrication of the Josephson junction test pads is described. Note that the fabrication of the junction test pads, although very similar, is different from the fabrication recipe for the actual superconducting quantum devices. The fabrication recipe uses a single side polished, high resistivity, 100 mm Si wafer with a thickness of 525 µm. The fabrication is separated into three steps: the substrate preparation, base patterning and junction deposition.

B.1. Substrate preparation

- UV ozone clean to remove organic contaminants
- Clean wafer with acetone and IPA
- Remove native oxides by immersing the wafer in a 1:1 mixture of HF:H_2O for 2 min.
- Create a capping layer to retard oxide formation using vapor priming with hexamethyldisilazane (HMDS) at 150 °C.
- Deposit 200 nm NbTiN using a super AJA with reactive magnetron sputtering in the presence of an RF field and nitrogen, using a target consisting of 59% Nb and 39% Ti. This film has a thickness of 200 nm, a critical temperature, T_c of 13 K to 14 K, a resistivity of 85 µΩ cm to 105 µΩ cm and a sheet resistance of 0.9 Ω/sq to 1 Ω/sq.

B.2. Base Patterning

- Deposite 100 nm Si_3N_4 using a Alliance Concept 450. This layer will act as a sacrificial inorganic mask during the etching process. This layer is deposited by RF magnetron sputter deposition with a 600 W Huttinger RF source.
- Spin ARP.6200-18 (CSAR) at 1500 rpm and bake for 3 min at 150 °C to create a resist layer of 1.3 µm.
- Exposure with a Raith EBPG5000+ or EBPG5200 with a bundle with a spot size of 45 nm and a step size of 35 nm. The bundle uses a dose of 365 µC/cm^2 and an accelerator voltage of 100 kV.
- Develop the sample by immersing it in pentyl acetate for 60 s. Then rinse the sample with IPA and dry with N2.
- Dry etch the wafer with a SF_6 plasma using a Sentech Etchlab 200. This system is only used for SF_6 and O_2 processes. The wafer is etched at a flow of 14 SCCM of SF_6 and a flow of4 SCCM of O_2.
- Remove the CSAR using NMP at 88 °C
- Clean wafer with acetone and IPA
- Wet etch using 1:1:5 mixture of hydroperoxide:ammonia:water (RCA-1) at a temperature of 32 °C.
- Remove Si_3N_4 using a 1:1 mixture of HF:H_2O

B.3. Josephson Junction

The procedure for the Dolan style and the Manhattan style Josephson junctions are different, therefore they are split into two. Some steps of the process are the same, the most important differences are the used resist stack and the angles used during junction deposition.

B.3.1. Dolan Bridge

- Spin bilayer resist stack
  PMGI SF7 at 2000 rpm, bake for 5 min at 180 °C to create a resist layer with a thickness of 400 nm.
  Spin 950 PMMA A3 at 2000 rpm, bake for 5 min at 180 °C to create a resist layer with a thickness of 150 nm.

- Exposure with a Raith EBPG5000+ or EBPG5200 with a bundle with a spot size of 18 nm and a step size of 4 nm. The bundle uses a dose of 1850 $\mu C/cm^2$ and an accelerator voltage of 100 kV.

- Development
  Develop in MIBK:IPA, 1:3, for 1 min
  Stop development in acetone:IPA, 1:3, for 20 s
  Stop development in IPA, for 20 s
  Dip in H_2O to make the wafer hydrophilic
  Development in MF321, for 20 s
  Stop development in H_2O, for 20 s

- Remove resist residuals with an O_2 plasma using a Sentech Etchlab 200. The system is operated at an RF power of 20 W, RF bias of 120 W, a reflected power below 1.5, for 45 s.

- Remove oxides introduced during ashing with a mixture of BOE 7:1, diluted 1:1 with H_2O for 30 s.

- Junction deposition using a Plassys MEB550S2
  Wait for the chamber pressure to reach a pressure below 10^{-8} mbar.
  Deposit 20 nm of Ti in the chamber as a getter material.
  Tilt the sample 15° and deposit 35 nm of Al.
  Oxidize the Al with O_2 for 11 min at a pressure of 1.3 mbar.
  Wait for the chamber pressure to reach a pressure below 10^{-8} mbar.
  Rotate the sample 90° and tilt it 15° and deposit 75 nm of Al.
  Oxidize the Al with O_2 for 11 min at a pressure of 1.3 mbar.

- Lift-off the Al in NMP at 88 °C.

B.3.2. Manhattan Style

- Spin bilayer resist stack
  PMGI SF7 diluted 1:1 with cyclopentane at 1500 rpm, bake for 3 min at 180 °C to create a resist layer with a thickness of 200 nm.
  Spin 950 PMMA A6 at 1500 rpm, bake for 5 min at 180 °C to create a resist layer with a thickness of 600 nm.

- Exposure with a Raith EBPG5000+ or EBPG5200 with a bundle with a spot size of 18 nm and a step size of 4 nm. The bundle uses a dose of 1850 $\mu C/cm^2$ and an accelerator voltage of 100 kV.

- Development
  Develop in MIBK:IPA, 1:3, for 1 min.
  Stop development in acetone:IPA, 1:3, for 20 s.
  Stop development in IPA, for 20 s.
  Dip in H_2O to make the wafer hydrophilic.
  Development in MF321, for 20 s.
  Stop development in H_2O, for 20 s

- Remove resist residuals with an O_2 plasma using a Sentech Etchlab 200. The system is operated at an RF power of 20 W, RF bias of 120 W, a reflected power below 1.5, for 45 s.

- Remove oxides introduced during ashing with a mixture of BOE 7:1, diluted 1:1 with H_2O for 30 s.
- Junction deposition using a Plassys MEB550S2
  Wait for the chamber pressure to reach a pressure below 10^{-8} mbar.
  Deposit 20 nm of Ti in the chamber as a getter material.
  Tilt the sample 35° and deposit 35 nm of Al.
  Oxidize the Al with O_2 for 11 min at a pressure of 1.3 mbar.
  Wait for the chamber pressure to reach a pressure below 10^{-8} mbar.
  Rotate the sample 90° and tilt it 35° and deposit 75 nm of Al.
  Oxidize the Al with O_2 for 11 min at a pressure of 1.3 mbar.
- Lift-off the Al in NMP at 88 °C.

C

Fabrication Recipe: All Aluminum Junctions

In this appendix the fabrication of all aluminum Josephon junction is described. For the all aluminum junctions only the Manhattan layout is used. The fabrication procedure is similar to that of the junction on a NbTiN base. However, the all aluminum junctions recipe is shorter, due to the absence of NbTiN. For the fabrication of all aliuminum junctions a single side polished, high resistivity, <100> Si wafer is used.

- Clean wafer with acetone and IPA
- Spin bilayer resist stack
  PMGI SF7 diluted 1:1 with cyclopentane at 1500 rpm, bake for 3 min at 180 °C to create a resist layer with a thickness of 200 nm.
  Spin 950 PMMA A6 at 1500 rpm, bake for 5 min at 180 °C to create a resist layer with a thickness of 600 nm.
- Exposure with a Raith EBPG5000+ or EBPG5200 with a bundle with a spot size of 154 nm and a step size of 100 nm for the pads. The bundle uses a dose of 1850 $\mu C/cm^2$ and an accelerator voltage of 100 kV.
  For the Josephson junctions a bundle with a spot size of 28 nm and a step size of 20 nm is used. The bundle uses a dose of 1850 $\mu C/cm^2$ and an accelerator voltage of 100 kV.
- Development
  Develop in MIBK:IPA, 1:3, for 1 min
  Stop development in acetone:IPA, 1:3, for 20 s
  Stop development in IPA, for 20 s
  Dip in H_2O to make the wafer hydrophilic
  Development in MF321, for 20 s
  Stop development in H_2O, for 20 s

After the development the variations are introduced in the recipe. For the sake of illustration the normal recipe is described her further. Alterations in the recipe are described in Chapter 4.

- Remove resist residuals with an O_2 plasma using a Sentech Etchlab 200. The system is operated at an RF power of 20 W, RF bias of 120 W, a reflected power below 1.5, for 45 s.
- Remove oxides introduced during ashing with a mixture of BOE 7:1, diluted 1:1 with H_2O for 30 s
- Junction deposition using a Plassys MEB550S2
  Wait for the chamber pressure to reach a pressure below 10^{-8} mbar.
  Deposit 20 nm of Ti in the chamber as a getter material.
  Tilt the sample 35° and deposit 35 nm of Al.
  Oxidize the Al with O_2 for 11 min at a pressure of 1.3 mbar.
  Wait for the chamber pressure to reach a pressure below 10^{-8} mbar.
  Rotate the sample 90° and tilt it 35° and deposit 75 nm of Al.
  Oxidize the Al with O_2 for 11 min at a pressure of 1.3 mbar.

- Lift-off the Al in NMP at 88 °C.

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