A Dynamic Zoom ADC for Instrumentation Applications

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Challenge the future

A Dynamic Zoom ADC for Instrumentation Applications

by

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Abstract

Analog to digital converters (ADCs) are critical blocks in most signal processing chains. Especially in low bandwidth applications, there exists a need to digitize signals with high resolution and accuracy, while at the same time, expending minimum energy.

This thesis presents a dynamic zoom ADC for use in such applications. The zoom ADC employs a high-speed asynchronous SAR ADC which works in tandem with a fully-differential $\Delta\Sigma$ ADC. Fabricated in a 0.16-µm CMOS process, the prototype occupies 0.26 mm^2 and achieves 119.1 dB peak SNR, 118.1 dB peak SNDR and 120.3 dB dynamic range in a 1 kHz bandwidth, while consuming 280 µW; resulting in a Schreier FoM of 185.8 dB.

Acknowledgments

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Chapter 1

Introduction

The physical environment around us consists of a sea of signals, existing in various forms of energy. Everything, from the light we see to the sound we hear, can be considered a signal, carrying information with it. While a natural system like our eyes and ears serve us well in sensing and relaying this information to our brain, we must rely on electronics if we wish to extract it for further use. Sensors are used to convert these physical quantities into appropriate electrical signals. More often than not, these signals are analog in nature.

In applications where straightforward signal processing such as amplification, multiplication, or filtering is required, pure analog circuits can work quite up to the mark. However, as the complexity of processing increases, carrying it out in the analog domain is inconvenient. Two major drawbacks associated with analog processing are noise and signal storage. Complicated analog processing requires a lot of electronic hardware, each contributing their own noise. Moreover, analog memory formats tend to degrade over time and have limited storage capacity.

Digital signal processors (DSPs) are optimized specifically for numerical computations needed for signal processing. Working with signals in the digital domain offers several advantages over analog processing. Digital signals, discrete in both amplitude and time, are represented as a logic using only 1s and 0s, making it almost perfectly immune to noise, and easier to process and store. Rapid device scaling over the years helped increase transistor count in processors, increasing DSP functionality and its capability to handle complex signal processing algorithms. At the same time, digital memory began shrinking in size and increasing in storage capacity. These advantages, along with several others, outweighed the drawbacks of digital processing- such as latency and limited bandwidth, and pushed for signal processing to be done digitally.

An analog to digital converter (ADC) forms a critical link in the signal chain of any signal processing system. To avoid the drawbacks of analog electronics, it is essential to have this conversion as early in the signal chain, as possible. In some cases, once the DSP completes its operation, a digital to analog converter (DAC) is needed at the output of the signal chain to convert the logical ones and zeros into an analog quantity for the real world.

1.1 Motivation

The requirements from an ADC varies with application in terms of accuracy, speed and power consumption. There always exists a trade-off between the three, and hence, there doesn't exist one perfect ADC for all. Like any other analog circuit, an ADC is designed taking into account the bandwidth of the input signal. Applications such as telecommunication, video imaging, etc., consist of high frequency signals, occupying bandwidths greater that 1-10 MHz; the mid frequency range consists of audio signals, such as that of speech or music, with bandwidths of approx. 4-24 kHz. This work focuses on signals in the low frequency end of the spectrum. Slow changing signals, with bandwidths of around 1-2 kHz, dominate applications such as industrial measurements of sensor outputs, instrumentation, biomedical signal processing, etc. Signals in these domains can vary from a micro-volt level to volts. Furthermore, many of the devices used in these applications are battery powered, such as wearable medical devices and portable instrumentation. The ADC used to acquire these signals should therefore, not only be precise and accurate, but also extremely energy efficient.

A measurand ranging from 1µV to 1V, typical in the desired application, translates roughly into a dynamic range (DR) of 120 dB (or a resolution of 20 bits). From an architectural perspective, both delta-sigma ($\Delta\Sigma$) and dual-slope ADCs are capable of achieving such a resolution. However, in case of a dual-slope ADC, the resolution is proportional to the conversion time, drastically limiting its bandwidth and increasing its power consumption. $\Delta\Sigma$ ADCs, although not the most energy efficient, use the principle of noise-shaping and oversampling to achieve high resolution more quickly [2]. From the point of view of a low power architecture, the SAR ADC is quite well known, while operating at moderate bandwidths. However, its resolution is limited to 12-14 bits [3, 4]. While architectures such as the error-shaping SAR ADC in [5] and the SAR assisted incremental ADC in [6] have been proposed to tackle this, their DR is limited to about

100 dB. Although the $\Delta\Sigma$ modulator ($\Delta\Sigma$M) proposed in [7] achieves a DR of 136 dB , it is at the expense of high power consumption (12.7 mW).

The concept of *zoom-in,* introduced in the incremental zoom ADC in [8], obtains the benefits of both the SAR ADC- in terms of its energy efficiency, and the $\Delta\Sigma$ ADC- in terms of its high resolution. However, while it achieves a dynamic range of 119.8 dB, its bandwidth is severely limited to pseudo-DC signals. The objective of this thesis is to design a zoom ADC that retains the resolution and energy efficiency, but dramatically expands the input bandwidth to the kHz range to satisfy the needs of most instrumentation and industrial applications.

1.2 Thesis Organization

This thesis project entails the architectural conception, circuit design, layout, and measurement of the fabricated prototype IC. The thesis report is organized as follows:

- **Chapter 2** presents different approaches to achieve a high resolution using $\Delta\Sigma$ modulation. The concept of *zoom-in* is introduced, along with some recent works that use this principle, and their limitations.
- **Chapter 3** presents some of the system level variables of a dynamic zoom-in ADC. Sources of errors, both systematic and random, are discussed in detail, along with techniques to mitigate them and determine their optimum values.
- **Chapter 4** deals with the finer circuits details of some of the building blocks.
- **Chapter 5** presents some of the challenges involved in characterizing an ADC, the measurement setup, and the measurement results of the prototype IC, and a comparison of its performance with existing state-of-the-art ADCs for similar applications.
- **Chapter 6** concludes this thesis project, along with suggestions for future research.

Chapter 2

High Resolution ADCs

2.1 Nyquist-Rate Converters

Converting an analog signal to digital primarily involves two steps- sampling and quantization [3]. No information is lost during sampling if the sampling frequency (f_S) follows the Nyquist criteria, given as,

$$f_S > 2 \cdot BW = f_{S,Nyquist} \tag{2.1}$$

where, BW is the bandwidth of the signal. The error associated with quantization is fundamental and unavoidable. In most practical cases it is safe to consider quantization error as white noise spread over DC to $f_S/2$. The peak signal-to-quantization-noise-ratio (SQNR) for a N-bit Nyquist-rate converter is given as,

$$SQNR_{Nyquist} = 6.02 \cdot N + 1.76\,\text{dB} \tag{2.2}$$

As evident from the equation above, to improve the peak SQNR, a higher resolution ADC must be used. The Successive Approximation (SAR) ADC has generally been the most energy efficient amongst all converter architectures [4].

2.1.1 Successive Approximation Converters

Successive approximation converters use the binary search algorithm to determine the N-bit output code. The output code is determined successively from MSB (a_N) to LSB (a_1) by comparing the sampled input with a set of binary scaled references generated by a DAC, one bit per cycle.

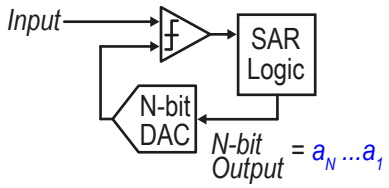

Figure 2.1: Block diagram of a N-bit SAR ADC

As shown in Fig. 2.1, the only components of a SAR ADC are a comparator running N times every f_S cycle, a DAC- usually a capacitive DAC, and some digital logic, making the SAR ADC very energy-efficient. However, due to the N-cycle operation, a clock with a frequency of at least $N \cdot f_S$ is required for a sampling rate f_S.

2.1.2 Limitations

Practical limits in semiconductor technologies prevent achieving resolutions higher than 12-14 bits (without additional correction techniques) in Nyquist-rate converters. This is due to the difficulty associated with generating accurate 2^N equidistributed quantization levels. This imperfection, also referred to as non-linearity of the converter, worsens when trying to increase N and limits the resolution of a practical ADC (or a DAC).

2.2 Oversampling and Noise-Shaping Converters

SQNR can also be increased by sampling at a frequency much greater than the Nyquist rate given by Eq. 2.1, using the same quantizer. In this case, the input is said to be oversampled with frequency,

$$f_S = 2 \cdot BW \cdot OSR \tag{2.3}$$

where OSR is the oversampling ratio, and assumed $\gg 1$. While the noise power is still the same in the full bandwidth of 0 to $f_S/2$, it gets reduced by a factor of OSR in the bandwidth BW of the signal, improving the SQNR of Eq. 2.2 to,

$$SQNR_{OS} = 6.02\,(N + 0.5\,log_2\,(OSR)) + 1.76\,\text{dB} \tag{2.4}$$

The SQNR improves by 6 dB and increases the effective number of bits (ENOB) by 1-bit for every 4x increase in OSR in an oversampled converter. The out-of-band noise is filtered using a digital decimation filter to give a higher resolution digital output at the original

sample rate- $f_{S,Nyquist}$.

2.2.1 ΔΣ Modulation

Quantization noise in an oversampled converter can further be reduced by noise-shaping using the principle of ΔΣ modulation, wherein, a loop filter, an N-bit quantizer, and an N-bit DAC are used in a feedback configuration as shown in Fig. 2.2(a). The overall structure is also referred to as a N-bit ΔΣ modulator (ΔΣM). For a linear analysis of the system in the z-domain, it is easier model the quantizer and the DAC together as a linear gain of 1, with the addition of quantization noise with power spectrum $Q(z)$, as shown in Fig. 2.2(b).$X(z)$ is the frequency spectrum of the sampled input signal- $x(t)$, $H(z)$ is the z-transform of the loop filter, and $Y(z)$ is the output spectrum.

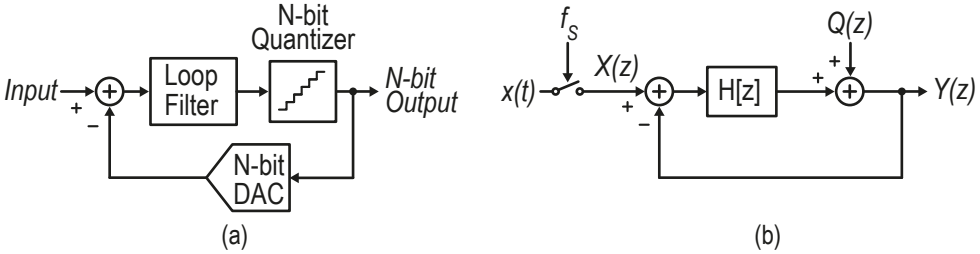

Figure 2.2: N-Bit ΔΣ Modulation- (a) block diagram; (b) linearized z-domain representation

The signal transfer function ($STF(z)$) and the noise transfer function ($NTF(z)$) are given as,

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.5)$$

$$NTF(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1+H(z)} \qquad (2.6)$$

It is evident from the above equations that if $H(z) \gg 1$, $STF \to 1$ and $NTF \to \frac{1}{H(z)}$, suggesting that a high loop gain within the signal band suppresses the quantization noise.

2.2.1.1 1st Order Loop Filter

In case of a discrete-time 1st order ΔΣM, the loop filter is a usually an integrator, also known as accumulator, with a transfer function of,

$$H(z) = \frac{1}{z-1} \qquad (2.7)$$

For such a modulator, the SQNR is given as,

$$SQNR_{1^{st}\,order\Delta\Sigma} = 6.02\,(N + (1.5\,log_2\,(OSR) - 0.86)) + 1.76\,\text{dB} \tag{2.8}$$

Thus, in case of a 1st order ΔΣM, the SQNR improves by 9 dB / 2x increase in OSR, as opposed to 6 dB / 4x increase in OSR by just oversampling.

Fig. 2.3 illustrates the suppression of inband quantization noise (Q_{noise}) noise due to oversampling and 1st order noise-shaping of a N-bit quantizer, with an initial Nyquist-rate quantization noise of Q_{nyq} in a bandwidth BW, when oversampled with OSR. The excess out-of-band noise is filtered with a digital decimation filter.

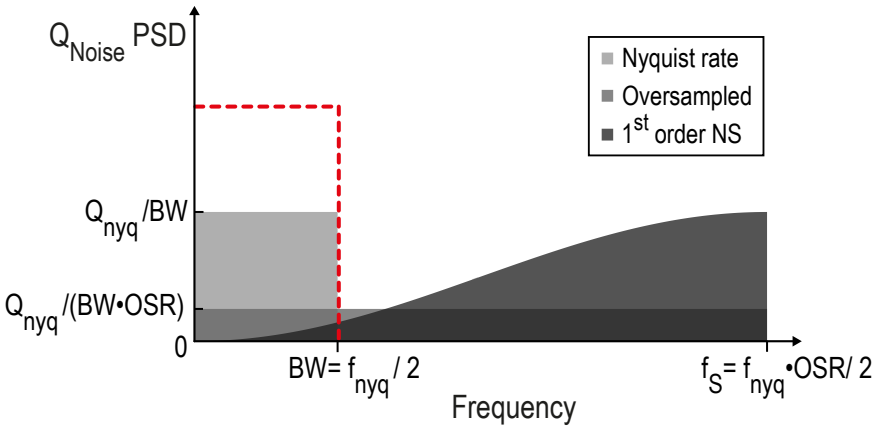

Figure 2.3: Inband quantization noise spectrums for Nyquist-rate, oversampled, and 1st order noise shaped ΣΔ ADCs

2.2.1.2 Higher Order Loop Filter

To suppress the quantization noise further, the loop filter order can be increased by cascading accumulators. In general, it can be shown that the SQNR improves by $(2n+1)\cdot 6$ dB / 2x increase in OSR for a n^{th} order ΔΣM [3].

However, higher order ΔΣMs are prone to instability, which requires additional circuit complexity to stabilize it, generally reducing the SQNR improvement. As a higher order loop filter pushes a larger amount of quantization noise out-of-band, the requirements of the decimation filter increase, together with its complexity and digital power consumption. Another major drawback of ΔΣ modulation is that the signal cannot cover the full scale of the ΔΣM without causing overload [3]. This problem worsens with the order of the ΔΣM.

2.2.2 Single-Bit Vs Multi-Bit ΔΣ Modulation

In many applications, the inband noise suppression achieved using ΔΣM is sufficient enough to simply allow the use of a 1-bit quantizer and 1-bit DAC. Fig. 2.4 shows the ideal SQNR in a 1-bit ΔΣM with increasing loop filter order, based on the equations above. As the quantizer, generally a comparator, outputs just a 1-bit stream, the DAC only has to operate between two levels. This makes this system almost perfectly linear, more so than any Nyquist-rate N-bit converter.

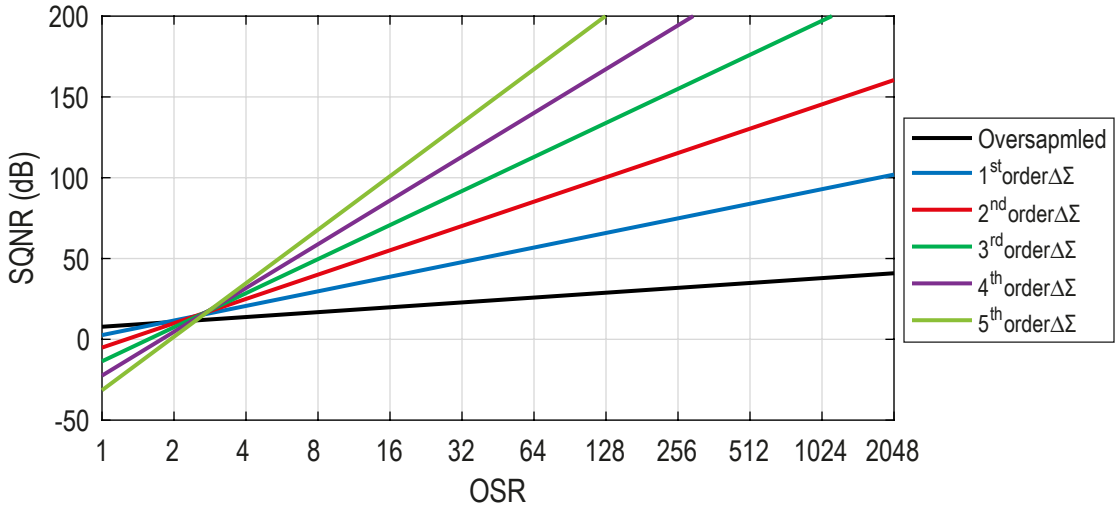

Figure 2.4: SQNR vs OSR for a n^{th} order 1-bit ΔΣM

A multi-bit ΔΣM theoretically suppresses the quantization noise power of a similar 1-bit ΔΣM by a factor of 2^{2N}, increasing SQNR proportionately. In other words, the loop filter order and the OSR are more relaxed in a N-bit ΔΣM, when compared to a 1-bit ΔΣM with similar SQNR, relaxing the decimation filter requirements. It also allows better use of the full scale, which improves with higher N.

However, the multi-bit operation requires a N-bit DAC, bringing back the issue of non-linearity. Being in the feedback path, its linearity is of more importance than that of the N-bit quantizer or the loop filter. The N-bit quantizer itself is generally a flash ADC requiring 2^N comparators, exponentially increasing power consumption. While oversampling allows the use of digital techniques like DEM to linearize the N-bit DAC, it is difficult to reduce the power consumption of the N-bit quantizer.

2.3 Zoom ADC

A zoom ADC has all the advantages of a N-bit ΔΣM, despite using a 1-bit quantizer, as in a 1-bit ΔΣM. This is done by combining a SAR ADC with a ΔΣM, into a single, energy-efficient, high resolution architecture as shown in Fig. 2.5. The N-bit SAR ADC helps make a coarse conversion using N clock cycles, outputting a coarse result K which follows the relation,

$$K \cdot V_{LSB} < V_{IN} < (K+1) \cdot V_{LSB}\,, \quad K = 0 \ldots (2^N - 1) \tag{2.9}$$

where, V_{LSB} is the quantization step size of the SAR ADC and V_{IN} is the input. N generally varies from 4 to 6, ensuring that the SAR ADC consumes negligible power compared to the rest of the ADC. The ΔΣM oversamples the input with a N-bit DAC switching only between $K \cdot V_{LSB}$ and $(K+1) \cdot V_{LSB}$, essentially *zooming in* on the signal by providing finer references. As the N-bit DAC in the zoom ADC only switches between two levels, the quantizer can be a simple comparator, avoiding a power hungry N-bit flash ADC. Some of the existing zoom ADCs are explained below.

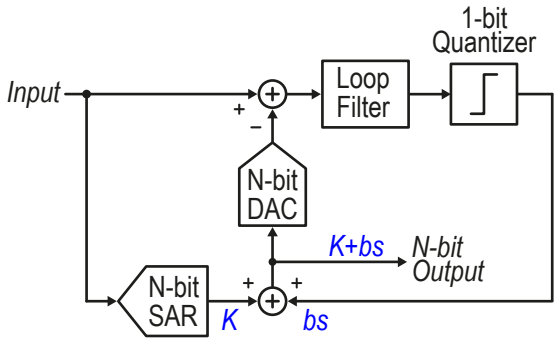

Figure 2.5: Block diagram of a dynamic zoom ADC

2.3.1 Incremental Zoom ADC

The incremental zoom ADC [8] was designed for pseudo-DC signals, allowing sequential operation of the SAR ADC and ΔΣM. The overall result is obtained by decimating the comparator 1-bit output stream ($bs = 0/1$) to a M-bit fine resolution, which, together with the N-bit coarse result K, provides a theoretical maximum ENOB of N+M.

2.3.2 Dynamic Zoom ADC

The dynamic zoom ADC [9] is another variant, wherein, the SAR ADC runs in tandem with the ΔΣM. To handle a higher bandwidth, the N-bit SAR ADC runs in the background and periodically updates K every N cycles. The free-running ΔΣM on the other hand, always uses an updated K to generate the fine references and zoom in on the input. As K keeps changing with input, the output of the dynamic zoom ADC is given as $K + bs$, a N-bit oversampled digital code, which is decimated to give a high resolution output.

2.3.3 Sources of Error

The zoom ADC, like any other ADC, has several sources of error. However, the flexibility offered by the architecture makes it is easier to tackle them.

2.3.3.1 Nonidealities in the SAR ADC

As explained previously, it is impossible to get perfect linearity when dealing with a multi-bit converter. In a zoom ADC, both the SAR quantization levels and DAC outputs are required to be perfectly matched and linear to the desired final accuracy (N+M=20 bits). This defeats the purpose of using an relaxed N-bit SAR ADC, if it is expected to have a full (N+M)-bit resolution. This constraint is easily overcome using over-ranging, where the value of bs is increased from $0\,|\,1$ to $-OR\,|\,(1+OR)$. The fine references provided by the N-bit DAC, thus, cover a larger range, accommodating the errors of the SAR ADC, as illustrated in Fig. 2.6. It also helps mitigate some of the other nonidealities of the SAR ADC such as offset and noise. In case of offset, there is an overall shift in the SAR quantization levels; whereas for noise, there is usually a bit error when the signal is close to a quantization level.

Over-ranging is essential for a dynamic signal when it approaches a quantization level, to keep the signal around the center of the fine references and avoid overloading the ΔΣM. This is illustrated in Fig. 2.7(a) where the ΔΣM saturates as the signal approaches the fine reference and (b) where an over-ranging of $OR = 1$ is added to bs and relaxes both the fine references by one V_{LSB}. The figure also illustrates that the coarse code K is updated every N=5 cycles.

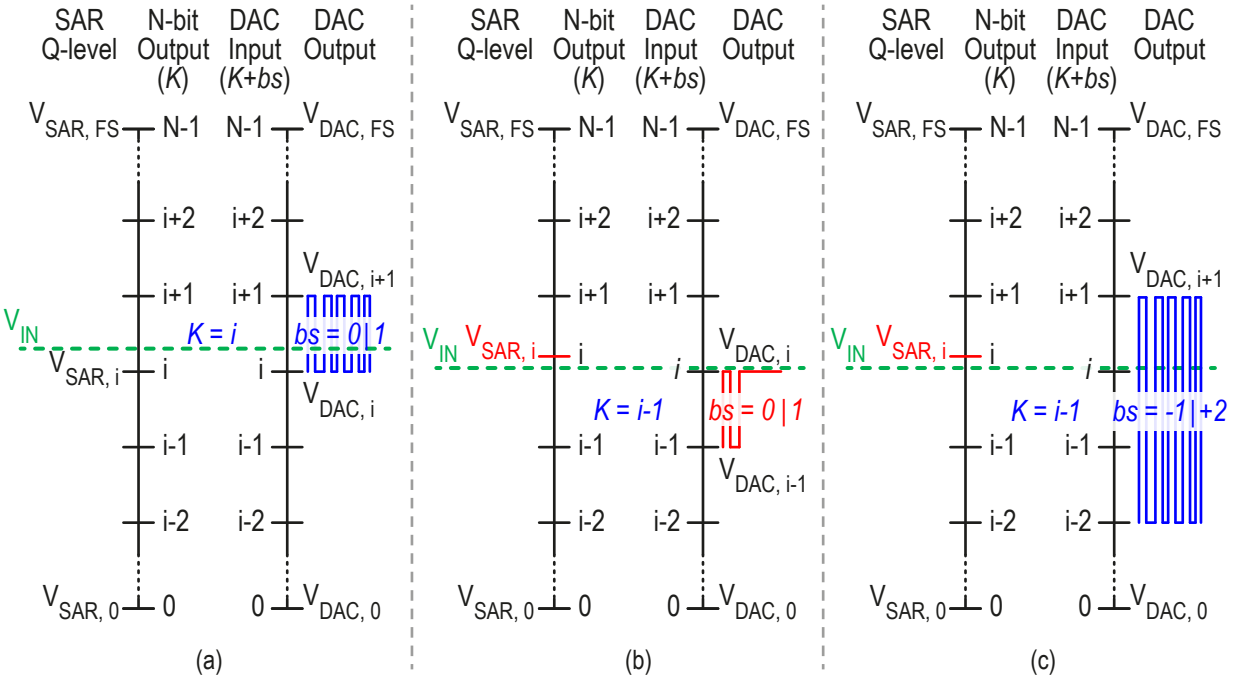

Figure 2.6: Fine references set by DAC- (a) without over-ranging; (b) same as (a), but with nonideality in SAR ADC; (c) same as (b), but with over-ranging

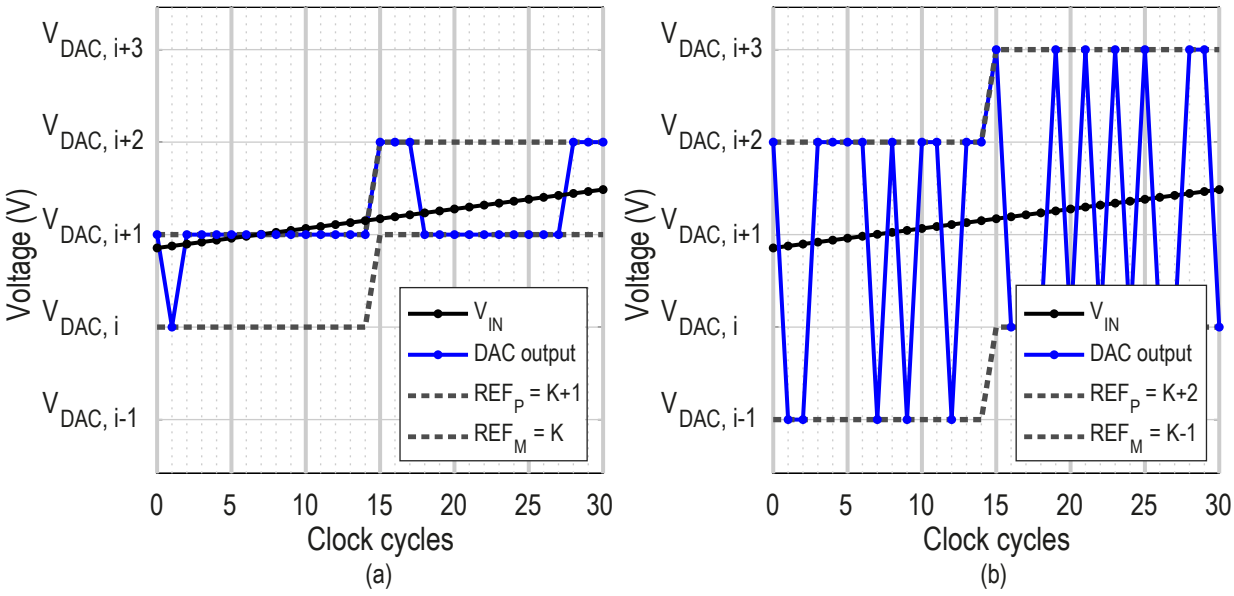

Figure 2.7: Time domain (discrete-time) operation of a dynamic zoom ADC- (a) without over-ranging; (b) with over-ranging $OR = 1$

2.3.3.2 Nonidealities in the ΔΣM

While over-ranging relaxes the constraints on SAR ADC by a huge extent, it does nothing to mitigate the non-linearity of the N-bit DAC. Techniques such as dynamic element matching are typically used efficiently in multi-bit designs to improve their linearity, and applies to the zoom ADC as well. Apart from non-linearity, the major contributors of errors that reduces the absolute accuracy and precision of an ADC are noise and offset. This becomes especially critical when targeting signals of low bandwidth, as flicker noise becomes dominant.

2.3.3.3 Robustness to Interferers

The zoom ADC has evolved, and is generally designed, to handled signals within a certain bandwidth. However, unlike a N-bit ΔΣM, it remains vulnerable to high frequency out-of-band signals. Although these out-of-band *interferers* are filtered out by the decimation filter, the zoom ADC's inability to track them increases the inband quantization noise. This limits the use of the zoom ADC to applications where these interferes are not expected, or, makes it necessary to use a sharper anti-aliasing filter before the ADC to block them. While the former may be tolerable, the latter is not typical in an oversampled converter, where the high sampling frequency actually benefits the anti-aliasing filter by relaxing its cutoff frequency and roll-off rate.

2.4 This work

The dynamic zoom ADC described in the following chapters, converts input signals limited to a 1 kHz BW with a 20-bit resolution, while consuming minimum power. This is done by employing an asynchronous SAR ADC instead of the conventional N-cycle SAR ADC. This change relaxes the loop filter design both on a system and circuit level, while making the zoom ADC immune to higher frequency out-of-band interferers. Similar to the previous zoom ADCs, a discrete time loop filter is chosen due to some of the advantages it offers over its continuous time counterparts in a high precision application.

Chapter 3

System Level Design and Optimization

To optimize for the different variables at a system level, it is essential to look into certain circuit aspects and the expected sources of nonidealities. The most dominant of them - noise, offset, and non-linearity, from both the SAR ADC and the ΔΣM, are considered for this design and tackled independently.

3.1 Continuous vs Discrete Time ΔΣMs

A continuous time (CT) ΔΣM consumes less power compared to the discrete time (DT) ΔΣM. This is due to the active elements (integrators) in the loop filter having a relaxed bandwidth specification, as they are generally designed for a signal bandwidth much lower than f_S [2]. The integrators in a DT loop filter are designed using switched-capacitor circuits, requiring a bandwidth higher than f_S for sufficient signal settling, increasing power consumption. However, for a precision application such as this, a DT-ΔΣM offers several advantages over their CT counterparts. A CT-ΔΣM is more sensitive to clock jitter, as it modulates the feedback DAC pulse widths and shows up as jitter noise, degrading SNR [10]. This effect is not dominating in a DT-ΔΣM, since sufficient settling ensures that the modulator is immune to jitter.

Another major drawback of the CT-ΔΣM is the spread of the loop filter's pole and zero locations, which compromises performance and stability when not taken care of using additional tuning/ calibration circuits. In a DT loop filter, the pole and zero locations can be more tightly defined, as they are designed using capacitors only, and as such, the

relative spread between them is much less. Hence, a discrete time ΔΣM is chosen in this design.

3.2 System Parameters

3.2.1 Sampling Rate

While a high sampling frequency f_S helps reduce the inband noise, it also increases digital and analog power consumption. Hence, it is important to find the lowest f_S (or OSR) that helps meet the design criteria. An energy efficient design is generally dominated by thermal noise. The input stage of any discrete time loop filter consists of a sampling capacitor (C_S) to sample the input signal. However, this is always associated with the addition of white noise, also called kT/C noise, with a power of,

$$\bar{v}_n^2 = \frac{kT}{C_S} \tag{3.1}$$

where k is the Boltzmann constant, T is the temperature in kelvin. Since sampling happens right at the input, it does not get shaped by the NTF and can only be reduced by oversampling. The inband thermal noise power and corresponding SNR for a differential signal of peak amplitude (A_p), are given as,

$$\bar{v}_{n,inband}^2 = \frac{4kT}{C_S} \cdot \frac{1}{OSR} \tag{3.2}$$

$$SNR = \frac{A_p^2/2}{\bar{v}_{n,inband}^2} \tag{3.3}$$

The additional factor 4 in the noise power is due to two reasons- first is due to a differential implementation requiring two seperate sampling capacitors; second, the feedback DAC that provides the fine reference is also a sampling operation, contributing to noise. Assuming a peak amplitude of 95 % of 1.8 V supply voltage and 120 dB SNR (ENOB ≈ 20 bits), a nominal value for C_S and OSR using above equations would be 11.3 pF and 1000 respectively. Thus, $f_S = 2$ MHz for a 1 kHz bandwidth.

The above values hold for room temperature of $T = 300$K. Furthermore, the peak amplitude tolerable changes with the resolution of the SAR ADC, and the amount of over-ranging. To account for them, with some additional headroom, the final chosen values are $C_S = 13.6$ pF and $OSR = 1000$.

3.2.2 Coarse Resolution and Loop Filter Order

Increasing the loop filter order and the coarse resolution-N of the SAR ADC helps in quantization noise suppression. However, a conventional SAR ADC takes N clock cycles to determine the coarse code K. Furthermore, this value of K is used to set the fine references of $\Delta\Sigma$M for the next N cycles before it updates again, constraining V_{IN} to stay withing the fine references for 2N cycles and making it difficult to track high frequency interferers. For this reason, an asynchronous SAR ADC is chosen for this design. The asynchronous SAR ADC calculates the N-bit coarse code within one clock cycle, thereby improving the zoom ADC's tracking ability.

To ensure that quantization noise doesn't add too much to the thermal noise, the target for SQNR is kept higher at 130 dB. Fig. 3.1 shows the variation of peak SQNR achievable with different coarse resolutions and loop filter orders for $OSR = 1000$. As a starting point, the coefficients for the 2$^{\text{rd}}$ and 3$^{\text{rd}}$ order loop filters are taken from [8] and [9] respectively. For every case, an over-ranging of 1 V_{LSB} is used ($OR = 1$), meaning the fine references are set as,

$$\{V_{REF\text{-}} = (K-1)\cdot V_{LSB}\} \;<\; V_{IN} \;<\; \{V_{REF+} = (K+2)\cdot V_{LSB}\}\;, \quad K = 1\ldots(2^N-2) \tag{3.4}$$

It can be seen that, while every configuration exceeds the target SQNR of 130 dB at $f_S = 2$ MHz, a 3$^{\text{rd}}$ order loop filter is unnecessary due to the high OSR. Among the 2$^{\text{nd}}$

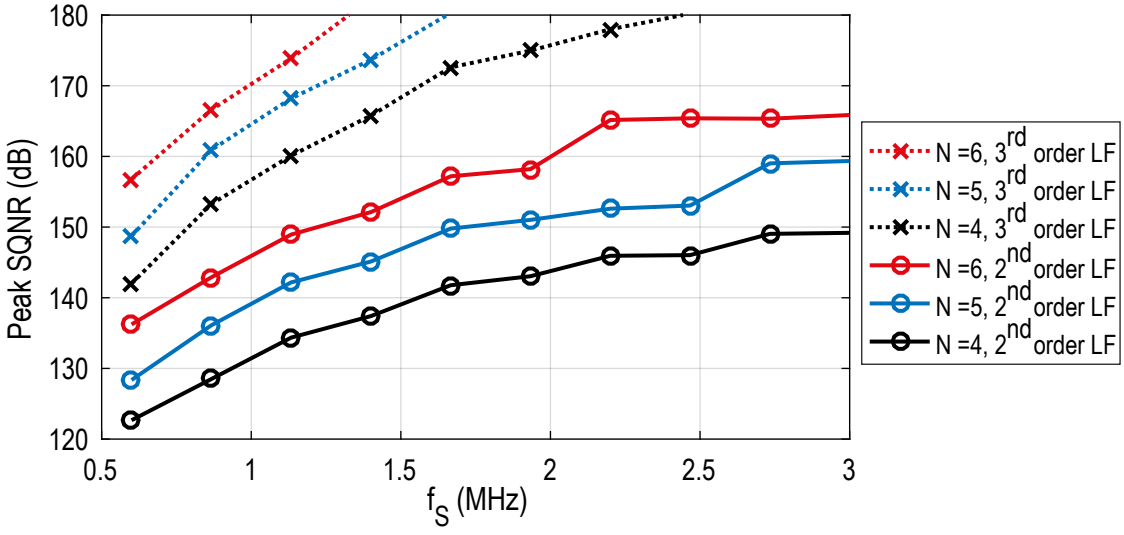

Figure 3.1: Peak SQNR vs N and loop filter order

order loop filters, for a 5-bit coarse resolution ($N = 5$), the output swing of the integrators is half of that when using $N = 4$. Furthermore, circuit nonidealities such as finite gain and bandwidth of the integrators degrade this SQNR, and hence, the extra headroom is beneficial in relaxing the design constraints on the integrators. On the other hand, a 6-bit course resolution has a lower tolerance to out-of-band signals, as explained in the next section. For theses reasons, a 5-bit SAR ADC is chosen over a 4 or 6-bit one. The drawbacks of a 5-bit SAR ADC over 4 bits include an extra bit processing by the SAR asynchronous logic, and slightly tighter constrains on its design.

3.2.3 Over-Ranging

A higher over-ranging means a higher bandwidth signal can be tolerated, but with a reduced SQNR. A sine wave with frequency f_{IN} and peak amplitude V_{FS} has a maximum slope of,

$$m_{sine} = 2\pi V_{FS} f_{IN} \tag{3.5}$$

The zoom ADC updates the coarse code every cycle ($\Delta t = t_S$), during which, the above signal changes by (assuming $f_{IN} \ll f_S$),

$$\Delta V = m_{sine} \cdot \Delta t \tag{3.6}$$

If this signal is initially close to a coarse quantization level K ($V_{IN} = K \cdot V_{LSB}$), it can generate a coarse code $K-1$ (bit error) due to any of the SAR ADC nonidealities discussed later. Based on these conditions, a relation between maximum tolerable frequency and over-ranging (OR) can be established as,

$$V_{IN} + \Delta V < \{V_{REF+} = (K + OR) \cdot V_{LSB}\} \tag{3.7}$$

$$\Rightarrow f_{IN} < \frac{OR \cdot f_S}{\pi \cdot (2^N - 1)} \tag{3.8}$$

Based on this equation, Fig. 3.2 shows the maximum tolerable input frequency $f_{IN,\,max}$ with over-ranging OR, for different coarse resolutions.

While this calculation neglects the headroom required to prevent the loop filter from overloading, it does provide a ballpark of input frequency range tolerable for different coarse resolutions. It can be concluded that, even with a minimum over-ranging $OR = 1\,V_{LSB}$ for $N = 5$, the asynchronous SAR ADC significantly improves the zoom ADC's tolerance to

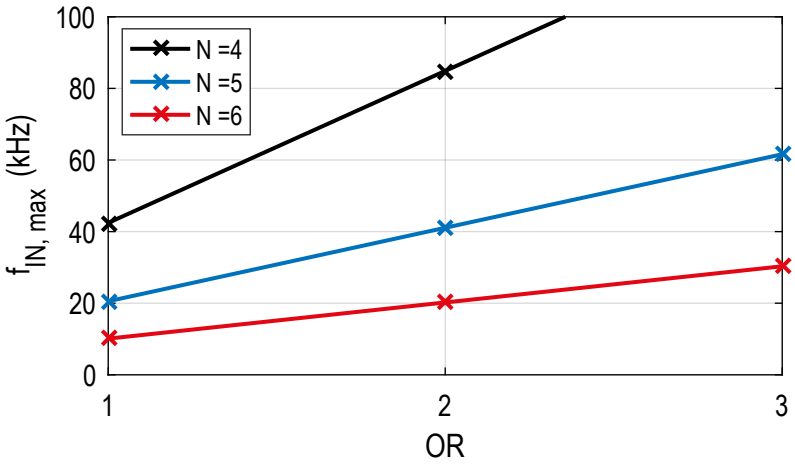

Figure 3.2: Maximum input frequency tolerable vs *OR* and N

out-of-band interferers.

3.2.4 Loop Filter Coefficients

A cascade-of-integrators with feed-forward (CIFF) structure is used to design the 2nd order loop filter $H_2(z)$, with coefficients for a non-aggressive noise shaping. Fig. 3.3(a). shows the loop filter with the negative feedback around it to assess its stability; (b) shows the

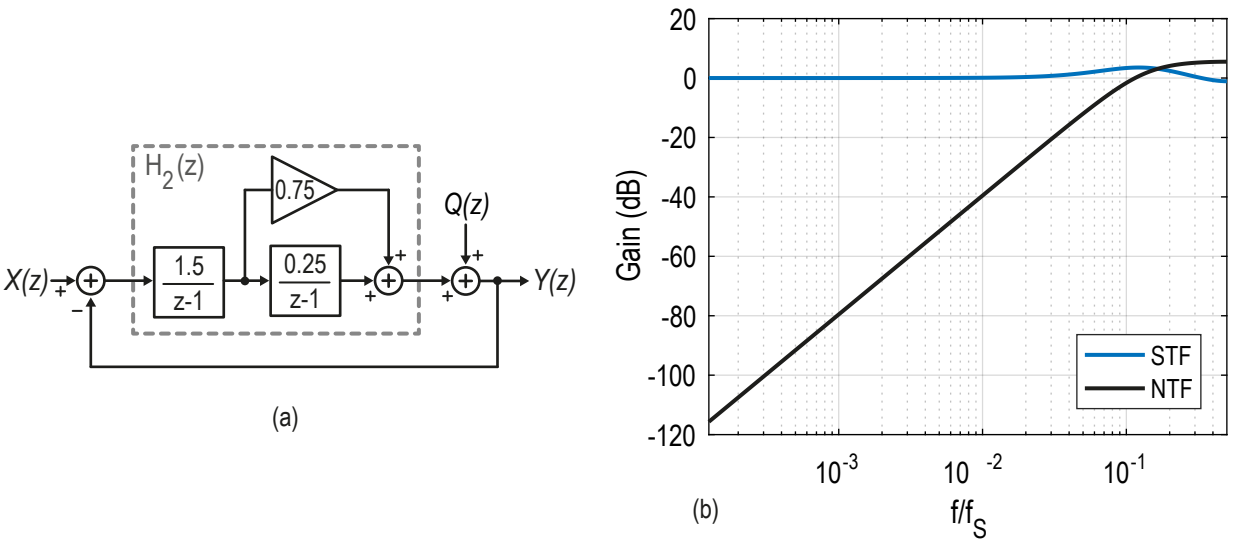

Figure 3.3: $H_2(z)$- (a) linearized z-domain representation; (b) closed loop gain magnitude plots

magnitude response of the *STF* and *NTF*.

Fig. 3.4 shows a more detailed block diagram of the dynamic zoom ADC and Fig. 3.5 shows the simulated SQNR for an input signal with peak amplitude $V_{IN\text{-}p} = 0.95V_{FS}$, with all the parameters determined so far, but without any circuit nonidealities.

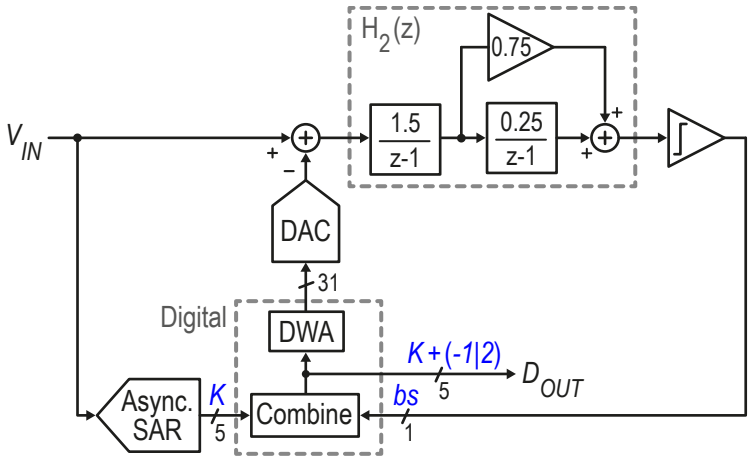

Figure 3.4: Block diagram of the dynamic zoom ADC employing a 5-bit asynchronous SAR ADC and a 2nd order loop filter

3.3 Circuit Nonidealities

So far it has been assumed that everything is ideal. However, circuit nonidealities exist and some of them need to be taken into account at this stage.

3.3.1 SAR ADC Inaccuracy

The SAR ADC's output code K can have bit errors due to the SAR comparator's offset, random spread of unit capacitance used to implement the SAR DAC, and sampling and reference noise during the SAR conversion. A coarse quantization error simply detracts from the over-ranging applied and reduces the maximum tolerable frequency. This changes Eq. 3.8 to,

$$f_{IN} < \frac{(OR\text{-}\epsilon)\cdot f_S}{\pi \cdot (2^N - 1)} \tag{3.9}$$

where $\epsilon = {}^{\sigma(V_{LSB})}/_{V_{LSB}}$, is the the standard deviation of the SAR ADC's quantization levels normalized to $1\,V_{LSB}$ with all the error sources combined. An $\epsilon = 10\%$ w.r.t. a V_{LSB} of

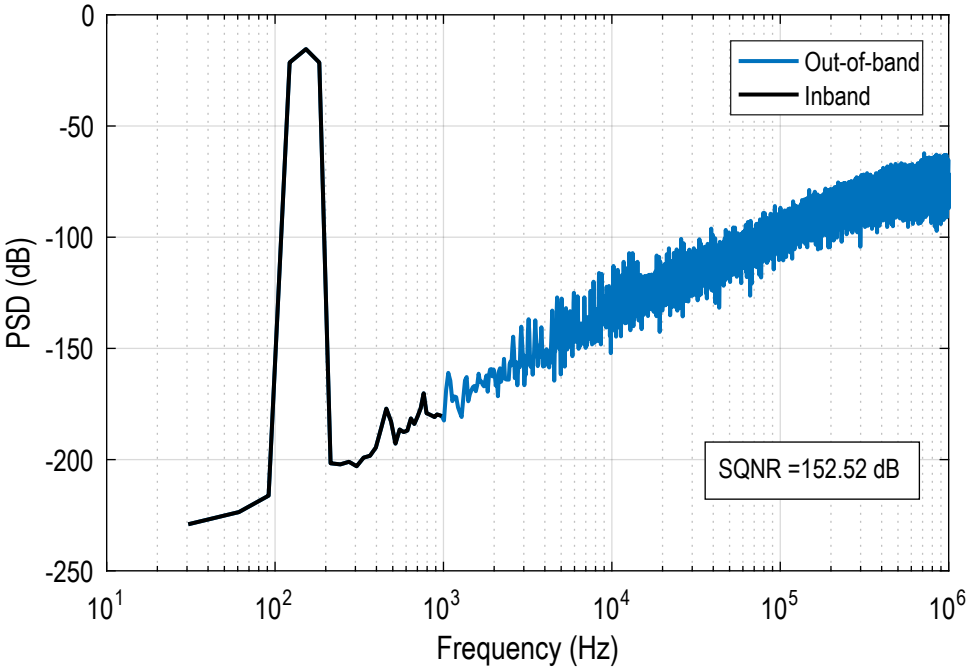

Figure 3.5: Power spectral density of the zoom ADC for $V_{IN\text{-}p} = 0.95V_{FS}$

a 5-bit converter translates roughly into an accuracy of 7-bit and decreases the maximum tolerable frequency by just 10% to $f_{IN,\,max} \approx 18\,\text{kHz}$. Since it is still 18x signal BW, the target accuracy of the SAR ADC is set to 7-8 bits.

3.3.2 Nonideal Integrators

The ΔΣM integrators in the loop filter are implemented as a switched-capacitor circuit, using operational transconductance amplifiers (OTA). However, these OTAs have a finite gain and bandwidth, which limit settling accuracy of the integrators, and thus, the maximum achievable SQNR. Increasing either the gain or the bandwidth requires more power, and therefore, it makes sense to assess how much of it is actually needed. Fig. 3.6 shows an approximate model of a discrete time integrator with finite gain.

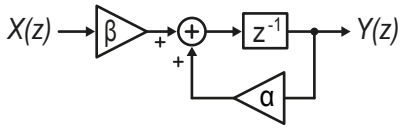

Figure 3.6: Discrete time model of an integrator with finite gain

The coefficients α and β are given as,

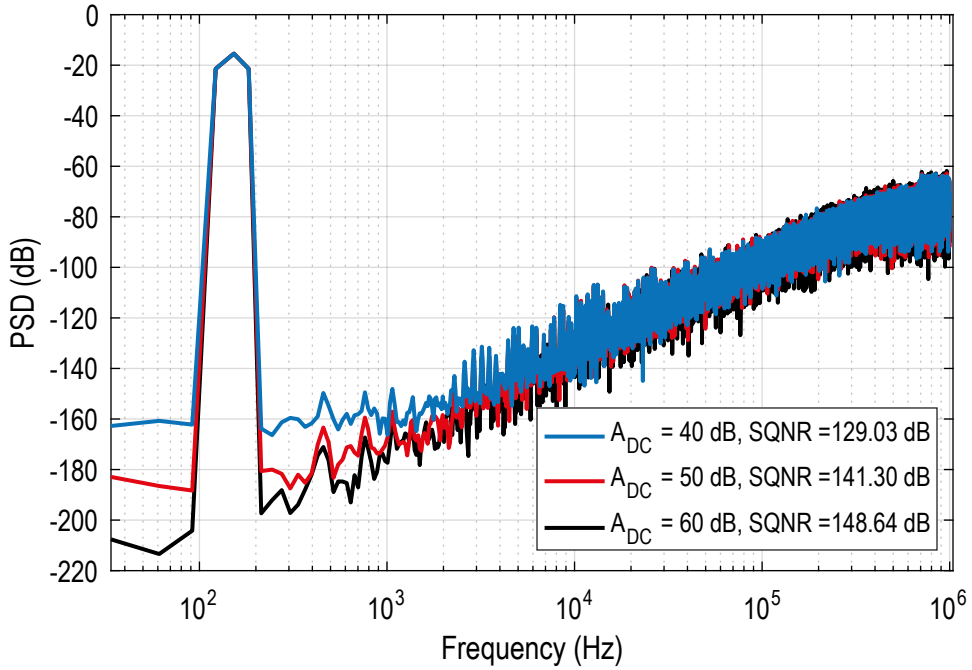

Figure 3.7: SQNR variation with integrator DC gain for $V_{IN\text{-}p} = 0.95V_{FS}$

$$\alpha = 1 - \frac{b}{A_{DC}} \qquad (3.10) \qquad\qquad \beta = b\left(1 - \frac{(1+b)}{A_{DC}}\right) \qquad (3.11)$$

where, b is a loop filter coefficient, and A_{DC} is the corresponding integrator's DC gain. Fig. 3.7 shows the variation of SQNR with different integrator DC gains, when using the above model. It can be seen that even a DC gain of 40 dB in both the integrators is sufficient to meet the target SQNR of 130 dB. However, as these integrators are also used for correlated double sampling to reduce their offset and flicker noise, the target gain is kept at 60 dB.

Due to the tight over-ranging, the output swing requirements of the OTAs of a zoom ADC are greatly reduced. Their simple structure, described in the next chapter, follows a first order response, wherein, incomplete settling when not slew-rate limited just results in an integrator gain error.

3.3.3 ΔΣM- DAC Non-linearity

As mentioned before, over-ranging simply helps reduce the accuracy requirements of the SAR ADC. However, the DAC (now, 5-bit) used in the ΔΣM still needs to be 20-bit

accurate. While the unit capacitors used to implement the DAC are much larger than the SAR DAC's (to the extent that it doesn't affect existing calculations), it is still not 20-bit accurate. This issue is resolved using an existing technique known as data weighted averaging.

Data weighted averaging (DWA) is a mismatch error shaping technique for unary DACs to improve the errors caused by mismatch in the unit elements [11]. A unary DAC consists of 2^N–1 unit elements, used to produce each of the quantization levels from 0 (all off) to 2^N–1 (all on). In this, instead of generating the DAC output using the same starting element, they are rotated in a cyclic fashion, where the 1^{st} element used is the immediate next of the last one used for the previous code. This process is illustrated in Table. 3.1. Since all the elements are used successively in cycles, their overall mismatch contribution is 0 on an average. In the frequency domain, this can be seen as a 1^{st} order mismatch error shaping.

Table 3.1: Rotation of elements with DWA for a 3-bit DAC

Clock cycle	DAC code (Binary)	Ptr.	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
1	2	0	1	1	0	0	0	0	0	0
2	4	2	0	0	1	1	1	1	0	0
3	5	6	1	1	1	0	0	0	1	1
4	1	3	0	0	0	1	0	0	0	0

Chapter 4

Circuit Design

In this chapter essential details of the SAR ADC and the ΔΣM are provided, along with some minor details of the add-on blocks, such as - bias generator, clock phase generator and output stage LVDS drivers.

4.1 5-bit Asynchronous SAR ADC

In the previous chapter, it was determined that a SAR ADC with 7-8 bit accuracy would work optimally for this zoom ADC design. Since over-ranging has also made it independent of the rest of the circuit, it is easier to handle this block first. Unlike a conventional SAR ADC, an asynchronous one does not require an N times oversampled clock, but relies on internal states and logic to carry out the binary search algorithm [12]. Fig. 4.1 shows the half circuit schematic of the asynchronous SAR ADC. It consists of an asynchronous digital logic, a binary weighted capacitor DAC (SAR DAC), and a comparator. A more detailed description of each of the blocks follows.

4.1.1 Asynchronous Digital Logic

The SAR ADC keeps tracking the input signal till the rising edge of the clock, at which point the asynchronous logic takes over. Fig. 4.2 illustrates the timing of the various signals used in this logic. Built as an asynchronous state machine, it uses the *outputRDY* signal to progress from one state to the next. A 5-bit ring counter- RC[4:0], as shown in Fig. 4.3, indicates the current state of the system, and a 5-bit DAC register- b[4:0] provides the digital input for the feedback SAR DAC. At the start, both are initialized (*init*) to

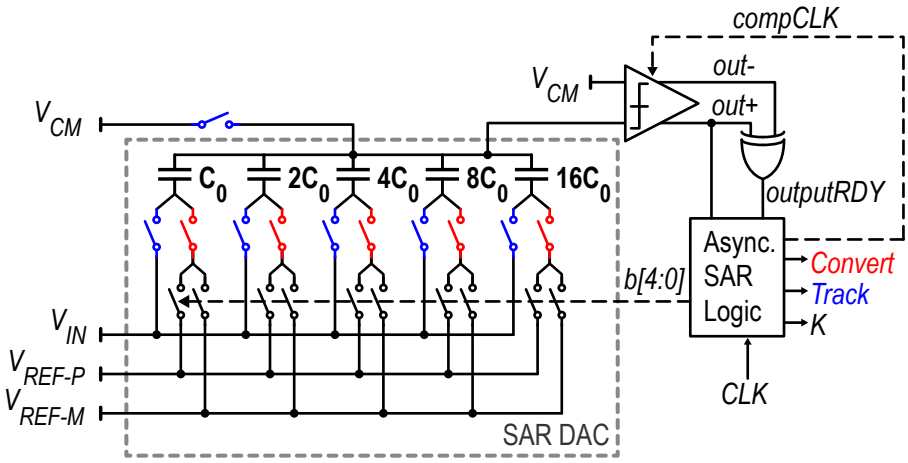

Figure 4.1: Half circuit schematic of the asynchronous SAR ADC

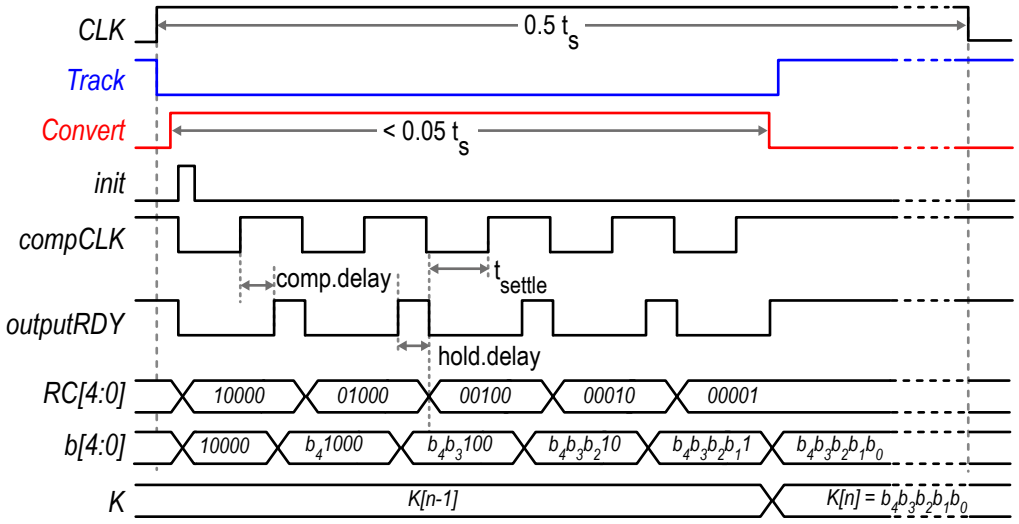

Figure 4.2: Timing diagram of the asynchronous SAR ADC

<10000>, after which, RC progresses with every falling edge of $outputRDY$ and indicates which DAC bit is to be set to 1. The SAR comparator clock ($compCLK$) is generated by simply inverting the $outputRDY$ signal, effectively making the SAR ADC run in a loop till all 5 bits are generated.

There are two intentional delays added to the loop, first is a hold delay before resetting the comparator ($compCLK \rightarrow 0$), to ensure that the comparator output ($out+$) is stored properly; and second- a delay t_{settle} before triggering the comparator ($compCLK \rightarrow 1$) ensures that the settling of the DAC voltage is at least 7-bit accurate. The comparator in

itself has a delay in making a decision (comp.delay), which varies with differential input voltage. *outputRDY* of the last bit is used to indicate end of conversion and switch back to tracking mode. Dynamic logic gates, similar to [13], with long length transistors are used to make the system fast while ensuring it performs satisfactorily at $100\,\text{kHz} < f_S < 25\,\text{MHz}$. The entire conversion is completed in less than 20 ns across PVT.

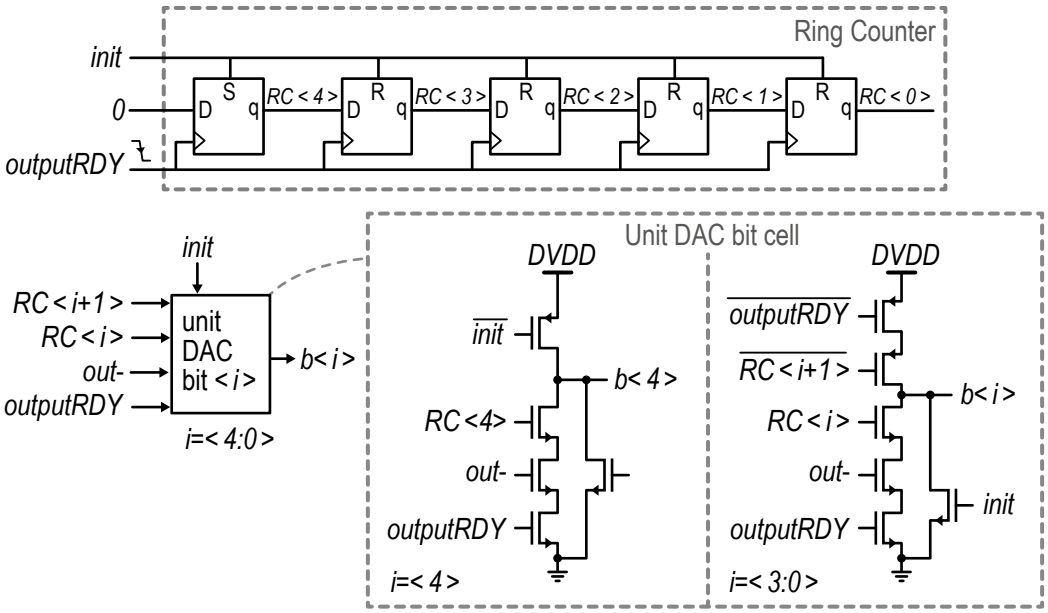

Figure 4.3: Ring counter and DAC register

4.1.2 SAR DAC

The 5-bit SAR DAC is built from 31 unit capacitors (C_0) connected in a binary manner as shown in Fig. 4.1, to form a total sampling capacitance of ($C_{S,SAR} = 31C_0$). It accepts the 5-bit digital code - b[4:0] from the DAC register and uses the principle of charge redistribution [14] to generate the corresponding voltage. Metal fringe capacitors are preferred over any other variant, due to their high level of matching and capacitance density. The sampling capacitance- $C_{S,SAR}$ mainly depends on unit element matching- for linearity, and kT/C noise from sampling, both of which must be lower than a 7-bit level. A larger capacitance also reduces the effect of the comparator kick-back. However, both $C_{S,SAR}$ and the main sampling capacitor C_S, draw currents from the same input and reference nodes as the ΔΣM, and as such, to minimize any coupling between them, $C_{S,SAR}$ must be kept as small as possible. For this reason, C_0 is chosen as 5.8 fF, with $C_{S,SAR} \approx 180\,\text{fF}$.

As a 5-bit SAR ADC will be quantization noise dominated, it is safe to assume that the thermal noise will only affect the LSB decision. The noise due to the SAR DAC at 300 K can be given as,

$$\bar{v}_{n,SAR\,DAC} = \sqrt{\frac{4kT}{C_{S,SAR}}} \approx 0.3\,\mathrm{mV_{RMS}} \tag{4.1}$$

Fig. 4.4 shows the spread of C_0 in a Monte Carlo simulation of 200 runs.

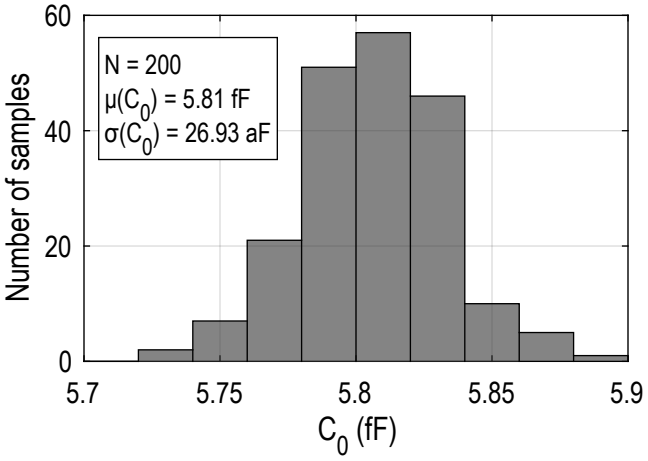

Figure 4.4: Mismatch MC simulation of unit capacitance C_0

The worst case integral non-linearity (INL) of a capacitor DAC is during the MSB-1 decision [3], and can be given as,

$$v_{INL,\,max} = V_{REF-P,M} \cdot \left(\frac{\sigma(C_0)}{C_0}\right) \cdot \sqrt{\frac{2 \times 15 \times 16}{31^3}} \approx 1.1\,\mathrm{mV} \tag{4.2}$$

where, $V_{REF-P,M} = V_{REF-P} - V_{REF-M} = 1.8\,\mathrm{V}$ is the reference voltage to the SAR DAC, and $\sigma(C_0)$ is the standard deviation in C_0. V_{LSB} of an 7-bit differential ADC with $V_{REF-P,M} = 1.8\,\mathrm{V}$ is given as,

$$V_{LSB\text{-}7} = \frac{2 \times 1.8}{2^7} \approx 28\,\mathrm{mV_{RMS}} \tag{4.3}$$

It can be seen that both the noise and non-linearity of the SAR DAC are much smaller than $V_{LSB\text{-}7}$.

4.1.3 SAR Comparator

A two stage dynamic comparator, as shown in Fig. 4.5, is used in the SAR ADC. The first stage consists of a constant current biased pre-amplifier, to minimize the kick-back noise to the SAR DAC. The second stage consists of a dynamic latch driven by the output of the pre-amplifier. A constant current bias in the pre-amplifier ensures that the input pair are held at a fixed V_{GS}, thereby mitigating dynamic offset. Cascodes to the input pair, biased with a fixed voltage V_{b1}, further help reducing kick-back. The pre-amplifier power consumption is minimized by keeping it on only during the conversion phase, which is $< 5\,\%$ of $t_S = 500\,\text{ns}$.

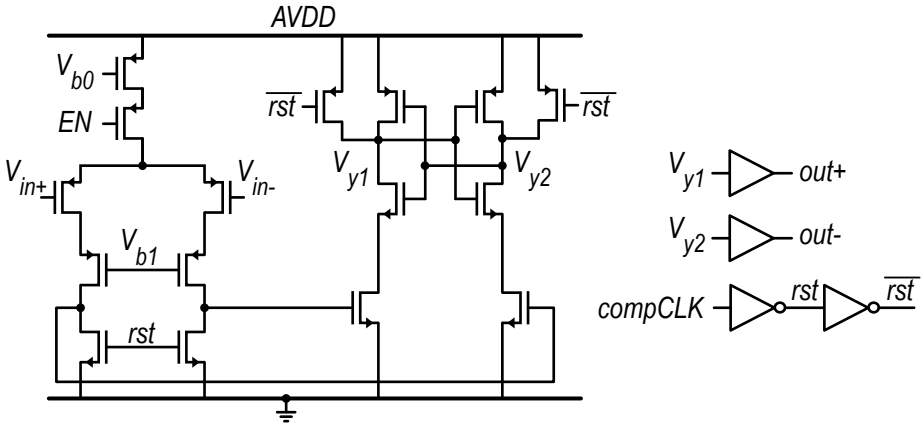

Figure 4.5: Dynamic comparator schematic

To assess the noise performance of the comparator, it is fed with random differential input voltages close to $0\,V_{diff}$, and its probability of a bit error is calculated. The resulting probability density function (PDF), as shown in Fig. 4.6(a), follows a Gaussian distribution, where the standard deviation ($\sigma \approx 1.2\,\text{mV}$) effectively translates into an input referred noise in V_{RMS}; (b) shows the spread in input referred offset of the comparator due to component mismatch, in a Monte Carlo simulation of 200 runs. In both cases, it can be seen that the 3σ values are smaller than $V_{LSB\text{-}7}$.

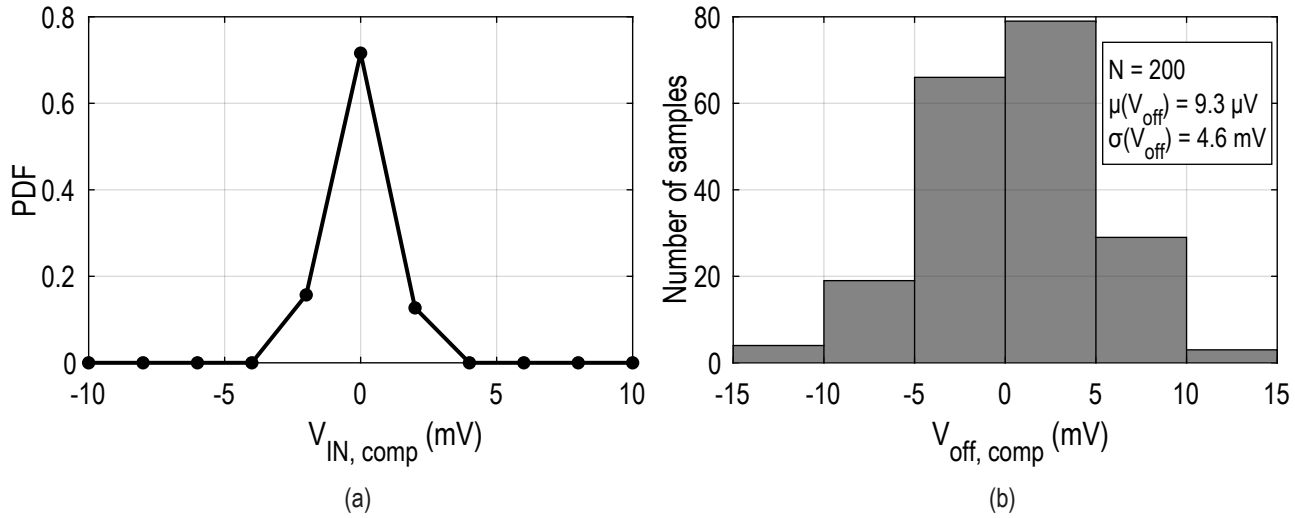

Figure 4.6: (a) PDF of bit error vs $V_{IN,\,comp}$; (b) Mismatch MC simulation of input referred offset

4.2 ΔΣ Modulator

A 2nd order CIFF ΔΣM is designed using the coefficients determined in the preceding chapter. The coefficients were optimized taking into account the stability of the loop filter, output swing of the integrators, and corresponding capacitor sizes. A simplified schematic of the loop filter is shown in Fig. 4.7. The main blocks of the loop filter include the Capacitive DAC and the other capacitors that define the coefficients, OTAs 1 and 2 which act as integrators, and the 1-bit quantizer.

4.2.1 DAC

A unary capacitive DAC, acts as the sampling capacitor for the input (C_S), as well as the feedback DAC. It is built from 31 unit elements with a value,

$$C_{DAC\,[J]} = \frac{C_S}{31} \approx 438\,\text{fF}\,, \quad J = 1 \ldots 31 \tag{4.4}$$

using metal fringe capacitors. During sampling phase ϕ_1, all the units are shorted and the input is effectively sampled on C_S; during ϕ_2, the digital back-end converts the 5-bit DAC code to a 31-bit thermometer code, which is presented to the DAC switches after DWA to generate the appropriate feedback voltage.

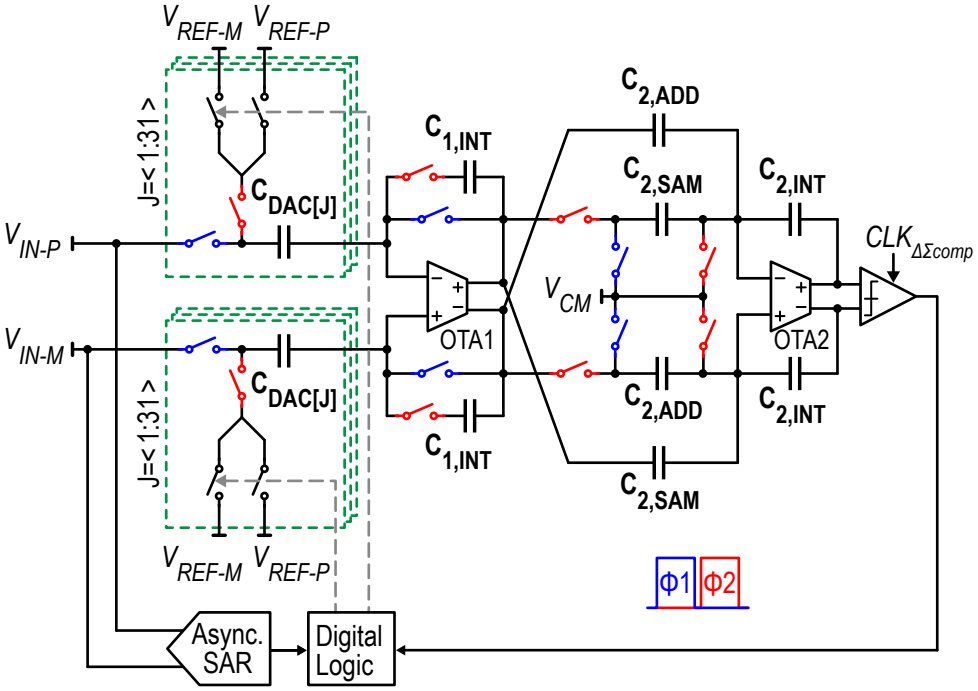

Figure 4.7: Simplified schematic of the 2nd order loop filter

4.2.1.1 Offset and 1/f Noise Suppression

Correlated double sampling scheme (CDS) is implemented, as given in [15], to suppress the offset of OTA1. While the input is shorted to the outer plate of C_S during phase ϕ_1, OTA1 is connected in unity feedback and samples its own offset and 1/f noise on the other plate. During ϕ_2, this offset is effectively canceled and the input gets integrated. However due to the finite DC gain A of OTA1, the offset sampled at the virtual ground node due to unity feedback is $V_{Off} \cdot {}^{A}/_{(1+A)}$. As a result, an input referred offset of an order of ${}^{1}/_{A}$ remains. A typical offset of millivolts gets suppressed to microvolts if the OTA gain is around 60 dB. The offset and noise of OTA2 and the comparator are suppressed by the gain of their preceding stages.

4.2.2 Current-Starved Inverter OTAs

The CDS sampling operation described above is also associated with the sampling of uncorrelated white noise of OTA1, adding to the kT/C sampling noise. This effect is much less pronounced in inverter based OTAs compared to other topologies, when biased with the same current and sizes, as the transconductance is contributed by both NMOS

(g_{mN}) and PMOS (g_{mP}). Its input referred noise voltage spectral density is given as,

$$v_{n,in}\,(V^2/\mathrm{Hz}) = \frac{4kT\gamma}{g_{mN} + g_{mP}} \tag{4.5}$$

where $g_{mN} + g_{mP}$ is the effective transconductance. For a nominal value of γ between $^2/_3$ and 1, this behavior is very similar to that of a resistor, eliminating any excess white noise. Hence, the earlier calculation of C_S based on kT/C thermal noise does not change.

However, the OTAs described in [8, 9] are dynamically biased, requiring additional switches that complicate the structure and layout. The reduced output swing in this design, allows the use of a simple class-A biasing scheme as shown in Fig. 4.8. The head and tail current sources, biased with 48 µA mirrored from a constant-g_m reference, suppress unwanted signal and noise from the supply lines. Cascodes are used to achieve a DC gain of 60 dB. Long length diode-transistors - $M_{c\text{-}N}$, $M_{c\text{-}P}$ are used to bias them to account for $V_{DS,sat}$ spread due to PVT variations.

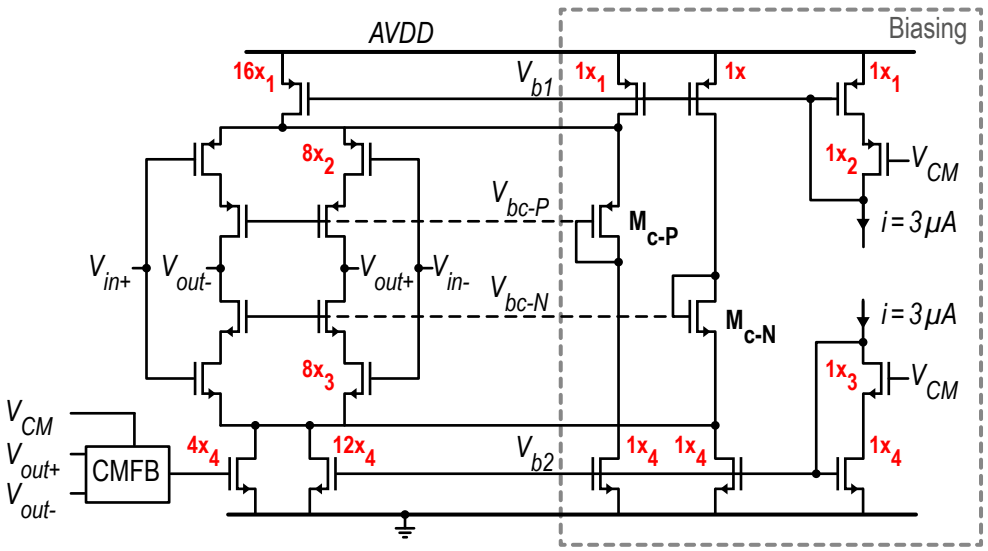

Figure 4.8: Current-starved inverter OTA with biasing

Fig. 4.9 shows the gain magnitude plot of OTA1 in an open loop periodic-AC (P-AC) simulation [16]. OTA2 is an $^1/_8\times$ scaled version of OTA1, with equal current densities and gain, allowing the use of the same bias circuit.

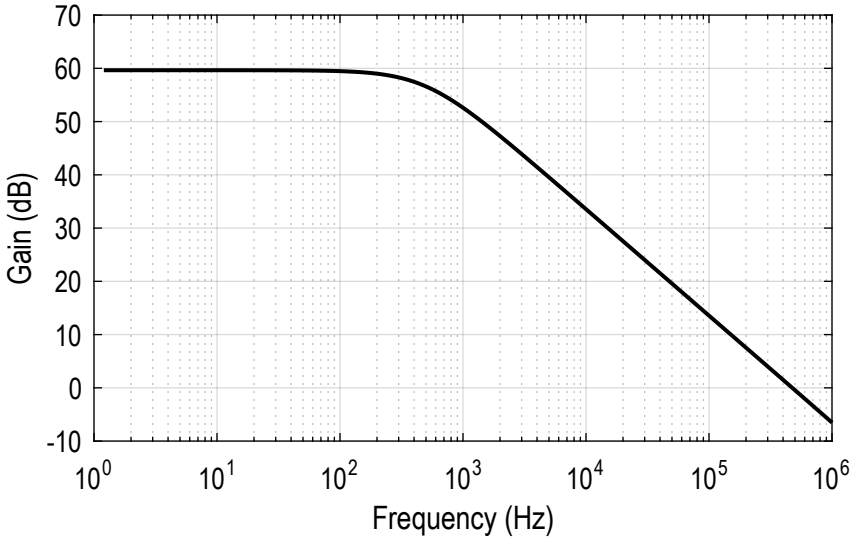

Figure 4.9: OTA1 gain magnitude plot

4.2.3 Capacitors

$C_{1,INT}$, in Fig. 4.7, is sized to 9.1 pF. Since the noise of the 2nd stage will be suppressed by the gain of OTA1, relaxed capacitances of 150 fF, 450 fF and 600 fF are used for $C_{2,SAM}$, $C_{2,ADD}$ and $C_{2,INT}$ respectively.

4.2.4 Comparator

The comparator used in the ΔΣM is the same as the one used in the SAR ADC, but with with a fully dynamic pre-amplifier instead of a constant current biased one. This makes the comparator more energy efficient, but increases the kick-back. Since it is driven by OTA2, the kick-back is absorbed and its effect mitigated.

4.2.5 Timing

Fig. 4.10 shows a simplified timing diagram of the zoom ADC. In order to minimize the coupling between the SAR ADC and the ΔΣM through the ADC input terminal, their sampling instants are kept half clock cycle apart. The clock phases ϕ_1 and ϕ_2 are also associated with their early versions (not shown) for bottom plate sampling. The comparator of the ΔΣM is clocked towards the end of ϕ_2. A conventional non-overlapping

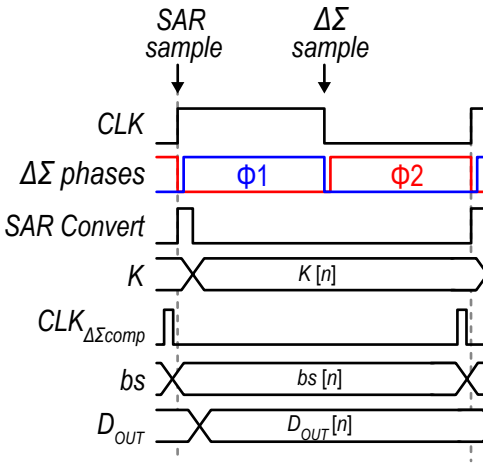

Figure 4.10: Timing diagram of the zoom ADC

clock generator, as described in [17], is used to generate the clock phases for the ΔΣM.

4.3 Miscellaneous Blocks

4.3.1 Constant-g_m Bias Generator

A beta-multiplier cell [17], as shown in Fig. 4.11, is designed to generate the constant-g_m bias source. When the currents through M_1 and M_2 are well matched, the g_ms of the transistors, depend only on the resistance R and relatives sizes of the M_1 and M_2, making it immune to PVT as long as the transistors are in saturation (assuming a square-law model). N-doped poly-silicon resistor was used since it offered the lowest temperature coefficient in the chosen process. A start-up circuit is included to avoid the unwanted state where all transistors are off, which can arise due to the positive feedback around the circuit. The transistors in the start-up circuit are sized to not affect the circuit performance during normal operation.

4.3.2 LVDS Output Buffers

To mitigate the off-chip coupling of the digital bits with the sensitive analog signals, LVDS drivers are designed following the specification of LVDS standard [18], to output the digital bits.

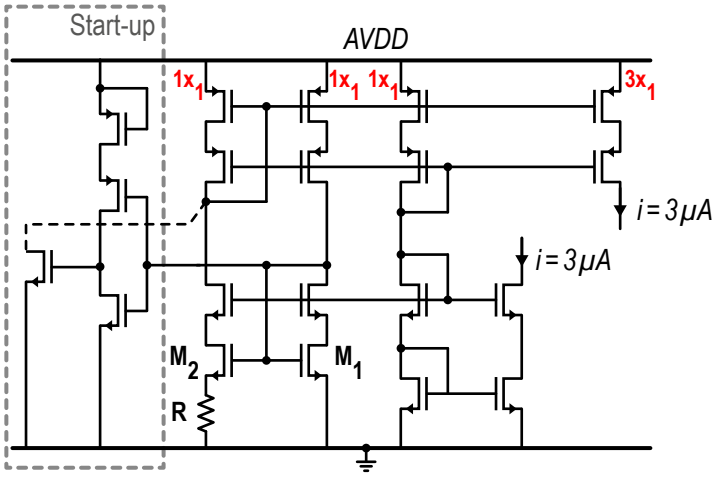

Figure 4.11: Constant-g_m generator circuit

4.4 Simulation Results

Table. 4.1 shows the current consumption of the various blocks at $T = 300\,\mathrm{K}$, post extraction for the typical corner, over a 1.8 V supply.

Table 4.1: Current consumption

Block	**Current (μA)**
OTA1	48
OTA2	6
β - multiplier + bias circuits	15
SAR ADC	12
Digital (Clock generator, digital BE)	40
Total	121

Figure. 4.12 shows the thermal noise spectral density of just the ΔΣM (without the SAR ADC) in a closed loop periodic-noise simulation (P-Noise), using the techniques proposed in [19]. It shows a low 1/f noise corner or around 0.8 Hz, suppressed due to CDS and the gain of the OTAs. Fig. 4.13 shows the results of two transient simulations. The blue PSD is the result of a transient-thermal noise simulation of the post-extracted netlist, whereas the black PSD is the same without thermal noise, effectively showing the quantization noise. The simulated results fit well with calculations, except for a higher 3^{rd} harmonic in the latter. This can be neglected as it is below the thermal noise floor and

does not affect the SNR.

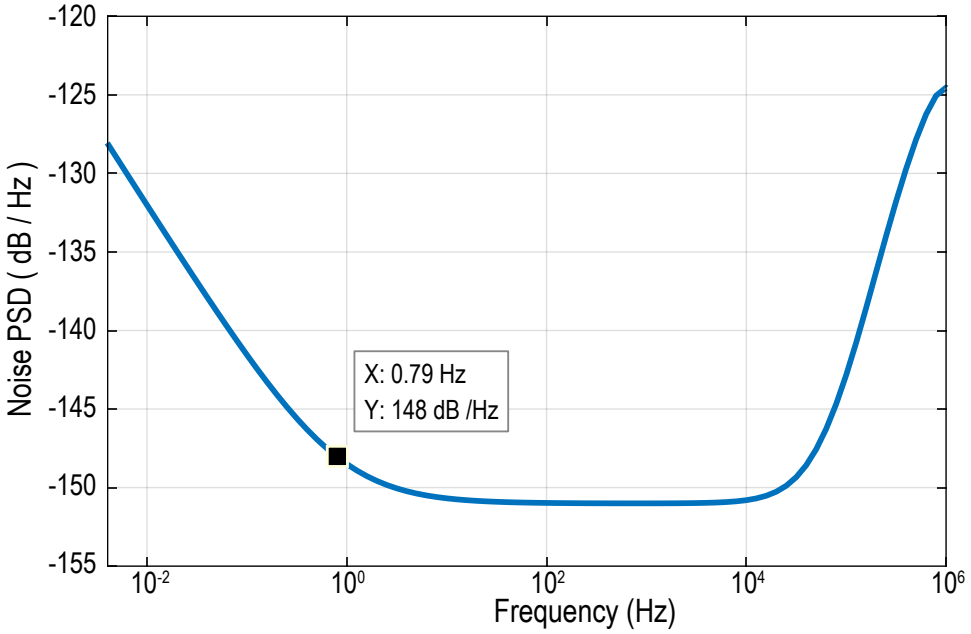

Figure 4.12: Periodic noise simulation result

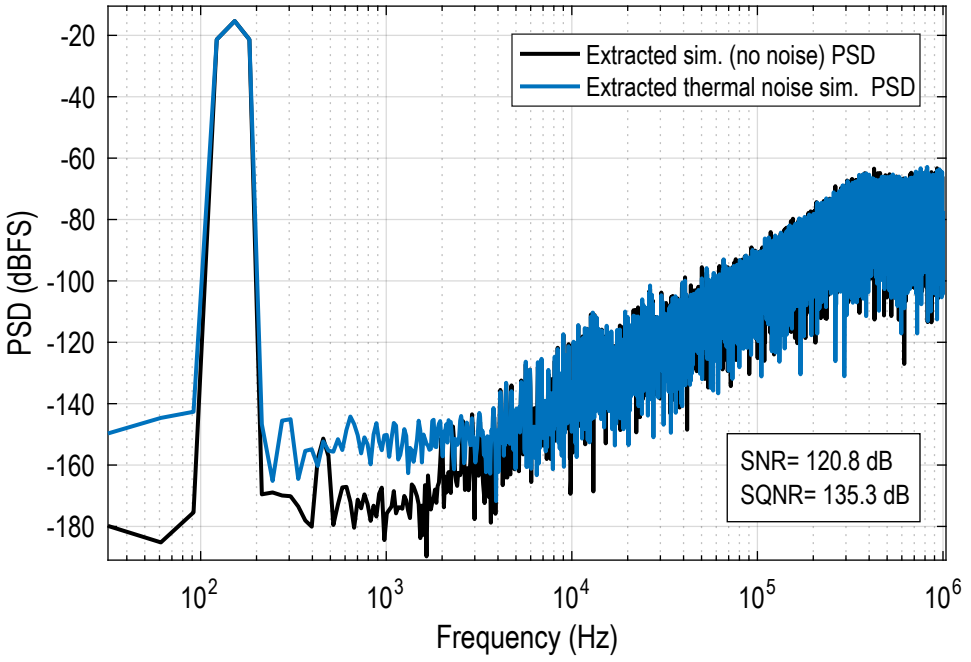

Figure 4.13: Transient simulation results

Chapter 5

Measurements and Evaluation

Since this prototype targets state-of-the-art specifications that have never been measured before, it is necessary to ensure that its performance is not degraded by the off-chip components, power supplies and signal generators, and the printed circuit board (PCB).

5.1 Measurement Setup

The three most critical signal networks of the ADC are its inputs, references, and the outputs. Any coupling between either of them can degrade performance in terms of noise and distortion. The techniques described below are implemented to minimize this.

5.1.1 PCB Layout

A low impedance ground node is critical as it forms the reference node for every other signal. Hence, a dedicated ground plane is used in this board, with three separate layers for supplies and signals. A star connection of the ground nodes of the aforementioned critical signals, along with proper signal routing, ensures that the return current loops do not cross over and help in decoupling. Furthermore, the 5-bit output stream of the ADC is recorded using a National Instruments data acquisition card (DAQ) connected to a PC. Since a PC ground itself can have large digital current spikes, isolators are used to separate it from the PCB ground. Fig. 5.1 illustrates the above described PCB ground layout in a simplified block diagram of the measurement setup.

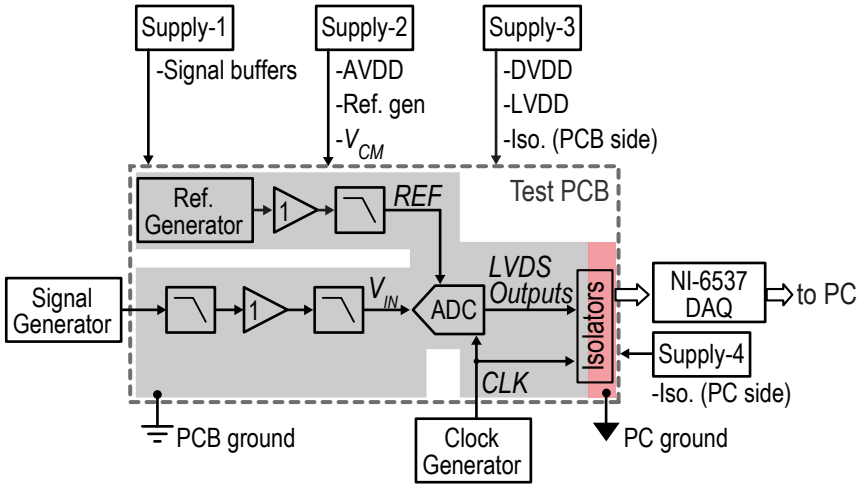

Figure 5.1: Simplified block diagram of the measurement setup with ground cuts

5.1.2 Signal Generator and Buffers

The output impedance of the input signal generator may not be able to drive a switched-capacitor load with the accuracy and speed required. The situation might worsen due to inductance of the long cable between the generator and the PCB. For high resolution measurements, it is therefore preferred to buffer the incoming signals from the generator before feeding it to the ADC. A similar argument holds for the on-board reference generator IC, and hence, that too is buffered. For a proper measurement, it is necessary that the overall noise contributed by both the generators and buffers be much lower than the ADC's noise floor.

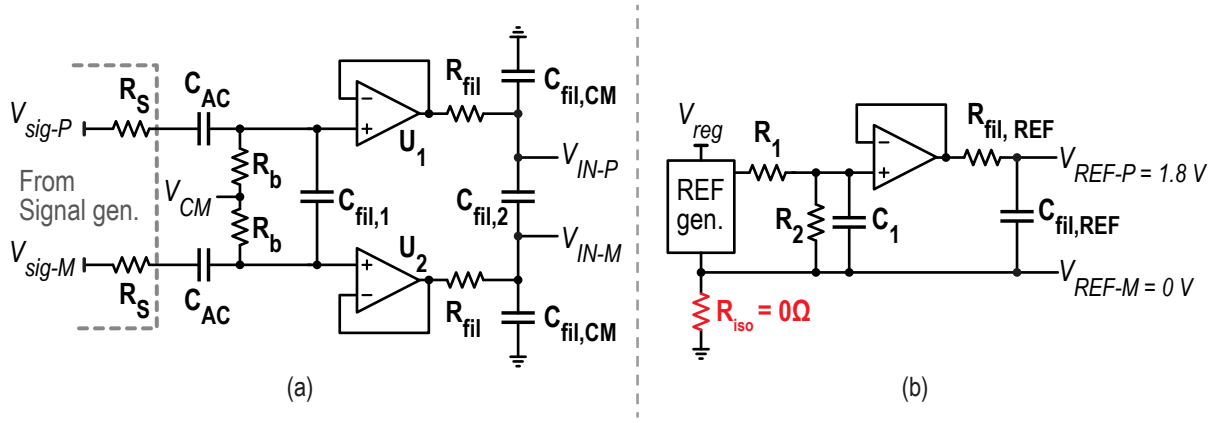

Figure 5.2: Signal buffer schematics- (a)inputs; (b)reference

Fig. 5.2 shows the buffer circuits implemented for the input and reference voltages. For the inputs, two op-amps with high linearity and low noise are used in a pseudo differential configuration to drive the ADC. The source impedance R_S, and $C_{fil,1}$ filters the wideband noise of the generator and the input current noise of the amplifiers. At the output, a 1st order filter, set by R_{fil} and $C_{fil,2}$, is used to limit the fold back of the wideband noise. $C_{fil,CM}$ helps filter the common mode noise. The circuit is biased for a common mode voltage $V_{CM} = 0.9\,\mathrm{V}$, derived separately. The circuit shown in (b) is used to buffer the reference voltage of the ADC. The linearity of this amplifier is not critical as the reference voltage is a DC signal, but the noise and bandwidth are. Since both the input and reference buffers are connected to the same switched-capacitor load, an incomplete voltage settling by either will result in distortion. The bandwidths of the output stage filters are therefore optimized to allow for sufficient voltage settling while limiting the fold back noise. The cut-off frequencies for the input and reference buffers are set at 2.3 MHz and 10 MHz respectively. The negative reference- V_{REF-M} is not directly connected to ground, but through a $0\,\Omega$ resistor at an isolated point.

5.1.3 Supply Regulators and Passive Components

Separate linear voltage regulators are used for input amplifiers, reference generator and amplifier, 3x VDDs, and isolators. The PSRR of these regulators and amplifiers, along with additional bypass capacitors placed close to the ADC, helps reduce noise and decouple signals from the supply lines.

Passive components can sometimes be a potential source of non-linearity as well. Large footprint thin metal film resistors and polypropelene dielectric capacitors were used in the signal path due to the high linearity they offer.

5.2 Measured Performance

The dynamic zoom ADC is realized in a standard CMOS 160 nm process and occupies an active area of 0.25 mm^2. Fig. 5.3 shows the die micrograph of the IC. It draws 154.5 µA (88 µA analog, 42 µA digital, and 24.5 µA references) from a 1.8 V supply.

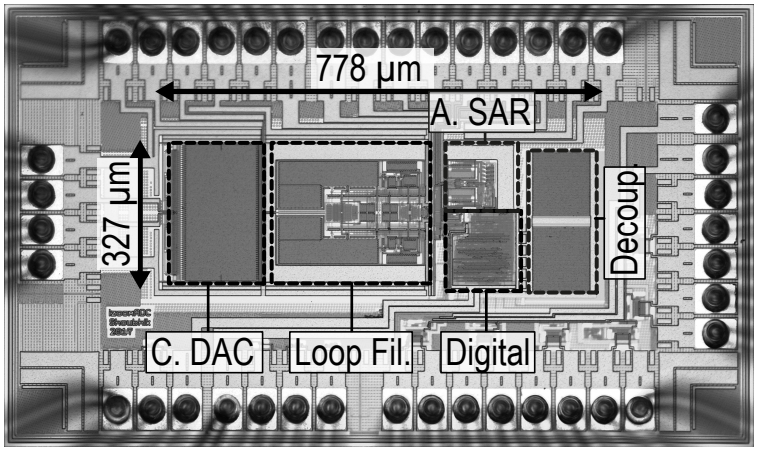

Figure 5.3: Die micrograph of the dynamic zoom ADC

5.2.1 Dynamic Performance

An input frequency of 152 Hz is used for characterization, to account for at least six harmonics while assessing distortion performance. The ADC achieves a peak SNDR of 118.1 dB with a 0.95 V_{FS} input signal, the output spectrum of which is shown in Fig. 5.4. This value is slightly lower than the target specification of 120 dB, as simulated earlier. The degradation in SNDR can be attributed to the off-chip buffer amplifiers not being able to drive the filter cap ($C_{fil,2}$), causing it to slew and distort the signal. The ADC's spectrum also shows a slightly higher noise floor when compared to the case with its inputs shorted and is more prominent at frequencies below 100 Hz. This may be due to the folded back noise of the amplifiers or the noise from the generator itself.

The spectrum shows skirts around the signal, due to clock jitter. However, being a fundamental limitation to any sampled system, the corresponding noise bins were avoided and the bandwidth lost due to them was accounted for by extrapolating the noise power.

The sharp tone at $f_S/2$ and others at lower frequencies, when the inputs are shorted, are due to the lack of randomization in the ΔΣM and DWA logic. The *fuzz* visible above 2 kHz is due to the fact that the output spectrum is the result of adding the SAR ADC's output which contains wide-band quantization noise to the fine ΔΣM's output, which is processed by the low-pass ΔΣM signal transfer function. Being a signal-processing artifact, it does not cause intermodulation issues and is suppressed by the ADC's decimation filter.

Fig. 5.5 shows the variation of SN(D)R and total harmonic distortion (THD) with input amplitude. The ADC has a peak SNR, peak SNDR, and peak THD of 119.1 dB, 118.1 dB

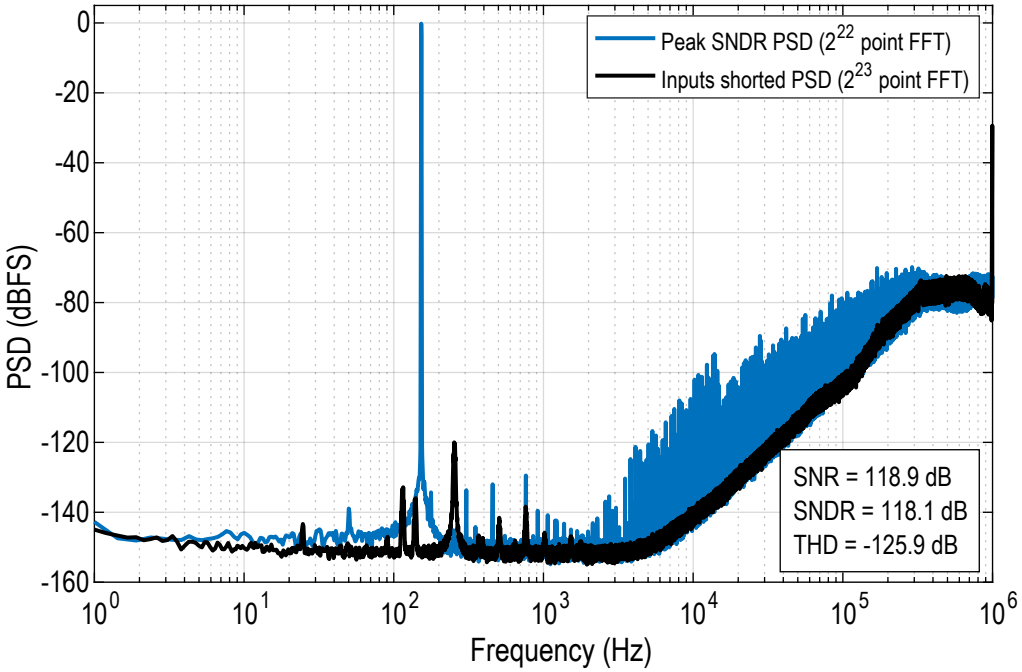

Figure 5.4: Measured output spectrum of the zoom ADC at peak SNDR and with inputs shorted

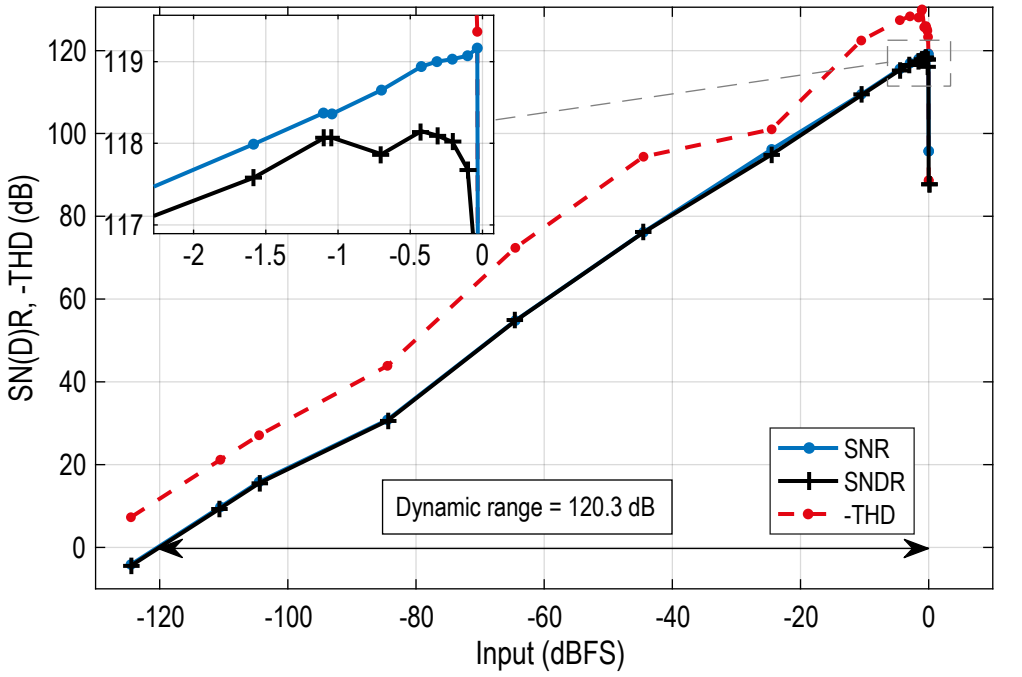

Figure 5.5: SN(D)R and THD versus input signal amplitude ($f_{IN} = 152\,\text{Hz}$)

and −129.9 dB respectively. The measured dynamic range of the ADC is 120.3 dB. It can also be seen that the performance is mainly limited by thermal noise as the THD is significantly better than the SNR.

5.2.2 Supply Rejection

A power supply rejection test is carried out by feeding a 100 mV_{PP} sine wave over a 1.8 V analog supply (AVDD) while keeping inputs shorted. The power supply rejection ratio (PSRR), defined as,

$$\text{PSRR} = 20 \cdot log_{10}\left(\frac{V_{supply}}{V_{OUT}}\right) \tag{5.1}$$

is measured at different frequencies of the sine wave. Fig. 5.6 shows that this value is greater than 96 dB till 5 kHz, after which it has a 2^{nd} order roll-off, demonstrating the current-starved OTA's ability to reject inband signal or noise from the supply.

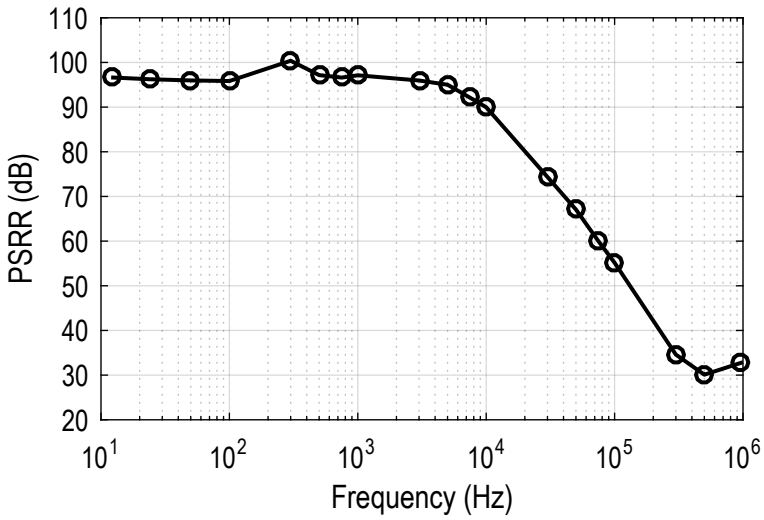

Figure 5.6: PSRR of the dynamic zoom ADC

5.2.3 Static Performance

Fig. 5.7 shows the spread in offset voltage from 10 different samples. A maximum value of 30 µV suggests that the CDS scheme is effective in suppressing the offset arising due to mismatch in component parameters. The 1/f noise corner is at 7 Hz and is measured by taking multiple (32×) averages of a 2^{23}-point FFT with the inputs shorted.

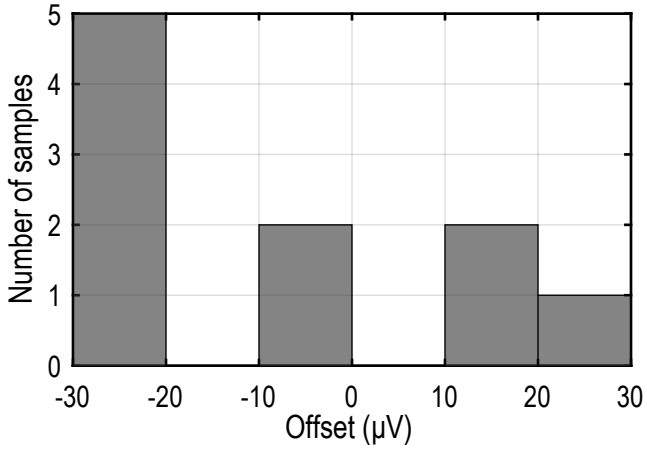

Figure 5.7: Measured offset histogram (10 samples)

5.2.4 Immunity to Interferers

To assess the asynchronous SAR ADC's signal tracking capability, a −1.5 dBFS input signal is applied and its effect on the ADC's noise floor is monitored while varying its frequency. Fig. 5.8 shows that the integrated inband noise power remains undisturbed with input frequencies as high as 48 kHz, making the dynamic zoom ADC immune to out-of-band interferers. This advancement in the zoom ADC, to track signals 48× the signal

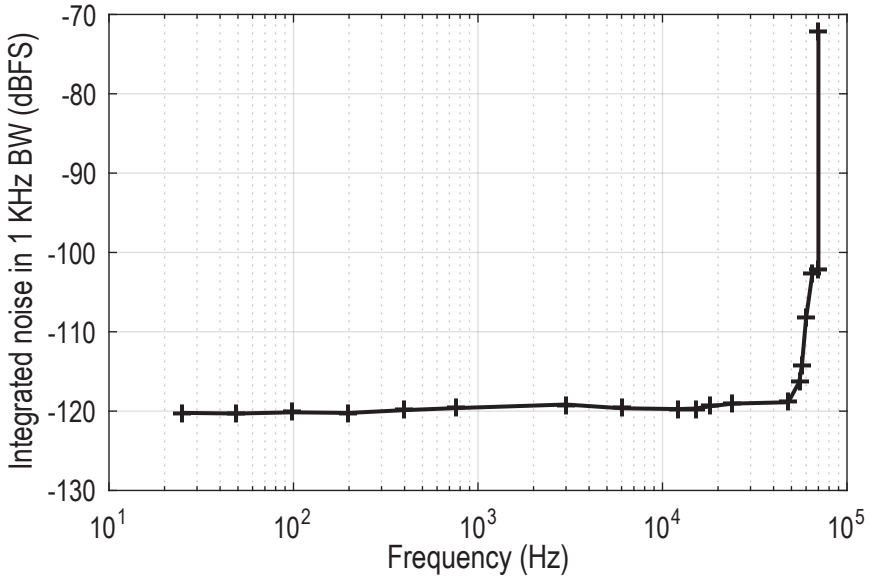

Figure 5.8: Inband integrated noise vs. frequency of input signal (−1.5 dBFS)

bandwidth, is a drastic improvement over [9], which could only handle signals up to 1.5x its bandwidth before its inband noise degraded; while also allowing it to be used with a more relaxed anti-aliasing filter.

5.3 Performance Summary and Comparison

Since most analog designs are a trade-off between energy consumption, precision and accuracy, and speed, several metrics exist to evaluate and compare their performance. For an ADC limited by its thermal noise, the most common figure of merit (FoM) is the Schreier FoM [2, 20], and given by,

$$FoM_S(\text{dB}) = DR + 10 \cdot log_{10}\left(\frac{BW}{Power}\right) \tag{5.2}$$

Based on the values determined by measurements, the FoM_S for this work is 185.8 dB. Table 5.1 summarizes the performance and compares it to other ADCs with similar resolution and bandwidth (SNDR $>$ 95 dB, BW $<$ 2 kHz). It outperforms all other

Table 5.1: Performance summary and comparison with state-of-the-art

Parameter	This Work	[5]	[6]	[7]	[8]
Year	2017	2016	2017	2016	2013
Tech (nm)	160	55	180	350	160
Area (mm^2)	0.25	0.072	0.27	11.5	0.375
Supply (V)	1.8	1.2	1.5	5.4	1.8
Power (µW)	280	15.7	33.2	12700	6.3
f_S(MHz)	2	1	0.64	0.64	0.05
Bandwidth (kHz)	1	1	1.2	1	0.013
Offset (µV)	30	-	-	-	1
SNR_{max} (dB)	119.1	104	97.1	-	119.8
$SNDR_{max}$ (dB)	118.1	101	96.6	-	-
THD_{max} (dB)	-129.9	-	-	-116	-
DR (dB)	120.3	101.7	100.2	136.3	119.8
FoM_S (dB)	185.8	179.7	175.8	185.3	182.7

designs in terms of peak SNDR, measured DR, and the Schreier FoM, and thus, demonstrates the effectiveness of the zoom ADC to convert low bandwidth signals with high resolution in an extremely energy efficient manner.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, an energy efficient dynamic zoom ADC, to convert low frequency signals with a high resolution, is presented. Using a top-down design approach, system level variables are defined to meet the specifications for the application, while at the same time, overcoming the limitations of its predecessors and other conventional high resolution ADCs. Possible error sources are tackled, following which, the individual blocks are implemented at a transistor level. The design is simulated at the transistor level, post-extraction, and taped out in a standard CMOS 160 nm technology. A measurement setup was developed to characterize the IC and evaluate its performance.

Measurement results support the theory and simulations, limited only by the measurement setup, and meet the target specifications. The asynchronous SAR demonstrates its ability to track high frequency signals, increasing the zoom ADC's immunity to out-of-band interferers. Tight over-ranging relaxes the loop filter and simplifies OTA's design. Although certain aspects such as power consumption and 1/f noise corner are slightly higher than simulated, the dynamic zoom ADC achieves state-of-the-art performance with regards to several essential parameters.

Fig. 6.1 shows the energy efficiency ($^{Power}/_{2BW}$) vs. peak SNDR performance of ADCs published in the two most reputed conferences over the years. The bold green line represents an FoM_S of 180 dB, where SNDR is used instead of DR in Eq. 5.2 to account for the distortion performance. This line determines the bound that defines state-of-the-art performance in recent years. The work presented in this thesis clearly crosses over, demonstrating that the dynamic zoom ADC can offer state-of-the-art

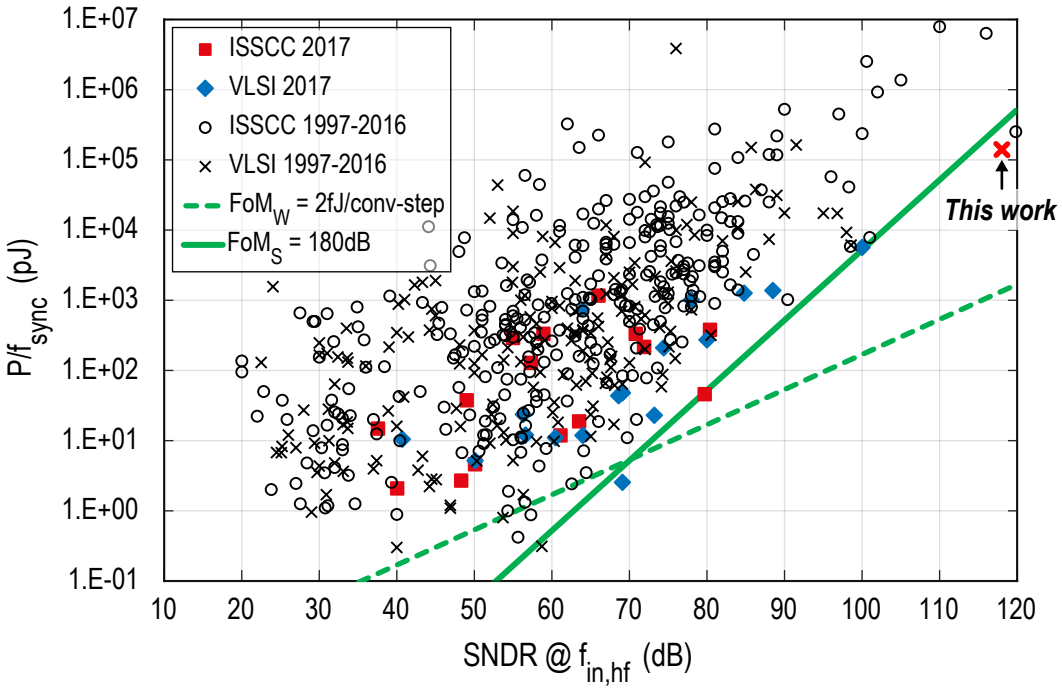

Figure 6.1: Energy efficiency vs. peak SNDR performance [1]

performance and robustness in low-bandwidth high-precision applications.

6.2 Future Work

While the measured offset is sufficiently low due to the CDS scheme, in many applications an offset lower than 1 µV is desirable. This can be achieved by simply operating the dynamic zoom ADC in an incremental manner and implementing system level chopping, as in [8]. However, since most switched-capacitor ADCs require the use of buffers to drive them, the overall offset is limited by the offset of these buffers.

An elegant solution would be to use clocked coarse amplifiers to buffer the inputs to the sampling capacitors. These amplifiers would be on only for a very short duration, to supply the bulk of the charge and prevent loading the inputs. Since the capacitors would be tracking the signal through conventional resistive switches for most of the tracking phase, the overall noise and offset sampled would be more or less independent of the amplifier. An incremental operation, followed by system level chopping, on this system would remove any residue offset and 1/f noise without the need for additional buffers.

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