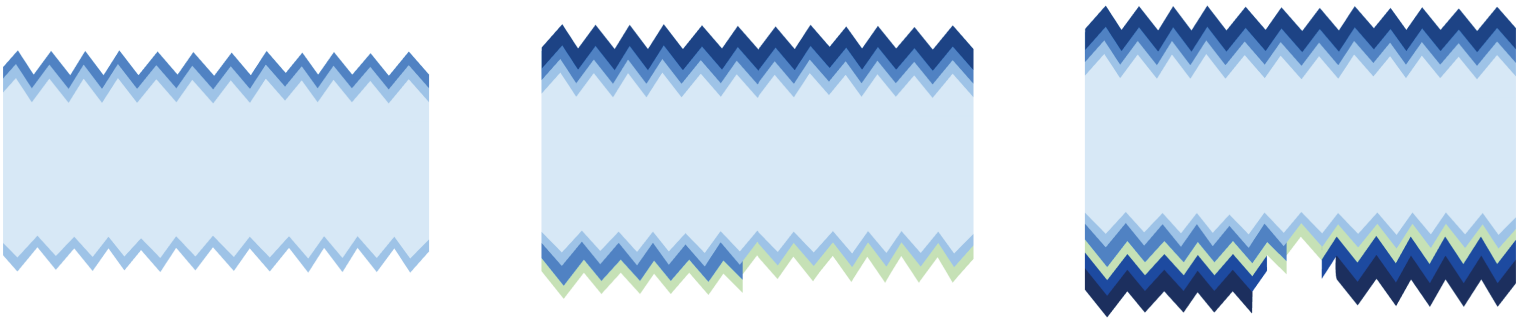
Simplified processing of interdigitated-back-contacted silicon heterojunction solar cells

Featuring novel MoO_x-based selective passivating contact stacks

Katarina Kovačević



TU Delft

Simplified processing of interdigitated-back-contacted silicon heterojunction solar cells

Featuring novel MoO_x-based selective passivating contact stacks

by

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Abstract

Silicon heterojunction (SHJ) solar cells are one of the most promising PV technologies nowadays due to high photoconversion efficiencies and low manufacturing costs. However, standard front/back-contacted (FBC) solar cells feature a front metal grid that brings shading to the front side of the devices, which limits the conversion efficiency of solar cells. One solution is to move metal contacts fully to the back by introducing interdigitated-back-contacted (IBC) architecture. In 2018, IBC-SHJ solar cells achieved a photoconversion efficiency of 26.7% holding a record for single-junction c-Si cells. However, the standard fabrication process of IBC solar cells comes with increased complexity and manufacturing costs. The focus of this research is on developing and optimizing a simple and industry-appealing fabrication process for high-efficiency IBC-SHJ solar cells.

The first part of the project investigates the simple processing of IBC-SHJ solar cells featuring tunneling recombination junction (TRJ). The first tunneling IBC devices are fabricated successfully with an efficiency of 13.90%. However, shunting is observed from the J-V curves of fabricated devices, which can be related to the internal shunting of tunneling IBC architecture and high lateral conductivity of *p*-type nc-Si:H-based blanket layer. Hence, alternative contact stacks are designed for application in the previously developed flowchart with the aim to minimize the lateral conductivity of the blanket layer and keep the fabrication process simple. MoO_x with low lateral conductivity is proposed as an alternative to *p*-type nc-Si:H-based blanket layer. Thus, in the proposed device architecture, hole transport takes place through MoO_x layer, whereas electron transport is achieved through a novel contact stack consisting of (*n*)nc-Si:H and MoO_x.

The proposed hole collection contact stack is firstly implemented in the front junction (FJ) FBC solar cells. The FJ FBC devices reach V_{OC} of 704 mV and FF of 79.29% with hole collector consisting of (*i*)a-Si:H and MoO_x with an intermediate plasma treatment (PT). On the other hand, rear junction (RJ) FBC solar cells are fabricated featuring a novel electron collection contact stack that is developed within this thesis. V_{OC} of 715 mV and FF of 82.24% are obtained in RJ devices with 50 nm (*n*)nc-Si:H and MoO_x without PT. The results of RJ FBC solar cells with newly developed contact stack show excellent results in terms of FF, making it a promising candidate for further application in IBC devices.

The introduction of the optimized device design enabled the successful fabrication of IBC solar cells with the simple process developed for tunneling IBC devices while ensuring no shunting occurs. The initial IBC-SHJ solar cells featuring novel MoO_x-based selective passivating contact stacks reach an efficiency of 12.88%. Further optimization of the thickness of MoO_x and PT conditions is executed to investigate the effect of these parameters on V_{OC} and FF. According to the results of the experiments, the optimal thickness of MoO_x is below 5 nm with the current process conditions, whereas the incorporation of PT appears necessary for an improved hole collection, thus also enabling higher FF in the devices.

Contents

Nomenclature

Abbreviations		**Unit**
ARC	Anti-reflection coating	
BSF	Back surface field	
DST	Double-side-textured	
ETL	Electron transport layer	
EQE	External quantum efficiency	[-]
IQE	Internal quantum efficiency	[-]
FBC	Front/back-contacted	
FJ	Front junction	
FSF	Front surface field	
FZ	Float zone	
HPT	Hydrogen plasma treatment	
HTL	Hole transport layer	
IBC	Interdigitated-back-contacted	
ITO	Indium tin oxide	
IWO	Indium tungsten oxide	
MCD	Minority carrier density	[cm^{-3}]
PECVD	Plasma enhanced chemical vapor deposition	
PVD	Physical vapor deposition	
PT	Plasma treatment	
RF	Radio frequency	
RJ	Rear junction	
SHJ	Silicon heterojunction	
SRH	Shockley-Read-Hall	
SST	Single-side-textured	
TCO	Transparent conductive oxide	
TMO	Transition metal oxide	
TRJ	Tunneling recombination junction	
VHF	Very high frequency	
WF	Work function	[eV]

Letters		
E_a	Activation enegy	[meV]
E_F	Fermi energy	[eV]
E_G	Band gap	[eV]
FF	Fill factor	[%]
I_{ph}	Photocurrent	[A]
iV_{OC}	Implied open-circuit voltage	[mV]
J_0	Saturation current density	[mA/cm^2]
J_{SC}	Short-circuit current density	[mA/cm^2]
$J_{SC,\ EQE}$	Short-circuit current density calculated from EQE measurements	[mA/cm^2]
pFF	Pseudo fill factor	[%]
R	Reflectance	[-]
R_S	Series resistance	[Ωcm^2]
$R_{S,\ SunsVoc}$	Series resistance calculated from SunsV_{OC} measurements	[Ωcm^2]

R_{SH}	Shunt resistance	[Ωcm^2]
V_{OC}	Open-circuit voltage	[mV]
η	Photoconversion efficiency	[%]
λ	Wavelength	[nm]
τ_{eff}	Effective minority charge carrier lifetime	[µs]
σ_{dark}	Dark conductivity	[S/cm]

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Introduction

1.1. Status and perspectives of solar energy

The increase in energy demand is one of the main challenges of the 21st century leading to a number of social and environmental concerns such as resource depletion, energy shortages, and climate change [1]. Predictions of global population growth of 2 billion by 2050 indicate a further increase in energy demand and related problems. Such problems are considered the most important drivers for the sustainable energy transition [2]. With the sun being an abundant energy source, solar energy plays a significant part in the energy transition as a possible alternative to traditional energy sources [3]. Photovoltaic (PV) technology, which converts solar energy to electricity, is currently considered a crucial renewable energy technology with a sharp increase in capacity installations over the past decade [4]. In 2021, newly installed PV capacity reached 183 GW, which is an increase of almost 40 GW compared to 2020 (Figure 1.1).

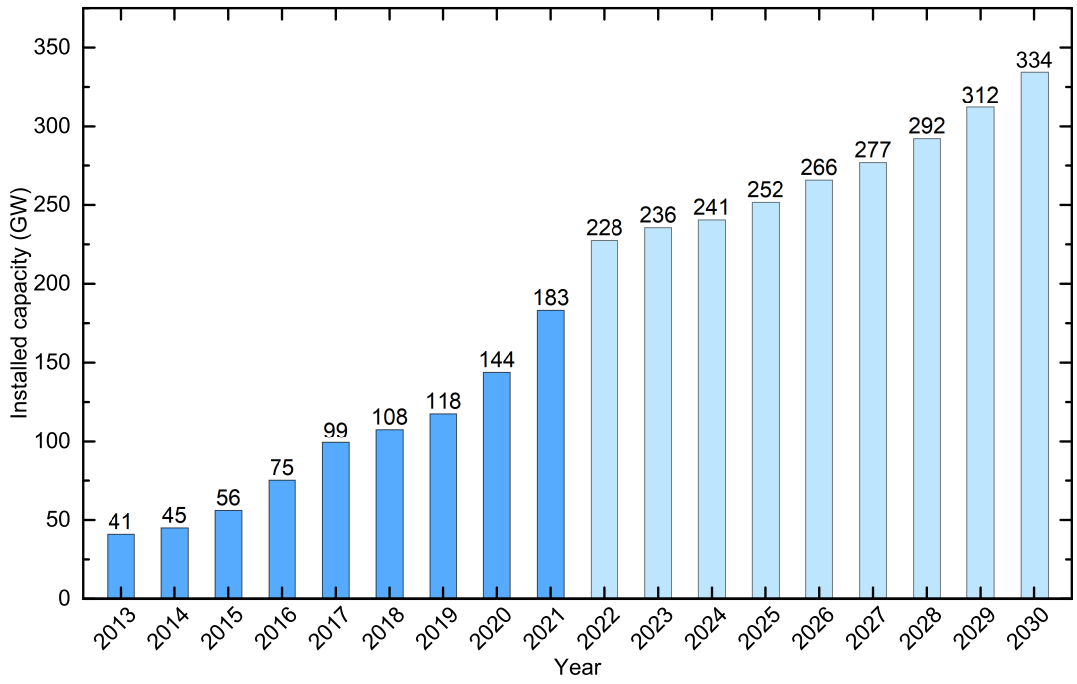


Figure 1.1: Global PV installation estimate (blue) and forecast (light blue) as of January 2022 [5].

Moreover, in March 2022 global installed PV capacity reached 1 TW, marking the start of the terawatt age for photovoltaics [6]. As shown in Figure 1.1, yearly installations are expected to further increase in the coming years as a result of a decrease in energy production costs [5]. Crystalline silicon (c-Si) modules represent the majority of PV modules produced and installed up to date, which can be ascribed to the abundance of silicon in nature and fast increase in volume manufacturing [7]. The trends of cost decrease and efficiency improvements of c-Si photovoltaics are expected to continue, ensuring that this

PV technology prospers as a global energy source playing a vital role in the decarbonization of energy systems and climate change mitigation [7].

1.2. Silicon heterojunction solar cells

Silicon heterojunction (SHJ) solar cells are one of the most promising PV technologies nowadays due to low manufacturing costs and high photoconversion efficiencies. In June 2022, LONGi reported the new record efficiency for front/back-contacted (FBC) SHJ device of 26.5% [8]. Previous record efficiency of 26.3%, also held by LONGi, was achieved as a result of improved passivation quality, decrease in contact resistance and use of a (n)µc-Si:H window layer [9]. Optimization of these parameters enabled enhancement of V_{OC}, FF and J_{SC}, respectively. Moreover, the highest certified photoconversion efficiency of single-junction c-Si cells was achieved by Japanese Kaneka Corporation in 2018, reaching an efficiency of 26.7% with interdigitated-back-contacted (IBC) SHJ device [10], [11]. In Figure 1.2, recent progress of SHJ devices is shown. Despite the later development of SHJ technology compared to other c-Si solar cells, SHJ devices have shown world record efficiencies in the past decade due to the use of passivating contacts. Namely, upon generation of charge carriers, it is important to efficiently collect them with minimal recombination losses. SHJ cells achieve excellent results due to the use of passivating contacts that allow the reduction of recombination at the surface of the silicon absorber. Typically, an intrinsic hydrogenated amorphous silicon layer ((i)a-Si:H) is deposited on both sides of the silicon absorber to reduce defect density, followed by the deposition of (n)a-Si:H and (p)a-Si:H layers. Doped layers induce band offset at c-Si/a-Si:H interface enabling selective carrier collection. Together, intrinsic and doped layers serve as selective passivating contacts allowing high V_{OC} (730mV – 750mV) [12], [13].

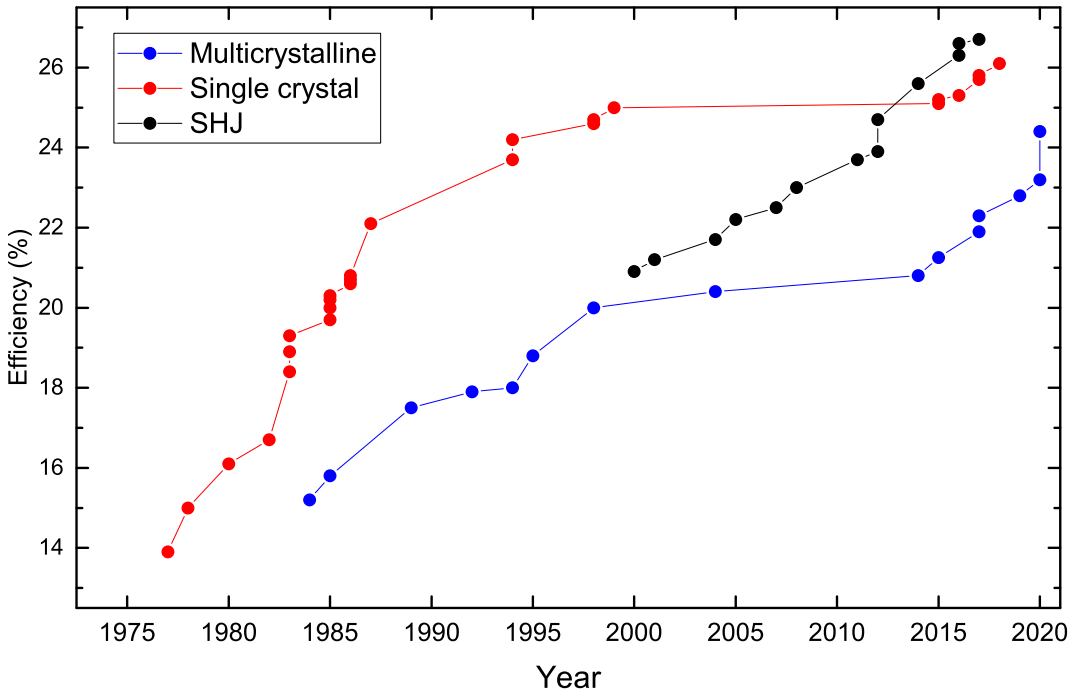


Figure 1.2: The best efficiency developments of c-Si solar cells [14].

In Figure 1.3 typical architecture of double-side-textured (DST) FBC-SHJ device is presented. As mentioned above, (i)a-Si:H layers are deposited on both sides of c-Si absorber. On top of the intrinsic layer, n- and p-type silicon layers are deposited serving as semipermeable membranes for electron and hole collection, respectively. On the front side, transparent conductive oxide (TCO) is deposited to improve lateral transport of charge carriers, while also serving as an anti-reflection coating (ARC). On the rear side, the TCO layer is deposited with the main purpose of preventing spiking during contact formation and maximizing the internal reflectance [15], [16]. The last step of SHJ device manufacturing involves the formation of metal contacts that allow the connection of the device to the external circuit.

Unlike the traditional solar cells that use *p*-type wafers, SHJ devices are typically made on *n*-type c-Si absorber due to lower price, lower light degradation and its better tolerance for impurities [3]. Moreover, results of SHJ cells based on *p*-type c-Si absorber show lower performance than their *n*-type counterparts [16], [17].

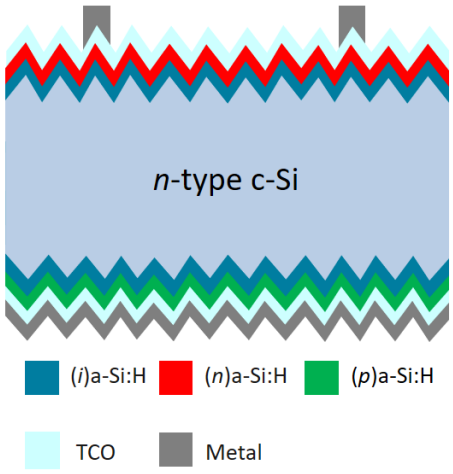


Figure 1.3: The structure of a typical FBC-SHJ solar cell with a-Si:H layers.

However, one of the limitations of FBC solar cells in general is lower J_{SC} due to the shading by the front metal contacts. Lower light absorption due to shading and resulting limitation in J_{SC} directly influence photoconversion efficiency of the devices. In the case of FBC-SHJ solar cells, additional losses are caused by the parasitic absorption of front TCO and front Si layers.

1.3. Interdigitated-back-contacted solar cells

By placing both electron and hole collection contact stacks on the rear side of the device and allowing the removal of the front metal grid and TCO, IBC cells offer a solution for above mentioned J_{SC} limitations and provide an improved cell performance. Moreover, front Si layers in IBC devices are only used for passivation purposes and, therefore, they can be optimized to decrease parasitic absorption and to serve as an ARC. Figure 1.4 shows a schematic representation of standard and tunneling IBC-SHJ.

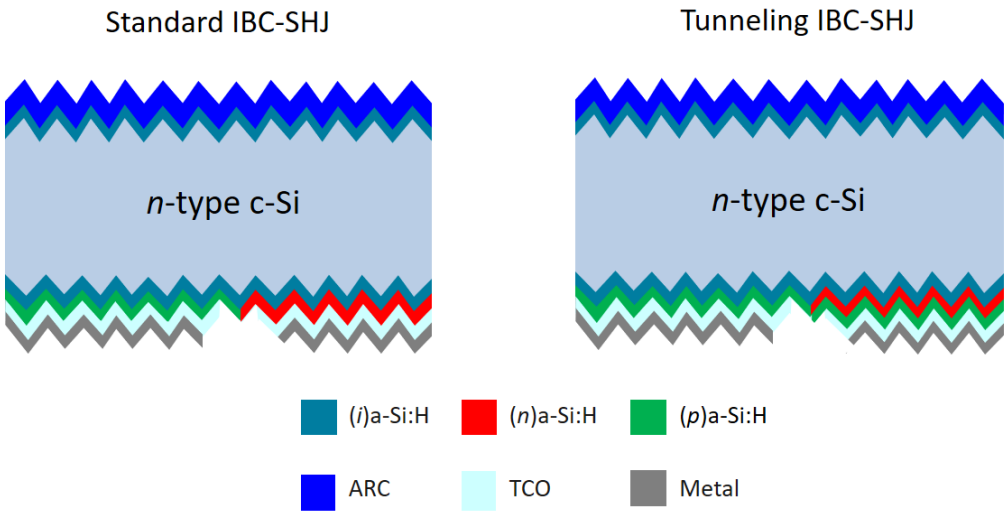


Figure 1.4: The structure of standard (left) and tunneling (right) IBC-SHJ solar cell with a-Si:H layers.

In the case of the standard IBC device, (*p*)a-Si:H layer is used as an emitter, whereas the (*n*)a-Si:H forms a back surface field (BSF). In order to ensure high V_{OC}, good passivation of both front and rear surfaces is obtained by deposition of high quality (*i*)a-Si:H. To secure high FF, it is important to ensure the good interface quality between intrinsic and (*p*)a-Si:H during the processing [18]. Moreover, low FF can be caused by the reduced area for electron and hole collection [19]. Therefore, it is important to carefully select the area and ratio of electron and hole collection regions. Lastly, High J_{SC} can be achieved by optimizing the front side of the device by introducing a transparent, dielectric layer (e.g. SiO_x) that acts as an ARC.

On the other hand, for a tunneling device (see Figure 1.4 (right)), the layer stack including (*n*)a-Si:H and (*p*)a-Si:H serves as BSF, while other aspects of the device are kept the same as in the standard IBC structure. This architecture is introduced as the standard fabrication process of IBC solar cells comes with high complexity and manufacturing costs [20]. The fabrication of tunneling IBC cells typically involves fewer patterning steps compared to the standard architecture, leading to lower manufacturing costs and a fabrication process that is more industry appealing and scalable.

Due to manufacturing defects such as imprecise patterning, significant power losses can occur in solar cells as a result of shunting. Namely, low shunt resistance provides an alternative path for the photogenerated current leading to power losses. In order to ensure high shunt resistance, in both standard and tunneling IBC devices proposed in this project, BSF and emitter are separated by 7 µm wide SiO_x gap. Even though this gap is expected to isolate electron and hole collection regions, due to relatively high lateral conductivity of *p*-type layer that is covering the full rear area of the cell, shunting can potentially be observed in tunneling devices. To overcome this problem, a layer with lower lateral conductivity can be introduced in place of *p*-type layers. As an alternative, so-called transition metal oxides (TMO) that act as carrier selective contacts can be implemented [21].

1.4. Transition metal oxides

Transition metal oxides (TMO) are an example of dopant-free materials that are characterized by low dark conductivity ($\sigma_{dark} = 2\times10^{-5}$ S/cm of MoO_x [22] compared to $\sigma_{dark} = 10^{-1}$ S/cm of (*p*)nc-Si:H [23]) [21], [24]. TMOs have lately gained a lot of attention in photovoltaic research, firstly in combination with organic semiconductors followed by applications combined with SHJ technology [25]. TMOs are characterized by a large span of work function (WF) values allowing them to act as carrier selective contacts in SHJ devices [22], [26], [27]. This is because the difference in WF values at TMO/Si interface induces band banding leading to enhanced transport of one type of charge carrier and acting as a barrier for the other. Low WF TMOs can be used as electron transport layers (ETL) replacing *n*-type silicon-based layers, while high WF materials can act as hole transport layers (HTL) in SHJ cells [25].

Owing to their high WF, the common TMOs used as hole transport layers (HTL) are molybdenum trioxide (MoO_3 with WF = 6.9 eV), vanadium pentoxide (V_2O_5 with WF = 7 eV) and tungsten trioxide (WO_3 with WF = 6.7 eV) [28]. Even though V_2O_5 is characterized by the highest WF among the three materials, MoO_3 with slightly lower WF is most commonly used as HTL in SHJ solar cells due to lower melting temperature allowing for simple deposition via thermal evaporation [28]. An important feature of MoO_3 is the high oxygen reactivity leading to the reaction of oxygen atoms from MoO_3 with the surrounding materials. Due to oxygen reactivity, sub-stoichiometric molybdenum oxide (MoO_x where x is in the range between 2 and 3) is deposited on the substrate [29]. Moreover, MoO_x FBC-SHJ devices have shown excellent results in the past. Solar cells with MoO_x as HTL on the front side and (*n*)a-Si:H as ETL on the rear side developed at PVMD group at the Delft University of Technology achieved conversion efficiency of 23.83%. During this project, contact stacks based on MoO_x have been further developed and implemented in an IBC device.

1.5. Research goals

Even though research on IBC-SHJ solar cells has yielded excellent results [10], [11], the manufacturing process is very complex, requiring extensive efforts for optimizing the process to minimize losses and ensure high device quality. Therefore, the development of a working process flowchart for obtaining high-efficiency devices can be particularly challenging.

To minimize the losses along the fabrication process of IBC-SHJ solar cells, two main research goals are

proposed. For each of the main research goals, sub-goals are defined to assist in efficiently achieving the research goals.

As the complex manufacturing of IBC devices involves potentially damaging steps leading to a decrease in device performance, the first main research goal of the project is:

1. Development and optimization of process flowchart for fabrication of high-efficiency IBC-SHJ solar cells.
   (a) Recognizing and resolving the main obstacles in the process flowchart hindering the successful fabrication of IBC-SHJ solar cells.
   (b) Identifying processing steps that lead to degradation in passivation quality of cell precursors and optimizing the damaging steps to preserve passivation quality.

Once the flowchart is developed and the working IBC device is fabricated, the focus will shift towards improving the performance of the devices. To achieve better performance, the second main research goal is proposed as:

2. Optimization of electron and hole collection layers of IBC-SHJ solar cells to fabricate high-efficiency solar cells.
   (a) Identifying the main physical properties of electron and hole collection layers required for cells to achieve high V_{OC} and FF.
   (b) Determining the main processing parameters that can be adjusted to fulfill the physical requirements.

1.6. Thesis outline

The key motivation for research on high-efficiency solar cells and specifically research on SHJ-IBC devices has been presented in Chapter 1. Subsequently, the main research goals of this thesis have been given.

Chapter 2 starts with an overview of the working principle of photovoltaic devices in general and introduces the fundamentals of SHJ technology, as well as the background on IBC architecture and the theory behind tunneling IBC devices. Moreover, in Chapter 2, the characteristics of materials used in fabricated devices and recombination and passivation mechanisms are covered. Chapter 3 introduces fabrication and characterization tools used during the work on this thesis. The results of FBC-SHJ devices used as proof-of-concept and the explanation and results of four main manufacturing approaches for IBC-SHJ devices with Si-doped layers are explained in Chapter 4. The main limitations of the attempted processes are highlighted, and the executed improvements and suggestions for future developments are described. In Chapter 5, alternative contact stacks are introduced in a simplified flowchart for the fabrication of IBC devices. The optimization of the IBC device structure and involved layers is covered in this Chapter. In Chapter 6, concluding notes and outlooks for future research are presented.

2

Fundamentals

This Chapter provides a theoretical foundation for the experimental study conducted in this thesis, as well as for the main assumptions and methods used in this work. Firstly, the basic principles of photovoltaic energy conversion are presented in Section 2.1. This Section focuses on the basis of semiconductor physics for solar cell applications with an emphasis on the fundamental limitations and recombination mechanisms. The concept and working principle of silicon heterojunction solar cells are described in detail in Section 2.2. Moreover, the properties of materials implemented in manufactured devices are addressed in this Section. Furthermore, IBC architecture is introduced in Section 2.3, focusing on its main advantages and limitations. Lastly, the working principle of TMO-SHJ devices is explained in Section 2.4.

2.1. Photovoltaic fundamentals

In this Section, the fundamental theory of photovoltaic energy conversion is presented. Section 2.1.1 briefly introduces the main characteristics of semiconductor materials, while Section 2.1.2 focuses on the working principle of a solar cell. Lastly, Section 2.1.3 covers the principal limitations of solar cells.

2.1.1. Semiconductor materials

Semiconductors are a group of materials with conductivity values falling between conductors and insulators [30]. The conduction in semiconductors occurs at energy states that are separated by a gap (band gap) where no electrons are allowed [30]. In order to participate in conduction, electrons must absorb enough energy to bridge the band gap between the valence (VB) and conduction band (CB). The absorbed energy can be taken from thermal energy of the surroundings or be a result of illumination. When an electron is excited from the valence to conduction band, it leaves a positively charged hole in the valence band. If the bottom energy of CB is defined as E_C and the top energy of VB as E_V, then the width of the band gap can be defined as E_G=E_C-E_V [3].

2.1.2. Working principle of a solar cell

The formation of a potential difference at the junction of two materials due to exposure to light, called photovoltaic effect, is the basis for solar cells' operation [3]. Photovoltaic effect starts with photon absorption in a material (absorber) that leads to excitement of an electron to a higher energy level as shown in Figure 2.1.

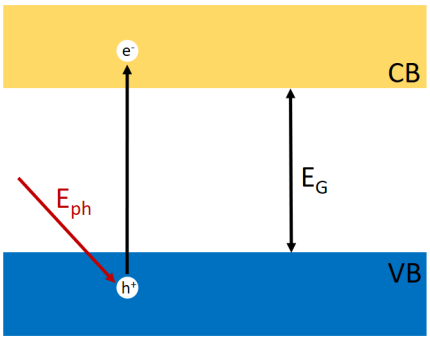


Figure 2.1: Schematic illustration of the photon absorption in a semiconductor with bandgap E_G. E_{ph} represents photon energy, CB represents conduction band and VB represents valence band [3].

The photon with energy (E_{ph}) larger than E_G of the absorber will excite an electron from VB to CB while leaving a positively charged hole in the valence band. In order to avoid recombination of the electron-hole pair, so-called semipermeable membranes formed by *n*- and *p*-type materials are placed on both sides of the absorber to selectively collect electrons and holes, respectively [3]. This is followed by the flow of charge carriers into an external circuit and their utilization in form of electricity. A simplified sketch of this process is shown in Figure 2.2.

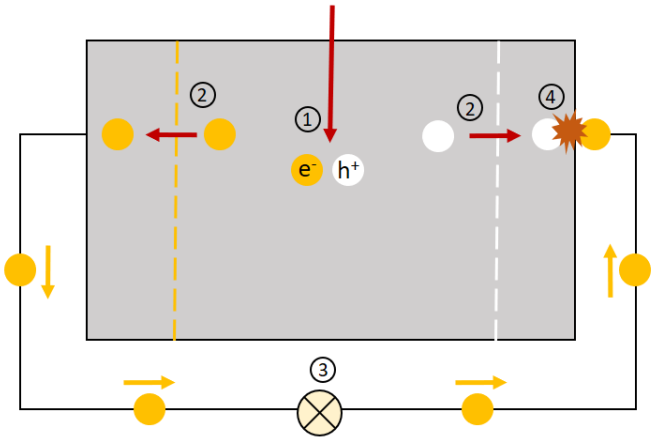


Figure 2.2: A simplified model of a solar cell showing (1) absorption of a photo leading to the generation of electron-hole pair, (2) separation of electrons and holes, (3) formation of an external circuit and (4) electron-hole recombination as the electrons pass through the circuit [3].

2.1.3. Fundamental limitations and recombination mechanisms

The fundamental losses of solar cells are highly dependent on E_G of the absorber [3]. Namely, the photons with energy lower than the E_G cannot be absorbed, while part of the absorbed photon energy, in the case of photons with energy above E_G, cannot be utilized and is released as heat. In the case of low E_G material, high current can be achieved, but high thermalization losses limit voltage values. On the other hand, high E_G absorber can generate high voltage, but current losses are high. An optimum E_G for the highest conversion efficiency can be found as a trade-off between current and voltage losses. E_G of c-Si is equal to 1.12 eV, which is slightly below the optimal value of 1.34 eV [3].

As explained in Section 2.1.2, electron-hole pairs are generated in the absorber as a result of illumination. The excitation of electrons to conduction band due to illumination induces a non-equilibrium state and the system will attempt to reestablish the equilibrium condition. This occurs through so-called recombination mechanisms. As a result, charge carrier collection is suppressed, lowering solar cell

performance. The recombination process has an effect on both the current and voltage of the solar cell, however the limitation it poses on the solar cell voltage is more restricting.

Depending on where the recombination takes place, two main sets of recombination mechanisms can be distinguished - bulk and surface recombination. Moreover, the characteristics of the material define the dominant recombination mechanism. Main recombination mechanisms in solar cells are radiative, Auger and Shockley-Read-Hall recombination.

Recombination mechanisms

The radiative recombination process, illustrated in Figure 2.3a, involves a band-to-band electron-hole recombination where an electron directly moves back to valance band and recombines with a hole [31], [30]. During this process, a photon with an energy close to E_G is released. The radiative recombination is a dominant mechanism in direct bandgap materials. As c-Si is an indirect bandgap material, a more significant recombination mechanism is Auger recombination.

The Auger recombination is a recombination mechanism that involves three particles (Figure 2.3b) [32]. In the Auger recombination process, the energy released during electron-hole recombination is transferred to the third carrier that can be either an electron or a hole. The third particle is then excited to higher energy levels, before returning to the edge of a conduction (or valence) band and releasing thermal energy. Recombination rate of the Auger recombination is dependant on doping concentration and at high doping levels it becomes more significant.

In the Shockley-Read-Hall (SRH) recombination process, recombination of electrons and holes is supported by an impurity atom or lattice defect [33], [34]. Impurities and defects introduce allowed energy level (E_T) within the band gap. An electron and a hole can be trapped at the same defect state where they recombine as shown in Figure 2.3c. Recombination rate is dependent on the location of the defects. In case the defect is located close to the valence or conduction band edge, the probability of recombination is lower. Namely, in case of the defect state close to the conduction band, the electron has a higher probability to move to the conduction band than to recombine with the hole that has to move from the valence band to the defect state. On the other hand, in case of the midgap defect state the recombination is more likely to happen making the SRH recombination more effective.

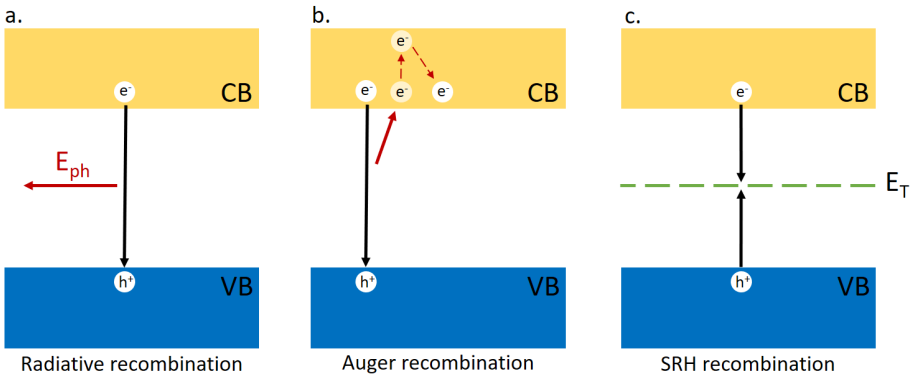


Figure 2.3: Schematic representation of (a) radiative, (b) Auger and (c) SRH recombination mechanisms [3].

The recombination mechanisms described above belong to bulk recombination mechanisms taking place in the bulk of a semiconductor. However, apart from the bulk recombination, the surface recombination can occur in semiconductor devices and, in low-defect semiconductors, it can be the dominant recombination mechanism [3]. Due to abrupt end of silicon crystal lattice and the breaking of covalent bonds, unpaired electrons are present at the silicon surface. The unpaired electrons are referred to as dangling bonds and they represent a surface defect which induces surface SRH recombination at high rate.

Effective minority carrier lifetime

Effective minority carrier lifetime (τ_{eff}) is described as the average time before minority carriers recombine with the corresponding majority carriers in a material [3]. τ_{eff} is commonly used to make an

estimate of the upper limit of V_{OC} of solar cells. The above mentioned recombination mechanisms influence the τ_{eff} as shown in Equation 2.1.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{surf}} \tag{2.1}$$

In the Equation 2.1, τ_{rad} is the lifetime due to the radiative recombination, τ_{Auger} is that due to the Auger recombination, τ_{SRH} is the lifetime due to the SRH recombination and τ_{surf} is the lifetime due to the surface recombination.

In the case of the high-quality Float Zone c-Si wafers that are used in this project, the recombination occurs mainly at the wafer surface and Equation 2.1 can be simplified to Equation 2.2.

$$\tau_{eff} \approx \tau_{surf} \tag{2.2}$$

The surface recombination can be reduced by saturating dangling bonds on the wafer surface [35]. This process is referred to as chemical passivation. As surface recombination plays a crucial role in determining the effective lifetime of solar cells and, therefore, the final performance of the fabricated devices, it is important to ensure good quality of surface passivation. During the work on this project and in order to ensure good performance of the final devices, the effective lifetime was followed throughout the process using photoconducance decay measurements as explained in Section 3.4.2.

Passivation mechanisms
The passivation quality is essential in the production of high-performance solar cells. Typically, two types of passivation mechanisms can be employed in solar cells - chemical and field-effect passivation [36], [37].

As mentioned above, chemical passivation mechanisms are introduced on the surface of the silicon wafer in order to saturate dangling bonds and consequently reduce the defect density at the interface. Wet chemical treatments are commonly used to minimize the defect density at the c-Si surface by removing the native oxide with an HF dip and forming bonds between the surface Si atoms and hydrogen [38]. The complete wafer cleaning and wet etching procedure used to minimize dangling bonds at c-Si surface as suggested by [39] are presented in Section 3.1.2. On the other hand, intrinsic hydrogenated amorphous silicon ((*i*)a-Si:H) can be deposited on the c-Si surface allowing excellent surface passivation as the dangling bonds are saturated [40], [41]. By deposition of (*i*)a-Si:H, high V_{OC} values can be achieved.

The field-effect passivation is a passivation mechanism that reduces the surface recombination by inducing a band bending at c-Si surface. As a consequence, the built-in electric field repels one type of charge carrier from the surface reducing the probability of recombination and improving the effective carrier lifetime. Dielectric materials such as SiO_2 can be introduced on the silicon surface to induce the field effect [42] but introducing non-conductive layers increases the design complexity. The field effect can also be achieved by introducing an optimized doped Si-based layer, that is introduced as front or back surface field or emitter in heterojunction devices [43].

In this research, both chemical and field-effect passivation methods are used in order to achieve low defect density at the absorber surface and improve selective collection of charge carriers. Wet chemical processing steps and deposition methods used for this purpose are explained in Chapter 3.

2.2. Working principle of silicon heterojunction solar cells

A heterojunction is a junction of two different semiconductors [30]. As the materials forming a heterojunction are characterized by different band gaps, work functions, and electron affinities, the band diagrams are more complex compared to that of a homojunction that features the same semiconductor material with different doping types (Figure 2.4a [44]). In the case of heterojunctions, as the Fermi level has to remain constant and the vacuum level continuous throughout the sample in the dark at thermal equilibrium, discontinuities at valence and conduction band are formed [30]. These discontinuities can represent a barrier for electrons and holes. In the case of SHJ solar cells, the heterojunction is formed between two different silicon-based materials [3]. SHJ is formed by depositing a-Si:H film on both sides

of the c-Si absorber. In Figure 2.4b [44] a schematic band diagram of SHJ solar cell with n-type c-Si absorber up to TCO layer is shown. The band bending at c-Si/a-Si:H interfaces represents barriers for electrons and holes and it is induced by different band gaps of c-Si (E_G = 1.12 eV) and a-Si:H (E_G = 1.6 - 1.8 eV).

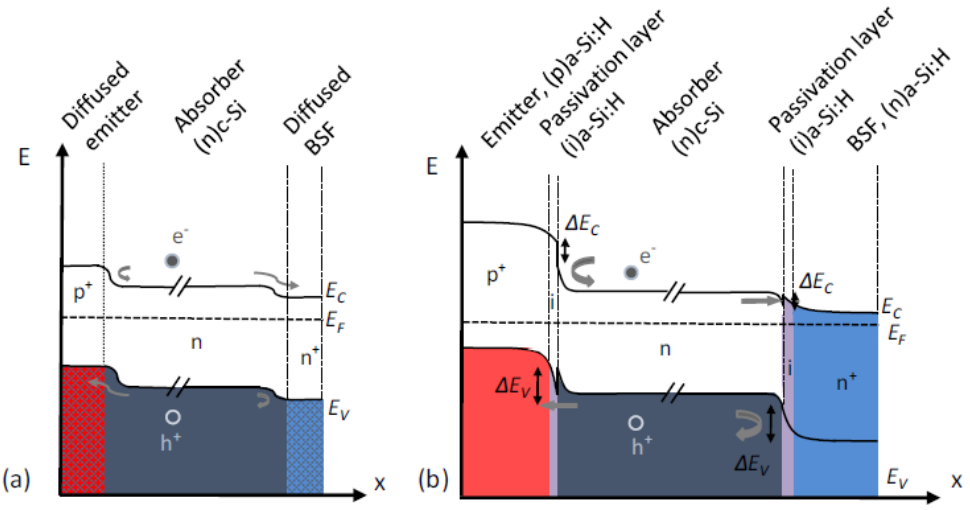


Figure 2.4: Band diagram of a (a) homojunction and (b) SHJ based on n-type c-Si absorber. E_C denotes the conduction band edge, E_V the valence band edge, E_F the Fermi level, e^- electrons, and h^+ holes. Adapted from [44].

While (i)a-Si:H layer ensures low defect density on the absorber surface, band bending induced by doped a-Si:H layers has a beneficial influence on charge carrier transport across the c-Si/a-Si:H interface. Together, good quality of chemical and field-effect passivation leads to a significant reduction in recombination losses compared to homojunction devices and high V_{OC} values can be reached [13].

In the case of SHJ solar cells, transparent conductive oxide (TCO) is deposited over doped Si layers on the front and rear side of the device prior to the deposition of metal contacts. As the doped a-Si:H layers have insufficient lateral conductivity, TCO is deposited to ensure lateral transport of charge carriers to the metal contacts at the front side of FBC devices where metal contacts are separated. In that case, TCO can be additionally optically optimized to serve as an anti-reflection coating (ARC). In the case of rear side TCO, it can prevent spiking during metal contact formation and maximize internal reflectance [16].

2.2.1. Hydrogenated amorphous silicon

As mentioned above, typical SHJ solar cells consist of c-Si absorber on which intrinsic and doped a-Si:H or nc-Si:H layers are deposited. In c-Si, every Si atom is tetrahedrally bonded to four other Si atoms [3]. As such structure is repeated throughout the material in long-range order, a homogeneous, highly structured crystal lattice with low number of defects is formed as shown in Figure 2.5 on the left. On the other hand, in the case of a-Si, the tetrahedral structure is only present in the short-range order as the bond between Si atoms is slightly distorted (Figure 2.5 right). In this distorted structure, some of the electrons cannot form bonds with surrounding Si atoms. The unbound electrons are known as dangling bonds [3]. Dangling bonds represent recombination centers allowing high rate of SRH recombination both in the bulk material, as well as at the a-Si/c-Si interface. In order to decrease the recombination rate caused by dangling bonds, hydrogen is incorporated during the deposition of a-Si as a way of passivating the dangling bonds. This way hydrogenated amorphous silicon (a-Si:H) is formed, as shown in Figure 2.5 on the right.

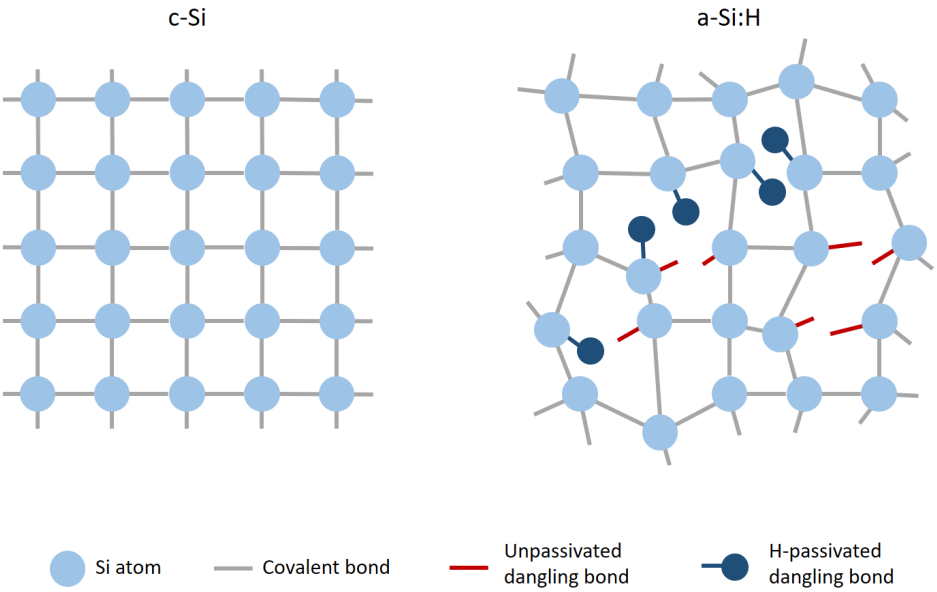


Figure 2.5: Schematic representation of crystalline silicon (left) and amorphous silicon (right) crystal lattice.

Growth mechanism of a-Si:H

a-Si:H is deposited using plasma enhanced chemical vapor deposition (PECVD) [45], which will be explained in detail in Section 3.2.1. For deposition of a-Si:H, silane (SiH_4) and H_2 precursor gases are used. As the SiH_4 collide with energized electrons in plasma, a series of reactions occurs producing different neutral radicals (SiH_3, SiH_2, SiH, Si, H). In the case of low power density (< 10 W/cm^2) and low pressure (< 10 Pa) conditions, SiH_3 radical, the main precursor for formation of low defect density a-Si:H, is the most abundant species within the mixture of products generated in plasma [46], [47], [48], [49]. Following the generation of radicals, transport and diffusion of radicals to the substrate occur. Lastly, the radicals react at the surface of the substrate forming a-Si:H layer.

A schematic representation of interaction of SiH_3 with hydrogen-terminated Si surface is presented in Figure 2.6 [45]. As the SiH_3 diffuses through plasma sheath towards the substrate surface, it can be weakly absorbed (physisorbed) at Si:H surface due to the low deposition temperature (< 200°C) where thermal energy is insufficient to break Si-H bonds. Once physisorbed, SiH_3 diffuses along the substrate surface and different processes occur during the diffusion. Processes such as desorption as SiH_3, recombination with another SiH_3, abstraction of H atom or formation chemical bonds with dangling bonds at Si surface can occur, where the last leads to a-Si:H layer growth on the surface of the substrate.

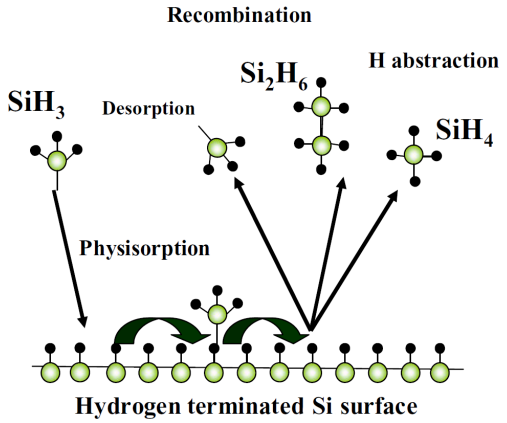


Figure 2.6: Schematic representation of a-Si:H growth on hydrogen-terminated Si surface. Adapted from [45].

As passivation of dangling bonds is not entirely accomplished by the above-explained mechanism, H_2 is included as a precursor gas during a-Si:H deposition. To avoid epitaxial growth of a-Si:H and ensure high quality of deposited layer, the ratio between H_2 and SiH_4 (hydrogen dilution ratio) [50] and deposition temperature [51] have to be carefully selected. Post-deposition hydrogenation step [41] or deposition of multiple layers [40] can be included to secure sufficient hydrogen content and avoid epitaxial growth, achieving better surface passivation. During this research, (*i*)a-Si:H layer is deposited in two steps, both at substrate temperature of 160°C. Firstly, (*i*)a-Si:H from pure SiH_4 with no additional H_2 is deposited in order to prevent epitaxial growth, followed by the deposition of the second (*i*)a-Si:H layer with SiH_4 and H_2. In the case of <111> textured surface, an additional hydrogen plasma treatment step is introduced following the deposition of (*i*)a-Si:H bilayer to include additional hydrogen in the layer.

2.2.2. Hydrogenated nanocrystalline silicon

As an alternative to a-Si:H doped layers, doped hydrogenated nanocrystalline silicon (nc-Si:H) layers can be deposited over (*i*)a-Si:H [3]. As shown in Figure 2.7, nc-Si:H is a material consisting of a crystalline phase embedded in the amorphous material. Just like for a-Si:H, hydrogen is used to passivate dangling bonds within the nc-Si:H bulk and ensure a lower SRH recombination rate. Moreover, hydrogen content plays an important part in the growth and quality of nc-Si:H material [52], as higher hydrogen content leads to a higher fraction of the crystalline phase. The growth of nc-Si:H is also highly dependent on the substrate, total thickness of the deposited layer, and inclusion of doping precursor gases for formation (*p*)nc-Si:H or (*n*)nc-Si:H [52].

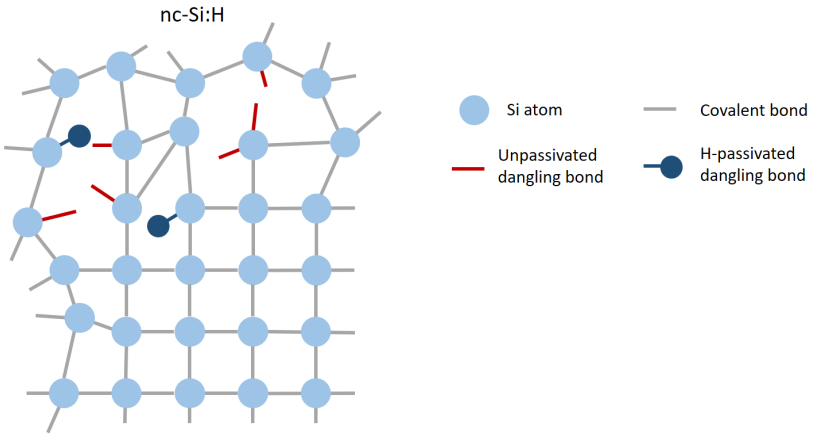


Figure 2.7: Schematic representation of nanocrystalline silicon.

Depending on these parameters, as well as on the deposition conditions, the structure of nc-Si:H layer can vary highly. The evolution of the structure through four phases from fully amorphous to highly crystalline can be observed within nc-Si:H layers [52], [53]. Figure 2.8 [44] shows the evolution of nc-Si:H layer. At the beginning of nc-Si:H growth a fully amorphous phase, the so-called incubation layer, is recognized. The thickness of the incubation layer is in the range of a few nanometers, however, it highly depends on the substrate. Following the incubation zone, the crystalline phase starts to form and the fraction of the crystalline phase increases with layer growth. To achieve faster nucleation and consequent stronger band banding at the c-Si/a-Si:H interface, it is important to minimize the thickness of the amorphous incubation zone for application in SHJ devices. This is particularly challenging as nc-Si:H layer grows on (*i*)a-Si:H layer which induces a thicker incubation zone leading to a reduction in the crystalline fraction of nc-Si:H layers [53]. By introducing a nc-Si:H seed layer [54], [55] or including CO_2 plasma [56], the thickness of incubation layer can be decreased.

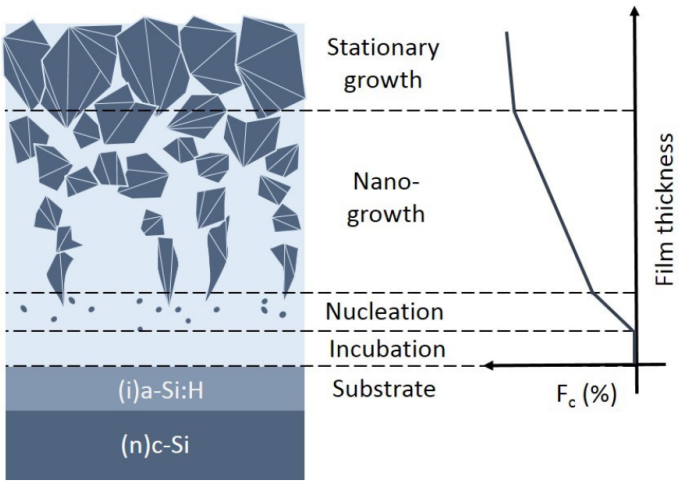


Figure 2.8: Schematic cross-sectional representation of nc-Si:H growth on c-Si substrate coated with thin (i)a-Si:H layer. Adapted from [44].

As the growth of nc-Si:H is highly dependant on the substrate, it is suitable for application in IBC devices with tunneling recombination junction where *p*-type nc-Si:H-based blanket layer is deposited on intrinsic (on the emitter side) and *n*-type layer (on the BSF side). By introducing both (*n*)nc-Si:H and (*p*)nc-Si:H layers in this situation, the growth, and, therefore, properties, of (*p*)nc-Si:H blanket layer will differ in emitter and BSF region [20]. This will be explained in more detail in Section 2.3.1.

2.2.3. Optical and electrical properties of a-Si:H and nc-Si:H

Depending on deposition conditions and parameters such as hydrogen content, doping concentration, or alloying with other atoms, electrical properties of a-Si:H and nc-Si:H can be varied and deposited material can be optimized for specific applications in solar cells. In the case of a-Si:H, dark conductivity varies with the doping type and concentration. While dark conductivity of intrinsic a-Si:H falls below 10^{-10} S/cm, addition of phosphorous and boron to plasma increases the dark conductivity of (*n*)a-Si:H and (*p*)a-Si:H up to 10^{-1} S/cm and 10^{-2} S/cm, respectively [57]. Similarly, the conductivity of nc-Si:H films can be increased by the inclusion of doping atoms and, in the case of both amorphous and nanocrystalline materials, *n*-type materials generally exhibit higher conductivity compared to *p*-type counterparts [58]. However, as the doping is more efficient in crystalline materials, the increase in conductivity with doping concentration is more pronounced in nc-Si:H.

Likewise, optical properties are dependent on hydrogen content, doping, and alloying of Si. The bandgap of a-Si:H is in the range from 1.6 eV to 1.8 eV and highly depends on hydrogen content [3]. As a-Si:H is direct bandgap material, it is characterized by a higher absorption coefficient compared to c-Si and nc-Si:H in the visible part of the spectrum. Therefore, employing nc-Si:H, with a similar bandgap to c-Si, instead of a-Si:H is favorable in order to minimize parasitic absorption at the front side of devices. Additionally, in order to widen the bandgap of nc-Si:H, oxygen can be added to plasma forming nc-SiO_x:H with bandgap over 2 eV [3]. However, the fraction of crystalline phase in nc-SiO_x:H is decreased compared to nc-Si:H leading to lower conductivity.

Lastly, in the case of nc-Si:H, different conductivity values are recognized in lateral and perpendicular direction as a consequence of nanocrystalline growth [59]. As explained in Section 2.3.1, this property of nc-Si:H films is significant for efficient charge collection in tunneling IBC devices, where lateral conductivity of *p*-doped Si should be minimized to avoid shunting without decreasing its perpendicular conductivity.

2.3. Interdigitated-back-contacted solar cell

In order to achieve high J_{SC} and improve overall device performance, IBC solar cell architecture is introduced (Figure 1.4). In this architecture, contact stacks from FBC devices are used for charge carrier collection, but both electron and hole collection takes place on the rear side of the device. J_{SC}

can be improved by optimization of the illuminated side of the device. Due to the complex manufacturing process [18] and reduced area for electron and hole collection, FF is typically lower compared to FBC devices [60]. Additionally, during the fabrication of IBC devices, (*i*)a-Si:H can be damaged leading to lower passivation quality and lower V_{OC}, as well as J_{SC} and FF.

Firstly, to secure high FF, it is important to ensure the good interface quality between intrinsic and (*p*)a-Si:H during the processing by minimizing the potential damage to the intrinsic layer due to processing steps, such as incomplete etching, and ensuring the surface free of contamination prior to *p* layer deposition [18]. Moreover, low FF can be caused by the reduced area for electron and hole collection [19]. Therefore, it is important to carefully select the pitch, as well as the ratio of electron and hole collection regions. Theoretically, a smaller pitch works in favor of device performance as series resistance can be reduced. However, experimental results show a decrease in performance for small pitch width, likely due to manufacturing difficulties and increased edge-to-area ratio [61]. As hole transport is less efficient compared to electron transport, the optimal coverage of *p*-type contact is found to be 60% of the pitch, independently of the pitch width [62].

In order to ensure high V_{OC}, good passivation of both front and rear surfaces has to be guaranteed. On the rear side, the passivation quality can be preserved by ensuring that (*i*)a-Si:H layer is not removed during processing. Specifically, along the processing of IBC devices in this project, SiO_x layer is deposited on top of the rear (*i*)a-Si:H as a sacrificial layer in order to avoid (*i*)a-Si:H removal during the patterning steps. More details about fabrication steps and the use of sacrificial SiO_x are presented in Section 4.2. Additionally, doped layers should provide sufficient field effect on the rear side enabling successful collection of charge carriers. Apart from the (*i*)a-Si:H layer, the front side passivation can be further enhanced by depositing a thin, transparent layer of (*n*)nc-SiO_x:H that serves as the front surface field (FSF) reducing recombination losses at the front side of the device [63].

2.3.1. Introduction to tunneling recombination junction

While for the standard IBC device, electron collection is achieved by *n*-type layer, in tunneling devices layer stack consisting of *n*- and *p*-type layers serves as electron collecting stack (Figure 2.9a). At the interface of highly doped *n*- and *p*-type materials, so-called tunneling recombination junction (TRJ) or interband tunnel junction can be formed as the high doping levels of these semiconductors induce narrow depletion region [61]. In TRJ, electrons are collected by *n*-type layer before tunneling through a potential barrier to recombine with holes from *p*-type layer as presented in Figure 2.9b. In order to achieve successful interband tunneling, the potential barrier has to be small enough which is enabled by high doping of both *n*- and *p*-type materials.

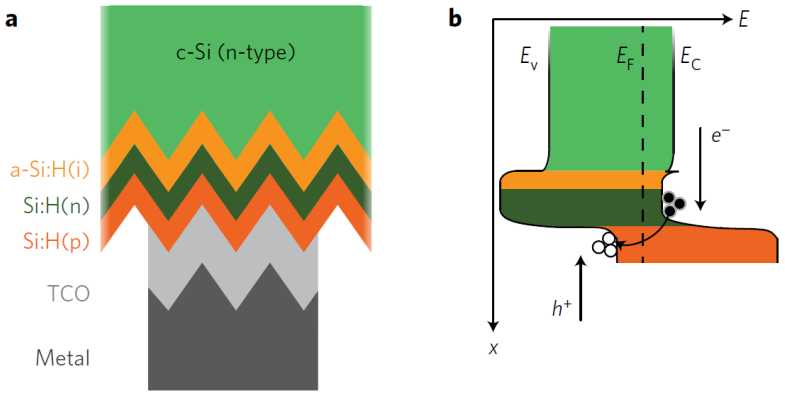


Figure 2.9: Schematic representation of (a) TRJ consisting of intrinsic and doped Si-based layers, TCO and metal and (b) sketch of band diagram of TRJ. Adapted from [20].

As reported in [61], three main criteria for an efficient TRJ contact stack are recognized. Firstly, electrons should be collected and transported through TRJ without resistive losses, requiring a low-resistance tunneling junction. Secondly, the sufficient field effect has to be achieved with *n*-type layer as it should enable efficient collection of electrons in TRJ, while being opaque to the influence of the

electronic band structure of the overlaying p layer. Lastly, as it covers the full rear area, p-type layer should have low lateral conductivity to prevent the formation of a short circuit in a tunneling device.

In order to fulfill the first requirement, high doping concentration of both n and p layers needs to be obtained. High doping of both doped layers induces a narrow depletion region and low contact resistivity. High doping concentration in n-type layer is also vital for good field effect and screening of c-Si surface from the overlaying p-type layer. Hence, due to more efficient doing compared to a-Si:H, nc-Si:H is a good candidate for doped layers in a tunneling device. Additionally, the growth of nc-Si:H is highly dependant on the substrate. As shown in Figure 2.10, the deposition of (p)nc-Si:H on (i)a-Si:H in hole contact stack leads to the growth of (p)nc-Si:H that is characterized by thicker incubation zone. On the other hand, the growth of (p)nc-Si:H on top of (n)nc-Si:H is determined by the crystalline fraction of (n)nc-Si:H, which induces highly crystalline growth of (p)nc-Si:H from the beginning.

While thicker incubation zone of (p)nc-Si:H in hole contact stack ensures low lateral conductivity of the layer and sufficient insulation between two contacts, highly crystalline growth of (p)nc-Si:H in TRJ enables high doping concentration, low contact resistivity and efficient tunneling. As discussed in [61], such properties could not be obtained when employing doped a-Si:H layers due to inefficient electron collection in TRJ and S-shaped J-V curve.

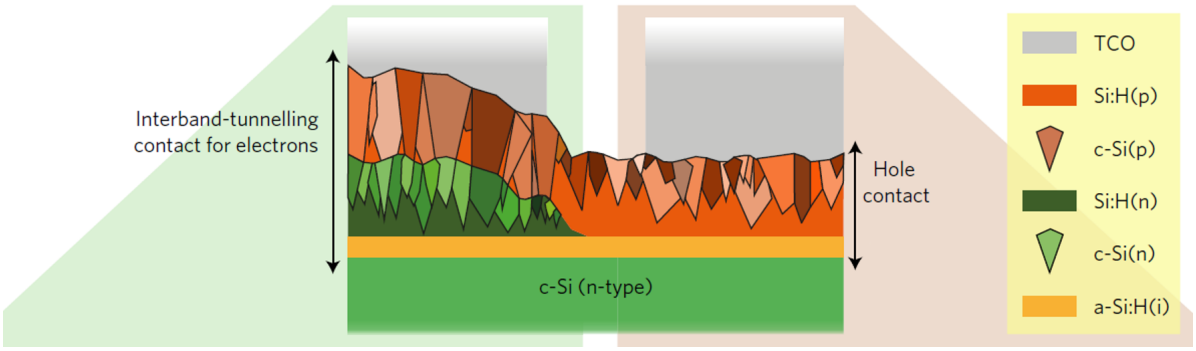


Figure 2.10: Cross-section of the doped nc-Si:H bilayer microstructure on the rear side of tunneling IBC device. Adapted from [20].

2.4. Working principle of TMO-SHJ solar cells

Similar to SHJ devices described in Section 2.2, in TMO-SHJ solar cells selective passivating contacts are formed on the surface of the c-Si bulk in order to secure efficient collection of electrons and holes. However, instead of doped Si-based layers, TMOs with low or high work function are deposited over (i)a-Si as ETL or HTL, respectively. Carrier selectivity is enabled by the band bending at the interface of c-Si, which leads to the efficient transport of one type of charge carrier while suppressing the transport of the other.

In this project, MoO_x is used as a alternative for p-type nc-Si:H-based layer acting as an HTL. As explained in Section 1.4, MoO_x is a suitable HTL due to high WF which induces band bending at c-Si/(i)a-Si:H interface and allows selective hole collection. Resulting from such oxygen vacancies, Fermi energy level of MoO_x becomes closer to the conduction band making it n-type material [64]. The amount of oxygen vacancies likely plays a role for hole transport as the vacancies are assisting the tunneling of the charge carriers at the contact with Si [65]. Moreover, as known from [66], the deposition of MoO_x leads to oxidation of the substrate, forming a thin layer of tunnel oxide at (i)a-Si:H/MoO_x interface. Typical structure of FBC-SHJ solar cell with MoO_x on the illuminated side is shown in Figure 2.11. In such device, hole collection occurs through contact stack consisting of (i)a-Si:H, MoO_x, TCO and metal.

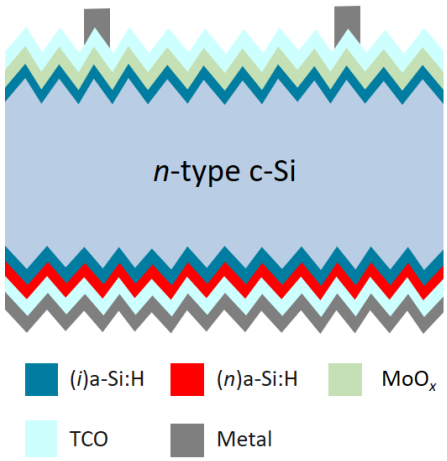


Figure 2.11: The structure of FBC-SHJ solar cell with MoO_x.

In Figure 2.12, a band diagram of HTL of solar cell with MoO_x is shown. Due to the band bending induced close to the surface of c-Si, holes are attracted to c-Si/(i)a-Si:H interface and they can eventually cross the barrier towards (i)a-Si:H via thermionic emission. Holes accumulated at the SiO_x interface can tunnel through SiO_x and recombine with electrons from MoO_x via band to band or trap assisted tunneling which is determined by the density of traps, energy alignment with (i)a-Si:H and work function of MoO_x. The electrons can reach to MoO_x from TCO by direct tunneling or thermionic emission through TCO/MoO_x interface, while electrons reach TCO from the metal contact.

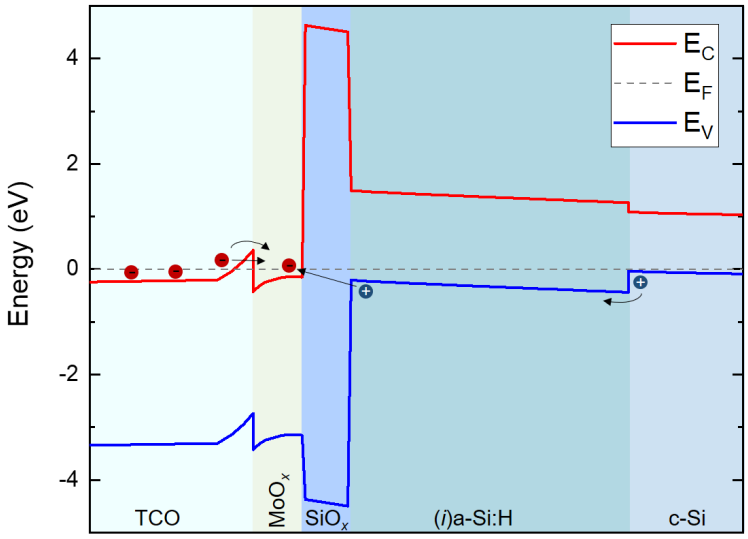


Figure 2.12: Band diagram of hole transport layer featuring MoO_x. Conduction and valence bands are shown in red and blue, respectively. Transport of electrons (red circles) and holes (blue circles) is sketched.

An important aspect determining the performance of cells featuring MoO_x is its WF value which is essential for controlling the band bending at c-Si/(i)a-Si:H interface [65]. Higher WF induces larger band bending at c-Si/(i)a-Si:H interface leading to higher accumulation of holes and more efficient carrier separation. Ultimately, this enables reduction in recombination and larger V_{OC} and FF. However, as the WF of MoO_x decreases with the increase in oxygen vacancies, the trade-off is made between the two [67]. In the case of either low WF or low number of oxygen vacancies, selectivity and hole transport are affected. This potentially leads to poor performance of the cells, low V_{OC} and FF and s-shaped J-V curve [68], [69]. To ensure good interface quality between Si and MoO_x, in this research an additional

plasma treatment (PT) is included between the deposition of (i)a-Si:H and MoO_x as proposed by [70]. By including optimized PT, higher FF and V_{OC} can be achieved compared to devices without PT.

3

Methods for SHJ Solar Cell Fabrication and Characterization

In this Chapter, an overview of the methods and tools used for manufacturing and characterization of solar cells during this thesis is given. The fabrication steps used for devices presented in this thesis are explained and main deposition parameters are highlighted. Characterization techniques described in this Chapter cover both electrical and optical characterization of manufactured devices.

3.1. Wafer preparation techniques

In this Section, preparation techniques that have been used before and during solar cell manufacturing are described. Techniques employed during this project include wafer texturing and wafer cleaning.

3.1.1. Wafer texturing

In order to decrease reflection losses and improve absorption, solar cells have been manufactured using single-side textured (SST) and double-side textured (DST) wafers. By introducing textured surface, part of the light that is reflected at a textured surface can be reflected at such angle that allows it to be incident at another surface and finally coupled into the wafer [3]. This will lead to higher light absorption.

In order to achieve a random pyramid structure, the texturing is done by the anisotropic etching method. Texturing process is performed by immersing the silicon wafer in a hot alkaline etching solution with a faster etching rate for <100> orientation compared to <111>. This way the <111> surface is exposed after etching forming random pyramid structures. For texturing, a 5% tetramethylammonium hydroxide (TMAH, $(CH_3)_4NOH$) hot solution (75±2°C) consisting of 1L 25% TMAH (SIGMA-ALDTICH), 4L od deionized water (DI water) and 120ml of ALKA-TEX.8 (ISRA), where ALKA-TEX.8 is used for increasing the reaction speed and extending the lifetime of the etching bath.

3.1.2. Wafer cleaning

For successful manufacturing of high-performance solar cells, it is important to work with c-Si wafers that are free of metal and organic contamination and have low surface defect densities. Even though both flat and textured surfaces suffer from contamination and defects, textured surfaces are typically more affected by these issues due to larger surface area. In order to decrease surface contamination and achieve lower surface defect density, wafer cleaning is performed after texturing. The main purposes of the cleaning step are:

- Removing impurities and contaminants left from the texturing process;
- Smoothing the surface irregularities such as nano-roughness resulting from the texturing process;
- Partially passivating the dangling bonds at the c-Si wafer surface and removing native oxide from the surface.

The wafer cleaning method used in this project is commonly referred to as the nitric acid oxidation cycle (NAOC). This cycle consists of wet-chemical oxidation followed by hydrofluoric acid (HF) dip to remove the oxide formed on the surface. Firstly, wafers are fully immersed into 99% room-temperature HNO_3 for 10 minutes to remove organic contamination and then rinsed for 5 minutes in DI water.

Next, to remove metal contaminants, wafers are dipped into 69.5% HNO_3 solution at 110 ±5°C. This is followed by 5 minute DI water rinse. Finally, the formed oxide layer is removed by Marangoni (0.55% HF) method. During this process, the dangling bonds at the c-Si surface are partially passivated as surface Si atoms form bonds with hydrogen. HF dip with a duration of 5 minutes is taken as a standard procedure. As suggested by [39], the complete NAOC cycle is repeated three times and after the last Marangoni step of the cycle, wafers are loaded immediately into the vacuum chamber in order to avoid the formation of native oxide on the wafer surface. This time is ideally kept within 5 minutes.

3.2. Deposition techniques

In this Section, deposition techniques used for manufacturing solar cells within this thesis are described. Firstly, plasma-enhanced chemical vapor deposition (PECVD) is used for the deposition of thin-film silicon layers such as intrinsic and doped hydrogenated amorphous silicon (a-Si:H), hydrogenated nanocrystalline silicon (nc-Si:H), and hydrogenated nanocrystalline silicon oxide (nc-SiO_x:H). a-Si:H, nc-Si:H and nc-SiO_x:H are deposited as selective passivating contacts. Additionally, silicon oxide (SiO_x) layer is also deposited using PECVD and it is used as a sacrificial layer for patterning the contacts on the rear side, as well as the ARC on the front side. The transparent conductive oxide (TCO), used for the improved lateral transport of charge carriers, is deposited by radio frequency magnetron sputtering. Metalization is performed by screen printing or by evaporation.

3.2.1. Plasma-enhanced chemical vapor deposition

Plasma-enhanced chemical vapor deposition (PECVD) is used for deposition of thin-film a-Si:H, nc-Si:H and nc-SiO_x:H layers on the c-Si substrate. PECVD is a simple procedure that allows for the deposition of thin films at temperatures below 200°C [3]. A wide range of gas precursors that can be used as well as good adhesion, surface coverage, and uniformity of deposited films are important advantages of the PECVD technique. Moreover, the quality of films can be controlled by a set of parameters such as chamber pressure and temperature, type and flow rates of gas precursors, or power of the radio-frequency (RF) or very high frequency (VHF) generator [3]. Optimization of such parameters can lead to the desired opto-electrical properties of deposited layers.

For thin-film depositions in this thesis, the multi-chamber PECVD cluster tool, also called AMIGO, (Elettorava S.p.A.) in Else Kooi Lab (EKL) at the Delft University of Technology is used. Figure 3.1 is the schematic representation of a typical PECVD chamber [39].

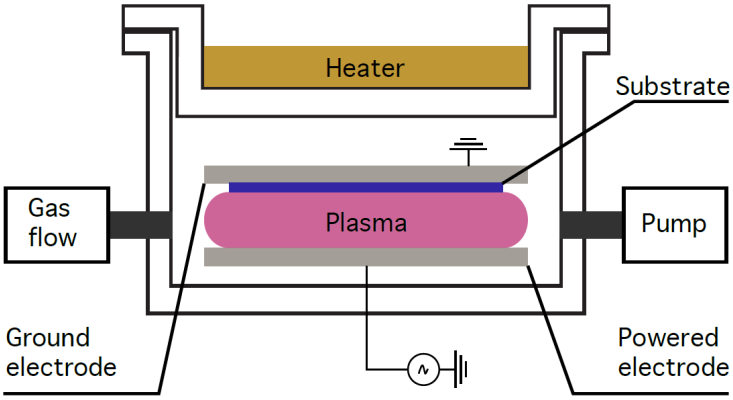


Figure 3.1: Schematic representation of a typical PECVD chamber. Adapted from [39].

Prior to deposition of the desired layers, the sample is loaded in the Loadlock Chamber (LLC) of AMIGO. Using the robot arm, the sample is transferred through Transfer Chamber (TC) to the Deposition Chamber (DPC) where the deposition is going to take place. LLC, TC, and DPCs are set to ultrahigh vacuum (UHV) conditions and the designated DPC is heated up to the desired temperature for the deposition that will take place. In the PECVD technique, plasma is created from a precursor gas mixture injected into the DPC. Depending on the material that is to be deposited, different gas precursors

are used. For deposition of (*i*)a-Si:H, silane (SiH_4) is used, while for deposition of *n*- and *p*-type layers phosphine (PH_3) and diborane (B_2H_6) are additionally included as doping gases, respectively. Hydrogen (H_2) is added to plasma for hydrogenation purposes either during the deposition or separately as hydrogen plasma treatment (HPT). Finally, carbon dioxide (CO_2) can be added to the gas precursor mixture in order to include oxygen in the layer. During deposition, the substrate temperature is typically kept at 160°C during the deposition of (*i*)a-Si:H and 180°C during the deposition of doped layers.

Gases released into the deposition chamber are converted into plasma by an oscillating electric field regulated through an RF signal of 13.56 MHz or a VHF signal of 40.68 MHz [3]. Collisions between electrons and gas molecules breakdown source gases in plasma forming reactive free radicals and ions. Formed radicals and ions are then coupled to the substrate leading to the formation of thin-film layers.

In this research, each of the DPCs shown in Figure 3.2 was used for the deposition of only one type of layer to prevent cross-contamination. Namely, DPC1 was used for *p* layer deposition, DPC2 for *n* layers, and DPC3 for deposition of *i* layers.

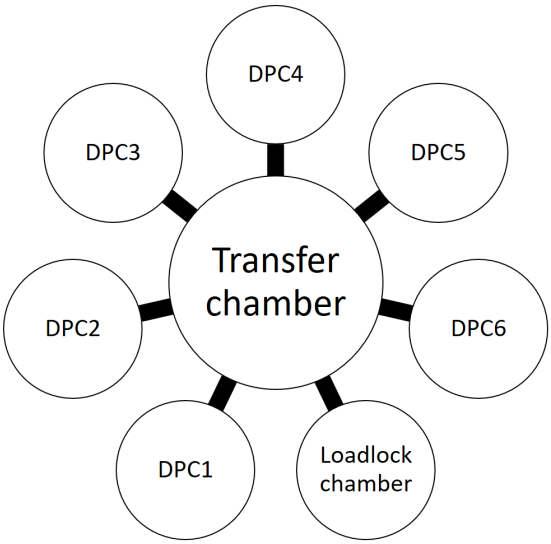


Figure 3.2: Schematic top-view of AMIGO PECVD (Elettrorava, S.p.A.) with six deposition chambers, loadlock chamber, and transfer chamber. All chambers are connected to pumps to allow high vacuum transfer and deposition.

Deposition parameters of layers deposited with AMIGO are summarized in Table 3.1.

Table 3.1: Deposition parameters of layers deposited with AMIGO PECVD (Eletrrorava, S.p.A.).

Layer	**$T_{substrate}$ (°C)**	**Pressure (mbar)**	**Power density (mW/cm^2)**	**SiH_4 (sccm)**	**PH_3 (sccm)**	**B_2H_6 (sccm)**	**CO_2 (sccm)**	**H_2 (sccm)**
(*i1*)a-Si:H	160	0.7	20.8	40	-	-	-	-
(*i2*)a-Si:H	160	1.4	20.8	10	-	-	-	30
(*n*)a-Si:H	180	0.6	27.8	40	11	-	-	-
(*n*)nc-Si:H	180	2.7	76.4	1	1.2	-	-	100
(*n*)nc-SiO_x:H	180	1.5	76.4	1	1.2	-	1.6	100
(*p*)nc-Si:H	180	2.2	90.3	0.8	-	10	-	170
(*p*)nc-SiO_x:H	180	2.2	76.4	0.8	-	10	1.4	170

For deposition of SiO_x PECVD (Oxford Instruments plc) in Kavli Nanolab at Delft University of Technology is used. This tool is simpler compared to AMIGO, having only one chamber for both loading samples and deposition. For deposition of SiO_x, SiH_4 and nitrous oxide (N_2O) gases were used

and chamber temperature was set to 150°C. Deposition parameters of SiO_x deposited by Plasmalab 80 Plus PECVD are presented in Table 3.2

Table 3.2: Deposition parameters of SiO_x deposited with Plasmalab 80 Plus PECVD (Oxford Instruments plc).

Layer	$T_{substrate}$ (°C)	Pressure (mbar)	Power density (mW/cm^2)	SiH_4 (sccm)	N_2O (sccm)
SiO_x	150	1.3	44.2	8.5	710

3.2.2. Radio frequency magnetron sputtering

Radio frequency magnetron sputtering is a physical vapor deposition (PVD) technique that is generally used for depositing TCO layers and metal contacts. In Figure 3.3, the schematic representation of magnetron sputtering process is shown [71]. Magnetron sputtering involves the use of high energetic argon (Ar) particles to bombard the target leading to the release of target atoms that are then diffused to the substrate surface.

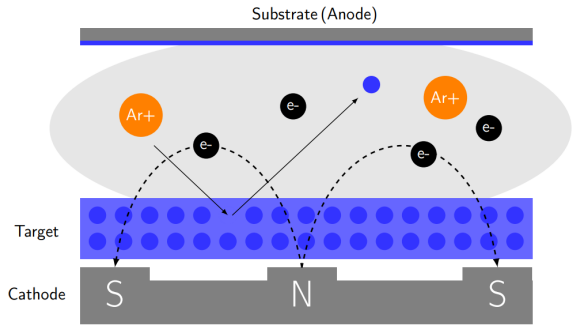


Figure 3.3: Schematic representation of magnetron sputtering process. Adapted from [71].

The sputtering tool used in this thesis is the so-called ZORRO manufactured by Polyteknik. During this project, ZORRO is used for indium tin oxide (ITO) and indium tungsten oxide (IWO) sputtering. ITO target consists of 90 wt.% In_2O_3 and 10 wt.% SnO_2, while used IWO target consist of 95 wt.% In_2O_3 and 5 wt.% WO_3 [72]. Sputtering was carried out at room temperature. Moreover, post-deposition annealing at 180 °C for 5 minutes was performed to mitigate sputter damage [73].

3.2.3. Screen printing

As a final step of FBC solar cell processing, metal contacts are formed on the front and back sides of the cell precursor by using screen printing. Screen printing involves sweeping viscous metallic paste over the surface of a wire mesh screen. The screen is designed with openings corresponding to the desired metal grid layout. The paste is firstly placed at the corner of the screen and afterward spread with a plastic squeegee over the screen. As the paste runs through screen openings, it is deposited on the cell precursor with the desired pattern. A schematic representation of screen printing is presented in Figure 3.4 [74]. After screen printing of both front and back sides, devices are cured at 170°C in air for 30 minutes to form metal contacts. Due to temperature limitations during manufacturing of SHJ devices, low-temperature silver polymer-based paste produced by KYOTO ELEX CO., LTD was used during this project. This paste requires baking at 170°C, which is suitable for SHJ devices and does not damage low temperature layers.

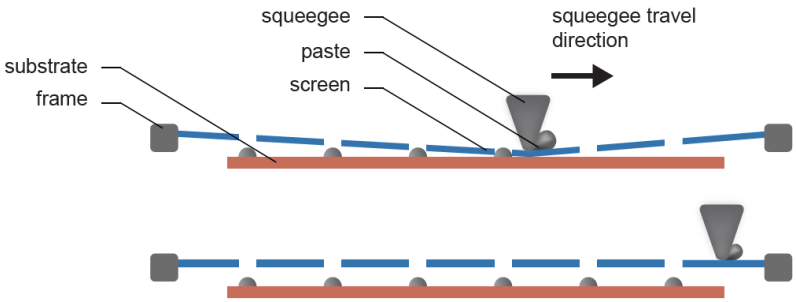


Figure 3.4: Schematic representation of screen printing during the process (top) and at the end of the process (bottom). Adapted from [74].

3.2.4. Evaporation

For metal contact formation of IBC cells, metalization is performed using evaporation. This method is based on heating up the source material leading to evaporation of the material in a high vacuum chamber enabling to precisely control the deposited thickness and oxidation level of the material [75]. The evaporated material is targeted to the substrate at a significantly lower temperature compared to the temperature of the evaporated material and, due to the temperature difference, the evaporated material condenses at the substrate surface forming a thin layer. Depending on the melting point of the evaporated material, either electron beam evaporation or thermal evaporation is used. Materials with lower melting points such as Ag, whose melting point is around 960°C, are evaporated by thermal evaporation [76]. During thermal evaporation, material is loaded in an open tungsten boat which is heated by the current passing through it (Figure 3.5 on the right). In the case of high melting point material such as Cr with a melting point of 1900°C, electron beam evaporation is used [76]. For this method, a water-cooled tungsten crucible filled with material source is bombarded by an electron beam directed to the crucible by a magnetic field (Figure 3.5 on the left). The kinetic energy of the electron beam is then converted into thermal energy leading to evaporation. Even though the melting point of Al is lower compared to Ag, Al is deposited using electron beam evaporation in order to avoid Al alloying with a heated tungsten boat which is used to hold source material.

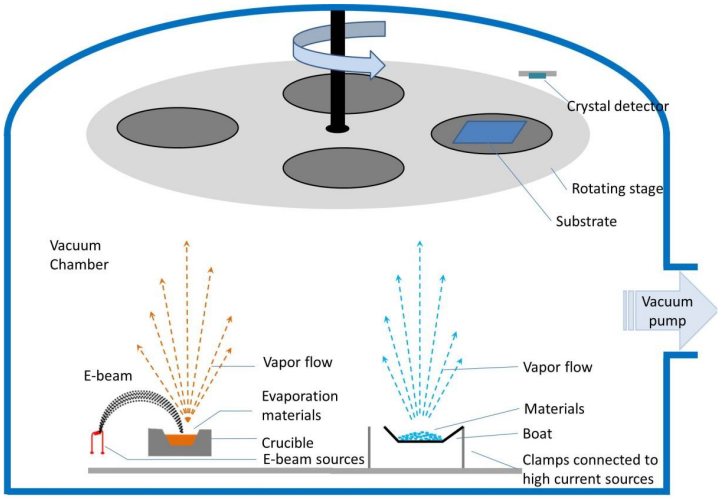


Figure 3.5: Schematic representation of metal evaporation system used in this project. Electron beam evaporation is shown on the left, while thermal evaporation is on the right side of the sketch. Adapted from [77].

For manufacturing of IBC solar cells presented in this thesis, Provac PRO500S (Figure 3.5 [77]) was used as an evaporation tool for electron beam evaporation of Al and thermal evaporation of Ag. Moreover, thermal evaporation in Provac PRO500S was used for deposition of MoO_x for devices featuring MoO_x

as HTL. MoO_x is deposited by thermal evaporation of MoO_3 powder. However, during the evaporation, MoO_3 loses some of the oxygen due to the reaction of oxygen atoms with the surrounding layers modifying the stoichiometry of the deposited layer from MoO_3 to MoO_x [29].

3.3. Patterning techniques - Photolithography

In order to form an alternating pattern of electron and hole selective contacts on the rear side of the IBC solar cell, it is important to precisely pattern the rear side of the devices to ensure carrier collection and avoid shunting losses. Some of the common methods used for patterning IBC-SHJ solar cells are photolithography, shadow masking, inkjet printing, and laser-based patterning [13]. In this project, photolithography technology is used for patterning of rear contacts as it can ensure more precise pattern formation (feature size < 1 µm) compared to shadow masking or laser-based patterning and is available in EKL cleanrooms.

Photolithography is a term for methods used to pattern thin films of photosensitive material (photoresist) by exposing parts of the film to UV light through a photomask. By light exposure, the mask patterns are transferred to the substrate. Photolithography process includes three main steps as shown in Figure 3.6 [74]. Firstly, the substrate is coated with a photoresist. Either positive or negative photoresist can be used. This is followed by exposure by UV light through the desired photomask. In case of positive photoresist, the exposed portion of the material is degraded and the exposed photoresist is etched away during the development process to form the pattern on the substrate. In case of the negative phototresits, the exposed part is hardened and the part that was covered by the photomask will be developed. Finally, the remaining photoresist is then used as an etching mask during the wet and dry etching of underlying layers. By using a photoresist as an etching barrier, the desired pattern can be developed on the substrate with high precision.

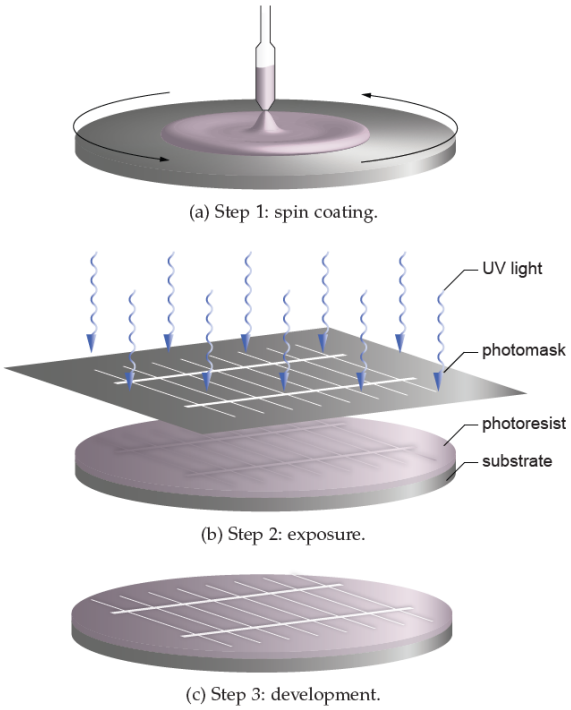


Figure 3.6: Schematic representation of the simplified working principle of photolithography using a positive photoresist. Adapted from [74].

Photolithography process during this research was performed in the lithography room and polymer lab of EKL at Delft University of Technology. Both rooms are lightened with yellow light only to avoid photoreaction of photoresist. The coating was performed manually using Brewer Science Manual Spinner and positive AZ ECI 3027 photoresist. Positive photoresist is used during this project as it can be removed with less damaging methods compared to the negative photoresist. Namely, as

the negative photoresist is hardened during the exposure, it cannot be dissolved in acetone that is typically used for positive photoresist removal. Therefore, the removal of negative photoresist requires the use of more resistant chemical solvents or an aggressive oxygen plasma treatment that can damage passivation quality. After coating, a soft bake step was done in a Memmert oven at 105°C for 5 minutes. The exposure was carried out with SUSS MicroTec MA/BA8 mask aligner and the exposure time was adjusted depending on the thickness and type of the photoresist film and the light intensity of the installed lamp. The photoresist was developed using alkaline developer Microposit^{TM} MF-322. The time of development varied depending on the resist thickness.

3.4. Characterization techniques

In this Section, characterization techniques used to understand the quality of deposited layers, cell precursors and final devices are presented.

3.4.1. Spectroscopic ellipsometry

Spectroscopic ellipsometry (SE) is an optical characterization method that can be used to describe deposited films with high precision in a non-destructive manner [78]. It measures the change in the polarization of the light following the interaction of light with the sample. Results of SE measurements are Ψ and Δ, parameters that describe the change in polarization. tanΨ represents amplitude ratio between p- and s-wave, while Δ represents phase difference. In order to gain valuable information about the material, such as film thickness, optical constants or surface roughness, a mathematical model describing the material of interest is used to fit Ψ and Δ data. Typically, Cauchy's equation is used to describe transparent films such as SiO_2, while completely absorbing films are described by B-Spline model. For a-Si:H layers in this research Cody-Lorentz model is used [79], while more complex films such as nc-SiO_x:H are modelled using EMA (effective medium approximation) with Bruggeman model. Figure 3.7 shows schematic representation of the SE measurement setup [39]. As seen in the Figure, the setup consists of a light source, a polarizer, an analyzer and a detector. The light source emits an unpolarized light, that is linearly polarized by passing through the emitter. Once the light is reflected from the sample, it passes through the analyzer that analyzes the reflected beam.

In this project an SE setup by J.A. Woollam Co., M-2000DI is used for thickness measurements of deposited and etched layers. The main purpose of thickness measurements in this project was to determine deposition and etching rates, and their uniformity. In case of SE measurements of etched samples, the thickness change with increasing etching time was followed to determine the most suitable etching conditions. However, the measurements have to be performed on the flat surface. Therefore, when interested in determining thickness of films deposited on textured wafers, separate samples had to be prepared for SE measurement either on corning glass or polished c-Si wafers. Both deposition and etching rates were assumed to be 1.7 times faster on flat surface.

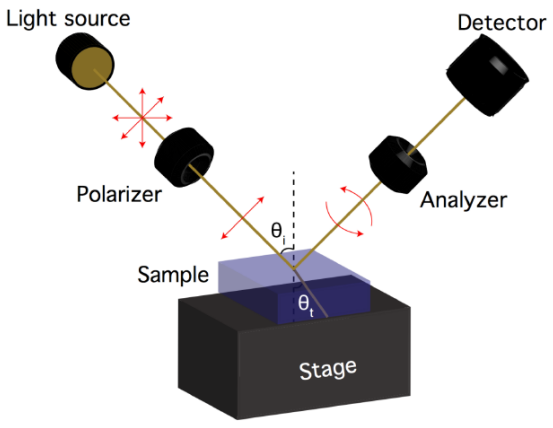


Figure 3.7: Schematic representation of the SE measurement setup. Adapted from [39].

3.4.2. Photoconductance lifetime tester

Ensuring good passivation quality of deposited layers and following the performance of cell precursors during processing is crucial for determining potential bottlenecks in the process. Therefore, photoconductance lifetime tester (Sinton WCT-120) is used to characterize precursors along the process in terms of effective minority charge carrier lifetime (τ_{eff}), implied open-circuit voltage (iV_{OC}), implied fill factor (iFF) and reverse-biased saturation current (J_0) [80]. In Figure 3.8 a schematic representation of a used setup is presented [39].

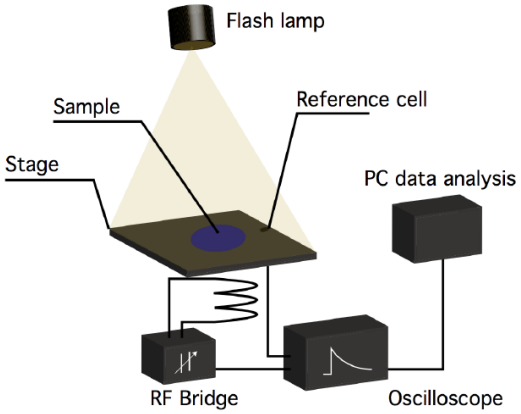


Figure 3.8: Schematic representation of Sinton WCT-120. Adapted from [39].

A sample is placed on a stage at uniform and constant temperature with a built-in reference cell (a light intensity detector). A coil is installed below the stage and it is inductively connected to an RF bridge. Above the stage, a flash lamp is located. Once the sample is placed on the stage and the measurement is initiated, the lamp flashes light to the sample at predetermined short periods of time. With the flash of light, the conductance of the sample changes due to generation of excess charge carriers as a result of optical excitation. This change is detected by the coil. The measured changes are directly analysed within a software in order to obtain τ_{eff}, iV_{OC}, iFF and J_0 [80].

Photoconductance (σ_L) measured with lifetime tester is defined as the change in conductance of the sample due to optical excitation. For an *n*-type substrate, it is related to the minority charge carrier density as shown in Equation 3.1 [80], where q is the elementary charge, Δp is the excess carrier density, W is sample thickness and μ_n and μ_p represent mobility of electrons and holes, respectively. From the measured photoconductsnce, Δp can then be determined.

$$\sigma_L = q\Delta p(\mu_n + \mu_p)W \tag{3.1}$$

Analysis can be performed using two different modes depending on the lifetime of the sample [80], [81]. The modes differ by the decay time constant of the flash lamp. Quasi-steady-state-photoconductance (QSSPC) mode featuring long time constant is typically used for samples with low τ_{eff} ($\tau_{eff} < 200$ µs), whereas for samples with $\tau_{eff} > 200$ µs transient photoconductance decay (Transient PCD) mode is recommended as it is involves shorter light decay time. Equation 3.2 represents a mathematical expression of τ_{eff} derived from continuity equation [3].

$$\tau_{eff} = \frac{\Delta p}{G(t) - \frac{\partial \Delta p}{\partial t}} \tag{3.2}$$

In Equation 3.2, G stands for the carrier generation rate calculated from the reference cell. For QSSPC mode, due to long decay time constant it can be assumed that the light flash is varying slowly enough so that $\partial\Delta p/\partial t$ can be neglected as $G(t) \gg \partial\Delta p/\partial t$. On the other hand, in transient mode the flash

light is off during the actual measurement and G(t) can be set to zero. Therefore, with the correct assumptions, Equation 3.2 can be used for analysis in both QSSPC and Transient PCD mode.

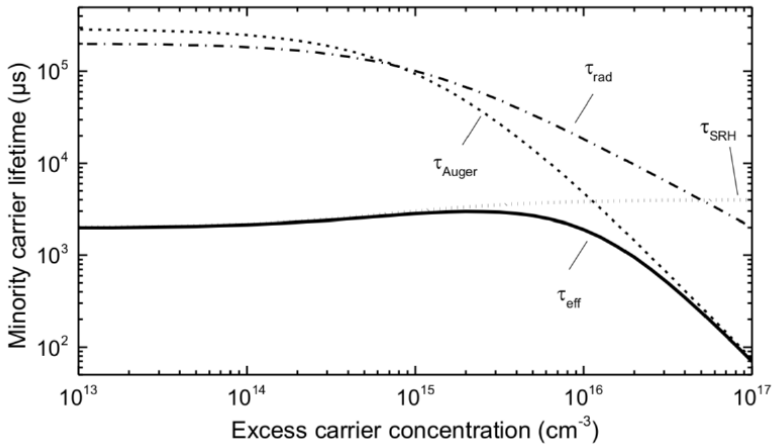


Figure 3.9: Simulated minority carrier lifetime curve as function of the excess carrier concentration. Adapted from [44].

An example of effective carrier lifetime curve and the influence of different recombination mechanisms is shown in Figure 3.9 [44], where τ_{eff} is presented as a function of minority carrier density (MCD). τ_{eff} is typically noted at MCD = 10^{15} cm^{-3} as it is a relevant point to be analyzed for evaluation of recombination at the a-Si:H/c-Si interface [76]. At this injection level, the recombination velocity is mainly influenced by Shockley-Read-Hall (SRH) recombination which is a good indicator of defects present in the material. On the other hand, at higher MCD values, Auger and radiative recombination become more dominant [81] (Figure 3.9). Moreover, MCD = 10^{15} cm^{-3} is comparable to the injection level at one-sun illumination.

Another important parameter that can be retrieved from photoconductance measurements is implied open-circuit voltage (iV_{OC}). The implied V_{OC} is determined based on the MCD and it represents the upper limit of V_{OC}. It is calculated by Equation 3.3, where N_D is the donor concentration.

$$iV_{OC} = \frac{k_B T}{q} \ln \frac{\Delta p(N_D + \Delta p)}{n_i^2} \tag{3.3}$$

During this research project, lifetime measurements have been performed after every deposition and etching step. The aim of the close monitoring of lifetime was to ensure that films of good passivation quality are deposited and that the quality is preserve during potentially damaging steps such as wet-chemical etching of doped layers.

3.4.3. Current-Voltage measurement

Solar cells fabricated in the course of this project are tested with an AAA class Wacom WXS-90S-L2 solar simulator to obtain external parameters of the devices. The tests are performed under standard test conditions (STC) at irradiance of 1000 W/m^2, solar cell temperature of 25°C and AM1.5 spectrum [3]. AM1.5 spectrum is simulated with use of a halogen and a xenon lamp [39]. Prior to measurements, the setup is calibrated with two reference cells. A schematic representation of the setup is shown in Figure 3.10 [39].

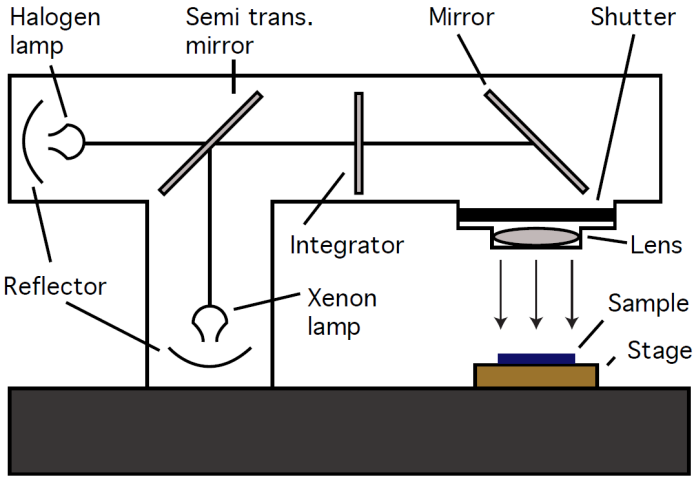


Figure 3.10: Schematic representation of current-voltage measurement setup. Adapted from [39].

Current-voltage characteristics of manufactured devices are obtained from the measurements and J-V curve is produced. From J-V curve as shown in Figure 3.11, external parameters of the solar cell such as open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), fill factor (FF) and photocoversion efficiency (η) can be extracted. Additionally, shunt and series resistance (R_{SH} and R_S) can be determined based on the slope of the curve at J_{SC} and V_{OC}, respectively. Both R_{SH} and R_S have a strong influence on FF and can pose limitations on performance of the devices. During the fabrication of IBC devices, low R_{SH} represented a significant obstacle due to high lateral conductivity of Si doped layers, which will be explained in detail in Chapter 4.

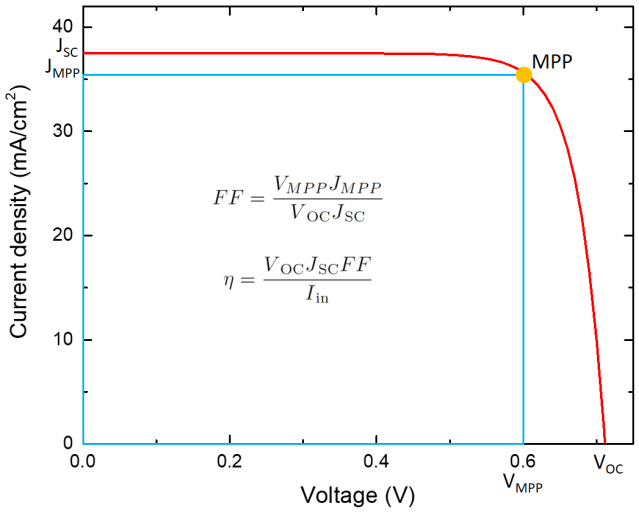


Figure 3.11: An example of a J-V curve with external parameters and definition of fill factor and photoconversion efficiency.

3.4.4. SunsV_{OC} measurement

To determine FF loses due to series resistance, SunsV_{OC} measurements are conducted. J_{SC} extracted from current-voltage measurements is used as an input parameter for the measurements and only voltage is measured. For SunsV_{OC} measurements performed for devices after metalization in this project, the Suns-Voc-150 (Sinton Instruments) illumination-voltage tester was used. In the setup, a flash lamp with a slow decay is employed to generate a pseudo I-V curve unaffected by series resistance. SunsV_{OC} reflects the top limit of V_{OC} that could be measured using Wacom. Moreover, pseudo fill factor (pFF)

is derived from SunsV_{OC} measurements. By comparing pFF and FF an indication about losses due to R_S can be obtained and, as shown in Equation 3.4 [82], R_S can be calculated. Lastly, R_{SH} can be directly measured with the setup and it is used for analyzing shunting issues of IBC cells, as it will be mentioned in Chapter 4.

$$R_{S,SunsVoc} = (pFF - FF)\frac{V_{OC}J_{SC}}{J_{MPP}^2} \tag{3.4}$$

3.4.5. External quantum efficiency

The external quantum efficiency (EQE) represents the ratio between photons that create electron-hole pairs in the absorber that are collected successfully and photons incident on the solar cell [3]. EQE measurements are performed to gain an insight in optical and electrical losses in the device. EQE can be calculated by Equation 3.5 where I_{ph} (λ) is the photogenerated current, q is the elementary charge and $\Psi_{ph,\lambda}$ is the spectral photon flow incident on the cell. As it is defined as the fraction of the incident photons that leads to successful collection of charge carriers, EQE values are in the range from 0 to 1.

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\Psi_{ph,\lambda}} \tag{3.5}$$

In-house-built EQE measurement setup (spectral response setup) is used for EQE measurements during this project. The setup consists of a halogen gas discharge lamp as a light source, a calibrated photodiode, and a current meter. As the spectrum of a halogen lamp spreads over a wide range of wavelengths and EQE is a wavelength-dependent measurement (see Equation 3.5), a monochromator is used to obtain narrow wavelength bands of photon energies.

As $\Psi_{ph,\lambda}$ cannot be directly measured, a calibrated photodiode with know EQE is used for obtaining $\Psi_{ph,\lambda}$. $\Psi_{ph,\lambda}$ is determined by Equation 3.6 where EQE^{ref} (λ) is EQE of the calibrated photodiode and $I_{ph}{}^{ref}$ is the photocurrent of the photodiode that can be measured with the setup. Obtained $\Psi_{ph,\lambda}$ is used as the input for EQE measurements of solar cells. Since it is assumed that the photon flow in the reference measurement and the actual measurement is the same, it is crucial that the light source is stable throughout the entire measurement process.

$$\Psi_{ph,\lambda} = \frac{I_{ph}^{ref}(\lambda)}{qEQE^{ref}} \tag{3.6}$$

After acquiring EQE (λ), $J_{SC,\,EQE}$ can be determined by Equation 3.7, where $\Phi_{ph,\lambda}{}^{AM1.5}$ is spectral photon flux. Unlike J_{SC} obtained via J-V measurement, $J_{SC,\,EQE}$ determined by EQE is independent of the spectral shape of the light source and the contact area of the solar cell.

$$J_{SC,EQE} = -q\int_{\lambda_1}^{\lambda_2} EQE(\lambda)\Phi_{ph,\lambda}^{AM1.5}d\lambda \tag{3.7}$$

$\Phi_{ph,\lambda}{}^{AM1.5}$ is described by Equation 3.8, where h is Planck constant, c is the speed of light in vacuum and $P_{ph,\lambda}{}^{AM1.5}$ is the power density.

$$\Phi_{ph,\lambda}^{AM1.5} = \frac{P_{ph,\lambda}^{AM1.5}\lambda}{hc} \tag{3.8}$$

For c-Si solar cells, the wavelength range of interest is from 300 nm to 1200 nm. Below 300 nm power density of AM 1.5 spectrum can be considered negligible, while the upper limit of 1200 nm is determined by the bandgap of c-Si.

As reflectance losses are included in EQE measurement, the total reflectance (R) of the cell is measured in order to determine the internal quantum efficiency (IQE). Measurement of reflectance will be addressed in detail in Section 3.4.6. IQE represents the fraction of absorbed photons that are successfully collected.

IQE is determined by Equation 3.9, where R (λ) represents the reflectance at the wavelength λ and 1-R (λ) is the effective absorbance considering that the solar cell's rear side is opaque and no transmission occurs.

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)} \tag{3.9}$$

3.4.6. UV-Vis-NIR spectroscopy

Ultraviolet-Visible-Near-Infrared (UV-Vis-NIR) is a characterization method for analyzing the materials' optical properties in ultraviolet, visible and near-infrared regions of the spectrum. LAMBDA 1050+ UV-Vis-NIR spectrophotometer (PerkinElmer) is used to measure wavelength dependant reflectance of manufactured devices in this thesis. The R (λ) and EQE (λ) measurements are used to get an insight into the IQE (λ) of the measured devices and hence the optical and electrical losses. In Figure 3.12 [83] a schematic representation of UV-Vis-NIR spectroscopy setup is shown.

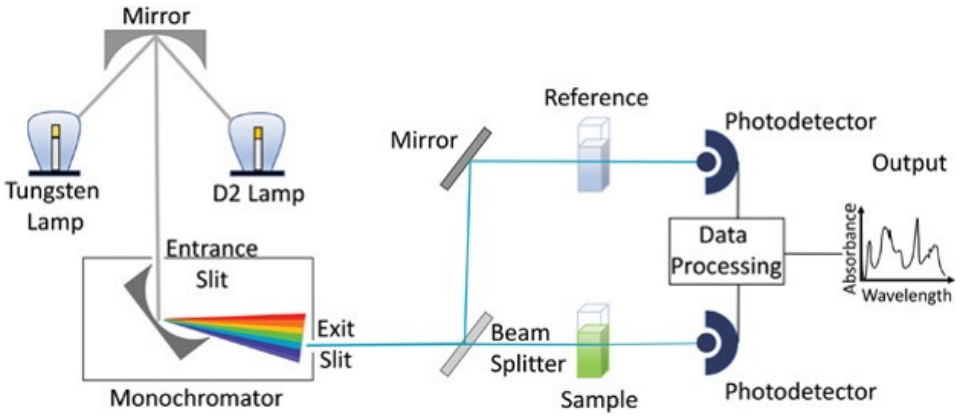


Figure 3.12: Schematic representation of UV-Vis-NIR spectrophotometer. Adapted from [83].

In the setup used during this project, two different light sources are used. The tungsten lamp generates light in the visible and near-infrared parts of the spectrum, while a deuterium (D2) lamp generates UV light. A monochromator is included in the setup to filter the light and illuminate the sample with a monochromatic light beam. After going through the monochromator, the beam is split by the beam splitter in order to illuminate the reference and the measured sample simultaneously.

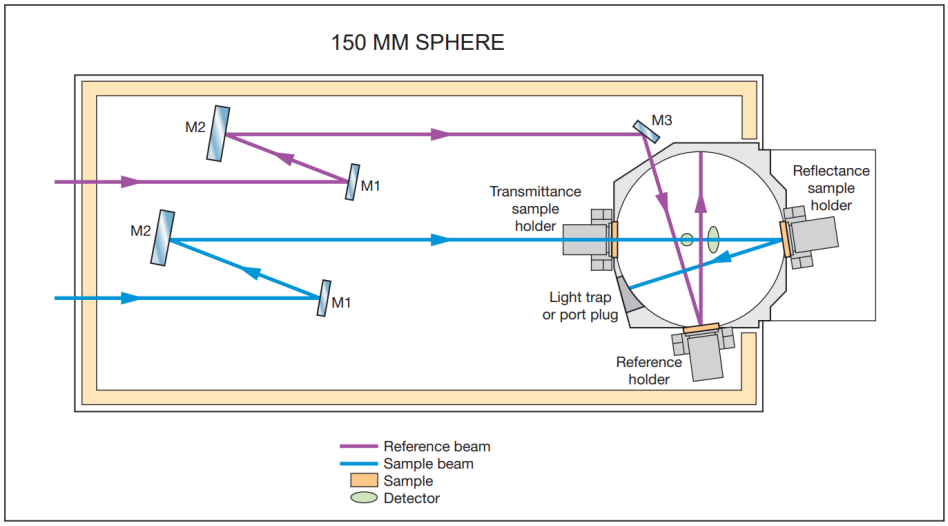


Figure 3.13: Schematic representation of the optical design of 150 mm integrating sphere including the position of sample holders for transmittance and reflectance measurements. Adapted from [84].

Depending on the purpose of the measurement, investigated samples are placed in a different position with respect to the integrating sphere. An integrating sphere is a hollow cavity whose inner walls are coated with a highly reflective material. Thus, the total scattering and reflection components can be considered, leading to more accurate measurements. As shown in Figure 3.13 [84], the transmittance and reflectance are measured by placing the sample in the front of or at the rear side of the integrating sphere, respectively. After interacting with the sample, the signal is acquired by photodetectors and processed to give the measured spectrum as output [83]. During this project, R (λ) is measured for wavelengths in the range from 300 nm to 1200 nm.

4

IBC-SHJ solar cells with Si-based doped layers

This Chapter covers the fabrication and results of IBC-SHJ devices with Si-based contact stacks. Firstly, proof-of-concept FBC devices are discussed in Section 4.1 followed by fabrication of tunneling IBC devices in Section 4.2 and standard IBC devices in Section 4.3.

4.1. FBC solar cells as a proof-of-concept

In order to check the passivation quality and performance of designed contact stacks before applying them to IBC devices, FBC-SHJ devices are used as a proof-of-concept due to the relatively simple processing compared to IBC devices. In this Chapter, the fabrication of standard and tunneling IBC-SHJ devices is presented and FBC-SHJ devices have been used as a proof-of-concept for contact stacks involved in both architectures. As Si-based contact stacks used for IBC-SHJ devices have already been developed within the PVMD group at Delft University of Technology, FBC devices fabricated by [85] have been used as a proof-of-concept. The performance of previously manufactured cells is analyzed to get an insight into the performance of IBC cells.

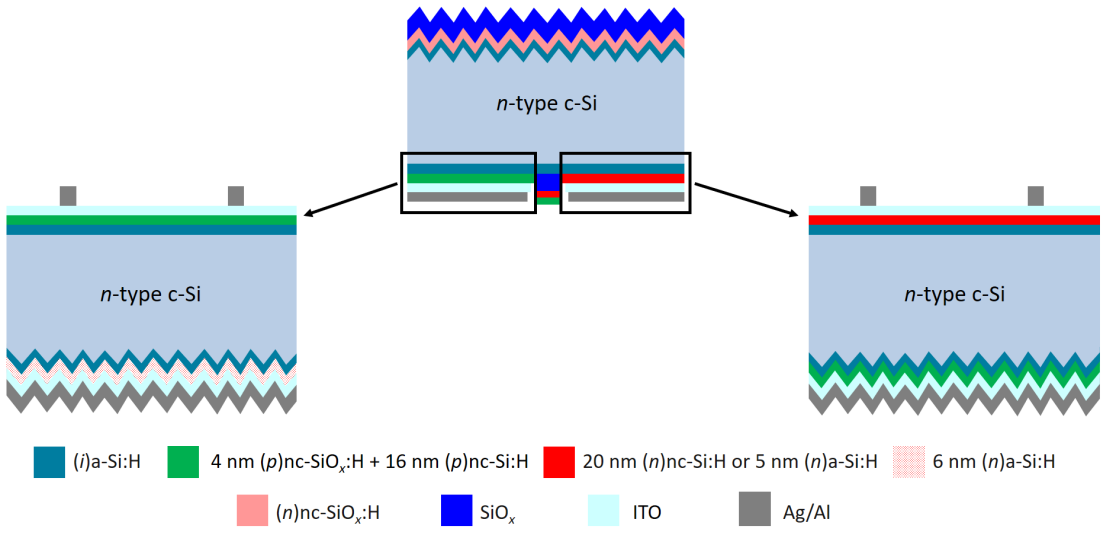


Figure 4.1: The structure of standard IBC-SHJ and corresponding FBC-SHJ solar cells with Si-based doped layers. FBC-SHJ devices are fabricated by [85].

Figure 4.1 shows the structure of a standard IBC-SHJ device together with corresponding FBC devices that have been used as a proof-of-concept. In order to check the contact stacks, the investigated stack is deposited on the front side of the cell due to the smaller metal contact area leading to stricter requirements for successful carrier collection. As all IBC-SHJ devices with Si-based doped layers were manufactured with a flat rear side, single-side textured wafers with a flat front side were used as a substrate for proof-of-concept cells. On the rear side of FBC devices, standard electron and hole

collecting contact stacks developed within the PVMD group by [86], [23], [87], [85] are used. For the front side, three different contact stacks (involving (n)nc-Si:H, (n)a-Si:H and (p)nc-SiO$_x$:H + (p)nc-Si:H) have been deposited in order to compare their performance.

In Figure 4.1 on the bottom left front junction (FJ) FBC device is shown. In the case of FJ devices, p-type layer is deposited on the front side of the device. (p)a-Si:H layer can be used for hole collection. However, optimizing (p)a-Si:H is challenging due to its high parasitic absorption [88] and inferior doping efficiency compared to (n)a-Si:H [57]. Moreover, band bending at (p)a-Si:H/TCO interface has to be well optimized to ensure successful hole collection, which leads to additional constraints to optimization of (p)a-Si:H [89]. (p)nc-SiO$_x$:H can be used as a good alternative as its optical and electrical properties can be tuned easily [44]. By depositing (p)nc-Si:H on top of (p)nc-SiO$_x$:H, hole selective transport can be enhanced. Namely, while (p)nc-SiO$_x$:H enhances passivation and hole accumulation at c-Si/a-Si interface due to its high E$_G$, (p)nc-Si:H improves transport at (p)nc-Si:H/ITO interface [87]. (p)nc-SiO$_x$:H + (p)nc-Si:H bilayer is implemented in standard IBC devices based on the proof-of-concept device presented in Figure 4.1 on the bottom left.

In the case of rear junction (RJ) devices (Figure 4.1 on the bottom right), the layer on the front side is n-type Si-based material. Commonly, thin (below 10 nm) (n)a-Si:H layers are used in order to reduce parasitic absorption. However, due to the limited doping efficiency of a-Si:H, thin layers allow for a higher recombination rate making it challenging to achieve both good optical and electrical properties [90]. Alternatively, (n)nc-Si:H can be used for n-type contact [91]. As it consists of a crystalline phase embedded in the amorphous matrix, nc-Si:H layers are characterized by better doping efficiency compared to a-Si:H counterparts and efficient carrier transport through a crystalline phase. Although the use of (n)nc-Si:H is characterized by better electrical properties compared to thin (n)a-Si:H, etching of (n)nc-Si:H during IBC cell manufacturing can pose additional difficulties due to the mix of a crystalline and amorphous phase in the material. Therefore, proof-of-concept devices with both (n)nc-Si:H and (n)a-Si:H on the front side are presented.

In the case of tunneling IBC devices, the contact stacks presented above are modified (Figure 4.2). Hole collection is achieved through (p)nc-SiO$_x$:H + (p)nc-Si:H bilayer with increased thickness, while electron collection is achieved through tunneling recombination junction (TRJ) consisting of (n)nc-Si:H and thicker (p)nc-SiO$_x$:H + (p)nc-Si:H bilayer. The thickness of p-type layers is increased from 4 nm to 10 nm for (p)nc-SiO$_x$:H and from 16 nm to 30 nm for (p)nc-Si:H to achieve better doping efficiency [91] which is necessary for efficient carrier collection in TRJ [61]. The reason for choosing doped nanocrystalline layers instead of amorphous counterparts for application in tunneling IBC devices is presented in detail in Section 2.3.1.

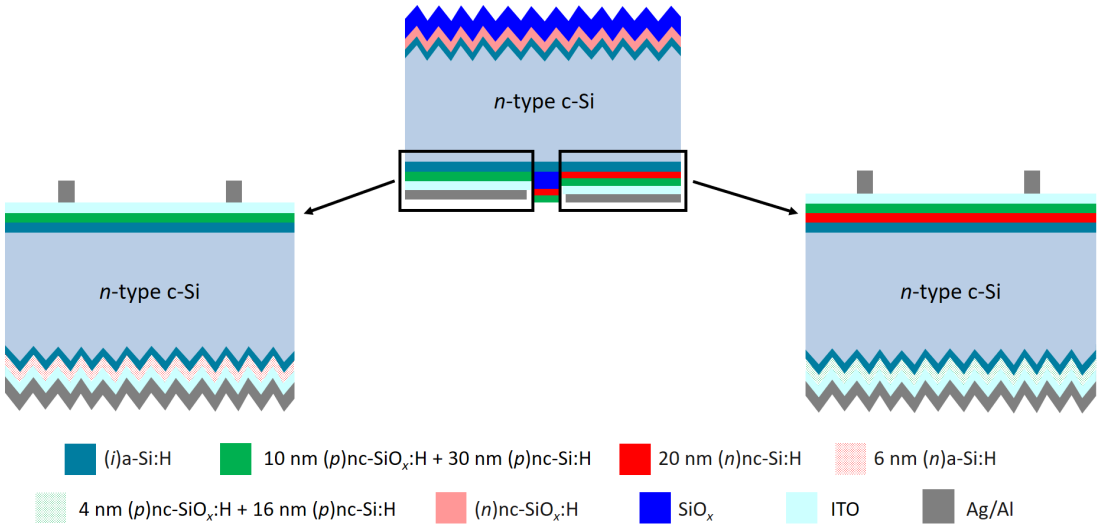


Figure 4.2: The structure of tunneling IBC-SHJ and corresponding FBC-SHJ solar cells with Si-based doped layers. FBC-SHJ devices are fabricated by [85].

FBC device featuring TRJ consisting of (n)nc-Si:H and (p)nc-SiO$_x$:H + (p)nc-Si:H bilayer at the front side of the device was fabricated by [85] and used as a proof-of-concept in this project. The FJ FBC device with 10 nm (p)nc-SiO$_x$:H + 30 nm (p)nc-Si:H bilayer was not fabricated by [85] or within this project. However, as presented in [87] and demonstrated within the PVMD group, devices with (p)nc-SiO$_x$:H + (p)nc-Si:H bilayer of varying thickness have shown FF over 75% and V$_{OC}$ around 700 mV. Moreover, thicker nanocrystalline layers are characterized by a higher crystalline fraction, therefore, bilayer consisting of 10 nm (p)nc-SiO$_x$:H + 30 nm (p)nc-Si:H is expected to work comparably well or better than 4 nm (p)nc-SiO$_x$:H + 16 nm (p)nc-Si:H bilayer. Hence, implementation of this contact stack in IBC devices is expected to be effective.

In Table 4.1 the results of single-side textured FBC devices fabricated by [85] are presented. Manufactured devices demonstrate FF over 80% and V$_{OC}$ over 700 mV, showing that developed contact stacks can be successfully implemented into solar cells. Presented results are used as a proof-of-concept of working contact stacks prior to the implementation in IBC devices which will be explained in detail in the following Sections.

Table 4.1: The results of proof-of-concept FBC-SHJ solar cells fabricated by [85].

Front contact (stack)	**Application in IBC devices**	**J$_{SC}$ (mA/cm^2)**	**V$_{OC}$ (mV)**	**FF (%)**	**η (%)**
20 nm (n)nc-Si:H	BSF	33.2	714	80.7	19.1
5 nm (n)a-Si:H	BSF	33.6	704	80.7	19.1
4 nm (p)nc-SiO$_x$:H + 16 nm (p)nc-Si:H	Emitter	33.4	705	80.5	18.9
10 nm (p)nc-SiO$_x$:H + 30 nm (p)nc-Si:H + 20 nm (n)nc-Si:H	BSF	33.2	709	80.9	19.1

4.2. Fabrication of tunneling IBC-SHJ solar cells

The first set of IBC-SHJ devices was manufactured based on the adapted approach developed by Yifeng Zhao during his master thesis in the PVMD group at Delft University of Technology [86]. This approach was selected as a starting point of the project due to its relative simplicity and fewer steps involved compared to the manufacturing of standard IBC-SHJ devices. The steps involved in this approach are presented in Figure 4.3.

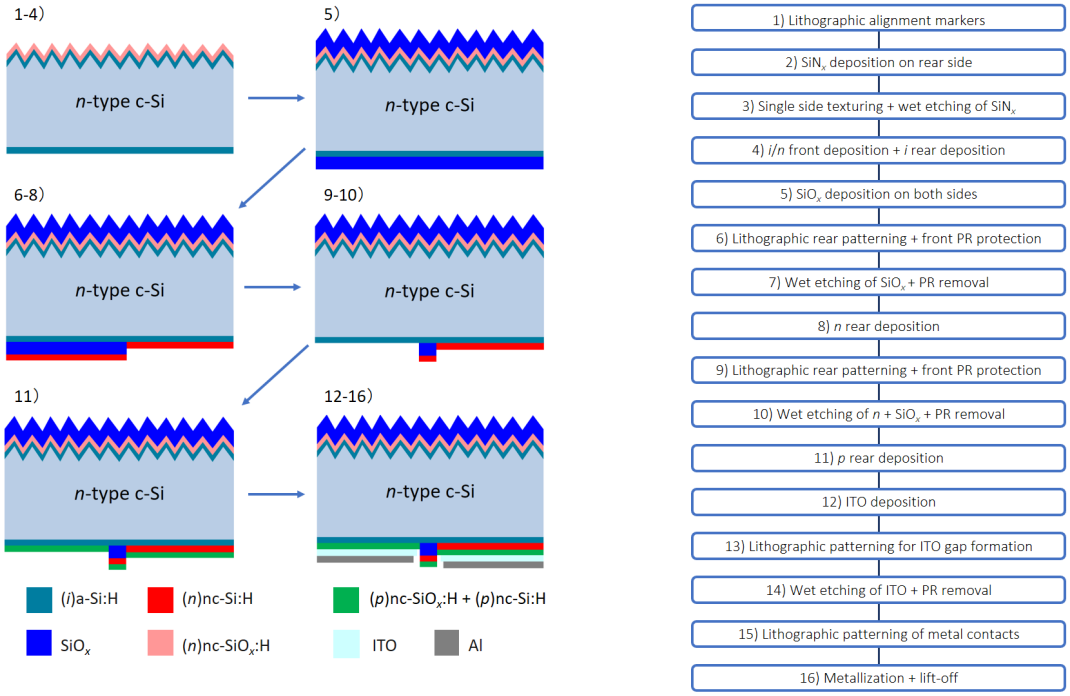


Figure 4.3: Flowchart of tunneling IBC-SHJ solar cell manufacturing process using wet etching steps.

The single-side textured FZ <100> n-type c-Si wafers are used as a substrate for the fabrication of IBC-SHJ devices. In order to perform texturing of only one side of the wafers, SiN_x is deposited on one side of double-side polished wafers by PECVD as a protection layer. The wafers are etched in TMAH solution in order to form random pyramids on the c-Si surface as described in Section 3.1.1. Once the texturing is completed, SiN_x is removed by etching in the BHF solution. NAOC standard cleaning procedure is performed three times [39] and, directly after the last Marangoni step, the wafers are loaded in AMIGO for the deposition of (i)a-Si:H on the rear side, and the deposition of (i)a-Si:H and (n)nc-SiO_x:H on the front side. Afterwards, SiO_x is deposited in PECVD in Kavli Nanolab at 150°C. SiO_x serves as ARC at the front side of the device and as a sacrificial layer during etching steps at the rear side. The first photolithography step is applied to open the BSF area prior to deposition of (n)nc-Si:H. SiO_x is etched from the BSF area with 0.55% HF solution, while the emitter area and the entire front surface were protected with photoresist.

Once the BSF region is open and the photoresist is removed with acetone, another 0.55% HF dip is applied in order to remove the native oxide from the rear side of the wafer. Directly after the 0.55% HF dip, the wafers are loaded in AMIGO for (n)nc-Si:H deposition on the full rear area. Afterwards, in order to open the emitter area, the second photolithography step is applied. BSF region and the entire front side are covered with photoresist, while (n)nc-Si:H is etched in 1% KOH solution followed by etching of SiO_x in 0.55% HF solution. The choice of the etching solution was based on the etching selectivity of the materials and the difference in etching rates. As the etching rate of Si in KOH is significantly higher compared to the etching rate of SiO_x, (n)nc-Si:H can be fully removed by KOH solution, while SiO_x stays intact and acts as etching barrier. Similarly, SiO_x can be fully removed by HF solution, while (i)a-Si:H is not damaged.

Once the etching is completed, the photoresist is removed and the wafers are dipped in 0.55% HF to remove the native oxide from the rear side. Following the native oxide removal, the wafers are loaded in AMIGO for full area deposition of (p)nc-SiO_x:H + (p)nc-Si:H bilayer. Next, ITO is deposited in ZORRO. The third lithographic patterning step is included for ITO gap formation in order to prevent shunting at the contact of emitter and BSF region. Etching of ITO in 37% HCl is done to create the gap between the two regions. The last photolithography step is applied prior to metalization. After the full area Al deposition, wafers are immersed in an acetone ultrasonic bath for metal lift-off.

4.2.1. Process challenges

In total, 16 steps can be recognized during the fabrication of tunneling IBC solar cells. However, in order to preserve passivation quality while fully opening BSF and emitter regions, steps 6 and 7 and steps 9 and 10 can be marked as the most critical steps of the process.

Photolithography and etching

To successfully complete photolithography steps, test samples were used to find the most suitable photoresist, optimize exposure and development steps and check the effect of photoresist removal with different methods. Furthermore, test samples were used to find the most suitable etching solution and check etching uniformity and rate.

To ensure that passivation quality is preserved, SiO_x was deposited on a test sample with (i)a-Si:H layer on the rear side and (i)a-Si:H and (n)nc-SiO_x:H on the front side, as proposed in the flowchart in Figure 4.3. Figure 4.4 shows that τ_{eff} improves with the deposition of SiO_x, potentially due to annealing of (i)a-Si:H and better incorporation of hydrogen into the layer. During the etching tests, front side was coated by positive photoresist to ensure front SiO_x is not removed during processing. The first etching tests were performed on samples without photoresist pattern on the rear side. SiO_x was etched from the full rear area with 0.55% HF and, as shown in Figure 4.4 with a black circle, passivation drop can be observed but τ_{eff} falls to 1028 µs. This passivation drop can possibly be assigned to etching of the surface (i)a-Si:H, which will be explained further in the next section. During this test, the etching rate was determined to be around 75 nm/min with observance of change from hydrophilic to hydrophobic behavior of the surface (SiO_x is hydrophilic, while (i)a-Si:H is hydrophobic).

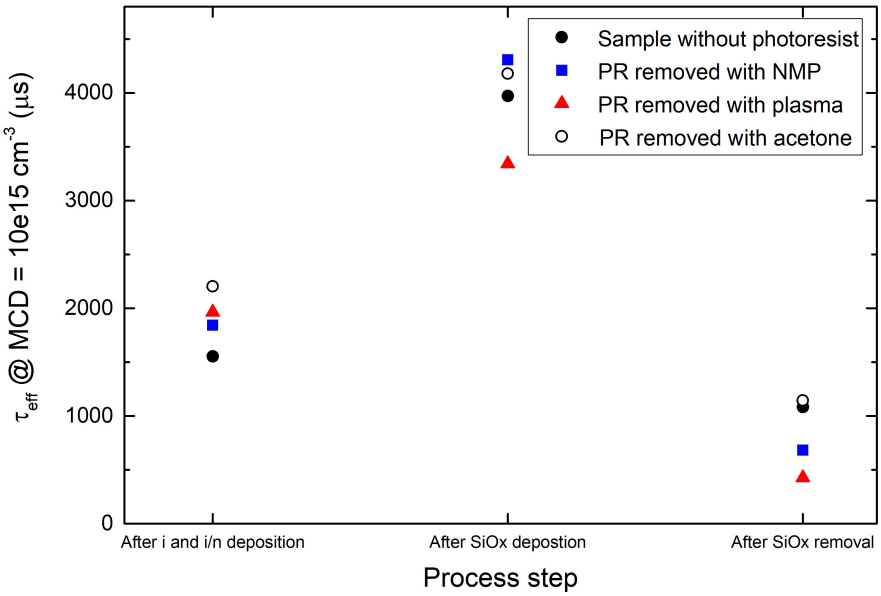


Figure 4.4: Effective carrier lifetime depending on the photoresist removal method.

Afterwards, negative photoresist (AZ nLOF 2020) was used to pattern the rear side of additional test samples (shown in Figure 4.4 with a blue square and a red triangle). Exposure time was determined based on photoresist type and thickness and lamp intensity, while development time is based on photoresist type and thickness. During the preliminary tests, poor photoresist adhesion was noticed during development. This was improved by including an HMDS (hexamethyldisilazane) step prior to photoresist coating and a hard (post-development) bake step. Once photolithography steps were concluded, SiO_x was etched from the BSF region only. Following the removal of photoresist, the lifetime of test samples was measured and a significant drop in passivation is observed compared to the sample without photoresist (Figure 4.4, marked with a blue square and a red triangle). For negative photoresist removal, both NMP (1-methyl-2-pyrrolidone) (blue square in Figure 4.4) and oxygen plasma (red triangle in Figure 4.4) were tested, however, both of these methods damaged passivation quality. A possible reason for this damage is that part of (*i*)a-Si:H layer is removed during resist removal by NMP which is an organic base or by oxygen plasma.

Subsequently, test samples with positive photoresist (AZ ECI 3027) were fabricated, as positive photoresist can be removed with acetone which is less damaging to the thin (*i*)a-Si:H layer. This was also observed during the performed tests as shown in Figure 4.4 with a hollow circle. Therefore, only positive photoresist was used for photolithography in this project. Exposure and development time have been determined following the same steps as in the case of negative photoresist and as explained in Section 3.3 and adhesion was improved by including HMDS and hard bake steps.

Lastly, etching of (*n*)nc-Si:H was addressed. From [92], it is known that low-concentration KOH solution at room temperature is a good candidate for the etching of thin doped Si-based layers. Accordingly, in this research, 1% KOH solution at room temperature was chosen for (*n*)nc-Si:H etching. In order to determine the etching rate and uniformity, 4 x 3 cm^2 test samples with (*n*)nc-Si:H were prepared and spectroscopic ellipsometry was used to track the thickness change after every 30 seconds of etching. The etching tests have shown poor etching uniformity of (*n*)nc-Si:H, however, as SiO_x serves as the etching barrier underneath (*n*)nc-Si:H, overetch can be allowed to fully remove (*n*)nc-Si:H layer. The etching rate used for complete removal of (*n*)nc-Si:H is determined to be around 10 nm/min.

Passivation damage following SiO_x removal

As shown in Figure 4.4 with black and hollow circles, passivation quality drops after the opening of the BSF region even when no or only positive photoresist is used. The possible reason for this can be related to deposition and removal of SiO_x causing a damage to (*i*)a-Si:H. Namely, as SiO_x is deposited on (*i*)a-Si:H, the surface of (*i*)a-Si:H can be oxidized. Hence, during the etching of SiO_x in 0.55% HF

the oxidized surface of (i)a-Si:H can also be removed. This leads to thinner (i)a-Si:H and decay in passivation quality.

4.2.2. Results and analysis

In the course of this project, three types of cells with different geometries are fabricated. In Figure 4.5, the sketch of the rear side of the wafer and manufactured cells is presented, while the main features of the cells are shown in Table 4.2. Half-pitch represents the distance between the middle of the emitter to the middle of the neighboring BSF. The devices are designed such that approximately 60% and 40% of the pitch is covered by the emitter and BSF, respectively, as proposed by [62] and a 7 µm gap is used to isolate the emitter and BSF to prevent shunting.

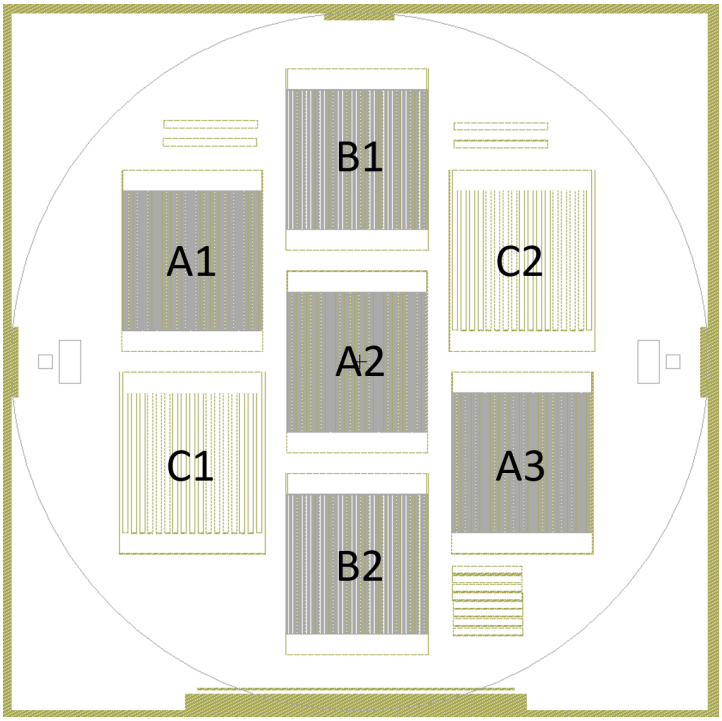


Figure 4.5: Sketch of the rear side of the wafer with manufactured IBC-SHJ solar cells.

Table 4.2: The geometry of three types of manufactured solar cells.

Cell	**A1-A3**	**B1-B2**	**C1-C2**
Pitch (µm)	300	650	1200
Emitter width (µm)	180	390	720
BSF width (µm)	106	246	466
Metal coverage (%)	59.59654	61.27207	84.13267
Cell area (cm^2)	4.047014	4.09224	4.186602

The results of fabricated tunneling IBC-SHJ solar cells are presented in Figure 4.6. Even though theoretically smaller pitch size should yield the best results due to the decrease in series resistance [61] and improved FF [62], from Figure 4.6 it can be seen that cells with a larger pitch show better performance. This can be explained by the increased edge-to-area ratio and the defects present at the edges of emitter and BSF due to manufacturing, where recombination is more likely to take place [61]. Defects at the edges of emitter and BSF can be caused by incomplete etching, where material residues can act as recombination centers, or by over-etching, which can potentially lead to damage to the passivating layer. Additionally, larger metal coverage, which is present in devices with larger pitch, has a positive impact on FF of the devices as it decreases resistive losses [93]. The best device

manufactured with this flowchart achieved an efficiency of 13.9% with FF of 62.66% and V_{OC} of 630 mV.

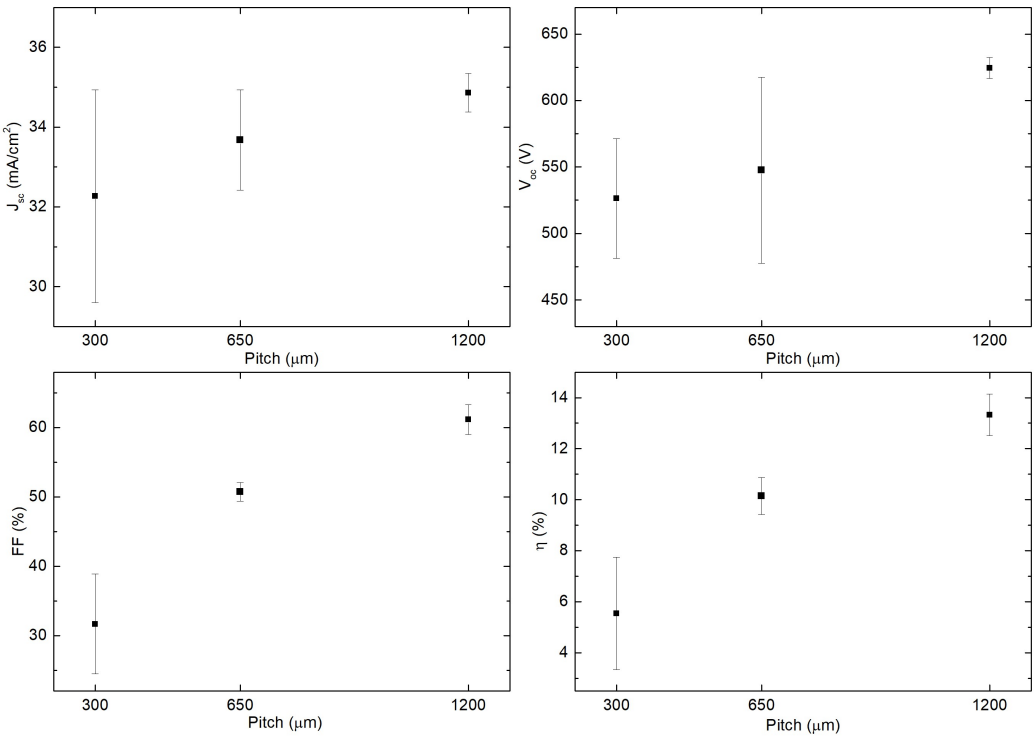


Figure 4.6: External parameters of single-side textured tunneling IBC cells with different pitch sizes.

J_{SC} values in the range between 30 and 35 mA/cm^2 are likely influenced by generally poor device performance and insufficient electron collection. Moreover, light management of devices with flat rear sides is not optimal compared to double-side textured devices and anti-reflection coating (ARC) of the manufactured devices is not optimized, which further decreases J_{SC}. To improve light trapping, double-side textured wafers were used for the fabrication of devices presented in Chapter 5. However, due to the limited time, ARC optimization was outside the scope of this project.

Similarly, low V_{OC} values around 500 to 630 mV are observed, which can be related to drop in τ_{eff} of cell precursors during the manufacturing process as shown in Figure 4.7. Following the etching of SiO_x, as well as the etching of (n)nc-Si:H and SiO_x, τ_{eff} significantly drops compared to the preceding steps indicating passivation damage. As mentioned in Section 4.2.1, the potential cause of passivation damage during etching steps can be related to the removal of SiO_x and consequently thinner (i)a-Si:H.

An additional drop in τ_{eff} occurs as a result of p-type layer stack deposition, which was also observed by [61]. According to [61], the decreased value does not correspond to the actual passivation quality of device precursors and cannot be reliably compared to prior τ_{eff} values during processing.

Moreover, a decrease in τ_{eff} is observed following the metalization. Hence, another cause of low V_{OC} can be related to the electron beam evaporation. The damage can potentially be caused by vacuum UV radiation or high-energetic particle bombardment leading to increased number of traps and damage to c-Si surface [94], [95], [96]. This damage can be avoided by replacing Al with thermally evaporated Ag or electroplated Cu. However, due to poor adhesion of Ag on polished wafer, Ag lift-off cannot be performed effectively. Thus, Ag metalization is applied for DST samples only which will be discussed in Chapter 5.

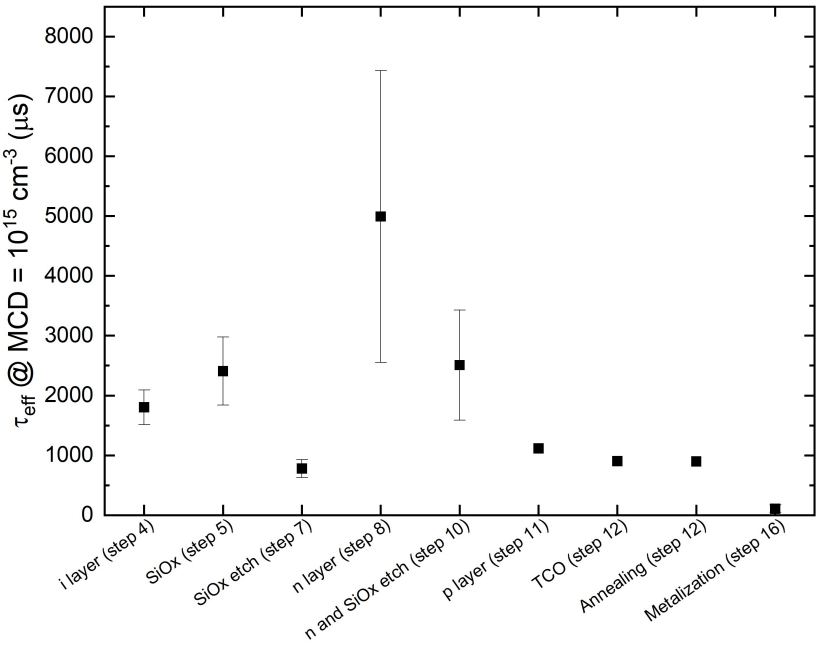
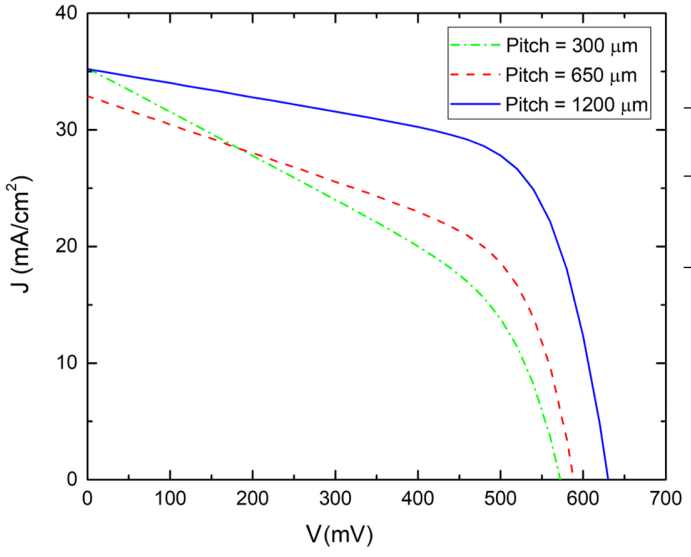


Figure 4.7: τ_{eff} of cell precursors during fabrication process.

Lastly, poor FF is observed for all manufactured devices and shunting can be noticed from the J-V curves shown in Figure 4.8, which is supported by R_{SH} values measured with SunsV_{OC} setup. Internal shunting of TRJ structure can be recognized as a possible reason for low shunt resistance. The probable cause of internal shunting is the high lateral conductivity of the *p*-type nc-Si:H-based blanket layer [61]. However, the lowest shunt resistance observed in the device with the smallest pitch can potentially be related to the largest influence of manufacturing defects due to the increased edge-to-area ratio.



Pitch (µm)	J_{SC} (mA/cm²)	V_{OC} (mV)	FF (%)	η (%)	R_{SH} (Ωcm²)
300	35.31	572	39.73	8.03	60
650	34.56	597	51.68	10.66	111
1200	35.20	630	62.66	13.90	299

Figure 4.8: J-V curves, external parameters and R_{SH} values of best single-side textured tunneling IBC-SHJ solar cells with different pitch sizes.

Conclusions and outlook on the tunneling IBC-SHJ architecture
The first tunneling IBC-SHJ devices have been manufactured successfully, with the best device reaching an efficiency of 13.9%. However, all manufactured devices are characterized by low shunt resistance which highly impacts device performance. To tackle this, standard IBC-SHJ devices will be investigated in the next Section as the absence of the *p*-type nc-Si:H-based blanket layer results in fewer constraints on both *p* and *n* layer properties. Moreover, requirements on lateral conductivity of doped layers can be neglected in the case of standard IBC devices as long as a gap between BSF and emitter is included. Additionally, the restriction on lateral conductivity of *p*-type nc-Si:H-based blanket layer will be further investigated by replacing it with a layer of lower lateral conductivity in Chapter 5.

4.3. Fabrication of standard IBC-SHJ solar cells

During this research, three flowcharts for the fabrication of standard IBC-SHJ devices are proposed. The first two (Section 4.3.1 and Section 4.3.2) include wet etching steps for the removal of doped layers. Additionally, a flowchart using a combination of wet and dry etching for removal of SiO_x and doped layers, respectively, is proposed in Section 4.3.3.

4.3.1. Fabrication of standard IBC-SHJ solar cells using wet etching

Firstly, the extension of the flowchart for tunneling IBC devices is presented in Figure 4.9. Compared to the flowchart from Figure 4.3, two additional lithography steps are added in order to pattern the emitter region, and an additional SiO_x layer is included to serve as an etching barrier during emitter patterning. As it can be seen in Figure 4.9, steps 11 to 16 are added to the processing, leading to more complex manufacturing. Additional SiO_x layer is etched with 0.55% HF, while *p*-type Si bilayer is etched with 1% KOH. As SiO_x with the same thickness and deposition conditions is implemented, the same etching time was necessary for its removal, while additional etching tests are necessary to determine the rate for *p*-type bilayer etching.

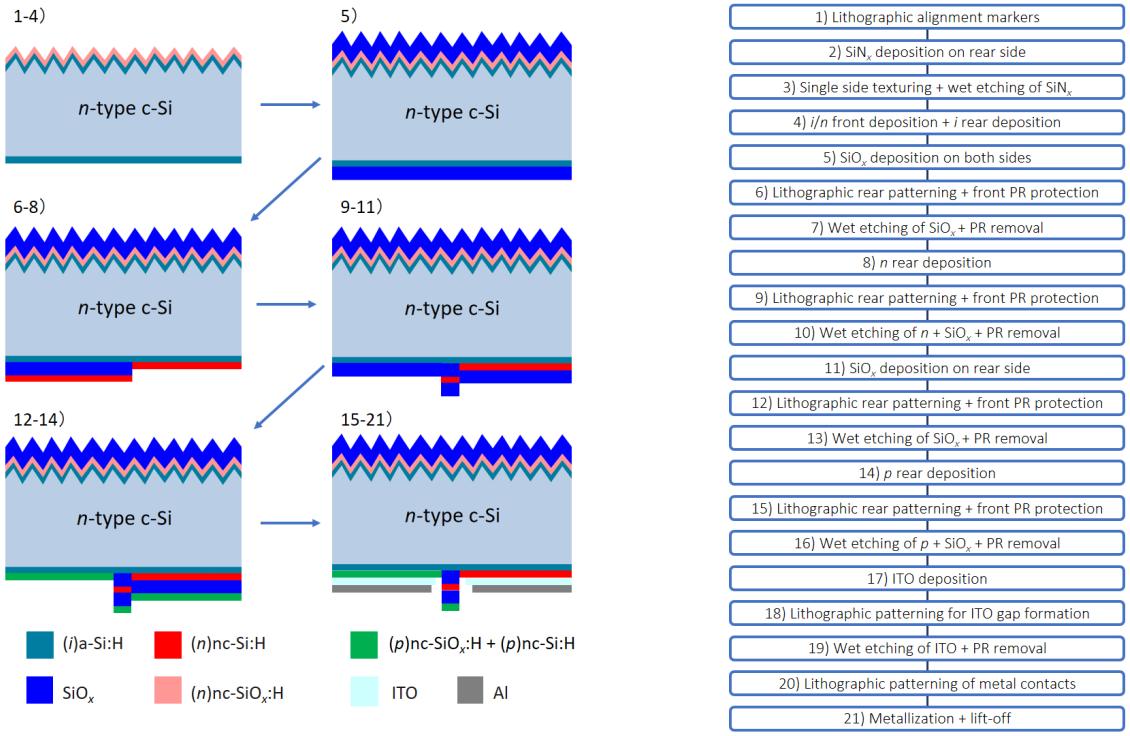


Figure 4.9: Flowchart of standard IBC-SHJ solar cell manufacturing process using wet etching steps.

Process challenge - Leftover material after the etching process
The main challenge of this process was encountered in step 10 after the removal of SiO_x from the emitter prior to deposition of (*p*)nc-SiO_x:H + (*p*)nc-Si:H bilayer. As shown in Figure 4.10, following the removal of SiO_x, the emitter area is not entirely clean. This material could not be removed with any

of the photoresist removal methods including oxygen plasma treatment. However, the leftover material can potentially be related to photoresist that is chemically modified during the etching process and redeposited in the emitter region.

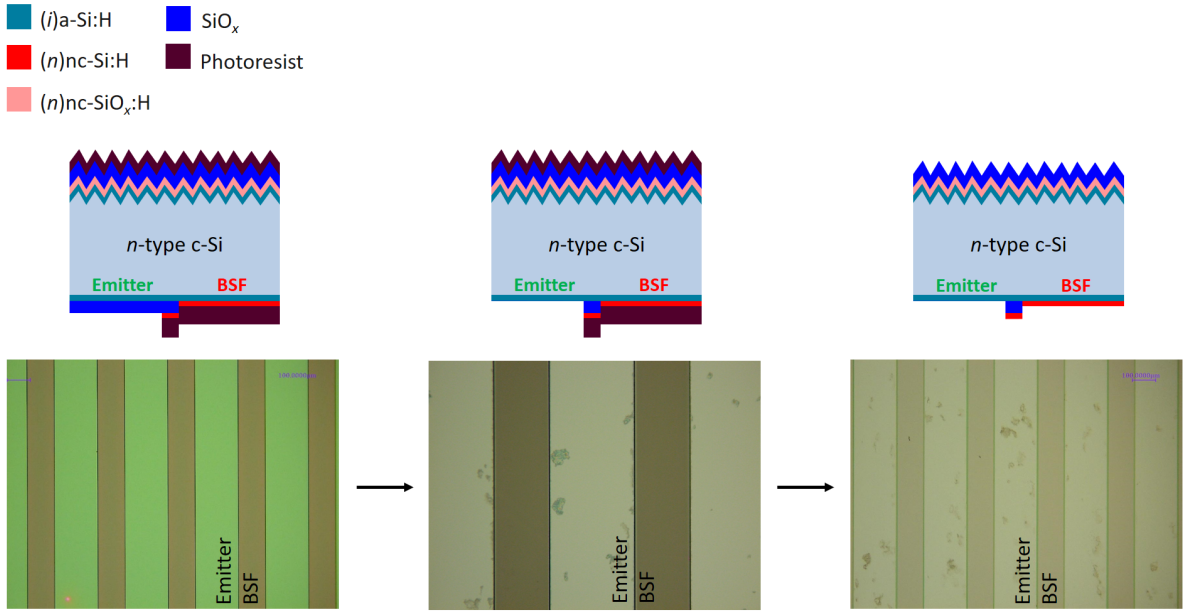


Figure 4.10: Cell precursor sketches in the case of ideal etching and optical microscope images of etching residues resulting from consequent removal of (n)nc-Si:H and SiO_x (step 10 in Figure 4.9).

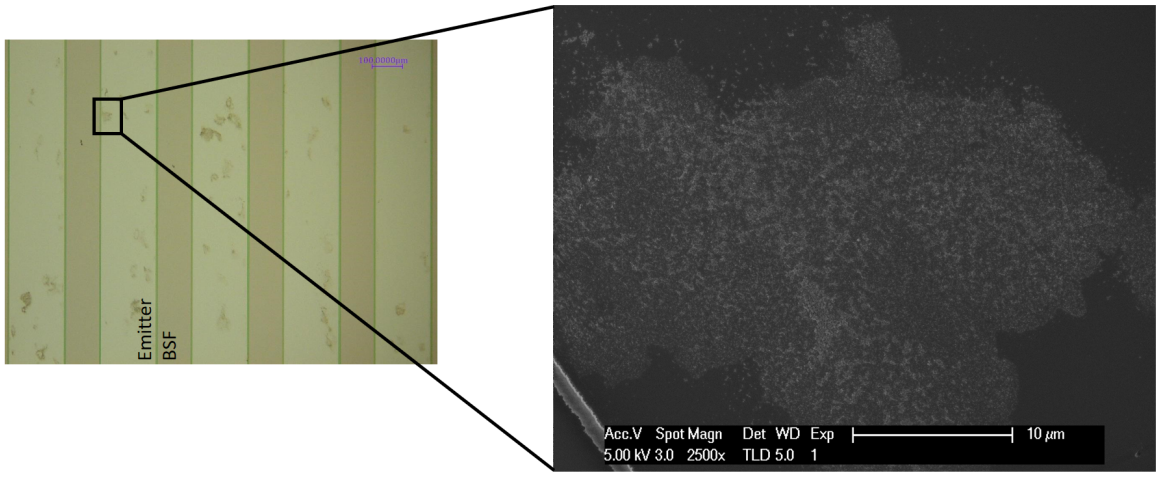


Figure 4.11: Optical microscope (left) and SEM (right) image of etching residues resulting from consequent removal of (n)nc-Si:H and SiO_x.

This etching step was part of the flowchart presented in Figure 4.3 and originally etching of (n)nc-Si:H and SiO_x was completed successfully. A possible reason for this switch can be related to nonoptimal conditions during photolithography steps, however, further analysis is required to get a better understanding of the composition and the origin of leftover material. This was not further investigated in this project due to the time restrictions. Instead, as the flowchart proposed in this Section consists of a large number of steps, an alternative flowchart is presented in the following Section.

4.3.2. Simplified fabrication of standard IBC-SHJ solar cells using wet etching

The flowchart presented in Section 4.3.1 consists of 21 steps with 6 steps involving photolithographic patterning, which significantly complicates the processing of solar cells and leads to high fabrication costs. In the previously proposed flowcharts, SiO_x layer is used as etching barrier in order to preserve (i)a-Si:H on the surface of the wafer and eliminate the need for repassivation of c-Si surface. In the flowchart presented in Figure 4.9, SiO_x barrier is not included and the complete i/p contact stack is removed. Thus, the flowchart is simplified from 21 to 17 steps and the number of photolithography steps is reduced from 6 to 4 to reduce complexity and accelerate the fabrication process. Accordingly, the steps involved in this flowchart differ significantly compared to the previously introduced flowcharts.

For manufacturing devices in the flowchart from Figure 4.12, single-side textured FZ <100> n-type c-Si wafers are used as a substrate. The texturing is performed in TMAH solution, while the front side is protected by PECVD SiN_x. Following the texturing, SiN_x is removed in the BHF solution and NAOC standard cleaning is performed three times [39]. Wafers are then loaded in AMIGO for the deposition of (i)a-Si:H and (n)nc-SiO_x:H on the front side and the deposition of (i)a-Si:H and (p)nc-SiO_x:H + (p)nc-Si:H on the rear side. SiO_x is deposited in PECVD in Kavli Nanolab serving as ARC at the front side of the device and as an etching mask at the rear side. Photolithography is used to pattern the BSF and SiO_x is removed with 0.55% HF solution.

i/p layer stack is removed from the BSF region, followed by the removal of SiO_x mask. Subsequently, (i)a-Si:H and (n)a-Si:H are deposited. (n)a-Si:H is chosen instead of (n)nc-Si:H as it is expected to have better etching uniformity being a homogeneous material consisting of an amorphous phase only rather than a mix of amorphous and nanocrystalline phase. Further, the rear side is patterned and the i/n layer stack is removed from the emitter region. Lastly, ITO and Al deposition and patterning are performed.

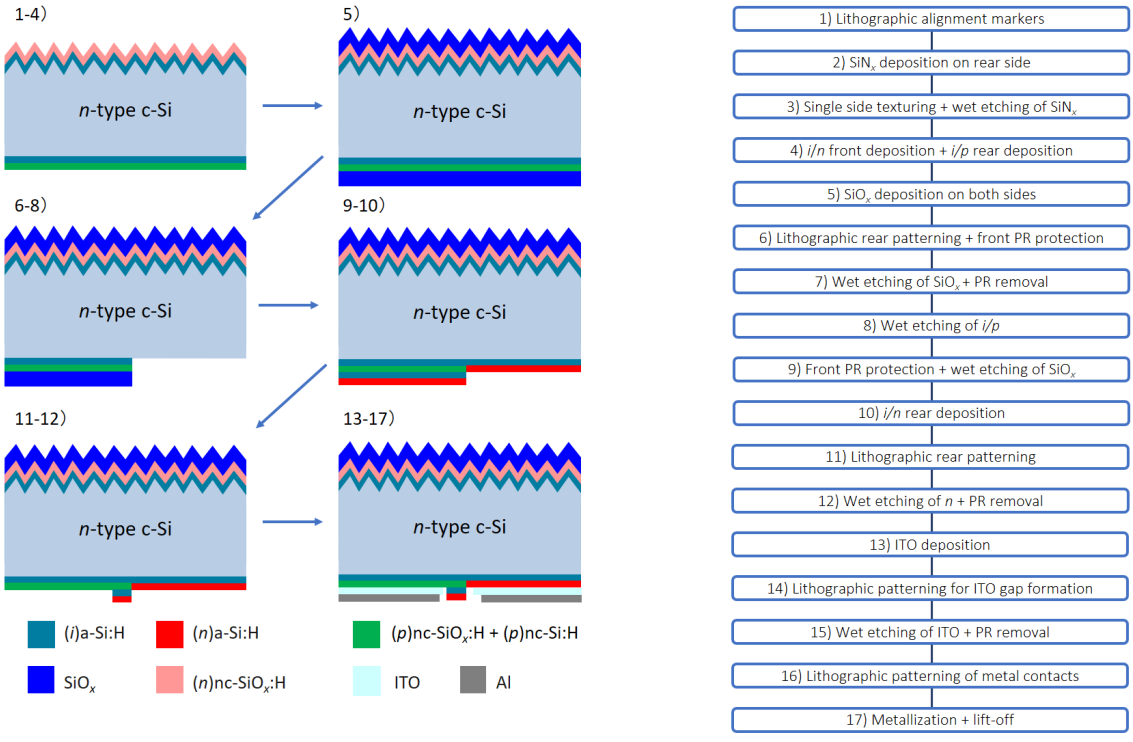


Figure 4.12: Simplified flowchart of standard IBC-SHJ solar cell manufacturing process using wet etching steps.

Process challenge - Etching of Si layers

Uniform etching of intrinsic and doped Si layers is crucial for the fabrication of devices using the simplified flowchart as they are deposited directly on the c-Si surface. Therefore, the order of doped

layer deposition, type of doped layers, and etching solution type and concentration have to be carefully selected.

The deposition of (p)nc-SiO$_x$:H + (p)nc-Si:H bilayer prior to the deposition of n-type layer is adopted due to the slower etching rate of p-type silicon layers compared to n-type equivalents [97]. For etching of p layer stack, polysilicon etch (consisting of HNO_3, HF and water) is selected due to the presence of (p)nc-SiO$_x$:H in the stack as oxidic layers cannot be etched by alkaline solutions such as KOH or TMAH. However, photoresist is removed by polysilicon etch due to the presence of HNO_3 in the solution, and SiO$_x$ is used as an etching mask for the opening of the BSF region. SiO$_x$ is etched at a slower rate in polysilicon etch compared to Si layers and a significantly thicker layer of SiO$_x$ is deposited to ensure that emitter area is protected (800 nm of SiO$_x$ compared to up to 20 nm for Si layers). For n-type layer, (n)a-Si:H is adopted as it can be etched more uniformly compared to (n)nc-Si:H. Moreover, it can be etched with low concentration KOH or TMAH solution, which etches p-type Si layers slower compared to n-type and intrinsic layers and no etching barrier is necessary.

Nevertheless, when conducting etching tests of the above layers in the corresponding solutions, relatively poor uniformity was observed. In Figure 4.13, nonuniform etching of the i/n layer stack in 1% KOH solution is illustrated. i/n layer stack is deposited on a polished wafer with 150 nm SiO$_x$ layer in order to track uniformity of etching by eye. After 30 seconds of etching, some of the i/n layer stack is fully removed from the wafer surface, while after 2 minutes the layer is still not entirely removed.

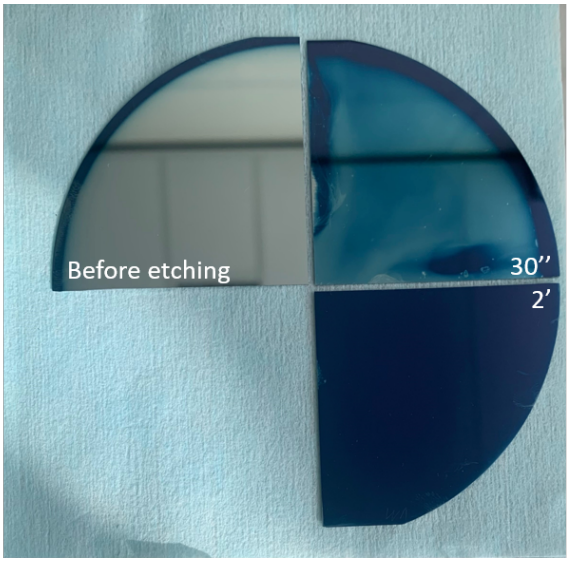


Figure 4.13: Samples showing nonuniform etching of (i)a-Si:H/(n)a-Si:H layer stack in 1% KOH solution after 30 seconds (top right) and 2 minutes (bottom right).

As proposed by [92], the uniformity of KOH etching could be improved by introducing isopropyl alcohol (IPA) as an additive, but no significant improvements were observed. Additionally, etching tests were conducted with increased concentrations of KOH of 2% and 5%, as well as in TMAH solution. Nonetheless, uniform etching of i/n layer stack was not achieved, and, in order to fully remove the stack and not cause damage to c-Si bulk, additional layers acting as etching barriers are necessary. This would lead to additional process complexity and it was not implemented in the course of this project. Thus, in order to achieve better etching uniformity, an alternative flowchart involving a combination of wet and dry etching for SiO$_x$ and doped layer removal, respectively, is proposed and presented in the following Section.

4.3.3. Fabrication of standard IBC-SHJ solar cells using dry etching

In Figure 4.14, a flowchart for fabrication of standard IBC devices using a combination of wet and dry etching steps is presented. Even though similar to the flowchart from Section 4.3.1, as shown in the Figure below, this flowchart involves 29 process steps, which is a significant increase compared to the initially proposed flowchart presented in Section 4.3.1. The main reason behind increased complexity

is the introduction of the SiO_x mask as a dry etching mask instead of a photoresist mask as photoresist is not allowed in the system used for dry etching. Moreover, once the photoresist is exposed to plasma during dry etching, it requires removal with another plasma treatment. However, as shown in Section 4.2.1, removal of photoresist by plasma treatment leads to a significant decrease in passivation. Therefore, SiO_x is patterned using a photoresist mask and etched in 0.55% HF solution in order to serve both as an etching barrier between doped and intrinsic layers and as a mask for dry etching. The thickness of SiO_x was significantly larger compared to the thickness of both *n*- and *p*-type layers (800 nm of SiO_x compared to up to 20 nm for doped layers) to ensure doped layers can be fully removed while SiO_x mask is still intact.

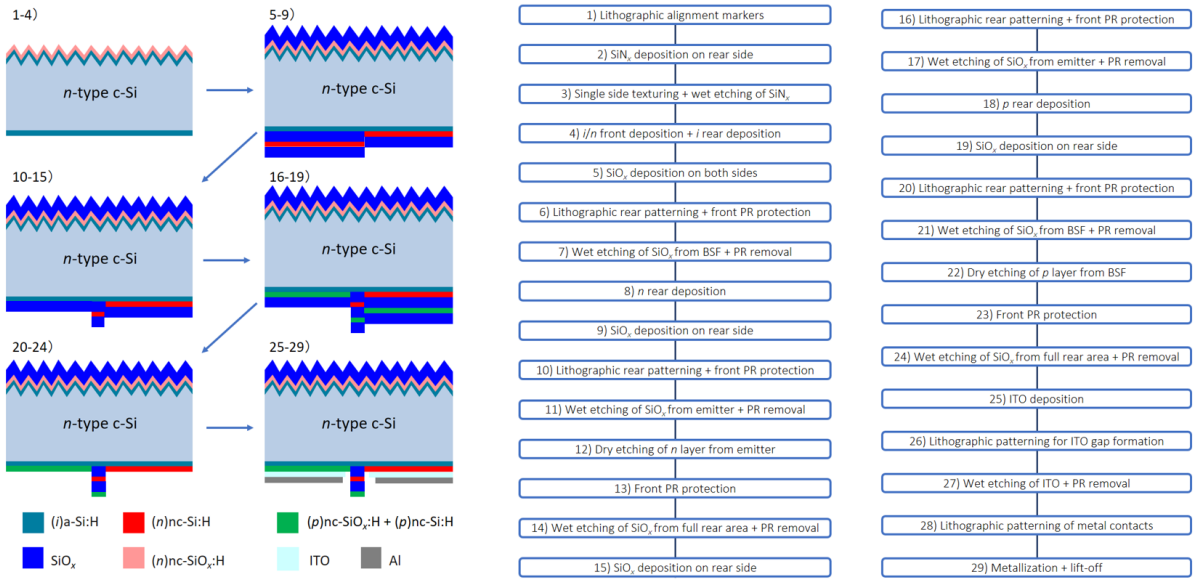


Figure 4.14: Flowchart of standard IBC-SHJ solar cell manufacturing process using dry etching steps.

Dry etching tests

Prior to the manufacturing of devices using dry etching, etching tests were performed to determine the etching rate of (*n*)a-Si:H, (*n*)nc-Si:H and (*p*)nc-SiO_x:H + (*p*)nc-Si:H bilayer. Moreover, SiO_x etching rate was tested in order to ensure that the intact layer of SiO_x remains on the wafer during the etching of doped layers. The thickness change was followed by spectroscopic ellipsomerty measurements. Dry etching was performed by SF_6 and O_2 plasma as proposed by [98]. In Table 4.3, etching rates of tested layers and layer stacks are presented.

Table 4.3: Dry etching conditions and approximate etching rate for materials used in this thesis.

Layer (stack)	Original thickness (nm)	Etching rate (nm/min)	SF_6 (sccm)	O_2 (sccm)	Power density (mW/cm^2)	Pressure (mbar)
(*n*)nc-Si:H	20	19	50	10	138.5	1
(*n*)a-Si:H	8	24	50	10	138.5	1
(*p*)nc-SiO_x:H + (*p*)nc-Si:H	4 + 16	16	50	10	138.5	1
SiO_x	800	13	50	10	138.5	1

Process challenge - Leftover material of the etching process

As shown in Figure 4.14, prior to dry etching of (*n*)nc-Si:H, SiO_x is deposited on the full rear area over (*n*)nc-Si:H in step 9 of the flowchart and removed by wet etching in step 11. However, the removal of SiO_x in this step could not be completed successfully. Figure 4.15 (middle) shows an optical microscope image of residues left in the emitter region following the removal of SiO_x. This can potentially be

related to the delamination of photoresist and consequent redeposition of chemically modified material that could not be removed with any of the standard photoresist stripping methods. Issues during photolithography steps such as inefficient HMDS step or insufficient baking time could be a possible reason for the delamination of photoresist.

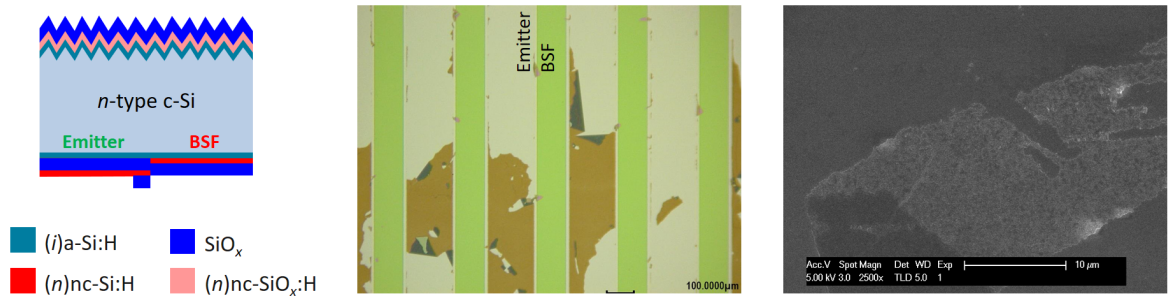


Figure 4.15: Sketch of the process step (left), optical microscope (middle) and SEM (right) image of etching residues resulting from removal of SiO_x.

Due to the complexity of the above manufacturing processes, encountered challenges as well as time constraints, more investigation is needed for the successful manufacturing of standard IBC devices. The focus of future research should be directed towards studying a variety of etching solutions and exploring alternative etching barrier materials (such as SiN_x) in order to successfully fabricate standard IBC devices with photolithography as patterning method. Alternatively, shadow masking can be used for deposition of doped layer replacing photolithography and wet etching.

4.4. Conclusions and outlook

In this Chapter, the fabrication of single-side textured IBC-SHJ devices with Si-based doped layers is presented. In this part of the project, a set of devices featuring a tunneling recombination junction was successfully fabricated. However, likely due to the tunneling IBC structure, low shunt resistance was observed in all fabricated devices significantly limiting their performance.

In order to address this limitation, the focus of the project shifted towards the fabrication of standard IBC devices, as the absence of a blanket layer leads to less sensitivity to internal shunting. Three process flowcharts for manufacturing standard IBC devices are proposed. Yet, each of the proposed flowcharts suffered from nonuniform etching in one or more steps. Hence, due to time constraints of the project, etching steps were not further optimized and more investigation is necessary for the successful fabrication of standard IBC-SHJ solar cells. Nevertheless, as the completed set of IBC devices indicated the main process limitations, adjustments to the original process flowchart are proposed.

To improve light management and enable higher J_{SC}, double-side textured wafers can be introduced as a substrate. Moreover, the front side of the device can be optimized by introducing ARC. By optimizing the properties of SiO_x or introducing an alternative layer as an etching barrier, the damage to (i)a-Si:H due to etching of SiO_x can potentially be minimized resulting in better passivation quality and V_{OC} enhancement. Moreover, alternative metalization methods such as Ag thermal evaporation or Cu electroplating can be implemented instead of Al electron beam evaporation to decrease passivation damage. Lastly, FF can be improved by altering the device structure and contact stacks to overcome the limitation of low shunt resistance. In order to keep the manufacturing process simple and avoid fabrication of standard IBC devices, internal shunting can be omitted by selecting a blanket layer with lower lateral conductivity compared to p-type Si layers that were used in the above-mentioned flowcharts.

Considering the aforementioned recommendations, in Chapter 5 the manufacturing process for IBC devices using novel contact stacks is proposed aiming to overcome the main limitations of TRJ devices while keeping the manufacturing process simple.

5

IBC-SHJ solar cells with MoO_x

As discussed in the previous Chapters, the introduction of IBC solar cell architecture is an important step towards achieving higher efficiencies as the illuminated side of the device can be fully optimized enabling high J_{SC}. By combining it with SHJ technology, high V_{OC} and FF can be achieved. However, to obtain industry appealing production process for IBC-SHJ devices, the number of fabrication steps should be minimized. As introduced in [61], the formation of TRJ can be utilized to reduce the number of patterning steps, as the emitter region does not need to be patterned and *p*-type layer is deposited on the full rear area. However, for the successful formation of TRJ, it is important to collect electrons without resistive losses in the BSF where TRJ is formed. Moreover, ensuring low lateral conductivity of *p*-type layer in the emitter region and preventing the formation of the short circuit in the device is necessary.

In Section 4.2, the fabrication process of IBC-SHJ devices featuring TRJ is addressed, showing low shunt resistance in all fabricated devices. To tackle this, an alternative device architecture with novel contact stacks is introduced in this Chapter. The approach presented in the following Sections aims to keep the number of processing steps as low as in Section 4.2, while ensuring sufficient shunt resistance.

5.1. Introduction to IBC-SHJ solar cells with MoO_x blanket layer

To overcome the issue of internal shunting of TRJ IBC devices, an alternative device architecture is presented in this Section. As depicted in Figure 5.1, *p*-type nc-Si:H-based blanket layer is replaced with MoO_x, which features lower lateral conductivity. In this architecture, hole collection takes place at the contact stack consisting of (*i*)a-Si:H, MoO_x, TCO and metal with an additional PT that can be included to improve (*i*)a-Si:H/MoO_x interface quality [70]. Hole collection contact stack used for devices in this project has been developed by [70] and further improved in PVMD group [66]. The principle of hole collection is explained in detail in Section 2.4.

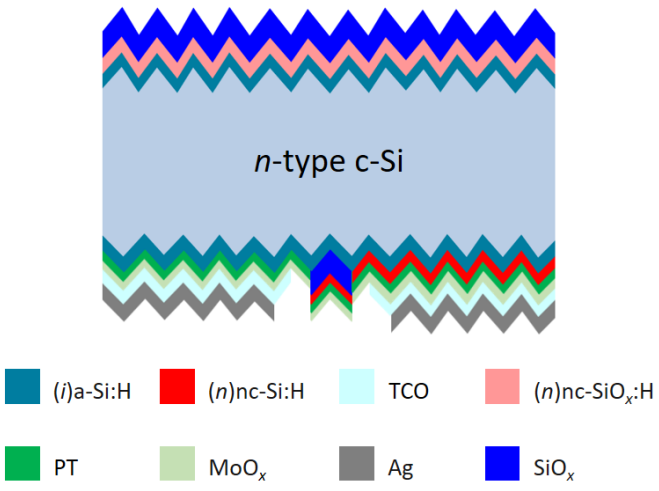


Figure 5.1: The structure of IBC-SHJ solar cell with MoO_x.

On the other hand, this thesis presents a novel contact stack for electron collection. This contact stack includes thick (n)nc-Si:H layer deposited between (i)a-Si:H and MoO_x. Figure 5.2 shows a band diagram of this contact stack. On the left side of the sketch, electrons are accumulated at the c-Si/(i)a-Si:H interface due to band bending induced by highly doped (n)nc-Si:H. Electrons can then overcome the barrier at c-Si/(i)a-Si:H interface mainly via thermionic emission. Once they reach the interface of (n)nc-Si:H with MoO_x, electrons can easily be transported to MoO_x via thermionic emission or direct tunneling. As the large population of electrons accumulates in MoO_x, they are able to cross the barrier at MoO_x/TCO interface via thermionic emission or direct tunneling. As ohmic contact is formed between TCO and metal, electrons can be easily transported to the metal electrodes.

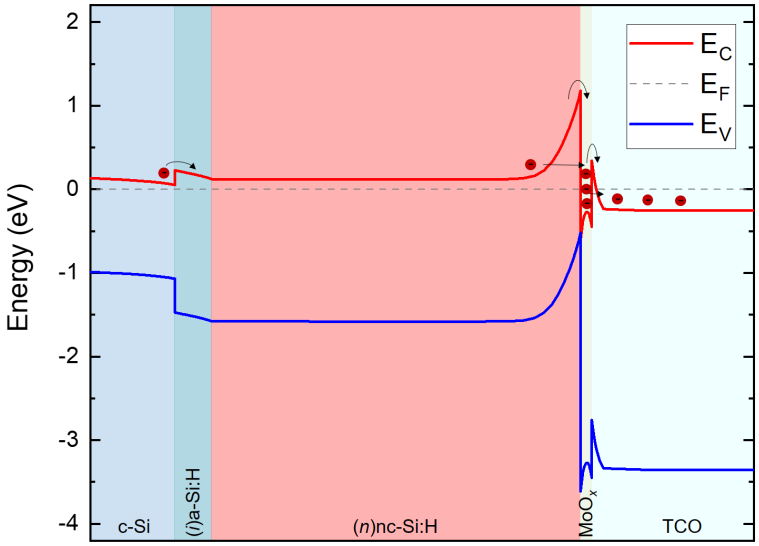


Figure 5.2: Band diagram of electron transport layer featuring (n)nc-Si:H/MoO_x contact. Conduction and valence bands are shown in red and blue, respectively. The transport of electrons (red circles) is sketched.

To achieve efficient transport in the proposed contact stack, it is important to ensure good quality of n-type layer in terms of low activation energy (E_a). Hence, (n)nc-Si:H is chosen for this contact stack instead of (n)a-Si:H as it achieves lower E_a (77 meV of (n)nc-Si:H compared to 284 meV of (n)a-Si:H as reported in [91]). This is essential for successful electron collection because lower E_a of (n)nc-Si:H induces a stronger electric field at c-Si/(i)a-Si:H interface. Such electric field enables the accumulation of electrons while repelling holes. Moreover, lower E_a decreases the barrier for electron transport across (n)nc-Si:H/MoO_x interface. Hence, lower (n)nc-Si:H E_a is crucial for this contact stack. It has to be noted that thicker (n)nc-Si:H layers with higher crystalline fraction usually exhibit lower E_a.

Moreover, the interface between (n)nc-Si:H and MoO_x can be susceptible to shunting due to the possible overlap of E_C and E_V, potentially presenting a limitation to the performance of the device. While in Figure 5.2 the overlap of E_C and E_V is visible, in manufactured devices such overlap is not expected. As the deposition of MoO_x most likely induces surface oxidation of (n)nc-Si:H, the formation of a thin SiO_x layer at (n)nc-Si:H/MoO_x interface is expected. Therefore, thin SiO_x layer could prevent the band overlap. Additionally, as discussed in Section 2.4, decrease in oxygen content of MoO_x during the reaction with the substrate decreases its WF. With lower MoO_x WF, the aforementioned overlap is less likely to happen. Therefore, two conditions can potentially prevent the formation of the overlap: formation of thin SiO_x layer and low MoO_x WF.

5.2. FBC solar cells as proof-of concept

As the IBC devices proposed in Section 5.1 feature novel contact stacks, it is important to check their passivation quality and performance before applying them to IBC devices. Therefore, FBC devices are used as proof-of-concept due to the simple fabrication process compared to IBC devices. In Figure 5.3, the proposed IBC device and corresponding proof-of-concept FBC devices are presented. Double-side textured (DST) wafers are used in this part of the project to improve light management. Additionally,

MoO_x devices manufactured by [70] and [66] are developed for DST substrate and implementing contact stacks with MoO_x on flat surface would require additional optimization.

As shown in Figure 5.3, the investigated contact stacks with MoO_x are deposited on the front side of the FBC devices as the smaller metal area poses stricter limitations on carrier collection. On the rear side of FBC cells, standard contact stacks developed within the PVMD group by [86], [23], [87], [85] are implemented.

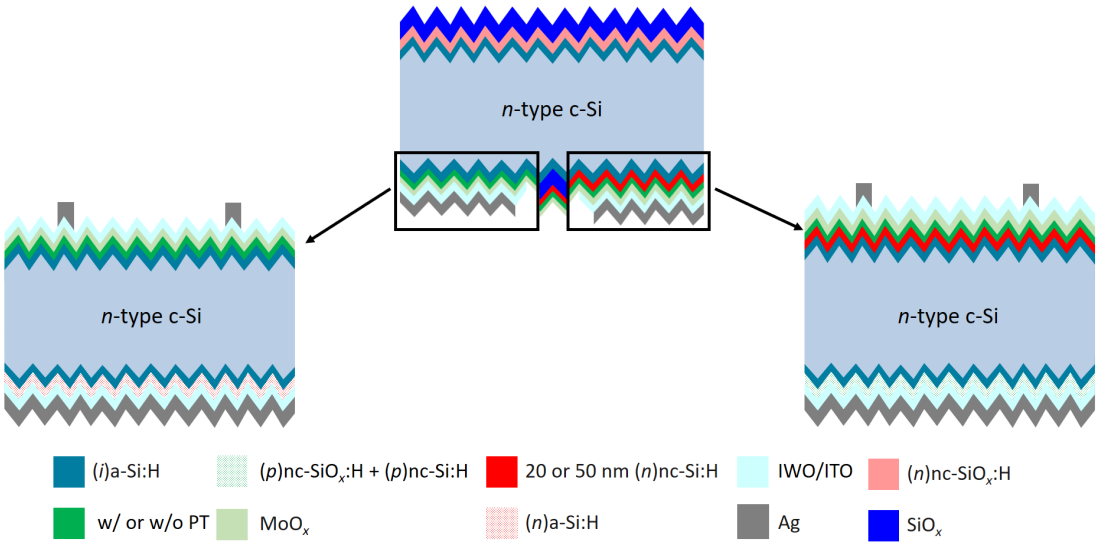


Figure 5.3: The structure of IBC-SHJ solar cell with MoO_x and corresponding FBC-SHJ solar cells.

In Figure 5.3 on the bottom left, a sketch of the manufactured FJ FBC devices is presented. On the rear side of the devices, a standard electron collection contact stack is used, while on the front side hole collection stack containing (i)a-Si:H/MoO_x/TCO/Ag is deposited. To avoid deposition of MoO_x directly on (i)a-Si:H, PT consisting of thin (i)nc-SiO_x:H + (i)nc-Si:H bilayer is introduced prior to the deposition of MoO_x to one set of devices. PT is introduced at (i)a-Si:H/MoO_x interface to pre-oxidize (i)a-Si:H surface and minimize decrease in MoO_x WF [70]. In this part of the project, FJ FBC devices with and without PT are manufactured to evaluate its effect on device performance.

On the bottom right in Figure 5.3, a sketch of the fabricated RJ FBC devices is shown. In this case, the standard hole collection stack is implemented on the rear side of the device. On the front side, electron collection takes place through a contact stack consisting of (i)a-Si:H/(n)nc-Si:H/MoO_x/TCO/Ag and additional PT is introduced in one set of devices prior to MoO_x deposition to investigate its influence on interface quality and device performance. As explained in Section 5.1, (n)nc-Si:H is chosen for this contact stack instead of (n)a-Si:H as it is characterized by better doping efficiency [57], [23] enabling larger band banding at the c-Si interface and ensuring good selectivity. Additionally, improved doping efficiency and, thus, band bending is expected by introducing thicker (n)nc-Si:H. Therefore, FBC devices with 20 nm and 50 nm (n)nc-Si:H are fabricated to assess the impact of (n)nc-Si:H thickness increase on device performance.

5.2.1. Fabrication of FBC-SHJ solar cells

The manufacturing process of FBC-SHJ solar cells starts with pre-deposition treatments as explained in Section 3.1. The silicon wafers used in this project are 4-inch Topsil n-type double-side polished FZ <100> c-Si wafers with resistivity of 1-5 Ωcm and thickness of 260-300 µm. As DST wafers are used in this part of the project, unlike for SST wafers, no preparations are necessary before texturing. Texturing in the TMAH solution is described in detail in Section 3.1.1. By immersing the wafers in the TMAH solution, random pyramids are formed on the surface of the wafer due to anisotropic and faster etching of the <100> plane compared to the <111> plane. Following the texturing, wet-chemical wafer cleaning is performed three times to achieve a contamination-free and low defect density c-Si surface before deposition.

After the pre-deposition treatments, wafers are directly loaded into a PECVD tool for deposition of intrinsic and doped Si layers. During this project, PECVD called AMIGO in EKL at the Delft University of Technology is used. The working principle of AMIGO is described in Section 3.2.1. Following the deposition of intrinsic and doped Si layers, MoO_x is deposited on the front side of the device by thermal evaporation in Provac in the EKL cleanroom. Room-temperature transparent conductive oxide (TCO) is sputtered on both the front and rear sides of the cell precursors and then annealed at 180°C for 5 minutes. During this project, both ITO and IWO are used as TCO. The sputtering tool called ZORRO in EKL has been used during this research. As a final step, metal contacts are formed during the screen printing process on both front and rear side. Detailed description of thermal evaporation, sputtering and screen printing can be found in Section 3.2.4, Section 3.2.2 and Section 3.2.3, respectively. Five identical cells with an active area of 4.05 cm^2 are manufactured per wafer. A picture of the front side of manufactured cells is presented in Figure 5.4.

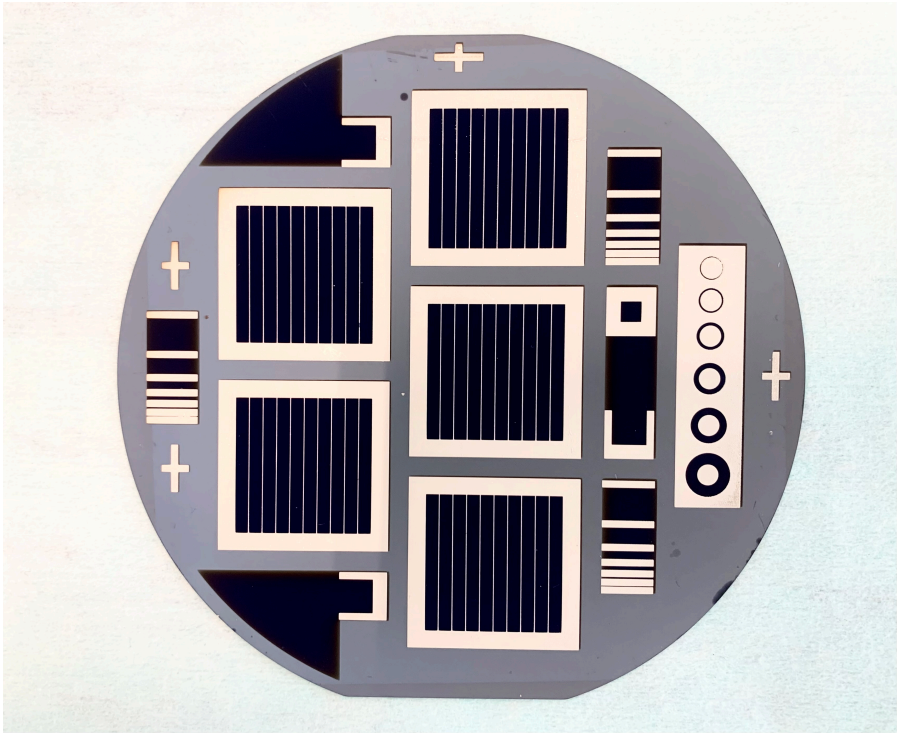


Figure 5.4: The front side of manufactured FBC-SHJ solar cells.

5.2.2. Results and analysis

In this Section, the main results of fabricated FBC solar cells are presented and discussed. Additionally, the performance of implemented contact stacks is analyzed in relation to further application in IBC solar cells. In the case of FJ FBC devices, the main point for analysis is the influence of PT on device performance, while for RJ FBC devices both the influence of PT and (n)nc-Si:H thickness are investigated. Lastly, devices with both IWO and ITO are manufactured to ensure that two TCOs can be interchanged without compromising performance.

FJ FBC solar cells

To check the performance of the hole collecting contact stack and investigate the influence of PT on device performance, FJ FBC solar cells are manufactured (Figure 5.5).

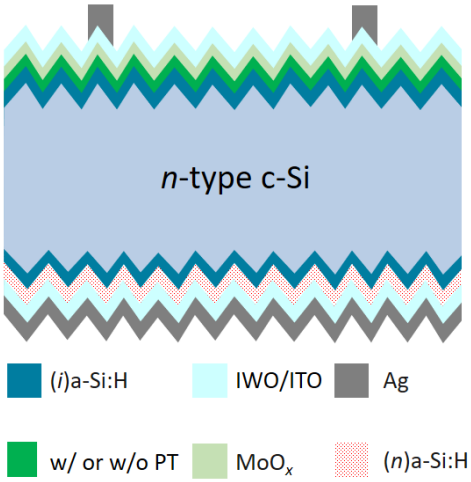


Figure 5.5: The structure of FJ FBC-SHJ solar cell.

In total, four types of FJ devices are included in the analysis in this Section. As presented in Table 5.1, PT conditions and type of TCO are varied, while MoO_x thickness is 1.7 nm in all devices.

Table 5.1: Four types of fabricated FJ FBC-SHJ solar cells.

PT conditions	**TCO**
w/ PT	IWO
w/o PT	IWO
w/ PT	ITO
w/o PT	ITO

In general, as presented in Figure 5.6, better FF and V_{OC} are observed for devices with PT. As introduced before, the interface between Si and MoO_x improves with the introduction of PT leading to better band bending at the interface and improved carrier selectivity and transport [70], [66]. Therefore, PT is an important addition for achieving high FF and V_{OC}. On the other hand, based on the results presented in Figure 5.6, no significant effect of PT on J_{SC} can be observed.

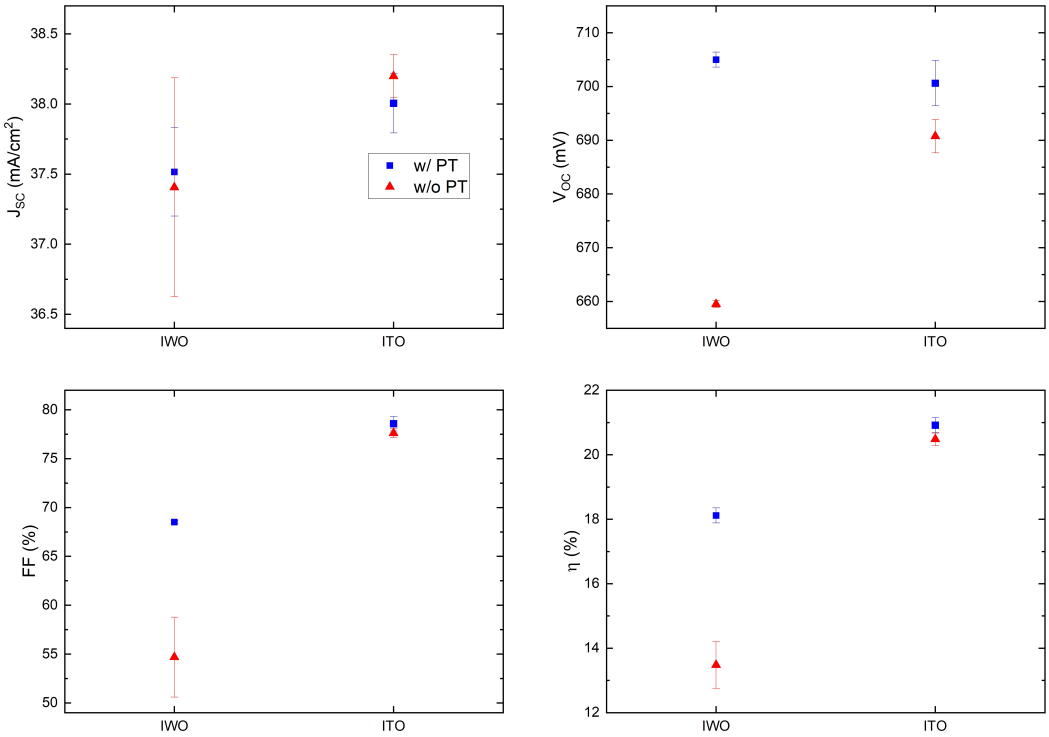


Figure 5.6: External parameters of double-side textured FJ FBC-SHJ solar cells with MoO_x as a function of selected TCO.

Figure 5.6 shows a significant drop in FF and J_{SC} when implementing IWO instead of ITO. This decrease can be related to the issues of the screen printing process during the fabrication of devices with IWO rather than the properties of two TCO. As shown in Figure 5.7, metal fingers of the devices shown on the left show more deformations compared to the devices on the right, which leads to higher series resistance and a decrease in FF. Moreover, poor metalization influences carrier collection and limits J_{SC} and V_{OC}. This can be observed from EQE and 1-R curves presented in Figure 5.8. In the range from approximately 500 nm to 1000 nm, the representative EQE curve of devices with IWO is lower compared to the curve of ITO devices indicating losses in carrier collection. Hence, despite lower reflectance of IWO in this part of the spectrum, higher J_{SC} is achieved with ITO devices.

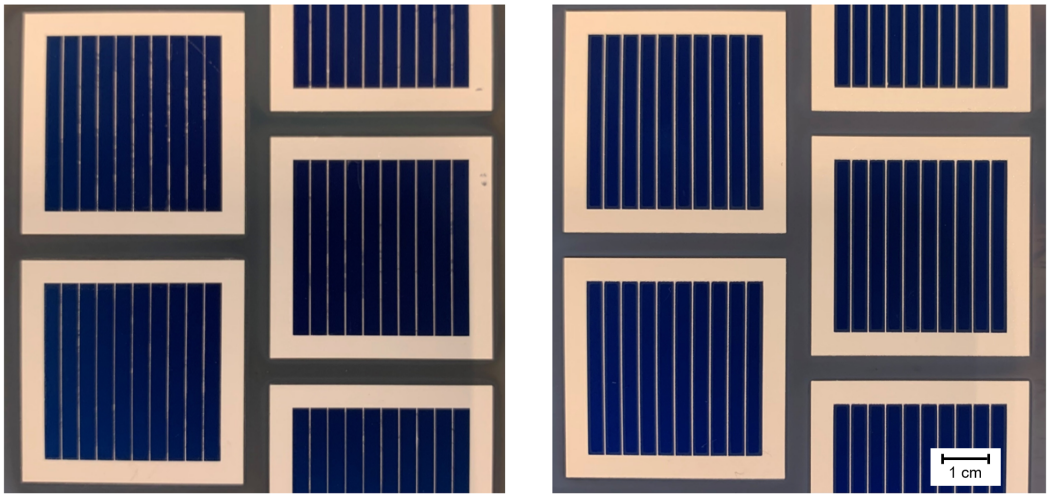


Figure 5.7: Devices with poorly printed metal fingers (left) and devices with successful screen printing.

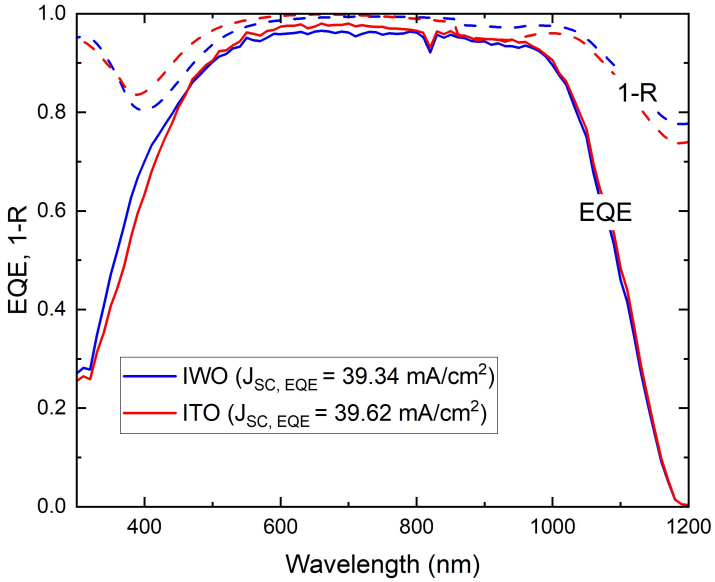


Figure 5.8: External quantum efficiency (EQE) and 1-R curves of FJ solar cells with PT. $J_{SC,\ EQE}$ values are indicated in the legend.

Table 5.2 summarizes the results of the best performing FJ FBC-SHJ devices manufactured in this part of the project. The performance of devices with IWO is significantly influenced by poor metalization, fabricated devices with IWO show FF close to and above 60% and V_{OC} above 650 mV. Devices with ITO perform notably better, especially in terms of FF with values above 78% for devices with and without PT. V_{OC} values over 695 mV are also observed. The results presented in this Section show that the developed hole collection contact stacks are working and performing well, therefore they are expected to be successfully implemented in IBC devices. From Table 5.2 the importance of PT can be observed. Hence, PT is included during the fabrication of IBC-SHJ solar cells.

Table 5.2: The results of best proof-of-concept FJ FBC-SHJ solar cells with MoOx.

PT conditions	**TCO**	**J_{SC} (mA/cm^2)**	**V_{OC} (mV)**	**FF (%)**	**η (%)**
w/ PT	IWO	37.74	706	68.62	18.28
w/o PT	IWO	36.85	659	57.58	13.99
w/ PT	ITO	38.01	704	79.29	21.21
w/o PT	ITO	38.21	695	78.16	20.77

RJ FBC solar cells

RJ FBC solar cells are fabricated to check the performance of the electron collection contact stack involving (n)nc-Si:H and 1.7 nm MoO_x (Figure 5.9).

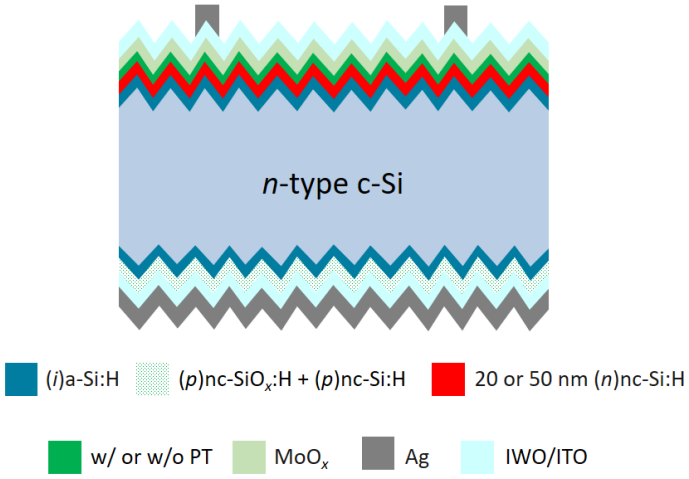


Figure 5.9: The structure of RJ FBC-SHJ solar cell.

To investigate the influence of the thickness of (n)nc-Si:H and PT, six sets of devices are manufactured and analyzed as presented in Table 5.3.

Table 5.3: Six types of fabricated RJ FBC-SHJ solar cells.

(n)nc-Si:H thickness (nm)	**PT conditions**	**TCO**
20	w/ PT	IWO
20	w/o PT	IWO
50	w/ PT	IWO
50	w/o PT	IWO
50	w/ PT	ITO
50	w/o PT	ITO

As presented in Figure 5.10, high FF values can be achieved with the proposed contact stack, reaching over 82% for devices with 50 nm (n)nc-Si:H without PT. Thicker (n)nc-Si:H layer yields higher FF, which can be assigned to higher crystalline fraction in the material and, consequently, improved doping efficiency and σ_{dark}. This leads to better band bending and more efficient carrier selectivity. It can also be observed that PT has a negative influence on FF in RJ devices with 50 nm (n)nc-Si:H. The explanation for this can be related to the role of PT when introduced prior to MoO_x deposition. By depositing MoO_x directly on (i)a-Si:H or (n)nc-Si:H, the substrate surface is oxidized and oxygen content in MoO_x decreases leading to a decrease in WF of MoO_x. In the case of layer stack implemented in FJ devices, higher WF induces a larger field effect and improves band bending at the surface of c-Si. However, as described in Section 5.1, lower WF of MoO_x is more favorable for n-type contact implemented in RJ devices. Hence, as PT enables preservation of high WF of MoO_x, it leads to a decrease in performance of RJ devices.

On the contrary, in the case of 20 nm (n)nc-Si:H, a positive influence of PT on FF is observed. As these devices were manufactured in one run only, the cause of this effect cannot be explained with certainty. Similar trends of FF and pFF indicate that this difference cannot be assigned to metalization process. Hence, more exploration is necessary to understand if the impact of PT on device performance of thin (n)nc-Si:H is related to processing fluctuations of PECVD process.

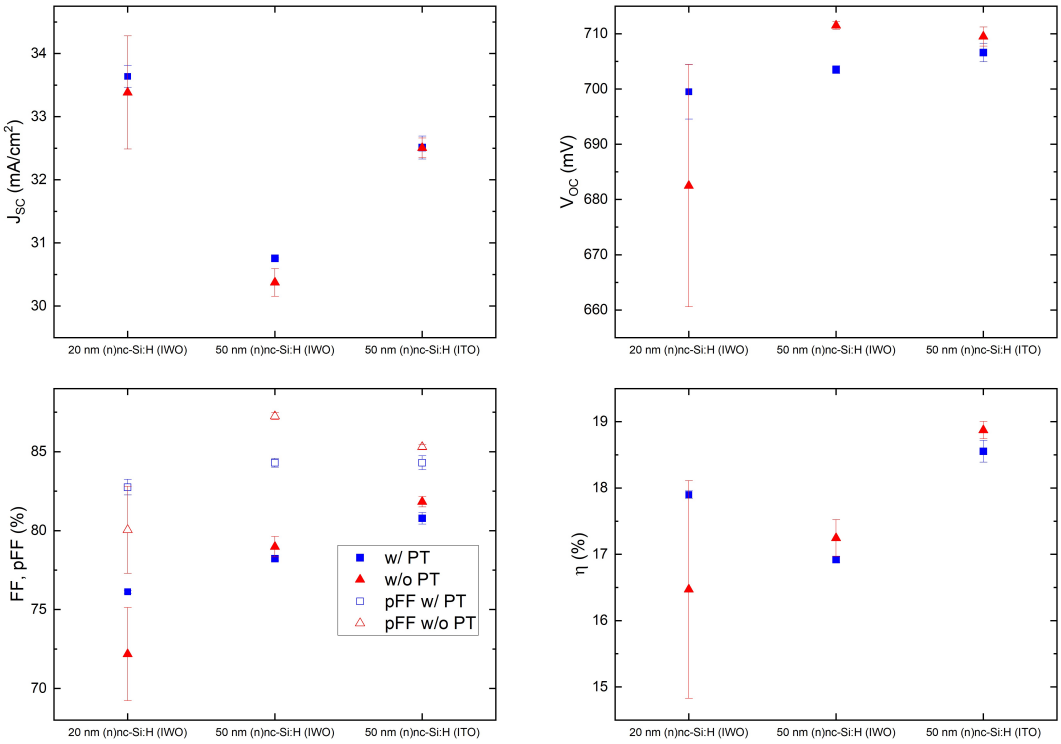


Figure 5.10: External parameters of double-side textured RJ FBC-SHJ solar cells with MoO_x as a function of (n)nc-Si:H thickness and selected TCO.

Similar trends can be observed with values of V_{OC} to that of FF. PT has a positive influence on the performance of devices with 20 nm (n)nc-Si:H and a negative effect on the performance of the devices with 50 nm (n)nc-Si:H. This can be assigned to the same reasons as described above for the FF. Additionally, devices with 50 nm (n)nc-Si:H show better V_{OC} which can be ascribed to better doping efficiency leading to the improved field effect.

Lastly, due to the large thickness of (n)nc-Si:H, all manufactured devices exhibit low J_{SC}. This is confirmed by the representative EQE and 1-R curves shown in Figure 5.11. It can be observed that EQE curve shows values close to 0 up to 400 nm and, when compared to the 1-R curve, large losses due to parasitic absorption in the region up to 400 nm can be noticed. However, as the aim of developing this contact stack is the application on the rear side of the IBC devices, this limitation is not crucial for further steps of the project.

Similar to the results of FJ devices, devices with ITO show better performance compared to the devices with IWO. As previously mentioned, the difference in the performance can be related to poor screen printing conditions causing an increase in series resistance rather than the impact of IWO. This can be observed from the difference between pFF and FF, as presented in Figure 5.10 and confirmed by calculated $R_{s,\ SunsVoc}$. In Table 5.4, the values of pFF and corresponding $R_{s,\ SunsVoc}$ are presented showing that better-performing devices in terms of V_{OC}, FF and η suffer less from resistive losses. Additionally, by comparing EQE curves from Figure 5.11, it can be observed that a large fraction of absorbed light in the range between 400 and 1100 nm is lost due to inefficient charge collection in devices with IWO. This can be ascribed to less resistive contact of ITO and p-type Si on the rear due to higher WF of ITO compared to IWO [99]. In Figure 5.11 shown in red, collection losses of ITO cell are lower leading to better overall device performance.

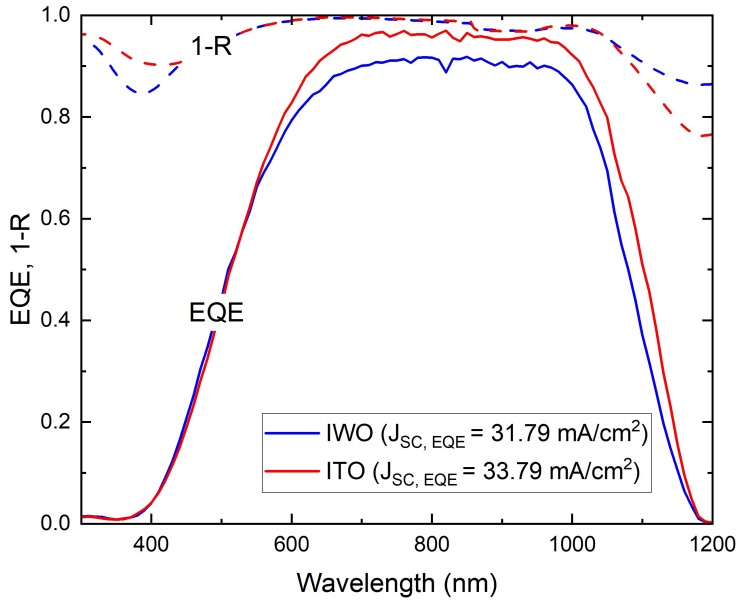


Figure 5.11: External quantum efficiency (EQE) and 1-R curves of RJ solar cells with 50 nm (n)nc-Si:H and without PT. $J_{SC,\ EQE}$ values are indicated in the legend.

The best RJ FBC-SHJ devices fabricated in this part of the project are presented in Table 5.4. All devices show V_{OC} above 700 mV and FF above 74%, making them suitable for further application in IBC-SHJ devices. As mentioned above, devices featuring 50 nm (n)nc-Si:H show better performance in terms of V_{OC} and FF compared to the devices with thinner n layer, thus, IBC devices are manufactured with 50 nm (n)nc-Si:H. The beneficial effect of PT for forming the hole contact stack outweighs its minor negative effects when applied in the electron contact stack. Moreover, including a unique treatment is necessary for simplifying the manufacturing process. Hence, PT is included in IBC devices as a blanket layer prior to the deposition of MoO_x.

Table 5.4: The results of best proof-of-concept RJ FBC-SHJ solar cells with MoOx.

***n*-type contact**	**TCO**	**J_{SC} (mA/cm²)**	**V_{OC} (mV)**	**FF (%)**	**η (%)**	**pFF (%)**	**$R_{s,\ SunsVoc}$ (Ωcm²)**
20 nm (n)nc-Si:H w/ PT	IWO	33.51	703	76.19	17.94	83.1	1.70
20 nm (n)nc-Si:H w/o PT	IWO	34.01	704	74.26	17.63	82.0	1.92
50 nm (n)nc-Si:H w/PT	IWO	30.75	704	78.29	16.95	84.5	1.63
50 nm (n)nc-Si:H w/o PT	IWO	30.22	712	79.44	17.44	87.1	1.95
50 nm (n)nc-Si:H w/ PT	ITO	32.70	708	81.26	18.81	84.8	0.86
50 nm (n)nc-Si:H w/o PT	ITO	32.64	715	82.24	19.18	85.4	0.79

5.3. Fabrication of IBC-SHJ solar cells with MoO_x

The IBC-SHJ with MoO_x devices are manufactured based on the adapted approach presented in Section 4.2 with an additional step for deposition of MoO_x. The steps involved in the process are presented in Figure 5.12.

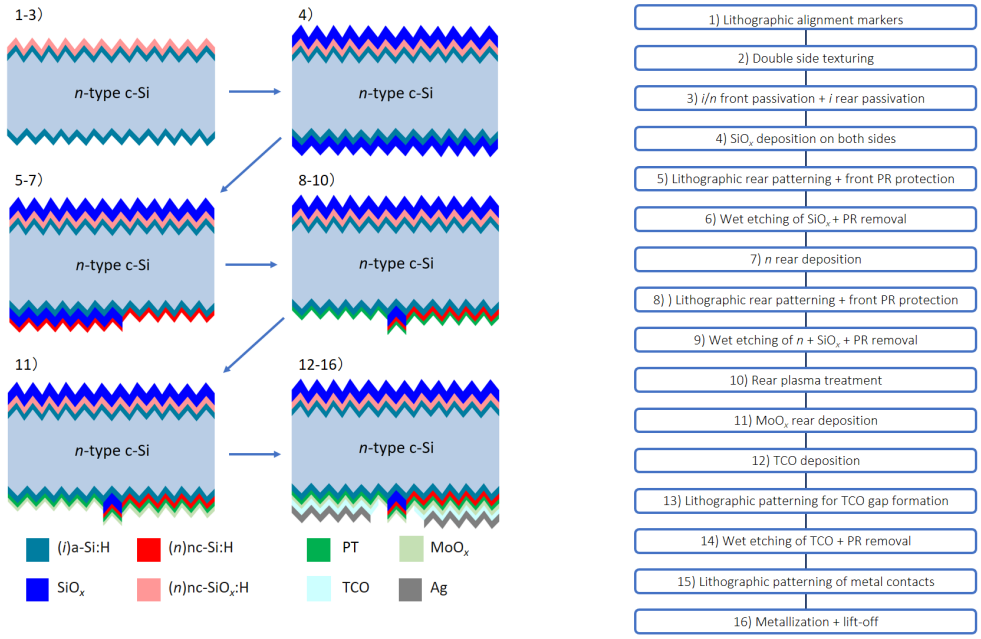


Figure 5.12: Flowchart of IBC-SHJ solar cell with MoO_x manufacturing process.

The DST FZ <100> n-type c-Si wafers are used as a substrate for the manufacturing of IBC-SHJ devices with MoO_x to improve light management compared to SST wafers. Texturing is performed by etching polished wafers in TMAH solution to form random pyramids on the c-Si surface as described in Section 3.1.1. Following the texturing, NAOC standard cleaning procedure is performed three times [39] and, directly after the last Marangoni step, the wafers are loaded in AMIGO for the deposition of (i)a-Si:H and (n)nc-SiO_x:H on the front side and the deposition of (i)a-Si:H on the rear side. PECVD in Kavli Nanolab is used for deposition of SiO_x that is used once again as both ARC at the front side of the device and as a sacrificial layer during etching steps at the rear side. To open the BSF region before the deposition of (n)nc-Si:H, the rear side of the wafers is patterned using photolithography. SiO_x is etched from the BSF area with buffered hydrofluoric acid (BHF) 1:7 solution, while the emitter area and the entire front surface were protected with photoresist. Unlike in the flowchart from Section 4.2, removal of SiO_x is performed in BHF 1:7 solution instead of 0.55% HF to accelerate the etching process. To observe the selectivity of BHF 1:7 etching towards Si and check the effects on τ_{eff}, etching test were conducted and no negative impact were discovered.

Following the opening of the BSF region, the photoresist is removed with acetone, and a 0.55% HF dip is used to remove the native oxide from the rear side of the wafers. The wafers are directly loaded in AMIGO and (n)nc-Si:H is deposited on the full rear area. To open the emitter region, the second photolithography step is included for patterning the rear side of the wafers. (n)nc-Si:H is etched in 1% KOH solution followed by etching of SiO_x in BHF 1:7 solution while keeping the BSF region and the front side of the wafers covered by photoresist. Following another native oxide removal in 0.55% HF, the wafers are loaded in AMIGO for full rear area PT. Directly after PT, the wafers are loaded in Provac for thermal evaporation of MoO_x and, immediately after the evaporation of MoO_x, the wafers are loaded to ZORRO for TCO deposition. As MoO_x is sensitive to air as mentioned in Section 2.4, it is crucial to minimize the time between breaking the vacuum of the evaporation chamber and loading the wafers to vacuum in ZORRO. As TCO deposition causes damage to passivation, TCO annealing is done following TCO deposition. Following the annealing step, the third photolithography step is used for TCO gap formation aiming to prevent shunting at the contact of BSF and emitter region. TCO is removed in the gap by etching in 37% HCl solution. Lastly, the fourth photolithography step is performed before Ag thermal evaporation. Ag is used as a replacement for Al (deposited by electron beam evaporation), as it shows good adhesion to the textured surface and thermal evaporation is not expected to damage passivation quality. Following the Ag evaporation, the wafers are dipped in an acetone solution in an ultrasonic bath for Ag lift-off.

5.3.1. Process challenges

Similar to the flowcharts presented in Chapter 4, the main process challenges during the fabrication of IBC devices with MoO_x are related to etching steps presented in Figure 5.12 as steps 6 and 9. In the case of SST wafers used in the previous flowcharts, all patterning steps are performed on the flat side of the device. However, processing on the textured surface impacts both etching uniformity and rate. Thus, etching tests were performed to determine the etching uniformity, the most suitable concentrations of etching solutions, as well as etching rates.

Etching of SiO_x

The first challenge was observed during the etching of SiO_x with 0.55% HF as the etching on the textured surface was found to be slower compared to etching on the flat surface. Thus, BHF solution is introduced for the etching of SiO_x. In this research BHF 1:7 solution is used, consisting of HF and NH_4F in ratio 12.5:87.5%, where NH_4F serves as a buffering agent. Based on the τ_{eff} measurements, it was observed that etching in the BHF 1:7 solution does not additionally decrease passivation quality compared to etching in 0.55% HF and, therefore, the BHF 1:7 solution is used further in this project. However, as demonstrated in Figure 5.13, the etching of SiO_x on a textured surface shows nonuniformities. This is likely due to layer thickness difference at peaks and valleys of the pyramids, leading to incomplete etching of SiO_x across the wafer. Hence, increasing etching time was necessary to fully remove SiO_x.

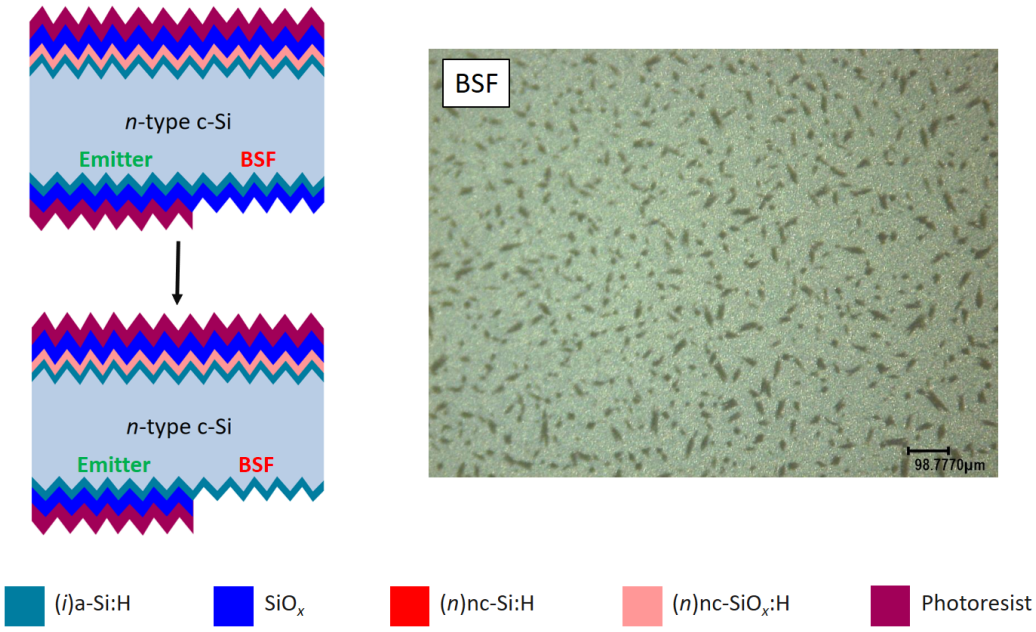


Figure 5.13: A sketch of the etching step (left) and optical microscope image (right) of a sample showing nonuniform etching of SiO_x in BHF 1:7 solution in step 6. Darker areas represent SiO_x, while lighter areas are underlying (*i*)a-Si:H.

Incomplete etching of SiO_x was also visible at the edges of BSF and emitter regions after SiO_x etching in both step 6 and step 9, respectively. In Figure 5.14, an optical microscope image of SiO_x residue is shown. To increase the etching rate and ensure SiO_x is fully removed at the edges, wafers are dipped in Triton X-100/DI water solution prior to etching in BHF 1:7. The role of Triton X-100 is to decrease surface tension and, thus, increase the wettability of SiO_x leading to complete and faster removal of SiO_x [100]. After performing etching tests with Triton X-100/DI water dip of 1 minute followed by etching in BHF 1:7, the etching rate necessary for complete removal of SiO_x is determined to be around 250 nm/min and a time of around 6.5 minutes is necessary to complete etching of 1.6 µm SiO_x layer.

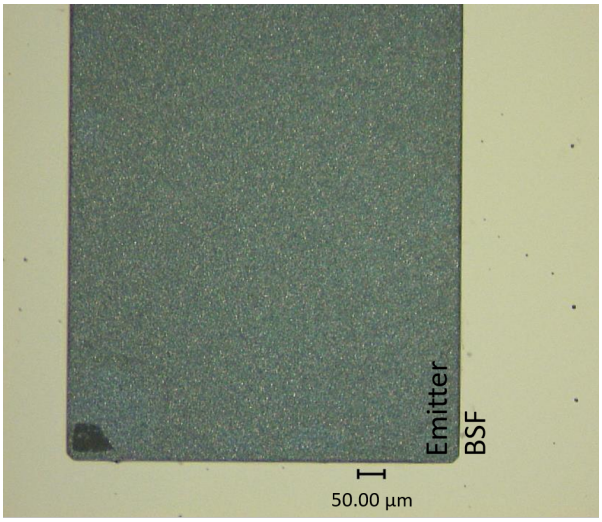


Figure 5.14: Optical microscope image of a sample showing SiO_x residue after etching in BHF 1:7 solution in step 9. The darkest area in the bottom left corner represents SiO_x.

Etching of (*n*)nc-Si:H

For removal of (n)nc-Si:H in step 9, room-temperature 1% KOH solution is used [92]. It was observed that the etching rate on textured surface decreases compared to the flat surface. However, the thickness of (n)nc-Si:H layers used in this project is up to 50 nm and the decrease in the etching rate is not expected to significantly impact the total etching time. As layer thickness on the textured surface cannot be measured with spectroscopic ellipsometry, the etching rate is estimated as being 1.7 times slower compared to the flat surface, just as the deposition rate decreases 1.7 times going from flat to textured substrate. As the estimated etching rate for flat surface accounts for overetch in order to fully remove the layer from the whole area, the calculated etching rate for textured surface is expected to be sufficient. Following etching, samples are investigated under an optical microscope to ensure no residues of (n)nc-Si:H are left. The etching rate is determined to be 6 nm/min.

Isotropic etching of SiO_x and damage to (*i*)a-Si:H

As discussed above, Triton X-100 is used prior to SiO_x etching in BHF to increase wettability of SiO_x. However, the use of Triton X-100 increases the etching rate in the lateral direction causing underetching and widening of etched structures in step 6. In Figure 5.15 on the left, the result of opening BSF region of the devices with the smallest pitch is shown. The width of BSF is represented with measurement 2, showing that the width of this region reaches 139 µm instead of 106 µm as defined by the mask and shown in Table 4.2. A similar issue is observed in Figure 5.15 on the right, where the width of the opened BSF region (measurement 2) is measured to be around 502 µm instead of 466 µm as defined by the mask. As total thickness of SiO_x is 1.6 µm, underetch of 15 µm on each side is not realistic within 6.5 minutes that is expected to etch 1.6 µm. However, BHF can stay trapped in the region covered by photoresist during the first few minutes of rinsing leading to prolonged etching time of regions covered by photoresist. This can potentially be mitigated by including a rinsing step with Triton X-100 prior to rinsing in DI water. Nevertheless, more investigation is required to understand the cause of the large underetch described in this Section.

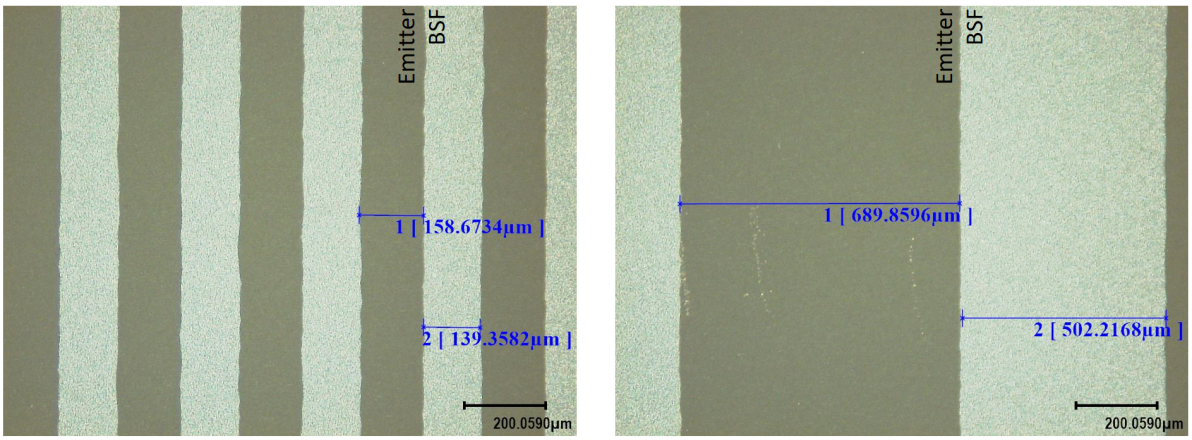


Figure 5.15: Optical microscope image of samples showing a result of isotropic of SiO_x after etching in BHF 1:7 solution in step 6. On the left, a device with the smallest pitch is shown (cell type A). On the right, a device with the largest pitch is shown (cell type C).

The isotropic etching and widening of BSF in step 6 causes additional issues during etching in step 9. Figure 5.16 depicts flowchart steps 5 to 9 in detail, showing the consequence of the isotropic etching of SiO_x in step 6. During the etching of SiO_x, a wider area is opened compared to the area of the designed mask and (n)nc-Si:H is deposited directly on (i)a-Si:H outside the designated BSF region. During the next patterning step, the photoresist covers only the originally designed BSF region, leaving a part of (i)a-Si:H/(n)nc-Si:H stack open as it falls in the emitter region. Thus, a part of (i)a-Si:H underlying (n)nc-Si:H in the open region is (partially) removed during etching of (n)nc-Si:H as KOH solution used for (n)nc-Si:H shows no selectivity to (i)a-Si:H. This leads to passivation damage and increased recombination rate at the gap, potentially causes epitaxial growth of PT and, ultimately, poses a limitation on V_{OC} and FF. Moreover, the gap that is included in the flowchart in Figure 5.12 from step 9 in order to isolate BSF and emitter region is not present in fabricated devices, which can lead to a decrease in shunt resistance.

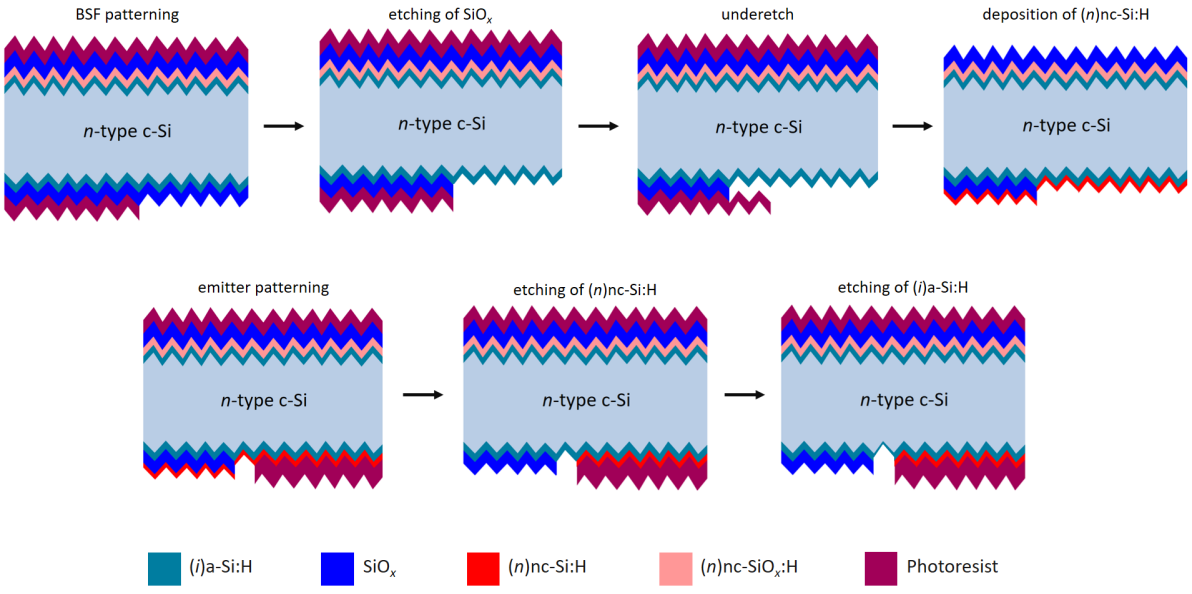


Figure 5.16: Sketch of processing steps including the underetch of SiO_x caused by isotropic etching and the influence of the underetch on further processing. The steps shown in this sketch correspond to steps 5 to 9 of the flowchart.

An extensive set of etching tests or optimization of the flowchart for the use of alternative patterning techniques can be conducted to overcome the issue caused by isotropic etching of SiO_x. Nevertheless,

due to the limited time available for the completion of this project, the devices are manufactured without further optimization and results are analyzed while keeping this limitation in mind.

5.3.2. Results and analysis

As discussed in Section 4.2.2, in the course of this project IBC cells with three different geometries are fabricated, with the main differences being the width of the emitter, BSF and pitch, and metal coverage. Devices with the largest pitch are also characterized by the largest metal coverage, as shown in detail in Figure 4.5 and Table 4.2. In this Section, the results of fabricated devices are presented as a function of pitch size in order to analyze the effect of cell geometry on device performance.

Figure 5.17 represents a summary of external parameters of fabricated IBC solar cells with MoO_x. Similarly to results discussed in Section 4.2.2, devices with MoO_x with larger pitch show better performance. The possible reason for this can be a decrease in the ratio between emitter and BSF edges compared to the total device area and thus a decrease in corresponding defects. Moreover, the increased metal coverage in these devices leads to lower series resistance as discussed in detail in Section 4.2.2. The best device manufactured during this process shows FF of 67.9%, V_{OC} of 542 mV, J_{SC} of 35.03 mA/cm^2 and final efficiency of 12.9%.

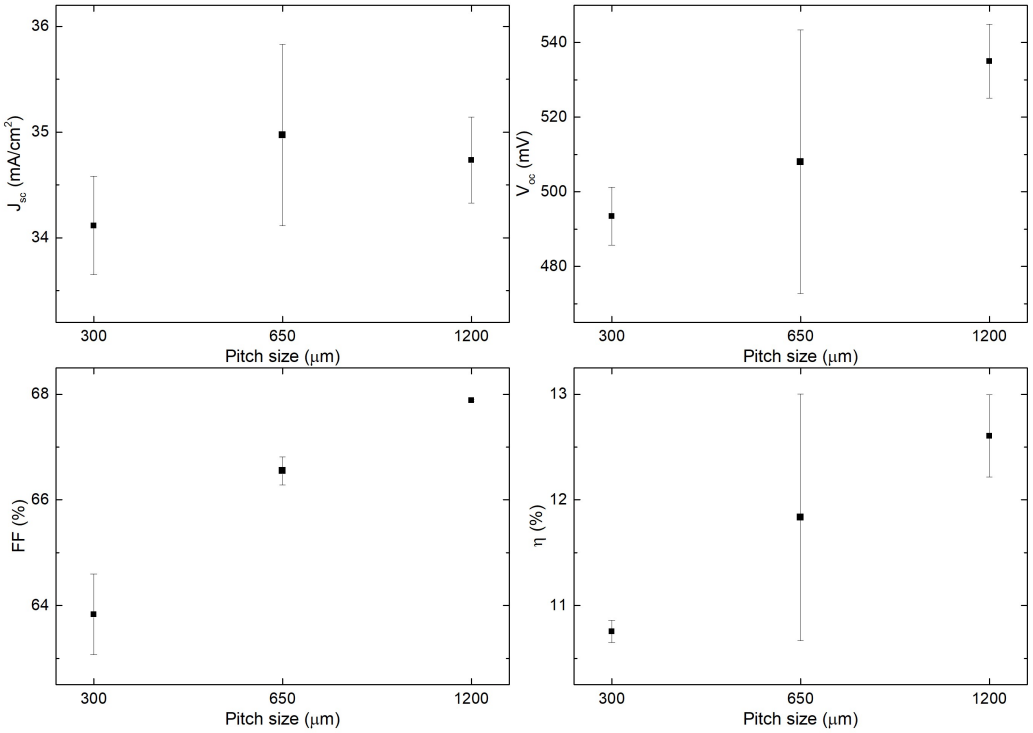


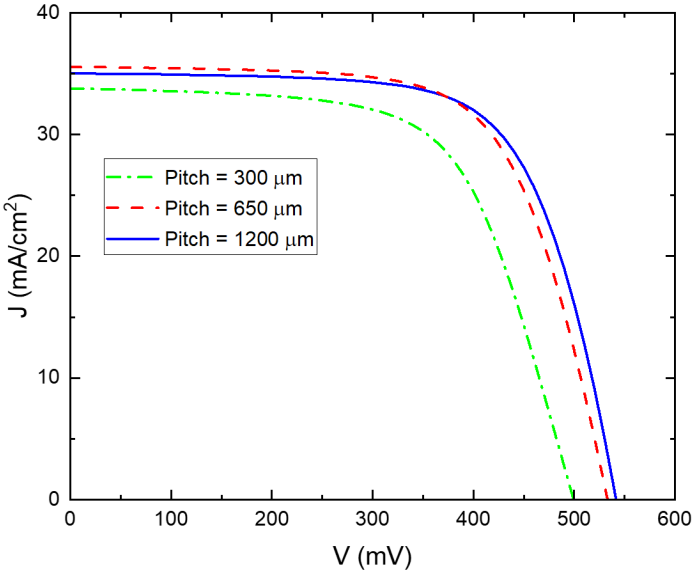
Figure 5.17: External parameters of double-side textured IBC-SHJ solar cells with MoO_x related to different pitch sizes.

J_{SC} values of the manufactured devices are in the range between 33 and 36 mA/cm^2, showing a slight improvement compared to tunneling devices presented in Chapter 4. The reason for this improvement can be assigned to the use of DST wafers instead of SST wafers leading to better light management. However, as the front side ARC is not optimized, the improvement is not significant. Moreover, generally poor performance of the devices, as reflected in low V_{OC}, can potentially be limiting to J_{SC}.

The main shortcoming of fabricated devices is low V_{OC}, reaching just above 540 mV for the best performing device. The possible reason for low V_{OC} can be related to insufficient field effect and, thus, band bending at c-Si/(*i*)a-Si:H interface in the emitter region leading to poor hole collection. To confirm this assumption, the field effect can be enhanced by increasing the thickness of MoO_x which is investigated further in this project and discussed in Section 5.4. Low V_{OC} can also be related to isotropic etching of SiO_x and consequent damage to (*i*)a-Si:H. As mentioned in Section 5.3.1, the regions

where (i)a-Si:H is damaged are characterized by high recombination rate leading to a decrease in V_{OC}. As (i)a-Si:H is (partially) removed, highly H-diluted PT is deposited directly on c-Si which may lead to epitaxial growth of PT and have detrimental effect on device performance.

Lastly, FF in the range between 63% and 68% is observed, showing an improvement compared to tunneling IBC devices from Chapter 4. Moreover, from J-V curves shown in Figure 5.18, it can be observed that no shunting occurs in the devices with MoO_x, indicating that by substituting (p)nc-SiO_x:H + (p)nc-Si:H bilayer with less laterally conductive MoO_x, internal shunting can be resolved. To further optimize FF, the effect of PT can be investigated. Namely, the purpose of PT is achieving good interface between (i)a-Si:H and MoO_x by ensuring (i)a-Si:H is oxidized prior to MoO_x deposition and MoO_x WF decay is avoided. However, the surface of (i)a-Si:H is oxidized during the deposition of SiO_x, potentially allowing for direct deposition of MoO_x without the need of pre-oxidation. Moreover, by excluding PT, the process can be further simplified and the performance of electron collecting contact could be enhanced as shown in Section 5.2.



Pitch (µm)	J_{SC} (mA/cm²)	V_{OC} (mV)	FF (%)	η (%)
300	33.78	499	63.29	10.68
650	35.58	533	66.73	12.66
1200	35.03	542	67.90	12.88

Figure 5.18: J-V curves and external parameters of best double-side textured IBC-SHJ solar cells with MoO_x with different pitch sizes.

In Figure 5.19, SEM cross-section of the election collection stack of the fabricated IBC device is presented. In the images, Ag grains can be clearly recognized as well as IWO layer. Moreover, approximate position (n)nc-Si:H is observed. The structures that can be distinguished in (n)nc-Si:H and extend to the IWO layer potentially indicate the crystalline growth of (n)nc-Si:H. A large crystalline fraction of (n)nc-Si:H suggests that efficient electron collection can take place. Due to the low thickness of (i)a-Si:H, PT and MoO_x, these components could not be recognized in SEM images.

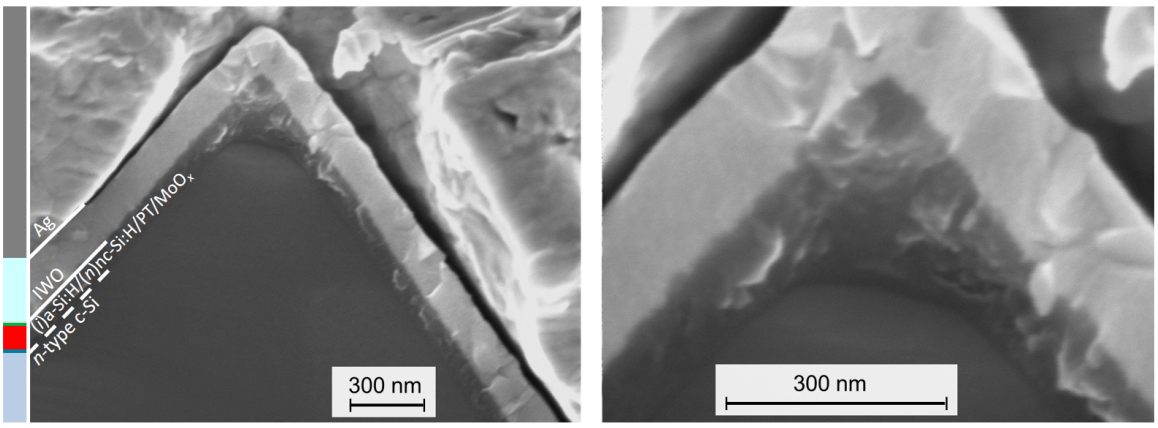


Figure 5.19: SEM cross-section of election collection stack. Images show the same contact stack with lower (left) and higher (right) magnification.

5.3.3. Conclusions and outlook on the IBC-SHJ architecture with MoO_x

Novel IBC-SHJ solar cells featuring MoO_x have been developed and manufactured reaching an efficiency of 12.9%. The novel architecture successfully combines the simplicity of the tunneling IBC manufacturing process with low lateral conductivity MoO_x aiming to increase shunt resistance between electron and hole collecting regions. However, manufactured IBC devices are characterized by moderate performance strongly limited by high recombination rate causing low V_{OC} as well as J_{SC} and FF. To overcome this constraint, the influence of MoO_x thickness on device performance will be evaluated, assuming that thicker MoO_x enables better field effect and more effective hole collection leading to higher V_{OC}. Additionally, the effect of PT on FF and general device performance will be investigated to understand the necessity of this step in the proposed IBC device structure. In the following Section, the main results of two optimization proposals are presented and discussed.

5.4. Optimization of contact stacks of IBC-SHJ solar cells with MoO_x

As discussed in the previous Section, significant limitations in the performance of the first set of fabricated IBC-SHJ devices with MoO_x are observed. To tackle this, two sets of experiments are conducted to get a better insight into the limitations of the fabricated devices. Firstly, to investigate the impact of field effect on V_{OC} and hole collection, devices with varying MoO_x thickness are prepared and the influence of thickness variation on external parameters of solar cells is analyzed. Secondly, the effect of PT is evaluated by manufacturing devices with varying thickness of MoO_x without PT. The aim of the second set of tests is to assess the necessity of PT in IBC devices as the surface of (i)a-Si:H is oxidized during SiO_x deposition. By excluding PT, the fabrication process can be simplified, while potentially allowing for better electron collection and simultaneously achieving a good interface between (i)a-Si:H and MoO_x.

5.4.1. MoO_x thickness series with PT

Based on the previous experiments from PVMD group, FBC devices with HTL consisting of 1.7 nm MoO_x and interfacial PT show the best performance due to the transparency of thin MoO_x with high WF preserved by the introduction of PT [70]. However, layer transparency does not have a detrimental impact on device performance when implemented on the rear side and a larger thickness of MoO_x allows for higher WF, which is beneficial for hole collection. Hence, in this Section, the effect of MoO_x thickness on IBC-SHJ solar cell performance is investigated.

In Figure 5.20, external parameters of manufactured devices are presented. MoO_x thickness is varied in the range from 1.7 nm to 7 nm, while other layer properties and fabrication parameters are kept the same as in devices presented in Section 5.3.2. As devices manufactured during this experiment show the same trend of improved performance with increased pitch size, all devices presented in Figure 5.20 are with 1200 µm pitch and analysis is this Section will focus on these devices. Details about fabricated devices with smaller pitch are presented in Appendix A. As only one set of experiments was conducted

during this project, generally poor performance of the devices can potentially be assigned to flaws related to the manufacturing process such as long downtime of the tools and waiting time between processing steps. Hence, only general trends will be addressed in this Section, and for the complete study and better understanding of the impact of MoO_x thickness additional investigation is essential.

In general, devices with 3 nm MoO_x show the best results overall followed by a decrease in performance with further thickness increase. Poor performance of devices with 1.7 nm MoO_x, which are comparable to the ones presented in Section 5.3, is assigned to manufacturing problems and cannot be related to general trends presented in this Section. Therefore, devices with 1.7 nm MoO_x will not be further addressed in the analysis. Nevertheless, it cannot be excluded that 1.7 nm MoO_x thickness might be the optimal one.

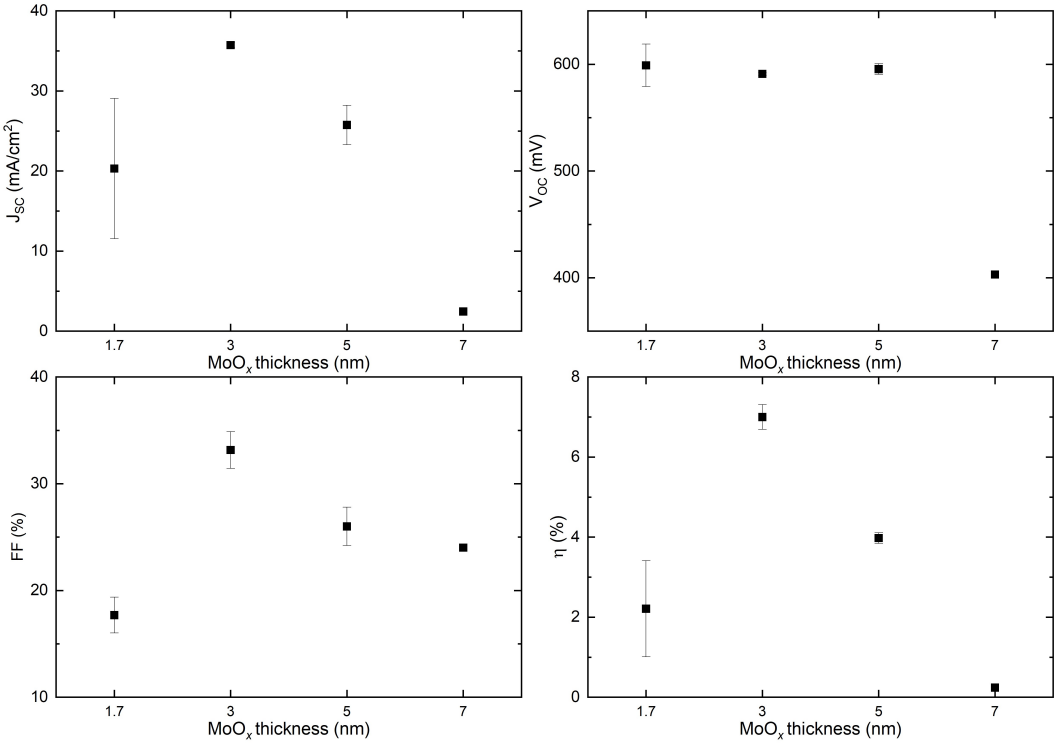
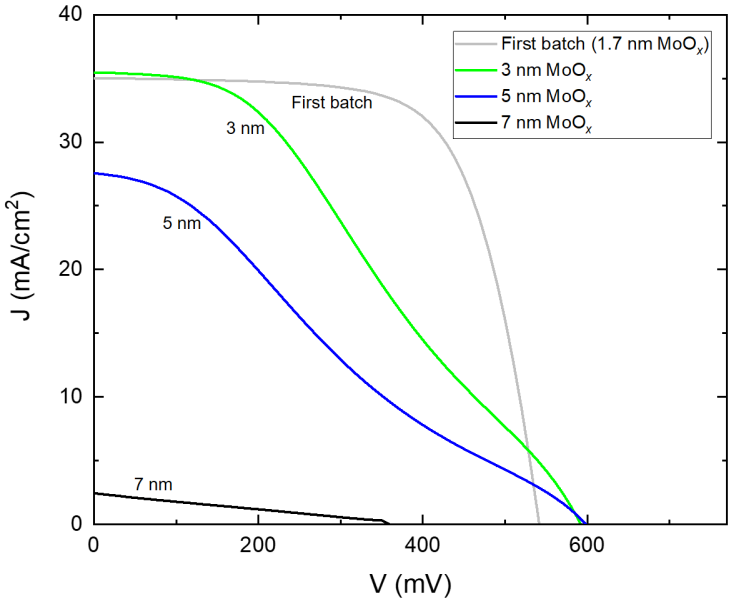


Figure 5.20: External parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x.

The best values of J_{SC} are comparable to the values achieved with the first set of devices. However, a drop in J_{SC} is observed with the increase in thickness of MoO_x indicating poor electron collection. This is potentially related to an increase in WF of MoO_x with the increase in thickness, which can have a negative effect on electron collection as discussed in Section 5.1. Improved V_{OC} for 3 nm and 5 nm can likely be coupled to improved field effect at c-Si/(*i*)a-Si:H interface in emitter. The sharp decrease of V_{OC} of 7 nm MoO_x devices is likely related to increasing dipole moment formed at the interface between MoO_x and (*i*)a-Si:H causing insufficient band bending and poor selectivity for holes, as described by [70] and [101]. However, due to poor FF and s-shaped J-V curves shown in Figure 5.21, more study is necessary to obtain realistic values of V_{OC} and analyse the impact of induced field effect.

While J_{SC} is comparable to previously fabricated devices and V_{OC} values show an improvement, very low FF is achieved. As shown in Figure 5.21, all manufactured devices are characterized by s-shaped J-V curves. In [65], [68], [102] and [103], s-shaped J-V curves of devices with MoO_x are also observed and [68] mainly ascribe the formation of s-shaped J-V curve to poor band alignment at c-Si/(*i*)a-Si:H/MoO_x interface and consequent poor hole collection. From Figure 5.21, it is also observed that thicker MoO_x leads to lower FF, which is also in agreement with the effect of increasing dipole moment explained above.



MoO_x (nm)	J_{SC} (mA/cm²)	V_{OC} (mV)	FF (%)	η (%)
First batch	35.03	542	67.90	12.88
3	35.47	592	34.37	7.22
5	27.50	599	24.73	4.07
7	2.45	403	24.01	0.24

Figure 5.21: J-V curves and external parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x.

However, s-shaped J-V curves are not observed in FBC devices with MoO_x or in the first set of manufactured IBC devices as presented in Section 5.2 and Section 5.3.2, respectively. Hence, s-shaped J-V curves can possibly be related to manufacturing problems and long downtime of tools interrupting processing of the presented devices. To obtain more understanding on the device performance, additional experiments are necessary.

5.4.2. MoO_x thickness series without PT

As explained in Section 1.4 and Section 2.4, PT is introduced in FBC devices where MoO_x serves as HTL to ensure pre-oxidation of (*i*)a-Si:H, preserve high MoO_x WF and to enable high FF [70]. However, during fabrication of IBC devices in this project, oxidation of the surface is possibly achieved during deposition of SiO_x indicating that introducing oxidic PT is potentially not necessary for preserving high-quality MoO_x. Moreover, as presented in Section 5.2, PT has a negative effect on the performance of the electron collection stack, thus excluding PT is expected to improve electron collection. To investigate the necessity of PT for application in IBC solar cells, devices without PT are manufactured. Moreover, MoO_x thickness is varied in the range from 1.7 nm to 7 nm as excluding PT potentially requires higher thickness of MoO_x as discussed by [70].

External parameters of fabricated devices are presented in Figure 5.22. Results presented in this Figure correspond to the results of devices with the largest pitch as the best performing devices from the manufactured batch, while information about other devices can be found in Appendix A. One set of experiments was conducted to test the performance of devices without PT, thus only general trends can be addressed in this Section. For better understanding of the role of PT in IBC devices and a complete analysis of device performance, further inquiry is required. Moreover, devices with 3 nm MoO_x show considerably lower performance compared to other devices, which is related to fabrication flaws. Hence, these devices are not included in the analysis in this Section.

Generally, increasing the thickness of MoO_x leads to a decrease in all parameters apart from V_{OC}. The decrease in J_{SC} following increase in MoO_x thickness is potentially related to higher WF of MoO_x and resulting reduced electron collection as described in Section 5.1. The substantial drop in J_{SC} for 7 nm MoO_x is likely caused by a more significant effect of increased WF and lower barrier for holes enabling higher recombination losses and suppressing electron collection. While improvement in J_{SC} was expected in devices without PT due to potentially better electron collection, this is not observed from fabricated devices.

On the other hand, an increase in V_{OC} can be ascribed to more successful hole collection due to improved field effect induced by MoO_x of larger thickness and, consequently, larger WF. This is in agreement with observations by [70] and [103], who conclude that optimal thickness for maximizing V_{OC} in MoO_x devices without PT is in the range of 5-8 nm.

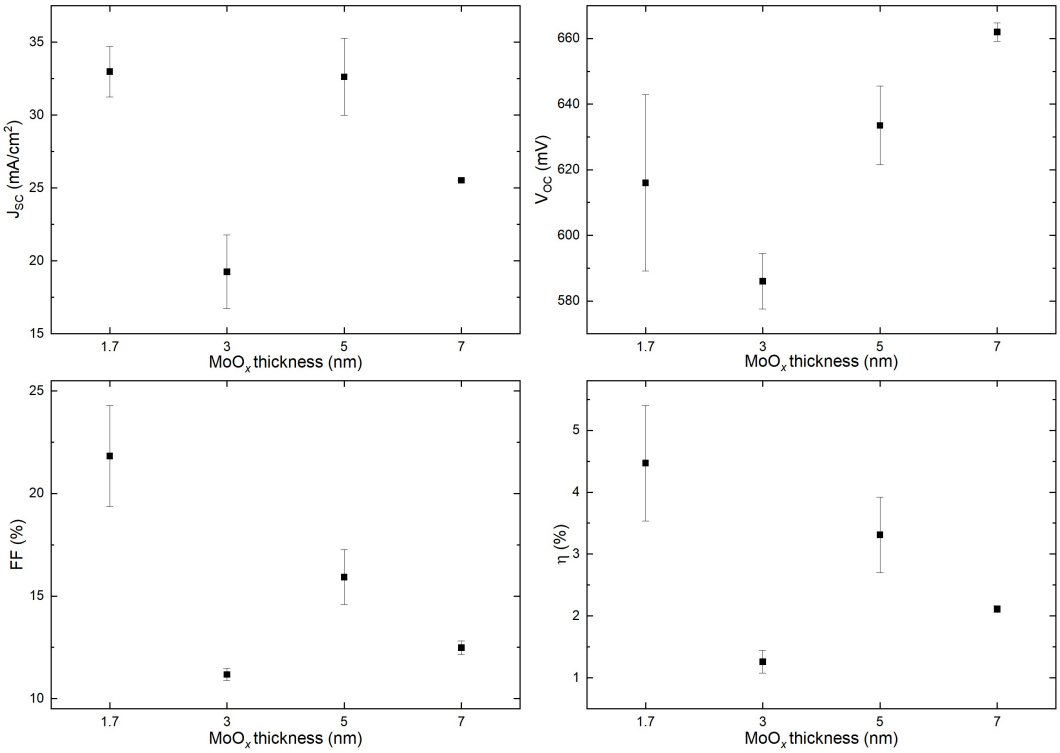
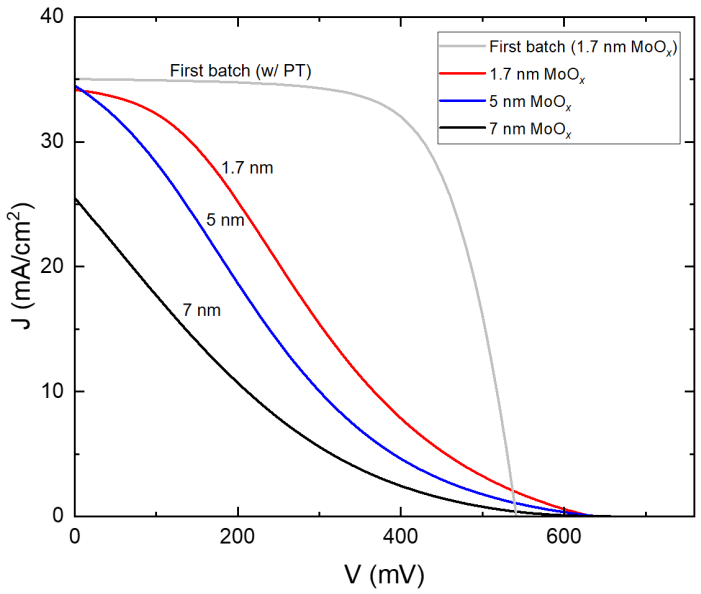


Figure 5.22: External parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x without PT.

Lastly, manufactured devices are characterized by lower FF compared to devices presented in Section 5.3.2 and Section 5.4.1. J-V curves presented in Figure 5.23 are s-shaped, indicating poor band alignment at c-Si/(*i*)a-Si:H/MoO_x interface. S-shape of J-V curves can be related to the absence of interfacial PT and consequent decay of WF of MoO_x, which can negatively impact band alignment and lead to poor hole collection.



MoO_x (nm)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	η (%)
First batch (w/ PT)	35.03	542	67.90	12.88
1.7	34.21	635	23.57	5.13
5	34.50	642	16.87	3.74
7	25.50	664	12.71	2.15

Figure 5.23: J-V curves and external parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x without PT.

5.5. Conclusions and outlook

To overcome the shunting observed in tunneling IBC-SHJ devices and simultaneously keep the fabrication process simple, a novel IBC-SHJ architecture is proposed in this Chapter. Namely, (p)nc-SiO_x:H + (p)nc-Si:H bilayer from tunneling IBC-SHJ devices is replaced with MoO_x as MoO_x is characterized by lower lateral conductivity leading to higher shunt resistance in the device. Hole collection in the proposed device takes place through layer stack involving (i)a-Si:H/MoO_x, while electron collection occurs through (i)a-Si:H/(n)nc-Si:H/MoO_x stack. From results presented in this Chapter significant information about the performance of the novel IBC solar cells is obtained and can serve as a solid starting point for further investigation.

All manufactured FBC devices with alternative contact stacks show satisfactory results with best achieving V_{OC} of 704 mV and FF of 79.29% when implementing the hole collection contact stack and V_{OC} of 715 mV and FF of 82.24% when implementing the electron collection contact stack. The results show that PT improves device performance in the case of devices with MoO_x in hole collection contact as described by [70] and 50 nm (n)nc-Si:H leads to more efficient electron collection. Hence, PT and 50 nm (n)nc-Si:H are implemented in fabricated IBC devices.

The first IBC devices with MoO_x show moderate performance reaching efficiency of 12.9%, which is mainly limited by low V_{OC} and FF. Further optimization of the thickness of MoO_x and PT conditions is executed to observe the impact of these parameters on V_{OC} and FF. From conducted experiments, it is observed that the performance of devices with $MoO_x > 3$ nm is substantially lower compared to devices with thinner layers. This can be explained by poor electron collection due to high WF of MoO_x or by the effect of dipole moment formed at (i)a-Si:H/MoO_x interface. When excluding PT, the best performing devices feature 1.7 nm MoO_x. However, all fabricated devices show poor FF and s-shaped J-V curves. S-shaped J-V curve indicates poor band alignment at Si/MoO_x interface, which can be related to the absence of PT. As thick MoO_x layer shows a detrimental effect on device performance, the focus of future research should shift to optimizing the devices while employing MoO_x up to 3 nm. Moreover, as the absence of PT leads to poor quality of Si/MoO_x interface causing poor FF, PT is necessary for obtaining high efficiencies. With that in mind, the following recommendations for future research are proposed.

Firstly, to achieve high performance of IBC devices, the limitations of the current manufacturing process should be addressed. This can be achieved by performing an extensive analysis of the etching behavior of SiO_x and optimizing etching conditions to minimize underetching of SiO_x. Underetching can be additionally addressed by adjusting the photomask used in photolithography steps. By widening the

overlap area of masks used for covering the BSF and emitter region, the buffer for isotropic etching will be increased and (i)a-Si:H layer will be protected during (n)nc-Si:H etching. Additionally, alternative patterning methods such as shadow masking can be used as a replacement to photolithography. By introducing shadow masks, wet etching processing can be partially or fully avoided, hence also the problem of isotropic etching. Moreover, the use of shadow masks will further simplify the process and is industry compatible.

Secondly, as the interface of MoO_x with (i)a-Si:H and (n)nc-Si:H is likely also the sensitive part of the device, the focus of future research should shift towards optimizing both interfaces. The need for a unique interfacial treatment for both electron and hole collection stacks arises due to the proposed IBC architecture. Hence, adjustments to the current treatment should be explored aiming to obtain an efficient collection of both electrons and holes.

6

Conclusions and outlooks

6.1. Conclusions

During this thesis, two main research objectives are investigated with the final aim of manufacturing high-efficiency IBC-SHJ solar cells. The first research objective addresses the development and optimization of process flowchart for the fabrication of high-efficiency IBC-SHJ solar cells, while the second objective is the optimization of electron and hole collection layers for IBC-SHJ solar cells. The key findings and conclusions are presented in this Section.

6.1.1. Development and optimization of process flowchart for fabrication of high-efficiency IBC-SHJ solar cells

The fabrication of IBC-SHJ solar cells with Si-based contact stacks was addressed in the first part of this project. Selective passivating contact stacks for SHJ solar cells and proof-of-concept FBC devices used for IBC devices are previously developed in PVMD group.

Firstly, IBC-SHJ solar cells featuring TRJ are fabricated. The tunneling IBC architecture is chosen as the starting point of this project due to the simple fabrication process compared to standard IBC devices. The process flowchart used for tunneling IBC solar cell fabrication is adapted based on the previous research from PVMD group to minimize the damage to (*i*)a-Si:H. Photolithography and etching, identified as the main limiting steps in device fabrication, are optimized through a series of experiments examining different photoresists and etching solutions. The first devices are manufactured successfully with an efficiency of 13.90%, J_{SC} of 35.20 mA/cm^2, V_{OC} of 630 mV and FF of 62.66%. However, shunting and consequently low FF can be observed from J-V curves which is likely caused by internal shunting of tunneling IBC architecture and high lateral conductivity of *p*-type nc-Si:H-based blanket layer. Hence, a set of experiments aiming to manufacture standard IBC-SHJ devices is proposed. However, due to the complexity of the manufacturing process of standard IBC-SHJ solar cells, encountered problems, and time restrictions, more research is required for the successful fabrication of standard IBC devices. Instead, novel electron and hole collection contact stacks are proposed for application in the developed tunneling IBC process flowchart. The alternative contact stacks aim to reduce lateral conductivity of the blanket layer while maintaining the fabrication process simple and industry-appealing.

6.1.2. Optimization of electron and hole collection layers of IBC-SHJ solar cells

In alternative contact stacks, MoO_x is proposed as a replacement for *p*-type nc-Si:H-based blanket layer due to its low lateral conductivity. Hence, in the newly developed IBC architecture, hole collection is achieved through MoO_x-based contact stack previously developed in PVMD group, while electron collection takes place through novel contact stack including (*n*)nc-Si:H and MoO_x. High WF of MoO_x is identified as an important prerequisite for effective hole collection, which is enabled by the introduction of PT. On the other hand, the main requirement for achieving efficient electron collection is high doping of (*n*)nc-Si:H, which is realized by a large crystalline fraction in (*n*)nc-Si:H.

Results of FBC devices with hole contact stack featuring MoO_x show V_{OC} of 704 mV and FF of 79.29% when PT is introduced. Devices with the novel electron contact stack reach V_{OC} of 715 mV and FF of 82.24% with 50 nm (*n*)nc-Si:H and MoO_x without PT. Based on the promising results of FBC devices, IBC devices are fabricated with PT and 50 nm (*n*)nc-Si:H. PT is included in IBC devices as

the advantages of PT for hole collection outweigh the minor negative effects on electron collection.

The first newly developed IBC-SHJ solar cells with MoO_x achieved an efficiency of 12.88%, J_{SC} of 35.03 mA/cm^2, V_{OC} of 542 mV and FF of 67.90%, with no shunting occurring in the devices. The preliminary results show that novel device architecture is a promising candidate for further development as it enables simple device processing without restrictions of low shunt resistance. Additional optimization of MoO_x thickness and PT conditions is carried out to investigate the impact of these parameters on V_{OC} and FF. From the conducted experiments it was observed that the optimal thickness of MoO_x is below 5 nm. Moreover, it is observed that PT is required for good interface of MoO_x with (*i*)a-Si:H, which is reflected in improved FF.

6.2. Outlooks

Based on encountered process challenges, the performance of the manufactured devices, and conclusions presented in the previous Section, outlooks for future research are discussed in this Section. Presented recommendations focus on the improvements of the fabrication process of IBC-SHJ solar cells and optimization of materials and layers implemented in devices.

6.2.1. Improvements of the fabrication process of IBC-SHJ solar cells

During the processing of IBC-SHJ devices as proposed in the flowchart developed in this thesis, nonuniform etching was observed as the main obstacle to the successful fabrication of the devices. To address this, an extensive set of etching tests should be carried out with varying concentrations of the solutions and etching times. Etching of doped Si layers can be tackled with a variety of etching solutions (e.g. KOH, TMAH or polysilicon etch) and additives (e.g. isopropanol in KOH solution) to obtain desired etching uniformity. As for SiO_x, different concentrations of HF and BHF solutions can be tested to ensure uniform etching on textured surface and minimize overetching time as it leads to the widening of BSF region. Additionally, as SiO_x only serves as an etching barrier in the proposed flowcharts, deposition conditions such as power and gas flows can be adapted to obtain a more uniform layer and adjust the layer's etch rate. On the other hand, if clear trends of widening of the structures due to isotropic etching of SiO_x can be established, an alternative photomask with narrower BSF region can be used so that isotropic etching is taken into account during lithographic patterning.

Alternatively, photolithography can be replaced by a different patterning technique such as shadow masking [104], [20], laser ablation [105], [106] or inkjet printing [107]. Thus far, successful patterning of doped layers has been achieved with shadow masking, which is also a cheap, industry-compatible patterning method. Moreover, by replacing a part of or all photolithography steps with shadow masking step, the need for wet chemical etching is minimized. Shadow masking has shown excellent results when patterning devices with TRJ [20], [108] as only one mask has to be aligned for patterning of doped layers. Hence, the use of shadow masks is suitable for processing of novel IBC design proposed in this thesis.

All fabricated devices show better performance with the increase in pitch size, which can be ascribed to imperfect edges between BSF and emitter due to etching. In this project the largest pitch size of fabricated devices is 1.2 mm, while other authors report devices with pitch size over 2 mm [61]. This is also favorable for the use of shadow mask patterning instead of photolithography, as shadow masks allow for lower precision and also suffer from imperfect edges between BSF and emitter. Therefore, further increasing pitch size should be investigated. However, as the increase in pitch size leads to higher series resistance, the optimal pitch size is expected to be a trade-off between the edge defects and series resistance losses.

6.2.2. Optimization of materials and layers implemented in devices

As the front side of IBC devices is not limited by carrier collection, once good surface passivation is guaranteed the front side can be relatively freely optimized to minimize optical losses. In this project, SiO_x serves as ARC and protective layer during etching at the front side of the device. However, SiO_x thickness is not optimized to act as efficient ARC. By introducing an improved ARC, reflection losses can be minimized leading to higher J_{SC}. A common ARC consisting of SiO_x and SiN_x can be explored as both materials can be deposited by PECVD at low temperatures suitable for SHJ devices. In [109], optimal thickness of SiO_x and SiN_x is proposed as 100 nm or 140 nm and 50 nm or 80 nm , respectively. However, to find optimal ARC while accounting for layer stack deposited on the front side of IBC

devices proposed in this project, optical simulations including specific device characteristics should be performed.

In order to decrease resistive losses in metal contacts and improve FF of the devices, thicker metal electrodes should be introduced. Thick metal electrodes can be efficiently obtained by Cu electroplating, with thickness in the range of tens of µm using the electroplating setup available in EKL [110]. Moreover, Cu is a good candidate for application in solar cells in terms of high conductivity and low cost [111]. However, the mass industrial application is hindered mainly by the complexity of the copper electroplating method [112]. Alternatively, metalization can be achieved by Ag screen printing, a simple technique that is already widely applied in industry. Moreover, screen-printed metal fingers can serve as a metal mask for wet etching of TCO layer, if a suitable TCO is selected [113], [114]. In combination with shadow masking for patterning of doped layers, photolithography-free patterning of IBC devices can potentially be achieved. However, a downside of screen printing process is low alignment precision compared to methods involving photolithography. Further investigation is necessary to compare the use of electroplated Cu and screen-printed Ag by analyzing patterning precision, process simplification and cost-effectiveness.

As discussed in Chapter 5, the (i)a-Si:H/MoO_x and (n)nc-Si:H/MoO_x interfaces are sensitive parts of manufactured devices for hole and electron collection, respectively, as they influence selectivity and transport of charge carriers. In the case of MoO_x/(i)a-Si:H high MoO_x WF is required, which can be achieved by introducing interfacial PT [70]. However, lower WF of MoO_x is necessary for efficient electron transport at the interface of MoO_x and (n)nc-Si:H. Due to the proposed IBC architecture and simplified fabrication process, a unique interfacial treatment for electron and hole collection stacks is required. Therefore, modifications to the current treatment should be investigated in order to achieve simultaneously efficient electron and hole collection.

A

Optimization of contact stacks of IBC-SHJ solar cells with MoO_x

Even though IBC devices with smaller pitch perform worse compared to devices with larger pitch, similar trends can be observed for all three analyzed pitch sizes. Poor performance of smaller pitch was explained by increased number of edges between emitter and BSF over total cell area where large amount of defects is present. However, this does not impact general trends when devices with the same pitch size are analyzed.

Figure A.1 and Figure A.2 show external parameters of IBC solar cells with PT with 300 µm and 650 µm pitch size, respectively. Low performance of devices with 1.7 nm MoO_x can be assigned to processing fluctuation. Hence, these devices cannot be analyzed accurately. Additionally, no devices with 650 µm pitch with 7 nm MoO_x are manufactured successfully, which can be be related to processing fluctuations.

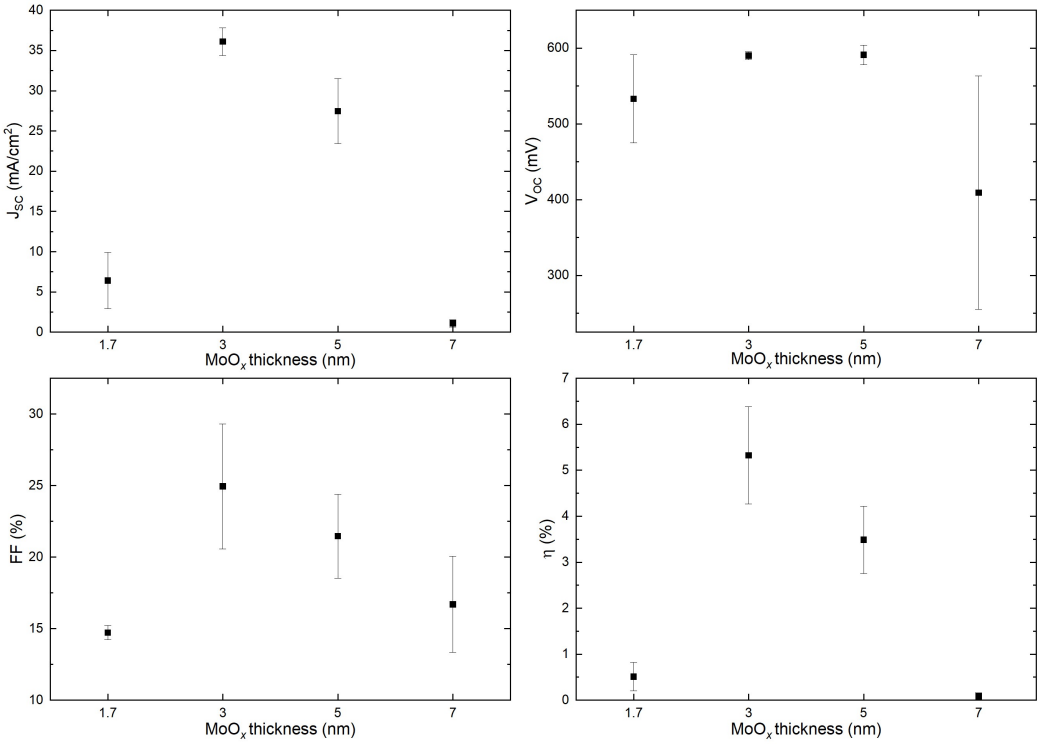


Figure A.1: External parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x with PT. Parameters of devices with 300 µm pitch (cell type A) are shown.

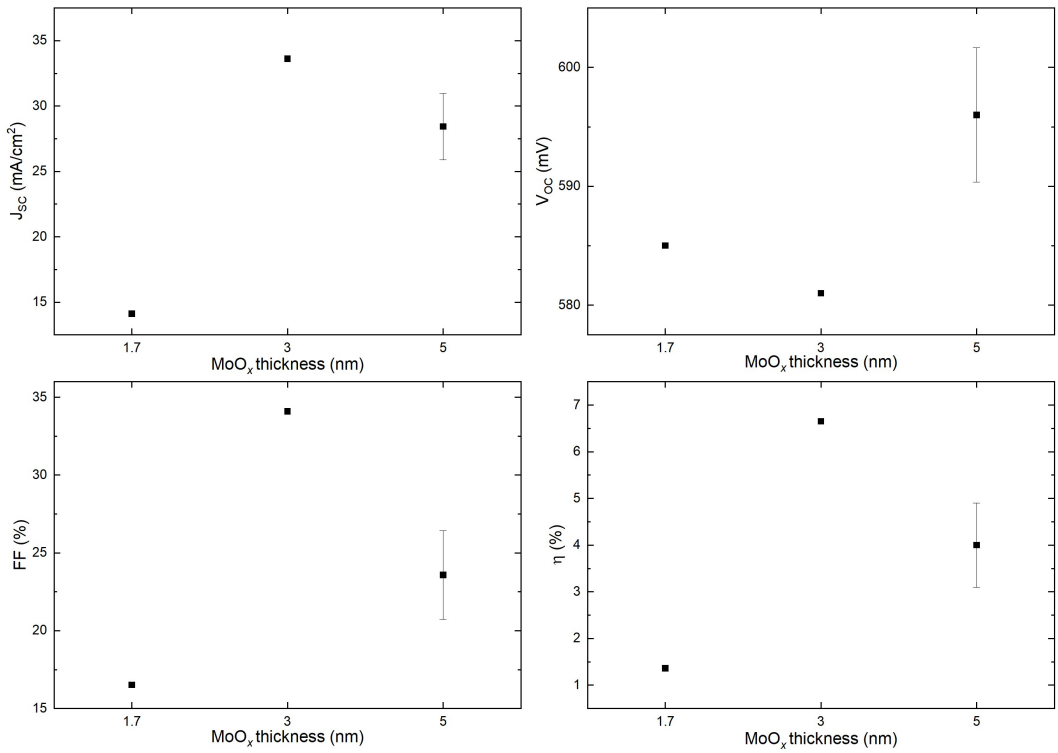


Figure A.2: External parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x with PT. Parameters of devices with 650 µm pitch (cell type B) are shown.

Figure A.3 and Figure A.4 show external parameters of IBC solar cells without PT with 300 µm and 650 µm pitch size, respectively. Similar trends are observed with devices of lower pitch sizes to the ones with pitch size of 1200 µm. In the case of devices with 300 µm pitch, the performance of devices with 5 nm MoO_x differs from trends observed with different devices. However, due to the poor performance of all fabricated devices with 300 µm pitch, more investigation is necessary for reliable analysis.

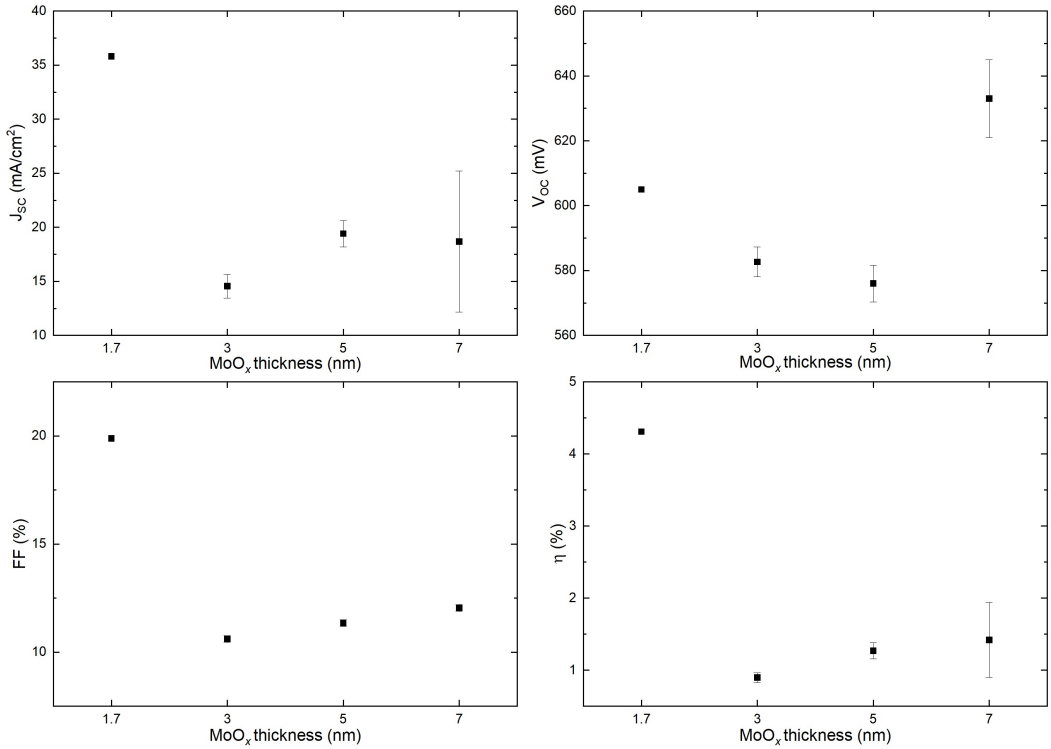


Figure A.3: External parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x without PT. Parameters of devices with 300 µm pitch (cell type A) are shown.

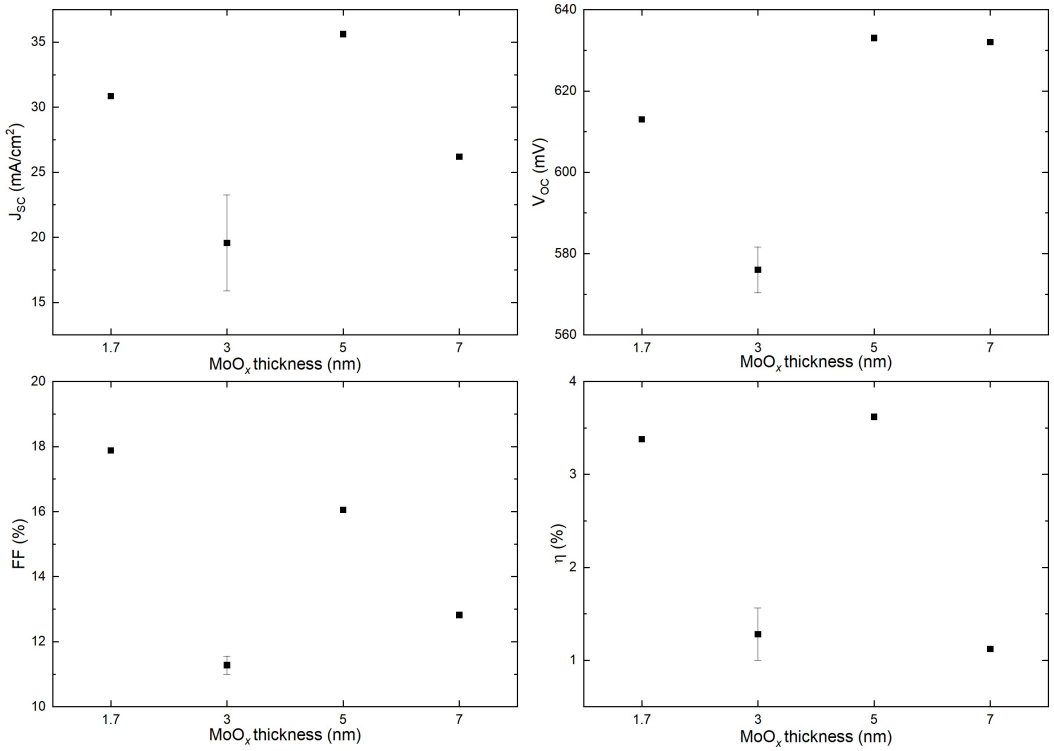


Figure A.4: External parameters of double-side textured IBC-SHJ solar cells with varying thickness of MoO_x without PT. Parameters of devices with 650 µm pitch (cell type B) are shown.

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With this master thesis, my time as a student at TU Delft comes to an end after five incredible years. The choice to pursue my master's education in Sustainable Energy Technology, a field that was far from my prior education, turned out to be a challenging but rewarding decision. During my master's studies, I had a chance to learn about solar energy and I found my passion in this dynamic field. Herewith, I'd want to express my gratitude to the whole PVMD group for the opportunity to do my master thesis in the solar energy field and for the support during the thesis.

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