A Capacitive Galvanically Isolated Full-Bridge Converter

Granello, Pierpaolo; Schirone, Luigi; Bauer, Pavol

DOI
10.1109/TTE.2025.3527724

Publication date
2025

Document Version
Final published version

Published in
IEEE Transactions on Transportation Electrification

A Capacitive Galvanically Isolated Full-Bridge Converter

Pierpaolo Granello, *Student Member, IEEE*, Luigi Schirone, *Member, IEEE*, and Pavol Bauer, *Senior Member, IEEE*

***Abstract*— This article proposes a transformerless, capacitively isolated converter based on a full-bridge topology with phase shift control. Compared to the existing capacitively isolated converters, the proposed design offers the advantage of zero mean voltage across the isolating capacitors, thereby reducing voltage stress. A comprehensive analytical model is developed to describe the converter's operation in both continuous and discontinuous conduction modes. The model is validated through an experimental prototype tested at power levels up to 6 kW and switching frequencies up to 500 kHz, achieving a peak conversion efficiency exceeding 98%. The experimental results confirm the accuracy of the theoretical model and waveforms.**

***Index Terms*— Capacitive isolation, dc–dc power conversion, full-bridge converter, isolated converter.**

I. Introduction

THE number of electric vehicles (EVs) in the world is rapidly increasing and arousing attractiveness for governmental initiatives due to their environmental advantages [1]. Nevertheless, several challenges remain, including high costs, limited driving range, long charging times, and limited urban charging infrastructure, all of which contribute to driving range anxiety [2], [3], [4]. The transition to electric mobility can thus be facilitated by improving the EV charging infrastructure, which is a more viable solution compared to increasing battery capacity [5]. Hence, remarkable research effort has been spent to enhance the efficiency, reduce the size, and lower the costs of power conversion stages for battery chargers [6], [7].

Due to the vulnerability of both the vehicle and driver during charging phases, especially as modern EVs operate with several hundred volts for their batteries, it is essential to galvanically isolate the battery from both ground and other vehicles [8]. Magnetically coupled switching converters are commonly used to achieve isolated voltage or current conversion. However, transformer design involves the complex optimization of parameters, such as winding and core losses, which can represent a significant portion of overall converter losses [9], [10]. As a result, there is growing interest in exploring alternative approaches to implement galvanic isolation [11], [12], [13], [14], [15].

The capacitively isolated power converters have been proposed in literature as an effective and highly efficient alternative for achieving galvanic isolation in dc/dc conversion [16]. These solutions have been shown to comply with human safety standards for EV applications, such as IEC 60990 [17]. The concept of galvanic isolation using capacitors was first patented in 1996 [18], where a transformerless line isolation single ended primary iductor converter (SEPIC) converter was obtained by adding a capacitor on the return line. Its inverting variant, based on a Ćuk topology, was patented in [19] and further detailed in [20]. However, these topologies are constrained in power handling capability and operating switching frequency due to the limited allowable capacitance, as the isolation capacitors impose a load on the main switch and contribute to current leakage from the grid [20]. A half-bridge-based isolation stage in series was patented in [21], with switching frequency variation control proposed in [22] and [23]. Isolation is achieved through capacitors placed on both the bridge output and return lines. Furthermore, a ladder-type switched capacitor-based step-down converter was proposed for LED applications in [24], where the isolation barrier is interfaced to ac output terminals of the ladder circuit. Despite their innovation, these topologies are typically designed for low-power applications and are constrained by output voltage (capped at half of the input) as well as the presence of a dc voltage across the isolation capacitors. This leads to variations in their effective capacitance and accelerated aging [25], [26]. These limitations become particularly significant in EV applications, where the isolated ground may experience a voltage lift relative to the input-side ground.

The capacitive isolated power converter presented in this work addresses these challenges by using symmetrical current drive throughout the entire switching cycle, reducing the dc offset across the isolation capacitors to a negligible level. This minimizes the risk of human shock and enables compliance with EV working voltages. The proposed power converter provides highly efficient transformerless galvanic isolation for voltage and power levels suitable for EV charging applications. It also enables 1:1 conversion while supporting the possibility for step-down voltage conversion via phase shift control. Furthermore, the integration of GaN FETs allows for higher switching frequencies, enabling the use of ceramic capacitors with low equivalent series resistance (ESR) and equivalent series inductance (ESL), contributing to reducing the conversion losses.

The remainder of this article is organized as follows: Section II presents a detailed explanation of the converter's working principle through a comprehensive analytical model, deriving the main equations for both continuous conduction

Received 20 September 2024; revised 26 November 2024; accepted 5 January 2025. Date of publication 9 January 2025; date of current version 14 May 2025. *(Corresponding author: Pierpaolo Granello.)*

The authors are with the Department of DC Systems, Energy Conversion and Storage of Delft University of Technology, The Netherlands, and with the School of Aerospace Engineering of Sapienza, University of Rome (e-mail: pierpaolo.granello@uniroma1.it).

Digital Object Identifier 10.1109/TTE.2025.3527724

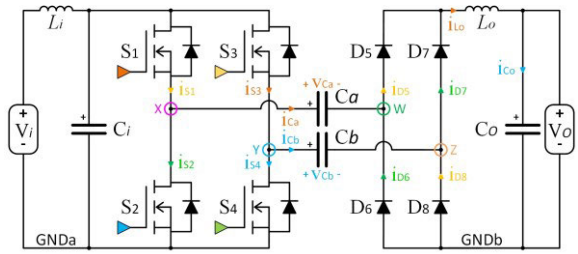

Fig. 1. PSCIFB.

mode (CCM) and discontinuous conduction mode (DCM). Section III validates the proposed analytical model and the converter's operation using the experimental setup, demonstrating the negligible impact of the isolation capacitors on the converter's power losses.

II. Capacitive Isolated Full Bridge

The proposed phase-shifted capacitive-isolated full-bridge (PSCIFB) topology is illustrated in Fig. 1. Configured as a conventional full-bridge converter, it comprises four active switches on the primary side (left) and four rectifying diodes on the secondary side (right). Power flows directionally from the input source, denoted as V_i, toward the output load, denoted as V_o. The interconnection between the input and output is established through the use of isolating capacitors C_a and C_b. As the current path between the source and load closes through the capacitors C_a and C_b, a 1:1 ratio transformer-equivalent isolation between the source and the load is typically achieved. Notably, the proposed phase-shifting control imparts versatility to the converter, enabling its operation in both step down and 1:1 conversion modes. Specifically, switches S_1 and S_2 are driven with a 50% duty cycle denoted as D and operate 180° out of phase with each other. This same phasing arrangement applies to switches S_3 and S_4, which are likewise offset in phase relative to those in leg of S_1–S_2. The degree of this phase shift controls the overlapping period (φ) between diagonal switches, thereby determining the amount of energy transferred to the secondary side. The input L_C filter, comprising the inductor L_i and capacitor C_i, is designed to filter the current drawn from the power supply V_i. Simultaneously, the output capacitor C_o is employed to filter out the alternating components from the output current. However, it is important to acknowledge that while the input L_C filter plays a role in current filtering, it lacks significance in the model analysis, and thus, it is omitted from the modeling analysis. Once the switches and diodes are closed, their parasitic capacitances are bypassed and do not contribute to the series connection with capacitors C_a, C_b, and C_o within the closed current path. These capacitors collectively form an equivalent series capacitance C_{eq}, which is in series with the output inductor L_o, resulting in a resonant frequency $f_r \approx (2\pi\sqrt{L_o C_{\text{eq}}})^{-1}$. To ensure that the resonant circuit behaves as an inductive impedance and thus allowing for the control of the inductor current amplitude through modulation of the diagonal overlapping period φ [27], it is crucial to drive the converter with a switching frequency

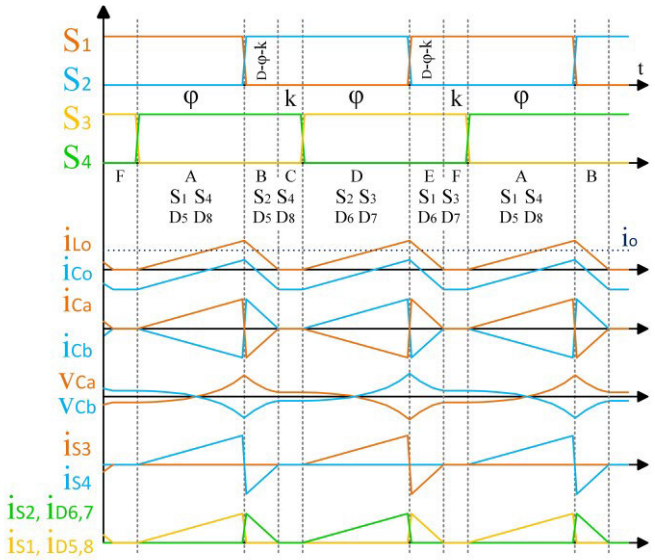

Fig. 2. Switching sequence in DCM (k vanishes in CCM).

that exceeds this resonance frequency. For the purpose of simplifying the analysis, the load is represented as a current source. Additionally, both isolating capacitors (C_a and C_b) are assumed to have equal capacitances, and all devices are treated as ideal in this model.

Fig. 2 illustrates the switching sequence and circuit waveforms based on the proposed control scheme during DCM operation. In the scenario of CCM operation, the duration "k" of the subintervals C and F diminishes, approaching zero, and becomes negligible in the calculations.

A single switching cycle is divided into six subintervals, as shown in Fig. 3, where subintervals C and F are grouped together.

The states are briefly described as follows.

State A: During this subinterval [see Fig. 3(a)] of length φ, switches S_1 and S_4 are driven ON and the current flowing through the isolation capacitors C_a and C_b is rectified on the secondary side by means of diodes D_5 and D_8. The current flowing in the output inductor L_o during this subinterval experiences a positive increment equal to

$$\Delta^{A}_{i_{Lo}} = \frac{(V_i - V_o - V_{Ca} + V_{Cb})\varphi T_s}{L_o} \approx \frac{(V_i - V_o)\varphi T_s}{L_o}. \quad (1)$$

The symmetry of the circuit drives the average capacitors' voltages, V_{Ca} and V_{Cb}, to be the same at steady state. Accordingly, the contribution of their difference can be omitted in (1).

The voltage ripple on C_a and C_b can be assessed based on the average current through them

$$\Delta V_{C_{a,b}} = \pm \frac{\varphi \cdot T_s}{C_{a+,b-}} i_{\text{AVG}(L_o)} \quad (2)$$

where C_{a+} represents the charging of capacitor C_a with a positive voltage (C_{b-} with a negative voltage) according to the polarities in Fig. 1. The values of C_a and C_b are chosen large enough to make their voltage ripple negligible with respect to the other voltages along the circuit.

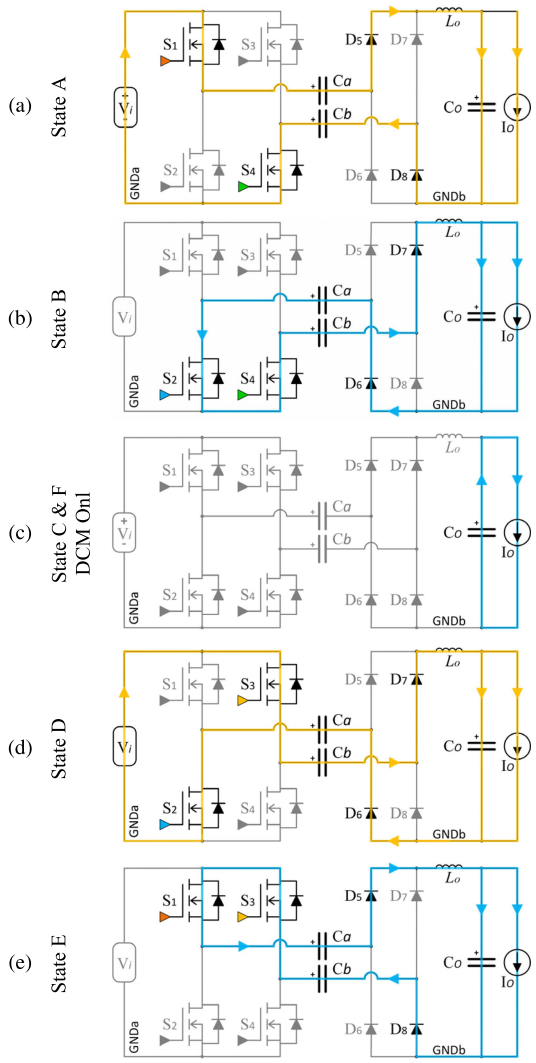

Fig. 3. Current paths during the different subintervals. In yellow, the current drawn from the power supply. (a) State A. (b) State B. (c) State C and F DCM only. (d) State D. (e) State E.

State B: During this subinterval [see Fig. 3(b)] of length D–φ–k, switch S_1 is turned off, while S_2 is driven ON. A ground path for the capacitors C_a and C_b is thereby established, resulting in a negative and positive voltage on the diode bridge rectifier nodes (W and Z nodes as in Fig. 1) due to their charge during the previous state (state A). Consequently, diodes D_6 and D_7 become forward biased, and the output inductor (L_o) undergoes discharge with a decrease in current equal to

$$\Delta^B_{i_{Lo}} \approx \frac{-V_o(D-\varphi-k)T_s}{L_o} \tag{3}$$

where the contributions of capacitors' voltages, V_{Ca} and V_{Cb}, were neglected for the same reasons as in (1). The isolation capacitors are now discharging with a voltage ripple of

$$\Delta V_{C_{a,b}} = \mp \frac{(D-\varphi-k)T_s}{C_{a-,b+}} i_{\mathrm{AVG}(L_o)}. \tag{4}$$

State D: During this subinterval [see Fig. 3(d)] of length φ, the switch S_4 is turned OFF, while S_3 is driven ON. With a positive voltage now applied to the node Z through capacitor C_b, diodes D_6 and D_7 rectify the current flowing through the output inductor L_o, resulting in a positive increase, as described in (1). Additionally, the isolation capacitors C_a and C_b are charging with an opposite current compared to that in state A, as indicated in (4), but with a negative sign.

State E: During this subinterval [see Fig. 3(e)] of length D–φ–k, the switch S_2 is turned OFF, while S_1 is driven ON. Analogous to the description for state B, capacitors C_a and C_b now, respectively, exhibit the positive and negative voltages on the diode bridge rectifier nodes (nodes W and Z) due to their charge during the previous state D. Consequently, diodes D_5 and D_8 become forward biased, and the output inductor L_o undergoes discharge with a decrease in current, as described in (3). Simultaneously, the isolation capacitors C_a and C_b are discharging as in state B [see (4)], but with negative sign.

States C and F: These states exclusively occur in DCM operation, where the output inductor L_o completely discharges during states B or E, driving all the bridge diodes OFF. Consequently, the output capacitor undergoes discharge, and capacitors C_a and C_b have no flowing current, ideally maintaining their charge state unchanged.

At steady state, where the average value of the output inductor current ripple must be zero ($\sum \Delta^i_{i_{Lo}} = 0$), it is possible to express the output voltage value as a function of the applied diagonal overlap period φ and the resulting zero current period k in the context of DCM operation

$$V_o = V_i \frac{\varphi}{D-k}. \tag{5}$$

Hence, it is also possible to express the average output current I_o for DCM as the sum of the areas covered by the output inductor current on a semi-period T_s, as delineated in the following equation:

$$I_{Lo_{\mathrm{DCM}}} = \frac{1}{DTs}\left(\frac{\frac{1}{2}(V_i-V_o)\varphi^2 T_s^2}{L_o} + \frac{\frac{1}{2}V_o(D-\varphi-k)^2 T_s^2}{L_o}\right). \tag{6}$$

Additionally, through the solution of (5) for the variable k

$$k = \frac{DV_o - \varphi V_i}{V_o} \tag{7}$$

and subsequent substitution in (6), the value of φ in DCM operation can be determined as

$$\varphi_{\mathrm{DCM}} = \sqrt{\frac{2I_o D L_o V_o}{T_s(V_i-V_o)V_i}}. \tag{8}$$

Furthermore, the value of φ in CCM can be found by substituting (5) with $k = 0$ into (6), resulting in

$$\varphi_{\mathrm{CCM}} = \frac{2I_o L_o}{(V_i-V_o)V_i T_s}. \tag{9}$$

Finally, the minimum output inductor current I_{Lmin} can be evaluated, being zero in DCM and as given in the following equation in CCM:

$$I_{Lo_{\mathrm{min}}} = I_o - \frac{\Delta_{i_{Lo}}}{2} = I_o - \frac{(V_i-V_o)\varphi T_s}{2L_o}. \tag{10}$$

Ultimately, the boundary conditions for φ can be expressed by substituting (5) with $k = 0$ in (10) and solving it for $I_{L\min} = 0$, yielding to

$$\varphi_{\text{crit}_{1,2}} = \frac{D \pm \sqrt{D^2 - \frac{8 I_o L_o D}{V_i T_s}}}{2}. \tag{11}$$

According to the analysis, the converter exhibits no critical or optimal load, as the output voltage is determined by the applied phase shift φ and the load current I_o. The converter dynamically operates in CCM or DCM based on the load conditions, with the boundary conditions defined by the critical phase shift $\varphi_{\text{crit}_{1,2}}$ as in (11).

Examining the plot in Fig. 2, the current drawn from the converter's input is exactly the current $i_{S1,S3}$ passing through switches S_1 and S_3 during states A and D, as highlighted in yellow in Fig. 3(a) and (d). In state E, no current is drawn from the input source as the inductor current i_{Lo} completes its path through switches S_1 and S_3, as illustrated in Fig. 3(e).

Furthermore, the use of a full-bridge topology offers significant advantages over other capacitively coupled configurations, such as the half bridge, by effectively mitigating the accumulation of forced dc voltage offset across the isolating capacitors C_a and C_b. Indeed, in this topology, current flows alternately through the capacitors for equal durations during an entire switching cycle. This balanced current flow reduces the voltage stress on these components and prevents voltage lift between the isolated and input-side grounds. However, it is worth noting that during subintervals, the isolating capacitors experience transient charging, resulting in temporary but zero-mean voltage offsets between grounds. These offsets are equal to the voltage reached in a single subinterval, as detailed by (2) and (4).

III. Experimental Results

The proposed analytical model was validated by a 6-kW experimental prototype, featuring IGOT60R070D1 GaN FETs from Infineon as power switches on the primary side (S1 through S4). The switches operated at a frequency in the range of 100–500 kHz. To ensure a safe operating margin, the device operated with a maximum input voltage of 500 V and a maximum current of 12 A, aligning with the voltage and current ratings of the selected switches. Notably, both the selected FETs and diodes featured a thermal pad on the top side of their case, offering a practical solution for thermal dissipation.

Table I summarizes the main prototype parameters, and Table II provides a list of the main components for the prototype. For the isolation capacitors C_a and C_b, a parallel configuration of ten ceramic capacitors was used, achieving a total of 10 μF, with a 650-V rating. This capacitance value was selected to ensure compliance with the current rating of a single capacitor with a safe margin and to maintain a capacitor voltage ripple below 4 V, as determined by (2) and (4) under worst case conditions (i.e., 1:1 conversion mode, f_S of 150 kHz and 12-A load). Additionally, this value satisfies the requirement for the equivalent series capacitance C_{eq} to maintain $f_S \gg f_r = 40$ kHz with the proposed switching frequencies f_S ranging from 150 to 500 kHz.

TABLE I
Main Prototype Parameters

Parameter	Value	Units
V_i	50÷500	V
f_S	100-500	kHz
V_O	50÷500	V
I_O	4÷12	A
P_{Omax}	6	kW

TABLE II
Prototype Components List

Component	Manufacturer	Part Number
$S_{1\div4}$	Infineon	IGOT60R070D1
$D_{1\div8}$	Infineon	IDDD20G65C6
$C_{\text{a,b,i,o}}$	Knowles Syfer	2220Y6300105KXTWS2
L_o	EPCOS - TDK	B82559B5472A019
L_i	EPCOS - TDK	B82559B2102A019
Gate Driver	Infineon	1EDF5673K

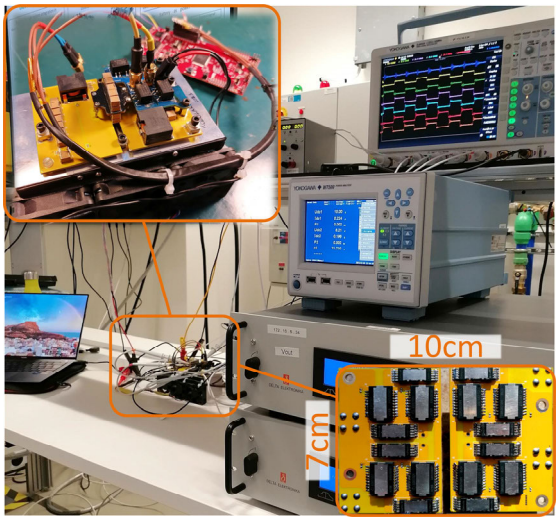

Fig. 4. Prototype and experimental setup.

Fig. 4 shows the designed prototype with a size of the main PCB of 10 × 7 cm. The circuit is driven open loop by a C2000 board manufactured by Texas Instruments, capable of generating pulse width modulation (PWM) signals at various frequencies and with different phase shift values through an easy programmable interface on Simulink.

Fig. 5 illustrates the test setup, featuring two bidirectional power supplies (SM500-CP-90) generating the input voltage and constant current load. The measurements of efficiency, current, and voltage values were conducted using a Yokogawa WT500 with a four-wire connection. The current through isolating capacitors C_a and C_b was measured using a Rogowski current probe, while the voltage across these capacitors was measured with an isolated voltage probe.

Figs. 6 and 7 display the oscilloscope waveforms representative of DCM and CCM operations, respectively. The system

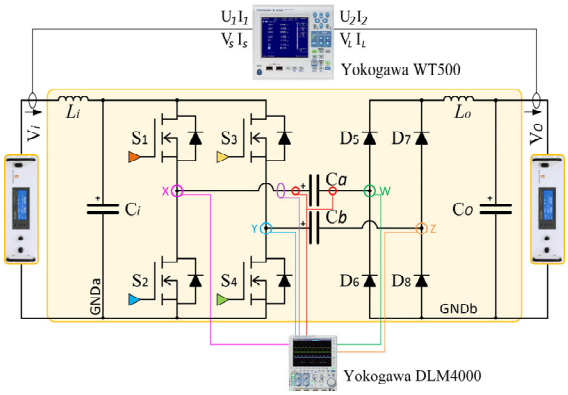

Fig. 5. Protype test setup.

Fig. 6. Oscilloscope waveforms for DCM operation.

Fig. 7. Oscilloscope waveforms for CCM operation.

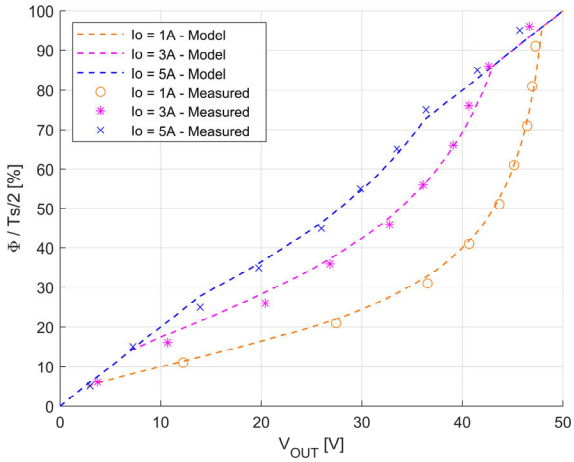

Fig. 8. Theoretical versus experimental φ at 500 kHz.

operates at a switching frequency of 100 kHz, with an input voltage of 50 V, and a constant current load of 2 A. The color scheme of the waveforms aligns with the probe colors specified in Figs. 1 and 5. Notably, in CCM, the drain–source voltages at nodes X, Y, W, and Z exhibit a 180° phase shift, as they are operated with $\varphi = 0\%$. Conversely, in DCM, they exhibit a 30% overlap based on the applied driving phase shift. The violet waveform represents the current through isolating capacitors C_a and C_b, measured by a Rogowski current probe. The behavior of the isolating capacitors current aligns with the model described in Section II. Notably, there is a discernible inversion of current direction marked by a sudden jump from positive to negative or vice versa. This phenomenon corresponds to the transitions between states A and B and D and E, as illustrated in the theoretical waveforms presented in Fig. 2. Accordingly, by confirming the isolating capacitors' current waveform, the compliance of the output rectifying diodes' current waveforms is also established in the theoretical waveforms of Fig. 2. Indeed, the shape of the isolating capacitors' current determines their charge state and consequently which diodes will be forward biased in the next state. In Fig. 6, states C and F are additionally involved for DCM operation, where no current flows through the isolating capacitors, and only the output capacitor is discharging. The red waveform represents the differential voltage measured with the isolated voltage probe across the isolating capacitors. Notably, the mean voltage across them is null, introducing no dc offset on the isolating capacitors and consequently no dc offset between the input and the output isolated ground.

As previously described in Section II, during specific subintervals, the charging dynamics of the isolating capacitors cause a transient voltage offset between the input and output grounds, equal to the voltage reached in a single subinterval, with a maximum peak of less than 4 V in the figure due to the given operating conditions.

A. Model Validation

In accordance with (5), (8), and (9) from Section II, the variable φ, normalized over the semi-period $T_s/2$, can be plotted against the controlled output voltage, as shown in Fig. 8. This plot is based on an input voltage of 50 V, different current loads of 1, 3, and 5 A, and a switching frequency of 500 kHz. Fig. 8 illustrates the close alignment between the theoretical curve and the experimental data points obtained from on-prototype measurements.

B. Loss Analysis

The efficiency of the converter was measured across a wide range of operating conditions, as detailed in Table I. Fig. 9

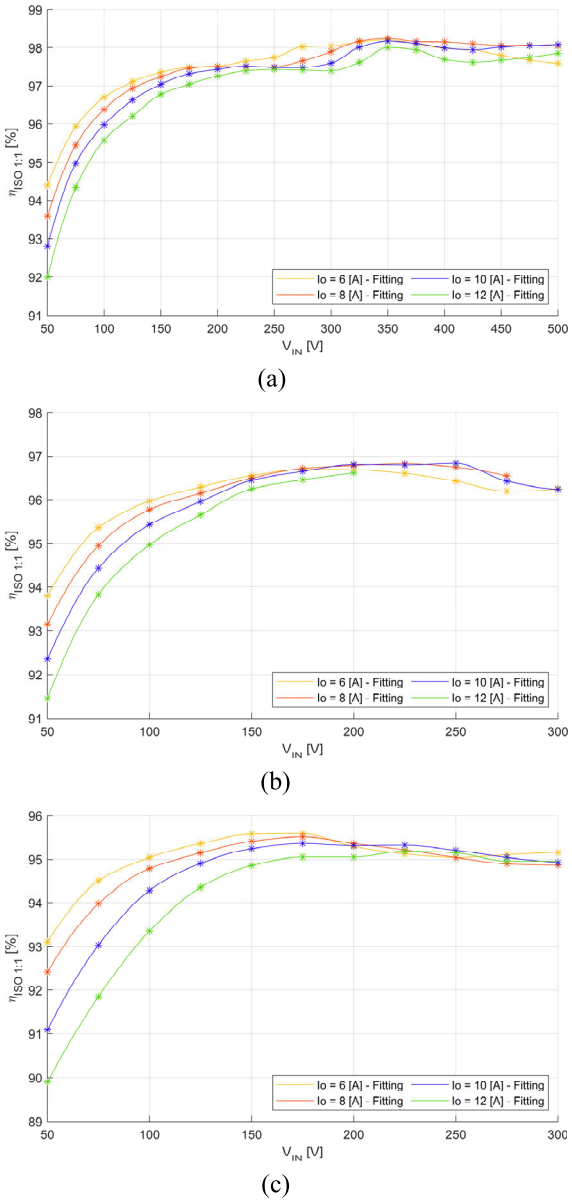

Fig. 9. Converter efficiency in 1:1 isolation mode. (a) $f_s = 150$ kHz. (b) $f_s = 300$ kHz. (c) $f_s = 500$ kHz.

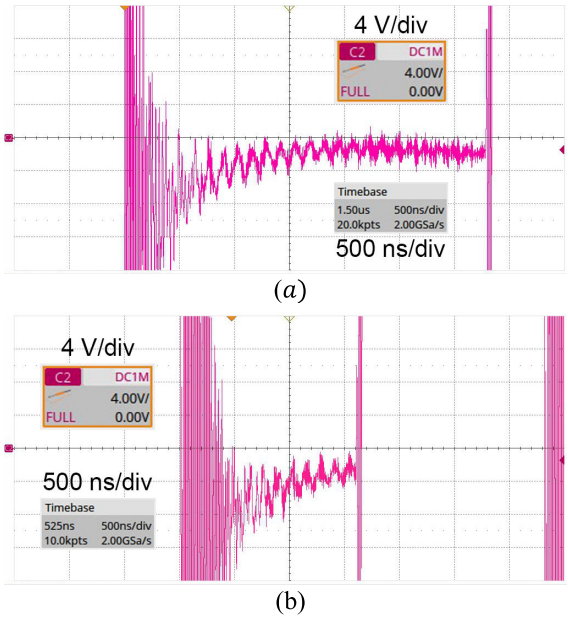

Fig. 10. Voltage drop across diodes D_7 and D_8. (a) $f_s = 150$ kHz. (b) $f_s = 500$ kHz.

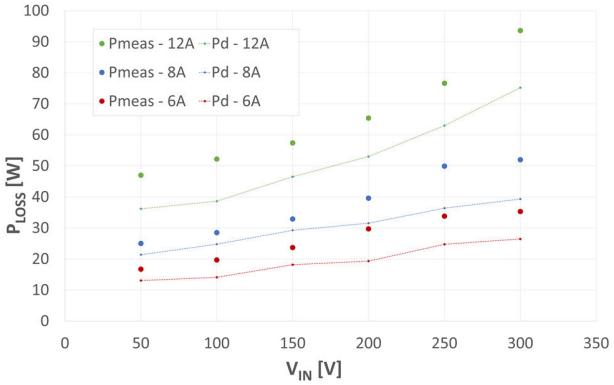

Fig. 11. Experimental power losses for $f_S = 150$ kHz. Pmeas: converter losses. Pd: diodes losses.

presents the results achieved in 1:1 isolation mode ($\varphi = 0$), with input voltages ranging from 50 to 500 V, load current between 6 and 12 A, and switching frequencies between 150 and 500 kHz. It can be observed that the conversion efficiency is always higher than 94.8% for $V_{\text{IN}} > 150$ V, with values greater than 97.5% for $f_S = 150$ kHz and $V_{\text{IN}} > 200$ V. The efficiency peaks at 98.2% at an input voltage of 350 V.

These high efficiency levels are attributed to the minimized losses in the capacitors, which are estimated to be less than a few hundred milliwatts when using multilayer ceramic capacitors with X7R dielectric within the operated frequency range [28].

The power dissipation in the rectifying diodes was also experimentally derived by analyzing the voltage drop waveforms measured across D_7 and D_8 under varying load currents and switching frequencies, as shown in Fig. 10. The curves reveal a forward recovery duration of approximately 1 μs, which minimally contributes to power losses at 150 kHz, as shown in Fig. 10(a). However, at higher frequencies, this forward recovery period becomes increasingly significant as its duration approaches the entire conduction subinterval, as shown in Fig. 10(b). It is important to highlight that power losses in the rectifying diodes constitute a dominant portion of the overall system losses, accounting for more than 75% of total power dissipation at $f_S = 150$ kHz, as shown in Fig. 11, while power losses on isolating capacitors remain negligible. As expected, at higher frequencies, switching-related losses become more prominent, leading to the efficiency reduction observed in Fig. 9(b) and (c). Thereby, the operating voltage range was restricted to 300 V to maintain a safe operating area and avoiding to exceed the power dissipation capability of the heatsink and the thermal resistance requirement on the output rectifying diodes.

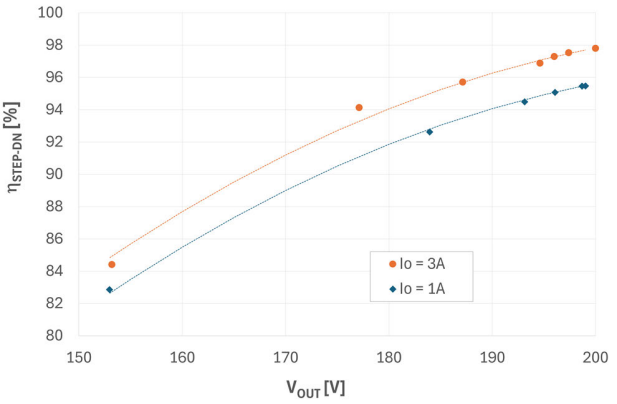

Fig. 12. Converter efficiency in the step-down mode (V_{IN} = 200 V, f_S = 150 kHz, and V_{OUT} varaible with φ).

It is worth to notice that, in transformer-based full-bridge topologies, in similar load conditions, copper and core losses can reach 10% of the output power [9], [10]. Moreover, designing a transformer capable of handling 6 kW of power at higher frequencies, such as 500 kHz, can be quite challenging.

C. Step-Down Operation

In Fig. 12, the converter was characterized in step-down mode with a constant input voltage of 200 V and constant current load conditions of 1 and 3 A.

As the phase shift (φ) increases, both the output voltage and the duration of the conduction subinterval decrease, while the current ripple in the circuit increases, as described by (1) and (3). As the conduction subinterval shortens due to the increasing value of ϕ, the rectifying diodes' forward recovery time contributes more significantly to power losses, as it occupies a growing portion of the conduction subinterval. Consequently, a decrease in efficiency is observed at lower output voltages, making circuit measurements challenging due to the increased power dissipation that must be managed on the rectifying diodes, as shown in Fig. 11. Therefore, although the step-down principle was demonstrated in Figs. 6 and 8 in alignment with the analytical modeling, the use of a passive rectifying diode bridge limits step-down operation to a narrow voltage control range. As a result, measurements were carried out only within a restricted voltage and power load range. To extend the control voltage and power range in step-down operation while maintaining high conversion efficiency, a full active bridge should be implemented. This approach would effectively minimize the otherwise significant impact of diode forward recovery and enable a highly efficient, capacitive-isolated bidirectional converter.

IV. Conclusion

This article introduced a capacitively isolated converter based on a full-bridge topology. A key advantage of this topology is the flexibility to achieve both 1:1 and step-down conversion modes via phase shift control. The use of capacitors for isolation allowed for reduced power losses and enabled operation at higher switching frequencies. Additionally, this topology eliminates any imposed dc offset across the isolating capacitors, avoiding any imposed voltage lift between input and output grounds while reducing voltage stress on the isolating capacitors. A comprehensive analytical model was developed to describe the converter's operation in both CCM and DCM. To validate the model, a prototype was built and experimentally tested up to 6 kW. The experimental results confirmed the accuracy of the analytical model and exhibited a peak conversion efficiency exceeding 98%. The rectifying diodes were identified as a major source of losses, while the isolating capacitors exhibited negligible losses. This work underscores the potential of capacitively isolated converters as a viable and highly efficient solution for relatively higher power applications. Future work may explore the use of active rectification techniques to further enhance conversion efficiency.

References

[1] M. Burunkaya and O. F. Demirkol, "Increase in the use of electric vehicles and its potential effects on electricity distribution network and situation analysis for Turkey," in *Proc. 6th Int. Conf. Electr. Electron. Eng. (ICEEE)*, Istanbul, Turkey, Apr. 2019, pp. 33–37, doi: 10.1109/ICEEE2019.2019.00014.

[2] P. Kadav and Z. D. Asher, "Improving the range of electric vehicles," in *Proc. Electr. Vehicles Int. Conf. (EV)*, Bucharest, Romania, Oct. 2019, pp. 1–5, doi: 10.1109/EV.2019.8892929.

[3] L. Dickerman and J. Harrison, "A new car, a new grid," *IEEE Power Energy Mag.*, vol. 8, no. 2, pp. 55–61, Mar. 2010, doi: 10.1109/MPE.2009.935553.

[4] A. Meintz et al., "Enabling fast charging—Vehicle considerations," *J. Power Sources*, vol. 367, pp. 216–227, Nov. 2017, doi: 10.1016/j.jpowsour.2017.07.093.

[5] V. M. Iyer, S. Gulur, G. Gohil, and S. Bhattacharya, "Extreme fast charging station architecture for electric vehicles with partial power processing," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018, pp. 659–665, doi: 10.1109/APEC.2018.8341082.

[6] T. Kanstad, M. B. Lillholm, and Z. Zhang, "Highly efficient EV battery charger using fractional charging concept with SiC devices," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Anaheim, CA, USA, Mar. 2019, pp. 1601–1608, doi: 10.1109/APEC.2019.8722191.

[7] P. Granello, T. B. Soeiro, N. H. van der Blij, and P. Bauer, "Revisiting the partial power processing concept: Case study of a 5-kW 99.11% efficient flyback converter-based battery charger," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 3, pp. 3934–3945, Sep. 2022, doi: 10.1109/TTE.2022.3170286.

[8] S. Rivera, S. Kouro, S. Vazquez, S. M. Goetz, R. Lizana, and E. Romero-Cadaval, "Electric vehicle charging infrastructure: From grid to battery," *IEEE Ind. Electron. Mag.*, vol. 15, no. 2, pp. 37–51, Jun. 2021, doi: 10.1109/MIE.2020.3039039.

[9] S.-W. Jeong, S.-H. Lee, D.-H. Kwon, J.-Y. Kim, and J.-K. Kim, "Two-transformer phase-shift full-bridge converter with a new rectifier for reducing conduction loss," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15634–15644, Dec. 2023, doi: 10.1109/tpel.2023.3303917.

[10] H. M. Maheri, D. Vinnikov, A. Chub, and V. Sidorov, "Power loss model and efficiency analysis of the quasi-Z-source isolated buck-boost converter with wide input voltage and load range," in *Proc. IEEE 61th Int. Sci. Conf. Power Electr. Eng. Riga Tech. Univ. (RTUCON)*, Riga, Latvia, Nov. 2020, pp. 1–8, doi: 10.1109/RTUCON51174.2020.9316587.

[11] B. Van Tassell et al., "Metacapacitors: Printed thin film, flexible capacitors for power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2695–2708, Apr. 2016, doi: 10.1109/TPEL.2015.2448529.

[12] J. L. Hudgins, "Power electronic devices in the future," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 1, pp. 11–17, Mar. 2013, doi: 10.1109/JESTPE.2013.2260594.

[13] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013, doi: 10.1109/TPEL.2012.2192503.

[14] P. Granello, F. Pellitteri, R. Miceli, and L. Schirone, "Highly efficient capacitive galvanic isolation for EV charging stations," in *Proc. Int. Symp. Power Electron., Electr. Drives, Autom. Motion (SPEEDAM)*, Sorrento, Italy, Jun. 2022, pp. 389–394, doi: 10.1109/SPEEDAM53979.2022.9842217.

[15] F. Pellitteri, N. Campagna, P. Granello, R. Miceli, and L. Schirone, "Automotive battery charging based on efficient capacitive power transfer," in *Proc. Int. Conf. Clean Electr. Power (ICCEP)*, Terrasini, Italy, Jun. 2023, pp. 464–468, doi: 10.1109/ICCEP57914.2023.10247406.

[16] D. Shmilovitz, A. Abramovitz, and I. Reichman, "A family of bridgeless quasi-resonant LED drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1833–1836, Mar. 2016, doi: 10.1109/TPEL.2015.2470600.

[17] J. Zhu, M. Xu, J. Sun, and C. Wang, "Novel capacitor-isolated power converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Atlanta, GA, USA, Sep. 2010, pp. 1824–1829, doi: 10.1109/ECCE.2010.5618141.

[18] G. Barbehenn and S. B. Elgee, "SEPIC converter with transformerless line isolation," U.S. Patent 005 583 421 A, Dec. 10, 1996.

[19] S. Bäurle, D. M. H. Matthews, and R. S. Saint-Pierre, "Transformerless safety isolation in a power supply using safety capacitors for galvanic isolation," U.S. Patent 7 453 710 B2, Nov. 18, 2008.

[20] D. Shmilovitz, S. Ozeri, and M. M. Ehsani, "A resonant LED driver with capacitive power transfer," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Fort Worth, TX, USA, Mar. 2014, pp. 1384–1387, doi: 10.1109/APEC.2014.6803487.

[21] G.-H. Wang, "Capacitor insulating power supply," U.S. Patent 20 070 120 541 A1, May 31, 2007.

[22] J. Zhang, J. Wang, and X. Wu, "A capacitor-isolated LED driver with inherent current balance capability," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1708–1716, Apr. 2012, doi: 10.1109/TIE.2011.2138111.

[23] Y. Hayashi, Y. Matsugaki, and T. Ninomiya, "Capacitively isolated multicell DC–DC transformer for future DC distribution system," *IEEJ J. Ind. Appl.*, vol. 6, no. 4, pp. 268–277, Jul. 2017, doi: 10.1541/ieejjia.6.268.

[24] M. Kline, I. Izyumin, B. Boser, and S. Sanders, "A transformerless galvanically isolated switched capacitor LED driver," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, Feb. 2012, pp. 2357–2360, doi: 10.1109/APEC.2012.6166152.

[25] J. Xu, L. Gu, and J. Rivas-Davila, "Effect of class 2 ceramic capacitor variations on switched-capacitor and resonant switched-capacitor converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2268–2275, Sep. 2020, doi: 10.1109/JESTPE.2019.2951807.

[26] P. Suskis, J. Zakis, A. Suzdalenko, H. Van Khang, and R. Pomarnacki, "A study on electrolytic capacitor aging in power converters and parameter change over the lifespan," in *Proc. IEEE 10th Jubilee Workshop Adv. Inf., Electron. Electr. Eng. (AIEEE)*, Vilnius, Lithuania, Apr. 2023, pp. 1–5, doi: 10.1109/AIEEE58915.2023.10135053.

[27] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 344–354, Feb. 2011, doi: 10.1109/TPEL.2010.2062537.

[28] *TDK Corporation, Multilayer Ceramic Chip Capacitors, Characteristic Graphs*. Accessed: Oct. 2024. [Online]. Available: https://product.tdk.com/en/search/capacitor/ceramic/mlcc

Pierpaolo Granello (Student Member, IEEE) was born in Rome, Italy, in 1993. He received the master's degree in electronics engineering from Sapienza University of Rome, Rome, in 2020. He is currently pursuing the Ph.D. degree in electrical engineering with the Department of DC Systems, Energy Conversion and Storage, Delft University of Technology, The Netherlands, and with the Department of Astronautical, Electrical and Energetic Engineering of Sapienza, University of Rome.

During his master's degree which he had a research fellowship for aerospace power electronics. His main research focus is on highly efficient power processing power electronics for grid-tied and aerospace applications. His research interests also include power electronics for Battery Energy Storage Systems, Electric Vehicles and DC distribution grids.

Luigi Schirone (Member, IEEE) received the master's degree (Hons.) in electronic engineering from the University of Rome, Rome, Italy, in 1983.

Since 1988, he has been with the University of Rome, where he is currently a Professor of Electronics at the School of Aerospace Engineering. His research interests are in electronics for power and energy systems, with a primary focus on power conversion systems. He aims to develop new design approaches to enhance efficiency, reliability, and/or power density. In aerospace applications, he holds a patent and has developed onboard power modules for spacecraft, planetary rovers, and aircraft. His other projects span automotive, renewable energy, and sustainability, including wireless power transmission, photovoltaic systems, smart power sources, and energy harvesting. Additionally, he is involved in research on materials technology for electronic devices. He has authored or co-authored over 150 scientific publications.

Pavol Bauer (Senior Member, IEEE) received the master's degree in electrical engineering from the Technical University of Kosice, Kosice, Slovakia, in 1985, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 1995.

He is currently a Full Professor with the Department of Electrical Sustainable Energy, Delft University of Technology, where he is the Head of DC Systems, Energy Conversion and Storage Group. He has authored or co-authored 72 journals and almost 300 conference papers (with H factor Google scholar 43, Web of Science 20) and eight books, and holds four international patents. He has organized several tutorials at the international conferences. He has worked on many projects for industry concerning wind and wave energy, power electronic applications for power systems such as Smarttrafo; HVdc systems, projects for smart cities such as PV charging of electric vehicles, PV and storage integration, contactless charging; and he has participated in several Leonardo da Vinci and H2020 EU projects as project partner (ELINA, INETELE, E-Pragmatic) and coordinator (PEMCWebLab.com-Edipe, SustEner, Eranet DCMICRO).

Dr. Bauer was a recipient of the title Prof. from the President of Czech Republic at the Brno University of Technology in 2008 and Delft University of Technology in 2016.