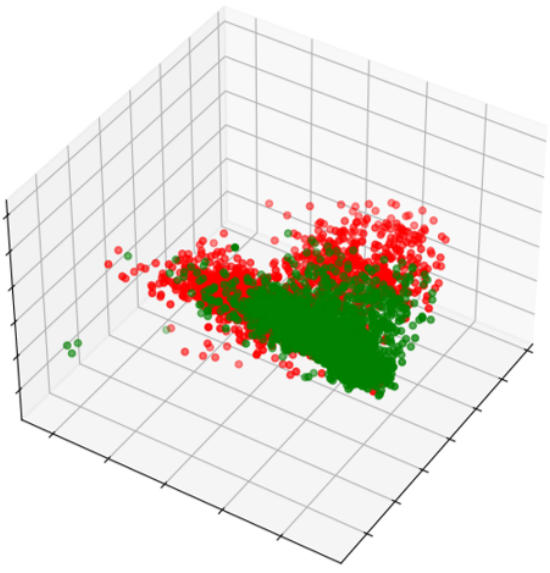
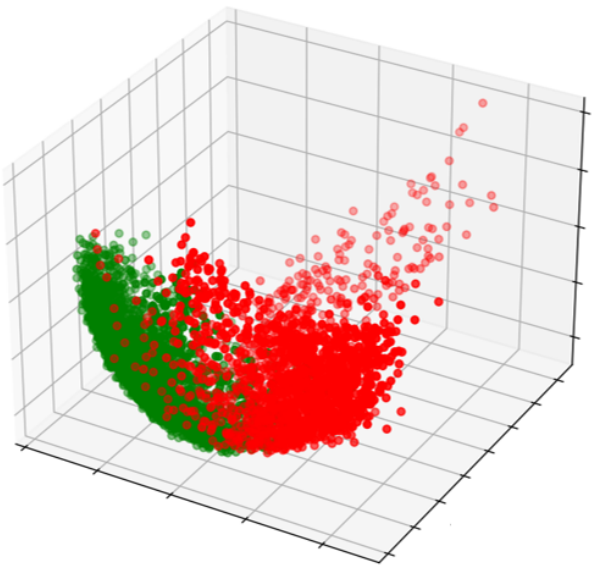
Automatic defect identification during RRAM characterization

Mathijs Heidekamp





TU Delft

Automatic defect identification during RRAM characterization

by

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Abstract

Resistive random access memory (RRAM) is an emerging memory technology that has the potential to replace dynamic random access memory (DRAM) or FLASH. The current memory technology suffer from scalability issues. SRAM consumes a lot of area as it requires 6 transistors for a single cell. DRAM stores data using a capacitor which needs to be refreshed periodically. The scalability of DRAM becomes more challenging as the sensing margin becomes smaller and the capacitor needs to be refreshed more frequently increasing the dynamic power consumption. To overcome these challenges new structures, materials and or processes have to be developed which will increase the complexity and cost of DRAM. Flash is volatile memory but has a high operating voltage and relative low endurance. RRAM can be used as potential replacement for Flash and DRAM. RRAM stores information using resistance states instead of charge. RRAM is non-volatile memory, power efficient, scalable and compatible with the current CMOS process.

Before RRAM can be commercialized the quality of RRAM devices needs to be guaranteed. For this we need to be able to diagnose RRAM devices. The diagnosis will allow us to improve the manufacturing process as well as built defect models for memory testing. Traditional fault models use linear resistors to model the manufacturing defects. These fault models do not incorporate the non-linear behaviour of the RRAM device. As a result, tests are created for the wrong test space resulting in a lower yield and more test escapes. To increase the yield and create more reliable fault models, defect models that incorporate the physical defect of the RRAM device are required. To ensure the manufacturing quality of the RRAM devices and for memory testing of RRAM the characterization and diagnosis of RRAM is required. The electrical characterization of RRAM is cheap, fast and is used to evaluate the performance of RRAM. However, none has used electrical characterization for diagnosis to identify defective RRAM devices.

The contribution of this work is to provide the electrical characterization of RRAM to automatically identify defective RRAM devices which can be used for diagnosis. For the first time this is attempted using the electrical characterization of RRAM. For the defect identification, the key electrical parameters are determined. To assess the performance of the defect identification algorithms a method to manually label RRAM devices is proposed. In total five methods have been implemented and evaluated to automatically label defective RRAM devices. A statistical analysis is performed on the key parameters of RRAM. Using the labelled data the devices are compared to a nominal device to identify defects in RRAM. Furthermore, one unsupervised and two supervised learning algorithms have been implemented. K-means, K-NN and a CNN is applied to RRAM devices. The classification algorithms allow the automatic identification of defective RRAM devices which can be used for diagnosis and will contribute to designing defect models that incorporate the non-linear behaviour of the RRAM device. The metrics used for the statistical analysis are insufficient to accurately identify defective RRAM devices. The nominal device method classifies 81% of the device correctly using the euclidean algorithm. The best performance is obtained for the supervised learning algorithm. K-NN classifies 94% of the cycles correct and 84% of the devices. If the data is not labelled the unsupervised learning algorithm can be used. Kmeans classifies 79.6% of the devices correctly which is slightly worse than K-NN. The CNN classifies 67% of the devices correctly using 20 epochs. However, the CNN has not yet been optimized and needs to be improved. For unlabelled data, the unsupervised learning algorithm should be used and for labelled data the K-NN. The electrical characterization of RRAM devices using machine learning looks promising and is much cheaper compared to optical characterization and memory tests. If in the future the defective devices can be linked to the underlying defect, this will lead to cheaper diagnosis of RRAM devices and allow the creation of accurate fault models.

Preface

After a lot of hard work I have been able to complete this thesis. It has not been easy as a lot of implementations and suggestions did not work at first. The goal was to determine which RRAM devices are defective and why but only the first part of this question has been answered. The manual labelling of the RRAM devices required a lot of additional background knowledge and consumed a lot of time. The assumption was that the RRAM characterization using statistics would allow us to identify defects in RRAM devices. However, it turned out that this did not seem possible and we had to switch to machine learning. The additional reading and background information took additional time which is why we have not been able to answer why the devices are defective.

I would like to thank Moritz Fieback for all the support and guidance. I worked a lot from home and the weekly meetings kept me on track and helped me to stay motivated when my suggestions did not work. Additionally, I want to thank my thesis supervisor Said Hamdioui, who provided critical feedback and support during the DfX meetings. I learned a lot from those meetings and would like to thank the members for their suggestions and critical questions during those meetings. I also want to thank Hanzhi Xun for all his help and Hassen Aziza for sharing the measurement data. I would like thank the department for sharing their vocal talents with me during the karoake nights.

I would like to conclude by thanking my mother, brother and girlfriend. Throughout my entire study, but especially during this thesis they have supported me unconditionally!

Mathijs Heidekamp
Delft, November 2023

Contents

1 Introduction

1.1. Motivation

Reducing the dimensions of current memory technologies below the 10 nm threshold is becoming more difficult due to increased leakage power and structural challenges [1, 2, 3, 4, 5]. Dynamic Random-Access Memory (DRAM) is volatile memory and requires a steady power supply to store information [1, 2, 3]. DRAM stores data using a capacitor that needs to be refreshed periodically. As the dimensions of DRAM are scaled down the capacitance decreases which affects the sensing margin and retention of the device and DRAM cells will need to be refreshed more frequently increasing the dynamic power consumption [1, 3]. To reduce the static and dynamic power consumption new structures, materials and or processes have to be developed which will increase the complexity and cost of DRAM. Additionally, as the dimensions of DRAM are reduced, the leakage power becomes more significant than the dynamic power consumption [1, 2]. Static Random-Access Memory (SRAM) is much faster than DRAM but is also volatile memory and requires 6 transistors to store information making large scale integration costly and infeasible [2, 6]. FLASH is non-volatile memory. However, the endurance is low, operation voltage (10 V) and write speed (1 ms) are high compared to DRAM and SRAM [2, 7]. Additionally, the leakage current is a problem for low power embedded systems. To overcome the scalability challenges and the leakage current alternative materials or memory systems are required [1, 2, 3, 8].

Three promising memory technologies have been developed to overcome these challenges.The emerging memory technologies are phase-change random access memory (PCRAM), spin-transfer torque magnetic random access memory (STT-MRAM) and resistive random access memory (RRAM). The emerging memory technologies are scalable, the read and write speed are better than FLASH memory. Additionally, the emerging memories are non-volatile. However, the focus of this work will be on RRAM. The cell density of STT-MRAM is larger compared to RRAM, the write time of RRAM is faster than of PCRAM and RRAM can be manufactured using the existing CMOS technology. [7].

RRAM is compatible with the CMOS fabrication process and the memory density is high. RRAM is scalable and has zero standby power consumption making it ideal for low power systems [9]. RRAM is not as fast as SRAM so it is unlikely to replace SRAM. However, RRAM can easily be scaled below $1xnm$ and does not have the scalability issues DRAM is facing [7, 10, 11, 12]. Due to the low leakage current and non-volatile memory RRAM be a good alternative for DRAM. Additionally, RRAM is non-volatile memory and the operation speed of RRAM is much higher than FLASH. The operating voltage is 1 V and operation speed (10 ns) which outperforms the operation voltage and write speed of FLASH [2, 7]. Therefore, RRAM is a good alternative to replace FLASH and DRAM to overcome the leakage power and scalability issues of current memory technologies.

Before RRAM can be commercialized we need high quality tests that can identify defects in RRAM devices. A defect is an unintended variation in the design. Defects are modelled using fault models. A fault model in an abstraction of a defect that describes the faulty behaviour at the electrical level [13]. . Current test methods use fault models that mimic physical defects using linear resistors [14, 15, 16, 17]. These models do not properly mimic the non-linear behaviour of RRAM and do not catch the unique faults that occur in RRAM leading to test escapes [14, 18]. The unique faults that are Hard-to-Detect occur occasionally or only result in parametric variations affecting the long-term reliability of the device

[9]. In order to commercialize RRAM devices the unique faults that can occur need to be identified and understood so that accurate fault models can be built and new test methods can be designed. To be able to build accurate fault models the manufacturing defects need to be identified and linked to the behaviour of the device. The manufacturing defects and the effect on the switching characteristics have already been investigated by Fieback, Taouil, and Hamdioui [14]. So far we have only attempted to identify the defects using fault models which are an abstraction of the defect and cannot be linked back to the actual defect. Diagnosis of RRAM devices is required to determine the cause of the defective behaviour.

1.2. State of the art

Defect characterization of RRAM devices is necessary to develop accurate fault models capable of detecting unique defects in RRAM. To identify the process variations and manufacturing defects the electrical parameters of the device need to be determined and the effect of the manufacturing defects on the electrical parameters needs to be studied [14]. Fieback, Taouil, and Hamdioui have already identified the defects that can occur during the manufacturing process and proposed the key parameters that should be used for characterization [14]. Lanza et al. proposed similar parameters together with a method to extract these parameters from measurement data and the figure of merits that should be used for visualization. The electrical parameters describe the switching behaviour of the device [19]. While there is no discussion about the electrical parameters, the method to extract and analyse these parameters is unclear. Lanza et al. does propose the figure of merits for each of the electrical parameter [19]. The figure of merits give information about the standard deviation, average and distribution of the RRAM cells. However, they do not mention how a healthy device behaves and how defects affects these parameters. The effect of the manufacturing defects on the parameters is difficult to assess due to the cycle-to-cycle and device-to-device variability. Poehls et al. do mention the physical defects that can occur during the manufacturing process [9]. But how exactly this affects the parameters or how the defects can be identified is unclear. The random misbehaviour in some cycles makes defect identification and fault diagnosis difficult as there is no baseline that mentions the minimum number of switching cycles that need to be analyzed to assess the performance of the device and whether the behaviour is due to the variability of the device or is caused by a defect. Additionally, the visual inspection of individual cycles is time-consuming and subjective, and there is no guarantee that the parameters can be used to identify defective behaviour. As a result, a reliable method is required that automatically extracts the key features of a RRAM cell and classifies the device.

The characterization of RRAM devices can be split into three categories. Electrical characterization, memory testing and optical characterization. Electrical characterization characterizes RRAM using electrical measurements from RRAM cells. Memory testing attempts to identify defective behaviour in RRAM using fault models and optical characterization characterizes the device using optical measurements.

Electrical characterization is much cheaper than optical characterization. In literature, there are two main methods for the electrical characterization of RRAM. Voltage sweeps (I-V sweeps) where the current of the device is measured while the voltage is gradually increased and pulsed voltage stress (PVS) in which short voltage pulses are applied to the device to make the device switch between states [2, 19]. Zahoor, Zulkifli, and Khanday has used I-V sweeps to study the impact on device dimensions [2]. Fantini et al. analysed the impact of oxide thickness on the switching characteristics by applying PVS [20]. Grossi et al. studied the effect of grain boundaries in polycrystalline and amorphous HfO_2 [21]. While these give information about how the physical properties of RRAM affects the device behaviour they do not discuss how unwanted parametric deviations in the physical design can be identified. The identification of these defects using electrical tests is cost effective, fast and will result in more accurate fault models leading to fewer test escapes.

Memory testing is cheaper than the electrical characterization, but more abstract compared to the electrical tests. Memory tests use fault models. A fault is an abstraction of a defect that describes the faulty behaviour at the electrical level. In literature a distinction between conventional and unique faults is made. Conventional faults are faults that can also be observed in mainstream memories and unique faults are new emerging faults caused by the analog characteristics of RRAM. March tests have been proposed by many. However, none are able to identify the unique faults in RRAM devices as the fault models are inaccurate leading to test escapes. Tests do not accurate catch the faults in RRAM devices

and are not linked to the unique defects [22, 23, 24]. Chen et al. and Liu et al. proposed a march test to identify unique faults in RRAM. In [22], read disturb faults in RRAM are identified, but the link to the physical defect is missing. In [23] they were able to identify faulty cells, but the root-cause of the fault is lacking. Kannan, Karri, and Sinanoglu uses sneak-paths to identify defects in RRAM but the effect of the defects on the parameters is not discussed. The problem is that the fault models do not incorporate the analog characteristics of RRAM. Fieback et al. proposes the device-aware-test which instead of the linear defect model by modelling the defective behaviour of the defect. However, to built a physical defect model we first have to identify which RRAM devices show abnormal behaviour and what defect causes the abnormal behaviour.

Optical characterization is the most expensive. For the optical characterization transmission electron microscopy (TEM), atomic force microscopy (AFM) and scanning electron microscopy (SEM) is used. The optical characterization has been used to study the switching of RRAM in situ as well as the effect of defects[26, 27, 28, 29]. Pey et al. studied the effect of the compliance current on the switching of RRAM cells using in-situ TEM. Nandi et al., Charpin-Nicolle et al. used AFM to measure the electrode roughness of RRAM cells. In [32] CAFM is used in-situ to study the effect of grain boundaries. Optical characterization visualizes the physical defect. However, the dimensions of the device affect the switching behaviour of RRAM. For TEM a thin cross-section is required for the examination of RRAM devices. As a result, the switching behaviour of the device is not comparable to that of typical devices the dimensions of the device are not representable. Furthermore, the number of cycles that can be characterized is limited and due to the high current density the number of cycles that can be characterized is limited and in some cases destroys the device [19].

Visualizing the defect using optical characterization is expensive, time consuming and cannot be used at array-level. The memory tests use faults to identify defective behaviour. As the faults are an abstraction of the actual defect it is good to use for identifying faulty devices, but cannot be used for diagnosis as the physical defect cannot be retrieved. Electrical characterization is cheap as we only require measure data. So far the electrical characterization has only been applied to study the impact of device dimensions and has not yet been used for the characterization and diagnosis RRAM.

1.3. Contribution of the work

This master thesis focuses on the automatic defect characterization of RRAM devices using the key parameters proposed by Lanza et al. and Fieback et al. to identify functional and defective RRAM devices [15, 19]. The electrical parameters describe the switching characteristics of RRAM. The methods to extract the electrical parameters will be evaluated and compared. A statistical analysis will be done on the electrical parameters of 49 devices and 936 cycles to assess the performance of the device. The statistical analysis will give insight in the distribution and behaviour of the different devices, which will be used to classify healthy and defective devices. Besides the statistical analysis, three machine learning techniques are used and applied to the IV measurements and the electrical parameters. To assess the performance of these methods, the devices are manually labelled for comparison. The method to do this is presented as well. This thesis presents a method to identify defects in RRAM devices using statistical and machine learning methods. To summarize the main contributions.

1. Identification of the key electrical parameters of RRAM devices
2. Comparison between different methods to extract the electrical parameters from RRAM devices
3. Extensive statistical analysis of the electrical parameters to characterize RRAM devices.
4. Framework to manually label RRAM devices which can be used to evaluate the performance of classification algorithms.
5. Implementation of one unsupervised and two supervised machine learning algorithms that can identify defective RRAM devices.
6. Software to automatically extracts the electrical parameters and identify defective RRAM devices.
7. Contribution to a paper that is to be presented at the Asian Test conference 2023. The software provided in this work aided in the analysis of the data. H. Xun et al. ”*Characterization and Test of Intermittent Over RESET in RRAMs*”. In: ATS conference 2023.

1.4. Outline

Chapter 2 provides an comparison of the state-of-the-art memory and emerging memory technologies. Furthermore, background information on RRAM is provided including the steps required to manufacture RRAM devices and the defects that can occur in the process. Chapter 3 presents the state-of-the-art in characterization and diagnosis in the microelectronics field and what is missing. Chapter 4 describes the measurement data, the method to extract the electrical parameters, the method to label RRAM devices and provides an initial characterization of the RRAM devices using statistics. Chapter 5 provides the algorithms that are used to classify the different RRAM devices. Three different methods are described. The statistical method, one unsupervised learning methods and two supervised learning algorithm. Chapter 6 shows the results of the different algorithms. Chapter 8 evaluates the results and provides a summary of the results and evaluates the performance of the algorithms. Chapter 7 evaluates the reliability of the work. What is the contribution to the scientific community, are the results reliable and what should be the next step.

2

Background

2.1. Overview

This chapter provides the background in memory and RRAM to understand the importance of RRAM characterization and defect identification. The first part explains the memory hierarchy, the fundamentals of the different memory types and provides a comparison between the different memory types in terms of performance and cost. The second part of the chapter focuses on the background information of RRAM. The hardware layout, the electrical and technological parameters and the basic principles of RRAM. The chapter will end with the fabrication process and the corresponding manufacturing defects in RRAM.

2.2. Memory background

2.2.1. Overview

The performance gap describes the increasing difference in processing speed and latency between the CPU and memory system [33]. The performance gap between CPUs and memory is growing at a rate of 50% per year [33]. The performance gains of CPUs and memory over the past three decades are illustrated in Figure 2.1 [33, 34]. Figure 2.1shows the increasing performance gap between memory and CPU indicating the recent developments of the CPU and memory. From 1990-2000 the lower level caches are introduced to reduce latency. Then multi-cores where developed which allowed the execution of multiple instructions in parallel. Each core was introduced with lower L1 and L2 cache and the L3 cache is introduced that is shared by the multiple cores. As the number of cores grew the L3 cache was distributed over the individual cores. The last development for the CPU to improve the performance are XPUs. An XPU is an additional unit that works together with a CPU. It is dedicated hardware designed for a specific task which can execute that task faster than a CPU [33]. Furthermore for Memory DDIO (Data Direct Input Output) was designed for networking. It allows direct placement of the data in the processor cache without having to place it first in memory. After which the quality of service (QoS) for cache was implemented to reduce resource contention between the different cores. The memory wall is a manifestation of the performance gap and implies the effects of teh growing performance gap between the CPU and memory. To adress the memory wall and minimize latency the memory hierarchy was introduced incorporating different types of memory [33].

2.2.2. Memory hierarchy

The memory hierarchy integrates different types of memory to reduce latency and increase bandwidth [33, 34, 35, 36]. Memory types are organized based on their size, cost, and access speed. The farther the memory is from the processor, the slower it becomes, but in return offers a larger storage capacity. Conversely, memory located close to or directly on the CPU is faster but has limited storage space.

The memory hierarchy shown in Figure 2.2 consists of several levels: registers, cache, main memory, flash, secondary storage and remote storage [37]. The figure shows the growing performance gap between CPUs and memory from 1990 up til 2020 and the attempts to reduce the performance gap. The development of the CPU went from single thread to multi-threading to the use of accelerators in-

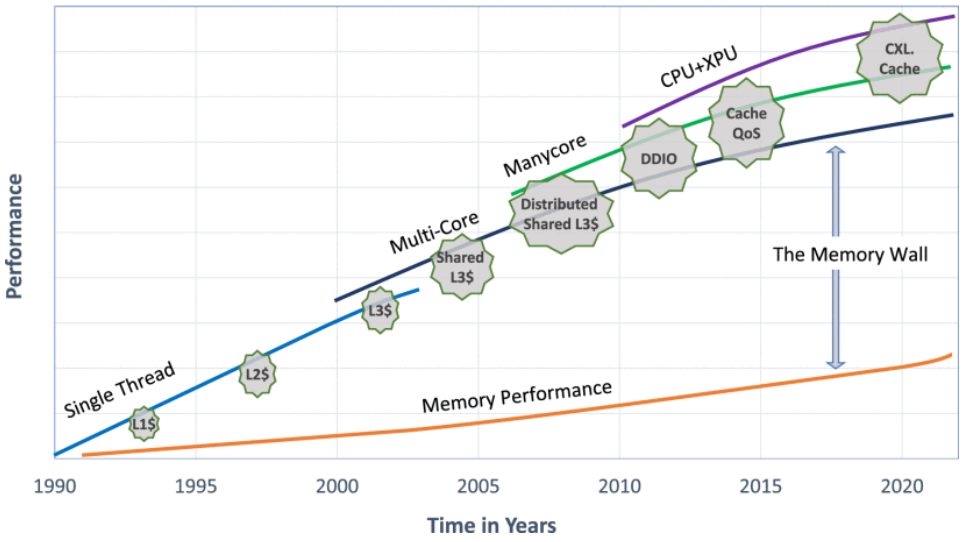

Figure 2.1: Yearly improvement of processor and DRAM memory speeds, for a time period of three decades obtained from [34]

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creasing the performance gap between memory and the CPU further. To overcome this cache memory is introduced that is placed closer to the CPU. Initially a single thread CPU was used with off-die level 1 cache consisting of a couple hundred of Kilobytes. Over time the lower levels cache moved on chip and can now store more than 100 MB [34]. The components of the memory hierarchy are:

1. Registers are located on the CPU and are the fastest memory type. The storage capacity is typically a few of bytes. Registers are built using flip-flops which require continuous power to maintain their state [36]. Due to the limited space on the CPU, expanding the register size is not feasible. Increasing the size would require more interconnects, resulting in a higher power consumption cost and circuit complexity. This would contradict the objective of having a low power, high performance device.

2. Cache memory is situated close to or directly on the CPU chip and can store more data than registers. Cache memory serves as a bridge between the CPU and main memory, holding frequently accessed instructions and data. Cache memory is typically constructed using Static Random Access Memory (SRAM) and is volatile memory. The memory size can vary between several kilobytes up to a few of megabytes. Data required by the CPU is copied in chunks from secondary storage to cache, assuming that the data is spatially distributed [36, 38].

3. Main Memory is larger than cache memory and is built using the same type of memory. However, it differs in terms of capacity and speed. As a result, main memory is not integrated onto the CPU, with the exception of embedded systems, but is housed in a separate module. Main memory predominantly holds the programs executed by the system, while cache memory stores data frequently used by the CPU. Dynamic Random Access Memory (DRAM) is commonly used for main memory [36, 39].

4. Flash Disk is a type of non-volatile memory designed for data storage. Non-volatile memory refers to memory that can retain stored data even when the power is disconnected. Unlike volatile memory, such as SRAM and DRAM, which loses data when the power supply is interrupted, non-volatile memory retains information over long periods. Flash memory, which falls into the non-volatile memory category, offers slower access times compared to cache memory and is placed further away from the CPU. It is commonly utilized in embedded systems such as cameras, smartphones, and USB drives. Flash memory is re-programmable, allowing for data to be written and erased multiple times. This characteristic, combined with its ability to retain data without a power source, makes flash memory a popular choice for applications requiring persistent storage [7, 40].

5. Secondary storage refers to the main hard drive used to store data that is not immediately required by the CPU. It can accommodate large amounts of data but is extremely slow [41].

6. Remote storage is not part of the local memory hierarchy and can be accessed through a network. This is the slowest type of memory within the memory hierarchy. The advantage is that the data can easily be accessed by multiple users, which makes it ideal for data storage, backup and cloud computing.

Overall, the memory hierarchy optimizes the balance between storage capacity and access speed, placing faster and smaller memory types closer to the CPU and utilizing slower but larger storage further away.

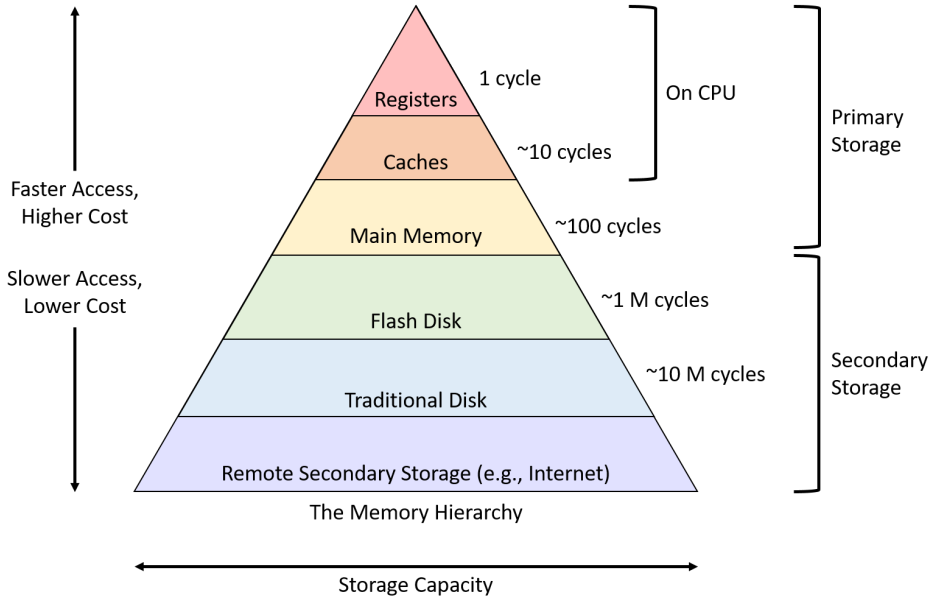


Figure 2.2: The memory hierarchy [37]

2.2.3. Types of memory

subsection 2.2.2 introduced the memory hierarchy. This section provides an overview of the memory types used in the memory hierarchy. SRAM, DRAM, flash, and magnetic storage are discussed to offer a more comprehensive understanding of their characteristics. The hardware layout, advantages, disadvantages, and limitations associated with each memory type are discussed.

SRAM

SRAM is faster compared to DRAM at the expense of area and cost. A typical SRAM cell is given in Figure 2.3a. A typical SRAM cell consists of six transistors. Two are used for the selection of the word and bit line and the other four transistors are cross-coupled inverters that store the state of the device [2, 6]. The additional transistors make large-scale integration costly and infeasible [2, 6]. Table 2.1 shows the device characteristics which shows that the read and write time is 10 times better compared to DRAM but that the area required is much larger with a cell area of $100F^2$ compared to $6F^2$ where F is the feature size of the lithography method used. Due to the performance, SRAM is used in cache memory which is placed close to the CPU [2, 7].

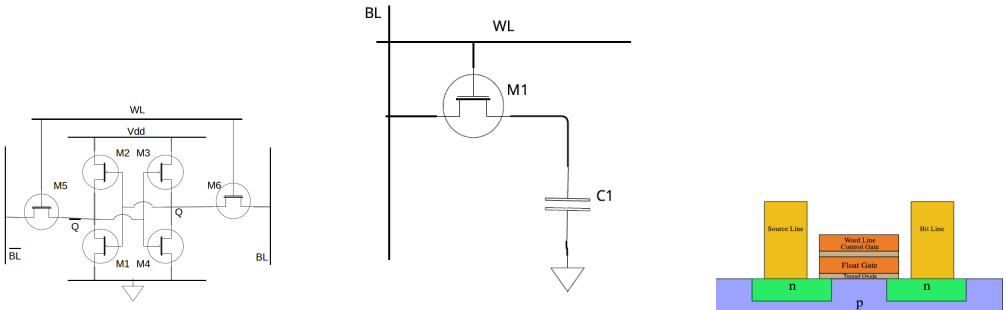
DRAM

DRAM is volatile memory. DRAM offers greater area efficiency as it only requires a single transistor and capacitor to store information [1, 2, 3]. Figure 2.3b shows the DRAM circuit. A charged capacitor represents a logical '1' and an uncharged capacitor represents a logical '0'. The capacitor leaks

charge over time. As a result, the DRAM cell needs constant refreshing to be able to distinguish a logical '1' from a logical '0'. The capacitance of the capacitor is determined by the plate dimensions and dielectric constant. However, scaling down DRAM cells presents challenges. The reduced size decreases the capacitance and makes the sensing margin smaller [1, 3]. Additionally, the dynamic power consumption increases because the capacitor needs to be refreshed more frequently to maintain its state. To further scale down DRAM devices, the development of new structures, materials, or processes becomes necessary. However, these advancements result in increased complexity and higher costs associated with DRAM production.

Flash

Flash uses floating gate transistors and utilizes the threshold voltage of transistor gates to store information. Figure 2.3c shows a flash memory cell. Flash memory is non-volatile memory that retains data even when the power is turned off. To write data to the cell, a high voltage is applied to the transistor gate, creating an electric field that allows electrons to flow through the oxide into the floating gate. To erase data a voltage is applied to the entire memory cell, causing the electrons to move back from the transistor gate to the source. As shown in Table 2.1, flash memory is considerably slower than DRAM and SRAM. However, its non-volatile characteristic makes it well-suited for long-term storage data in embedded devices and solid-state drives. Another limitation of flash is that the endurance is low compared to SRAM and DRAM and the write voltage is high [7, 40].



(a) Hardware layout of SRAM adapted from [42]

(b) Hardware layout of DRAM obtained from [43]

(c) Hardware layout of flash[44]

Figure 2.3: Hardware layout of SRAM, DRAM and flash [42, 43].

Emerging memory

SRAM has fast read and write speeds but is limited by its low density, high cost and volatile characteristics [2]. Scaling down DRAM below the $1xnm$ threshold is challenging and expensive, and also suffers from high leakage current as well as dynamic power consumption [45, 46]. Flash is non-volatile memory and cheap to implement but suffers from drawbacks such as high operating voltage, slow write and read speeds, and limited endurance. These limitations drive the need for new memory technologies that offer improved scalability, lower leakage current and reduced costs. The emerging memory technologies that show potential are phase-change random access memory (PCRAM), spin-transfer torque magnetic random access memory (STT-MRAM) and resistive random access memory (RRAM). These memory technologies are discussed in more detail in this section.

PCRAM

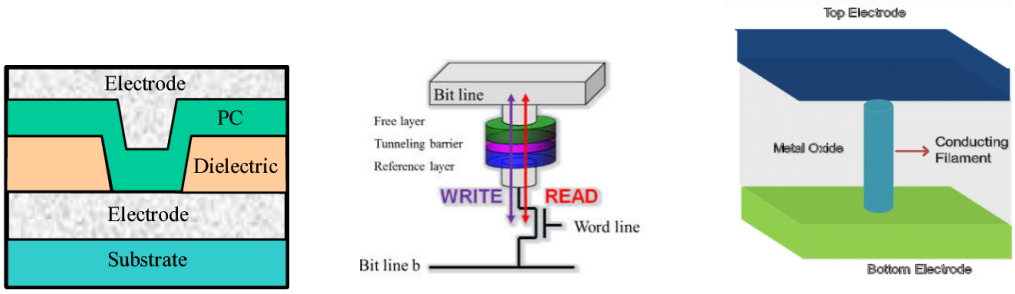
PCRAM consists of two electrodes, a dielectric isolator and a phase change material. The phase change material has the ability to switch between two phases: amorphous and crystalline [47, 48]. By applying a large electrical pulse to the device, the material heats up and switches from the crystalline to the amorphous state. By applying a longer medium current pulse the crystalline state is restored [48]. The resistance of the device changes depending on the state of the phase change material. PCRAM offers several advantages. The read time is comparable to DRAM while having non-volatile memory similar to flash. The operation voltage is lower with $3\,\mathrm{V}$ compared to the $10\,\mathrm{V}$ required for flash and as is shown in Table 2.1 the endurance is much better compared to flash memory.

STT-MRAM

STT-MRAM uses a magnetic tunnelling junction (MTJ) to store data. The MTJ consists of two ferromagnetic layers: the reference layer and free layer which are separated by a dielectric material [49]. The reference layer has a fixed magnetic direction, while the magnetic field of the free ferromagnetic layer can be altered by an external electromagnetic field. The value read or stored from the STT-MRAM cell depends on the relative orientation between the reference layer and the free layer. STT-MRAM is a non-volatile memory that retains data when there is no power. The operation voltage of $1.5\,\mathrm{V}$ is $0.5\,\mathrm{V}$ higher than SRAM and DRAM with comparable endurance, with an expected lifespan of more than 10^{16} write cycles as can be seen in Table 2.1. Making it a perfect candidate to replace flash.

RRAM

RRAM consists of a bottom, a top electrode, and an insulator in between. When a voltage is applied across the electrodes, a filament is formed within the insulator, connecting two electrodes. By applying a voltage of opposite polarity, the filament is broken down. The conducting filament (CF) allows current to flow, reducing the resistance over the electrodes. The resistance of the RRAM device varies based on the length of the CF to which a logical one or zero can be assigned [2, 7]. Compared to DRAM and flash, RRAM exhibits superior scalability below the $10\,\mathrm{nm}$ threshold as can be seen in Table 2.1. RRAM also has better endurance than flash, while occupying a smaller cell area. Moreover, RRAM demonstrates comparable read and write speeds to DRAM. Thanks to its non-volatile nature, RRAM can serve as a viable replacement for flash memory. Furthermore, in low power embedded systems where zero leakage current is desired, RRAM might even be used as a substitute for DRAM. However, new materials and additioanl manufacturing steps are required to fabricate RRAM. These manufacturing steps give rise to new faults for which specialized tests have to be developed.



(a) Hardware layout of PCRAM[47] (b) Hardware layout of STT-MRAM[50] (c) Hardware layout of RRAM. [2]

Figure 2.4: Hardware layout of PCRAM, STT-MRAM and RRAM

Summary

The device characteristics of different memory types are presented in Table 2.1. The emerging memory technologies, including RRAM, STT-MRAM, and PCRAM, demonstrate superior scalability and improved cell area compared to current state-of-the-art memory technologies. While SRAM remains the top performer in terms of performance, RRAM, STT-MRAM, and PCRAM offer potential as replacements for Flash memory and as competitors to DRAM due to their volatile nature. Currently, the emerging memory technologies are not yet used for large scale production. The emerging memory technologies require different manufacturing steps giving rise to new defects. To catch and identify these defects new tests have to be developed before these memory types can become mainstream memory types.

Based on Table 2.1, both STT-MRAM and RRAM are promising replacements. However, the cell density of STT-MRAM is larger compared to RRAM. RRAM devices can be manufactured using existing CMOS technology and the available data we have comes from RRAM cells [7]. Therefore, this master's thesis work will focus on RRAM as a potential replacement for traditional memory types.

Table 2.1: Device characteristics of mainstream and emerging memory technologies [7]

	Mainstream memories				Emerging memories		
			Flash				
	SRAM	DRAM	NOR	NAND	STT-MRAM	PCRAM	RRAM
Cell area	$> 100F^2$	$6F^2$	$> 10F^2$	$< F^2(3D)$	$6 - 50F^2$	$4 - 30F^2$	$4 - 12F^2$
Multibit	1	1	2	3	1	2	2
Voltage	$< 1V$	$< 1V$	$> 10V$	$> 10V$	$< 1.5V$	$< 3V$	$< 3V$
Read time	$\sim 1ns$	$\sim 10ns$	$\sim 50ns$	$< 10\mu s$	$< 10ns$	$< 10ns$	$< 10ns$
Write time	$\sim 1ns$	$\sim 10ns$	$\sim 10\mu s - 1ms$	$100\mu s - 1ms$	$< 10ns$	$\sim 50ns$	$< 10ns$
Retention	N/A	$\sim 64ms$	$> 10y$	$> 10y$	$> 10y$	$> 10y$	$> 10y$
Endurance	$> 1e16$	$> 1e16$	$> 1e5$	$> 1e4$	$> 1e15$	$> 1e9$	$> 1e6 - 1e12$
Write energy (J/bit)	$\sim fJ$	$\sim 10fJ$	$\sim 100pJ$	$\sim 10fJ$	$\sim 0.1pJ$	$\sim 10pJ$	$\sim 0.1pJ$

Notes: F: feature size of the lithography. The energy estimation is on the cell-level (not on the array-level). PCRAM and RRAM can achieve less than $4F^2$ through 3D integration.The numbers of this table are representative (not the best or the worst case)

2.3. RRAM Background

Resistive Random Access Memory (RRAM) has a metal-insulator-metal structure [2, 7].Figure 2.5 illustrates the schematic of a typical RRAM device. The resistance of the device can be altered through electrical stress [19]. By applying a positive voltage to the device, a conducting filament (CF) forms within the insulator, reducing the resistance of the device. In the case of bipolar switching, the polarity is reversed to disrupt the CF. resulting in an increase in resistance. In the case of unipolar switching the resistive state is controlled by the same polarity [2, 19].

2.3.1. Types of RRAM

Conductive bridge RAM (CBRAM) and Metal Oxide Resistive Memory (OxRAM) are two distinct variations of RRAM that differ in the type of insulator material used. OxRAM utilizes an oxide as the insulator, whereas CBRAM employs a solid electrolyte. In OxRAM, the formation of the conducting filament (CF) occurs through the creation of oxygen vacancies within the oxide. CBRAM forms a CF through the migration of metal ions into the electrolyte [7]. One advantage of CBRAM is that the metal atoms can recombine more rapidly with the solid electrolyte, thereby enhancing the switching speed. However, this comes at the expense of retention and endurance [7]. Retention refers to the duration for which data can be reliably preserved, while endurance denotes the number of reliable switching cycles a device can endure. Given that the available measurement data pertains to OxRAM and considering its improved retention and endurance characteristics, our focus will be directed towards OxRAM devices.

Figure 2.5: RRAM layout [2]

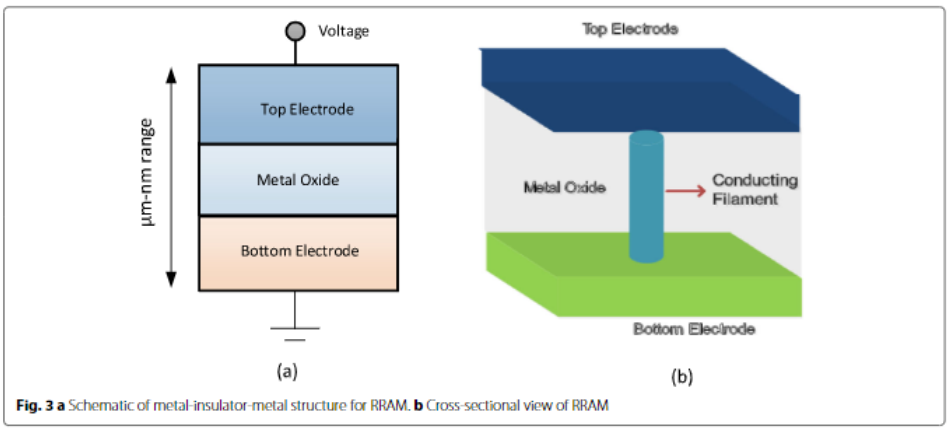


Fig. 3 a Schematic of metal-insulator-metal structure for RRAM. **b** Cross-sectional view of RRAM

2.3.2. Switching behaviour of RRAM

To be able to identify defective behaviour in RRAM the switching process of RRAM needs to be understood. The focus lies on OxRAM, but the principle is similar for CBRAM. Figure 2.6 illustrates the different states of RRAM [51].

Step A: The unformed device after fabrication. The device consists of two electrodes: a top and bottom electrode, separated by a metal-oxide containing a few oxygen vacancies which acts as a semiconductor. Typically there is a capping layer just below the top electrode (TE) where the oxygen atoms are stored. A soft breakdown is required before the device can be used [51].

Step B: During the soft breakdown phase a positive voltage is applied to the device. The voltage causes the metal-oxide bonds to break. The oxide atoms migrate towards the capping layer leaving oxygen vacancies in the metal-oxide. The oxygen vacancies form the conductive filament (CF) that connects the two electrodes, decreasing the resistance of the metal-oxide. After this process the device is in a low resistive state [51].

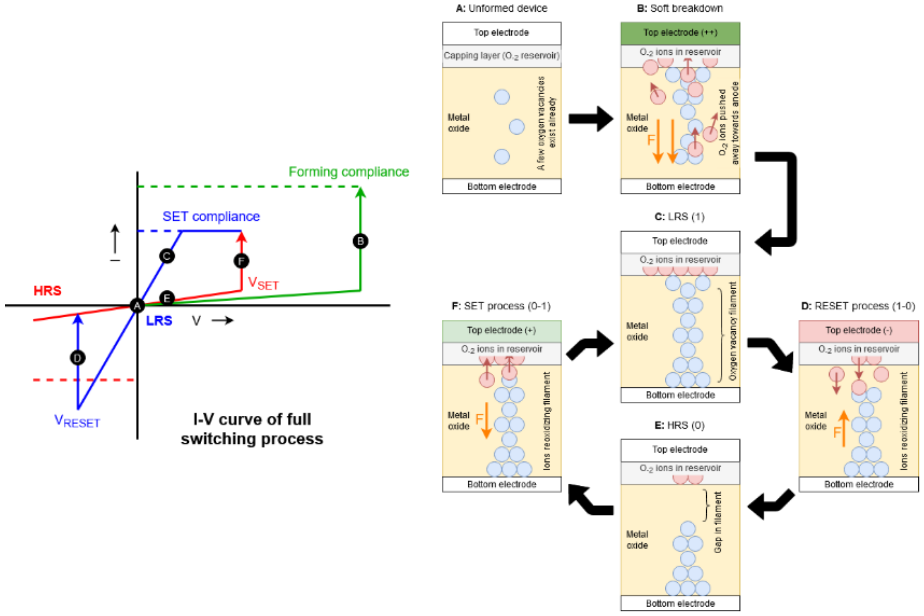
Step C: In the low resistive state (LRS) the filament connects the top and bottom electrode. Thanks to the CF, the resistance of the device is low. The state is considered as a logical '1' .

Step D: During the reset process a voltage with opposite polarity is applied to the device. The voltage causes the oxygen atoms to migrate from the capping layer to the metal oxide. The oxygen atoms migrate from the capping layer back to the metal-oxide. The metal-oxide bonds are restored and the oxygen vacancies in the metal-oxide fare filled. The CF is broken down, which increases the resistance of the RRAM cell. After this process the device is in a high resistive state [51].

Step E: In the high resistive state (HRS) the filament no longer connects the top and bottom electrodes. There is a gap between the filament and the top electrode. The conductive properties of the metal-oxide is lower than that of the oxygen vacancies of the CF. As a result, the resistance of the RRAM cell is several orders of magnitude higher. This state represents a logical '0' [51].

Step F: During the set process a positive voltage is applied to the device. The oxidized metal-oxide bonds break and migrate back to the capping layer. As a result, the gap between the CF and the top electrode disappears, and the CF re-establishes the connection between the two electrodes. The voltage during this process is lower compared to the initial soft breakdown, as the filament has already been partially formed. After the set process the device is in a low resistive state [51].

Figure 2.6: RRAM switching behaviour obtained from [52] who adapted it from [51]



2.3.3. Technological and electrical parameters

The characteristics of RRAM devices are described by technological and electrical parameters. The technological parameters describe the device structure and the physical properties of the RRAM cell. The electrical parameters describes the electrical behaviour of the device. The electrical parameters are affected by the device structure and the electrical properties of the used materials. The electrical and technological parameters are used to characterize the device.

Technological parameters

The technological parameters of an OxRAM device as described by Fieback et al. are presented in Table 2.2 [15]. Figure 2.7 gives a schematic view of the technological parameters. The technological parameters include the thickness of the oxide (t_{ox}), the length of the conductive filament (l_{CF}), the gap between the top electrode and the CF (l_{gap}), the width of the top of the CF (ϕ_T) and the width of the bottom of the CF (ϕ_B).

Each technological parameter impacts the behaviour of the RRAM cell [9, 14, 19]. The oxide thickness affects the resistance distribution of the device. The presence of grain boundaries in the oxide has a mitigating effect on the resistance distribution [32, 53]. A grain boundary is a boundary between two crystallites (grains). The structure of a single crystallite is highly ordered. This structure can be disrupted at the boundary by an adjacent crystallite when the two crystals are not aligned relative to each-other [54]. The disruption of the atomic structure at the boundary affects the electrical properties of the crystalline structure [32] . At these boundaries the number of oxygen vacancies is larger. As a result the conductive filament tends to form along these grain boundaries affecting the switching characteristics of the RRAM device. As the size of RRAM devices decrease the impact of single grain boundaries increase the device-to-device variability. Consequently, a thicker oxide reduces the device variability. Additionally, a higher forming voltage is required during the soft breakdown process to connect the two electrodes in LRS.

The gap length and the length of the filament are antagonistic parameters [15]. As the filament length increases, the gap length decreases. The gap affects both the switching voltage and the resistance of the device. A larger gap length results in a higher resistance in HRS. However, this will also lead to longer switching times, as more time is required to transition to the LRS.

The thickness of the filament impacts the retention and variability of the RRAM device [15]. In the high resistive state, the residual conductive filament can serve as a source of vacancies that bridge the gap between the filament and the top electrode, thereby reducing the retention of the device. However, a thicker filament leads to decreased variability, affecting both the voltage and resistance distributions of RRAM.

Electrical parameters

The electrical parameters describe the electrical properties of a single RRAM cycle. The parameters are described in Table 2.2.

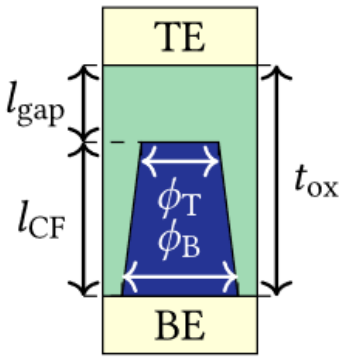
- V_{reset} is the voltage at which the device switches from a low resistive state to the high resistive state.
- V_{set} is the voltage at which the device initiates the transition from a high resistive state to low resistive state.
- HRS is the resistance of the device in high resistive state.
- LRS is the resistance of the device in low resistive state.
- $t_{H \Rightarrow L}$ describes the time required to switch from high resistive state to low resistive state
- $t_{L \Rightarrow H}$ describes the time required to switch from low resistive state to high resistive state

The electrical parameters are influenced by the corresponding technological parameters. Thicker and larger devices have a higher switching probability, which affects the reset and set voltage. As mentioned previously, the thickness and length of the conductive filament also affect the resistance distributions of LRS and HRS [55]. The electrical parameters are mainly used to study the characteristics and behaviour of the RRAM device [15, 19].

Table 2.2: Key technological and electrical RRAM parameters

	Technological parameters		Electrical parameters
t_{ox}	Oxide thickness	V_{reset}	Reset threshold
l_{CF}	CF length	V_{set}	Set threshold
l_{gap}	Gap length	HRS	Reset resistance
ϕ_T	CF top width	LRS	Set resistance
ϕ_B	CF bottom width	$t_{H \Rightarrow L}$	HRS to LRS delay
		$t_{L \Rightarrow H}$	LRS to HRS delay

Figure 2.7: Schematic view of technological parameters RRAM device obtained from [15].



2.3.4. Manufacturing of RRAM devices

Overview

The manufacturing process of RRAM devices consists of two main stages: The front-end-of-line (FEOL) and back-end-of-line (BEOL) [14, 15]. The FEOL describes the construction of the transistor. The manufacturing process in the FEOL stage has been studied extensively and refined, resulting in a streamlined process. The defects that can occur are known and comprehended. The BEOL describes the construction of the interconnects and any passive device which in this case is the RRAM cell. This stage of the fabrication process is less reliable and the impact of defects on the RRAM devices has not yet been fully characterized. To get a better understanding of the unique faults that can occur in RRAM devices, the effects of the defects on the electrical parameters need to be studied in more detail.

Front-end-of-line

The front-end-of-line stage(FEOL) describes the fabrication of transistors, which is similar to the conventional CMOS production. To construct the transistors on a single-crystalline silicon wafer the following processing steps are required: Photolithography, etching, doping ,material deposition and planarization. After the explanation of the different processing steps during FEOL an overview of the corresponding defects will be discussed [56].

1. During photolithography a photoresist coating of about 1 µm is created to protect specific areas of the wafer during the etching process. A mask consisting of transparent and opaque regions is placed above the wafer. The wafer and the mask are then exposed to ultra-violet light. Assuming a negative photoresist coating, the UV-light makes the transparent regions insoluble. The wafer is exposed to a base or acid to remove the photoresist that has not been exposed to the UV-light and soft-baked to harden the remaining photoresist [56].

2. Etching is performed to remove areas of the wafer that are not protected by the photoresist coating. The etching is done using chemical solutions [56].

3. Doping modifies the electrical properties of the exposed material. Atoms are introduced to the material which alters the electrical characteristics of the material. There are two methods: Diffusion and ion implantation. In diffusion implantation, dopants diffuse into the exposed regions of the wafer under high temperatures. The disadvantage is that you have limited control over the distribution as the dopant concentration is highest at the surface and decreases with a guassian profile as you go deeper into the wafer. In ion implantation, the dopants are introduced as ions to the exposed materials. Based on the duration and the acceleration of the ions you can control the dept and concentration of the dopants in the exposed material. Ion implantation is more expensive and an additional annealing step is required to repair the displacement of substrate atoms[56].

4. Material deposition creates thin layers of different materials that are stacked on top of each other. This can be done through physical vapor deposition or chemical vapor deposition[56].

5. Material deposition creates thin layers of different materials that are stacked on top of each other. This can be done through physical vapor deposition (PVD) or chemical vapor deposition (CVD). Chemical vapor deposition uses a chemical reaction in combination with a gas-phase precursor to deposit a solid film on a substrate. This occurs at high temperatures. Physical vapor deposition uses a physical process either sputtering or evaporation which evaporates the material in a vacuum after which the material evaporates on the thin film. The technique depends on the type of material. For CVD higher temperatures are required and is generally used for depositing dielectric materials. PVD is generally used for the metal layers and interconnects as the PVD techniques provides more accuracy, but is also more expensive[56].

6. Planarization is done to flatten and smoothen the surface of the wafer. This step is necessary to address the rough topography caused by the material deposition process[9, 15, 56].

Back-end-of-line
In the back-end-of-line (BEOL) stage, the interconnects for both the transistor and the RRAM device are built on the wafer. Several processing steps are required to build the RRAM device introducing different defects than the traditional CMOS production process [9].

1. Metallization involves applying a thin-film metal layer to create interconnects between the different components of the integrated circuit [9].

2. Bottom electrode patterning, the bottom electrode is deposited and patterned so that it connects to the underlying metal layers. Generally this is done using physical vapor deposition. PVD leaves a rough electrode surface which needs to be planarized [9].

3. BE planarization is required to reduce the surface roughness of the BE created by the PVD during patterning [9].

4. Metal-oxide deposition deposits the oxide on top of the BE. The thickness of the oxide affects the electrical parameters of the device so this process needs to be carefully controlled. As a result, atomic layer deposition (ALD) is used to place the oxide on top of the BE. ALD is more accurate than physical vapour deposition, which improves the uniformity and reduces the variability of the device [9].

5. Cap deposition is required to store the free oxygen atoms from the metal-oxide [9].

6. TE deposition is similar to the bottom electrode patterning. The top electrode is placed on top of the capping layer using physical vapour deposition [9].

7. Post-processing methods are applied to finish the RRAM device. Passivation is performed to protect the semiconductor from interaction with air or other materials. Etching is done to remove the parts that are not masked. An additional metallization layer is added to finalize the device [9].

8. Before the device can be used, initialization is required to form the conductive filament. A voltage is applied across the RRAM device that allows a CF to form. The forming current affects the thickness and length of the CF which in turn affects the resistance of the device [9].

2.3.5. Defects in RRAM devices

Overview

To be able to characterize and identify defects in RRAM devices we need to known the type of defects that can occur in RRAM devices. Defects are unwanted differences caused by the manufacturing process between the intended design and the actual device. The defects can be linked to a specific manufacturing step. For FEOL the defects can be divided in historical and emerging defects [57]. For the BEOL stage a distinction can be made between defects in the interconnect and the RRAM Device. An overview of the different types of defects is given in Table 2.3.

FEOL defects

The FEOL stage of the fabrication process refers to defects that occur during during the production of the transistor. These defects have been studied extensively. These defects can be classified into two categories: Historical defects and emerging defects [57]. Historical defects refer to variations that have been observed over and analyzed over time. These defects include patterning proximity effects, regions that should by protected by the photoresist are still affected by photons. Line-edge and line-width roughness are variations in the edge and width of the pattern resulting in a rough surface. Polish variations which impact the thickness and uniformity of the layers. Variations in the gate dielectric, which are caused by impurities in the gate oxide of the transistor [57].

Emerging defects are defects that were insignificant in impacting device performance until the dimensions of the device components were reduced. These defects include random dopant fluctuations, annealing effects, strains and metal granularity [57]. These defects have been studied extensively and test methods have been developed to detect and mitigate their impact on device performance.

BEOL defects

In the BEOL stage defects can occur in both the interconnect and the RRAM device. Defects in the interconnect, which are part of the conventional CMOS process, include opens, shorts, line roughness, irregular shapes, big bubbles and small particles [9, 15].

Defects in RRAM devices can be categorized based on their location, such as defects in the top electrode, bottom electrode, and oxide. An overview of the defects and their effects is presented in Table 2.3. For each manufacturing step the corresponding defects are discussed.

1. Metallization gives rise to defects part of the conventional CMOS process. These defects in the interconnect include opens, shorts, line roughness, irregular shapes, big bubbles and small particles [9, 15].

2. BE patterning is done using physical vapor deposition. As mentioned PVD leaves a rough surface Generally this is done using physical vapor deposition. PVD leaves a rough electrode surface which needs to be planarized. The rough surface leads to surface defects between the oxide and the bottom electrode. This increases the probability of hard oxide breakdown and device variability[9, 15].

3. Improper BE planarization will give rise to polish variations which are similar to the variability that can occur during the BE patterning. The under- and over etching of the BE can result in opens, shorts and bridge defects [9, 15].

4. Metal-oxide deposition uses ALD to control the thickness of the oxide. Thickness variations in the oxide will affects the the resistance and switching behaviour of the device increasing the device-to-device variability. Additionally, the oxide has a crystalline structure of which the edges may contain grain boundaries. These boundaries have a higher concentration of defects and conductive filaments tend to form along these boundaries [9, 15].

5. The addition of the capping layer and TE can give rise to sidewall redeposition creating a path with lower resistance affecting the device behaviour. Additionally, variation in the thickness can significantly reduce the resistance of the device[9, 15].

6. TE deposition gives rise to similar defects as the BE patterning. Surface roughness can affect the device behaviour. Additionally, sidewall redeposition can create a leakage path lowering the devices resistance.

7. Post-processing methods are applied to finish the RRAM device. The etching can give rise to re-deposition of materials and sidewall leakage, affecting device behaviour. Additionally, the RRAM devices on the wafer need to be separated, which can lead to variations in the device's dimensions as well as sidewall redeposition[9, 15].

8. The forming current affects the thickness and length of the CF which in turn affects the resistance of the device. Fluctuations in the forming current will increase the device-to-device variability and in extreme cases increase the chance of a hard breakdown[9, 15].

In the BEOL stage defects can occur in both the interconnect and the RRAM device. Defects in the interconnect, which are part of the conventional CMOS process, include opens, shorts, line roughness, irregular shapes, big bubbles and small particles. [15] Defects in RRAM devices can be categorized based on their location, such as defects in the top electrode, bottom electrode, and oxide. An overview of the defects and their effects is presented in Table 2.3. The deposition process of the BE can result in a rough surface on the BE, leading to surface defects between the oxide and the bottom electrode. This increases the probability of hard oxide breakdown and device variability. To address the rough surface, the BE is planarized which can give rise to polish variations [9, 15]. The oxide thickness affects the device resistance and switching behaviour of the device. To achieve tighter control over the oxide thickness, atomic layer deposition is used. The oxide has a crystalline structure of which the edges may contain grain boundaries. These boundaries have a higher concentration of defects and conductive filaments tend to form along these boundaries [21, 32] . The addition of the capping layer and TE will give rise to sidewall redeposition creating a path with lower resistance affecting the device behaviour [9]. The main focus of the work is on the identification and characterization of defects in RRAM devices. Table 2.3 presents an overview of all the defects and the effect on the electrical parameters of the device.

Table 2.3: The effect of manufacturing defects on the device characteristics.

Location	Defect	Defective behaviour	Parameters affected.
BE	Contamination	Affects the heat conductance and the quality of the forming process	HRS LRS V_{set} V_{reset}
	Increased electrode roughness	Affects the contact with the oxide. Which affects the resistance and the chance of a hard breakdown.	HRS LRS V_{set} V_{reset}
	Poor bonding with contact	Increases the contact and line resistance.	HRS LRS
	Thickness variations	Affects the heat conductance of the device	HRS LRS
	Over- and under-etching	Results in opens, shorts and bridges. Which affects the line resistance and capacitance	HRS LRS
Metal-Oxide	Contamination	Increases the variability of the device; Increased or decreased resistance	HRS LRS V_{set}
	Variations in the crystalline structure	Concentration of oxygen vacancy.	V_{set} V_{reset} $t_{H\rightarrow L}$ $t_{L\rightarrow H}$
	Thickness variations	Affects the switching characteristics of the device. Number of grain boundaries; Concentration of oxygen vacancies	HRS LRS V_{set} V_{reset} $t_{H\rightarrow L}$ $t_{L\rightarrow H}$
	Poor bonding with BE	Affects resistance; Increased set/reset voltage; increased chance of hard breakdown	HRS LRS
TE	Sidewall leakage	Increased variability; reduced set voltage and resistance.	HRS V_{set}
	Surface roughness	Affects resistance; device variability	HRS LRS V_{set} V_{reset}
	Poor bonding with capping layer	Affects resistance; device variability	HRS LRS
Forming	Overforming	Increased variability of HRS. Increased retention.	HRS V_{set} V_{reset}
	Underforming	Decreased variability of HRS; Lower retention.	HRS V_{set} V_{reset}

3

State of the art in characterization and diagnosis

3.1. Overview

This chapter present the state of the art in defect characterization and diagnosis. Defect characterization attempts to understand how defects affect the performance and electrical behaviour of the device. Where diagnosis focuses on finding the cause and location of the defect. The methods for defect characterization are divided in three categories: Electrical characterization, memory testing and optical characterization. Electrical characterization focuses on identifying defective devices based on electrical measurements of the RRAM cells. Memory tests focus on fault identification using fault models. Fault models are an abstraction of the defect at an electrical level that mimic the faulty behaviour of the device [13]. Optical characterization uses optical measurements to study the physical characteristics of the device. In some cases this is combined with electrical measurements. The three different techniques for defect characterization are evaluated and compared.

3.2. Electrical characterization

Electrical characterization attempts to characterize RRAM cells using electrical measurements from RRAM cells and arrays. In general there are three different setups to measure RRAM: I-V sweeps and pulsed voltage sweeps(PVS) which can be further divided into current-visible and current blind PVS [19].

3.2.1. I-V sweeps

In an I-V sweep the electrical behaviour of the RRAM device is studied by gradually increased the voltage [19]. The device is connected to a probe station. One of the electrodes is grounded and an increasing voltage is applied to the other electrode [58]. To prevent damaging the device the current is limited to reduce the amount of energy supplied [19, 58]. While gradually increasing the voltage, the current going through the device is measured. In the case of bipolar switching, a positive and negative voltage sweep is done [19]. The positive sweep monitors the SET process, the negative sweep monitors the RESET process. An I-V diagram is generated that can be used as proof-of-concept and to verify that the RRAM cell switches properly [19]. Figure 3.1 shows a typical I-V graph using an I-V sweep. The advantage is that you can guarantee the correct switching of the device as it provides insight into the intrinsic switching characteristics and visualizes one complete switching cycle. The downside is that one I-V sweep takes up to 60 seconds to generate and the method does not match the normal operation conditions [19]. RRAM normally operates using pulsed voltage sweeps. The voltage stress applied during PVS is larger which can affect the endurance of the device. However, because I-V sweeps show the entire switching cycle it is frequently used for the characterization of RRAM [19].

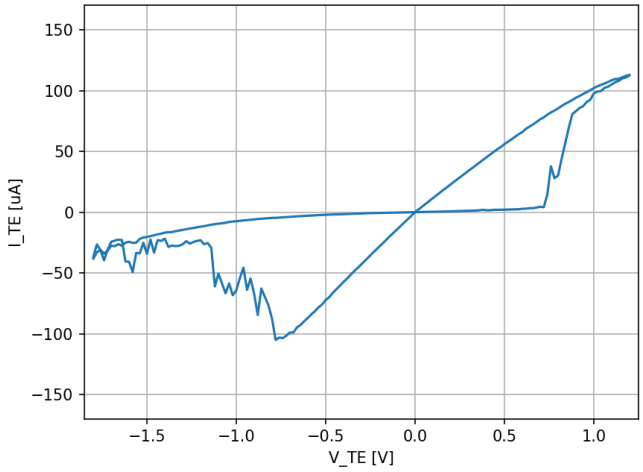


Figure 3.1: Current vs voltage diagram using I-V sweep showing the intrinsic switching characteristics.

3.2.2. Pulsed voltage sweeps

Current-visible PVS

In CV-PVS short voltage pulses larger than >1 V are applied to the device while monitoring the current of the device. One pulse may have a duration on the order of microseconds, which is much faster compared to the 60 seconds needed for a single I-V sweep [19].

The main advantage of CV-PVS is that one cycle only lasts a few microseconds and that the switching characteristics are comparable to how a device usually switches between states. However, PVS is more expensive as the current needs to be measured which is usually done using a parameter analyzer. Furthermore, the intrinsic switching characteristics of the RRAM device can not be studied as you can only retrieve the state of the device before and after switching by applying a small read voltage [19].

Current-blind PVS

CB-PVS does not monitor the current and is the cheapest method to measure RRAM devices. After a specified number of cycles the resistance of the device is measured. The method is fast and cheap but you cannot guarantee that the device has switched each cycle making it unreliable.

The different measurement setups can be used to study the characteristics of RRAM devices. The electrical characteristics of a RRAM device are described using the following metrics: endurance,variability, retention, switching time and energy consumption. These metrics are described using the electrical parameters: V_{set} V_{reset} , HRS, LRS, $t_{L \Rightarrow H}$ and $t_{H \Rightarrow L}$. The electrical parameters have already been described in subsection 2.3.3. A brief description of each metric is given here

- The endurance describes the number of times a device can switch between states where the sensing margin between HRS and LRS (R_{ratio}) is large enough. After each cycle the R_{ratio} is determined by extracting the resistance in HRS and LRS. The common method to visualize the endurance is a HRS and LRS vs. cycle graph. Figure 3.2 shows an endurance diagram. Normally, the number of cycles should be larger to assess the endurance of the device [19].
- The retention describes how long the RRAM cell will preserve its state. This mainly concerns the LRS, as HRS is the natural state of a RRAM cell. This is measured by exposing the device to a constant voltage over time by applying a read voltage of 0.1 V. Which is visualised using an current-time figure.
- The variability describes the device-to-device and cycle-to-cycle variability. This is done using the electrical metrics. These metrics are visualized using a cumulative density graph or histogram. When using I-V sweeps this can also be depicted by showing multiple cycles in a single graph.

- Switching time describes how long the device needs to switch from HRS to LRS and vice versa. This is typically determined using CV-PVS by applying triangular voltage pulses to the device.
- Energy consumption can be calculated by integrated the current and voltage over time.

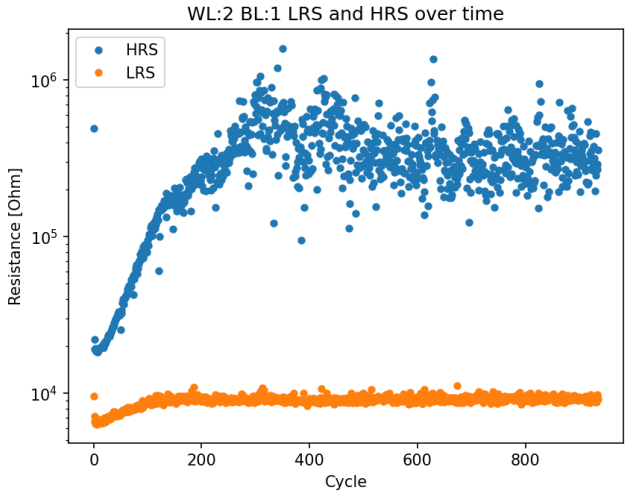


Figure 3.2: Endurance graph by plotting HRS and LRS for each cycle.

Table 3.1 shows which measurement setup can be used for the different metrics. Overall, CV-PVS and the I-V sweep give the most information and CB-PVS can only be used to determine the endurance of a RRAM cell.

Table 3.1: A comparison between the different measurement setups.

Method	Endurance	Variability	Retention	Energy consumption	Performance	Cost	Visual inspection
I-V sweep	Yes	Yes	Yes	Yes	Slow	Normal	Yes
CV-PVS	Yes	Yes	Yes	Yes	Fast	Expensive	No
CB-PVS	Yes	No	No	No	Fastest	Cheap	No

In literature, these metrics have only be used for characterization and not for defect identification of RRAM cells. Zahoor, Zulkifli, and Khanday performs a series of I-V sweeps in which the endurance is used as a metric to analyse the impact of device dimensions [2]. Different cell sizes were used. The endurance of cell sizes with 10 nm,20 nm,30 nm and 40 nm was lower compared to larger devices. Fantini et al. analysed the effect of oxides thickness on the endurance of RRAM cells. Devices with an oxide thickness of 10nm performed better than an oxide thickness of 2nm [20]. Grossi et al. evaluated the impact of grain boundaries using I-V sweeps on array level for both polycrystalline and amorphous HfO_2 [21]. The polycrystalline structures showed higher cell-to-cell variability which is contributed to the effect of the grain boundaries. The effect was illustrated using the cumulative density graphs of V_{set} and V_{Reset}.

In Table 2.3 the defects that can occur during manufacturing and how they impact the electrical parameters of the device have already been discussed. However, no one has yet attempted to use these electrical parameters to identify these defects in RRAM devices.

3.3. Memory tests

Memory tests attempt to identify defective devices using fault models. A fault model is an abstraction of a defect that describes the faulty behaviour at the electrical level. The defective behaviour of a fault is described by the memory operations that sensitizes the fault as well as the actual value stored in the memory after sensitization of the fault [13].

A fault can be described as a fault primitive using the following notation <S/F/R> [14, 15, 59, 60]. In [15] this notation was adapted so that faults with similar behaviour are grouped together. The notation is:

- S describes the chain of memory operations required to sensitize the fault. The notation is described as $x_0O_1x_1 \cdots O_nx_n$. x describes the value that is stored in the cell and O describes the type of operation e.g. read or write. E.g. $S = 0w1r1$ indicates a memory cell which holds a '0' to which a '1' was written so the expected read output is a '1'.
- F described the value that is stored in the memory cell after the sensitizing memory operation. For the current memory types this is either a '0' or a '1'. However, because RRAM is an analog device more states can be defined than '0' and '1'. Besides '0' and '1' , RRAM also has an extremely high resistance state (H) in which the resistance is larger than HRS, extremely low resistance state (L) where the resistance is lower than LRS and an undefined state (U) in which the resistance value is between HRS and LRS.
- R describes the output after a read operation. When there is no read operation

Generally speaking, faults can be divided into two categories: strong and weak faults which can be further divided into Easy-to-Detect (EtD) and Hard-to-Detect (HtD) faults [15]. Strong faults are faults that can be described by a fault primitive e.g. $(1W0/1/-)$. Weak faults are faults that cannot be described by a fault primitive because the cells content remains unaffected. Strong faults that are guaranteed to be caught after a specific memory operation are called EtD. This is not necessarily the case for all weak faults. For example, $(0r0/0/?)$ the read value can either be a '0' or a '1'. These faults together with all strong faults are HtD.

For RRAM a distinction can be made between conventional faults models and unique faults model [14]. Conventional faults are faults that can also be observed in mainstream memories such as SRAM and DRAM. Unique faults are new emerging faults caused by the analog characteristics of the RRAM device. A brief description of the conventional faults found in literature are:

- Stuck-at-Faults are faults where a cell is always in a specific state. E.g. (0/1/-), (1/L/-) are fault primitives belonging to this class. These can be caused by an defect in the word- or bit line. E.g. a short or a missing link in the WL or a defect in the forming of the device [14, 17].
- Transition Fault, the cell fails to switch from HRS to LRS or vice versa after a SET or RESET operation within the allowed time. Examples of FPs belonging to this category are (1w0/1/-), (0w1/H/-). Can be caused by defects in the interconnects and or the transistors. A defect in the capping layer or contacts [14, 17].
- State coupling Fault [61, 62, 63]: Two or more cells are connected via a bridge, bit line or world line. When the state of the addressed cell is altered the state of the neighbouring cell is affected as well.
- Write disturbance fault is caused by a defective transistor on the word line or bit line [61]. During a write operation a cell on the same line as the addressed cell also changes state.
- Read disturb fault [22]: A read fault that due to the small bias current required to read a cell changes the state of the cell.
- Incorrect read fault [64]: The addressed cell contains the correct value before and after the read operation but the wrong value is returned. This is mainly caused by resistive defects in the RRAM cell.

The unique faults are caused by the additional states present in RRAM. The ones found in literature are:

- Undefined write fault [17]: The cell fails to switch from HRS to LRS or vice versa after a SET or RESET operation and remains in the undefined state. So after a read operation either a '1' or '0' is returned. This is an indication that the bias current in the cell is too low which can be explained by a weak SL line.

- Deep state fault [65]: The resistance is larger (lower) than the boundaries defined for HRS (LRS), which can be a result of overforming [14].

- Unknown read fault [66]: A random value is returned after a read operation. This means that either the sensing margin is too small and LRS and HRS are too close to each other or that the device is in the undefined state.

To identify these faults different testing techniques have been designed that are able to detect and sensitize the conventional and unique faults. Generally march tests or specialized Design-for-testability (DfT) are used for fault detection. A March test is a sequence of read and write operations that are able to sensitize the fault [22]. DfTs add additional hardware to make the manufactured device more easily testable [15]. For example by adding scan chains so that internal states within the circuitry can be extracted. These test methods are widely used within the industry and specialized DfTs and march tests have been developed to catch the conventional and unique faults in RRAM.

The problem is that these fault models cannot be linked back to the specific defect of the RRAM device as multiple defects can result in the same fault. In mainstream memories, defects are modelled using linear resistors [14, 15, 16, 17]. For RRAM and STT-MRAM this has also been the main strategy [67, 68]. However, the fault models based on the linear defect models are not an accurate abstraction of the defect. Fieback et al. created an model for the over-forming defect and compared this to traditional method where a linear resistor is used to mimic the over-forming defect [15]. The results showed that the fault space was completely different and that the linear resistor could not be used to model the over-forming defect. As a result, the yield loss is low because we design tests for the wrong fault primitives leading to test escapes and low quality devices.

Memory tests are used for identifying defective devices. However, the fault models are incomplete and inaccurate. Additionally, these can no longer be linked back to the specific defect that resulted in the fault and cannot be used for defect identification.

3.4. Optical characterization

The most expensive method to identify defects in RRAM devices is optical characterization. Optical characterization uses optical measurements to study the physical characteristics of the device. Different methods have been used to examine RRAM devices for defect characterization. The most common practice is transmission electron microscopy (TEM), atomic force microscopy (AFM), scanning electron microscopy (SEM).

3.4.1. TEM

A focused beam of electrons is transmitted through the specimen to visualize the internal structure of the cells at nanoscale. In RRAM, this has been used to visualize the RRAM structure at both cell and array level. Additionally, this method has been used to study in-situ switching in RRAM cells [26, 27, 28, 29, 69].

At cell level TEM is frequently used to characterize the resistive switching real-time [26, 27, 28, 29]. For in-situ TEM an scanning tunnelling microscopy (STM) tip and holder is used to apply electrical stress to the cell.

Kwon et al. was the first to study the resistive switching using in-situ TEM to study the filamental switching of 3 by 1.5 µm single crystal TiO_2 devices. The conductivity of the filament is described as the extension and retraction of Wadsley defects indicated the migration of oxygen vacancies. When there was no extension there was no set process [26]. However, TEM was insufficient to analyse the complete ($Pt/TiO_{2/}TiN$) cells. The thickness of the specimen prevented the observation of structural changes. For this scanning transmission electron microscopy (STEM) was used in combination with high-angle

annular dark field (HAADF) imaging. Sun et al., Wang and Wu performed similar measurements but with different device structure: ($Ni/HfO_{2/}SiOx/n^{+}$) and ZrO_2 based RRAM devices [27, 28].

Pey et al. studied the effect of the compliance current on the switching of RRAM cells using in-situ TEM. A specimen of $100\,\text{nm}$ was processed to generate multiple metal insulator semiconductor structures ($Ni/HfO_{2/}SiOx/n^{+}$) which are isolated using focused ion beam milling. For forming a voltage sweep from $0\,\text{V}$ to $5\,\text{V}$ is done. Then for different compliance currents the switching behaviour was studied. They found that for compliance currents larger than $10\,\text{nA}$ an unique geometric defect was observed due to metal migration from the top electrode [29]. Which could be related to the intermittent undefined state faults described [70] [70].

The downside is that only a thin slice can be used for TEM [26, 27, 28, 29, 30]. The thickness of the device is not representable and can drastically alter the switching statistics of the device. Additionally, RRAM cells using in-situ TEM are studied at cell level and not array level consisting of an additional transistor, word and bit lines. TEM does not incorporate these influences and can only be applied to destructive ex situ imaging experiments [19].

3.4.2. AFM

AFM uses a probe tip which scans over the sample surface. The tip interacts with the atomic forces between the surface and the tip creating a topological map of the surface. Unlike, TEM for AFM the sample thickness does not matter and is in preferred over TEM due to sample thickness. Nandi et al., Charpin-Nicolle et al. uses AFM to measure the electrode roughness of RRAM cells. Both studied the forming voltage as a function of electrode roughness. In which the failure rate of devices increases when the electrode roughness increased [30, 31].

Variations on AFM use a conductive tip (CAFM) so that electrical characterization can be performed in-situ while measuring the surface topology. However these cannot be used for endurance tests, the CAFM tip suffers from lateral thermal drift and the high current density is harmful for the tip. Limiting the number of cycles to up to a 100 [71, 72].

In [32] CAFM is used in-situ to show the impact of grain boundaries and that the resistive switching of RRAM cells is more likely to occur at those boundaries [32]. Hence as the device dimensions decrease the impact of single grains grows larger affecting the device to device variability.

In [73] CAFM is also used to demonstrate the switching of RRAM cells. However, they also used X-ray spectroscopy to show that the oxygen atoms migrate to the anode changing the composition of the NiO film which induced a resistance change [73].

3.4.3. SEM

SEM is mainly used for visualization purposes of RRAM cells and array for visualization of RRAM cells and arrays [74].

The optical techniques are able to identify the process variations which lead to defects in RRAM cells. The physical dimensions of the RRAM device can be measured accurately. Electrode roughness can be monitored which affects the variability and the forming voltage of the device. Additionally, the switching mechanism can be studied real-time. However, due to the high current density, the number of cycles that can be characterized is limited. The tools required is expensive and measurements are time consuming. Furthermore, the optical inspection can only be applied to isolated cells and has not yet been extended for characterization at array-level. The inspection of RRAM devices using optical measurements is time consuming and costly and in some cases even destructive for the RRAM cell [19].

3.5. Conclusion

The three methods for defect characterization have been compared. Optical characterization is the most accurate, but is expensive. The physical examination of the RRAM device makes it easy to detect defects such as electrode roughness which can be studied in-situ. However, due to the high current density, the number of cycles that can be characterized is limited. Optical characterization is mainly used for individual RRAM cells and has not yet been extended to array-level characterization. Additionally, the physical dimensions of the device are not realistic as the thickness of the device is thinner than what is found in practice. The memory tests identify defective devices using fault models. The tests can be linked back to the fault model. However, the fault models in most cases cannot be

linked back to the specific defect. Additionally, most fault models are based on the linear resistance models which does not incorporate the analog behaviour of the device decreasing. Which affects the yield loss as we do test for faults that may not exist and vice versa leading to test escapes. Due to the incorrect, fault models and the inability to link the faults back to Electrical characterization is a cheap defect characterization method. This method can be used to detect faults in devices such as the undefined intermittent-state-fault, but may also be used to identify defects in RRAM at both cell and array-level as we have an basic understanding of how the manufacturing defects affect the electrical behaviour of the device. So far electrical characterization has mainly been used to study the switching characteristics and variability of RRAM devices. However, nobody has attempted to identify defective devices using electrical characterization. In the next chapters, we will evaluate the best method to automatically identify defective RRAM devices using electrical characterization.

4

RRAM data analytics

4.1. Overview

Chapter 3 showed that the electrical characterization of RRAM at cell and array level has not yet been attempted for defect identification. Chapter 4 presents a general characterization of the RRAM data using electrical characterization. First, the structure of the RRAM devices are discussed. This is followed by an evaluation of the different methods to extract the electrical parameters. The electrical parameters and visual inspection of the device are used to manually label defective RRAM devices. This is followed by a complete characterization of the devices which will be used to evaluate the important metrics used to automatically identify defective devices.

4.2. Device structure

The RRAM devices have been fabricated by ST Microelectronics using their 130 nm technology. For the top and bottom electrode TiN is used, for the oxide layer HfO_2 and a Ti capping layer is used. The structure is shown in Figure 4.1. The measurements are performed using a staircase voltage sweep with a step-size of 20 mV ranging from -1.8 V to 1.2 V. The parameters were extracted using the Keysight B1500 semiconductor parameter analyzer. The current flow and the corresponding time is measured across the device. The wafer consists of 49 devices arranged in a 1T-1R crossbar array. For each device 936 IV-sweeps were done.

4.3. Metric extraction technique

This section discusses the extraction methods for the electrical parameters: V_{set}, V_{reset}, $t_{H\to L}$, $t_{L\to H}$, R_{set} and R_{reset} . For each parameter the extraction methods are evaluated and compared. The performance of the different extraction methods are evaluated using CDF plots, individual IV plots and summary statistics.

4.3.1. V_{set}

The set voltage describes the point where the device switches from the high resistance state (HRS) to the low resistance state (LRS). Maldonado et al. describes three numerical methods to extract V_{set} from I-V sweeps[75, 76] of which two are evaluated in this thesis. The method that is not evaluated requires an additional tuning parameter and does not perform as well as the other two methods [75]. The variance of V_{set} is larger and the results are severely affected by the tuning parameter [75]. The tuning parameter will add additional complexity and make comparison to other data sets less reliable. The first method that is evaluated uses the current derivative to determine V_{set}. The second method uses the maximum distance to an imaginary straight line that connects the start and end point of a set curve [75].

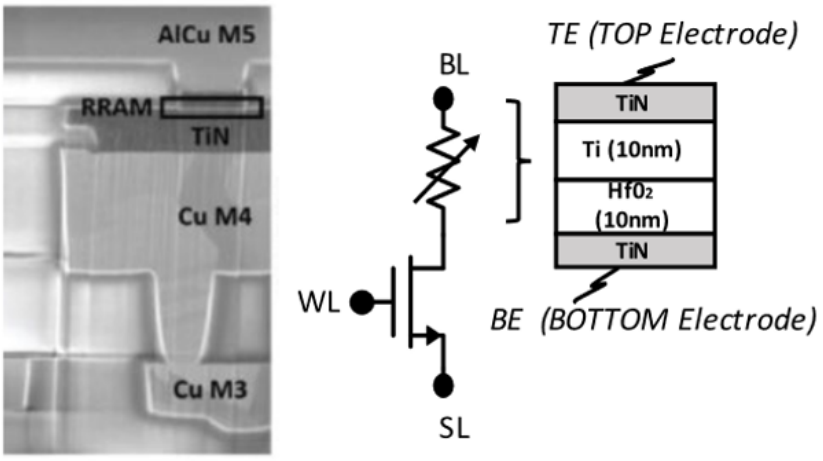


Figure 4.1: RRAM device:TiN/10 nm HfO_2/10 nm Ti/TiN

Method 1: Current derivative

The first method proposed by Maldonado et al. uses the current derivative to determine V_{set} [75]. The maximum value of the derivative defines the point where the conductive filament forms the bridge between the two electrodes which characterizes the switch from LRS to HRS. The numerical noise in the measurement data can be high under influence of external fields and temperature fluctuations [75, 76]. Figure 4.2a illustrates the method for the one point derivative. To account for the numerical noise we will need to take the derivative over a larger interval to filter out the noise. Maldonado et al. uses a five point numerical derivative Equation 4.3 to account for the numerical noise [76]. However, we have also included the one-, three- and seven-point stencils to calculate the numerical derivative. The expectation is that the one-point stencil will be less accurate due to the noise in the measurement data. Increasing the number of neighbours will improve the accuracy but the computational cost will increase. The equations for the different stencils are shown in equation 4.1,4.2, 4.3 and 4.4.

$$f'(x) = \frac{f(x+h) - f(x)}{h} \tag{4.1}$$

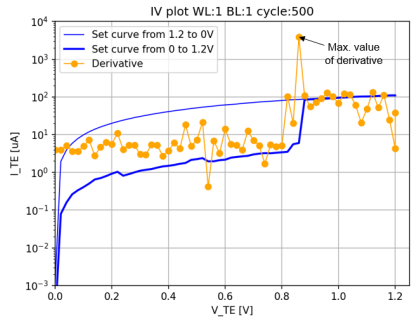
$$f'(x) = \frac{f(x+h) - f(x-h)}{2h} \tag{4.2}$$

$$f'(x) = \frac{f(x-2h) - 8f(x-h) + 8f(x+h) - f(x+2h)}{12h} \tag{4.3}$$

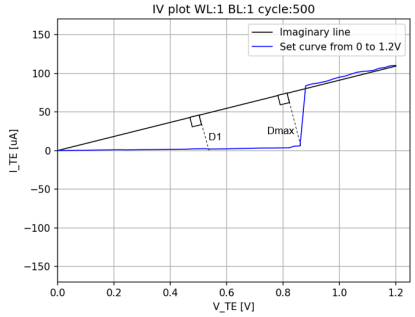
$$f'(x) = \frac{-2f(x-3h) + 9f(x-2h) - 45f(x-h) + 45f(x+h) - 9f(x+2h) + 2f(x+3h)}{60h} \tag{4.4}$$

Method 2: Maximum separation to a straight line that connects the start and end point

The second method described by Maldonado et al. calculates the orthogonal distance from each data point to an imaginary line. Figure 4.2b illustrates the method. The imaginary line is a line through the origin at 0 V and the end point at 1.2 V [75, 76]. The point that is furthest from the line is defined as V_{set}. At V_{set} the curve visibly bends and increases rapidly. This point can be described as the knee curve [76, 77]. The knee curve is the furthest away from the imaginary line [76].



(a) Illustration of extracting V_{set} using method 1 the current derivative.



(b) Illustration of extracting V_{set} using method 2 an imaginary line.

Figure 4.2: Extraction methods for V_{set}

Conclusion
Table 4.1 shows the mean and standard deviations for the different methods using all cycles of the 49 devices. The standard deviation and average are similar for the different extraction methods.However, Table 4.1 does not provide any information about the distributions and how well the methods performs for the edge cases. The CDF in Figure 4.3 shows that the one-point-stencil defines V_{set} one time-step earlier. Where the set voltage lies $0.03V$ higher for the method that calculates the maximum distance to the line. Overall, the five methods perform similar and in most cases accurately define V_{set}. The difference between the stencils is negligible. As a result, method 1 is referred to as the method which uses the derivative to determine V_{set} and method 2 uses the maximum distance to an imaginary line to determine V_{set}. Figure 4.4 shows three IV plots in which the edge cases can be observed for the extraction of V_{set}. In 2.5% of the cycles, method 2 finds a V_{set} that differs at least $0.08\,\text{mV}$. Overall, the switch from HRS to LRS is instant as can be seen in Figure 4.4a. However, in some cases the transitioning from HRS to LRS happens in two steps as is illustrated in Figure 4.4b. Method 1 is more susceptible to the second slope as it is based on the maximum derivative and as a result does not determine V_{set} accurately, while method 2 does work. In only a few cases method 2 does not extract V_{set} correctly. When the transitioning from HRS to LRS is a gradual process method 1 performs better than method 2 Figure 4.4c. This occurs in a few cases ($< 0.1\%$) and is acceptable. As a result, method 2 will be used to extract V_{set}

Table 4.1: V_{set} mean and standard deviation for the different extraction methods

Method	**Maximum distance**	**One-point**	**Three-point**	**Five-point**	**Seven-point**
Mean	0.8083	0.7601	0.7771	0.7763	0.7765
σ	0.1202	0.1121	0.1120	0.1122	0.1124

4.3.2. Reset voltage

Maldonado et al. describes five methods to extract V_{reset} [75]. In this work only two of the five methods are implemented and evaluated. Method one is similar to method one of V_{set}. The method determines the minimum current derivative of the reset curve. The second method that is implemented finds the maximum current. The other methods are not implemented because the methods add unnecessary complexity or are less reliable. One of the methods that is not implemented requires an additional tuning parameter. Another method uses the first point at which the current starts to decrease. However, due to the electrical noise we have in our measurement setup this method has not been implemented since it will lead to errors due to the current jumps. The last method that is not implemented transforms the I-V curve to the charge flux domain [75]. This method has not been implemented due to the additional complexity and is time consuming as all the data has to be transformed first. The results in [75] show that the difference between method one and method five are similar. Method one and method two are discussed in more detail as they are used in our work for the extraction of V_{reset}

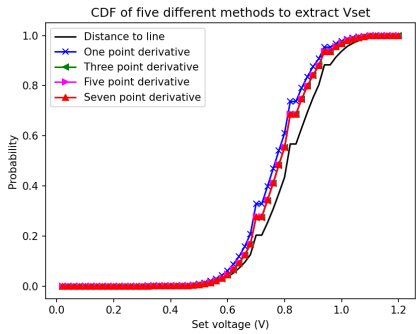
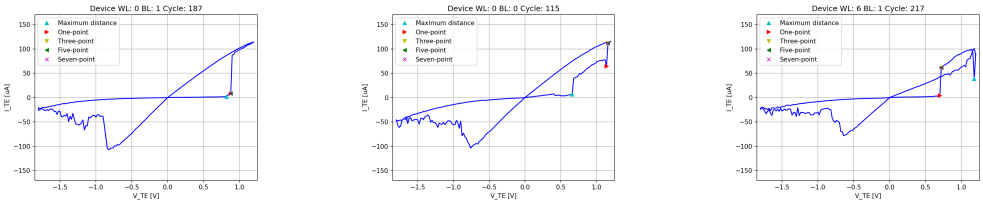


Figure 4.3: Cumulative density plot (CDF) of the five different methods to extract V_{set}.



(a) IV plot of 1T-1R device WL:0 BL:1 cycle:187

(b) IV plot of 1T-1R device WL:2 BL:0 cycle:115

(c) IV plot of 1T-1R device WL:6 BL:1 cycle:217.

Figure 4.4: IV sweep of three different 1T-1R devices. Figure 4.4a in which both method 1 and method 2 extract V_{set} accurately. Figure 4.4b where only method 1 works. Figure 4.4c in which only method 2 works.

Method 1: Minimum current derivative

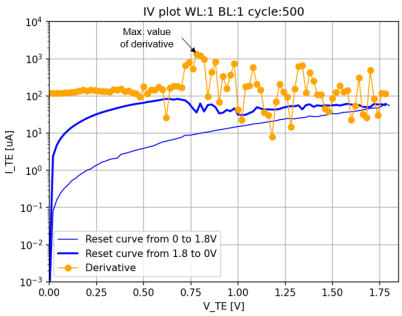
The minimum current derivative described by Maldonado et al. is similar to method one of V_{set} [75]. Figure 4.5a illustrates the method. The figure shows the reset process as well as the corresponding derivative. The process from LRS to HRS is opposite from V_{set}. So instead of finding the maximum current derivative we know need to determine the minimum current derivative. Unlike with V_{set} the rupture of the conductive filament is not as smooth as the formation and is a more gradual process which contains more measurement noise. As a result, the three-point or seven-point stencil might be more suitable to determine the derivative. The results are shown in Table 4.2 and Figure 4.6.

Method 2: Maximum current

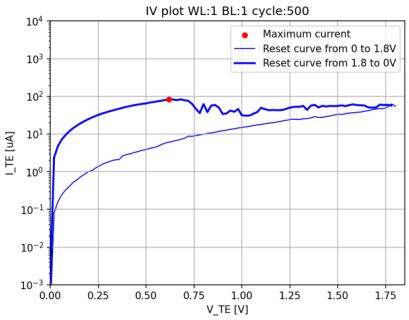
The maximum current is used more frequently to determine V_{reset} [75, 76, 78, 79]. Figure 4.5b illustrates the method. The red point is the point where the maximum current is. As the voltage decreases to $-1.8V$ the current running through the device will increase. As soon as the filament breaks the resistance will increase and the current will decrease. This is the start of the transitioning from LRS to HRS and defines V_{reset}. However, due to hysteresis the reset point can be classified at the end of the curve. [75]. To account for this the search space for V_{reset} should be constricted to -0.2 and -1.5 volt. These values are based on Maldonado et al. [75]. Maldonado et al. checked the interval between 30% and 80% of the voltage range [75]. However, in some cases the device had already switched. As a result the interval was changed to 10% and 80% of the voltage range with -0.2 and -1.5 volt.

Conclusion

The average V_{reset} of method 2 varies with more than $0.4\,\mathrm{V}$ compared to method 1 which uses the current derivative (Table 4.2). This is already a clear indicator that the two methods are not coherent. To assess which method performs better the CDF is shown in Figure 4.6. Here we see that CDF of the numerical derivative is much more spread out compared to method 2. Investigating the individual IV plots in Figure 4.7 we can see that method 2 can accurately extract V_{reset} while method 1 does not.



(a) Illustration of extracting V_{reset} using method 1 the current derivative.



(b) Illustration of extracting V_{reset} using the maximum current.

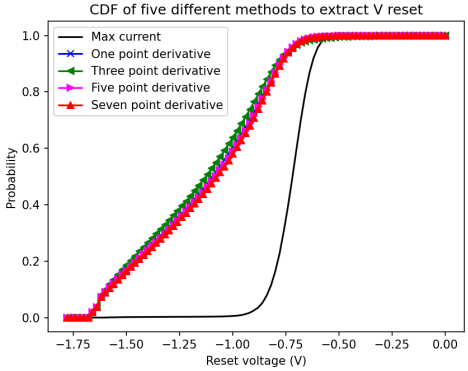
Figure 4.5: Extraction methods for V_{reset}

This is due to the fact that our measurement data contains a lot of electrical noise. The switch from LRS to HRS takes longer and consists of multiple steep slopes. This makes it difficult to determine V_{reset} using the minimum derivative.

Table 4.2: V_{reset}: mean and standard deviation for the different extraction methods

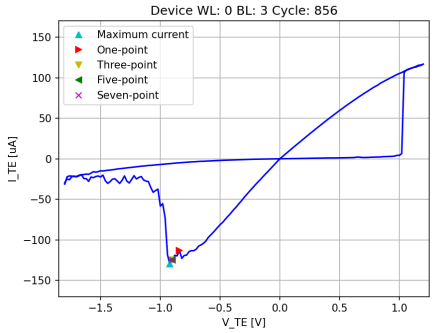
Method	**Maximum current**	**One-point**	**Three-point**	**Five-point**	**Seven-point**
Mean (V)	-0.7166	-1.1297	-1.1505	-1.1227	-1.1183
σ **(V)**	0.0888	0.2984	0.3009	0.2986	0.2991

Figure 4.6: Cumulative density plot (CDF) of the five different methods to extract V_{reset}.

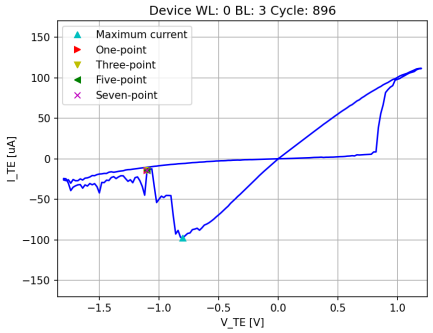


4.3.3. Resistance

The universal method to extract the HRS and LRS is described by Lanza et al. [19]. The common practice to extract the HRS and LRS is to extract the current at a read voltage of $\pm$ 0.1 V-0.3 V [19]. Figure 4.8 shows the boxplots of LRS and HRS for different read voltages. In LRS averages of the different read voltages are similar with 9918Ω, 9964Ω and 9976Ω, respectively. The median is slightly lower for a read voltage of $0.3V$. For HRS we find that the difference in resistance is larger for different read voltages. With 523982Ω, 462035Ω and 415072Ω. While the median and standard deviation decreases as well. The R_{ratio} at a read voltage of $0.1V$ is 21.8% higher compared to when a read voltage of 0.3 Volt is used. This can be explained by the fact that in some cases the device is already switching from HRS to LRS at $0.3V$. Figure 4.9 shows an I-V plot of a device with a V_{set} of 0.3 Volt. For this reason we from now on use a read voltage of 0.1 Volt.

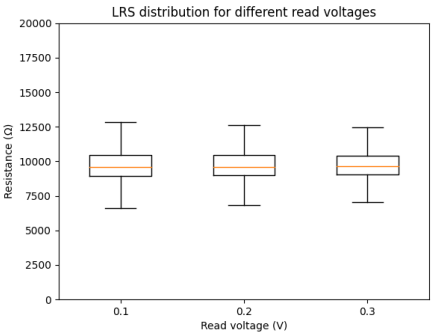


(a) IV plot of 1T-1R device WL:0 BL:3 cycle:856

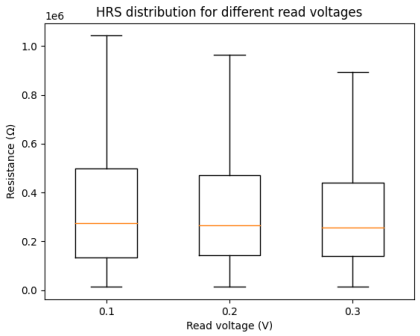


(b) IV plot of 1T-1R device WL:0 BL:3 cycle:896

Figure 4.7: IV sweep of two different cycles. Figure 4.7a in which both method 1 and method 2 extract V_{reset} accurately. Figure 4.4b where only method 2 works.



(a) LRS distribution for read voltage at 0.1,0.2 and 0.3 Volt



(b) HRS distribution for read voltage at 0.1,0.2 and 0.3 Volt

Figure 4.8: Boxplot of LRS and HRS for different read voltages. Figure 4.8a shows the LRS distribution and Figure 4.8b the HRS distribution.

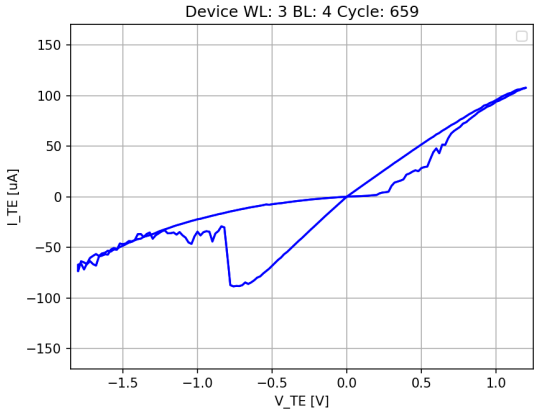


Figure 4.9: I-V plot of device with V set of 0.3 Volt

4.3.4. Switching time set

The switching time is only described for PVS in literature [19]. However, in our measurement data we also record the time stamp of each data point. As a result, we can make an estimate for $t_{H\rightarrow L}$ if we can determine the start and end point. The starting point is defined by V_{set} which uses the maximum distance to a line. For the end point we have tried two different methods.

In theory, the current derivative will keep increasing after V_{set} until the device has switched from HRS to LRS. So when the current derivative starts to decrease again we have found the end point. However, in practice the noise in our data will create negative slopes during the transitioning from HRS to LRS making this method unreliable and inaccurate.

The second method uses an additional parameter α. The resistance at V_{set} and the minimum resistance is calculated. The end point is then defined using Equation 4.5. An universal threshold value based on the average of all devices or only one device will not find an end point because the maximum resistance is too high, even when the R_{Ratio} is good enough. As a result, the resistance is based on the minimum resistance of each cycle.

$$f'(x) = \alpha R_{min} + R_{min} \tag{4.5}$$

4.3.5. Switching time reset

For the reset the same methods are implemented. Only the tuning parameters are different. The reset voltage is based on the maximum current which is described in subsection 4.3.2. The end point is based using the tuning parameter β and the maximum resistance. Equation 4.6 shows the corresponding equation.

$$f'(x) = \beta R_{max} \tag{4.6}$$

4.3.6. Energy consumption

The energy consumption can be calculated by integrating the current traces over time. According to Lanza et al. depending on the materials used the set and reset energy are similar. To extract the energy consumption from the data we use Equation 4.7. After each time step the current is multiplied with the voltage to get the power generated. This is multiplied by the time to obtain the energy consumed.

$$E = \sum_{i=1}^{n} V_i I_i (t_i - t_{i-1}) \tag{4.7}$$

4.3.7. Endurance

The endurance can only be measured by switching at least 10^6 cycles or by exposing the devices to stress by increasing the temperature. Since the measurement of our data only contains 1000 cycles for each device we cannot use the endurance as a metric.

4.3.8. Variability

The variability is studied using the electrical parameters that have already been extracted. Rather a figure of merit than an electrical parameters. Can be visualised by plotting all the IV cycles in one plot and showing the median for each device [19]. Additionally, cumulative density plots of the electrical parameters can be shown together with histograms to illustrate the cycle-to-cycle variability.

4.4. Nominal device

Before we implement the statistical analysis and machine learning algorithms to automatically identify defective RRAM devices we have to show that the nominal specifications defined in Table 4.3 by ST Microelectronics are insufficient to identify defective RRAM devices. From each device, using cycle 200 up to cycle 936, the LRS and HRS are extracted using a read voltage of $0.1\,\mathrm{V}$ as is described in section 4.3. After the extraction of LRS and HRS the R_{ratio} can be calculated for each cycle. These values are compared to the boundary values described in Table 4.3. The results are shown in Figure 4.10.

Figure 4.10 shows that only 2 devices pass the hardware specifications. The numbers in the figure indicate the number of defective cycles that were found for that device. While this can be possible it

Table 4.3: Hardware specification defined by ST Microelectronics.

Parameter	Lower bound	Upper bound
LRS	500Ω	20000Ω
HRS	90000Ω	2000000Ω
Rratio	5	400

seems unlikely that from the wafer only 4% of the devices are functional. Twelve devices have less than five defective cycles. The defective cycles need to be inspected to visually to determine whether the cycles are classified correctly.

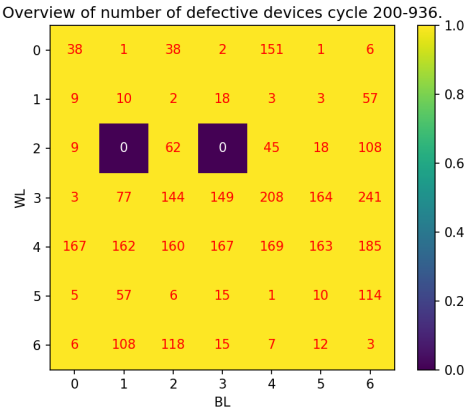
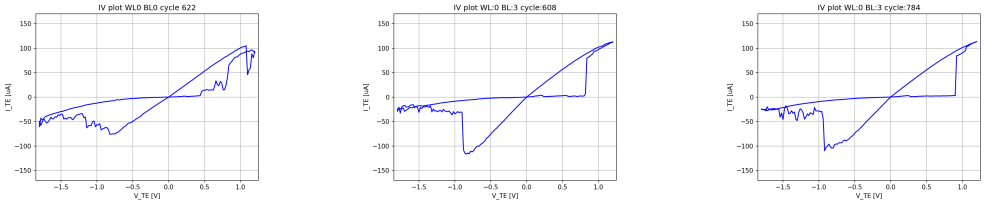


Figure 4.10: Number of defects per device

Figure 4.11 shows three cycles that have been wrongly labelled using the specifications defined by ST Microelectronics. Figure 4.11a meets the hardware specifications. However, it is evident that the device does not switch from HRS to LRS in the correct way and contains an intermittent undefined state-fault [70]. The switch should be immediate, while here the current is gradually increasing. Additionally, Figure 4.11b and Figure 4.11c do not meet the hardware specifications because the resistance in HRS is too low with 64 000 Ω and 88 723 Ω. Visual inspection of the cycles does not reveal any abnormalities. Due to these two cycles the device on wordline 0 and bitline 3 is wrongly classified as defective.



(a) Functional cycle according to hardware specifications

(b) Defective due to low HRS value of 64 000 Ω.

(c) Defective due to low HRS value of 88 723 Ω.

Figure 4.11: False positives and false negatives using the hardware specifications to identify defective devices.

The visual inspection of the I-V graphs shows that the specifications defined by ST Microelectronics for a nominal device are insufficient to identify defective RRAM devices resulting in false positives as well as false negatives. In chapter 6 the statistical methods and machine learning algorithms will be implemented to automatically identify defective RRAM devices. To evaluate the performance of the automatic defect identification methods we will first propose a method to manually label RRAM devices.

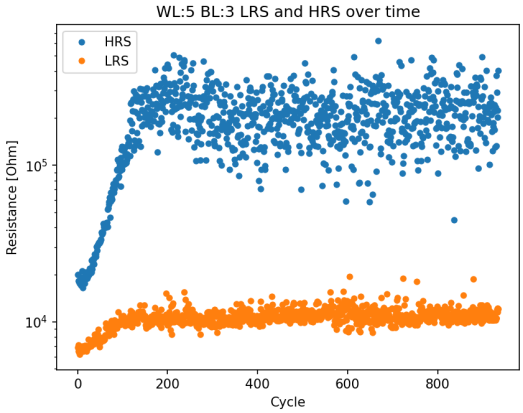


Figure 4.12: Endurance graph showing the HRS and LRS for each cycle

4.5. Labelling of the data

The hardware specifications defined in section 4.4 do not accurately identify defective devices. Additionally, we do not know the the optimal number of cycles required to reliably identify defects. To assess the performance of the hardware specifications, as well as the algorithms used in chapter 6 we will propose a method to manually label RRAM cycles. The first 200 cycles are not taken into consideration because erratic resistance states are shown. Figure 4.12 shows the resistance in the HRS and LRS. The figure illustrates that the first 200 cycles should not be taken into consideration.

From the 736 cycles of each device the sample size is determined using Equation 4.8, where n is the sample size, z is the z-score, e is the error margin, p the variance and N the population size. Assuming a confidence interval of 95%, margin of error of 5%, variance of 50% and a population size of 736 we need to label 253 cycles for each device to accurately determine whether the device contains defects.

$$n = \frac{\frac{z^2 p(1-p)}{e^2}}{\frac{z^2 p(1-p)}{e^2 N}} \tag{4.8}$$

For each device 253 cycles are randomly selected. The IV plot along with the electrical characteristics of the corresponding cycle are visualized. The cycle is then classified as either defective, functional or unknown based on the following criteria.

For the criteria the specifications from ST Microelectronics are taken into consideration. However, as was shown in section 4.4 using Figure 4.11 the specifications do not accurately identify defective devices. As a result, additional criteria are introduced to reduce the number of false positives. These criteria are based on the visual inspection of defective cycles and what we found in literature. Figure 4.11a suffers from intermittent undefined state faults and does not show a instant V_{set} [70] but according to the specifications of a nominal devices is labelled functional.

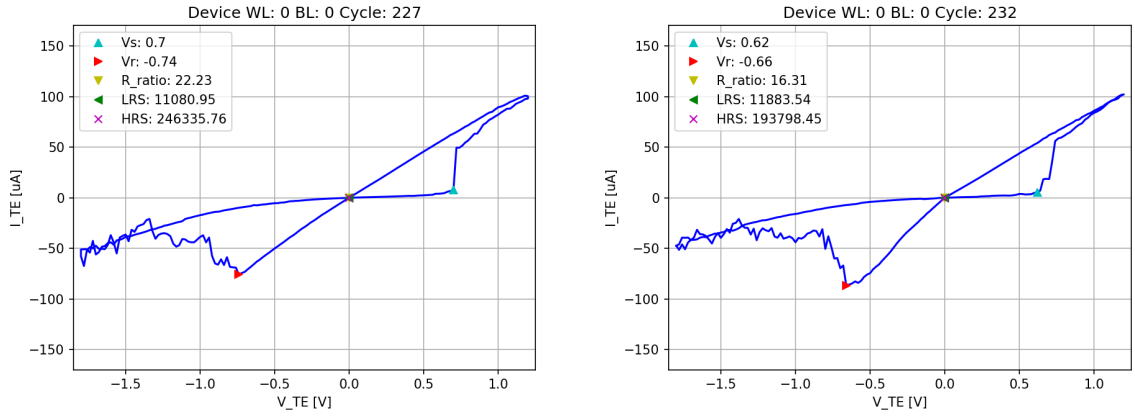
The criteria for a functional cycle are as follows.

1. The R ratio is between 5 and 400
2. LRS is between $2\,\text{k}\Omega$ and $20\,\text{k}\Omega$
3. HRS is above $90\,\text{k}\Omega$
4. The switching of V_{set} is instant as illustrated by Figure 4.11b.
5. No intermittent undefined state-fault [70]
6. V_{set} is between $0.4\,\text{V}$ and $1.0\,\text{V}$
7. V_{reset} is between $-0.4\,\text{V}$ and $-1.2\,\text{V}$

Additionally, a cycle is considered defective when one of the unique faults is observed:

1. Intermittent undefined state fault
2. V_{set} increases gradually as illustrated by Figure 4.11a.
3. No switching behaviour observed for V_{set} or V_{reset}.

The cycles that do not fall in the defective or functional criteria are assigned to the third category which specifies the cycles that need further investigation to assess the performance. Figure 4.13a is an example of a I-V graph that is labelled as to be determined. While the device meets the specifications the reset process is suffering from over-reset [80]. While this has not been linked yet to a specific defect it is not nominal device behaviour. Additionally, the criteria of an instant V_{set} is based on the visual inspection of I-V graphs. Figure 4.13b is an example in which the switching of V_{set} is not instant and consists of two steps. While this does not correspond with nominal behaviour we also do not consider the device to be defective. As a result, the device remains unlabelled.



(a) I-V graph of device labelled as to be determined

(b) I-V graph of device labelled as to be determined.

Figure 4.13: False positives and false negatives using the hardware specifications to identify defective devices.

Figure 4.14 shows the results for each device. The figure shows for each device the percentage of cycles classified as functional, defective and those of which we are not certain. In some cases the percentage of correct cycles are high, but a few defective cycles are detected. For $WL0BL6, WL1BL0, WL1BL1$ 15% of the cycles are defective applying the manual labels. $WL0BL5$ contains one defective cycle

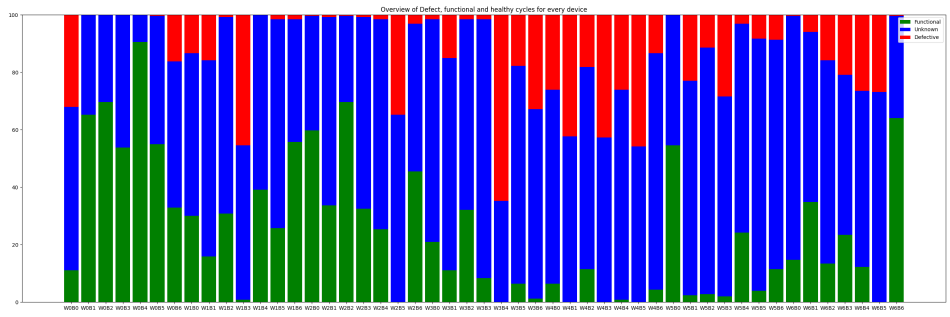


Figure 4.14: Overview of the defective, functional and healthy cycles for each device. For each device 236 cycles have been labelled.

Figure 4.15 shows the number of defective cycles for each device in a heatmap. Here we see that 12% of the devices do not show defective behaviour assuming that the cycles which have not been classified are also functional. 30% of the devices have less than 5 defective cycles which is $\approx 2\%$ of the cycles. A device is considered defective when it has more than five defective cycle. This tolerance is to account for human error and the inherent variability of the device. Based on the results of the manual labelling 20 devices are considered to be functional and 29 devices are defective.

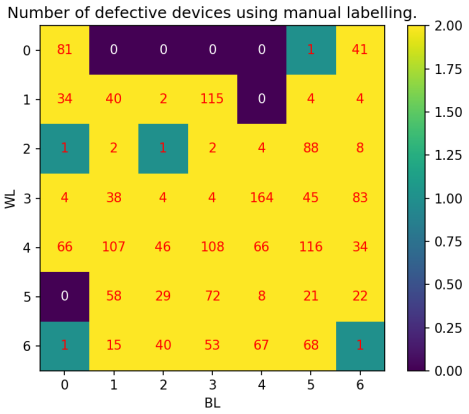


Figure 4.15: Heatmap which shows the number of defective cycles for each device for the manual labelling.

The results of the manual labelling is for the characterization of the devices, used to train the supervised learning algorithms and to evaluate the performance of the classification algorithms used in chapter 6.

4.6. Characteristics of RRAM device

4.6.1. Overview

This chapter present the characteristics of the RRAM devices. The characterization is required to set up the defect criteria and choose the correct parameters for the classification algorithms in chapter 6. For each device the electrical parameters are characterized. The analysis is used to determine if they can be used to identify defects in RRAM devices. The RRAM devices are characterized using V_{set}, V_{reset}, HRS and LRS

4.6.2. V_{set}

Figure 4.16 compares the devices labelled as defective and functional based on the manual labelling method from section 4.5 . The figure shows that on average defective devices have a lower set voltage, $0.84\,\mathrm{V}$ versus $0.78\,\mathrm{V}$ and a larger standard deviation of $0.133\,\mathrm{V}$ compared to $0.103\,\mathrm{V}$ for functional devices. However, the overlap between defective and functional cycles is too large to identify defective devices using V_{set}.

The variability of RRAM devices is studied using cumulative density plots and histograms [19] . Figure 4.17 shows the cumulative density plot and Figure 4.17b shows the histogram of V_{set} for functional and defective cycles. From this can be concluded that the spread of the defective cycles is larger and that the V_{set} is lower for defective cycles. The histogram also shows that the mode of the curve for defective cycles is lower and that the variability of defective RRAM devices is larger.

Figure 4.18 shows the results for each individual device in which the defective and functional devices are labelled. The figure confirms that the cycle-to-cycle variability is lower and set voltage is higher for functional RRAM cells. However, a low V_{set} does not guarantee that the device is defective. It is not possible to distinguish device $WL3BL5$ from the other functional devices using Figure 4.18. While the devices with the lowest V_{set} are all defective. Based on these results it is not possible to only use V_{set} to identify defective RRAM devices.

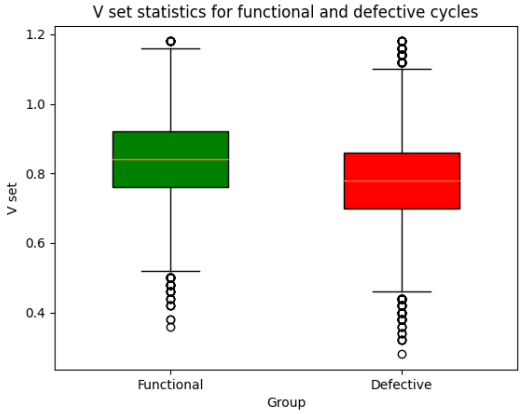
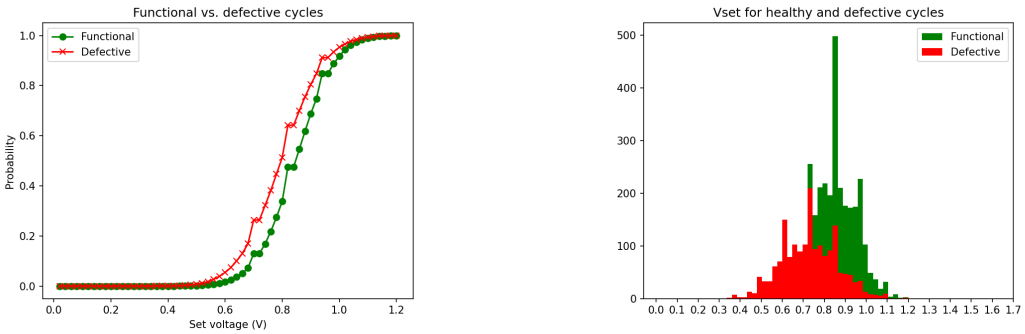


Figure 4.16: Device-to-device variability for V_{set}



(a) Cumulative density plot of V_{set} for functional and defective cycles. (b) Histogram of functional and defective cycles for V_{set}

Figure 4.17: CDF and histogram of V_{set} of functional and defective cycles

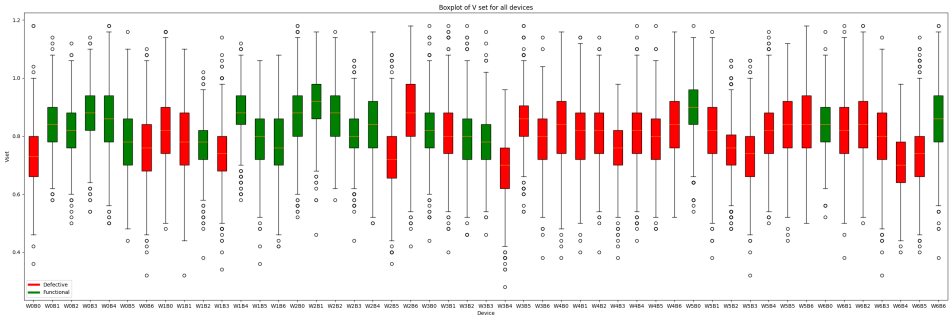


Figure 4.18: Device-to-device variability for V_{set}

4.6.3. V_{reset}

For V_{reset} a similar methodology is applied for the characterization. Figure 4.19 shows V_{reset} for the functional and defective devices. The spread is comparable which is confirmed by the standard deviation with $0.081\,\text{V}$ for the functional devices $0.094\,\text{V}$ for defective RRAM cells. The main difference is that V_{reset} has more outliers that fall outside the interquartile range (IQR). Figure 4.21 shows that the defective devices has much more outliers. These outliers could be used to identify defective RRAM devices.

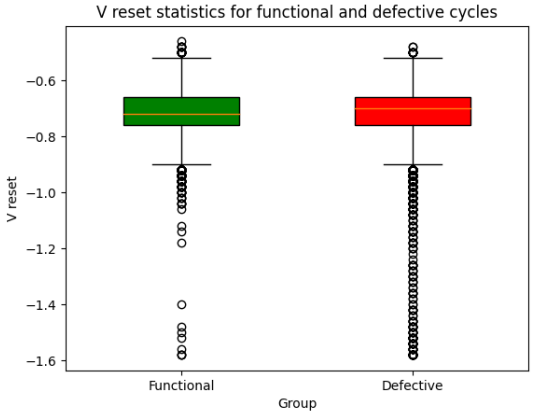
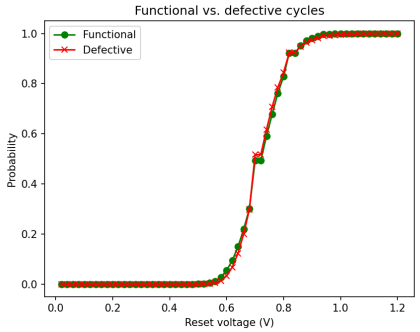
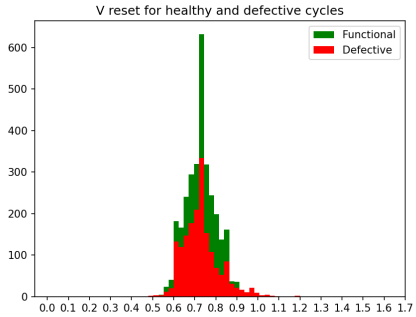


Figure 4.19: Functional vs defective devices for V_{reset}

Figure 4.20 shows the CDF and histogram of the defective and functional devices. Figure 4.6 confirms that the average and spread are similar. Whilst Figure 4.20b shows that the distribution of the defective devices is right skewed, which is confirmed by the surplus of outliers for the defective devices in Figure 4.19. Analysis of the individual devices in Figure 4.21 reveals that the excessive number of outliers for defective RRAM devices can be used as a metric.



(a) Cumulative density plot of V_{reset} for functional and defective cycles.



(b) Histogram of functional and defective cycles for V_{reset}

Figure 4.20: CDF and histogram of V_{reset} of functional and defective cycles

4.6.4. LRS

Figure 4.22 shows the functional versus the defective devices. The average resistance for the functional group is $9319\,\Omega$ compared to $9920\,\Omega$ for the defective group. The standard deviation is much lower $1077\,\Omega$ compared to $25\,452\,\Omega$. The large difference in standard deviation is explained by the cycles that did not switch from HRS to LRS.

Figure 4.23 shows the resistance distribution for each device. From this can be concluded that the

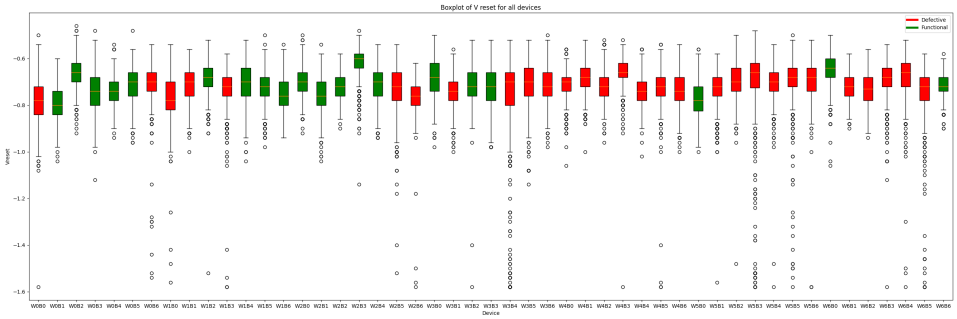


Figure 4.21: Device-to-device variability for V_{reset}

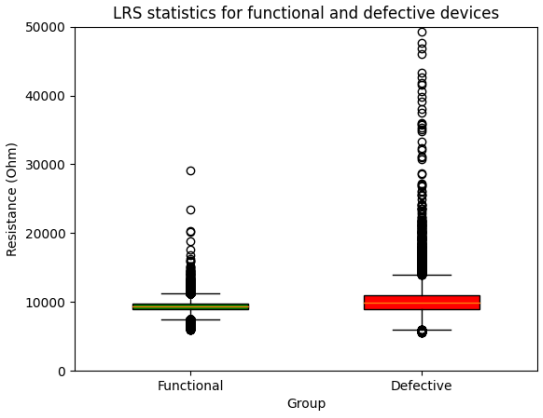


Figure 4.22: LRS functional and defective group

data distribution is wider for the defective devices. Based on the figure it is not evident which devices are defective and which are functional.

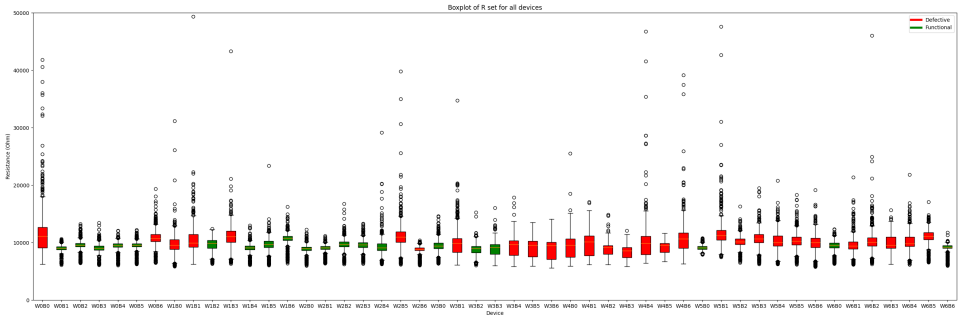


Figure 4.23: Device-to-device variability for LRS

4.6.5. HRS

Figure 4.24 shows the defective devices for HRS. The functional cycles have a median of$355\,682\,\Omega$ and standard deviation of $510\,923\,\Omega$. The defective cycles have a median of$225\,199\,\Omega$ and standard deviation of $527\,517\,\Omega$. The boxplot shows that the distribution of the defective cycles is tighter than that of the functional cycles and that overall the defective cycles will have a lower HRS.

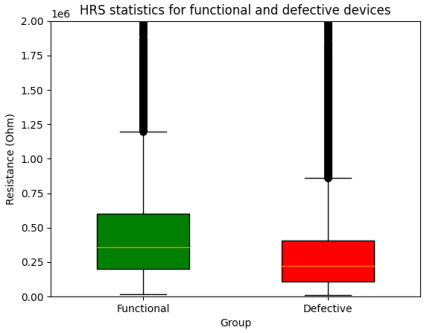


Figure 4.24: Device-to-device variability for HRS

Figure 4.25 shows the distribution for each device. From the results it is difficult to conclude how this metric can be used to identify defective devices.

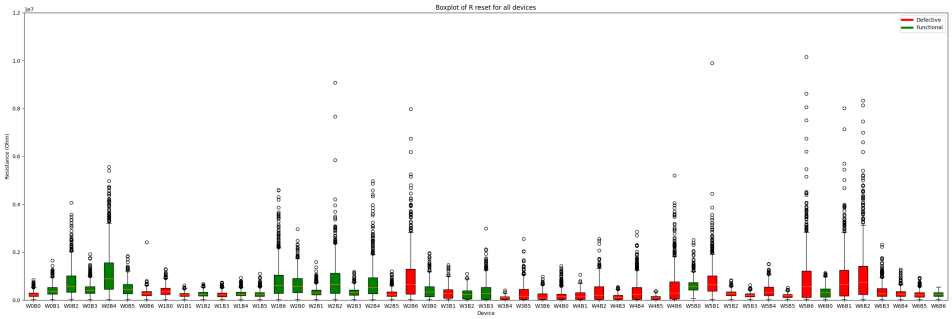


Figure 4.25: Device-to-device variability for HRS

4.7. Conclusion

Based on the characterization of RRAM four metrics will be used to evaluate for the statistical analysis of RRAM devices. These are HRS, LRS, V_{reset} and V_{set}. The extraction of the switching time is not robust enough to use for the defect identification of RRAM devices.

5

Defect identification methodologies

5.1. Overview

Chapter 4 characterized the RRAM devices, which showed that the values of the electrical parameters in defective devices differed from functional RRAM devices. This chapter describes the different methods to automatically classify RRAM devices. The first part of the chapter focuses on statistical methods to identify defective devices. The second part of this chapter focuses on machine learning techniques for defect classification.

5.2. Statistical methods for defect identification

The hardware specifications described in the previous chapter do not accurately identify defective devices. Two statistical methods have been applied. Method one uses the interquartile range (IQR) to determine new decision boundaries for each of the electrical parameters. The second method uses the functional cycles from the manually labelled data to design a model I-V curve. Using the dynamic time algorithm (DTW) and the Euclidean distance as a metric the cycles are compared to the model I-V curve which is linked back to each device. This chapter describes the method and in chapter 6 the results are discussed.

5.2.1. IQR range

The interquartile ranges provides information about the dispersion of the dataset [81]. The IQR is defined by the difference between the 75th (Q_3) and 25th (Q_1) percentiles of the data. The equation to determine the IQR is given in Equation 5.1.

$$IQR = \frac{Q_3 - Q_1}{2} \tag{5.1}$$

The IQR can be used as an outlier detection technique. The method uses the median to determine the cut-off and as a result is not sensitive to extreme outliers from defective cycles. The upper bound and lower bound is established by Equation 5.2

$$\begin{aligned} upper\_bound &= Q_3 + 1.5IQR \\ lower\_bound &= Q_1 - 1.5IQR \end{aligned} \tag{5.2}$$

$Q_1$and Q_3 are the 25th and 75th percentiles. The IQR is described in Equation 5.1. Traditionally, 1.5 is used since this corresponds to the 3σ used in traditional statistical tests and comprises about 1% of the measurement data. The IQR is used as an outlier technique on the following metrics: V_{set}, V_{reset}, HRS, LRS and the R_{ratio}

For each metric the upper- and lower bound is determined. This is applied to each cycle which is linked back to the device. The results are discussed in chapter 6

5.2.2. Model I-V curve

The method is a distance based metric based on the difference between an ideal I-V plot and the actual data. The functional cycles from the manual labelling in section 4.5 are combined into one single I-V curve. The result is depicted in Figure 5.1.

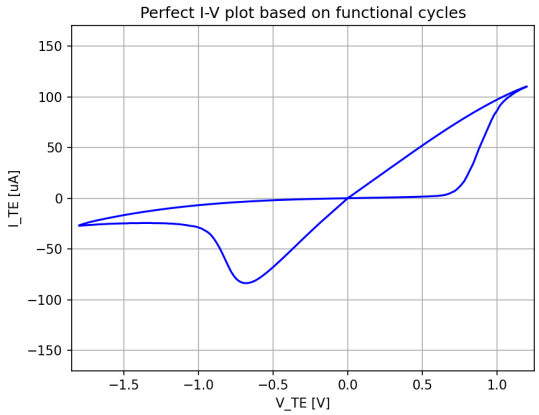
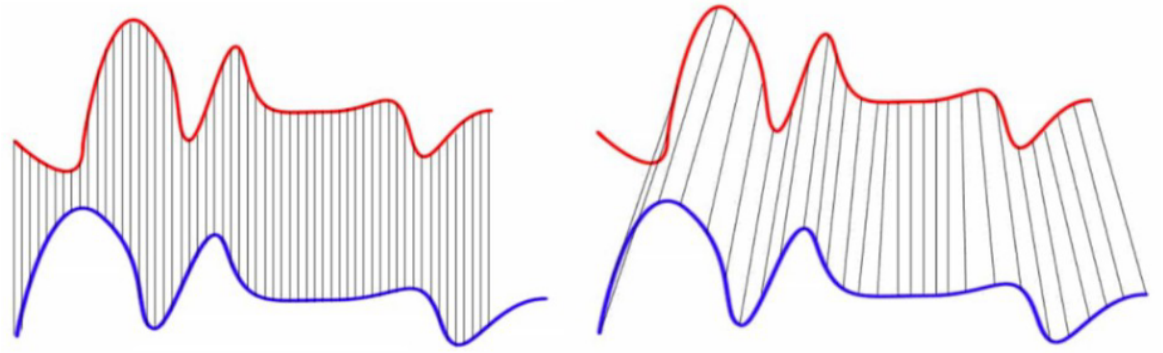


Figure 5.1: I-V curve from functional cycles averaged into one individual cycle

Two distance metrics are used to compare the I-V cycles to the model I-V curve: Euclidean distance and dynamic time warping (DTW). Figure 5.2 illustrates the difference between the two algorithms. The Euclidean distance bases the similarity of two I-V plots by adding the straight line distances between the corresponding data points. DTW contains an additional step. DTW first aligns the two data series so that the Euclidean distance between the two series is minimized after which the Euclidean distance is used to calculate the similarity between the aligned points.



(a) Euclidean matching obtained from [82]

(b) Dynamic time warping matching obtained from [82]

Figure 5.2: Euclidean and dynamic time warping algorithm [82]

DTW is computationally expensive and time consuming. As a result, the data is processed in two ways. The first method averages the cycles from each device into a single I-V plot. The I-V plot is compared to the model I-V curve using DTW and the Euclidean distance. This way only 49 cycles have to be processed. The other method is to calculate the distance of each cycle using the two algorithms with respect to the model I-V curve. Then for each device the values of the individual cycles are summed to represent a single value. This value is used to determine whether a device is defective or functional.

5.3. Machine learning methods

For machine learning three methods have been used for the classification of RRAM devices of which one unsupervised and two supervised machine learning algorithms. K-Means is an unsupervised clustering algorithm that attempts to group data based on the distance between the data points. K-Nearest Neighbour (KNN) is a supervised learning data that assigns new data points to the class of its nearest neighbours in the feature space. The third method applies the convolutional neural network (CNN) as described by [83] to identify defective devices. Before the machine learning algorithms can be applied the data is preprocessed using the principal component analysis.

5.3.1. Input data

For the machine learning algorithms we use the measurement data of the RRAM devices in three different methods. The measurement data is transformed to three different input sets:

1. Input 1 is the raw measurement data as input as described in section 4.2. A staircase voltage sweep with a step-size of 20 mV ranging from -1.8 V to 1.2 V.
2. Input 2 consists of the electrical parameters used in the statistical analysis. These are V_{set}, V_{reset}, HRS and LRS. The advantage is that the input size is much smaller and it is easier to determine why the device is defective.
3. The third input stores the raw measurement data of each cycle as an image. The x-axis ranges from -1.8 V to 1.2 V and the y-axis ranges from -170 µA to 170 µA. This method is mainly used for the CNN algorithm.

Input 1 is used so that the algorithms might recognize difference between defective and functional devices that we have not yet discovered. Input 2 is to see if the current metrics that we use in literature are valid to characterize RRAM devices. Input 3 is mainly used for the CNN as the algorithm is mainly applied on images.

Principal component analysis

K-NN and K-Means do not work well for high dimensional data [84]. As a result, a principal component analysis is applied to the three datasets to reduce the number of dimensions. This section describes the concept of the principal component analysis and how it is applied to the input data.

The principal component analysis reduces the number of dimensions by creating new variables (Principal components) which are a linear combination of the original variables [85, 86, 87]. The principal components are the eigenvectors of the covariance matrix. The first principal component (PC) maximizes the variance of the data and contains the most information. The second PC is an orthogonal vector on the first PC and describes a percentage of the variance. The result is a new coordinate system that describes the variance of the data in the most efficient way [85, 86, 87]. The python library scikit-learn has a function that can apply PCA to the input data [88].

The PCA is applied to all three input data sets. The number of principal components that is used for the K-Means and K-NN clustering is determined by the percentage of variance explained by the corresponding PCs. This value is set at 95%. For each input the results are shown for the functional and defective cycles of the manually labelled data to see if a difference can be observed between defective and functional cycles. Additionally, the PCA points of the cycles are summed for each device and labelled using the results from the manual labelling of the device to determine whether groups can be distinguished.

5.3.2. Unsupervised method 1: K-means

After PCA, K-Means is one of the methods used to classify the data points from the PCA. The advantage of K-means is that the method works for large datasets, converges quickly and is relatively simple to implement. Additionally, the data does not need to be labelled in advance. The disadvantage is that the clustering method, similar to all clustering methods, is sensitive to outliers.

The K-means algorithm works the following way and requires the number of classes (K) to be known in advance.

1. For each class a random centroid is selected.

2. For each data point PCA the distance to each centroid is calculated using the Euclidean distance. The data point is assigned to the centroid that is closest to the data point.
3. The centroid are redefined by taking the average of all data points that are in the same cluster.
4. Repeat the previous two steps until the convergence criteria is met.

Due to the simplicity of the algorithm the K-Means clustering method is applied to the PCA of all the inputs. The results from the K-Means algorithm are compared to the predefined labels of the cycles and devices to evaluate the performance of the algorithm.

5.3.3. Supervised learning method 1: K-NN

Overall unsupervised learning algorithms are less accurate and since we now have information about which cycles are defective and functional we can also use supervised learning algorithms. The advantage of K-NN is that the algorithm is fast and does not require any training. The labelled data of the functional and defective cycles are stored and based on a similar principle as K-Means. The difference is that with K-NN the clusters are already defined by the labelled data. The algorithm for a new data point consists of the following steps.

1. The distance of the new data point to the labelled data points in the training set is calculated
2. The number data points K that are nearest to the new data point are determined.
3. The new data point is assigned the label that occurs most frequent among the K neighbours.

5.3.4. Supervised learning method 2: Convolutional Neural Network

The CNN architecture is copied from Kocak, Mitard, and Naskali uses the architecture as a pass/fail check in the quality control of FETs [83]. The architecture is used as a baseline for the RRAM devices to use as a pass fail check. The CNN is trained using the labelled data.

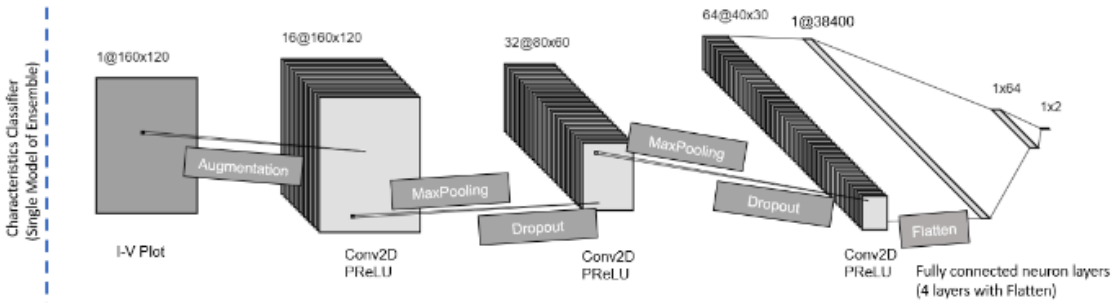


Figure 5.3: Architecture of CNN [83]

6

Results

This chapter provides the results from the different classification algorithms described in chapter 5.

6.1. Statistical analysis for defect identification

6.1.1. Results: Statistical analysis

Instead of the hardware specifications we propose a more statistical approach where the boundaries are defined using the interquartile range. For each electrical parameter we have determined the upper and lower limit using Equation 5.2. The limits for each parameter are given in Table 6.1. The table shows each metric and the corresponding upper and lower bound that was determined using Equation 5.2.

Table 6.1: Upper and lower boundary for each metric using the IQR.

Metric	Lower bound	Upper bound
V_{set}	$0.48\,\mathrm{V}$	$1.12\,\mathrm{V}$
V_{reset}	$-0.91\,\mathrm{V}$	$-0.51\,\mathrm{V}$
LRS	$6979.80\,\Omega$	$12\,944.58\,\Omega$
HRS	$10.73\,\log(\Omega)$	$14.80\,\mathrm{Log}(\Omega)$
$Log(R_{Ratio})$	1.39	5.69

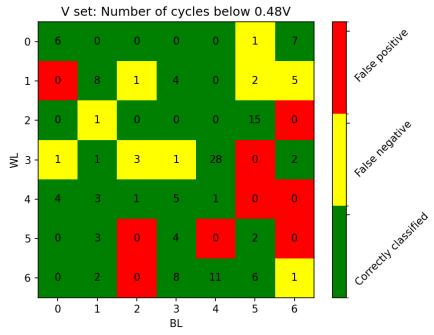
For each metric the performance is evaluated. Figure 6.1,Figure 6.2,Figure 6.3,Figure 6.4 and Figure 6.5 show the results for V_{set},V_{reset}, LRS, HRS and the R_{Ratio}. The figures show a heatmap in which the result of the algorithm is compared with the corresponding labels. The colors represent the false positives, false negatives and the devices that have been classified correctly. The numbers in each box represent the number of defective cycles the algorithm found for that device.

Figure 6.1a shows the devices that have been labelled as defective because V_{set} was below the threshold of $0.48\,\mathrm{V}$. In total the metric as classifier consists of 9 false negatives and 9 false positives which is a accuracy of 62%. Figure 6.1b shows the devices of which the upper limit of $1.12\,\mathrm{V}$ for V_{set} is exceeded. 15 devices are wrongly labelled as defective and 9 defective devices are not identified by the upper threshold of V_{set} resulting in an accuracy of 48%.

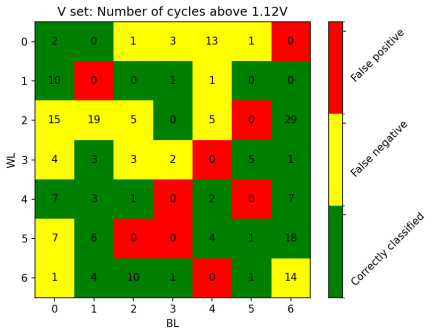
Similar for V_{reset}, Figure 6.2a shows the number of devices detected as false positive, false negative and correctly classified for the lower threshold and Figure 6.2b for the upper threshold. The lower threshold identifies 4 devices as functional of which 1 device is a false positive and 17 out of 20 functional devices are wrongly classified as defective. Figure 6.2b miss-classifies 7 devices as defective, 25 devices as functional and 4 true defective devices are found.

Figure 6.3a shows the result for the lower threshold in LRS. The lower threshold of the hardware specification of $500\,\Omega$ is too strict. The threshold of $6979\,\Omega$ determined by the IQR range correctly identifies 4 defective devices. The other devices are all considered functional. Figure 6.3b find 11 false negatives and 2 false positives. The other 36 devices are correctly classified as defective or functional.

Figure 6.4a shows the results for the lower threshold of the logarithmic value of HRS. The method identifies the defective devices on word line 3 and 4 and contains 3 false positives. Figure 6.4b does not work. Seven device are correctly identified as defective but also contains seven false negatives.

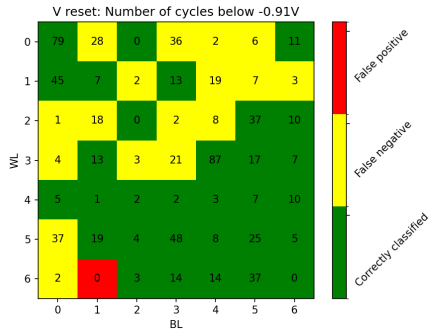


(a) Identification of defective RRAM devices using the lower bound of V_{set}.

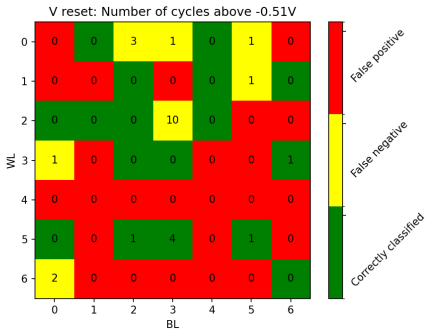


(b) Identification of defective RRAM devices using the upper bound of V_{set}.

Figure 6.1: Defect identification of RRAM devices using V_{set}

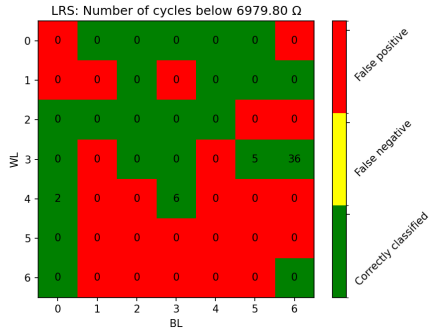


(a) Identification of defective RRAM devices using the lower bound of V_{reset}.

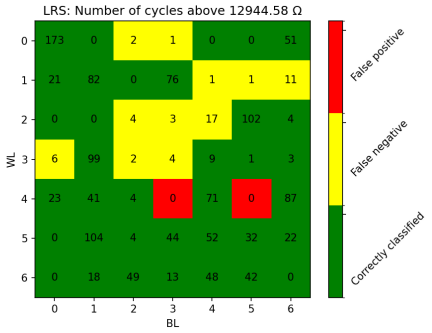


(b) Identification of defective RRAM devices using the upper bound of V_{reset}.

Figure 6.2: Defect identification of RRAM devices using V_{reset}

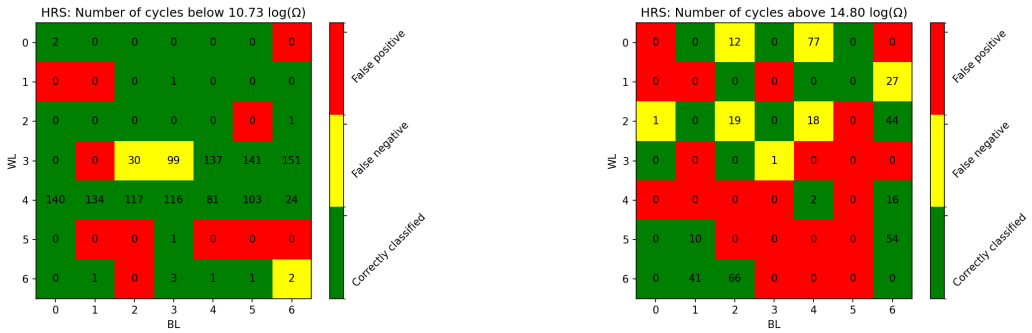


(a) Identification of defective RRAM devices using the lower bound of LRS.



(b) Identification of defective RRAM devices using the upper bound of LRS.

Figure 6.3: Defect identification of RRAM devices using LRS

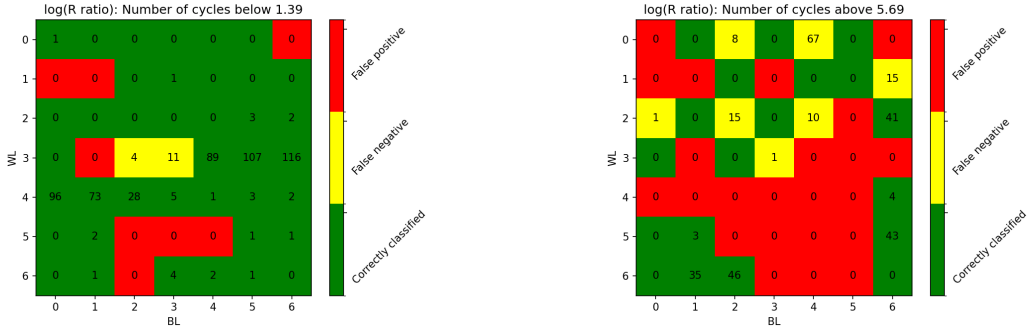


(a) Identification of defective RRAM devices using the lower bound of HRS.

(b) Identification of defective RRAM devices using the upper bound of LRS.

Figure 6.4: Defect identification of RRAM devices using HRS

The logarithm of the R_{ratio} in Figure 6.5 is an extension of LRS and HRS. The results of lower threshold of the R_{ratio} shown in Figure 6.5a are similar to the results of the lower threshold of the LRS and HRS metric. The lower bound of the R_{ratio} performs slightly better as only 2 false positives are found. The results of upper threshold of the R_{ratio} are identical to that of the upper threshold of HRS and is not a good metric to use as it is to identify defective devices.



(a) Cumulative density plot of V_{reset} for functional and defective cycles.

(b) Histogram of functional and defective cycles for V_{reset}

Figure 6.5: Defect identification of RRAM devices using R_{ratio}

The statistical analysis is a combination of different metrics that are analysed to identify defective devices. As a result, devices that are wrongly classified as defective (false negatives) are more important than false positives. However, non of the metrics are able to identify devices without identifying multiple false positives.

6.1.2. Results: Model I-V curve

The golden I-V is a similarity metric that is used to measure the similarity between two RRAM devices. A model I-V curve is generated by averaging the cycles from functional devices as was shown in Figure 5.1, which is compared to the test data using dynamic time warping and the euclidean distance as metric.

Figure 6.6 and Figure 6.7 applies the two algorithms on the averaged cycle for each RRAM device. Figure 6.8 and Figure 6.9 first applies the algorithm to each cycle after which the scores of each cycle are added for each device. The labels from section 4.5 as well as a decision boundary that is optimized for the least number of false negatives (FN) are added to each figure .

Figure 6.6 shows that the dynamic time warping algorithm does not perform well to classify defective

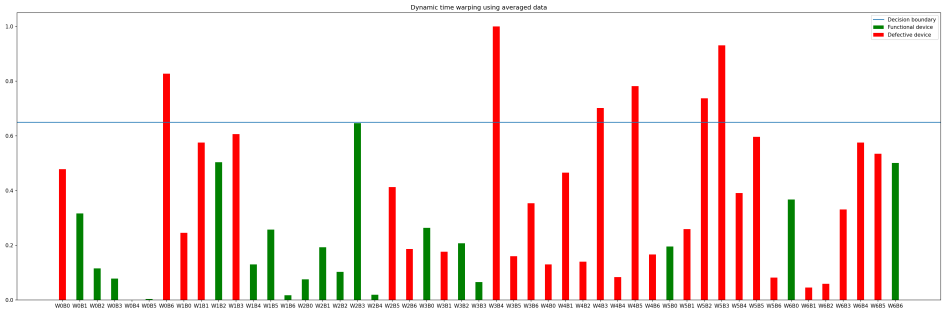


Figure 6.6: Dynamic time warping algorithm applied to each individual cycle and linked back to each device.

devices. Figure 6.10 shows the performance of the algorithm for each decision boundary. The score is based on the percentage of devices that are correctly classified. The highest performance is 69% when the decision boundary is set at 0.14. The decision boundary Figure 6.6 displays the threshold for the least number of FN. Based on this 6 of the 29 devices can be identified as defective using this algorithm.

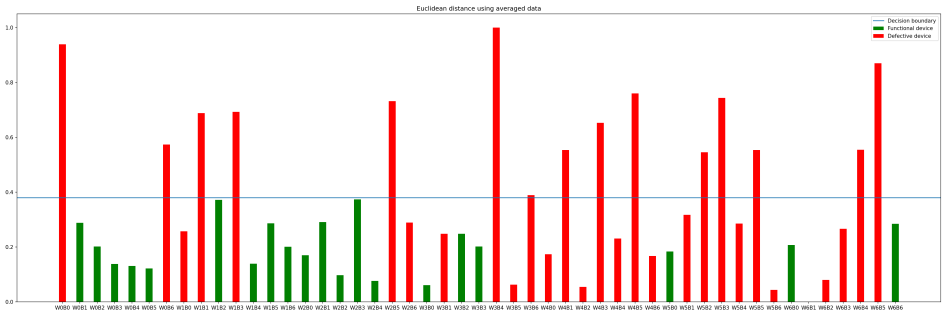


Figure 6.7: Euclidean distance applied to each individual cycle and linked back to the corresponding device.

Figure 6.7 scores better compared to the dynamic time algorithm applied in Figure 6.6. The highest score is 71% with a threshold of 0.21 (Figure 6.10). If the decision boundary is optimized for the least number of FN 14 defective devices can be identified.

The dynamic time algorithm applied to each individual cycle performs the worst. The highest percentage of devices correctly classified is 67% at a threshold of 0.15.Figure 6.8 shows that 4 of the 49 devices can be correctly identified as defective focusing on the least number of false negatives. However, in practice without the manual labels as reference it will be challenging to determine the boundary as the margin between the functional device ($W5B0$) and the defective devices is small. Figure 6.9 shows the distance metric for each individual device of the averaged cycles. Optimizing for the number of FN, we can correctly identify 20 from the 29 defective devices which results in an accuracy of 69%. The Euclidean distance as similarity measure for each cycle performs the best. Figure 6.10 shows that 81% of the devices can be correctly classified at a threshold of 0.22.

Based on Figure 6.10 the performance of the euclidean distance as a metric applied to each individual cycle performs the best with a performance of 81%. The other three methods perform similar with a performance of $\approx 70\%$. If we evaluated the score based on the number of false positives the euclidean distance performs better with an accuracy of 48% and 69% for the averaged and not averaged data. Where dynamic time warping scores 21% and 14%, respectively.

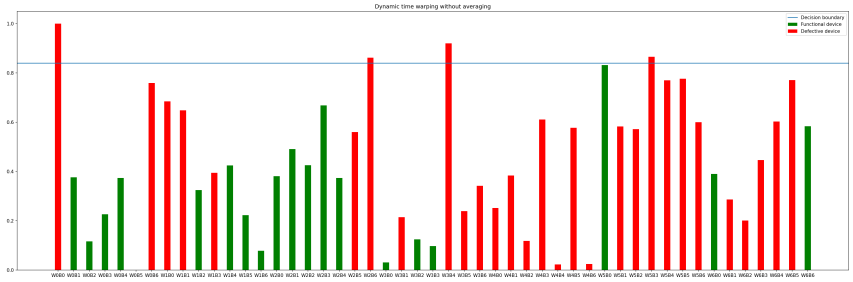


Figure 6.8: Dynamic time warping algorithm applied to averaged cycle from each device

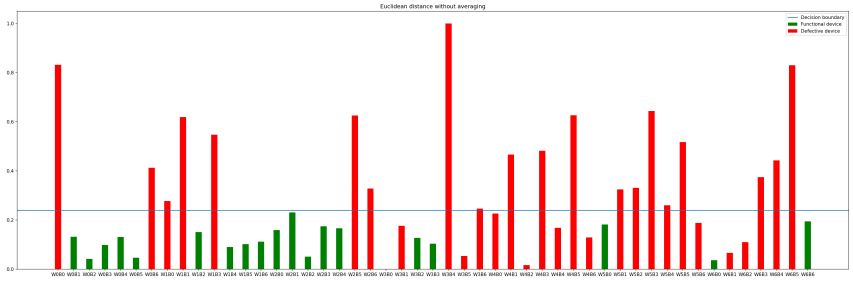


Figure 6.9: Euclidean distance applied to averaged cycle from each device

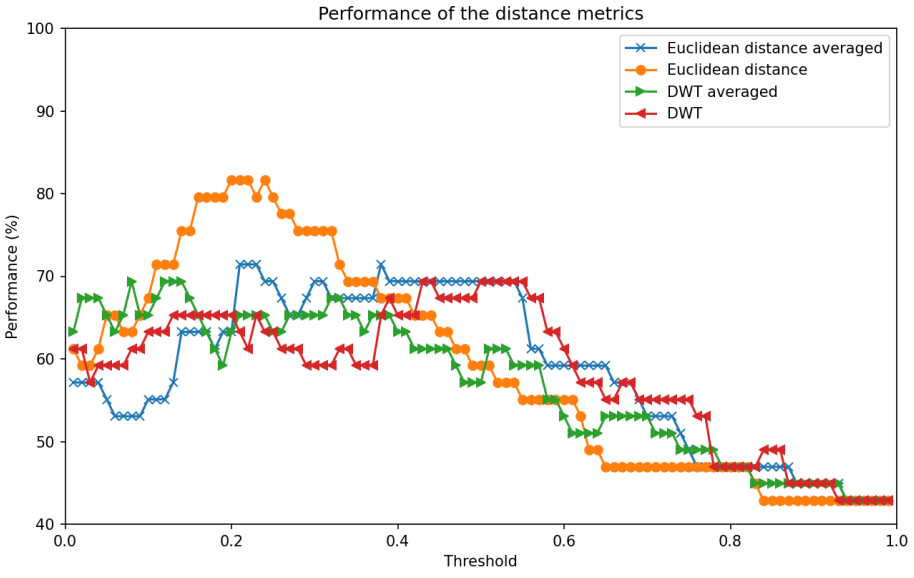


Figure 6.10: Performance of the applied algorithms for difference decision thresholds.

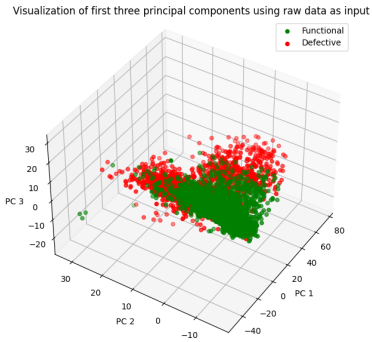
6.2. Unsupervised learning

This section shows the results of the three machine learning algorithms as well as the results from the principal component analysis.

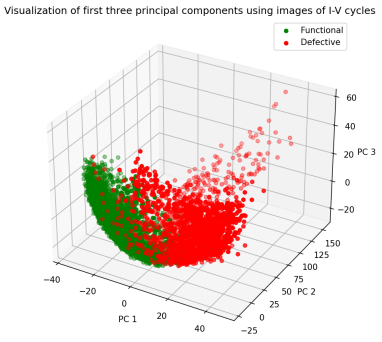
6.2.1. Pre-processing: Principal component analysis

The principal component analysis (PCA) is a preprocessing technique that simplifies complex datasets by reducing the number of dimensions, while keeping the trends and patterns from the data. This method is used as a pre-processing step for the unsupervised learning algorithms as well as the supervised learning algorithms. As explained in chapter 5, PCA has been applied on three different input sets. The raw data, the cycles stored as an image and the extracted metrics.

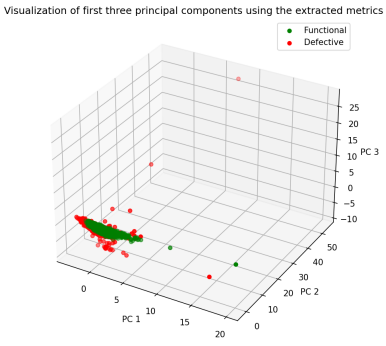
Figure 6.11 shows the results for each dataset, each figure displays the first three principal components of the PCA analysis. In each figure the labels of section 4.5 are incorporated. Figure 6.11a shows the result in which the measurement data is directly used for PCA. Figure 6.11b shows the result where the PCA is applied on the images of I-V cycles and in Figure 6.11c PCA is applied on the extracted metrics. For each figure two clear clusters can be identified. Figure 6.11a has the functional cycles in the middle of which the defective devices are on the outskirts of the functional cycles. Figure 6.11b contains two groups and the metrics from Figure 6.11c is affected by a few extreme outliers.



(a) Analysis of I-V cycles using raw data as input and manual labels.



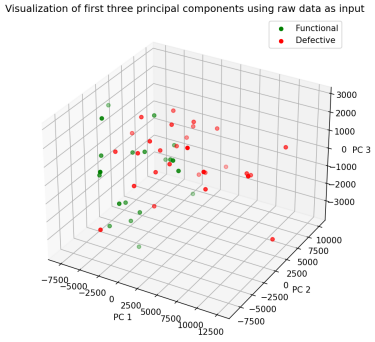
(b) Analysis of I-V cycles using images of I-V cycles as input and manual labels.



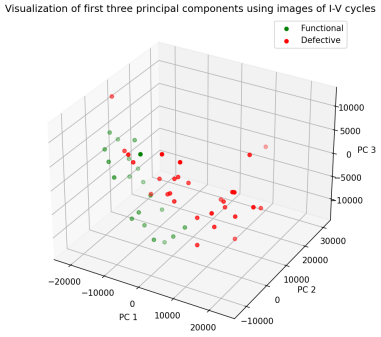
(c) Analysis of I-V cycles using the metrics as input and manual labels.

Figure 6.11: The results of the three different input data using the principal component analysis in which the manual labels from section 4.5 are used as classification

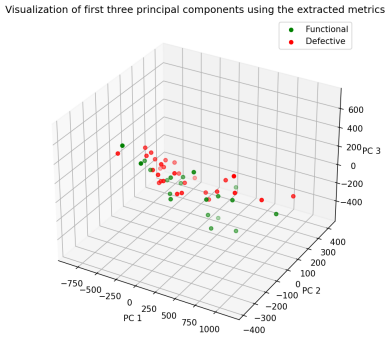
The purpose is to automatically identify defective devices. To link the cycles back to the devices we can either accurately identify defective I-V cycles and link the defective cycles back to the corresponding RRAM device. The other approach would be to add the principal components from each cycle for every device after which a classification algorithm is applied. The results are shown in Figure 6.12. The results of Figure 6.12b and Figure 6.12a look promising as two groups can be identified. For the metrics in Figure 6.12c the two groups seem to have more overlap. While the machine learning algorithms will most likely perform better for Figure 6.12b and Figure 6.12a we will apply the algorithms to all three formats.



(a) Defective and functional devices using PCA of raw data as input including the manual labels.



(b) Defective and functional devices using PCA of images of I-V cycles as input including the manual labels.



(c) Defective and functional devices using the metrics as input.

Figure 6.12: PCA plot of the first three principal components using the metrics, raw data and images of I-V cycles as input.

The manual labelling of the RRAM devices is time consuming and prone to human error. As a result, unsupervised learning algorithms are also used to classify RRAM devices. In the next part K-Means, K-NN and CNNs are used to classify the results from the PCA analysis.

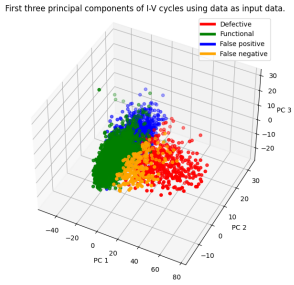
6.2.2. K-Means

KMeans is applied on three different input sets. For each input each device is classified using two different techniques. By applying K-means to each individual cycle and linking that back to the device or by applying K-means directly to the devices.

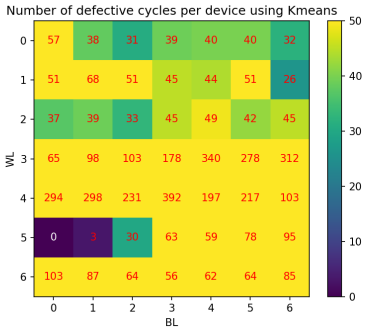
Cycle classification

Figure 6.13 uses the raw data as input and evaluates the performance of the individual cycles. Figure 6.13a shows which cycles the cycles which are wrongly classified as functional, defective and which

are correctly classified. Kmeans does not work well for spectral data in which the functional cycles are surrounded by the defective cycles. Figure 6.13b shows the number of defective cycle for each device. Only the device $WL5BL0$ does not contain any defective cycles. Furthermore, the device on $WL3$ and $WL4$ contain the most number of defective cycles. This could be an indication that these devices contain the same type of defect.



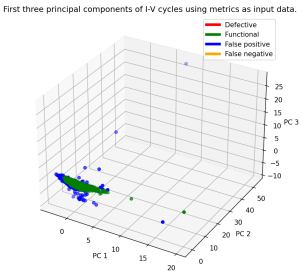
(a) Visualization of the defective and functional cycles after K-means.



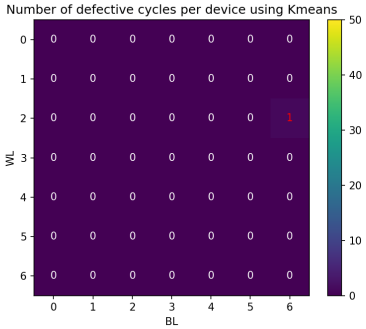
(b) Number of defective cycles for each device after applying K-Means on raw data as input

Figure 6.13: Result of the Kmeans clustering Figure 6.13a shows the number of correctly classified and wrongly classified cycles. Figure 6.13b shows the number of defective cycles for each device.

Figure 6.14 does not perform well due to the extreme outliers. K-means is not deterministic. However, as Figure 6.14a shows, the outlier is too far apart from the main cluster and is classified as a separate class. As a result, all the cycles are classified as functional devices as is confirmed by Figure 6.14b which shows the defective cycles for each device.



(a) Visualization of the defective and functional cycles after K-means.

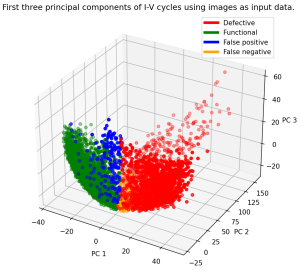


(b) Number of defective cycles for each device after applying K-means on raw data as input

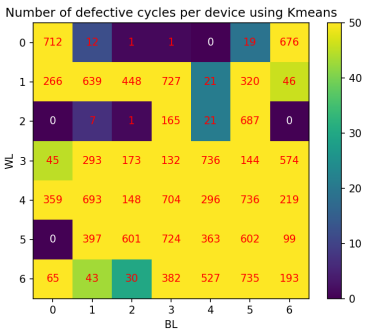
Figure 6.14: Result of the Kmeans clustering Figure 6.14a shows the number of correctly classified and wrongly classified cycles. Figure 6.14b shows the number of defective cycles for each device.

Figure 6.15 shows the result of the K-means algorithm in which the I-V cycles are processed as images. The algorithm performs the best for this algorithm as two clear clusters can be identified which can be separated by a straight line. Figure 6.15b shows the number of defective cycles for each device. From this we can see that the functional devices contain few defective cycles, while the defective devices such as $WL0BL0$ have more than 700 from the 736 cycles that are defective.

Figure 6.16 shows the performance for the different inputs. The green bar presents the percentage of cycles that are classified correctly and the red bar links the classified cycles back to the RRAM devices to determine the percentage of devices that are correctly classified as defective. The classifi-



(a) Visualization of the defective and functional cycles after K-means.



(b) Number of defective cycles for each device after applying K-means on raw data as input

Figure 6.15: Result of the Kmeans clustering Figure 6.15a shows the number of correctly classified and wrongly classified cycles. Figure 6.15b shows the number of defective cycles for each device.

cation algorithm is not 100% accurate as can be seen in Figure 6.16. 90% of the cycles are correctly classified when using the images as input. 70.6% of the cycles are correctly classified using the raw data as input and 63.3% of the cycles are correctly classified using the metrics. To link this back to the devices we have to incorporate a tolerance. This tolerance is based on the visual inspection of the heatmap as well as the percentage of cycles that has been classified correctly. For the images as input the number of defective cycles is set at 25 cycles. For the raw data the allowed number of defective cycles per device is set at 50 and for the metrics the number of defective devices is set at 1. The

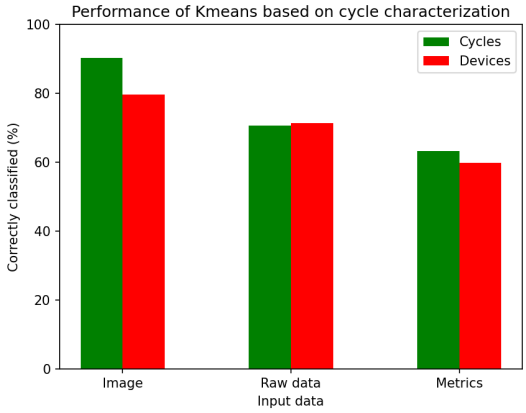
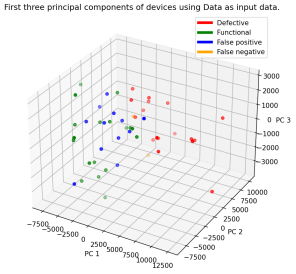


Figure 6.16: Performance of K-Means for different input data

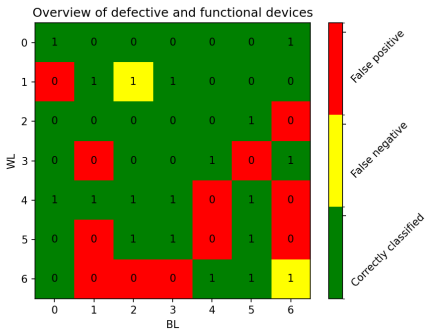
percentage of devices is slightly lower with 79.6% compared to 90% of the cycles but still outperform the raw data and metrics as input. When using Kmeans the images should be used as input data.

Device characterization

Applying K-Means on the PCA of the devices results in the following plot for each input set.Figure 6.18, Figure 6.17 and Figure 6.19 show the PCA plot of the first three principal components after K-Means clustering as well as a heatmap to evaluate the performance of the clustering algorithm. Figure 6.17b shows that the clustering algorithm results in two false negatives, twelve false positives and the rest is labelled correctly as functional or defective.



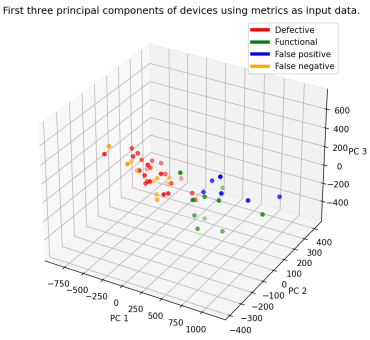
(a) Visualization of the defective and functional cycles after K-means.



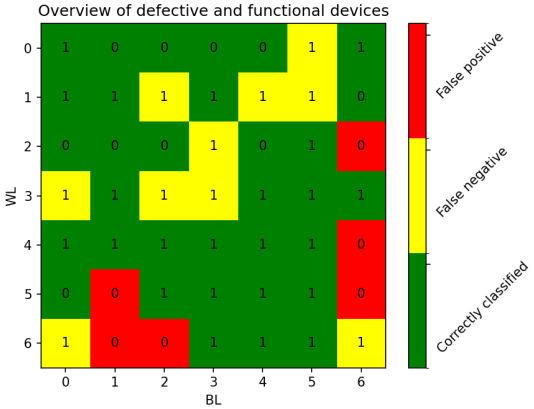
(b) Visualization of the defective and functional devices after K-means.

Figure 6.17: Kmeans clustering of PCA using images as input data.

Figure 6.18a shows that the clustering algorithm divides the devices over PC 1. As indicated by Figure 6.18b this will lead to 10 false negatives and 6 false positives.



(a) Visualization of the defective and functional cycles after K-means.

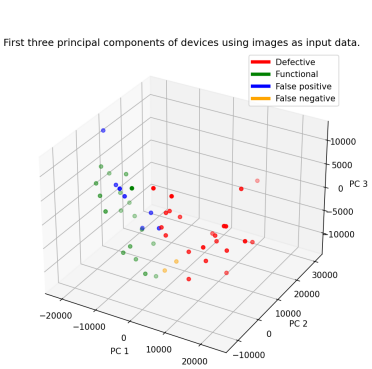


(b) Visualization of the defective and functional devices after K-means.

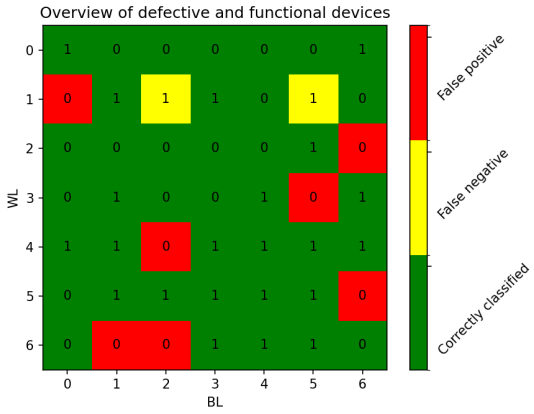
Figure 6.18: K-means clustering of PCA using images as input data.

Figure 6.19 seems to perform best for the K-Means algorithm. In total two devices are wrongly classified as functional and 7 devices are wrongly labelled as functional.

Figure 6.20 shows the performance of each input set using K-Means on the PCA results of each device. The algorithm classifies 81.6% using images as input data, 71.6% when the raw data is used as input and 67.3% when the metrics are used as input. The percentage of correctly classified devices is lower for the metrics compared to the raw data. As section 4.4 showed the predefined criteria are too strict and the number of false negatives is much larger. However, the number of false positives is 50% lower. The results need to be further analyzed to determine whether we need to incorporate additional metrics such as the switching time or perhaps some of the metrics are redundant and need to be removed to decreased the number of false negatives. The algorithm which uses images as input data performs the best and gives the fewest false positives and negatives. Based on these results the spatial information provided by the images is relevant to the classification algorithm.



(a) Visualization of the defective and functional cycles after K-means.



(b) Visualization of the defective and functional devices after K-means.

Figure 6.19: Kmeans clustering of PCA using images as input data.

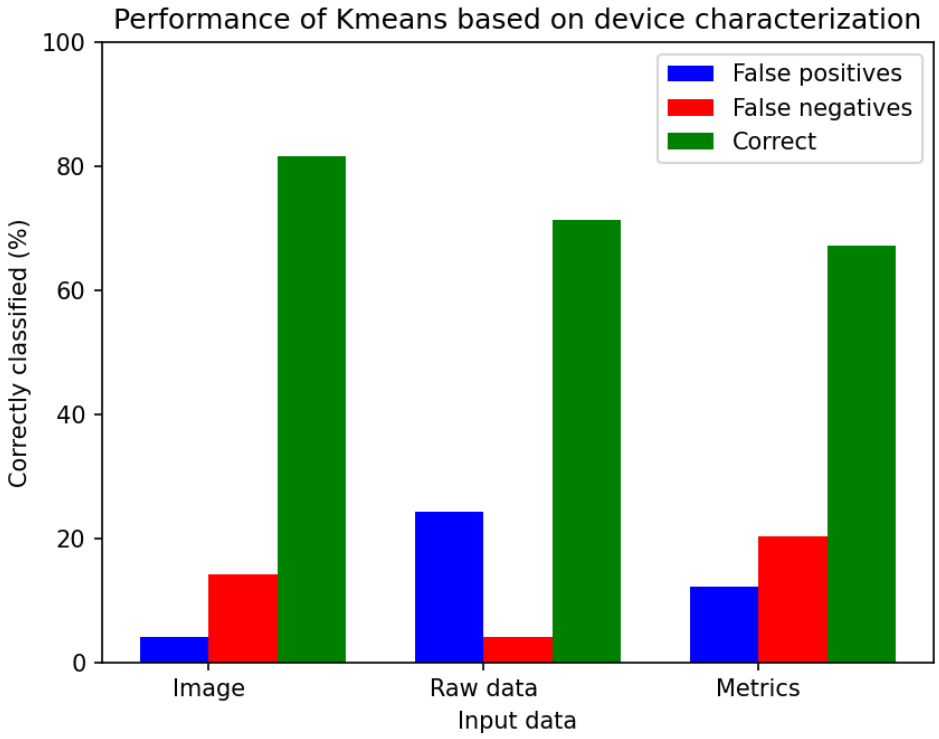


Figure 6.20: Performance of K-Means for different input data

6.3. Supervised learning

The algorithm is used to automatically classify defective and functional cycles, which are then linked to the corresponding device. We only have 49 devices which is too small of a dataset to split in a training and test set for such a complex problem. As a result, we will only use the supervised learning algorithms to classify the cycles of RRAM devices. These will then be linked back to the RRAM devices.

6.3.1. K-Nearest Neighbours

The performance of each input is shown in Figure 6.24. The results of the K-NN classifier in which the PCA analysis of the images are used as input are shown in Figure 6.21. Figure 6.22 shows the results in which the PCA analysis of the metrics is used as input and Figure 6.23 does this for the PCA analysis of the raw data.

Figure 6.21 shows that the cycles can be used as an indication to identify which devices are defective and which are not. Based on the results we set the tolerance of the number of defective cycles allowed per device at 30. If we link this to the results from the manual labelling then 87.8% of the devices can correctly be classified.

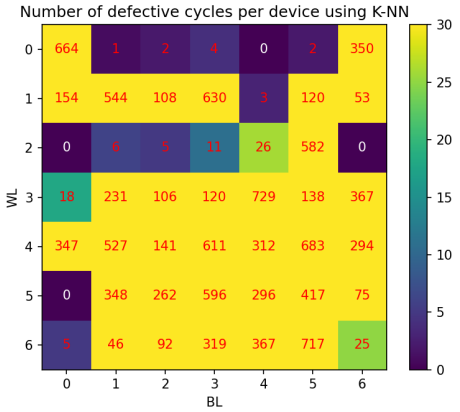


Figure 6.21: Number of defective cycles for each device using K-NN on image data.

For Figure 6.22 we set the tolerance at 80. This value is chosen based on the visual inspection of Figure 6.22. If we link this to the manual labels 79.6% of the devices are correctly classified.

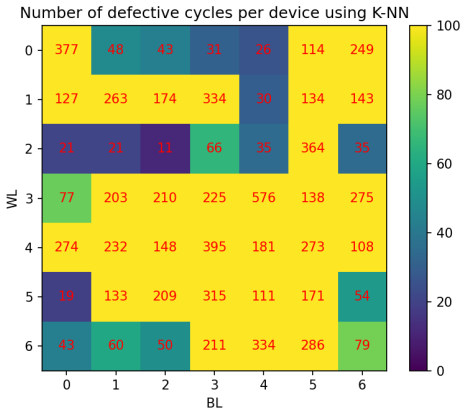


Figure 6.22: Number of defective cycles for each device using K-NN on the metrics.

For the raw data as input set the accepted tolerance is set Figure 6.23 at 50 defective cycles for each device. Above that the devices are labelled as defective and below that the devices are labelled as functional. 81.6% of the devices are classified correctly using the K-NN algorithm on the raw data as input.

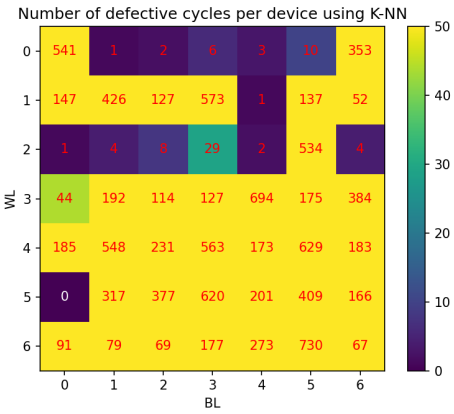


Figure 6.23: Number of defective cycles for each device using K-NN on raw data.

Figure 6.24 shows the performance of the K-NN algorithm using the different input sets. The images score the highest as 94% of the cycles are correctly labelled which translates to 84% of the devices. The raw data and metrics do not differ that much when looking at the number of devices that are correctly classified with 81.6% and 79.6% respectively. However, the number of cycles differs by 4% with 84% compared to 80% when the metrics are used as input.

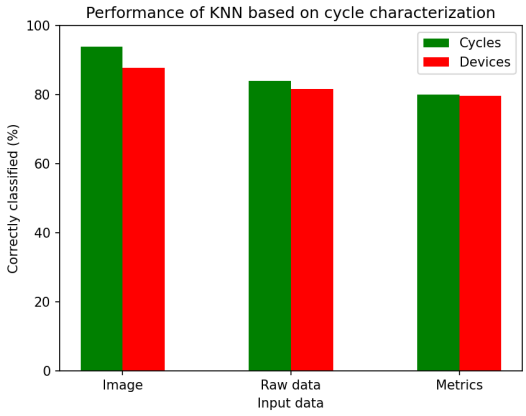


Figure 6.24: Number of defective cycles for each device using K-NN on the metrics.

Figure 6.22,Figure 6.23 and Figure 6.21 show that all devices on word line zero with the exception of those on bitline zero and six can be considered functional devices.

6.3.2. Convolutional neural network

For the CNN we implemented the algorithm as described by [83]. The architecture is described in subsection 5.3.4. 80% of the cycles were used to train the convolutional neural model. 10% was used to test the CNN and 10% was used for validation. In total 20 epochs were used to train the convolutional neural network. After training for 20 epochs the CNN was validated using the validation dataset. The CNN classified 66.5% of the cycles correctly. To improve the functionality of the CNN we need to

improve the complexity of the CNN by adding additional layers, training for more epochs or using a larger sample size.

6.4. Summary

A statistical analysis was done on the HRS, LRS, V_{set}, V_{reset} and the R_{ratio}. Furthermore, the dynamic time warping and euclidean algorithm is applied to a model I-V curve based on the manually labelled data. Three machine learning algorithms have been implemented: Kmeans, K-NN and a convolutional neural network. The statistical analysis of the individual metrics did not result in any viable results and none of the metrics were able to identify devices without detecting multiple false positives. V_{set} and V_{reset} are crucial metrics as the euclidean distance algorithm outperformed the dynamic time algorithm in which 81% of the devices are correctly classified compared to 70% for the DTW. The euclidean distance algorithm is not reliable enough to accurately classify RRAM devices but can be used as an initial data analysis for further processing. However, when the data is not labelled it is better to use the K-Means algorithm compared to the Model I-V curve and statistical analysis. The K-Means algorithm also performs best when the images are used as input data in which 90% of the cycles translating to 79.6% of the devices when the cycles are linked back to the device. The raw data and metrics perform worse with 71.4% and 59.6% respectively. First adding the principal components of each cycle for each device and then applying the Kmeans algorithm works as well as applying the algorithm on the individual cycles. 81.6% of the devices are correctly classified when the images are used as input. 71.6% when the raw data is used as input and 67.3% when the metrics are used as input. First combining the principal components for each device is better than linking the cycles back to the device afterwards. The K-NN algorithm classifies 94% of the cycles correctly and 84% of the devices when the images are used as input. The raw data and metrics do not differ that much when looking at the number of devices that are correctly classified with 81.6% and 79.6% respectively. The CNN classified 66.5% of the devices correctly. The image data as input scores the best and should be used when assessing the quality of the RRAM devices. If you have labelled data the K-NN is the best solution and should be used as the method is fast. However, the labelling of data is time consuming and can be challenging due to the device variability. In that case the K-means algorithm can be used for a quick analysis of the RRAM devices as it will already classify 90% of the cycles and 84% of the devices correctly. The CNN does not perform as well as expected but we think that if the CNN is optimized and tuned it can perform as well as the K-NN.

7 Discussion

This chapter discusses the validity of the work of this thesis work. First, the methods to extract the electrical parameters and the manual labelling of the device are discussed. After which the approach and the algorithms for RRAM classification are evaluated. The last section consists of the contribution of this masters work and suggestions for future research.

7.1. RRAM Data analytics

The RRAM data analysis as well as the statistical analysis of the results required the extraction of the electrical parameters: V_{set}, V_{reset}, HRS, LRS, $t_{H \Rightarrow L}$ and $t_{L \Rightarrow H}$. For all metrics the extraction technique was robust with the exception of a few edge cases. Additional, boundary conditions should be added to catch those boundary conditions as they affect the outlier detection algorithm as well as the K-means clustering. The method to extract the switching time is commonly done using an oscilloscope by applying pulsed voltage stresses. The electrical noise makes it challenging to determine a universal end point for the switching time for both from high resistive state to low resistive state and vice versa.

Furthermore, the data were not labelled. We designed a framework to label the individual cycles based on the current knowledge about the switching characteristics of RRAM devices. Kocak, Mitard, and Naskali did a similar approach in which the test data-set of MOSFETS was classified by researchers [83]. They concluded that the accuracy lies around 85% for a junior researcher and 92% for a expert researcher. To evaluate the performance of the classification algorithms we have also labelled the devices manually. Classifying RRAM devices using the opinion of a researcher is just as or maybe even more difficult than assessing the functionality of MOSFETs as we have less experience with RRAM. As a result, the method we have proposed to manually label RRAM cycles is not 100% accurate. Especially, because it is not yet fully understood how precisely a defect affect the electrical parameters. The manual labelling of the device, but additional data or devices with known defects should be evaluated using these methods to determine the performance of the algorithm.

7.2. Classification algorithm

The different classification algorithms provides an initial analysis of which devices are defective and which are not. The current method using the classification of individual I-V cycles which are linked to the devices. The cycles are classified independently from one another and the algorithm does not know to which device the cycle belongs. Ideally, the information about this is known and presented as a time series so that the information from other cycles of the same device are incorporated more efficiently in the classification of the RRAM device. However, the dataset consists of 49 RRAM devices are all from the same wafer. More devices from different wafers are required to validate the functionality of the classification algorithms.

7.3. Value of this work

This work presents a cheap method to automatically classify RRAM devices as defective or functional. The machine learning algorithms can be used as an initial classification algorithm to identify defective

RRAM devices. After, this further characterization of the defective RRAM devices is required to enable the origin of the defect. For this more expensive methods such as optical characterization can be used or the visual examination of the individual I-V cycles. This work can be used as a foundation for further analysis of RRAM devices so that accurate defect models can be built for which new tests can be generated.

Additionally, the software used for this thesis work can be used to quickly characterize and identify defective RRAM devices. Further improvements of the classification methods or larger datasets to train the K-NN algorithm can improve the classification of RRAM devices. The classification method can be used to speed up the labelling of RRAM which can be used for the diagnosis of RRAM devices.

7.4. Future work

In the future, the work can be extended so that it can also identify which defect is present in the RRAM device. Currently, the algorithms only consists of two classes: defective and functional. Adding multiple classes for specific defects could make this possible. Additionally, the architecture of the CNN algorithm is directly copied from Kocak, Mitard, and Naskali and the training data we have is limited [83]. A more elaborate CNN architecture might be required consisting of additional layers, different tuning parameters or more epochs might give better results. However, due to time and the complexity of the CNN architecture this has not yet been explored completely and further analysis is required.

The electrical characterization of RRAM devices using machine learning looks promising and is much cheaper compared to optical characterization and memory tests. If in the future the defective devices can be linked to the underlying defect, this will lead to cheaper diagnosis of RRAM devices and allow the creation of accurate fault models.

8

Conclusion

This work focused on the automatic characterization of RRAM devices using electrical characterization. The software package allows the automatic identification of defective RRAM devices which is faster and cheaper than optical characterization. In the future the package could be elaborated so that it does not only indicate which device is defective but can also identify the defect that caused the abnormal behaviour.

Initially, the background information as well as a comparison is provided between the current and emerging memory technologies. Additionally, the manufacturing process of RRAM, the defects that can occur and how these defects affect the electrical parameters of RRAM are discussed. Then the state-of-the-art in defect identification and diagnosis is discussed in which a distinction was made between optical characterization, electrical characterization and memory testing.

The state-of-the-art highlighted the need for a cheap and cost-effective method to identify defects in RRAM devices. Optical characterization is expensive and in some cases destructive and memory tests are an abstraction of defects and are difficult to link back to the actual defect. Where electrical characterization has mainly been used to describe the behaviour of the RRAM device and how design choices affect this behaviour.

The electrical characterization has so far been done using the electrical parameters such as the switching voltage, switching time and the resistance in the high and low resistance state. Chapter 4 showed that the hardware specification were insufficient to identify defective RRAM devices and proposed a method to manually label RRAM cycles and devices which can be used for comparison and as a training set for supervised learning algorithms. The results from the manual labelling showed that 29 from the 49 devices did not behave as expected. The characterization of the electrical parameters in combination with the manual labelling of the RRAM cycles showed that there was a difference between the values of the electrical parameters for defective and functional RRAM devices.

Chapter 6 continued on this by doing a statistical analysis using the electrical parameters commonly used for RRAM characterization to identify defective RRAM devices. The analysis showed that the metrics were insufficient to identify defective devices and cannot account for the cycle-to-cycle variance of the RRAM device. The comparison between a model I-V curve and the test data using the euclidean distance resulted in 81% of the devices that can be correctly classified.

As the manual labelling is time consuming we also investigated the performance of the K-Means algorithm. When the I-V cycles were stored as images we showed that the algorithm can correctly classify 90% of the cycles correct and 79.6% of the devices are correctly classified. Furthermore, because we have labelled data we also evaluated the performance of two supervised algorithms: K-NN and a CNN. The K-NN is able to classify 90% of the cycles correctly which translates to 84% of the devices. The CNN classified 67% of the cycles correctly. The CNN has not yet been linked to the devices because the CNN has not been optimized yet and needs further improvement by changing the architecture of using more epochs before we can assess the performance of the CNN for the identification of defective RRAM devices.

This work forms the basis of using electrical tests to automatically identify defective RRAM devices and shows the relevance of machine learning algorithms in defect identification of RRAM.

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