Electrostatic Dust Removal System for a Lunar Rover Solar Panel Assembly

Electronics Design

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TU Delft

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to obtain the degree of Bachelor of Science
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Preface

The aim of this project is to create a system that uses electrostatic forces to remove dust particles from the surface of a lunar rover, offering a simple and effective solution to the problem of dust accumulation. This thesis presents the design and implementation of the driving circuit for the electrostatic dust removal system, demonstrating the feasibility of the system and its potential for improving the performance and longevity of lunar rovers. The thesis outlines the constraints faced by the researchers during the design and implementation of the system, as well as the solutions developed to address these constraints.

We would like to express our sincere gratitude to our supervisor, Dr. ir. C.J.M. Verhoeven, for his invaluable guidance and support throughout the project. His expertise and insights were instrumental in the success of the project.

We would also like to thank Dr. M. Ghaffarian Niasar and Dr. A. Shekhar for their valuable feedback and contributions to the project. Their expertise and insights helped us to overcome many of the challenges we faced during the project.

We would like to extend a special thanks to Floris van Mourik, Head of Electronics of Lunar Zebro who proposed this research and provided us with invaluable assistance throughout the project.

Tycho Appelman, Carli Bruinsma, Anass Ouaissa
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Abstract

Lunar dust presents a serious problem for future lunar rovers. Due to the charged nature of this fine dust, it tends to stick to sensitive elements like solar panels. It is clear that a system needs to be implemented in order to remove lunar dust to keep the output power of the solar panel at a satisfactory level. This paper develops the proof of concept electronics for a method sometimes called an electrodynamic screen, that uses electrostatic fields to sweep away the dust adhered to the surface of the solar panel. The electronics for this system needs to produce a high voltage three phase pulse wave in order to drive the electrodes placed on top of the solar panel. The design of the electrodes themselves are not part of this thesis, but it is the main subject of the companion thesis produced by other members of our group.

Contents

1 Introduction

The harsh environment on the Moon poses significant challenges to the operation of lunar rovers [1]. One of the most pressing challenges is the accumulation of dust on critical components, such as solar panels and mechanical parts. The problem of dust accumulation on lunar rovers is a significant challenge that can severely degrade their performance and longevity. The lunar environment is characterized by a lack of atmosphere, extreme temperatures, and exposure to space radiation, which makes it particularly harsh for mechanical and electrical systems. The dust on the Moon is also very fine and abrasive, which can cause damage to critical components such as solar panels, radiators, and mechanical joints.

The dust on the Moon is created by a variety of processes, including meteorite impacts, solar wind, and micrometeoroid bombardment [1]. The dust particles are very small, ranging in size from a few micrometres to several millimetres, and can be easily lifted by the slightest disturbance, such as the movement of a rover wheel [2]. Once the dust settles on a surface, it can be difficult to remove, as it tends to adhere strongly due to the lack of atmosphere and the electrostatic charges that build up on the surface. The accumulation of dust on the rover's solar panels is an urgent issue, as it can significantly reduce the amount of energy generated by the rover [3]. This can restrict the rover's operational range, durability, and ability to conduct scientific experiments. Dust accumulation on mechanical components can also be problematic, as it can impede the movement of joints and gears, leading to eventual failure.

While several solutions exist to mitigate this problem, each has its own limitations and drawbacks. Slowing down the rover's speed can help mitigate dust disturbance, but it does not prevent the settling of dust on the rover. Special materials can help to reduce the adhesion of dust, but they do not actively remove it from the surface. Gas dispensers are not a viable option because they run out, and water cleaners do not work in vacuum conditions because the water would boil immediately, and run out, too. Brushing can create scratches and further exacerbate the problem, while mechanical parts can be destroyed by dust.

A team of students at the Delft University of Technology has developed an electrostatic dust removal system for lunar rovers to resolve this issue. The system utilizes electrostatic forces to remove dust particles from the rover's surface, providing a straightforward and effective solution to the dust accumulation problem. This thesis describes the design and implementation of the electric driving circuit for the electrostatic dust removal system, demonstrating the system's viability and its potential to enhance the performance and longevity of lunar rovers. Specifically, this project focuses on the *Lunar Zebro* [4], which is a Moon rover fully developed by students of the TU Delft and uses a special locomotion system without wheels.

1.1. Problem Statement

Past space missions conducted without effective dust removal systems have faced rapid equipment degradation due to the adhesion of lunar dust. [5]. Nowadays, different dust removal systems are implemented in space missions. First, the rover *Zhurong* that landed on Mars in 2021 mitigates the adhesion of dust with a special coating [6]. However, the rover did not wake up after its hibernation in December 2022 after it was affected by a dust storm. Second, NASA's rover *Curiosity* has explored the surface of Mars since 2012 and implemented a dust removal system based on a moving brush for the first time [7]. It is still active in June 2023. Although different dust removal systems have been implemented in space missions, an electrostatic curtain has never been used in space, yet. Despite its widely acknowledged potential, it is a solution that still lies in the future. An electrostatic dust removal system also seems the optimal solution for the small *Lunar Zebro* Moon rover, due to its efficiency and lack of moving parts.

Most electrostatic dust removal systems use an electric curtain to sweep adhered dust particles away [8][9][10]. In these types of systems, multiple groups of parallel electrodes create a non-uniform electric field that is strong enough to repel the adhered dust. The field can be dynamically adjusted to make it travel along the electrode surface. Appropriate electronics are needed to drive the electrodes. Not only does the creation of the appropriate waveform matter but most importantly the voltages on the electrodes need to be in the range of kilovolts to create a field that is strong enough to repel the adhered dust [11]. The radiation, temperature and vacuum on the lunar surface [1] create an extra challenge, as well as the limited size of the *Lunar Zebro*. Thus, the central question that this thesis hopes to answer is:

Is it possible to create driver electronics for an electrostatic dust removal system for the Lunar Zebro*?*

1.2. Existing Technologies

While several solutions exist to mitigate this problem, each has its own limitations and drawbacks. Driving slower is a possible solution, but it does not prevent dust from swirling in the air and settling on the rover. This is because the Moon's atmosphere also contains dust [8]. Special materials can help to reduce the adhesion of dust, but they do not actively remove it from the surface. Gas dispensers are not a viable option because they run out, and water cleaners do not work in vacuum conditions because the water boils immediately. Brushing can create scratches and further exacerbate the problem, while mechanical parts can be destroyed by dust.

Of course, it is optimal to prevent lunar particles from ever reaching solar panels. The more lunar material that falls on a solar panel, the more difficult it is to remove it electrostatically. Therefore, the first mission is to prevent as much lunar material as possible from landing on the solar panels. In a simulation described by Gao (2023) [3], the lunar dust rising direction was opposing the driving direction. The higher the speed, the higher the lunar dust rose and the larger the impact on the solar panels was.

When it comes to actively removing dust particles from solar panels and optical elements using electric fields, there are several methods. The first is using electrostatic travelling waves. This method comprises a cleansing system that generates four-phase high voltage and utilizes a particle conveyor with parallel electrodes to transport particles away from the surface [8]. The system can likely be designed to be small, lightweight, highly transparent, and energy efficient. Furthermore, it was built on top of previous research that determined that the rectangular waveform is more effective than a square or sinusoidal wave at transporting particles using electrostatic travelling waves [12]. This is because synchronized particle movement requires a finite amount of time. The sharp rise and fall times of the rectangular waveform give the particles more time to jump and move forward with the wave. In addition, it was discovered that the transport rate was highest at low frequencies, specifically less than $100 - 200\,\mathrm{Hz}$.

Another system consisted of a device that generates an electric field between two electrodes and charges the dust particles on the solar panel's surface [13]. The charged particles are then attracted to an electrode with an opposite charge and removed from the panel's surface. On the surface of the solar panel, the electrodes are arranged in a specific pattern, and the electric field generated by the electrodes is designed to be strong enough to charge dust particles without damaging the solar panel. The research describes that an investigation of the optimal voltage to remove particles determined $2.8\,\mathrm{kV}_{pp}$ for low voltage, while $11.8\,\mathrm{kV}_{pp}$ was sufficient to move particles continually. It has been

demonstrated that electrostatic cleaning effectively removes dust and similar debris (except algae) from the surface of solar panels.

1.3. Goal and Scope of the Project

This project's objective is to design and produce the first version of the driving circuit for a lunar rover electrostatic dust removal system. The project's scope is restricted to the design of the driver electronics and high-voltage supply, but not the electrode design. The objective of the project is to demonstrate the viability of the system by demonstrating that simple electronics can reliably achieve the intended result.

The scope of the project includes the design and implementation of the driver electronics and the high-voltage supply for the electrostatic dust removal system. The driver electronics are responsible for generating a three-phase rectangular waveform with adjustable frequency and duty cycle, while the high-voltage supply provides at least $1\,\mathrm{kV}$ to power the drivers. The project does not include the design of the electrodes themselves.

Overall, the electrostatic dust removal system developed for lunar rovers has the potential to address a wide range of environmental and industrial challenges on Earth. With further research and development, the system could become a valuable tool for improving the sustainability and efficiency of various processes and industries.

The project's performance will be determined by well-defined, SMART (Specific, Measurable, Attainable, Realistic, Time-bound) criteria. These criteria include the system's performance in terms of dust removal efficacy, energy consumption, and dependability, as well as the design's practicability and adherence to the project schedule. With this thesis, we have at least a proof of concept for the electrostatic dust removal system, and it has a great deal of potential, so additional research should be conducted.

1.3.1. Constraints

The constraints of the project are described. These constraints must be considered in the design and implementation of the electrostatic dust removal system, as they can significantly affect its performance and dependability.

The lunar environment is characterized by a high level of radiation[14], which can damage electronic components and degrade their performance over time. The electrostatic dust removal system must be designed to withstand this radiation and operate reliably in this environment.

The lunar environment is also characterized by a vacuum, which can affect the behaviour of electrical and mechanical systems [2]. The electrostatic dust removal system must be designed to operate reliably in this vacuum environment, without the need for external cooling or lubrication.

The lunar environment is subject to extreme temperature fluctuations, ranging from $-157^{\circ}\mathrm{C}$ to $114^{\circ}\mathrm{C}$ [15]. The electrostatic dust removal system must be designed to operate reliably over this temperature range, without the need for external heating or cooling.

The electrostatic dust removal system relies on high-voltage electrical fields to remove dust particles from the surface of the rover. The system must be designed to generate and maintain these high voltages in a safe and reliable manner, without posing a risk to the rover or its components.

The dust removal system must be designed to operate within the power constraints of the lunar rover. This requires careful consideration of the power consumption of the system, as well as the efficiency of the components and the overall design.

The system must be designed to minimize electromagnetic interference with other systems on the lunar rover. This requires careful shielding and grounding of the system, as well as the use of appropriate filtering and isolation techniques.

Overall, these constraints represent significant challenges that must be addressed during the design and implementation of our electrostatic dust removal system. By taking these constraints into account, we can design a system that can operate reliably in the harsh lunar environment.

1.4. Thesis Overview

The outline of this thesis is as follows. Chapter 2 provides a summary of all requirements for the prototype developed. There are two types of requirements: mandatory requirements and trade-off requirements. Table 2.1 outlines all prototype requirements, and the chapter provides brief justifications for the most essential ones. Chapter 3 describes the system subdivision design for the electrostatic dust removal system, including the electrode design and driver electronics. We subdivide the driver electronics into three subsystems: the driver, the controller and the high-voltage generator. The chapter also provides a concise summary of each subsystem's responsibilities. Afterwards, Chapter 4 will discuss the design of the system's three controllers. The final driver design and component selection are then presented. Chapter 5 describes the design of the controller for the electrostatic dust removal system, including the control algorithm and the failure detection mechanism. It also presents the simulation and testing results. Chapter 6 describes the design of the high-voltage supply for the electrostatic dust removal system, including specific requirements and their justification. It also makes suggestions about further improvements. Afterwards in Chapter 7 we outline the different types of testing and validation that were performed on the system and presents the overall performance evaluation. Finally in Chapter 8 we summarize our thesis' key findings and contributions. The limitations and potential for future enhancements and expansions of the electrostatic dust removal system are also discussed. We conclude with suggestions for future research and development in this field.

2

Programme of Requirements

This chapter summarizes all requirements for the prototype constructed in this thesis. The requirements consist of two types. First, the system must meet the mandatory requirements (MR) at the end of the project. Second, the prototype should meet the trade-off requirements (ToR), but this is not necessary for considering the project successful. Table 2.1 lists all requirements for the prototype. We will now provide a short motivation for the most important ones. [8] concludes that a rectangular wave is the most efficient waveform for driving an array of electrodes to generate an electric curtain, which is our motivation for requirement MR-F1. This requirement also states that the system should output a three-phase rectangular waveform. The number of output phases is agreed upon with the team designing the electrodes, as the electrodes will consist of three interconnected sets. MR-P1 and MR-P2 state that the frequency and duty cycle of the rectangular wave must be adjustable to allow experimentation with different settings. We based the ranges on the conclusions of [8]. The short rise and fall times of MR-P5 are unnecessary for dust removal but create the possibility of generating very short rectangular pulses, which adds to the testing possibilities. MR-P3 sets a minimum for the required voltage. [8] shows that dust removal systems yield good results with this voltage. However, extrapolating the results of [8] implies that higher voltages could have even better dust removal results. ToR-P3 is present as it is still unknown what kind of electrodes the system will have and what the minimum voltage the electrodes require to generate forces of sufficient magnitude. MR-C1 sets a maximum power consumption for the system. The power limit is based on the power budget of the *Lunar Zebro*: 15W in total. The chosen limit is quite a significant fraction of this budget, but as the dust removal system will only be used for short amounts of time and therefore the average consumption will be much lower, as the system will mostly be turned off. Requirement MR-C3 puts a limit on the sizes of the used components. The goal is to design a system that fits in the *Lunar Zebro*. However, in technical requirements, a maximum PCB size is a more common way to define a physical size maximum. As this project focuses on creating a prototype for assessing feasibility and includes experimentation with different settings, the total prototype size is not a concern. To allow for size minimization in later design iterations without wasting resources on minimizing the prototype, we MR-C3 in this way.

MR-I1 forces the system to use an external $12\,\mathrm{V}$ power supply, which complies with the current conventions within the *Lunar Zebro* team. Lastly, MR-I3 implies the usage of a microcontroller in the design. We based this choice on the need for rapid prototyping and because of its implementation possibilities in a final system. Microcontrollers are very convenient for generating accurately timed signals.

ID	Type	Description	Validation
MR-F1	Functional	The system must generate a 3-phase high-voltage block wave that can generate an electric curtain on the electrodes.	Inspection
MR-P1	Performance	The pulse width must be adjustable within the range of $500\,\mu$s up to $500\,\mu$s less than the wave period.	Measurment
MR-P2	Performance	The frequency of the block wave must be adjustable between $1\,\mathrm{Hz}$ and $100\,\mathrm{Hz}$.	Measurement
MR-P3	Performance	The block wave must have an amplitude of at least $1\,\mathrm{kV}$.	Measurement
ToR-P3	Performance	The system should be adaptable by only changing components or settings to create amplitudes that are as high as possible.	Analysis
MR-P4	Performance	The ripple voltage of the block wave shall be smaller than 5%.	Measurement
MR-P5	Performance	The rise and fall time of the block waves shall be smaller than $50\,\mu\mathrm{s}$.	Measurement
MR-C1	Constraint	The system must consume less than $3\mathrm{W}$ from the power supply for all possible frequencies and duty cycles.	Measurement
ToR-C1	Constraint	The system should consume as little power through both controller and power channels.	Inspection
MR-C2	Constraint	The prototype must be completed within 8 weeks.	Inspection
MR-C3	Constraint	The system shall only use components smaller than $2 \times 2 \times 1\,\mathrm{cm}$ or components that can be replaced by a component of $2 \times 2 \times 1\,\mathrm{cm}$.	Inspection
MR-S1	Safety	Any failure of the high-voltage part shall leave the rest of the system intact.	Analysis
MR-S2	Safety	The maximum energy in the system in the form of electric charge shall be below $0.5\,\mathrm{J}$ to avoid the risk of a lethal electric shock [16].	Analysis
MR-S3	Safety	The accidental disconnection of a jumper wire must leave the system intact.	Measurement
MR-I1	Interface	The system shall be powered by an external $12\,\mathrm{V}$ source.	Inspection
MR-I2	Interface	The system must have three outputs that connect to the three groups of electrodes.	Inspection
MR-I3	Interface	The duty cycle and frequency shall be controlled by reprogramming an in-system microcontroller.	Inspection

Table 2.1: Requirements for the prototype designed in this thesis.

3

System Subdivision Design

This chapter will elaborate on different possible solutions for the subdivision of the system into multiple subsystems. We will first derive a top-level subdivision based on interface requirements and then look at different options for the black box within this subsystem. At the end of this chapter, we will introduce the system subdivision of the final prototype.

3.1. Top-level System Subdivision

The interface requirements of table 2.1 are our point of entry to dividing the system into subsystems. The system has 3 connections: a programming link which connects to a microcontroller in the system, a $12\,\mathrm{V}$ power supply and a 3-phase output to connect to the electrodes. As the output voltage must be at least $1\,\mathrm{kV}$ by MR-P3, we quickly see the need for another electronic subsystem with two functions. First, the system must create at least $1\,\mathrm{kV}$ with energy from the $12\,\mathrm{V}$ power supply. Second, the subsystem must use this high voltage to create a three-phase rectangular wave at the output.

The timing must be controllable by the microcontroller. Depending on the specific solution, we must implement safety requirements MR-S1 and MR-S3 by feeding information back to the microcontroller about possible failures of the rest of the system.

3.2. Electronics Subdivision Design

The next step is to find an appropriate subdivision of the electronics into different subsystems. First, we will introduce labels $i \in I = \{1, 2, 3\}$ for each output connected to an interconnected set of electrodes. Appendix A derives that the load can be modelled as a single capacitor with capacitance C_i. The value of the capacitances will depend on the results of the team that designs the electrodes. In this report, we assume a value of $220\,\mathrm{pF}$ for each output, which is in line with their first rough estimations. Using this model, we can say that creating block waves requires charging a capacitor to make the output rise and discharging the capacitor to make it fall. Each output, therefore, needs its own network to charge and discharge the equivalent capacitor.

The charge networks must source the high voltage from an appropriate high-voltage supply. The high-voltage supply must create at least $1\,\mathrm{kV}$ to satisfy MR-P3 and can only use the $12\,\mathrm{V}$ power supply as its energy source. Two choices for system subdivisions arise: the charging networks can either share a single high-voltage supply or all contain their own. Hybrid versions of these options are left out of the scope, as this would introduce the need for too many components in a system that must — at the end — be as small as possible. The following section will compare the two options.

3.2.1. High-Voltage Generators: Separated or Shared

Section 6 about the high-voltage generator design concludes that a high-voltage generator will be responsible for most of the system's power consumption. ToR-C1 states that the power consumption must be as small as possible. We will now create a simple model to gain insights into the influence of the system layout choice on power consumption.

Suppose that a high-voltage generator consumes a static power of P_{gen} when it is turned on, and consumes an additional amount of energy E_{charge} for charging a single capacitor. As the generators only need to charge one capacitor at a time — a conclusion of appendix A — we assume that both systems can use similar high-voltage generators with equal parameters. We will assume that all output capacitances are approximately equal, and therefore E_{charge} can be considered equal for each phase.

Consider a system with three separate high-voltage generators for each phase, where charging an equivalent output capacitor simply means turning on the corresponding high-voltage generator and discharging it means turning it off combined with an extra discharge network to speed up the process. The high-voltage generators then consume a total power of $3P_{\text{gen}}D + 3fE_{\text{charge}}$, where D denotes the wave's duty cycle and f denotes the wave frequency. On the other hand, the system with one generator consumes a total power of $P_{\text{gen}} + 3fE_{\text{charge}}$ as the generator must be on permanently. To find conditions for which the system with three generators is more efficient than the other system, we solve $3P_{\text{gen}}D + 3fE_{\text{charge}} < P_{\text{gen}} + 3fE_{\text{charge}}$ and find that the system with three generators is only more efficient if $D < \frac{1}{3}$. because the model also neglects the energy consumption associated with turning on each power supply, which is worse for a system with three power supplies, we quickly see that a system with one power supply results in lower power consumption for most operating conditions of our system. Therefore, we chose a system with a single shared generator for the final design. Additionally, this choice could reduce the physical size of the final product

3.2.2. Final System Subdivision

Figure 3.1 summarizes the system subdivision visually. A summary of the tasks of each subsystem is as follows:

- The high-voltage generator generates at least $1\,\text{kV}$ from the $12\,\text{V}$ supply to power the drivers. Chapter 6 discusses its design.

- The driver, consisting of three separate charge and discharge or source and sink networks, connects to the three electrodes at the output. Chapter 4 discusses its design.

- The controller is responsible for making the driver function such that the desired waveform is present at the output. It is also responsible for safely operating the system. Reprogramming the controller allows changing the duty cycle and the frequency of the output wave. Chapter 5 discusses its design.

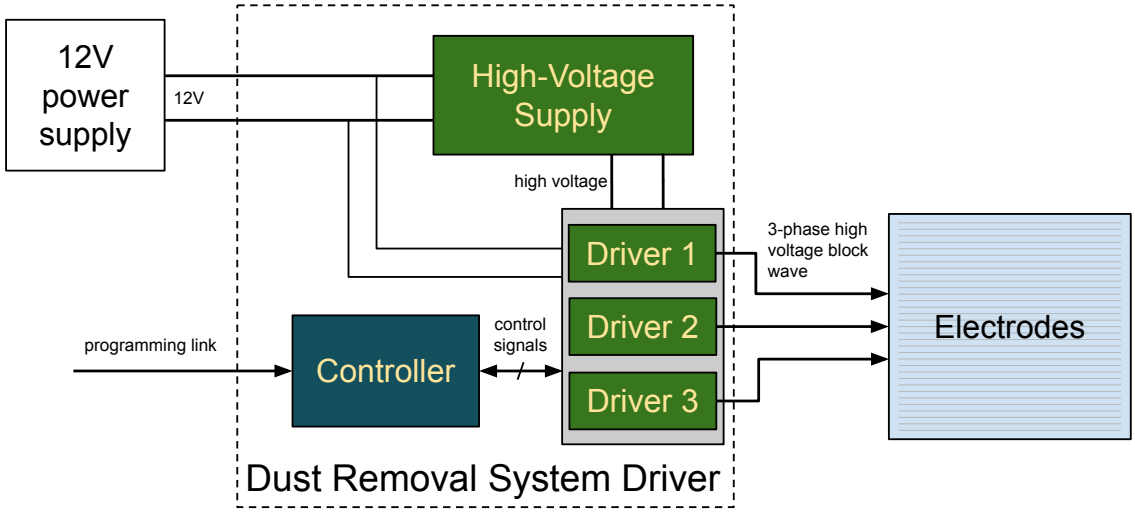


Figure 3.1: An overview of the entire system.

4

Design of the Driver

This chapter will concern the design of the three drivers in the system. First, we will derive requirements for the drivers from the system requirements. Then, we will discuss different solutions and their feasibility concerning the subsystem requirements. Afterwards, we present the final driver design and the component selection. A risk analysis of the final design will explain the implemented safety features of the prototype. Throughout this chapter, we will also perform a quick feasibility check concerning a lunar environment and provide recommendations for further iterations of the driver design.

4.1. Driver Requirements

Based on requirement MR-F1, the output must be a block wave, which induces the following classification of the states of an output, also described in appendix A.

- In the “low” state, the driver keeps the output voltage to $0\,\mathrm{V}$.
- In the “rising“ state, the driver brings the output from $0\,\mathrm{V}$ to a voltage V_H which is at least $1\,\mathrm{kV}$ by MR-P3 but preferably higher by ToR-P3. A single phase may rise for a maximum of $50\,\mu\mathrm{s}$ according to MR-P5.
- In the “high” state, the driver keeps the output at V_H with a ripple voltage of maximally 5% according to MR-P4. However, as most ripple voltage will come from the power supply, the ripple voltage must be much lower.
- In the “falling” state, the driver brings the output voltage back from V_H to $0\,\mathrm{V}$ within $50\,\mu\mathrm{s}$ according to MR-P5.

ToR-C1 states that the total power drawn from the microcontroller and the high-voltage generator must be minimal. Also, a failure in the high-voltage output part should not propagate back into the controller by MR-S1, which requires galvanic isolation in the high-voltage stage of both the charging and discharging network. Furthermore, a thorough analysis of failing components and accidentally loosened controller signal wires must provide insight into the required safety features to satisfy MR-S3 and avoid failures at the high-voltage side in the first place.

4.2. Design Options

Figure 4.1 shows a decomposition of the drawing of a single driver schematic based on the results of chapter 3, which state that the drivers must be able to charge and discharge the equivalent output capacitor through dedicated networks. We will now discuss different options for implementing the charging and discharging network. As the tasks are highly symmetric — charging concerns connecting the output to the high-voltage and discharging to the ground — we discuss all options without distinguishing the two functionalities.

4.2.1. Resistor

The simplest solution is to use a resistor to either charge or discharge the output capacitor passively. The resistor always connects the driver output to either the ground or the high-voltage generator. Figure

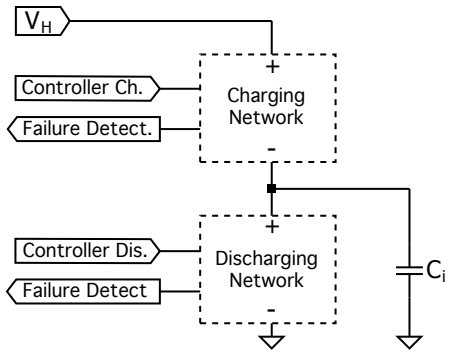


Figure 4.1: General structure of a single driver. Capacitor C_i represents the load which is an interconnected set of electrodes. A calculation method for the value of this capacitance is derived in appendix A in equation A.7.

4.2a shows a schematic of this solution. Only one of the two networks could implement this technique, as the system would otherwise be an uncontrollable voltage divider.

With a resistor as either a charging or discharging mechanism, the complementary network would be fully responsible for the controlled driving of the output. To assess the feasibility of this solution concerning the requirements, we first look at MR-P5, which puts a maximum on the rise and fall time of the output. For clarity, we only consider the case of a rise with the resistive network acting as a charging network, as the other placements of the resistor or a falling analysis yield similar results. In the ideal case, the complementary discharge network would instantly change from a closed circuit to an open circuit and analysis of the unit step response quantizes the rise time t_r. The electrical model of this situation consists of the discharging resistor with resistance R, the output capacitor and a voltage source stepping from 0 to V_H at time 0 in series in a closed loop. By mesh analysis, we find the current $I(t)$ through the loop to satisfy the following differential equation:

$$V_H u(t) = RI(t) + \frac{1}{C_i}\int_{-\infty}^{t} I(t')dt' \tag{4.1}$$

Here, $u(t)$ denotes the Heaviside unit step function. Solving this by separation of variables with initial conditions for the capacitor voltage $V_C(t)$ at time $t = 0$ returns a closed expression for $I(t)$. The output voltage is equal to the voltage over the capacitor and therefore equal to $V_o(t) = \frac{1}{C_i}\int_{-\infty}^{t} I(t')dt'$ and the following solution for the output voltage appears:

$$V_o(t) = V_C(t) = V_H\left(1 - e^{-\frac{t}{RC_i}}\right) \tag{4.2}$$

Requirement MR-P4 defines a maximum ripple voltage of 5%. We, therefore, define the end of a rise when the output reaches a voltage of 95% of V_H. In the context of equation 4.2, we find the rise time t_r by filling in $V_o(t_r) = 0.95V_H$:

$$t_r = -RC\ln(0.05) \approx 3RC \tag{4.3}$$

Note that we will measure the final rise time between 10% and 90% of the high voltage. Requirement MR-P1 states that $t_r \leq 50 \times 10^{-6}\,\mathrm{s}$, which poses a maximum value on the resistor value, which is

$$R \leq \frac{50 \times 10^{-6}}{3C_i} \tag{4.4}$$

With $C_i \approx 220\,\mathrm{pF}$, the maximum resistor value will be somewhere around $75\,\mathrm{k\Omega}$.

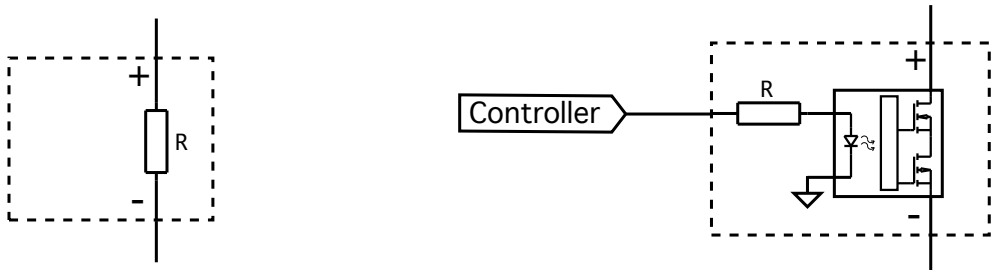
We will now look at the power consumption of the system. The power dissipated in a resistor with a voltage of V_H across its terminals is equal to $P_R = \frac{V_H^2}{R}$. If with a resistance equal to the maximum value of approximately $75\,\mathrm{k\Omega}$ and V_H equal to its minimum of $1000\,\mathrm{V}$, the power dissipated is $13.3\,\mathrm{W}$, which

is far above the maximum allowed power consumption of the entire system. However, the resistor only dissipates this power when a voltage is present across the resistor. We conclude that when the output waves are extremely short pulses, a resistor as a discharge network could provide a suitable solution. But due to the wide range of duty cycles required to satisfy MR-P1, we conclude that a resistor is not a working solution. Still, the analysis of this network provided some insights that are very useful for the rest of this chapter.

4.2.2. PhotoMOS-Relay

[8] uses photoMOS relays from Panasonic for high-voltage switching in a similar dust removal system. They propose these components for the implementation of a lightweight space-grade dust removal system. Panasonic, one of the leading manufacturers of photoMOS relays, explains in a blog on their website that "A PhotoMOS is a semiconductor relay with an LED as an input and MOSFET as an output" [17]. PhotoMOS relays have MOSFETs at their output which solves the problem of arcing found in the widely-used electro-mechanical relays. This difference allows switching at high voltages with only a few small components. PhotoMOS relays are also known for their high switching speed. Additionally, they provide galvanic isolation between the high-voltage stage and the low-voltage parts of the circuit connected to all sensitive electronics of the rest of the system, which immediately makes the driver meet MR-S1.

Most photoMOS relays are typically suitable for switching voltages of a few hundred volts. The maximum voltage of the photoMOS technology of Panasonic goes up to $1.5\,\mathrm{kV}$, which satisfies MR-P3. However, the required high-voltage level was still unknown until halfway through the project. Hence, in compliance with ToR-P3, we decided to design a system with an output amplitude scalable to a few kilovolts by only replacing single components. We conclude that photoMOS relays are out of the scope of the current prototype. Still, when the system properly works with voltages lower than $1.5\,\mathrm{kV}$, photoMOS relays are very recommendable for future iterations. Figure 4.2b shows a schematic of an implementation of a photoMOS relay as a charge or discharge network.



(a) Resistor network.

(b) PhotoMOS network.

Figure 4.2: Two optional implementations of charge and discharge networks in figure 4.1.

4.2.3. High-Voltage N-type MOSFET

Another option is to use a high-voltage N-type MOSFET. These components are available for maximum drain-source voltages of multiple kilovolts. A schematic of its implementation is shown in figure 4.3. The N-type MOSFET implementation works as follows: when the gate-source voltage is 0, the MOSFET is turned off and does not conduct. Only some minor leakage currents could be present. When the gate-source voltage increases to a value above the threshold voltage V_{Th}, the transistor turns on and arrives in the saturation region if the drain-source voltage is sufficiently high. This will be the case, as the drain-source voltage will be in the kilovolts range. After the MOSFET is turned on, the drain-source voltage quickly decreases when the capacitor either charges or discharges, moving the MOSFET into the ohmic region.

To assess the rise and fall time of a MOSFET charging or discharging the load capacitor, we can split the source of the delay into two categories: the delay in charging the gate to turn on the MOSFET and the delay in charging the equivalent capacitor at the output. The gate-charging delay will depend on the specific gate-driving circuit and can therefore not be estimated yet. To get an insight into the output-charging delay, an over-simplified model would be to use the equivalent on-resistance of the MOSFET, which typically ranges from a few hundred milliohms to $750\,\Omega$ for the required voltage level.

If the MOSFET is modelled as a simple resistor, the rise time can be calculated with equation 4.3. For the worst case of a $750\,\Omega$ on-resistance and with $C_i \approx 220\,\mathrm{pF}$, we see that the output-charge time is only $495\,\mathrm{ns}$ which is 100 times lower than the allowed rise and fall time.

An N-type MOSFET seems to be the optimal solution for the current prototype. In future iterations, the selected MOSFETs can be replaced by MOSFETs with alternative characteristics, making this design very flexible. The only difficulty is that MOSFETs do not provide galvanic isolation. Failure of a MOSFET could propagate back into the driver, with catastrophic consequences for the rest of the electronics. Therefore, the MOSFET driver circuit must implement the required galvanic isolation.

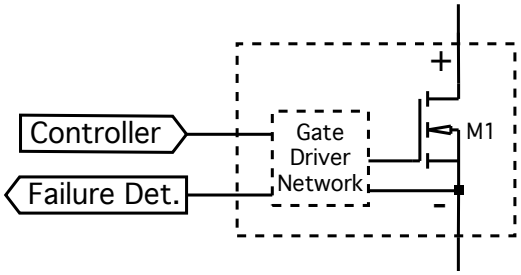


Figure 4.3: N-type MOSFET implementation of charge and discharge networks in figure 4.1.

4.3. Selected Design

The final design of the driver is shown in figure 4.4. It consists of an N-type MOSFET half-bridge and a driver circuit for each of the two MOSFETs. For most MOSFET switching applications, dedicated driver ICs are easily available. However, while some of these are designed to provide isolation in the range of kilovolts for higher frequencies, the DC isolation is limited to mostly a few hundred volts. This is not enough for the amount of isolation needed, especially when the system must be scalable to even higher voltages than $1\,\mathrm{kV}$. Therefore, custom driver circuitry had to be designed. The driver circuit of each MOSFET has a few main functions:

- The driver circuit must keep the MOSFET off when no input signal is present.
- The driver circuit must be able to quickly charge the gate above the threshold voltage (rise state)
- The driver circuit must be able to keep the gate charged for a longer period of time
- The driver circuit must be able to switch off the MOSFET quickly
- The driver circuit must provide galvanic isolation between the high-voltage part and low-voltage part of the system
- The driver circuit must feedback information about critical failures of critical to the controller.

The driver circuits work as follows: R5 and R6 are present to keep the MOSFETs turned off passively. They will be of a high value to avoid quick discharging of the gates in the case that the MOSFETs need to be turned on. Second, the MOSFETs can be turned on by providing very short pulses into the “on” terminals. Generating these pulses is the task of the controller. Bipolar junction transistors (BJTs) Q1 and Q2 allow for current amplification to send an increasing current through the transformers T1 and T2 during a pulse. The transformers will transfer the short current pulses and the charge will accumulate in the gates. At the end of a charge, diodes D1 and D2 prevent the accumulated gate charge to flow back to the source through the transformers. This keeps the MOSFETs on for a longer amount of time. Diodes D3 and D4 provide a current flyback path at the primary side of the transformers. To turn the MOSFETs off, a signal can be sent to the “off” terminal to turn on the optocouplers. The transistor at the output of the optocouplers will then provide a low-resistance path for the gate charge to flow back to the source. The transformers provide galvanic isolation of DC signals by magnetic coupling. The optocouplers provide galvanic isolation through optical coupling.

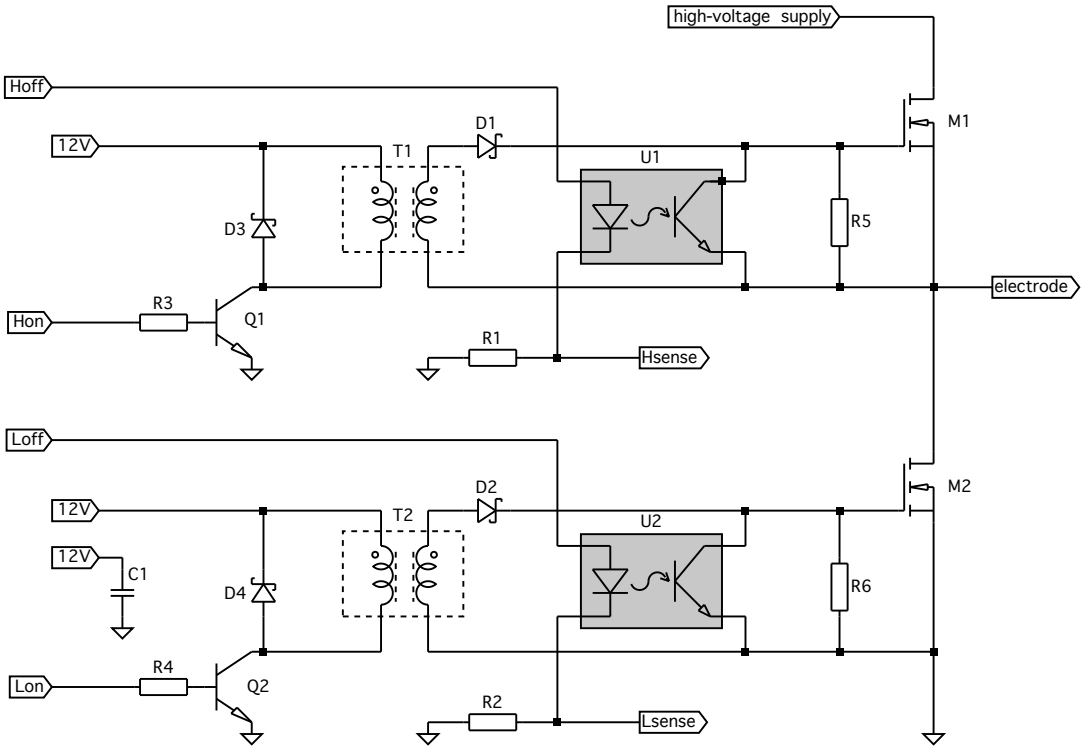


Figure 4.4: Schematic of the selected driver design.

4.4. Risk Analysis and Failure Detection

Before analyzing and explaining the required controller signals and design choices, we will identify the main risks associated with the chosen solution. First of all, when something goes wrong in the high-voltage part, the high voltage could propagate back into the driver and controller. This would ruin the electronics of the lunar rover, or the laptop used for controlling the microcontroller in the test setup. The galvanic isolation protects against DC voltages, but high-frequency signals can still partly propagate back through the gate-drive transformers. To avoid MOSFET breakdown at all, the high-voltage supply has a maximal output voltage of 80% of the MOSFET breakdown voltage but is normally kept to around 70%. The output of the high-voltage generator has a current limit to avoid excessive currents causing a breakdown in the MOSFETs. Also, the transformers have a ratio of 1:1 so that the gate-source voltage of the transistor can never exceed the voltage of the power supply. This ensures that the gate-source voltage is kept well below its maximum value.

Another risk associated with any MOSFET half-bridge is the case when two MOSFETs are accidentally turned on at the same time. In this system, this could happen if one of the gates does not properly discharge through the optocoupler before the other MOSFET is turned on. The timely discharging of the gate is totally dependent on the functioning of the optocouplers. As a critical safety feature, the controller must be able to detect optocoupler failure to handle this accordingly. The optocouplers can malfunction in three different ways:

1. The optocoupler is accidentally disconnected from the controller in a test setup dependent on jumper wires. This is a very likely scenario.

2. The optocoupler input LED is broken. This is also a likely scenario that even occurred two times during testing.

3. The optocoupler output transistor is broken. This is not very likely, as the maximum output voltage of the selected optocoupler is more than two times higher than the maximum gate-source voltage of the MOSFET.

To detect the first two and most important failure modes of the optocoupler, the voltages at “Hsense” and “Lsense” are fed back to the controller. During normal operation, a small voltage V_F will fall across the LED at the input of the optocoupler and a big voltage will fall across the resistor. With a signal voltage V_s of $5\,\mathrm{V}$ of the controller and a forward voltage $V_F = 1.2\,\mathrm{V}$ for the chosen optocouplers, the output voltage for the components would be $3.8\,\mathrm{V}$, which is considered ”high” by the used microcontroller. If a wire is disconnected, the voltage at the sense terminals will be 0 and be considered ”low” by the controller. If the LED is broken — which can be modelled as an open circuit — the voltage at the sense terminals will be 0, too. This allows the microcontroller to easily detect the most important failures in the system.

4.5. MOSFET Selection and Space-Grade Upgrade suggestion

The most important components of this circuit are the N-type MOSFETs M1 and M2 that drive the output in a half-bridge configuration. For the choice of MOSFET, the main requirement for the prototype is that the maximum drain-source voltage V_{ds} must be high enough to support a voltage of at least $1\,\mathrm{kV}$. To have a safe margin, MOSFETs with an absolute maximum V_{ds} of $1.5\,\mathrm{kV}$ are chosen that are relatively cheap and widely available: the STFW3N150 from STMicroelectronics[18].

For later iterations, good functionality over a wide range of temperatures will become important. At $25°\mathrm{C}$ and V_{ds} equal to $1.5\,\mathrm{kV}$, the STFW3N150 has a maximum zero gate voltage drain current of $10\,\mu\mathrm{A}$. When $V_{ds} = 1\,\mathrm{kV}$, the drain-source current will be lower, but a worst-case leakage current already results in $10\,\mathrm{mW}$ of static power dissipation of a single output. This can be considered high but acceptable with respect to the power requirements. However, at temperatures of $125°\mathrm{C}$, the zero gate voltage drain current can rise to a maximum value of $500\,\mu\mathrm{A}$, which results in unacceptably high power consumption due to leakage current. As high temperatures are not uncommon in a lunar environment, the STFW3N150 is unsuitable for usage in the final system. However, these transistors offer a good solution for the prototype which will only be tested at room temperature.

4.5.1. Selecting a MOSFET for Space Applications

If there do not exist transistors that can perform properly in a lunar environment, the development and testing of the current design with N-type MOSFETs could be declared useless. We will do a small investigation into space-related problems that N-type MOSFETs can encounter, and check if solutions exist. For radiation effects, we studied chapter 11.5 of [19], which is the main source of information for this section.

When MOSFETs are exposed to ionizing radiation, such as gamma or x-rays, the radiation can create electron-hole pairs in oxide and semiconductor materials. The electrons can move away through the oxide under the influence of an electric field with relative ease. They will flow away into the gate and not cause a problem. On the contrary, the holes have a lower effective mobility in the oxide. They will be travelling towards the semiconductor interface for much longer. Once they have finally arrived at the interface, they can get trapped due to variations in the oxide structure that form charge traps, which causes a negative shift in threshold voltage. [19] concludes this explanation with the statement that “This trapped charge can last from hours to years”. For N-type MOSFETs, the radiation-induced reduction of the threshold voltage can ultimately lead to passive turn-on of the MOSFETs. This is a critical risk for the dust removal system, as the half bridges driving the outputs would then form a short circuit passively.

Another effect of radiation is that interface states of the MOSFET can be charged. The charges will interact with the carriers in the channel, affecting carrier mobility and increasing the threshold voltage. For increased amounts of radiation, the threshold voltage will drop, but for even higher amounts of radiation, the threshold voltage of N-type MOSFETs could rise again due to interface state effects. In conclusion, the MOSFETs can be affected by radiation in many different ways largely due to two sources of radiation-induced alterations in the transistor: electron-hole pairs and charge interactions at the interface states. This information is largely sourced from [19]

One way to solve the radiation-induced shift in threshold voltage is by using a different semiconductor than silicon (Si), such as silicon carbide (SiC), of which different polytypes like 4H-SiC and 6H-SiC are common for semiconductor devices. SiC has a greater bandgap than Si, which creates a greater barrier for the creation of electron-hole pairs. In addition, SiC has a higher thermal conductivity than silicon, making it more resistant to radiation-induced thermal damage. Further, SiC also has a much higher breakdown field than Si[20]. Another advantage of SiC is that it provides a stable functionality

of the MOSFET over a wide range of temperatures. This will also be of great importance in a lunar environment.

Another solution to radiation-induced problems is to protect the MOSFETs from radiation. The MOSFET can be shielded by positioning it in a radiation-resistant enclosure or by utilizing radiation-blocking materials, such as lead or tungsten. Radiation-hardened components are designed to withstand the effects of ionizing radiation and are frequently used in applications where radiation exposure is a concern, including space exploration and nuclear power facilities.

In conclusion: for the next iterations of the system, it is crucial to consider temperature resistance, radiation resistance, and breakdown voltage when selecting MOSFETs for use in space applications. SiC-based MOSFETs are an excellent choice for space applications due to their better radiation resistance and high-temperature resistance and their greater breakdown strength than Si, which makes them suitable for the production of high-voltage semiconductor devices.

4.6. Selection of Resistors R5 and R6

Resistors R5 and R6 function as a passive connection between the gate and source that keeps the voltage between them equal to zero if no input signals are applied. Their value is chosen to be $10\,\mathrm{M\Omega}$. A negative side effect of the presence of these resistors is that when the transistor is turned on, the resistors provide an extra path when for gate-charge to flow away. The value of $10\,\mathrm{M\Omega}$ is chosen so that the current through the resistor is slightly higher than the leakage current of the optocoupler output transistor, the rectifier diode and the MOSFET itself. If the gate-source voltage is $10\,\mathrm{V}$ — which is a realistic scenario based on measurements and simulation results — the current through the resistor is $I_R = \frac{V_{gs}}{R} \approx 1\,\mu\mathrm{A}$. Together, the other sources of leakage current are at most $350\,\mathrm{nA}$ at $T = 25°\mathrm{C}$ and at $V_{gs} = 10\,\mathrm{V}$ which is a rough estimate based on the sum of the leakage current specifications of the optocoupler, the diode and the MOSFET.

4.7. Diode Selection

The main function of diodes D1 and D2 is to prevent the accumulated charge in the gate to flow back through the transformer once the voltage of the transformer drops. The DC blocking current does not have to be very high, as the maximal reverse voltage will be the gate-source voltage of the MOSFET. The primary requirement for D1 and D2 is a very low reverse recovery time. Schottky diodes are very well known for their low reverse recovery time. Additionally, a leakage current preferably not higher than $3\,\mu\mathrm{A}$ is required to avoid discharging the gate too quickly between PWM pulses. For the prototype, the SD101A from Diodes Incorporated [21] was chosen. It has a very low reverse recovery time of $1\,\mathrm{ns}$ and a reverse current of maximally $200\,\mathrm{nA}$ at a reverse voltage of $50\,\mathrm{V}$. Additionally, the forward voltage drop is very low. However, for space applications, special diodes are needed that are both radiation resistant and function over a large voltage in addition to the previously stated requirements. The radiation resistance does not pose a problem, as many radiation-resistant devices are available. For example, ST Microelectronics produces many radiation-resistant diodes which are listed in [22]. However, the large leakage current of many Schottky diodes at higher temperatures can pose a problem with the functioning of the system across a range of temperatures. Therefore, other types of diodes with a very low reverse recovery time could provide a better solution.

4.8. Gate-Charge Network and Maximal PWM Frequency

We will now define the required charge-network input signal to keep the MOSFETs properly turned on. The controller sends these signals into the “Hon” and “Lon” terminals of the schematic in figure 4.4. We chose to keep the gate-source voltage above the voltage V_{gp} of the Miller plateau that can be observed in the gate-source voltage vs gate-charge characteristics in the MOSFET datasheet[18]. Alternatively, a voltage can be chosen that is a few volts above the threshold voltage to ensure that the MOSFET is turned on. For the STFW3N150, we read from the datasheet that $V_{gp} = 6\,\mathrm{V}$.

When the gate-source voltage V_{gs} is larger than V_{gp}, the V_{ds} vs I_d characteristics also show that the behaviour of the transistor is almost independent of the gate-source voltage, especially at low values of the drain-source voltage, which indicates a constant resistance. We assume that above V_{gp}, the ripple in the gate-source voltage will not propagate to the output.

To keep the gate-source voltage above V_{gp}, a PWM signal is sent into the transformer by the con-

troller, providing very short pulses of length t_{PWM} every T_{PWM}. After turning on the MOSFET by sending an initial pulse of length t_{init} into the gate-charge network, the gate-source voltage is observed to rise above $8\,\text{V}$. This has been validated by measurements and simulations. Hence, the maximum of T_{PWM} is determined by the time that V_{gs} takes to passively drop from $8,\text{V}$ to $6\,\text{V}$.

We use a very simple model for this. First of all, the gate-source charge is modelled to be contained by an equivalent capacitor C_{gs}, as the datasheet of the STFW3N150 seems to model the gate-charge vs gate-source voltage to be linear above the miller plateau, which suggests that it can be modelled as a differential capacitor. In the model, this capacitor discharges through the $10\,\text{M}\Omega$ resistor in parallel with a current source I_L, representing the maximal leakage current of the optocoupler, the diode and the MOSFET. The schematic of the electrical circuit associated with this model is shown in 4.5a. The voltage in the capacitor satisfies the following differential equation:

$$C_{gs}\frac{\partial V_{gs}(t)}{\partial t} = -\frac{V_{gs}(t)}{R} - I_L \tag{4.5}$$

We solve this equation — for example by separation of variables — and find that

$$V_{gs}(t) = (V_{gs}(0) + RI_L)e^{-\frac{t}{RC_{GS}}} - RI_L \tag{4.6}$$

If the gate-source voltage after the first pulse is $V_{gs}(0)$ of $8\,\text{V}$, the gate-source voltage will slowly drop to V_{gp} of $6\,\text{V}$ after a certain amount of time. This time sets the maximum value of T_{PWM}, because a new pulse is needed to recharge the gates before the gate-source voltage drops to V_{gp}. We therefore find the upper limit for T_{PWM} by solving $V_{gs}(T_{\text{PWM}}) = V_{gp}$:

$$T_{\text{PWM}} < -RC_{gs}\ln\left(\frac{V_{gp} + RI_L}{V_{gs}(0) + RI_L}\right) \tag{4.7}$$

The actual value for C_{gs} seems hard to determine. The datasheet does not specify the very non-linear gate-source capacitance characteristics for the specific conditions. The characteristics of C_{iss} and C_{rss} at $V_{ds} = 0\,\text{V}$ could be used to find $C_{gs} = C_{iss} - C_{rss} = 450\,\text{pF}$. However, it is specified that these conditions hold when $V_{gs} = 0$, which is clearly not the case. Calculating the differential capacitance from the gate charge against the gate-source voltage characteristics suggests that $C_gs = \frac{dq}{dV} \approx 1.8\,\text{nF}$, which is way larger and only holds when $I_d = 2.5\,\text{A}$, which is clearly also not the case. Therefore, we decided to estimate the equivalent capacitance using measurement data.

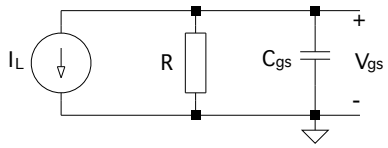
The measurement data and the fitted model are visualized in figure 4.5b. To find estimate parameters C_{gs} and I_L, the problem was reduced to a nonlinear least-squares problem with model $V_{gs} = (V_{gs}(0) + a)e^{-bt} - a$. The problem was solved using the Levenberg–Marquardt algorithm as described in [23] using Matlab and the code is given in appendix C. We found that $C_{gs} = 211\,\text{pF}$ and $I_L = 53.3\,\text{nA}$ results in the best fit of the model to the data. Therefore, a PWM period limit of $T_{\text{PWM}} < 568\,\mu\text{s}$ is given by equation 4.7 is given. As this limit is an absolute maximum, we decided to use $T_{\text{PWM}} = 200\,\mu\text{s}$ to be on the safe side. For any replacement of components, this calibration procedure will be necessary. Also, for space applications, it will be important to do this test across a range of temperatures, as especially the leakage currents modelled by I_L are very temperature dependent.

4.9. Gate-Charge Network, PWM Pulse Width and Minimal PWM Frequency

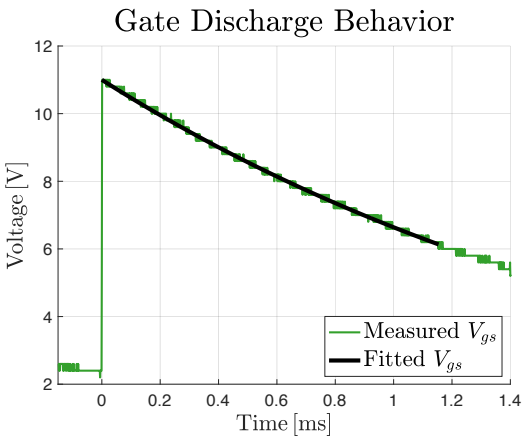
To charge the gate through the transformers, transistors Q1 and Q2 can be turned on for a short amount of time to send current through the transformers into the gates. In this section, we will first determine the range of values for the base resistors that will result in the desired behaviour of efficiently charging the gates. Then, we will find the optimal PWM pulse length by experimentation.

If a changing current is sent into the primary side of the transformers, a changing magnetic flux Φ_B is generated in the transformer core, as flux is directly proportional to current. Then, by Faraday's law, an electromotive force ε is induced in the secondary side that will try to resist the changing flux by creating a changing magnetic field in the opposite direction:

$$\varepsilon = -\frac{d\Phi_B}{dt} \tag{4.8}$$



(a) Equivalent electrical model used to determine the passive discharge time of the gate.



(b) Measured and modelled gate-source voltage of a MOSFET in the gate driver circuit during a passive discharge state. At $t = 0$, the gate is charged. After $t = 0$, the passive discharge state applies.

Figure 4.5: Gate charge model.

This electromotive force is realized by a charge displacement at the secondary side so that the gate of the MOSFET is charged. Thus, we need to create a changing flux in the transformer coil to charge the gate successfully. We achieve this by providing a changing current on the primary side which is created by the rise characteristics of the transistors Q1 and Q2.

For the pulse length, this means that as soon as the collector current of the transistor stops rising, $\frac{d\Phi_I}{dt}$ drops to zero causing $\frac{d\Phi_B}{dt}$ to become zero, too. However, the current will still flow at the primary side without creating any charge displacement at the secondary side. In this way, the system would be wasting energy. As soon as the current stops rising, the transistor should be turned off again.

Because transient modelling of transistor behaviour with simple mathematical equations did not seem feasible for our application, we decided to base the pulse duration on both simulation results and testing the gate driver circuit with an equivalent capacitor instead of the MOSFET. We discovered that for turning on the MOSFET, a single initial pulse of duration $t_{\text{init}} = 5\,\mu\text{s}$ worked well, and for keeping the gates charged afterwards, a PWM signal with pulses of length $t_{\text{PWM}} = 2\,\mu\text{s}$ worked well.

The resistors at the base of the BJTs will determine the maximum current that will flow through the primary side of the transformer before it is turned off. A very simple model of the collector current of a BJT is

$$I_C = h_{FE} I_B \tag{4.9}$$

where I_B is the current flowing into the base and h_{FE} is the DC current gain which is between 420 and 800 for the chosen transistor: BC547C[24]. In the driver circuit, the base current in DC is equal to

$$I_B = \frac{V_s - V_{BE}(sat)}{R} \tag{4.10}$$

Where V_s denotes the signal voltage of the controller — $5\,\text{V}$ for the chosen microcontroller — and $V_{BE}(sat)$ is the base-emitter voltage of the transistor in saturation, which is a little higher than $700\,\text{mV}$ for the chosen transistor. R is the resistance of R3 and R4 in the driver circuit of figure 4.4.

If we assume that the rise time of the transistor is independent of the DC-value of I_C, then $\frac{dI_C(t)}{dt}$ will be larger during the rise for a higher DC value of I_C. As $\Phi_B(t) \propto I_C(t)$, we see that this also leads to a larger $\frac{d\Phi_B(t)}{dt}$. However, the core of the transformer can only contain a limited amount of flux, as the material will saturate when a certain magnetic flux density is exceeded. When the core of the transformer is saturated, no signal will be transferred at all and unpredictable behaviour occurs. To ensure that the magnetic flux density stays below the saturation level, we can limit the current that may flow through the transformer.

The datasheet of the used transformer [25] — B82804A0354A110 by TDK Electronics — specifies a maximal voltage-time product of $25.8\,\mu\text{Vs}$. We can interpret the voltage-time product as the maximal allowed time that a voltage of $1\,\text{V}$ can be applied at the primary inductor with the secondary inductor

open before saturation occurs. As both inductors have an inductance of $L = 350\,\mu\mathrm{H}$, we could say the current increases with a rate of $\frac{1}{L}$ for the gate drive transformer, saturation will occur at a current of $73.7\,\mathrm{mA}$.

To determine the minimum resistance value, we will calculate the resistance at which the DC collector current of the transistor is $73.7\,\mathrm{mA}$. We combine equations 4.9 and 4.10 as follows:

$$R = h_{FE}\frac{V_s - V_{BE}(sat)}{I_C} \tag{4.11}$$

and find that $R > 46.7\,\mathrm{k\Omega}$ by assuming the worst-case h_{FE} of 800. We chose a resistor of $51\,\mathrm{k\Omega}$, which should maximally result in a current of $67.5\,\mathrm{mA}$. In practice, simulations show that the collector current will probably not exceed $50\,\mathrm{mA}$.

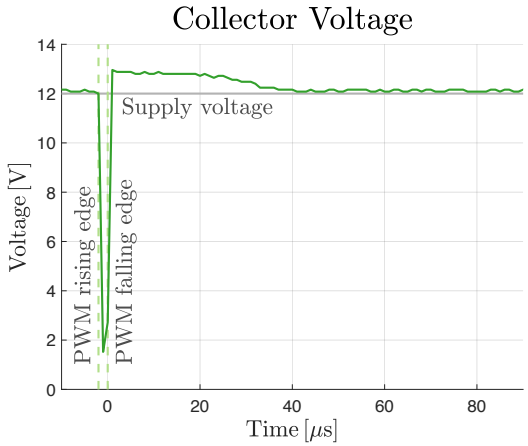


Figure 4.6: Voltage measurements at the collector of BJT Q2 after a PWM pulse of $2\,\mu\mathrm{s}$. The recovery time ends when the collector voltage restores to the level of the power supply at about $t = 40\,\mu\mathrm{s}$.

While at higher maximum collector currents the gates charge faster per pulse, there is also a timing-related negative side effect. Assume that at the end of the pulse a current of I_C as described in equation 4.9 is present. When the pulse ends, diodes D1 and D2 prevent the accumulated charge from flowing back through the transformer at the secondary side. As no current will be present at the secondary side, we can model the secondary side as open and the primary side behaves like an inductor. From basic electrical circuit theory, we know that the current in an inductor must be continuous. This means that all current in the primary side will flow through diode D3 or D4 because the transistors close at the end of a pulse. A forward voltage of V_F will fall over the diodes, and the diodes will dissipate power. In this way, the magnetic energy of the transformer is dissipated in the diodes and the flux in the transformer decreases. Note that the voltage at the collector will now be slightly higher than the power supply, which is also visible in the measurements of the collector voltage after a pulse in figure 4.6. We can quantify this phenomenon with the following formula from basic circuit theory:

$$\frac{dI_L}{dt} = \frac{V_F}{L} \tag{4.12}$$

With a forward voltage V_F of $0.41\,\mathrm{V}$, an initial current of approximately $50\,\mathrm{mA}$ and a primary inductance of $350\,\mu\mathrm{H}$, this results in a "recovery time" of about $40\,\mu\mathrm{s}$. Figure 4.6 shows that the measurements validate this calculation. If the datasheet would provide a more accurate specification of h_{FE}, the following formula sets the minimum PWM period.

$$T_{\mathrm{PWM}} > t_p + \frac{h_{FE}V_F\,(V_s - V_{BE}(sat))}{LR} \tag{4.13}$$

For our application, we choose $T_{\mathrm{PWM}} > 40\,\mu\mathrm{s}$ based on the measurements visualized in figure 4.6. The used value for T_{PWM} of $200\,\mu\mathrm{s}$ is well above this lower limit.

4.9.1. Optocoupler and Series Resistor Selection

To discharge the gate, an optocoupler is used. For the prototype, we chose the 4N35 from Liteon Optoelectronics[26]. However, for a space application, this model would not be suitable as the leakage current at higher temperatures will drain the gate rapidly, requiring a T_{PWM} that will be lower than the minimal T_{PWM}. For a space-grade optocoupler, the collecter dark current should be low even at high temperatures and the optocoupler should be radiation resistant.

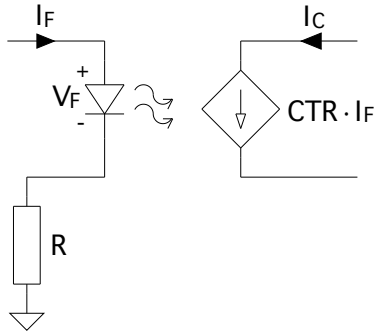
To model the time needed to discharge the gate, we will use the CTR specifications of the optocoupler datasheet. The CTR specifies the collector current of the output to be dependent on the input current. The input of the optocoupler consists of an LED with a voltage drop of $V_F = 1.2\,\text{V}$ as specified by the datasheet. If the pulse voltage of the controller output is equal to V_p, the input current of the optocoupler can therefore be modelled as

$$I_F = \frac{V_p - V_F}{R} \tag{4.14}$$

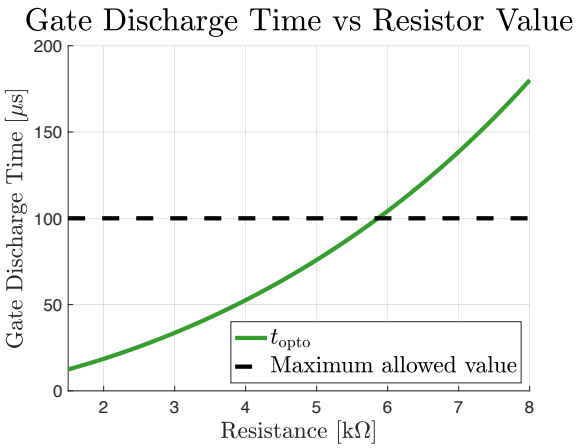
where the resistance R is the value of resistors R1 and R2 in figure 4.4. The current at the collector of the output transistor of the optocoupler is equal to

$$I_C = \text{CTR} \cdot I_F \tag{4.15}$$

Figure 4.7a shows the schematic of the equivalent electrical model for the optocoupler and the resistor. The model assumes a constant input voltage will cause I_C to be constant, too. Therefore, the gate charge will be decreased with a constant rate of $I_C\,\text{J}\,\text{s}^{-1}$, which suggests a flaw in this model. If the gate charge decreases at a constant rate, it will become negative and continue decreasing until the end of time. In the real world, the CTR is dependent on the collector-emitter voltage V_{CE} at the output of the optocoupler, and when $V_{CE} = 0$ then $\text{CTR} = 0$. The CTR model only holds if the collector-emitter voltage at the output of the optocoupler is above the saturation voltage and the output transistor is in active mode. Below the saturation voltage, the current will be lower than suggested by the CTR and the model would be too optimistic in terms of minimal discharge time. However, as the saturation voltage is far below the threshold voltage of the MOSFET, we can safely use this model, because the MOSFET will already be off before the transistor goes from active mode to saturation mode.



(a) The schematic of the equivalent electrical model of the optocoupler output collector current I_C.



(b) Modelling results of the required optocoupler pulse time t_{opto} to fully discharge the MOSFET gate dependent on input series resistance R. The model is described by equation 4.17. The maximum allowed value of t_{opto} is shown, too.

Figure 4.7: Optocoupler output current model and results.

The datasheet of the MOSFET suggest that at a V_{gs} of $12\,\text{V}$, a gate charge of $Q_g = 32.5\,\text{nC}$ is present. To remove this charge using a constant current I_C, we need a time of $t_{\text{opto}} = \frac{Q_g}{I_C}$. However, the datasheet shows that for low values of the forward voltage I_F — which is required to minimize the power consumption by the optocoupler signals — The CTR is highly dependent on I_F. From inspection

of the datasheet, the CTR-I_F characteristics resemble a straight line for $0.5\,\mathrm{mA} < I_F < 3\,\mathrm{mA}$ when plotted with a logarithmic I_F axis. This allows us to model the CTR for this region as

$$\mathrm{CTR} = x_1 \ln(I_F) + x_2 \tag{4.16}$$

Finally, we first combine equation 4.15 and 4.16 to find a better model for the collector current. By using the fact that the charge displaced by the constant collector current is equal to tI_C, we find the minimal required optocoupler on-time as a function of the resistance:

$$t_{\text{opto}} = \frac{Q_g R}{\left(x_1 \ln\left(\frac{V_p - V_F}{R}\right) + x_2\right)(V_p - V_F)} \tag{4.17}$$

By using some eye-balled CTR-I_F samples from the datasheet, we estimate that $x_1 = 0.3907$ and $x_2 = 3.3695$ using the linear least square solution of the model specified in 4.16. The resulting optocoupler pulse time vs resistance characteristics are shown in figure 4.7b. Further, we require that $t_{\text{opto}} < 2t_{r,\text{max}} = 100\,\mu\text{s}$. This ensures that the output is not left in a floating state for too long before it rises or falls. By setting t_{opto} to $100\,\mu\text{s}$ in 4.17 and finding the roots with Matlab, we find the maximal resistor value as $R < 5.86\,\text{k}\Omega$. To be safe, we chose a value of $R = 4.7\,\text{k}\Omega$, which requires a t_{opto} of $68.4\,\mu\text{s}$. However, we still chose to operate the system at $t_{\text{opto}} = 100\mu\text{s}$. The measurement data of the gate-source voltage in figure 4.8 validate that the model is quite pessimistic, as the gate-source voltage seems to drop below the threshold voltage in less than $50\,\mu\text{s}$. This is another guarantee for the safe operation of the system.

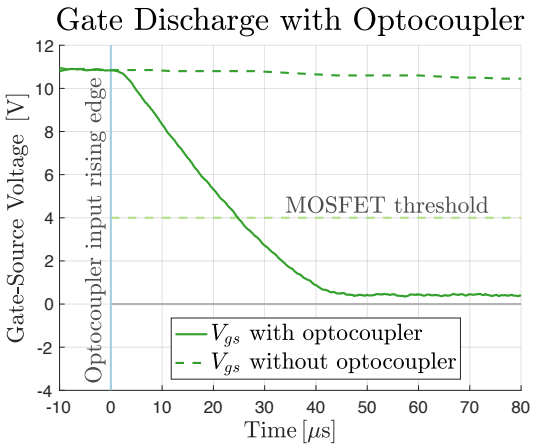


Figure 4.8: Measurements of the discharge behaviour of the gate with an optocoupler. The discharge without an optocoupler is also shown as a reference. A moving average filter is applied to the measurements to smooth out the quantization noise of the oscilloscope.

5

Design of the Controller

In this chapter, we will discuss the driver that was implemented on an Arduino Mega which uses the Atmega2560 microcontroller from Microchip Technology[27]. The *Lunar Zebro* team already uses space-grade microcontrollers but for the prototype, we decided to use an Arduino, as this allows for faster and easier prototyping. This project is after all a proof of concept. In the previous chapter, we derived the required control signals that the controller has to provide. The signals for a single driver are summarized in figure 5.1. Additionally, the controller must detect the failure of the optocouplers and handle them to ensure safety. The code that implements the entire controller is included in appendix B.

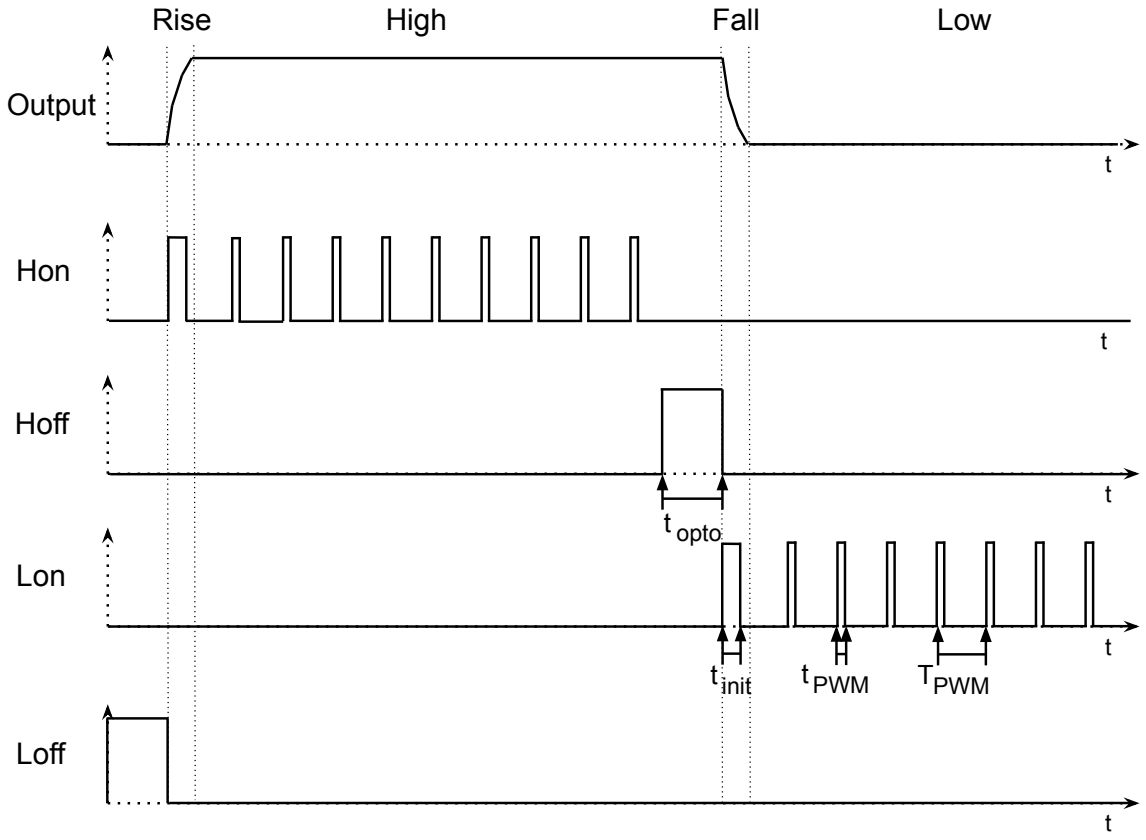


Figure 5.1: Controller signals required to drive one of the three outputs through the gate network. “Output” corresponds to the corresponding electrode voltage. The other signals correspond with the signals in figure 4.4.

5.1. Implementation with a Circular Linked List

Each output can be in four different states: low, rising, high and falling. Appendix A specifies the timings of the state transitions in equation A.4 and the possible state transitions are represented in figure A.1. This allows us to specify a cycle of output events that the controller goes through to generate the required signals, even for multiple phases. The order of events is constant for a set duty cycle.

As the required signals in figure 5.1 are highly symmetric, the total functioning of the controller can be constructed using only two types of events. First, an “optocoupler event” is able to turn on a MOSFET and measure if it is working correctly to prepare for either a rise or a fall. The global variable $broken$ is used to keep track of the well-functioning of each state.

Algorithm 1 Optocoupler Event

Data: `off_pin1`, `sense_pin1`, `on_pin1`, `PWM_generator1`, `output_index`

1: **if** $broken$[`output_index`] = false **then**
2: Disconnect `on_pin1` from `PWM_generator1`
3: Turn on `off_pin1`
4: Measure `sense_pin1`
5: **if** `sense_pin1` = LOW **then**
6: $broken$[`output_index`] = true
7: turn on indication LED
8: turn off all pins of output[`output_index`]
9: **end if**
10: **end if**

Second, the transformer event can turn on a MOSFET to initiate a rise or a fall.

Algorithm 2 Transformer Event

Data: `off_pin1`, `on_pin2`, `PWM_generator2`, `output_index`

1: **if** $broken$[`output_index`] = false **then**
2: turn off `off_pin1`
3: turn on `on_pin2`
4: wait for t_{init}, possibly shorter to compensate for execution time
5: turn off `on_pin2`
6: connect `on_pin2` to `PWM_generator2`
7: **end if**

For each output, the controller has to ensure that two MOSFETs are never turned on simultaneously at all costs. If the program always switches off one MOSFET before switching on the other, we can ensure very safe operating conditions of the system. To implement a fixed order of events that can not be violated, we choose the implementation of a circular linked list of events. Therefore, each event will — besides containing information about the event itself — also contain information about what the next event is. By connecting the “last” to the “first” event, the cycle is closed. While in operation, the code will contain a global pointer to the current event in the list. After executing the current event, the code will move to the next one. The different types of events are implemented using polymorphism in C++.

5.2. Timing: CTC interrupts and PWM generators

Each event also contains information about the time that it takes until the next event has to take place. To accurately time the delays between events, hard-coded delays are not an option, as code can have variable execution times. To achieve high timing accuracy, we use Clear Timer on Compare (CTC) interrupts. Timer 1 of the Atmega2560 is used for this. It will count up to a predefined value and triggers a special function if this value is reached. The “interrupt service routine” will interrupt the main code briefly and sets a flag to indicate that the current event may be executed. The timer will also be reset immediately to start counting again. The only risk of using this method is that when for some reason an interrupt is missed, the clock does not reset and there will be a big delay in the execution of events. In the worst case, one of the outputs may float for a while or the frequency is not as specified.

However, safety is still ensured by the linked list implementation. These conditions are likely for duty cycles close to $\frac{1}{3}$ and 23, which is derived in appendix A. In this case, events will be very close together.

For timer 1, a prescaler of 8 is used. With a $16\,\mathrm{MHz}$ internal clock, this means that the counter of timer 1 increases by 1 every 8 clock cycles and operates at a time resolution of $500\,\mathrm{ns}$. So if the compare value of the clock is for example set to 399, the interrupt will be called $500 \times 10^{-9}(399+1) = 200\,\mu\mathrm{s}$ after the last reset. Note that the $+1$ is added because the timer needs one prescaled clock cycle to reset.

As timer 1 has a 16-bit counter, it can count up to set delays of $500 \times 10^{-9} 2^{16} = 0.032768\,\mathrm{s}$ with a prescaler of 8. This maximal time is not enough when the output must be a $1\,\mathrm{Hz}$ rectangular wave. Therefore, another type of event is implemented: the idle event does nothing when it is executed and it takes a maximum amount of clock cycles until the next event. In this way, an event with a delay of — for example — 2.7 times the maximum time can be replaced by the event with only 0.7 times the maximum time as delay followed by two idle events.

For generating the required PWM signals, which are required for “Lon” and “Hon” for each of the three drivers, timers 3 and 4 will be used. The timers can be programmed to act as a PWM generator, and as this is all implemented in hardware, it will not interfere with the execution of code.

5.3. Scheduling of the Events

When the microcontroller starts up or resets, all events will be scheduled and the circular linked list of events will be prepared for execution. First, all events that occur for each phase will be scheduled chronologically. Equation A.4 in appendix A specifies the exact times at which all state transitions occur, which forms a base for the timing of the events. Note that the chronological time will be within $[0, T)$. Secondly, the times are converted into differential times or delay times and idle events are added to accommodate for potential CTC counter overflows. The loop is then closed and ready for use. The pseudocode below goes into these steps in more depth.

Algorithm 3 Scheduling of Events

Data: `events_list` (empty)
for `output_counter` $= 0, 1, 2$ **do**
  for `side` $= L, H$ **do**
    set `starttime_opto` $\in [0, T)$ based on `output_counter` and `side`
    create new `opto_event` for pins based on `side` and `output_counter`
    `opto_event->`$time$ = `starttime_opto`
    Insert `opto_event` into `events_list` chronologically by updating all $next$ attributes
    `starttime_trafo` = `starttime_opto` + t_{opto}, ensure `starttime_trafo` $\in [0, T)$
    create new `trafo_event` for pins based on `side` and `output_counter`
    `trafo_event->`$time$ = `starttime_trafo`
    Insert `trafo_event` into `events_list` chronologically by updating all $next$ attributes
  end for
end for
Set `first` and `event` to the first in `event_list`
while `event.`$next$ is non-empty **do**
  `event.`$delay$ = `event.`$next.time$ - `event.`$time$
  if `event.`$delay$ > max time of counter **then**
    Insert idle events between `event` and `event.`$next$
  end if
  `event` = `event.`$next$
end while
`event.`$delay$ = T - `event.`$time$
if `event.`$delay$ > max time of counter **then**
  Insert idle events at the end of `events_list`
end if
`event.`$next$ = `first`

6

Design of the High-Voltage Supply

6.1. Introduction

There are many methods for producing high voltage. Some other papers on electrostatic dust mitigation shortly discuss the test setup used. [8] used an off-the-shelf high voltage power supply and [28] uses four high voltage transformers for each phase, but it does not go into much detail. Therefore it was necessary to look at different methods. Here is a short list of other ways to generate high voltage: First, a Cockcroft–Walton's voltage multiplier can be used to boost an AC signal up to a very high DC voltage. In addition to that, a Marx generator can be used, its operation involves spark gaps and is not very practical for the current situation. Then there is a Tesla coil that generates high voltages using an air-core resonant transformer. Furthermore, there is the more commonly used flyback converter. [29]

Most high-voltage flyback converters use a flyback transformer to obtain the high voltages. Those transformers once were readily available due to their use for powering LCD display backlights [30], however, they are now more difficult to obtain, but some manufacturers still make them.

The goal for the high voltage boost converter is to generate a voltage of at least $1\,\mathrm{kV}$ that only needs to supply low currents. The design presented here uses a more typical boost converter design with a voltage multiplier circuit at the output. Furthermore, the design does not contain any dedicated switching regulator IC. However, performance would most likely be increased if it did.

6.2. Basic Boost Converter and Some Mathematical Insight

Boost converters are all about storing energy in an inductor and transferring that energy into a capacitor. Figure 6.1 demonstrates a basic boost converter topology. The circuit operates by first closing the switch, resulting in a current buildup in the inductor L. When the switch opens up again it results in a voltage spike that gets rectified to DC by the diode D and the capacitance C. The switch element itself is quite often built using a MOSFET transistor and an example of this voltage spike can be seen in figure 6.4, the switch gets opened when the gate voltage of the MOSFET goes low, resulting in the voltage spikes seen in the bottom waveform. The resistance R in figure 6.1 represents the load of the circuit.

In order to get an idea of the maximum output voltage it is useful to first look at the equations for energy stored in an inductor and a capacitor. The basic equations are:

$$E = \frac{1}{2}LI^2 \tag{6.1}$$

$$E = \frac{1}{2}CV^2 \tag{6.2}$$

The height of the voltage spike will consist of the stored energy in the inductor being transferred to a capacitor. The diode network with the capacitor C and resistor R will be ignored for now, this will be explained later. The remaining capacitance is the output capacitance of the MOSFET transistor used as the switch and some parasitic capacitance. All of the energy in the inductor will be transferred to

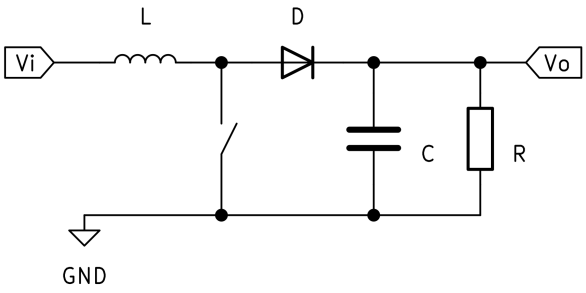


Figure 6.1: A basic boost converter circuit.

this capacitance, the equation of the height of the voltage spike can be derived by combining equation 6.1 and 6.2, which results in:

$$V_{spike} = I_0 \sqrt{\frac{L}{C_{OSS}}} \tag{6.3}$$

Where I_0 is the current through the inductor right before the switch is opened, and C_{OSS} is the output capacitance of the MOSFET switch. This equation represents the theoretical maximum output voltage when there is no load. The capacitor C has only a small impact on the maximum output voltage because this capacitor is not ”seen” by the inductor since the diode D is reversed-biased when C is fully charged.

6.3. Design Overview

The whole schematic for the high voltage boost converter is shown in figure 6.2. This circuit consists of mostly control circuitry, however, the core is still the same. L1 is the inductor used to store the current and the switch is the MOSFET transistor Q7. The voltage spikes at the drain of Q7 are boosted by a voltage multiplier circuit that boosts and rectifies the already high voltage spikes up to around $1\,\mathrm{kV}$.

The height of the voltage spike at the drain of Q7 is controlled by ensuring that the peak current through the inductor is constant. This is done by measuring the voltage drop across R1 and turning off Q7 accordingly.

Furthermore, the monostable multivibrator ensures that Q7 is turned off for a time period long enough so that the voltage spike has time to occur.

In addition to that, the boost converter can be turned off by some other circuits as well. First, there is a turn-on delay ensuring a stable startup. Second, there is an additional turn-off control for the microprocessor. And lastly, the auto turn-off circuits regulate the output voltage by turning off the boost converter when it has reached its desired output voltage.

6.3.1. Voltage Multiplier

The voltage multiplier (also called a Cockcroft–Walton multiplier) uses diodes and capacitors in a special arrangement to boost the already high voltage spikes of around $335\,\mathrm{V}$. The output voltage of the voltage multiplier is approximately equal to the input voltage spike multiplied by 3, which will in this case be around $1\,\mathrm{kV}$.

Capacitors C6, C8, and C10 all store a rectified DC voltage of around $335\,\mathrm{V}$. And capacitors C7 and C9 act as DC-blocking capacitors, only passing the high-voltage AC spikes. Those AC voltages are given a DC offset by diodes D4 and D6. Diodes D3, D5, and D7 rectify the AC pulses into DC.

In general, the circuit is high impedance and cannot supply large currents, this is because AC signal has to pass through capacitors to get to the final output. This makes voltage multipliers only suitable for low-current applications. A benefit is that the circuit is less dangerous to handle, but that is also determined by the total energy stored in the voltage multiplier. When the circuit is operating the voltage on each capacitor in the voltage multiplier is around $335\,\mathrm{V}$, which corresponds to a total energy of $2.8\,\mathrm{mJ}$.

The components used are able to withstand high voltages, the capacitors are $500\,\mathrm{V}$ ceramic capacitors and the diodes are $1000\,\mathrm{V}$ 1n4007’s.

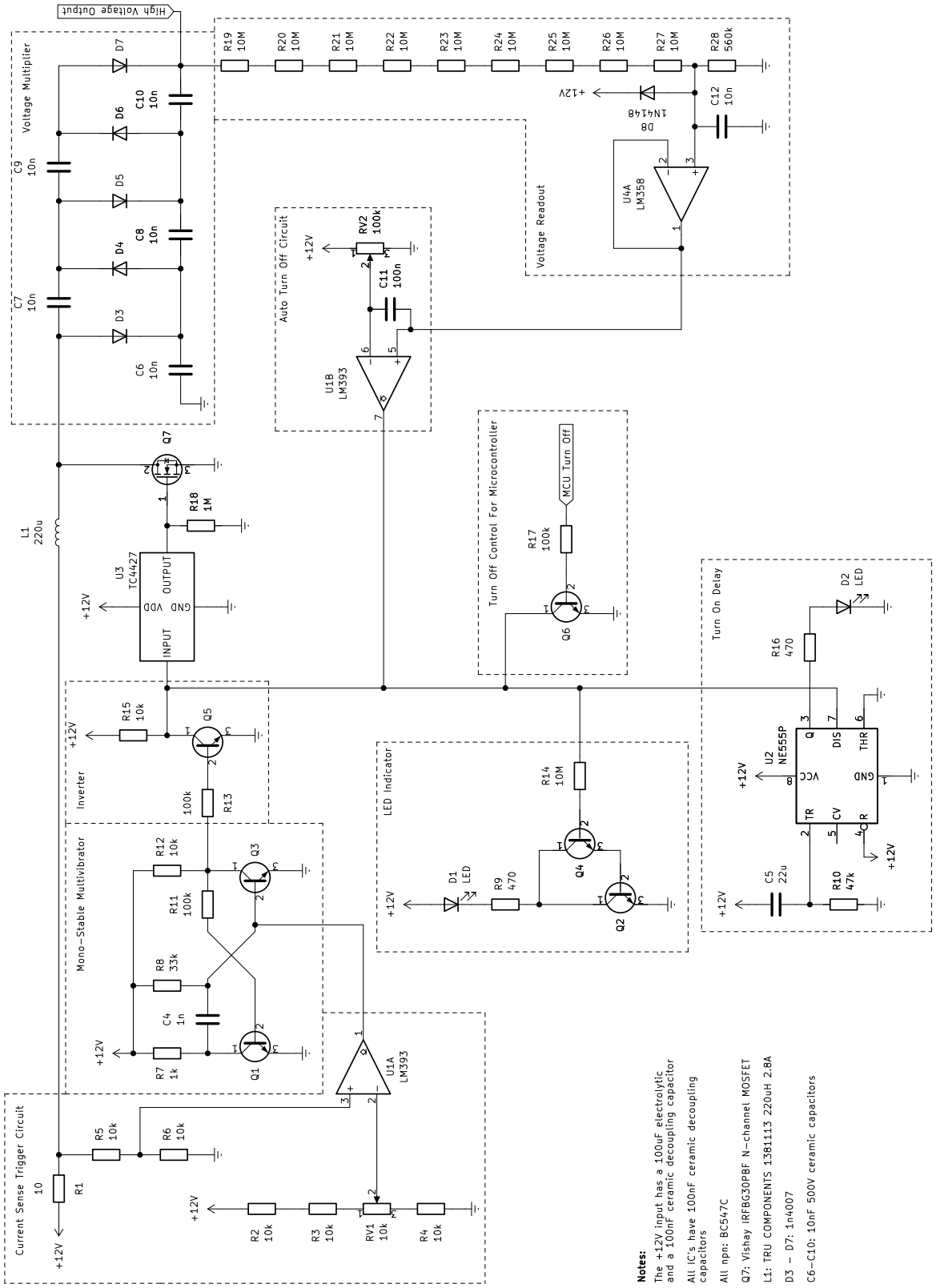


Figure 6.2: Full schematic of the high voltage boost converter.

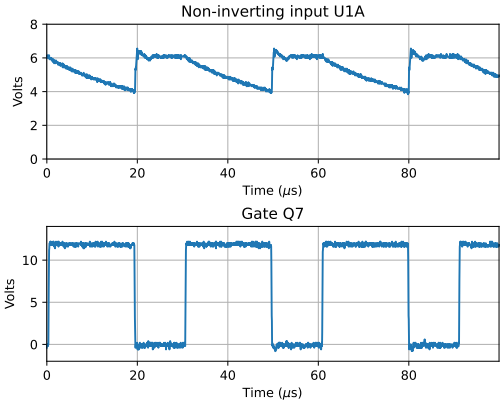


Figure 6.3: The current through the inductor L1 measured at the input of the LM393, and the gate voltage.

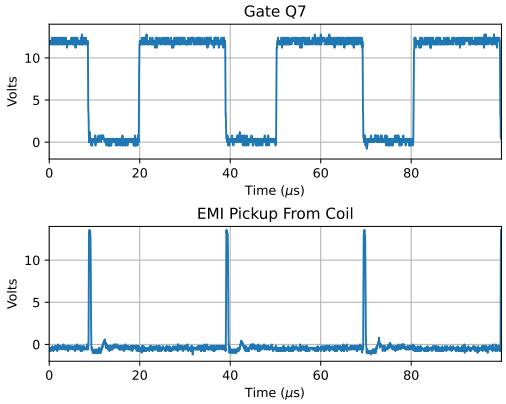


Figure 6.4: The gate voltage and the EMI waveform measured by an unconnected oscilloscope probe in proximity to the coil L1.

6.3.2. Current Sensing and the Monostable Multivibrator

In order for the high voltage spikes to be mostly consistent in amplitude it is important to control the peak current through the inductor carefully. In other words, to set I_0 in equation 6.3. This is done by measuring the current through the inductor and turning the switching transistor Q7 off when it reaches a threshold current. The current is measured by measuring the voltage drop across R1. When the current increases the voltage at the non-inverting input of the LM393 comparator (U1A) decreases through the voltage divider consisting of R5 and R6 (see figure 6.3). The voltage at the inverting input of U1A sets the threshold current I_0 and can be adjusted from $0\,\mathrm{mA}$ to about $600\,\mathrm{mA}$. When the current threshold I_0 is reached it triggers the monostable multivibrator by pulling the base of Q3 below $0.7\,\mathrm{V}$ (the LM393 has open collector output), which ensures that the switching transistor Q7 is turned off for around $10\,\mu\mathrm{s}$. This ensures that the voltage spike has enough time to live and find its way through the voltage multiplier before Q7 turns on again.

Figure 6.3 demonstrates this action, when the current increases through the inductor, the voltage at the non-inverting input of the comparator does down. It then triggers the monostable multivibrator pulling the gate voltage of Q7 down to zero volts, thereby turning the switching transistor off for $\approx 10\,\mu\mathrm{s}$.

Furthermore, figure 6.4 shows the resulting voltage spike when Q7 opens (gate voltage goes down). The spike was not measured directly, but the signal was picked up by an unconnected oscilloscope probe in close proximity to the coil L1.

6.3.3. Gate Driver and Open Collector Logic

Driving the gate of the switching MOSFET Q7 requires rapid charge and discharge of the gate capacitance ($C_{iss} \approx 980\,\mathrm{pF}$), which can require quite some current. U3 takes care of providing this current and ensures rapid switching of the gate voltage. The input of the gate driver appears to be a complex node, but its operation is rather simple. It can simply be seen as a logical NOR gate consisting of 4 different inputs, when any of these signals is high it has the effect of turning off the switching transistor Q7. The four different inputs are the output of the monostable multivibrator, the auto turn-off circuit, the turn-on delay circuit, and an additional turn-off control for the microprocessor.

The logic gate is implemented using common collector logic, R15 acts as a pull-up resistor that can be pulled down by four different transistors. These transistors are Q5, Q6, and the internal pull-down transistors inside U2 and U1B.

In addition to the input signals there is an LED indicator circuit indicating when the input to the gate driver is high, this indicates that the generator is on and producing high voltages. It is connected through R14: a $10\,\mathrm{M\Omega}$ resistor that ensures that there is a minimal voltage drop across R15. The two npn transistors Q2 and Q4 are connected in a Darlington configuration, which makes sure that there is enough gain to turn the LED on.

Furthermore, the gate driver IC U3 is a Mircochip TC4427 and it has some input capacitance (≈

$12\,\mathrm{pF}$ [31]), this results in an RC network with R15. However the gate driver does not translate this slow rise time to the output, its output is still fast as can be seen in figure 6.5.

6.3.4. Voltage Measurement and Auto Turn Off Circuit

Measuring high voltages can be a difficult thing to do. Of course, there exists special measurement equipment like high voltage probes. However, the lack of such equipment and the need to regulate the output facilitated the need for a built-in measurement circuit. The output voltage is measured through a large resistive voltage divider consisting of nine $10\,\mathrm{M\Omega}$ resistors (R19-R27) and one $560\,\mathrm{k\Omega}$ resistor (R28). The large number of resistors has two reasons, the first reason is that it provides a very low load to the boost converter. The second reason is more important for safe operation, it is to simply not exceed the breakdown voltage of the resistors. The voltage at the output of the voltage divider is $\approx 1/161$ times the output of the boost converter.

The voltage at the output of the voltage divider is then buffered by U4A, an LM358 opamp. The input bias current of the opamp is $250\,\mathrm{nA}$ maximum flowing out of the input pins at room temperature [32], this causes a measurement error of about 2.25% maximum when the output voltage is $1000\,\mathrm{V}$. Diode D8 protects the input of the opamp in case any high-voltage signal makes it through the voltage divider.

In section 6.3.2 it was described how I_0 could be controlled and that the height of the voltage spike is approximately determined by equation 6.3. Using the variable resistor control for I_0 the output voltage can be varied from about $150\,\mathrm{V}$ to $1.4\,\mathrm{kV}$. However, the output voltage is not very stable and tends to change with temperature, the inductor in particular heats up quite a bit. Furthermore, this continuous operation is very inefficient because the boost converter continuously tries to put more energy into the voltage multiplier. The problem of a stable output voltage is solved using a simple solution: the boost converter is simply turned off when it reaches a threshold output voltage and turned on again when the voltage has dropped a bit. This action is performed by U1B, an LM393 comparator.

U1B compares the output voltage to a threshold and turns the boost converter off when it exceeds that threshold. This action can be seen in figure 6.6. The output of the buffer opamp looks messy because the probe also picked some EMI from the inductor. Furthermore, the shown AC waveform rests on top of a $+6.2\,\mathrm{V}$ DC-offset (output voltage $\approx 1\,\mathrm{kV}$). But the measurement does make it clear that the boost converter does indeed turn off when it reaches the threshold voltage and turns on again after the output has dropped slightly in voltage. The oscillation at the gate of Q7 indicates that the boost converter is on.

The measured output ripple in figure 6.6 is around $50\,\mathrm{mV}$ this corresponds to approximately $8\,\mathrm{V}$ ripple on the $1\,\mathrm{kV}$ output. That is 0.8% ripple with no load.

Capacitors C11 and C12 were added to make the system more stable, this was necessary because the auto turn-off circuit would otherwise cause unwanted oscillations. The values and locations were found experimentally.

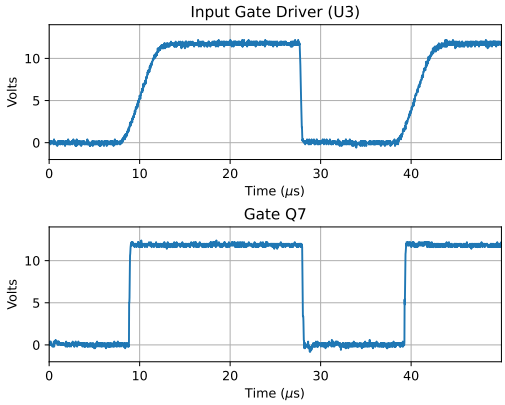


Figure 6.5: The input and output signals of the gate driver IC.

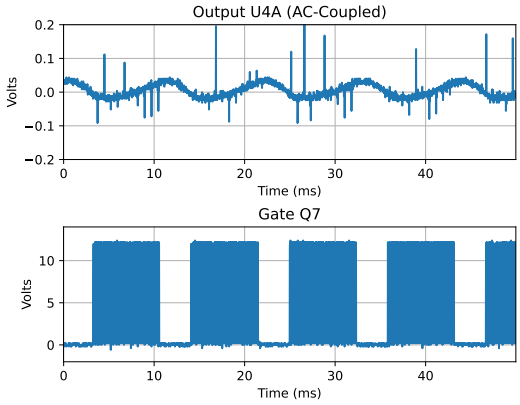


Figure 6.6: The measured output ripple with some EMI being picked up by the probe and the gate voltage.

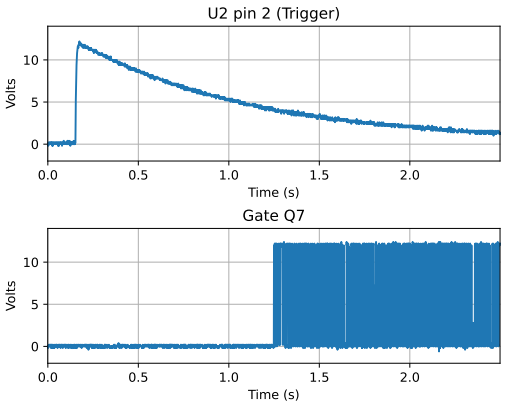


Figure 6.7: The 555 trigger pin signal at startup and the gate voltage.

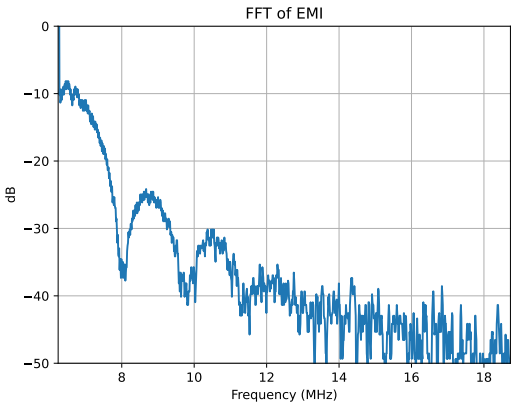


Figure 6.8: The frequency spectrum contents of the emitted EMI.

6.3.5. Turn On Delay

The turn-on delay ensures a stable startup of the system by preventing the startup of the boost converter for approximately $1.14\,\mathrm{s}$. This is done to give the microcontroller enough time to reset when turned on. The delay is created by U2, a 555 timer, that pulls the input of the gate driver to the ground through its own discharge pin. The actual time delay set by R10 and C5, the equation is: $T_{delay} \approx 1.1 \cdot R10 \cdot C5 \approx 1.14\,\mathrm{s}$.

Figure 6.7 shows the waveform at the trigger pin of the 555 timer and the gate voltage. The 555 keeps the converter from turning on until the voltage at the trigger pin is below $\approx 4V$. The oscillation at the gate of Q7 indicates that the boost converter is turned on.

6.4. Further Improvements and Recommendations

The circuit presented here is by no means perfect, there are quite some points for improvement. Here is a quick summary: First the layout of the physical prototype is functional but not all that good (more on this later). Second, the design itself uses comparators, gate drivers, and opamps instead of a dedicated switch mode power supply IC. Third, the output regulation used is rather primitive and could be improved. And lastly, there are energy losses in the inductor, which results in the inductor getting quite hot.

These problems suggest that a slightly different topology could be greatly beneficial. First, the inductor itself could be replaced with a high turn ratio transformer, similar to the circuits shown in [30] [33]. This would have the benefit of requiring a lower voltage switching transistor, and the voltage multiplier circuit is then not needed anymore. Those transformers are not as readily available as they once were, but they are still being made by some manufacturers. Second, the circuit presented here shows some similarity with a current-mode switching regulator like the LT1070, they both measure the current through the inductor and control the height of the voltage spike[34]. Using a dedicated IC greatly reduces the parts count and the physical size of the boost converter.

6.4.1. Layout and EMI

The layout of switch mode power supplies is rather important because it is important not to mix signals. This is done by taking care of a good grounding scheme and accounting for stray inductor-generated flux [34]. Figure 6.4 already showed that the signal can be picked up by an unconnected oscilloscope probe that is near the coil. And figure 6.8 shows the frequency contents of this signal using the fast Fourier transform on the oscilloscope. Of course, the signal can still be picked at greater distances albeit with a lower amplitude. The circuit build had little thought put into the physical layout, besides what is most convenient to lay out on a prototype board.

6.4.2. Radiation Resistance

Radiation greatly affects the characteristics of semiconductors, multiple effects at play affect different types of transistors differently. The threshold voltage of MOSFET transistors tends to shift when exposed to radiation. And the effect on bipolar transistors is typically gain reduction. [14]

The circuit presented here would most likely not survive the effects of radiation. A shift in the threshold voltage for the switching MOSFET is not a big problem, since the gate is driven with a digital signal. However, the MOSFET is still subject to gate rupture, which can cause severe degradation of the transistor. [35] The effect on bipolar transistors poses a bigger problem for the control circuitry used. Base currents would slowly increase and the gain of the comparators and opamp would decrease, leading to a failure of the boost converter.

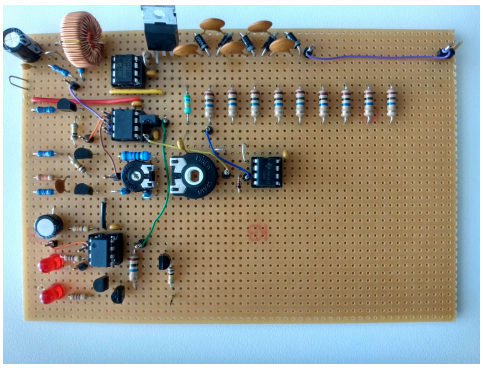


Figure 6.9: The assembled high voltage boost converter.

7

Testing and Validation of the Entire System

In order to assure the system's robustness, dependability, and suitability for the lunar environment, testing and validation are essential. In addition, testing and validation are essential to ensuring that the Electrostatic Dust Removal System meets the requirements of the engineers and scientists who will operate the lunar rover. Evaluating factors such as user-friendliness, integration with the rover's existing systems, power requirements, and overall performance permits the implementation of any required modifications. In this section, we evaluate the results of the system and investigate the extent to which they meet the requirements outlined in the Program of Requirements. First, we tested the driver and controller with the high-voltage supply connected to the ground to see if the gate-source voltages of all half-bridges were behaving as expected. Afterwards, we connected the high voltage terminal to a low voltage power supply of $25\,\mathrm{V}$ to see if the output was as specified by the requirements. Lastly, we connected the high-voltage supply to the driver and increased the voltage step by step in search of overheating components. When the power supply reached a level of $1\,\mathrm{kV}$, the power consumption was measured.

Figure 3.1 now serves as an illustration of the final system in the test procedure. The controller is the Arduino Mega programmed with the code of appendix B. The driver implements the schematic of 4.4 as a custom-printed PCB which we designed for a robust test setup. The control signals are transferred with jumper wires. As the load, an electrode PCB designed by the team doing research on the electrodes is used. The high-voltage supply represented by the schematic in figure 6.2 was implemented with a prototype PCB.

7.1. Testing the Driver and Controller System

After that the gate-source voltages of all half-bridges were measured to behave appropriately, we were ready to validate the efficacy of the system's driver and controller. The objective of the setup was to investigate the system's compliance with the specified requirements and evaluate its functionality under different operating conditions. For the test setup, a few factors were considered. The requisite power for the driver was supplied by a $12\,\mathrm{V}$ power source. This option meets the power requirements specified in requirement MR-I1, which corresponds to *Lunar Zebro*'s power characteristics.

In order to facilitate the connection between the system and an oscilloscope, a $25\,\mathrm{V}$ power source rather than a high-voltage source was utilized. The test configuration included the connection of the driver, Arduino, and a representative electrode board designed by the other team as load. This configuration mimics the actual system configuration and permits testing and validation of the requirements. Different duty cycles and frequencies were used to evaluate the system. By adjusting the duty cycle, the system's response and efficacy at various power levels were assessed. Likewise, the frequency was altered to evaluate the system's capacity to generate block waves within the specified range.

Relevant parameters such as pulse width, rise time, fall time, amplitude, and output ripple were meticulously measured and recorded throughout the testing procedure. The compliance of the system

with the specified criteria was then determined by comparing these measurements to the corresponding requirements (MR-P1, MR-P2, MR-P3, MR-P4, MR-P5).

In order to evaluate the system's efficacy in meeting requirements MR-P1 and MR-P2, testing was performed on the low-voltage driver and controller system. This method was chosen because it was simple to measure and allowed for a thorough evaluation of the system's ability to modify the block wave's frequency within the specified range. By subjecting the driver and controller system to a variety of low-voltage test scenarios, the response and performance of the system were closely monitored and analyzed. The frequency of the block wave was meticulously adjusted, and measurements were performed to confirm its conformance to the specified range of 1 Hz to 100 Hz. Figure 7.1 present the low-voltage measurements of the driver outputs under different operating conditions, showcasing the system's response and performance.

In appendix A, we derived special operating conditions for the system where the rise and fall of two distinct phases occur simultaneously. We tested this, too, by testing the system at a duty cycle of 33% and a high frequency, which is expected to be the only way in which timing errors can occur in the controller as the event will be scheduled very close after one other. Figure 7.2 shows the results of this test.

To determine if MR-P5 is satisfied, we will perform an analysis of the transients of the outputs during a rise and a fall. We define the rise time as the time that it takes to go from 10% to 90% of the final voltage and the fall time is defined the other way around. This is a standard measure of rise and fall time in the field of electrical engineering. Figure 7.3 shows the results of the test.

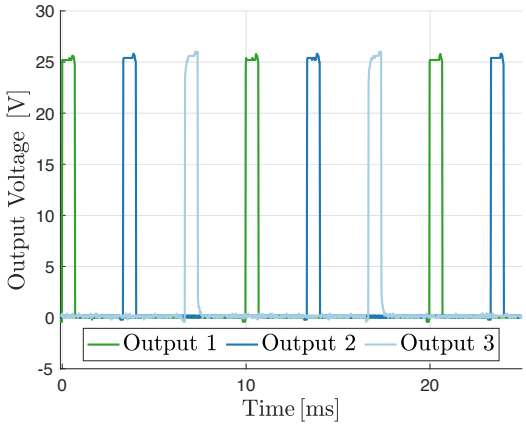
7.1.1. Safety Requirements: Measurement and Results

MR-S3 addresses the dangers associated with loose wires and system malfunctions. In chapter 4, we concluded that the optocouplers are critical in the system's operation, and the system must switch one of the outputs off immediately when a loose wire or a damaged LED at the optocoupler input is detected. We tested this on a breadboard before assembling the final test setup using a low voltage and a small ceramic capacitor of $1nF$ to replace the gate-source terminals of the optocoupler. We tested if the controller stopped all signals as soon as a critical wire was loosened and when a broken optocoupler was used. We accidentally maintained the broken optocouplers during this test, which shows how critical this function is. We discovered that the system behaved as expected, and all appropriate signals went to zero timely.

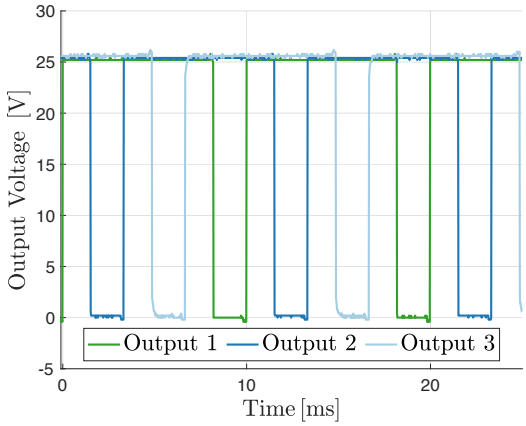
7.1.2. Power Consumption: Measurement and Results

MR-C1 requires testing of the entire system, including the high voltage, the driver, and the controller. The system is powered by a $12\,\mathrm{V}$ source for the driver, which corresponds to *Lunar Zebro*'s power requirements as specified in MR-I1. A computer is linked to the controller. A Tenma power supply model 72-10505 is used for this test, which is specified to be suitable for simple current and voltage measurements. This power supply's Read Back Accuracy is $10\,\mathrm{mV}$ for voltage and $1\,\mathrm{mA}$ for current. The used formula for calculating the average power is $\bar{P} = V_{DC}\bar{I}$. The test determines the power consumption of the entire system by administering a high voltage of approximately $1000\,\mathrm{V}$ and energizing the driver and controller with a $12\mathrm{V}$ source. The accuracy specifications of the Tenma power supply permit precise measurements of the voltage and current, facilitating the calculation of the average power. Across a wide range of operating conditions, the current stayed close to $231\,\mathrm{mA}$ which is equivalent to the power consumption of $2.77\,\mathrm{W}$. Below $9\,\mathrm{Hz}$, the current and power consumption decreased with decreasing frequency.

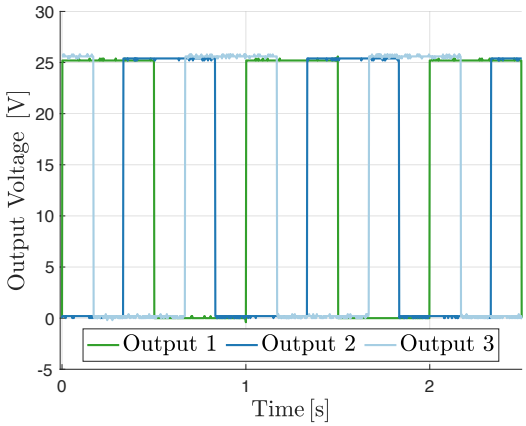
7.2. Results



(a) Maximal frequency of 100 Hz and a duty cycle of 20%.

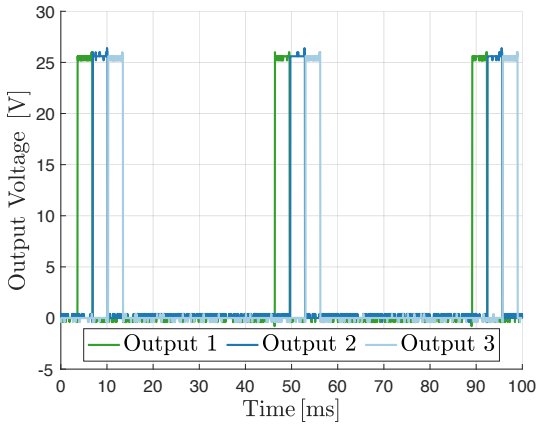


(b) Maximal frequency of 100 Hz and a duty cycle of 80%.

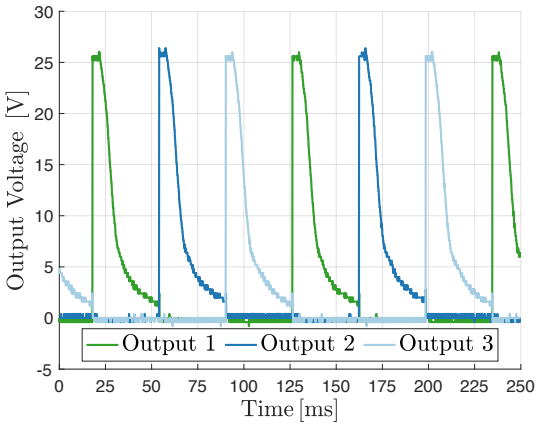


(c) Minimal frequency of 1 Hz and a duty cycle of 50%.

Figure 7.1: Low-voltage measurements of the driver outputs at different operating conditions.

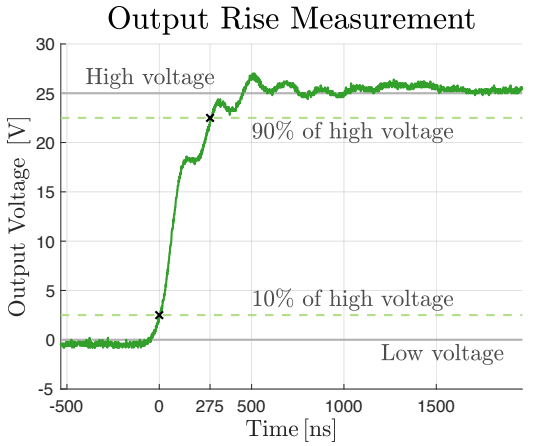


(a) Maximal frequency of 100 Hz and a duty cycle of 30%, which results in timing errors in the controllers causing a fault in intra-phase offset and frequency.

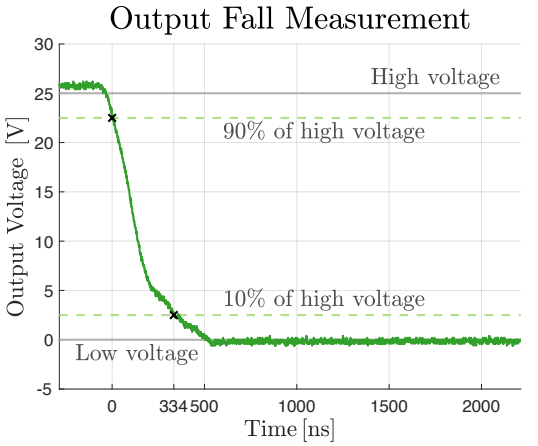


(b) Maximal frequency of 100 Hz and a duty cycle of 33.33%, which results in excessively long optocoupler discharge times causing the output to float.

Figure 7.2: Faulty output signals under very specific conditions that cause timing problems in the controller



(a) Rise time measurement results.



(b) Fall time measurement results.

Figure 7.3: Measurement results of the rise and fall time.

8

Conclusion and Recommendations

Many of the requirements are met by inspection. We completed the final system within 8 weeks and met the deadline, meeting requirement MR-C2. The system was able to generate accurately timed block waves at a high voltage, indicating that the main functional requirement MR-F1 is met. We also see that all interface requirements are met, as the system was able to operate using a $12\,\mathrm{V}$ power supply, the controller could be reprogrammed to specify operating conditions and the system could be connected to the load with 3 outputs. The final system only made use of small components and shows great potential for reduction of the system size, which satisfies MR-C3.

8.1. Interpretation of the Measurement Results

The pulse width is highly adjustable by adjusting the duty cycle of the controller. We were able to generate pulses as short as $500\,\mu\mathrm{s}$ up to $500\,\mu\mathrm{s}$ shorter than the total period, although we did not include the associated oscilloscope data in the report. This indicates that MR-P1 is met. Figure 7.1 shows the system output voltage with a low voltage at different operating conditions.

However, it was discovered that the system encountered problems when operating with duty cycles very near to 33.33% and 66.66% as can be seen in figure 7.2, where faulty output waves are detected. In these instances, the controller's events occurred in rapid succession, resulting in timing errors. This observation is consistent with the analysis presented in appendix A. Consequently, it was determined that the system did not satisfy the MR-P1 requirements for these particular duty cycles.

However, it is essential to observe that this limitation does not substantially affect the functionality of the prototype. Even though the driven 33.33% and 66.66% duty cycles may not produce the desired waveforms by the specifications, the controller still ensures that all events happen in order due to its implementation with a linked list of events, which is a robust safety feature to ensure safe operation. Therefore, even though MR-P1 is not completely met, it is acceptable for the prototype.

According to MR-P3, the system's block wave must have an amplitude of $1\,\mathrm{kV}$. The output voltage of the high-voltage generator can be varied from approximately $150\,\mathrm{V}$ to $1400\,\mathrm{V}$ by adjusting the I_0 variable resistor as stated in Chapter 6. However, the output voltage is not necessarily stable over the entire output voltage range, but the output voltage of $1\,\mathrm{kV}$ is tested to be stable.

When a critical jumper wire was removed in the test setup, all driver signals of the corresponding output go to 0 immediately, indicating a reliable safety mechanism. In the worst-case scenario, the output may float and dissipate slowly due to MOSFET leakage. The activation of the light on the controller indicates a defect or malfunction in the system. The evaluations specified help evaluate the efficacy of these enhancements and permit adjustments to be made to enhance the safety and dependability of the system. This method enables us to determine with absolute certainty that we meet this requirement.

For the power consumption, MR-C1 is met as the system functions below the power limit of $3\,\mathrm{W}$ across all operating conditions. However, for lower frequencies, the power consumption drops. This could indicate that at higher frequencies, the high-voltage power supply is not able to provide the amount of current necessary.

8.2. Validation of Requirements by Analysis

MR-P4 concerns the ripple voltage of the block wave and that it should be lower than 5%. This requires that the high voltage supply should be able to maintain voltage ripple with a maximum of 5%. The high-voltage boost converter can maintain a low ripple. With no load connected to the output, the ripple voltage was measured to be less than 1%. However, the electrode driving circuit was found to be a significant load when the switching frequency was higher than $10\,\mathrm{Hz}$.

Requirement ToR-P3 states that the system should be adaptable by only changing components or settings to create amplitudes that are as high as possible. The solution to this requirement is to choose a high-voltage SiC MOSFET, which is more resistant to radiation and has a larger breakdown strength than Si-based MOSFETs. This allows the system to generate higher amplitudes while still meeting the requirements for a lunar environment. However, an environmental test needs to be conducted to validate the radiation resistance and temperature resistance of the MOSFET, if it is not explicitly specified that the chosen SiC MOSFET is space-grade. Possibly, new transformers with a higher isolation voltage need to be chosen, too.

Transformers and optocouplers are used to accomplish galvanic isolation for the driver circuit, which satisfied MR-S1. The used optocouplers have an isolation voltage of $3550\,\mathrm{Vrms}$ and the transformers have an isolation voltage of at least $1.5\,\mathrm{kV}$. This assures the safety and dependability of the system by preventing potential damage to the electronics. Also, the specific design of the high-voltage supply prevents a fault in the high-voltage side to propagate back into the power supply.

To avoid the risk of a lethal electric discharge, the requirement with the ID code MR-S2 stipulates that the maximal energy in the system in the form of electric charge must be less than $0.5\,\mathrm{J}$ [16]. After performing the requisite measurements, it was determined that the electrostatic energy stored by the system is less than the specified limit of $0.5\,\mathrm{J}$. Consequently, MR-S2 is met, ensuring that the system maintains a secure level of energy storage and reducing the risk of a fatal electric charge.

8.3. Conclusion

Considering the difficulties posed by the lunar environment and the limited dimensions of the rover, the problem statement emphasized the need for an effective dust removal system on the *Lunar Zebro*. Our proposed solution, the Electrostatic Dust Removal System, is a promising method for reducing the adhesion of dust particles to the surface of the rover. A reliable driving circuit and high-voltage generator are critical for the dust removal system and have been designed in this thesis. The system generates the necessary high-voltage rectangular waves to ensure efficient dust removal.

Throughout the design process, we focused on developing the necessary driver electronics for the electrostatic dust removal system. By studying existing literature and incorporating innovative design techniques, we successfully created a driving circuit that generates the appropriate waveform and voltage levels required for effective dust removal.

We can certainly conclude that it is possible to construct driver electronics for an electrostatic dust cleaning system for the *Lunar Zebro* based on the results of testing and validation. The implemented technology has proven its ability to successfully remove dust particles from the surface of the rover, consequently improving its performance and longevity. It is vital to emphasize. However, there is still a lot of work to be done in the next iterations of the prototype. Specifically, the next steps include minimization of the system size, reducing the power consumption and possibly increasing the output voltage. But most importantly, the next iterations should make the system space-grade using the suggestions in this thesis as a starting point.

8.4. Recommendations

For the next engineering cycle, the focus could be on minimizing design size and making the design space-grade. The range of operating conditions for the duty cycle and frequency can be narrowed down after conclusions about their optima are known. Also, the system could scale up to a higher voltage if necessary.

If it is not necessary to use higher voltages than $1.5\,\mathrm{kV}$, optoMos Relays can be used instead of MOSFETs with a gate driver. The controller design would have to change slightly, too, but can still make use of the same program structure. On the other hand, if measurements indicate that a higher voltage is required, radiation-resistant SiC MOSFETs should be used. Additionally, the used driver

circuit components could change to space-grade versions. Chapter 4 can be used as a guide, with most importantly, a constraint on leakage current of the optocouplers and diodes D1 and D2 in figure 4.4. The limit of this leakage current is set by equations 4.13 and 4.7. The exact equation for the optocoupler time will depend on the CTR-I_F characteristic of the specific optocoupler and result in an equation similar to 4.17.

The controller code has to be made resistant to the timing errors encountered for specific duty cycles. This could be achieved by implementing new functionality for events that follow each other closely. They should then be executed in order but be triggered by one shared CTC interrupt. The delay time would be the sum of the delay times of the simultaneous events.

As for the high-voltage generator, a new design is necessary to make the system more compact, efficient, and radiation resistant. As mentioned in section 6.4, these problems can be solved using a high turn ratio transformer and a dedicated switching regulator IC. This also has the benefit of requiring a lower voltage switching transistor, which can also be easier to find a radiation-hardened version of. If even higher output voltages are required, then a high-voltage transformer in combination with a voltage multiplier may prove to be a viable option. Such a circuit was also commonly found in old CRT-based oscilloscopes.

A

Modelling Switching Behaviour and the Electrical Load

In this appendix, we will analyze the switching behaviour of the system and derive an equivalent electrical model for the load. To start with, we will give each output to which an interconnected set of electrodes is connected an index i so that

$$i \in I = \{1, 2, 3\} \tag{A.1}$$

First, we will define states in which a single output can be, as well as the timing of the state transitions. Second, we derive a state for the entire system and derive three different operating modes. The insights about the operation will be very useful for the next step: modelling the load. This model can be easily extended to an arbitrary number of phases, but in this appendix, we assume that the number of phases is 3.

A.1. State of a Single Output

We will now develop a classification of the state of a single output and specify the timing of the state transitions. Requirement MR-F1 states that a rectangular wave must be present, which leads to the definition of 4 different output states, collected in set Ω:

$$\Omega = \{\text{rising}, \text{high}, \text{falling}, \text{low}\} \tag{A.2}$$

We assume that all transients happen during the rising and falling state, and that output in the rising or falling states can be described as a DC signal. In this case, we neglect the ripple voltage to simplify the model.

To assign a state to each output i, we define a function $s_i' : \mathbb{R} \to \Omega$. As the signal at each output is periodic, we can define a period $T \in \mathbb{R}^+$ and say that $\forall k \in \mathbb{Z}\left(s_i'(t) = s_i'(t + kT)\right)$. This allows us to define a new function $s_i : [0, T) \to \Omega$ that maps the time elapsed since the start of a period to a state of the output. Now not that a rectangular wave at an output i can only through the states in one single order, which can be represented by the directed graph visualized in figure A.1.

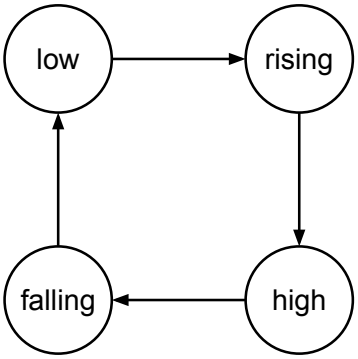


Figure A.1: Possible state transitions of a single output.

Moreover, the timing of the state transitions is set by the period T, the duty cycle $D \in (0,1)$, the rise time $t_r \in [0,T)$ and the fall time $t_f \in [0,T)$. This allows us to completely define $s_i(t)$. First, we define the time at which a phase starts rising: output 1 starts rising at $t = 0$, output 2 starts rising at $t = \frac{T}{3}$ and output 3 starts rising at phase $t = 2\frac{T}{3}$. Equivalently, we say that phase i starts rising at $t = (i-1)\frac{T}{3}$. Then, output i will be rising for t_r, after which it will be in the high state which is the only allowed state transition as visualized in figure A.1. The output will be in the high state for a duration of DT and afterwards in the falling state for a duration of t_f. Then, the output is in the low state until the end of the period. We have arrived at a definition for the system state s_i'

$$s_i'(t) = \begin{cases} \text{rising} & \text{if} \quad \exists k \in \mathbb{Z} : t - \left(k + \frac{i-1}{3}\right) T \in [0, t_r) \\ \text{high} & \text{if} \quad \exists k \in \mathbb{Z} : t - \left(k + \frac{i-1}{3}\right) T \in [t_r, t_r + DT) \\ \text{falling} & \text{if} \quad \exists k \in \mathbb{Z} : t - \left(k + \frac{i-1}{3}\right) T \in [t_r + DT, t_r + DT + t_f) \\ \text{low} & \text{if} \quad \exists k \in \mathbb{Z} : t - \left(k + \frac{i-1}{3}\right) T \in [t_r + DT + t_f, T) \end{cases} \tag{A.3}$$

For programming the controller — which is more focused on state transitions than on intervals — it is useful to define the timings of the state transitions of $s_i(t)$, as the controller will schedule all state transitions of a single period when it starts up. If we denote the directed graph of figure A.1 as $G = (V, E)$ with $V = \Omega$ the vertices and $E \subset \Omega \times \Omega$ the arcs representing the allowed state transitions, we can define a state transition timing function for each phase i as $T_i : E \to [0,T)$ as follows:

$$T_i(E) = \begin{cases} g_T\left((i-1)\frac{T}{3}\right) & \text{if} \quad E = (\text{low}, \text{rising}) \\ g_T\left((i-1)\frac{T}{3} + t_r\right) & \text{if} \quad E = (\text{rising}, \text{high}) \\ g_T\left((i-1)\frac{T}{3} + t_r + DT\right) & \text{if} \quad E = (\text{high}, \text{falling}) \\ g_T\left((i-1)\frac{T}{3} + t_r + DT + t_f\right) & \text{if} \quad E = (\text{falling}, \text{low}) \end{cases} \tag{A.4}$$

with $g_T : \mathbb{R} \to [0,T)$ defined as

$$g_T(t) = t - \left\lfloor \frac{t}{T} \right\rfloor T \tag{A.5}$$

With $\lfloor \cdot \rfloor$ the floor function. We will now continue to define the behaviour of the entire system.

A.2. Limit on the Number of Simultaneously Changing Outputs

The next step would be to classify the state of the entire system. If we would model the state of the entire system with a function $\mathbf{s} : [0,T) \to \Omega^3$, we would have $4^3 = 64$ different output states. This is not

very helpful in analyzing the system's behaviour. Therefore, we will determine the subset of possible system states that can realistically occur when the requirements are met.

In this section, we will now prove that no two voltages will be rising at the same time, and no two voltages will be falling at the same time if and only if $t_r < \frac{T}{3}$. The last condition is the case if the requirements are met. By equation A.3, we know that an arbitrary node $i \in I$ is rising if and only if

$$t \in \bigcup_{k\in\mathbb{Z}} \left[(i-1)\frac{T}{3} + kT, t_r + (i-1)\frac{T}{3} + kT\right)$$

Suppose that two distinct nodes $i, j \in I$ are rising simultaneously. This requires that

$$\bigcup_{k_1\in\mathbb{Z}} \left[(i-1)\frac{T}{3} + k_1T, t_r + (i-1)\frac{T}{3} + k_1T\right) \cap \bigcup_{k_2\in\mathbb{Z}} \left[(j-1)\frac{T}{3} + k_2T, t_r + (j-1)\frac{T}{3} + k_2T\right) \neq \emptyset$$

Equivalently,

$$\exists k_1, k_2 \in \mathbb{Z}\left(\left[(i-1)\frac{T}{3} + k_1T, t_r + (i-1)\frac{T}{3} + k_1T\right) \cap \left[(j-1)\frac{T}{3} + k_2T, t_r + (j-1)\frac{T}{3} + k_2T\right) \neq \emptyset\right)$$

Take any fixed k_1 and k_2 for which rising times of the voltages overlap as we supposed. In this case, there are only two intervals of equal length t_r to consider, specified in the last statement. Because the intervals are of equal length t_r, we know that the intervals overlap if and only if one of the following 3 statements holds:

1. $(i-1)\frac{T}{3} + k_1T < (j-1)\frac{T}{3} + k_2T$ and $t_r + (i-1)\frac{T}{3} + k_1T > (j-1)\frac{T}{3} + k_2T$
   (The first interval starts before the second one)
2. $(i-1)\frac{T}{3} + k_1T > (j-1)\frac{T}{3} + k_2T$ and $(i-1)\frac{T}{3} + k_1T < t_r + (j-1)\frac{T}{3} + k_2T$
   (The first interval starts after the second one)
3. $(i-1)\frac{T}{3} + k_1T = t_r + (j-1)\frac{T}{3} + k_2T$
   (The intervals start at the same time)

The first case We rewrite the cases as follows by subtracting $(j-1)\frac{T}{3} + k_2T$ from the right side of each inequality and equation and define $p := (i-j) \in \{-2, -1, 1, 2\}$ (because $i \neq j$ and $i, j \in I$) and $q := (k_2 - k_1) \in \mathbb{Z}$. Then we find the following:

1. $p\frac{T}{3} < qT$ and $t_r + p\frac{T}{3} > qT$
   (The first interval starts before the second one)
2. $p\frac{T}{3} > qT$ and $p\frac{T}{3} < t_r + qT$
   (The first interval starts after the second one)
3. $p\frac{T}{3} = t_r + qT$
   (The intervals start at the same time)

For the first two intervals, we reformulate

1. $0 < \left(q - \frac{p}{3}\right)T < t_r$
2. $0 < \left(\frac{p}{3} - q\right)T < t_r$

As $t_r < T$ by definition, we see that $\left|q - \frac{p}{3}\right| < 1$ Also, because $|\frac{p}{3}| < \frac{2}{3}$, we see that $q < 1$ and because $q \in \mathbb{Z}$, we conclude that $q = 0$. Finally, we see that to satisfy these equations, we require that $t_r > \frac{T}{3}$ with solutions $p = -1$ for case 1 and $p = 1$ for case 2 or that $t_r > \frac{2T}{3}$ with solutions $p \in \{-1, -2\}$ f

for case 1 and $p \in \{1, 2\}$ for case two. This both contradicts the assumption that $t_r < \frac{T}{3}$ and therefore cases 1 and 2 can not hold.

The only way in which we could solve the assumption is case 3. By solving the equality for q, we get:

$$q = \frac{p}{3} - \frac{t_r}{T}$$

As q is an integer by definition, $\frac{p}{3} - \frac{t_r}{T}$ must be an integer, too. Let us now define $\alpha \in (0, 1)$ such that $t_r = \alpha\frac{T}{3}$, which is a valid step because we assumed that $0 < t_r < \frac{T}{3}$ at the beginning of the proof. We rewrite:

$$q = \frac{p + \alpha}{3}$$

Therefore, $p + \alpha$ must be divisible by 3. This requires that α is an integer, because p is an integer by definition, and we arrive at a contradiction because $\alpha \in (0, 1)$. Therefore, case 3 can never hold. We have proven by contradiction that two distinct voltages can never be rising at the same time when $t_r < \frac{T}{3}$.□

Similarly, if and $t_f < \frac{T}{3}$ then no two distinct nodes are falling at the same time.

A.3. Classification of System Switching Behaviour

Equation A.4 defines the start of a rise and the start of a fall of each phase. We see can easily see that in the entire system, one phase will be rising every $\frac{T}{3}$ seconds and one phase will be falling every $\frac{T}{3}$ seconds. Moreover, the starts of the rising and falling intervals occur at the same frequency, which allows us to define two different operation modes if we assume a constant frequency and duty cycle. In operation mode 1, the rise and fall intervals of the entire system will not overlap. In operation mode 2, the rise and fall intervals will overlap each other.

We will now derive conditions for each operation mode. We know that the system is in operation mode 2 if and only if a rising interval and a falling interval have a nonempty intersection. We know that output 1 starts rising at $t = 0$. If output 2 or 3 is falling at this time, we conclude that the system is in operation mode 2. We will consider the time in $[0, T)$. Then, the rising interval of state 1 is $[0, t_r)$ by equation A.3. The falling interval of output 2 is the interval $[\frac{T}{3} + t_r + DT, \frac{T}{3} + t_r + DT + t_f)$ remapped to the interval $[0, T)$. So only if the upper bound of the interval is bigger than T, the interval will be near 0 again. To overlap with the rising interval of output 1, we require two conditions for output 2:

1. The upper bound exceeds the period: $t_r + DT + t_f > T$
2. The lower bound does not exceed the rising interval of output 1 in the next period: $t_r + DT < T + t_r$

By rewriting both inequalities, we arrive at the condition that $\frac{2}{3} - \frac{t_r + t_f}{T} < D < \frac{2}{3}$. Similarly, the falling interval of output 3 only overlaps the rising interval for if $\frac{1}{3} - \frac{t_r + t_f}{T} < D < \frac{1}{3}$

$$\text{The operation mode is 2} \leftrightarrow \qquad D \in \frac{2}{3} - \frac{t_r + t_f}{T} < D < \frac{2}{3} \cup \frac{1}{3} - \frac{t_r + t_f}{T} < D < \frac{1}{3} \tag{A.6}$$

At a maximum frequency of $100\,\mathrm{Hz}$ and a rise and fall time of the maximum allowed value of $50\,\mu\mathrm{s}$, we could say that the total interval width of D for which operation mode 2 occurs is equal to $2\frac{t_r + t_f}{T} = 0.02$. If we consider a realistic operation range of D to be $[0.05, 0.95]$, we could say that operation mode 2 will only occur at 2.2% of the possible values for D. We have concluded that the actual rise and fall times are much lower, and for lower frequencies, this percentage will be even lower. We therefore decided to model the load as if only operation mode 1 exists.

A.4. Simplifying the Load Model

For modelling the loads, we assume the inductive properties of the load to be negligible when compared to the capacitive properties. This has also been discussed with the team designing the electrodes. As different interconnected sets of electrodes are supposed to be isolated, we also assume that the load

has no part. Each interconnected set of electrodes, simply denoted as “electrode i”, is represented by an electrical node. The model will consist of an equivalent capacitor between each distinct node i and j with capacitance $C_{ij} = C_{ji}$. This capacitor models the ability of charge difference in the electrodes to create the required electric field for repelling the lunar dust. Furthermore, we assume that between any set of connected electrodes with index i and the ground, an equivalent capacitor C_{Gi} exists, as the electrodes will be placed at some distance away from the ground plate of the solar panel and any non-zero voltage applied on a set of connected electrodes will therefore create a significant electric field between the electrode and the ground plate. This concludes our electrical load model. Figure A.2 shows the schematic of this equivalent model.

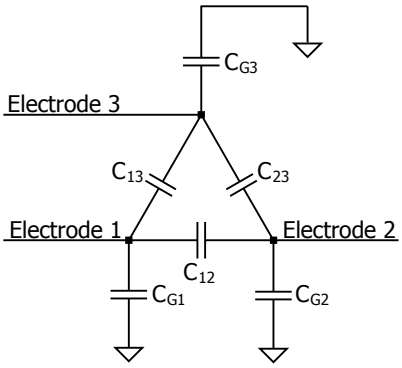


Figure A.2: Schematic of the equivalent electrical model of the electrodes

This model is very hard to work with. Luckily, we have previously derived that we only have to consider operation mode 1, in which only one node is either rising or falling at the same time. As the rising or falling nodes will contain all non-DC voltages in the system, this will simplify the model a lot. For modelling the load, we will now say that the node with index i is either rising or falling.

The first important notion is that the capacitor between every node with a DC voltage can be modelled as an open circuit, which is a result of basic electrical circuit theory. This includes the nodes that are not rising or falling and the ground node. We are therefore only left with capacitors C_{ij} with $j \neq i$ and C_{Gi}. We know that the other nodes are either high or low. Let $I_L \subseteq I \setminus \{i\}$ denote the subset of indices of nodes that are in the low state and $I_H \subseteq I \setminus \{i\}$ denote the subset of indices of nodes that are in the high state. We also know that $I_H \cap I_L =$ and $I_H \cup I_L = I \setminus \{i\}$. As all high nodes have the same voltage, we can see their capacitors connected to changing node i as parallel which allows us to add their capacitances into an equivalent capacitor with value $C_H = \sum_{j \in I_H} C_{ij}$. Similarly, we define $C_L = C_{Gi} + \sum_{j \in I_L} C_{ij}$. The model is visualized in figure A.3. It includes a black box with a source that represents the source driving the electrode through an unknown driver network.

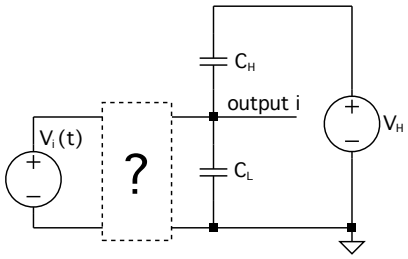


Figure A.3: Simplified load model

We will now apply the method of superposition. When $V_i(t)$ is shorted, the high-voltage source is

a DC source and the capacitors under this source will therefore be open circuits. The source does not affect the circuit. When the DC high-voltage source is shorted, the source $V_i(t)$ will see C_L and CH_H as parallel capacitors, which allows us to add their values. We arrive at our final source model, which is a single capacitor with value C_i.

$$C_i = C_{Gi} + \sum_{j \in I \setminus \{i\}} C_{ij} \tag{A.7}$$

The equivalent circuit is shown in figure A.4.

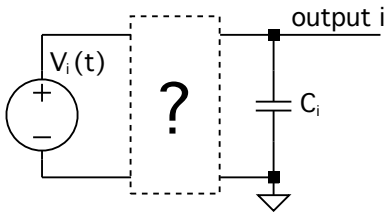


Figure A.4: The final equivalent load model when only one output is changing at a time. The value of C_i is given by equation A.7.

B

Controller code

B.1. Main Arduino File

This is the code that the Arduino runs. The function “setup” is running once at the start of the program. Afterwards, the function “loop ” keeps repeating until the power is disconnected or a reset is activated. Only the ISR function (Interrupt Service Routine) can interrupt the loop, in this program when timer 1 causes an interrupt.

```
/* Carli Bruinsma, June 5 2023 A.D.
CONNECTIONS on ARDUINO MEGA
High voltage control:
  ON/OFF:     Pin D?

Phase 1:
  LOW_UP:     Pin D5    (PE3, PWM by Timer 3A)
  LOW_DOWN:   Pin D10   (PB4)
  LOW_READ:   Pin A0
  HIGH_UP:    Pin D6    (PH3, PWM by Timer 4A)
  HIGH_DOWN:  Pin D11   (PB5)
  LOW_READ:   Pin A1

Phase 2:
  LOW_UP:     Pin D2    (PE4, PWM by Timer 3B)
  LOW_DOWN:   Pin D18   (PD3)
  LOW_READ:   Pin A2
  HIGH_UP:    Pin D3    (PE5, PWM by Timer 3C)
  HIGH_DOWN:  Pin D19   (PD2)
  LOW_READ:   Pin A3

Phase 3:
  LOW_UP:     Pin D7    (PH4, PWM by Timer 4B)
  LOW_DOWN:   Pin D20   (PD1)
  LOW_READ:   Pin A4
  HIGH_UP:    Pin D8    (PH5, PWM by Timer 4C)
  HIGH_DOWN:  Pin D21   (PD0)
  LOW_READ:   Pin A5
*/

//behaviour specification
#define FREQUENCY           100    // [Hz]. 1Hz-50Hz
#define DUTY_CYCLE          40    // [%]. 5%-95%

```

```
35 //PWM settings for keeping a MOSFET on through a transformer
36 #define PWM_KEEP_ON_T       399   // 200µs
37 #define PWM_KEEP_ON_PULSE   3     // 2µs
38 //PRESCALER 8 --> resolution of 500ns. For CTC interrupt
39 #define RESOLUTION          0.0000005
40
41 //Time needed to turn a MOSFET off through an optocoupler
42 //PRESCALER 8 --> resolution of 500ns
43 #define OPTO_TIME           200   //µs
44
45 #include "events.h"
46 #include <math.h>
47
48 // GLOBAL VARS THAT DEFINE ALL PINS AND REGISTERS AND BITS
49 // First low-side, then high-side
50 volatile uint8_t*          PWM_REGS[3][2]     = {{&TCCR3A, &TCCR4A},
    ↪  {&TCCR3A, &TCCR3A}, {&TCCR4A,&TCCR4A}};
51 const volatile uint8_t     PWM_BITS[3][2]     = {{COM3A1, COM4A1}, {COM3B1,
    ↪  COM3C1}, {COM4B1, COM4C1}};
52
53 volatile uint8_t*          TRAFO_REGS[3][2]   = {{&PORTE, &PORTH}, {&PORTE,
    ↪  &PORTE}, {&PORTH,&PORTH}};
54 const volatile uint8_t     TRAFO_BITS[3][2]   = {{PE3, PH3}, {PE4, PE5},
    ↪  {PH4, PH5}};
55
56 volatile uint8_t*          OPTO_REGS[3][2]    = {{&PORTB, &PORTB}, {&PORTD,
    ↪  &PORTD}, {&PORTD, &PORTD}};
57 const volatile uint8_t     OPTO_BITS[3][2]    = {{PB4, PB5}, {PD3, PD2},
    ↪  {PD1, PD0}};
58
59 const uint8_t              ADC_PINS[3][2]     = {{0, 1}, {2, 3}, {4, 5}};
60
61 const uint8_t              TRAFO_PINS[3][2]   = {{5, 6}, {2, 3}, {7, 8}};
62 const uint8_t             OPTO_PINS[3][2]    = {{10, 11}, {18, 19}, {20, 21}};
63
64 // GLOBAL VARS TO KEEP TRACK OF SYSTEM STATE
65 bool                       broken[3]          = {0,0,0};
66 volatile bool              flag               = 0;
67 volatile uint16_t          next_CTC_time;
68 Event*                     event_pointer      = NULL;
69
70 // TIMING CONSTANTS
71 const uint32_t             opto_cycles        = 2 * OPTO_TIME;
72 const uint32_t            on_cycles          = ((float) DUTY_CYCLE / ((float)
    ↪  FREQUENCY * RESOLUTION * 100));
73 const uint32_t             period_cycles      = (1 / (float) FREQUENCY) /
    ↪  RESOLUTION;
74 const uint32_t             delta_t_cycles     = round((float) period_cycles /
    ↪  3.0);
75
76 void setup() {
77   // SET PIN MODES: PWM PINS, DIGITAL OUTPUTS, LED
78   for(int i = 0; i < 3; i++)
79   {
80     for(int j = 0; j < 2; j++)
81     {
```

```
82        pinMode(TRAFO_PINS[i][j], OUTPUT);
83        pinMode(OPTO_PINS[i][j], OUTPUT);
84      }
85    }
86    pinMode(LED_BUILTIN, OUTPUT);
87    PORTB &= ~(1 << PB7); //turn LED off
88
89    // GENERATE EVENTS FOR EVERY PHASE WITH CHRONOLOGICAL TIME ASSIGNED TO
      ↪ THEM
90    for(uint8_t setup_phase_counter = 0; setup_phase_counter < 3;
      ↪ setup_phase_counter++)
91    {
92      for(uint8_t high = 0; high < 2; high++)
93      {
94        int32_t start_time;
95        start_time    = high*(opto_cycles + on_cycles);     // so 0 when low
      ↪ and before fall when high
96        start_time   += setup_phase_counter*delta_t_cycles; // phase ofset
97        //time may not exceed a period: then it "wraps around" to 0
98        if(start_time >= period_cycles)
99          start_time -= period_cycles;
100       Event* event1  = new OptoEvent(setup_phase_counter,  start_time,
101           OPTO_REGS[setup_phase_counter][high],
      ↪ OPTO_BITS[setup_phase_counter][high],
102           PWM_REGS[setup_phase_counter][high],
      ↪ PWM_BITS[setup_phase_counter][high],
103           ADC_PINS[setup_phase_counter][high]);
104       addEventChronologically(event_pointer, event1);
105       start_time   += opto_cycles;                              // end of
      ↪ change
106       Event* event2         = new TrafoEvent(setup_phase_counter,
      ↪ start_time,
107           TRAFO_REGS[setup_phase_counter][1-high],
      ↪ TRAFO_BITS[setup_phase_counter][1-high],
108           PWM_REGS[setup_phase_counter][1-high],
      ↪ PWM_BITS[setup_phase_counter][1-high],
109           OPTO_REGS[setup_phase_counter][high],
      ↪ OPTO_BITS[setup_phase_counter][high]);
110       addEventChronologically(event_pointer, event2);
111     }
112   }
113
114   // MAKE THE EVENT TIMES DIFFERENTIAL
115   Event* first  = event_pointer;
116   while(event_pointer->getNext() != NULL)
117   {
118     uint32_t cycles_till_next = event_pointer->getNext()->getTime() -
      ↪ event_pointer->getTime();
119     event_pointer->setTime(cycles_till_next -1);
120     //add "void blocks" to avoid CTC interrupt counter overflow
121     int num_void_blocks = floor( (float) event_pointer->getTime() /
      ↪ 65536.0);
122     for(int i = 0; i < num_void_blocks; i++)
123     {
124       insertEvent(event_pointer, new VoidEvent());
125       event_pointer = event_pointer->getNext();
```

```
126       }
127       event_pointer = event_pointer->getNext();
128     }
129     //also make the last one differential (slightly different!)
130     uint32_t cycles_till_next = period_cycles - event_pointer->getTime();
131     event_pointer->setTime(cycles_till_next -1);
132     //add "void blocks" to avoid CTC interrupt counter overflow
133     int num_void_blocks = floor( (float) event_pointer->getTime() / 65536.0);
134     for(int i = 0; i < num_void_blocks; i++)
135     {
136       insertEvent(event_pointer, new VoidEvent());
137       event_pointer = event_pointer->getNext();
138     }
139
140     // 3. CLOSE THE LOOP
141     event_pointer->setNext(first);
142     event_pointer = first;
143
144     //set ADC prescaler to 8: ADPS2-ADPS0 = 011 (SPEEEEEEDDDDD!!! 10µs
    ↪  instead of 100µs)
145     ADCSRA &= ~(1 << ADPS2);
146     ADCSRA |= (1 << ADPS1) | (1 << ADPS0);
147
148     // PWM SETUP FOR TIMER 3 AND 4
149     TCCR3A  = 0x00;                         // clear timer 3 registers
150     TCCR3B  = 0x00;
151     TCCR4A  = 0x00;                         // clear timer 4 registers
152     TCCR4B  = 0x00;
153     TCCR3A  = (1 << WGM31);                 // Timer 3 in Fast PWM (mode 14),
    ↪  prescaler 8
154     TCCR3B  = (1 << WGM33) | (1 << WGM32) | (1 << CS31);
155     TCCR4A  = (1 << WGM41);                 // Timer 4 in Fast PWM (mode 14),
    ↪  prescaler 8
156     TCCR4B  = (1 << WGM43) | (1 << WGM42) | (1 << CS41);
157     ICR3    = PWM_KEEP_ON_T;              // PWM TOP settings to set frequency
158     ICR4    = PWM_KEEP_ON_T;
159     OCR3A   = PWM_KEEP_ON_PULSE;          // Set all PWM duty cycles
160     OCR3B   = PWM_KEEP_ON_PULSE;
161     OCR3C   = PWM_KEEP_ON_PULSE;
162     OCR4A   = PWM_KEEP_ON_PULSE;
163     OCR4B   = PWM_KEEP_ON_PULSE;
164     OCR4C   = PWM_KEEP_ON_PULSE;
165
166     // CTC SETUP FOR TIMER 1
167     cli();                                  // Disable global interrupts
168     TCCR1A  = 0;                            // clear timer 1 registers
169     TCCR1B  = (1 << WGM12) | (1 << CS11); // Set timer 1 to CTC mode,
    ↪  prescaler 8
170     OCR1A   = next_CTC_time;                // Set the compare value
171     TCNT1   = 0;                           // Set the starting value for Timer 1
172     TIMSK1  = (1 << OCIE1A);                // Enable timer 1 CTC interrupt
173     sei();                                  // Enable global interrupts
174 }
175
176 // Interrupt handler
177 ISR(TIMER1_COMPA_vect) {
```

```
178   OCR1A   = next_CTC_time;  // Set new time
179   flag    = 1;           // Set flag
180 }
181
182 // Main loop
183 void loop() {
184   if(flag == 1)
185   {
186     event_pointer->execute();
187     event_pointer   = event_pointer->getNext();
188     next_CTC_time   = event_pointer->getTime();
189     flag = 0;
190   }
191 }
```

B.2. Events C++ Library

As Arduino does not treat header files like a normal C++ compiler, the .h file combines the usual contents of a header file (.h) and a C++ file (.cpp) in one file.

```
1  /*
2   *  Carli Bruinsma, June 6 2023 A.D.
3   *  This file contains a class for all pin events for the prototype
4   *  of the high voltage block wave driver.
5  */
6  #ifndef EVENTS_H
7  #define EVENTS_H
8  #define VOLTAGE_MIN 102 //minimally 0.5V  --> 1023 * 0.5 / 5 = 102
9  #define VOLTAGE_MAX 409 //maximally 2V    --> 1023 *  2  / 5 = 409
10 #include <stdint.h>
11
12 extern bool                        broken[3];
13
14 extern volatile uint8_t*           PWM_REGS[3][2];
15 extern const volatile uint8_t      PWM_BITS[3][2];
16 extern volatile uint8_t*           OPTO_REGS[3][2];
17 extern const volatile uint8_t      OPTO_BITS[3][2];
18 extern volatile uint8_t*           TRAFO_REGS[3][2];
19 extern const volatile uint8_t      TRAFO_BITS[3][2];
20
21 class Event
22 {
23   protected:
24     uint32_t          time;
25     Event*            next;
26     uint8_t           phase;
27   public:
28     Event(uint8_t event_phase, uint32_t event_time);
29     void              setNext(Event* nextEvent);
30     Event*            getNext();
31     void              setTime(uint32_t cycles);
32     uint32_t          getTime();
33     virtual void      execute() { };
34
35     friend Event*     addEventChronologically(Event*& eventlist, Event*
    ↪  event);
36     friend void       insertEvent(Event* eventlist, Event* event);
```

```
37  };
38  //constructor
39  Event::Event(uint8_t event_phase, uint32_t event_time)
40  {
41    phase = event_phase;
42    time  = event_time;
43    next  = NULL;
44  }
45  //for setting and getting timing properties
46  void Event::setNext(Event* nextEvent)
47  {
48    next  = nextEvent;
49  }
50  Event* Event::getNext()
51  {
52    return  next;
53  }
54  void Event::setTime(uint32_t cycles)
55  {
56    time  = cycles;
57  }
58  uint32_t Event::getTime()
59  {
60    return  time;
61  }
62
63  class OptoEvent: public Event
64  {
65    private:
66      volatile uint8_t* opto_reg;
67      uint8_t           opto_bit;
68      volatile uint8_t* PWM_reg;
69      uint8_t           PWM_bit;
70      uint8_t           ADC_pin;
71    public:
72      OptoEvent(uint8_t event_phase, uint32_t event_time,
73      volatile uint8_t* new_opto_reg, uint8_t new_opto_bit,
74      volatile uint8_t* new_PWM_reg, uint8_t new_PWM_bit,
75      uint8_t new_ADC_pin)
76      : Event(event_phase, event_time)
77      {
78        opto_reg      = new_opto_reg;
79        opto_bit      = new_opto_bit;
80        PWM_reg       = new_PWM_reg;
81        PWM_bit       = new_PWM_bit;
82        ADC_pin       = new_ADC_pin;
83      }
84
85      virtual void      execute();
86  };
87
88  void OptoEvent::execute()
89  {
90    if(!broken[phase])
91    {
92      *PWM_reg          &= ~(1 << PWM_bit);
```

```
93      *opto_reg          |= (1 << opto_bit);
94      uint16_t voltage    = analogRead(ADC_pin);
95      if(voltage > VOLTAGE_MAX || voltage < VOLTAGE_MIN)
96      {
97        broken[phase]     = 1;
98        //turn all pins off
99        for(uint8_t i = 0; i < 2; i++)
100       {
101         *PWM_REGS[phase][i]   &= ~(1 << PWM_BITS[phase][i]);
102         *TRAFO_REGS[phase][i] &= ~(1 << PWM_BITS[phase][i]);
103         *OPTO_REGS[phase][i]  &= ~(1 << PWM_BITS[phase][i]);
104       }
105      PORTB             |= (1 << PB7); //turn LED on
106     }
107   }
108 }
109
110 class TrafoEvent: public Event
111 {
112   private:
113     volatile uint8_t* trafo_reg;
114     uint8_t           trafo_bit;
115     volatile uint8_t* PWM_reg;
116     uint8_t           PWM_bit;
117     volatile uint8_t* opto_reg;
118     uint8_t           opto_bit;
119   public:
120     TrafoEvent(uint8_t event_phase, uint32_t event_time,
121     volatile uint8_t* new_trafo_reg, uint8_t new_trafo_bit,
122     volatile uint8_t* new_PWM_reg, uint8_t new_PWM_bit,
123     volatile uint8_t* new_opto_reg, uint8_t new_opto_bit)
124     : Event(event_phase, event_time)
125     {
126       trafo_reg     = new_trafo_reg;
127       trafo_bit     = new_trafo_bit;
128       PWM_reg       = new_PWM_reg;
129       PWM_bit       = new_PWM_bit;
130       opto_reg      = new_opto_reg;
131       opto_bit      = new_opto_bit;
132     }
133
134     virtual void      execute();
135 };
136
137 void TrafoEvent::execute()
138 {
139   if(!broken[phase])
140   {
141     *opto_reg   &= ~(1 << opto_bit);
142     *trafo_reg  |= (1 << trafo_bit);
143     delayMicroseconds(3);
144     *trafo_reg  &= ~(1 << trafo_bit);
145     *PWM_reg    |= (1 << PWM_bit);
146   }
147 }
148
```

```
149 class VoidEvent: public Event
150 {
151   public:
152     VoidEvent() : Event(NULL, 65535){ };
153     virtual void      execute() {}
154 };
155 
156 Event* addEventChronologically(Event*& eventlist, Event* event)
157 {
158   // NB: eventlist must be already chronological!
159   if (eventlist == NULL)
160   {
161     // In case there is nothing in the list
162     eventlist = event;
163   }
164   else if (eventlist->getTime() > event->getTime())
165   {
166     // In case it must be the first in the list
167     event->setNext(eventlist);
168     eventlist = event;
169   }
170   else
171   {
172     // In case it must not be the first in the list
173     Event* current = eventlist;
174     int i = 2;
175     while (current->getNext() != NULL && current->getNext()->getTime() <
    ↪  event->getTime())
176     {
177       current = current->getNext();
178       i++;
179     }
180     event->setNext(current->getNext());
181     current->setNext(event);
182   }
183 }
184 
185 void insertEvent(Event* eventlist, Event* event)
186 {
187   event->next = eventlist->next;
188   eventlist->next = event;
189 }
190 
191 #endif
```

C

Matlab Code for Model Parameter Estimation

C.1. Main File For Gate Discharge Parameter Estimation and Plotting

```
%Import Data
CSV                 = readtable('gate_discharge/gate_dischargeCH1.csv');
t                   = table2array(CSV(1:2500,4));
PWM                 = table2array(CSV(1:2500,5));
CSV                 = readtable('gate_discharge/gate_dischargeCH2.csv');
V_gs                = table2array(CSV(1:2500,5));

%prepare numerical method
index_of_t0         = find(t == 0);
index_of_t_end      = find(V_gs == 6);
index_of_t_end      = index_of_t_end(1);
t_cut               = t(index_of_t0:index_of_t_end);
V_gs_cut            = V_gs(index_of_t0:index_of_t_end);
x0                 = [300e-12;350e-9];

%model parameters
V_gs_0              = 11;
R                   = 10E6;
I_L                 = 550e-9;

%fit data
[xopt, stat] = Levenberg_Marquardt(@fit_fun, x0, t_cut, V_gs_cut, V_gs_0);
C_gs                = 1/(R*xopt(1))
I_L                 = xopt(2)/R

%model with the found parameters
V_gs_model =  @(C,t) (V_gs_0 +R*I_L)*exp(-t_cut/(R*C))-R*I_L;
V_gs_modelled = V_gs_model(C_gs, t);

%set voltage conditions and calculating PWM limit
V_gp = 6;
V_first_pulse = 8;
limit_max_ms = -C_gs*R*log((V_gp+R*I_L)/(V_first_pulse+R*I_L))*1000

```

```
%plot signals + model
hold on
color1 = [51,160,44]/255;
plot(t*1000,V_gs, "LineWidth", 1, "Color", color2);
plot(t_cut*1000,V_gs_modelled, "k", "LineWidth", 3);
xlim([-0.15,1.4]);
ylim([2, 12]);
legend(["Measured $$V_{gs}$$", "Fitted $$V_{gs}$$"], "FontSize", 18,
 ↪  "Interpreter", "latex", "Location", "southeast");
title("Gate Discharge Behavior", "Interpreter", "latex", "FontSize", 24);
ylabel("Voltage$$\,[\mathrm{V}]$$", "Interpreter", "latex", "FontSize",
 ↪  18);
xlabel("Time$$\,[\mathrm{ms}]$$", "Interpreter", "latex", "FontSize", 18);
grid on
set(gca,'xtick',[-0.4:0.2:2]);

%function to fit - model
function [r, J]=fit_fun(x,t,y,V0)
    r = y - (V0 + x(2))*exp(-t*x(1)) + x(2);
    J = [t.*(V0+x(2)).*exp(-t*x(1)),  -exp(-t*x(1))+1];
end
```

C.2. Levenberg–Marquardt Method

```
function [x,stat] = Levenberg_Marquardt(fun_rJ,x0,varargin)
    % Stopping criteria setting
    maxit = 100*length(x0);
    tol = 1.0e-10;
    % preparing the outputs
    stat.converged = false; % converged
    stat.iter = 0; % number of iterations
    % Initial iteration
    x = x0;
    it = 0;
    % Calculate the Jacobian Jx, the residual rx,
    % the function value f and the gradient df.
    [rx, Jx] = feval(fun_rJ, x, varargin{:});
    f = norm(rx,2)^2/2;
    df = Jx'*rx;
    converged = (norm(df,'inf') <= tol);
    % Initial lambda
    lambda = norm(Jx'*Jx,2);
    % Store data for plotting
    stat.X = x;
    stat.F = f;
    stat.dF = df;
    % Main loop of L-M method
    while ~converged && (it < maxit)
        it = it+1;
        % Calculate the search direction by solving a linear LSQ problem
        A = [Jx; sqrt(lambda)*eye(length(x))];
        b = [-rx; zeros(length(x),1)];
        p = linearLSQ(A,b);
        % Update the iterate
        x_new = x + p;
        % Save the new residual as rx_new,
```

```
        % the new Jacobian as J_new
        [rx_new, Jx_new] = feval(fun_rJ, x_new, varargin{:});
        % the new function value as f_new
        f_new = norm(rx_new,2)^2/2;
        % Update the Lagrange parameter lambda
        rho = (f-f_new)/(0.5*(p'*(lambda*p-Jx'*rx)));
        if rho > 0.75
            lambda = lambda / 3;
        elseif rho < 0.25
            lambda = 2*lambda;
        end
        % Accept or reject x_new
        if rho > 0
            x = x_new;
            rx = rx_new;
            Jx = Jx_new;
            f = f_new;
            df = Jx'*rx;
        end

        % check if it is converged
        converged = (norm(df,'inf') <= tol);
        % Store data for plotting
        stat.X = [stat.X x];
        stat.F = [stat.F f];
        stat.dF = [stat.dF df];
    end
    % Prepare return data
    if ~converged
        x = [];
    end
    stat.converged = converged;
    stat.iter = it;
end
```

C.3. Linear Least Squares by QR-Factorization

```
function x = linearLSQ(A, y)
    % Solve Linear Least Squares by QR factorization
    % (more numerically stable)
    [Q, R] = qr(A,0);
    x = R\(Q'*y);
end
```

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