Enhancing device passivation in poly-Si IBC cells and investigating PECVD tunnel oxides in poly-SiOx FBC cells

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Enhancing device passivation in poly-Si IBC cells and investigating PECVD tunnel oxides in poly-SiOx FBC cells

by

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to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday September 2, 2019 at 14:00.

Student number:	470 6986	
Project duration:	November, 2018 – September, 2019	
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An electronic version of this thesis is available at http://repository.tudelft.nl/.

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List of publications

Ultra-Thin SiOx Prepared by PECVD N2O Plasma as Tunnelling Layer for Poly-SiOx Carrier-Selective Passivating Contacts - *G. Yang, L. Franco, M. Singh, P. Procel, L. Mazzarella, A. W. Weeber, O. Isabella, M. Zeman,*

Acknowledgements

First I would like to thank my amazing partner J. Kelly for supporting me throughout this masters course. You provided an infinite source of motivation for me, allowing me to work hard and achieve my goals.

Next I would like to thank my family back home in the United Kingdom. Again you provided a huge amount of support for me that enabled me to pursue my passion in this masters.

I also want to show my appreciation for my excellent supervisors at the TU Delft PVMD group. To my daily supervisor, Dr. G Yang, I thank you for being the great fountain of knowledge of PV technologies. You helped me throughout my thesis research and were always willing to make time to help me with experimentation. I would not have been able to complete this research without your support and forever thank you for this. To Dr. O Isabella, I also give a huge thank you. First for taking me on as a master student and second for making me feel like such a valued member of the PVMD group. With your help and advice I have learnt a great deal here. I would like to extend this thanks to the rest of the research group. It was a pleasure being a part of such a welcoming collection of intellectuals. I am thankful for the support each of you were able to give to me and will fondly remember the time that I spent here.

To my housemates and my fellow SET coursemates I also give thanks. On arrival to the Netherlands I thought I would spend two years learning about sustainable energy but the reality is I have learnt so much more. It was amazing to work alongside so many brilliant minds from all across the globe. The atmosphere of collaboration on our course was particularly special and I hope that this ethos will only continue in the coming years.

Finally, I would like to give thanks to all my fellow cleanroom users. Many of you helped train me on the different pieces of equipment which I am very grateful for. More importantly you provided a source of great joy and comradery when things did not go so well and for this you will always be appreciated.

I will always remember the great times I had at TU Delft and thank each of you for playing your part in that. I wish you all the very best in your futures.

Abstract

The poly-Si IBC topology is one of the most promising silicon solar cell designs and has already achieved >26% efficiency. In this work we optimise the front surface field (FSF) and apply rear hydrogenation to the poly-Si IBC structure developed by the TU Delft PVMD group. An investigation is also made of a PECVD tunnel oxide as a replacement for NAOS oxide currently used. The PECVD method allows greater control of the layer thickness and stoichiometry, as well as the ability to grow and cap the oxide layer without breaking vacuum. This process also leads to the development of poly-SiO$_x$ passivating contacts, which exhibit lower parasitic absorption as compared with their poly-Si counterpart. The optimised PECVD oxide is implemented into FBC solar cells.

In the optimisation of the FSF the best performance came from the a-Si:H/SiN$_x$:H stack using thicknesses of 18 and 75 nm respectively. It achieved an iV_{oc} of 731 mV and a J_0 of 4 fAcm^{-2} on undoped textured samples. This was owing to the high hydrogen content of the materials, but had the disadvantage of parasitic absorption from the a-Si:H layer. The stack was tested against different FSF doping levels and with varying thickness to reduce the parasitic absorption. The best performance remained on the undoped (No FSF) case with 18 nm a-Si, achieving 731 mV and 13.5 fAcm^{-2}. The selected a-Si thickness for implementation into IBCs was 9 nm. This was estimated to provide lower parasitic absorption whilst still achieving high passivation. A peak value of 722 mV was obtained for No FSF case.

A study of rear hydrogenation options revealed the a-Si:H/SiN$_x$:H layer provided the best results. The layer thicknesses were 6 and 75 nm respectively. This led to an overall passivation of 725 and 709 mV on poly-Si IBC BSF and emitter symmetrical samples. This was due to the high hydrogen content in the layers raising the passivation quality of the poly-Si passivating contacts on the c-Si interface.

The implementation into IBCs was unsuccessful owing to shunting of emitter and BSF regions. The SiN$_x$ layer was too thin to withstand the post-metalisation annealing and both poly-Si regions were contacted. Peak values of 7.22% efficiency and 600 mV Voc were obtained.

In the investigation of the PECVD tunnel oxide measurements different layer thicknesses were made. After a 3 minute reaction time of c-Si in N$_2$O plasma a thickness of 1.22 nm was achieved. Growth saturated after 21 minutes at a thickness of 1.98 nm. Implementation in flat n-poly-SiO$_x$ passivating contacts showed that the oxide with 1.97 nm thickness, oxide 18, obtained the best result of 723 mV. On flat p-poly-SiO$_x$ passivating contacts the 1.85 nm oxide, oxide 12, achieved the best result of 668 mV. On textured n-poly-SiO$_x$ passivating contacts oxide 18 again performed best, with 710 mV. As the p-poly-SiO$_x$ was limiting, oxide 12 was selected for implementation into FBC cells.

The implementation into FBC cells revealed that the oxide layer had a very high $R_{contact}$ value that limited performance. The best V_{oc} of 517 mV came with an FF of 89%. A TLM measurement showed that for oxide 12 $R_{contact}$ was 3.71 kΩ. This was therefore restricting the flow of current within the cell.

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Nomenclature

Symbols

η Conversion efficiency

FF Fill factor

$iVoc$ Implied open circuit voltage

J_0 Recombination current

J_{sc} Short circuit current density

pFF Pseudo-fill factor

$R_{contact}$ Contact resistance

R_{series} Series resistance

R_{sheet} Sheet resistance

R_{shunt} Shunt resistance

V_{oc} Open circuit voltage

a-Si:H Hydrogenated amorphous silicon

Ag Silver

Al Aluminium

ALD Atomic layer deposition

AlO_x:H Hydrogenated aluminium oxide

ARC Antireflective coating

B Boron

BHF Buffered hydrofluoric acid

BSF Back surface field

c-Si Monocrystalline silicon

EQE External quantum efficiency

FBC Front back contacted

FGA Forming gas annealing

FS Front surface

FSF Front surface field

FZ Floatzone

H_2 Hydrogen

HF Hydrofluoric acid

HNO_3 Nitric acid

IBC Interdigitated back contacted

LPCVD Low pressure chemical vapor deposition

N_2O Nitrous oxide

NAOS Nitric acid oxidation of silicon

O_2 Oxygen

P Phosphorous

PECVD Plasma enhanced chemical vapor deposition

poly-Si Polycrystalline silicon

poly-SiO_x Polysilicon oxide

SiH_4 Silane

SiN_x Silicon nitride

SiN_x:H Hydrogenated silicon nitride

SiO_2 Silicon dioxide

SRH Shockley-Read-Hall

STC Standard test conditions

TCO Transparent conductive oxide

TLM Transmission line method

1
Introduction

The field of photovoltaics was born at Bell Labs, Los Alamos in 1954 when Gerald Pearson and his team designed the first silicon solar cell. Back then their application was intended for orbiting satellites, but it is almost certain they envisioned a future one day fuelled by these devices on Earth. 65 years later this vision has become a reality. The total installed PV capacity in 2017 was 398 [GW] and this looks only set to increase in the coming years [1]. Indeed, when one looks at the major issues affecting today's world, the necessity of this technology is clear.

Humanity is faced with an increasing population [2], finite fossil fuel resources [3], and the threat of climate change based on the emissions related to these fuels. Couple this with the fact that approximately 1 billion people still do not yet have access to electricity [4], and it is clear that energy is a major concern for the future. New technologies must be developed to meet this demand. Solar energy represents one of these new technologies, and as such has been highlighted as a key actor in the energy transition.

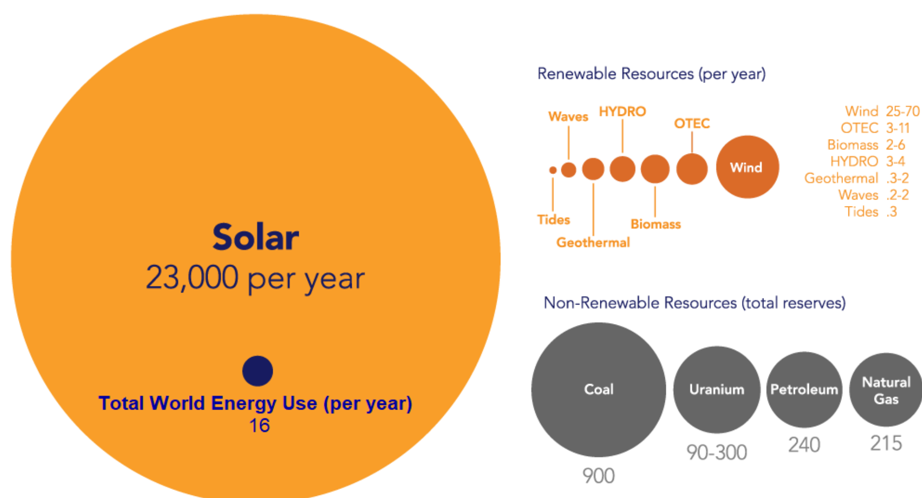

Figure 1.1: Power available for each energy source in Terrawatts [5]

Analysing the source of solar energy, it is obvious why it has garnered so much interest in recent years. The Sun is the powerhouse of the solar system and is its most abundant energy source. The energy it radiates exceeds global demand by a factor of 10,000, figure.1.1, and

on human timescales it is effectively infinite. Harvesting this energy gives the means to meet the needs of the growing population and move away from fossil fuels. This eradicates the problem of scarcity and reduces the man-made contribution to climate change. It is for this reason that research in this field is of such high importance. To support this energy transition, research must provide better products at a lower cost so there is no competition from fossil fuels.

Taking a look at the current state of this field reveals some interesting insights. From figure.1.2 it is clear that the dominant technology is silicon based, specifically polycrystalline silicon (poly-Si). This comes as another plus, as silicon is one of the most abundant elements. What can also be seen is that a growing share of new installations are based on monocrystalline silicon (c-Si). This technology yields higher conversion efficiencies than its poly-Si counterpart but is more expensive to fabricate.

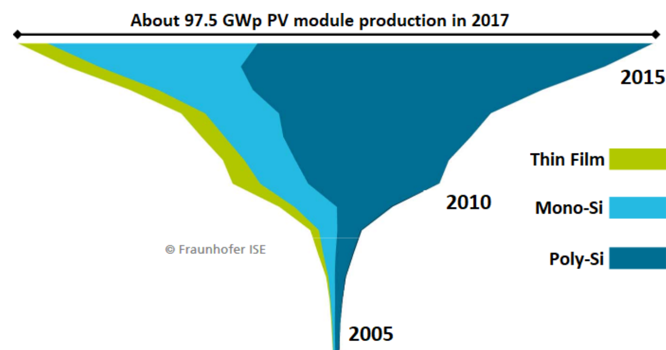

Figure 1.2: Market trends for solar materials. Poly-Si dominates but mono-Si is increasing [6]

1.1. Solar cell working principle

A solar cell converts incident light into usable electrical energy via the photovoltaic (PV) effect, figure.1.3. Photons enter the semiconductor bulk where they are absorbed. This absorption gives energy to electrons, exciting them into the conduction band. If an external circuit is present, they can be used to power a load.

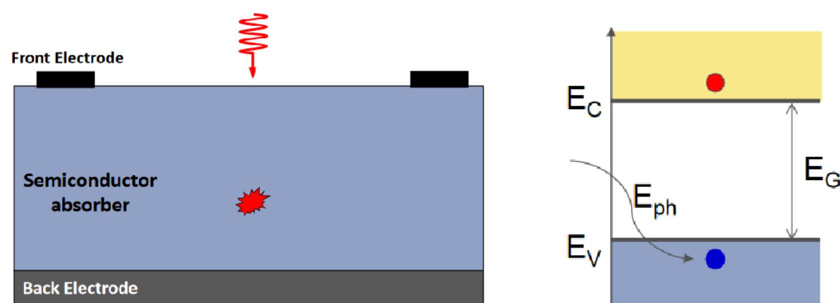

Figure 1.3: Left: Simplified representation of the photovoltaic effect.Arrow represents incident photon. Collision represents a photon-electron interaction [7]. Right: Band diagram showing electron (red) and hole (blue) generation from an incident photon. The electron is excited from the valence into the conduction band [8]

.

The entire process can be explained in 4 steps:

- Generation
- Separation
- Collection
- Recombination

Generation occurs when an absorbed photon excites an electron into the conduction band, figure.1.3. In its wake a quasi-particle known as a hole is left which moves through the valence band. Thus we have the generation of an electron-hole pair. This generation only occurs for the absorption of photons above a particular energy threshold. This is the difference between the valence and conduction band, the band gap energy, E_g. For c-Si E_g is equal to 1.12 [eV].

Separation of generated charge carriers comes next. This is done to stop the electron and hole from recombining. Upon recombination the electron falls back to the valence band, shedding the photon energy to the lattice. In a crystalline silicon (c-Si) cell, this is mitigated using Boron and Phosphorous doped silicon layers to construct an electric field which separates the carriers. B-doped silicon creates a p-type semiconductor to attract holes and P-doped silicon creates an n-type layer to attract electrons, figure.1.4.

Collection occurs at the electrodes. In order for the electron energy to be utilised it must travel through the external circuit. For a p-type device, meaning the absorber layer is boron doped, electrons are collected at the front electrode. For n-type they are collected at the back.

Recombination is the final step. Once the electron has successfully passed through the external load, it returns to the bulk where it recombines with a hole. Again the electron is in the valence band.

1.2. Cell structure

In this section the solar cell structure is discussed in more detail.

Looking at figure.1.4 the cross-section of a front back contacted (FBC) solar can be seen. Starting at the top of the device, the front electrodes provide the means of collection for excited electrons. Next, an anti-reflective coating (ARC) layer is employed. This increases the amount of light transmitted into the cell. By applying a layer with a refractive index between the semiconductor and the medium above, a so called Rayleigh film [9], reflection from the front surface is reduced. A process called surface texturing can also be applied here. The c-Si surface is etched to add roughness. Incident light is then scattered at different angles improving the likelihood of absorption.

The cell in figure.1.4 is p-type so below the ARC is an n-type emitter layer. For an n-type absorber, the emitter would be p-type. This forms the first pn-junction of the device, aiding the separation of charges before collection.

To create this junction B and P dopant atoms are used. By doping c-Si with B, an element with one less electron in its outer shell, you reduce the total number of free electrons. Each B atom accepts one of these electrons becoming a negative ion. This leads to a semiconductor layer with holes as the majority carriers as there are less free electrons. The positive hole charge creates the p-type layer. Conversely, P is an element with one extra electron so adding this to the lattice donates electrons. The P atoms become positive ions and the electrons are now

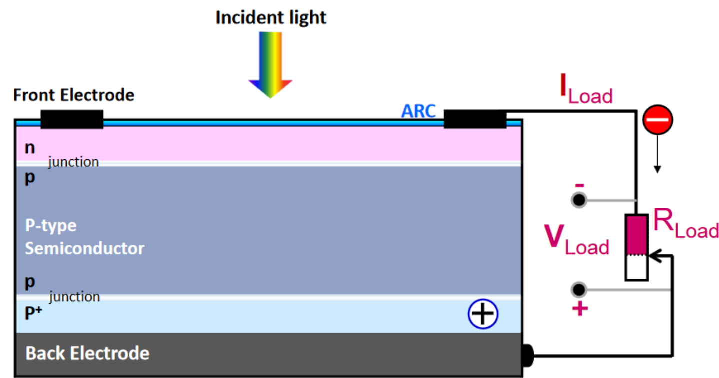

Figure 1.4: P-type solar cell with n-type emitter layer and p^+ back surface field (BSF). [7]

the majority carriers. Their negative charge creates the n-type layer. In each case, however, the overall charge remains neutral as the extra free carriers are compensated by the new ions.

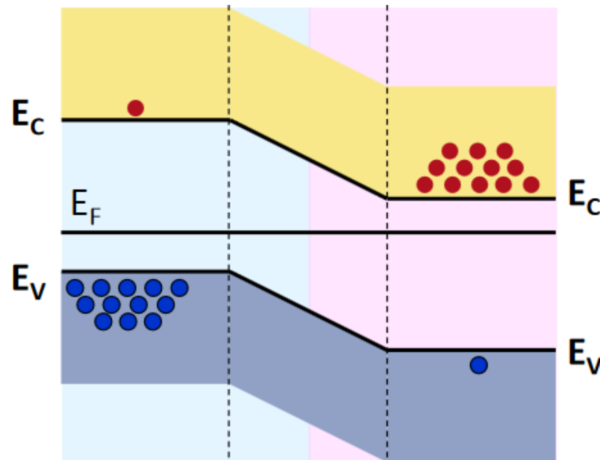

Figure 1.5: Band bending due to presence of electric field across the pn-junction. Left to right shows p-type, depletion and n-type regions. Electrons (red) are pulled to towards the n-type layer, whilst holes (blue) drift to the p-type [9].

Sandwiching B- and P-doped layers side by side creates a pn-junction. At this junction there is a high concentration of holes and electrons in the respective p- and n-type regions. These concentrations give rise to a diffusion current across the boundary, with each set of carriers moving to the layer of lower concentration. Over time this diffusion plateaus and in its wake an area across the junction with no free carriers remains. This is known as the depletion region. In the depletion region there are only the fixed dopant ions are left and their charge gives rise to an electric field. This causes a drift current which now drives carrier transport. Holes are thus attracted to the negative B ions in the p-type layer and electrons to the positive P ions in the n-type layer. This is effect is visualised in figure.1.5. The bending in the energy bands represents the direction of the electric field across the depletion region. The electrons are pulled down the conduction band slope, towards lower energy levels. The holes travel upwards along the valence band.

Returning to figure.1.4, below the pn-junction is the bulk absorber layer. Here the energy from incident photons is utilised to excite electrons before separation and collection. This layer can be p-type, n-type or undoped (intrinsic). Towards the back of the device the p^+ back surface

field (BSF) is shown. This highly doped region region leads to second junction with the same properties as the pn-junction above. The band bending caused by the change in dopant concentration facilitates the separation of carriers from the absorber layer. Holes are attracted whilst electrons are repelled, improving the collection at the back electrode.

Finally, the back electrode is shown. Here electrons return to the device, recombining with holes and returning to the c-Si bulk.

1.3. Loss mechanisms

In this section the losses in a solar cell are described. These can be split into two categories: optical and electrical. The optical losses concern the successful absorption of photons, whilst the electrical losses concern the successful collection of electrons.

1.3.1. Optical

Beginning with the optical losses, the most considerable of these is the spectral mismatch. This was already alluded to in section.1.1, and is related to the energy gap of the material, E_g. Photons below this energy cannot be used for the promotion of electrons and so are not usefully utilised by the cell. They may be absorbed outside the bulk in non-photoactive layers, but this does not add to the energy output of the device. Similarly, photons with energy above E_g can only be partially utilised. The rest of this energy is lost to the lattice in a process known as thermalisation.

Additionally, photons with an energy equivalent to E_g will take the longest time to be absorbed. As such they may travel through the bulk and be absorbed in non-photoactive areas. These photons are said to be 'parasitically absorbed'. Parasitic absorption will also happen at the front of the device, where very high energy photons are absorbed very quickly. Because of this ARCs and emitter layers must be designed carefully to mitigate this effect.

The next major loss mechanism is reflection. Reflected photons either do not reach the absorber layer, or are reflected away from this layer before they have been absorbed. As such, the use of ARCs and surface texturing is implemented to improve light in-coupling in the cell. As mentioned in section.1.2, texturing can also be used to reduce front surface reflection. The scattering induced by texturing also increases the path length of photons through the cell, increasing the probability of absorption.

Finally, there are losses due to shading. These represent the loss in photoactive presented by non-photoactive elements on the front surface. For example, the front metal contacts take away area for incident light absorption and therefore provide a shading effect. What's more, these elements are 3D so will form a shadow across the device. The geometry of the front metal contacts is thus of great importance. They must be optimised to minimise this shading effect.

1.3.2. Electrical

Electrical losses are defined as the unsuccessful utilisation of excited electrons. Recombination is one of the major loss mechanisms. This is not the same as the recombination mentioned earlier, after travelling through the external circuit, but rather recombination before being collected. This recombination comes in three forms; radiative, Auger and Shockley-Read-Hall (SRH), figure.1.6.

Radiative recombination happens when an excited electron relaxes back to its original energy state. The energy released is then lost to the lattice in thermalisation. Auger recombination is a three-particle process. An electron sheds its energy to another electron in the conduction band, or a hole in the valence band, and falls back to the valence band to recombine. SRH recombination comes from the presence of defects in the semiconductor that lead to extra holes or 'trap states'. A special case of SRH is surface recombination. This happens at the semiconductor edges where not all silicon atoms are fully bonded. The presence of these so called 'dangling bonds' provides further trap states.

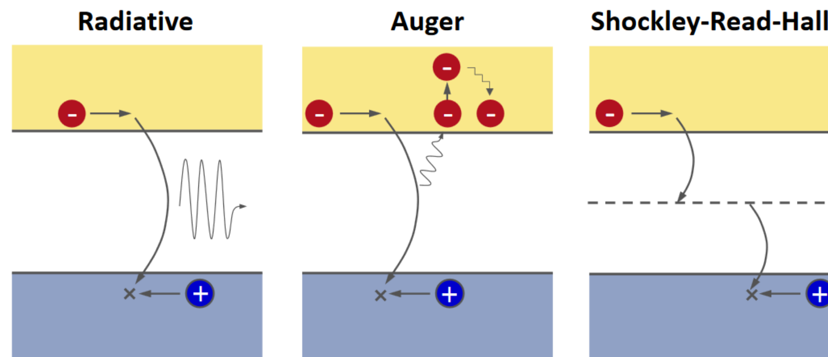

Figure 1.6: Diagram showing recombination mechanisms. Radiative recombination releases energy to the lattice. Auger recombination gives energy to a third particle. SRH recombination is due to trap states that provide extra holes. [8]

Radiative recombination is not a major issue for c-Si as it has an indirect band gap. This means electrons need momentum as well as energy to be excited. It is therefore not so easy for an excited electron to relax back to its original state. Auger recombination only occurs when there is a large amount of free carriers. It is most common in the depletion region, in highly doped regions and at times of high light absorption. For c-Si solar cells, the most important recombination mechanism is therefore SRH.

SRH is largely dependent on material quality and surface passivation. Lower quality means more defects, or in the case of poly-Si, different lattice orientations which form 'grain boundaries'. Generally speaking, the material quality for c-Si is now very high so bulk defects can be neglected. Surface recombination is then of more importance here. In fact it is surface recombination at the metal/semiconductor interface that is now the limiting factor in c-Si solar cells.

$$R = \nu_{th}\sigma_n N_{sT} \tag{1.1}$$

The rate of surface recombination in an p-type semiconductor is described by equation.1.1. Where ν_{th} is the surface recombination velocity, N_{sT} is the surface trap density and σ_n is the capture cross-section for electrons. It is thus evident that by reducing the number of trap states (dangling bonds) this loss can be reduced. Passivation materials are often used for this purpose [10]. These decrease the density of defect states by bonding at these points. This is discussed in more detail in section.1.5

Apart from recombination, there are also resistive losses. There is a series resistance, R_{series} associated with each layer of the solar cell which acts to reduce the total output current. The relation for the series resistance is given by equation.1.2.

$$R_{series} = \frac{\rho l}{A} \tag{1.2}$$

Where ρ is the resistivity of the material, l is the length and A is the area. This is of particular importance in the design of the front metal contacts. As can be seen from equation.1.2, a greater metal area will lead to a lower resistance, but this will cause more optical shading. Therefore in FBC cells the contact geometry must be carefully managed so that an optimum between these two loss mechanisms is found.

The other resistive loss is the shunt resistance, R_{shunt}. This refers to the amount of leakage current across the pn or $p^{+}p$ junctions. Ideally R_{shunt} would be infinitely high so that this current is zero and this loss mechanism is minimised.

Finally, there are the band gap utilisation losses. These arise from the fact that the maximum possible voltage, V_{oc}, achieved by the cell will always be less than E_g. For c-Si the max V_{oc} is 720 [mV] [11].

The combination of these mechanisms leads to a theoretical maximum conversion efficiency known as the Shockley-Queisser limit. For c-Si this gives a value of just under 30 [%] [9]. This, however, does not consider Auger recombination.

1.4. Cell parameters

There are a number of parameters used to characterise the performance and properties of solar cells. In this section these parameters are well defined, as they will be referred to throughout this thesis.

Open circuit voltage

The open circuit voltage, V_{oc}, is the potential when no current flows the solar cell. It is the maximum voltage that can be supplied by the device. The V_{oc} is also a measure of the recombination within the device, and so is often used as an indicator of device quality.

Short circuit current density

The short circuit current, I_{sc}, is the current that flows in the device when no voltage is applied. It is related to the light incident on the cell; the photon flux and photon energy. A greater photon flux or energy will lead to a greater I_{sc} value. The short circuit current density, J_{sc}, is the short circuit current given per unit area of the solar cell. This gives the maximum deliverable current and indicates the level of absorption in the device.

Fill factor

The fill factor, FF, is a comparison of the maximum output achieved by a solar cell against the open and short circuit conditions, equation.1.3.

$$FF = \frac{P_{mpp}}{V_{oc}J_{sc}} \tag{1.3}$$

Where P_{mpp} is the maximum power output. This is a key indicator in cell performance, as it shows how close the device is to its operating limits.

Recombination current

The recombination current, J_0, is an indication of the recombination within the cell and encompasses each specific type of recombination, equation.1.4 .

$$J_{0,tot} = J_{0,s-front} + J_{0,d} + J_{0,Aug} + J_{0,SRH} + J_{0,s-rear} \quad (1.4)$$

Where $J_{0,tot}$ is the total recombination current for the device, $J_{0,s-front}$ and $J_{0,s-rear}$ is the recombination at the front and rear surfaces, and $J_{0,d}$, $J_{0,Aug}$ and $J_{0,SRH}$ are the radiative, Auger and SRH recombination respectively.

Conversion efficiency
The conversion efficiency is the ratio of achieved power output, against the power available under standard test conditions (STC), equation.1.5

$$\eta = \frac{P_{mpp}}{P_{STC}} \quad (1.5)$$

Where P_{STC} is the power available from the Sun, 1000 [Wm^{-2}].

External quantum efficiency
The external quantum efficiency is the ratio of collected electrons to incident photons and is defined by equation.1.6.

$$EQE = \frac{I_{ph}}{q\Psi_{ph}} \quad (1.6)$$

Where I_{ph} is the photogenerated current, q is the charge of an electron and Psi_{ph} is the photon flux incident on the solar cell. This is also a measure of the absorption in the cell but here wavelength specific information is given. Using this quantity one can understand what part wavelengths are not being successfully utilised. For example a device may be very good at absorbing high energy blue photons, but poor at absorbing low energy red photons. This helps inform the design of better performing solar cells.

1.5. Surface passivation

In this section a description of the surface passivation process is given. Four materials are then discussed; SiO$_x$, SiN$_x$:H, AlO$_x$:H and a-Si:H. These are chosen based on demonstrations of their high passivation performance in literature.

As mentioned in section.1.3.2, passivation materials are used to reduce the defect density at the c-Si surface. This helps carrier collection by decreasing the likelihood of recombination. This is known as chemical passivation and is achieved by applying a material that can bond at these points, in place of free carriers, figure.1.7. Passivation materials can also provide field effect passivation. This has a similar effect to doping and is caused by the fixed charge density within the passivation layer. Materials with a negative fixed charge density are better for passivating p-type layers, as they create a field which repels electrons and attracts holes, and vice versa.

SiO$_x$
SiO$_x$ was one of the most commonly used passivation materials for solar cells during the 1980s and 1990s and allowed the first solar cells with efficiencies above 20 [%] to be developed [12]. It has a small positive fixed charge density making it more suitable for n-type layers

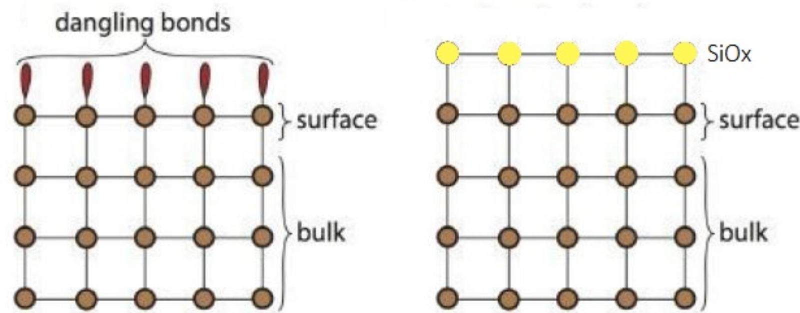

Figure 1.7: Left: Dangling bonds on c-Si surface. Right: Chemical passivation of dangling bonds using SiO_x. Adapted from [9]

than p-type, but can be used as an effective passivation in both cases [13]. This is because its fixed charge density is very low and so the passivation is mainly chemical. What's more, thermally grown SiO_x has a band gap of 9 [eV] and so is optically transparent in the absorption range of c-Si. This is another benefit of the material as it will induce parasitic absorption when on the front surface [14][15].

SiN_x:H

Unlike SiO_x, SiN_x:H does has a high negative fixed charge density so has a much stronger field passivation effect. This means it is not an effective passivation material for p-type layers, however. It also provides better chemical passivation. This is due to its high hydrogen content of around 20 [%] [16][17]. After high temperature annealing this hydrogen diffuses into the bulk passivating defects further enhancing cell performance. SiN_x:H has a tunable band gap based on the SiH_4 content used but is typically around 1.7-1.8 [eV] [18]. This is higher than c-Si so again will not induce parasitic absorption. For this reason, SiN_x:H is commonly used as an ARC.

AlO_x:H

AlO_x:H has a high density of positive fixed charge and so works best on p-type c-Si. This material is also able to chemically passivate materials effectively after annealing thanks to its hydrogen content of around 2-3 [%] [19]. It also has a high band gap, 6 [eV], making it optically transparent in the absorption range of c-Si [19]. It is a comparatively recent material for solar cell passivation but has been able to achieve excellent results despite this [13]. At the time of writing, the world record on c-Si uses this material for FSF passivation [20].

a-Si:H

a-Si:H is an extremely versatile material for passivation because it can be doped to serve p- or n-type layers. In this way it has been used in high efficiency silicon heterojunction cells to achieve great results [21]. When undoped it provides high quality chemical passivation because it again has a high hydrogen content, ranging from 12-18 [%] [22][23]. In contrast to the other layers, parasitic absorption is a big problem in a-Si:H. This is because the random orientations in the lattice lead to a large amount of defect states within the typical c-Si energy gap [9].

1.6. Hydrogenation

Hydrogenation has already been alluded to in section.1.5 and is given a more full explanation in this section.

Hydrogenation is an important technique for improving the quality of c-Si solar cells [24][25]. This is because hydrogen atoms can very successfully attach themselves to unbonded atoms in the bulk and at the c-Si surface [26]. It is thus a form of chemical passivation. Once an H_2 atom has bonded at one of these points it is no longer a trap state for a free charge carrier.

There are two main forms of hydrogenation. The first is the addition of H_2 to the lattice from a material with high H_2 content. The second is adding H_2 via forming gas annealing (FGA). In the first case the H_2 is either released from the material during the deposition, or released in a post annealing step. In the second case, the sample is annealed in an H_2 atmosphere at 400 [^{o}C] [27]. Under these conditions the H_2 atoms can diffuse through the device, towards defects. In both cases the application of hydrogenation is an effective means of raising cell performance.

1.7. High efficiency solar cells

Up to this point the focus has been on the more established FBC cell, however, the world of PV is now moving towards more complex high effieciency cell designs. These high efficiency cells strive ever close to the Schockley-Queisser limit by implementing back contacted metal grids and carrier selective contacts. In this section these structures are introduced and their high performance is analysed.

1.7.1. Interdigitated back contacted cells

The IBC topology shown in figure.1.8 is a radical change from the typical design as it moves all metal contacts to the rear side. This maximises the photoactive area on the top surface, enhancing light absorption, but has some important impacts on the complexity of the cell.

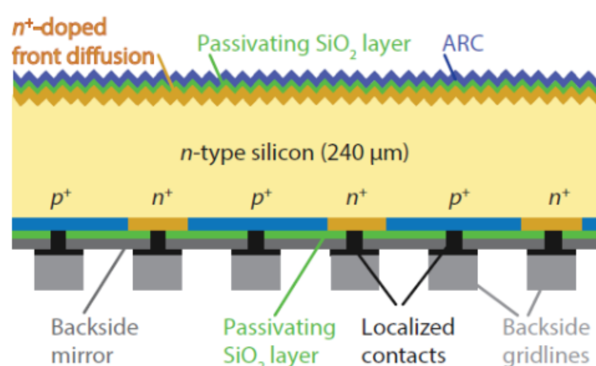

Figure 1.8: Diagram showing topology of IBC cell concept [28]

To successfully collect carriers alternating p^+ and n^+ junctions are placed at the bottom of the device. These create small BSF/emitter pn-junctions which act in the same way as in a typical cell. They provide effective carrier separation but the field effect from the neighbouring regions also has a negative 'electrical shading' effect. This inhibits minority carrier collection when the distance travelled to the emitter is greater than the diffusion length. To compensate for this the minority carrier regions are larger, increasing the likelihood of successful collec-

tion. Generally this configuration uses an n-type bulk making holes the minority carrier, so it is the p+ regions that form the emitter. At the top of the device a front surface field (FSF) is implemented. This highly doped region helps drive minority carriers towards the bottom junctions.

In this design the metal/semiconductor interface is reduced in what is known as a localised contact. This decreases the recombination at the metal interface. Furthermore, it separates the two electrodes so no short circuit can occur. An SiO_2 layer passivates the areas that are not in direct contact with the metal and a back reflector is also added to improve light absorption. This reflects photons that have not been absorbed back into the bulk.

The obvious advantage of this topology is the lack of optical shading on the top of the cell, improving the photogenerated current by 4-5 [%] [29]. Next the metal grid can be optimised for the best R_{series}/FF values as there is no longer shading be considered. As stated above, the local contacting helps reduce recombination, another benefit of this metallisation process.

Other benefits come from the FSF. This implementation can be designed more freely to reduce parasitic absorption compared with an FS emitter. Usually a balance must be struck between low doping to reduce Auger recombination and high to mitigate contact and lateral resistance. Having the emitter at the rear side means the doping can be optimised for high lateral conductivity with little effect on the short wavelength response [29].

The key disadvantage is the increased production complexity. Having alternating p^+ and n^+ regions means extra steps in the manufacture process. High annealing temperatures are also required to activate these dopants [30][31]. The other disadvantage is the already mentioned electrical shading effect. It is mitigated through the reduction of BSF size but this presents a compromise between passivation quality and contact resistance [29].

Overall this design has led to huge improvements in the capabilities of c-Si solar cells. In 2018, Trina Solar achieved a milestone 25.04 [%] conversion efficiency with this structure [32].

1.7.2. Carrier selective contacts

As mentioned above, another important advance in the design of solar cells is the implementation of carrier selective contacts. In this section a description of these contacts is given with some important examples.

Thanks to improvements in the quality of the c-Si bulk, the limiting factor in c-Si solar cells is now the recombination at the metal/semiconductor interface. To combat this a new form of CSC solar cells has been implemented. These use an interlayer of SiO_x or a-Si between the metal/c-Si interface. This interlayer provides chemical passivation of dangling bonds and is used in conjunction with a doped layer to provide high quality field effect passivation [33]. Some important examples of these cells are the tunnel oxide passivating contact (TOPCon), silicon-heterojunction (SHJ) and the poly-Si IBC.

Tunnel oxide passivating contact cells

The TOPCon topology, figure.1.9 left, uses a tunnel oxide passivated contact at the rear side of the cell in place of a back surface field. This is an SiO_2 layer approximately 2 [nm] thick [34] that acts as a carrier selective membrane. It creates a barrier to minority carriers that

want to recombine at the metal surface, whilst being thin enough for majority carriers to tunnel through. Behind this there is a doped a-Si layer which provides the band bending that attracts majority carriers, figure.1.9 right.

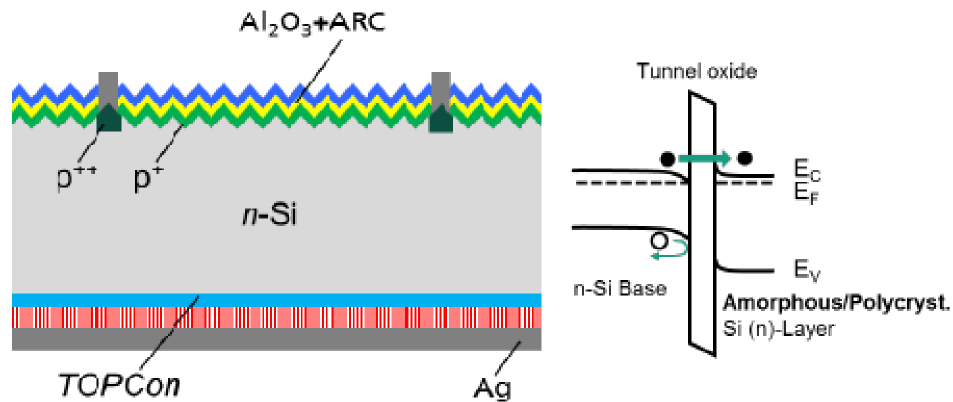

Figure 1.9: Left: n-type TOPCon cell structure showing tunnel oxide layer at the bottom of the device. Right: Diagram of band bending at the oxide layer. Holes are repelled whilst electrons tunnel through [35]

The tunnel oxide acts to reduce recombination at the metal contact, improving overall performance. In this case, holes cannot travel directly from the absorber to the rear contact, therefore electrons can travel freely to the metal.

At the front side of the cell, a typical application of surface texturing, anti-reflective coating (ARC) and a passivation layer is seen above the emitter layer.

An important advantage of this design is the impact on the manufacturing simplicity. The entire rear-side is now metallised in one step, which means the removal of complex patterning techniques for the back contact. Utilising these advances, Fraunhofer ISE achieved 25.7 [%] efficiency with this design in 2017 [36].

Silicon heterojunction cells

The silicon heterojunction cell is one of the highest performing CSC designs and Panasonic achieved 25.6 [%] with it in 2014 [21]. The diagram for this cell is shown in figure.1.10.

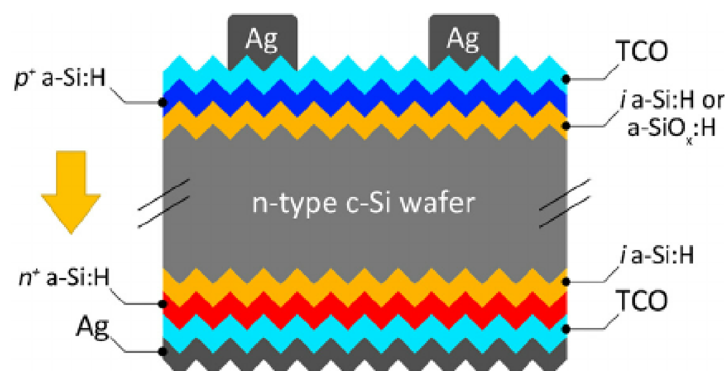

Figure 1.10: Schematic of SHJ cell structure [37]

The front surface is textured to improve light absorption. Above the texturing comes the first

a-Si intrinsic layer. This applies the chemical passivation to the c-Si surface. a-Si has a higher band gap than c-Si this interface forms a so called heterojunction. Above this there is doped p-type a-Si. This layer supplies the field effect passivation that completes the carrier selective contact. Now holes are attracted to the front metal contacts whilst electrons are repelled. Between the a-Si layers and the metal contact there is a transparent conductive oxide (TCO). This helps the lateral conductivity of charges towards the front contacts, as the conductivity of a-Si is poor [9].

At the rear of the cell a similar structure is present, but in this case the field effect passivation comes from n-type a-Si. It can also be seen that texturing is present on this structure meaning this cell can also be used to absorb light on this surface.

Some of the key advantages of this cell are that it has a very low thermal budget as the doping of a-Si is done at low temperature via PECVD. Usually dopant activation is done at 850 [^{o}C] so this massively reduces the fabrication complexity. Conversely, this does mean that the cell is less robust against high temperature conditions such as hot spots. Another advantage is the high V_{oc} potential thanks to the band gap of the a-Si layer [9]. This is higher than any of the other high efficiency c-Si concepts. As already mentioned, the combination of the SHJ - IBC cells designed by *Kaneka* hold the current world record efficiency for c-Si [38]. This cell achieved an efficiency of 26.7 [%] [20].

Poly-Si interdigitated back contacted cells

This thesis is concerned with the poly-Si IBC cell structure. This is a very promising design that has great potential for high efficiency devices. ISFH achieved 26.1 [%] with this structure in 2018 [39].

Looking at figure.1.11 the topology for this design can be seen. Starting at the top of the device there is a SiN$_x$ layer that provides passivation and anti-reflective coating. Below this is another passivation layer which can be SiO$_2$, AlO$_x$ or many other materials. Next there is the FSF typical of the IBC structure, pushing minority carriers towards the back contacts. Below the semiconductor absorber, the p$^+$ and n$^+$ regions are located. Between this layer and the bulk is the SiO$_2$ tunnel oxide layer. A small gap is etched to prevent any shunting between the two doped regions - and this is also passivated. Below this layer there is again SiN$_x$ which here is used as a capping layer. The SiN$_x$ is locally opened so the metal electrodes make direct contact with the doped regions.

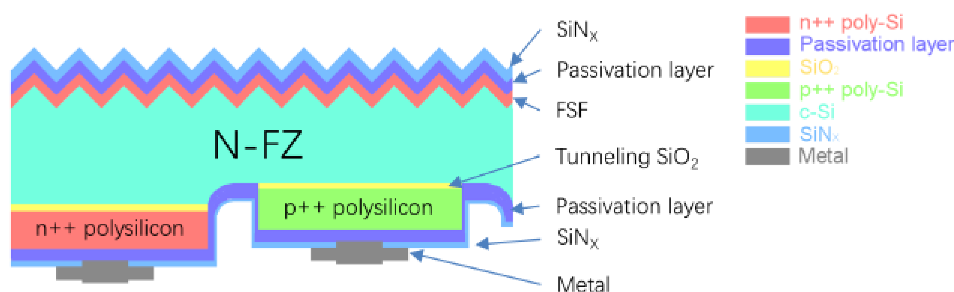

Figure 1.11: Schematic of poly-Si IBC structure developed by TU Delft PVMD group [40].

This structure can achieve very high efficiencies because it utilises the best aspects of the TOPCon and IBC topologies. The tunnel oxide layer together with the doped p$^+$ and n$^+$ doped regions provide excellent chemical and field effect passivation [41][42]. Combining this

with the optical improvements from the removal of the front metal contacts and rear-metal design flexibility leads to very impressive results. Additionally, the use of poly-Si as opposed to a-Si as seen in other high efficiency structures allows for higher flexibility in the design process. Poly-Si has a higher thermal budget, where a-Si cannot withstand temperatures above 250 [^{o}C] [31]. This means it can survive more intensive processes, such as ion-implantation, perfect for creating the doped regions [43].

The main drawback of the structure is again the complexity required for processing. The IBC topology already requires many steps, so adding a tunnel oxide only further complicates this. Furthermore, although the high temperature mean greater thermal stability, they are not ideal for industry [44] [31] [45]. The other disadvantage is parasitic absorption in the doped layers at the front and rear of the device. This is mainly due to free carrier absorption in these layers and can be reduced by in situ doping or decreasing the layer thickness [44].

Poly-Si passivating contacts
In this section the poly-Si passivating contact is analysed in more detail.

The poly-Si passivating contact is the combination of the tunnel oxide layer and the doped poly-Si regions. Together these form the very effective passivation of the c-Si surface. The key parameters in these effects are the thickness of the oxide layer, and doping of the poly-Si layer. If the tunnel oxide is too thick, carriers will not be able to tunnel to the doped regions. However, if the field effect is too weak, they will not be selective to the right carriers. In fact, the so called doping profile is of particular importance, figure.1.12

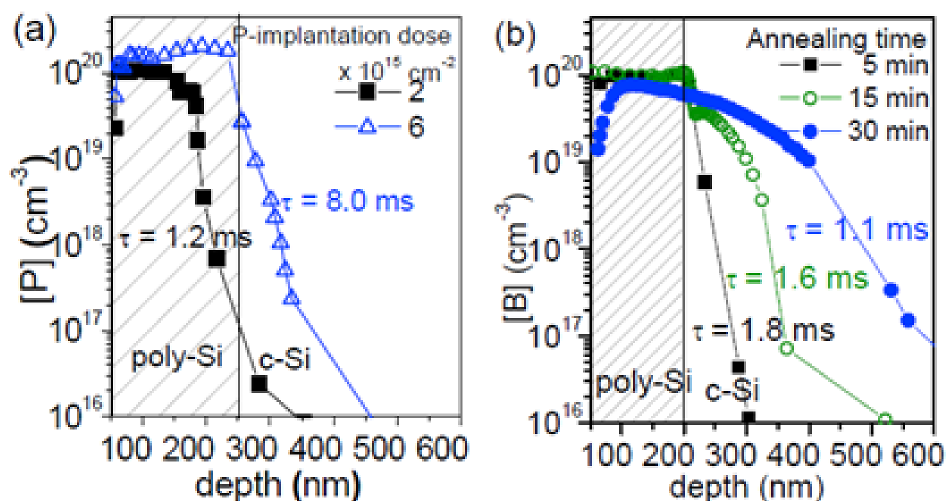

Figure 1.12: (a) P-doping profile of poly-Si passivating contacts with varied implantation dose and fixed annealing time (b) B-doping profile with fixed dose and varied annealing time [44].

Ideally, this will show an abrupt change from high to low doping upon extension into the absorber layer. Obtaining this provides the high field effect across the tunnel junction that is needed for carrier selectivity[44]. However, this profile must be more than just an abrupt change, it has also been shown that some trail off into the bulk is also necessary. To control this three parameters are paramount; the doping level, annealing time and annealing temperature. The doping level obviously affects the number of dopants entering the poly-Si layer. The annealing time affects the depth to which these dopants diffuse. Higher annealing time

and temperature drives these dopants further.

1.7.3. Poly-Si IBC design considerations

In this section a literature review of the important design considerations for the poly-Si IBC cell design is given. The thickness of the tunnel oxide layer; the thickness, doping and annealing of the p^+ and n^+ regions; the passivation of the rear topology; the FSF thickness, doping and annealing and finally the passivation of the front surface are all discussed below.

For the tunnel oxide the general belief is that 1.5 [nm] is the normalised thickness [46][40][44]. Some opt for slightly smaller at 1.2-1.4 [nm] [35][30], whilst others go slightly larger at 2.2-2.4 [nm] [39][43]. At this distance the majority carriers can successfully tunnel through, but the barrier is still thick enough to halt the minority carriers.

Deposition methods for the ultra-thin tunnel oxide also vary. Some groups favour thermal oxidation [39][43], others wet chemical immersion, [44][40] and some UV/O_3 ozone oxidation [35][45]. The major difference comes from uniformity, stoichiometry and density of the layers formed. In this respect UV/O_3 performs best [35], but wet chemical immersion is perhaps the preferred option for industry as only a 69.5 [%] HNO_3 bath is required [44].

The thickness of the poly-Si layers is much more varied across different groups. Typically it is in the range of 100-250 [nm] [44][40][43][39] but in some cases can be less than 50 [nm] [45][46]. In almost all cases it is formed through a low pressure chemical vapor deposition (LPVCD) of a-Si, which is crystallised to poly-Si in a later annealing step [44]. Annealing is done at temperatures of 800-950 [^oC] which also activates and drives in dopants. There are, however, some groups using in situ doped a-Si deposited via PECVD. In the standard process doping is done after LPCVD deposition via ion-implantation. This is done at a wide range of levels dependent on the poly-Si layer thickness, annealing time and temperature [44], and whether the layer is being counterdoped [43]. Typical levels are on the order of 10^{15}-10^{16} [dopants/cm^3]. The same is true when applying doping to the front surface field.

At the rear of the cell a number of hydrogenation stacks can be selected. The most popular choice is the a-Si:H/SiN_x:H stack. The thicknesses for these layers vary. In the TU Delft PVMD group the a-Si:H is 3 [nm] and the SiN_x:H layer 75 [nm] [44].

At the front surface lots of groups opt for and AlO_x/SiN_x stack for passivation [45][43][35][46]. It should be noted that for each of these cases n-type wafers are used. The record IBC cell [39] mentioned above used p-type wafers and in this case AlO_x/SiN_x/SiO_2 was used for front surface passivation. Here the SiN_x/SiO_2 layer acts as a double antireflective coating, increasing light absorption into the cell.

1.8. Research goals

The motivation of this thesis is to support the uptake of solar energy by striving towards higher efficiency solar cells. To do this, steps are taken to enhance the passivation of poly-Si IBC cells. The research has 3 main aims:

1. Improving the passivation quality of the front surface field

2. Applying an optimised hydrogenation process to the rear of the cell

3. Investigating the performance of a PECVD tunnel oxide layer as a replacement for NAOS

The outcomes of aim 1 and 2 will be implemented directly into poly-Si IBC cells and the performance measured. The results of aim 3 will be tested in poly-SiO$_x$ FBC cells as a simplified demonstration of the layer quality.

1.9. Outline

This thesis consists of 7 chapters. In chapter 2 the fabrication and measurement techniques used in this thesis are described. Chapter 3 presents the results of the front surface field and rear hydrogenation tests. In chapter 4, these results are implemented in poly-Si IBC cells and the performance is measured. The investigation of the PECVD tunnel oxide is made in chapter 5 and in chapter 6 this layer is implemented in FBC cells. Finally, the reported is concluded in chapter 7 with a summary of the findings and recommendations for future work.

2

Experimental method

In this chapter the methods used for experimentation are given. First, the fabrication steps to design the test samples and solar cells are presented. Then, an outline of the tools used for characterisation of these devices is given. The chapter proceeds in order of usage of each process or characterisation tool.

2.1. Fabrication

For every fabricated device/sample n-type float-zone (FZ) c-Si wafers manufactured by *Topsil* were used. The specification for these wafers is given in table.2.1.

Table 2.1: c-Si wafer parameters

Paramater	Value
Doping	n-type
Orientation	$<100>$
Finish	Polished
Resistivity [Ω-cm]	1-5
Thickness [μm]	280 $\pm$ 2
Diameter [mm]	100 $\pm$ 2

The decision to use n-type wafers as the semiconductor bulk is due to the detrimental light induced degradation effect seen by p-type wafers [47]. As well as this, n-type wafers tend to show superior minority carrier lifetimes, due to a reduced sensitivity to recombination introduced by transition metals [26].

Standard cleaning

At the start of any process, wafers must first be cleaned. This is a 4 step procedure designed to remove any organic or metallic contaminants. The first step is to remove organic materials and this is done by immersing wafers in a 99 [%] HNO3 bath for 10 [min]. Next, wafers are rinsed for 5 [min] using deionized (DI) water. To remove metallic contaminants, another immersion is made using HNO_3 69.5[%] at 110 [^{o}C] for 10 [min]. During this process a small native oxide is formed on the wafer.

Removal of native oxide

After standard cleaning, high temperature annealing, or a given amount of time at room temperature, a native oxide is formed on the surface of the wafer. This must be removed before depositions can be made and is done via HF 0.55 [%] for 4 [min]. This is followed by 4 [min] rinsing with DI water, and then 1 [min] isopropyl alcohol (IPA) for drying.

NAOS tunnel oxide growth

In the fabrication of the IBC solar cells the tunnel oxide is grown via wet chemical oxidation. This step is done directly after the removal of the native oxide to ensure the uniformity of the c-Si surface and consistency in the tunnel oxide thickness between samples. Here the wafers are submerged in HNO_3 69.5 [%] at room temperature for 60 [min]. This leads to the growth of an SiO_x layer of thickness 1.4 [nm] [41][48]. This process is known as Nitric Acid Oxidation of Silicon (NAOS).

The major benefits of this process are that it is done at room temperature, unlike thermal oxidation, and that the formed oxide has uniform thickness and very low current leakage [49][44].

Low pressure chemical vapor deposition (LPCVD)

Low pressure chemical vapor deposition (LPCVD) is a commonly used method of layer deposition in semiconductor devices. The major benefit of LPCVD is that the low pressure process means minimal diffusion of the reactant gases. This leads to a high level of uniformity and purity in the layer [50]. The diagram of a LPCVD chamber is shown in figure.2.1.

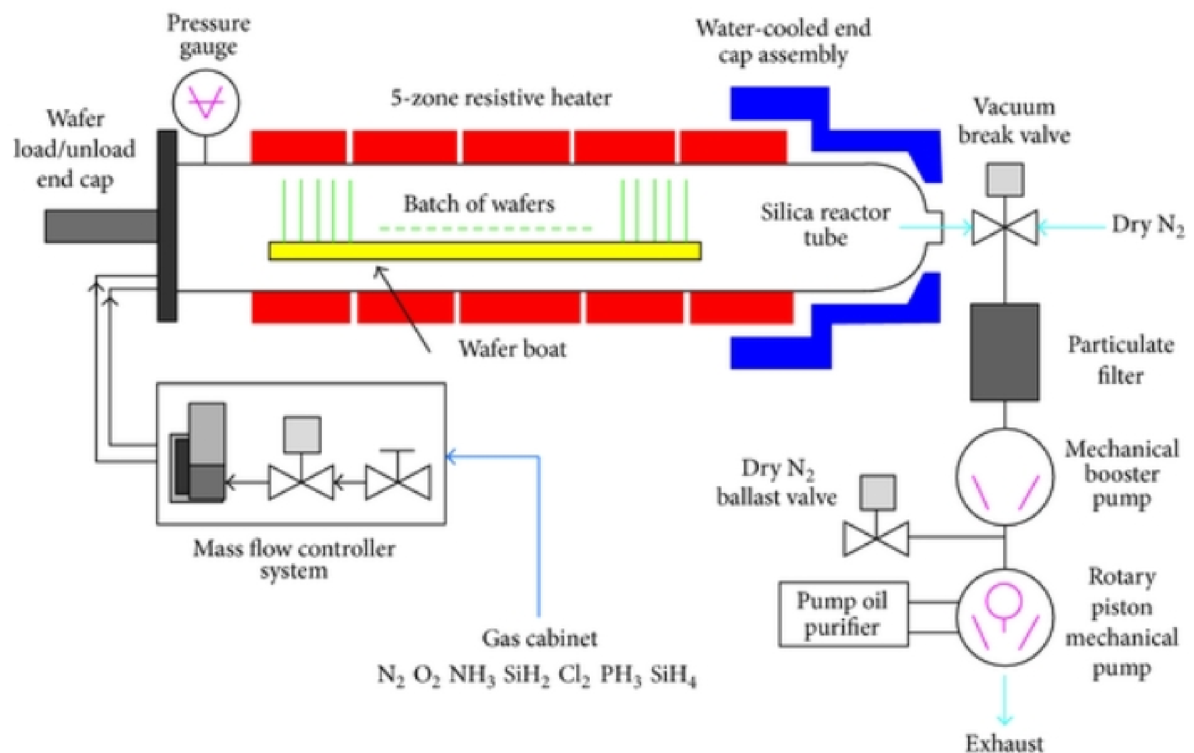

Figure 2.1: Schematic of LPCVD chamber [51]

In this thesis a LPCVD tube furnace from *Tempress Systems* was used to deposit 250 [nm] of a-Si on IBC cells. The parameters for the deposition are listed in table.2.2. This is deposited on both sides of the wafer. After the deposition step the furnace performs a post-deposition annealing at 600 [^{o}C] for 60 [min] to release stress from the layer. This layer is later annealed

to form the doped poly-Si layers at the rear of the device.

Table 2.2: LPCVD a-Si deposition parameters

Paramater	Value
SiH_4 flow [sccm]	45
Pressure [mTorr]	150
Temperature [^{o}C]	580
Deposition Rate [nm/min]	2.2

Photolithography

Photolithography is used design complex patterns on the wafer before fabrication. It can be used for the very precise definition of structures due to its small feature size, below 1 [μm], as compared with other technologies [52]. First a layer of photoresist (PR) is deposited across the entire wafer. This can be either positive or negative. Positive resist is sensitive to UV light and will undergo a chemical transition after a given exposure time. By covering the wafer with a mask, the PR can be exposed in the desired pattern for the next fabrication step. After the exposure the wafer is developed and any exposed material is etched away. In this process the unexposed PR is hardened, leaving the required design outlined by the exposure mask. For negative resist the opposite is seen. The exposed area is not etched during development, whilst the rest of the PR is. Once the necessary fabrication step has been completed using the PR pattern it is generally removed via immersion in Acetone. However, if the PR is further hardened in the following fabrication step, it can be removed by dry-etching with plasma [53].

In this thesis photolithography is used to define the emitter and back surface field (BSF) areas on the rear of the IBC devices. This way only the emitter is doped whilst the BSF can remain protected, and vice versa. It is also used to define specific regions for etching, and for the metal contact patterning. For the coating and development the *EVG 120* tool from *EV Group* was used. For exposure the *EVG 420 contact alligner* from *EV Group* was used.

Ion implantation

Ion implantation is used in solar cell fabrication to form doped semiconductor layers. This technique is very valuable as there is a large amount of control over the dopant species, dose and implantation energy. This allows for careful management of the doping profile within the device [54]. Ions from a chosen source are accelerated at high energy towards the wafer implanting the surface. This leads to a change in the physical and chemical properties of the target [55]. A key disadvantage of this process is the damage it causes during implantation. The ions collide with the surface at such high energies, that extra defects are added to the lattice. A diagram of this process is shown in figure.2.2.

Table 2.3: Parameters for ion-implantation of doped poly-Si regions

Region	Ion Species	Dose [ions-cm^{-2}]	Energy [keV]
FSF	P	Variable	10
BSF	P	6e15	20
Emitter	B	5e15	5

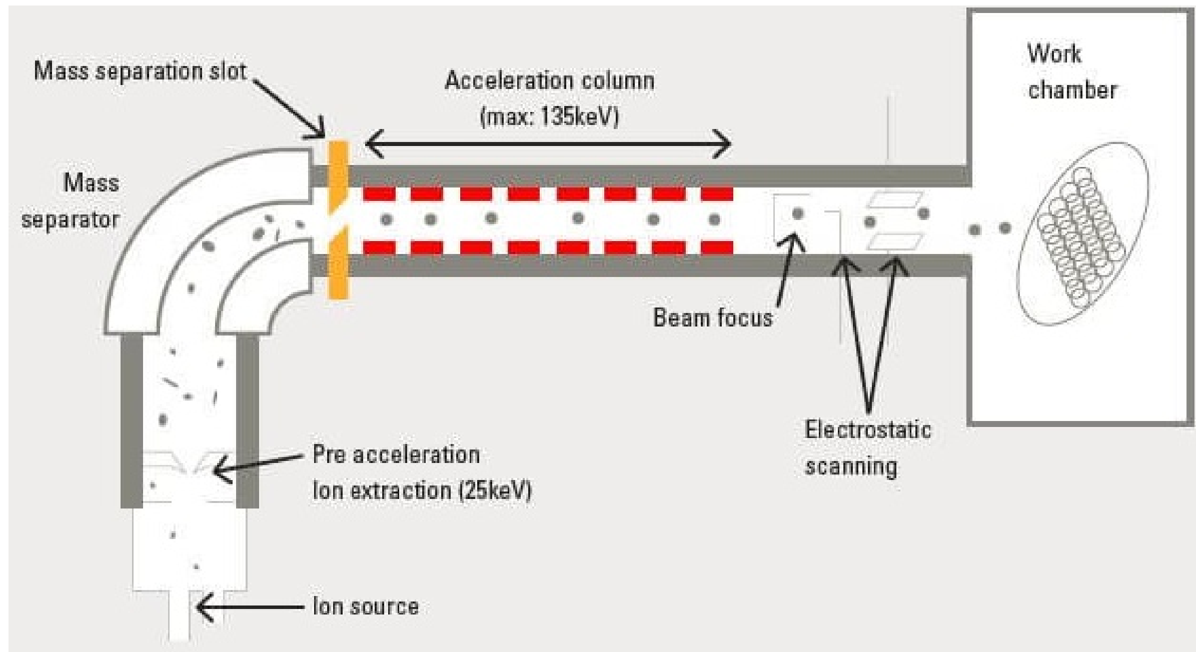

Figure 2.2: Schematic of ion-implantation process [56]

In this thesis ion-implantation was used to dope the emitter, BSF and FSF. For this purpose a *Varian* ion implanter was used. The doping species, dose and implantation energy for each of these layers is outlined in table.2.3.

Plasma enhanced chemical vapor deposition (PECVD)

Plasma enhanced chemical vapor deposition (PECVD) is used in the deposition of a wide range of materials in solar cell research. Usually, temperatures above 600 [^{o}C] are required to break up the precursor gases before layer depositions, but PECVD machines typically work between 200-400 [^{o}C]. This is due to the presence of a plasma which provides energetic free electrons and ions able to break the chemical bonds of the gases [57]. The plasma is ignited by placing a highly energetic field across the electrodes either side of the chamber. These machines are able to ensure good layer uniformity and quality and are industrially scalable [58]. A schematic of this process is shown in figure.2.3.

In this thesis 3 separate PECVD tools are used. First, the *Concept 1* supplied by *Novellus*, was used for thick depositions of SiN_x as capping layers. A 500 [nm] layer was deposited on the rear of the IBC cells to protect the doped regions before texturing the front surface. This technique was also used to protect the rear structure when texturing the front surface of the plasma oxide asymmetrical samples discussed in Chapter.5 and the FBC solar cells in Chapter.6. In all cases depositions were made at 400 [^{o}C] with a deposition rate of 21 [nm/s].

The second PECVD tool used in this thesis was the *Plasmalab System 100* produced by *Oxford Instruments*. This tool was used for the deposition of front surface passivation and rear hydrogenation materials for symmetrical tests, and eventually in the complete IBC devices. The materials and respective reaction rates and temperatures are shown in table.2.4.

The final PECVD tool used in this thesis was the *AMOR* manufactured by*Elettrorava*. This was used for the growth of the plasma oxide layers and subsequent a-Si depositions for symmetrical testing and finally the FBC solar cells. Here the deposition temperature was 300 [^{o}C].

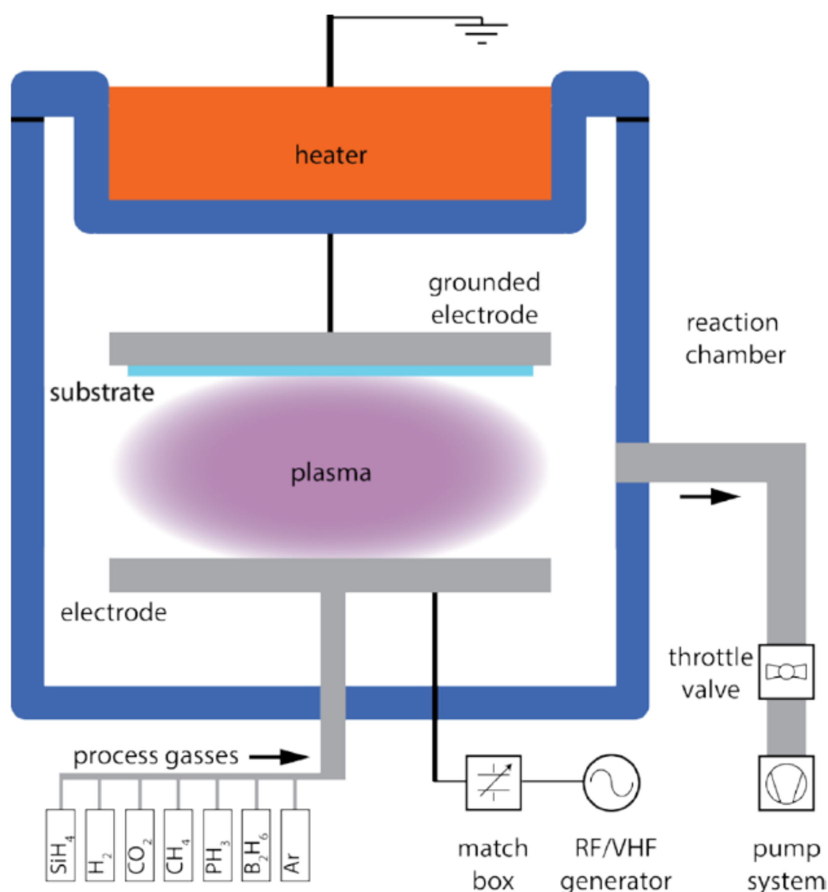

Figure 2.3: Schematic of PECVD chamber [58]

The deposition parameters for each layer are listed below:

The plasma oxide layers were deposited using a N_2O flow rate of 71 [sccm], an RF power of 5 [W], a pressure of 1.33 [mbar], a load of 17 and a tune of 15.

The intrinsic a-SiO_x layers had a SiH_4 flow rate of 4 [sccm], a CO_2 flow rate of 6.4 [sccm] and an H_2 flow rate of 35 [sccm]. The RF power used was 5 [W], the pressure was 1 [mbar], the load was 80 and the tune 27.

The n-type a-SiO_x layers had a SiH_4 flow rate of 4 [sccm], a CO_2 flow rate of 6.4 [sccm], an H_2 flow rate of 35 [sccm] and PH_3 flow rate of 4.8 [sccm]. The RF power used was 5 [W], the pressure was 1 [mbar], the load was 80 and the tune 27.

The p-type a-SiO_x layers had a SiH_4 flow rate of 8 [sccm], a CO_2 flow rate of 2 [sccm], an H_2 flow rate of 100 [sccm] and B_2H_6 flow rate of 5 [sccm]. The RF power used was 5 [W], the pressure was 2 [mbar], the load was 69 and the tune 27.

The p-type samples also had a different intrinsic layer deposition with a SiH_4 flow rate of 8 [sccm], a CO_2 flow rate of 2 [sccm], an H_2 flow rate of 100 [sccm] and B_2H_6 flow rate of 5 [sccm]. The RF power used was 5 [W], the pressure was 2 [mbar], the load was 69 and the tune 27.

Table 2.4: Oxford PECVD deposition parameters

Material	Deposition rate [nm/min]	Temperature [^{o}C]
a-Si:H	45	250
SiN$_x$:H	12	400
SiO$_2$	120	300

Texturing

Texturing is used to enhance light absorption in solar cells. This is achieved by anisotropic etching of the cells surface. The c-Si lattice can be described by two orientations: $<100>$ or $<111>$. When exposed to certain solutions these orientations are etched anisotropically. Etching in the $<100>$ plane proceeds much faster than the $<111>$, until this becomes the new lattice structure. This converts the initially flat surface to a series of random pyramids [59]. The pyramidal structure is much more effective at scattering incident light, increasing absorption in the cell [60]. Figure.2.4 shows an image of a textured c-Si surface.

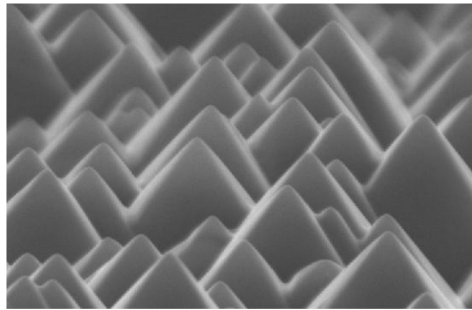

Figure 2.4: Random pyramid structure of c-Si surface after texturing [61]

In this thesis 25 [%] Tetramethylammonium hydroxide (TMAH) is used for surface texturing. Immersing wafers into this solution at 80 [^{o}C] and 300 [RPM] for 10 [min].

Etching

Etching of layers was done for multiple processes in this thesis. Most importantly it was done to etch the gap between the emitter and BSF regions on the IBC cells to avoid shunting. In this case, photolithography is first used to define the appropriate area between these regions to be etched. It was also used to remove the capping layer for the asymmetrical plasma oxide samples and FBC solar cells.

Two methods of etching were used; dry-etching and wet-etching. Dry-etching was used when the process required the use of photolithography. Here wet-etching cannot be used as there will have been some undercut. Wet-etching is therefore used when this was not an issue, such as in the fabrication of the asymmetrical samples and FBCs.

Dry-etching is done via plasma. Gas is pumped into the chamber and once the plasma is ignited, this gas is broken down into highly reactive species. These species then diffuse towards the surface being etched and are absorbed. After reacting with the exposed film they desorb removing part of this surface [62]. Some advantages of this process are better control of the etch rate and less material consumption as there is minimal etching of material below the PR

[63]. For dry-etching the *Drytek* tool from *Triode* was used. Figure.2.5 shows a diagram of this process.

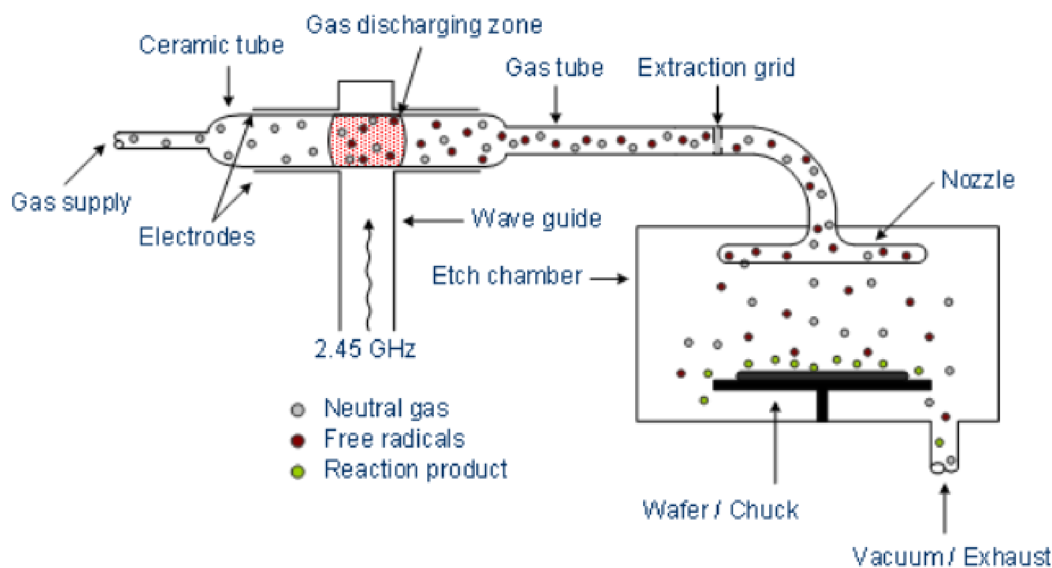

Figure 2.5: Schematic of dry-etching process [64]

Wet etching is done via immersing wafers into an echant solution. In this thesis Buffered Hydrofluoric acid, BHF, 1:7 solution was used to etch SiN_x. This has high selectivity of SiN_x against c-Si and etches isotropically at a rate of 18 [nm/min]. Similar to dry-etching, the first step is the diffusion of reactants towards the target surface. These reactants then diffuse into material reacting to form soluble products. Once formed these products desorb into the solution [62]. The key advantages of this process are the selectivity and simplicity. A major disadvantage is the undercut, or over-etch, seen when a mask is used. Being totally submerged in the etchant means material underneath the mask can be etched. This is shown in figure.2.6.

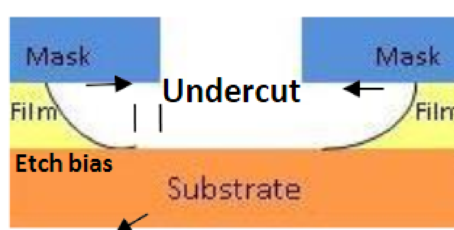

Figure 2.6: Undercut formed after wet-etching process [62]

High temperature annealing

High temperature annealing was performed throughout this thesis to crystallise the a-Si layers to poly-Si, and to activate the dopants. This leads to a lower series resistance in these layers due to the improved carrier mobility [33][65]. Conversely, this annealing may lead to the Boron dopants diffusing too deep, reducing the quality of the passivation. This step will also affect the integrity of the tunnel oxide layer, causing the formation of pinholes and potential layer breakdown for longer annealing periods.

To conduct the annealing a *Tempress Systems* tube furnace is again used. For the fabrication of the IBCs the annealing was at 950 [^{o}C] for 3 [min] in O_2 atmosphere. This does not include the ramp up and down times for these furnaces. For the FBCs and plasma oxide samples the annealing temperature was 850 [^{o}C] and the annealing time was variable.

Atomic layer deposition (ALD)

After the crystallisation of the poly-Si layers, the rear hydrogenation was applied to the IBC cells. This step involved different materials including SiO_x, SiN_x:H, AlO_x:H and a-Si. All of these layers were deposited using PECVD except the AlO_x:H layer which is was done via atomic layer deposition (ALD). This method was also used in the fabrication of the AlO_x:H/SiN_x:H symmetrical samples for front surface passivation tests.

ALD is a four step process. First the wafer is coated with Trimethylaluminium (TMA) precursor which adsorbs into the surface. Next, the remaining TMA vapor is purged, as well as any unwanted reactant products. The wafer is then exposed to a plasma containing highly reactive oxygen radicals that oxidise the surface. The final step is a second purge, where the unwanted products and remaining gas is removed. This process is self-limiting so a fixed thickness is achieved in each cycle [66][67]. Cycling multiple times allows for greater thicknesses . The *Flexal ALD* supplied by *Oxford Instruments* was used.

Forming gas annealing (FGA)

Forming gas annealing is a lower temperature annealing process typically done at 400 [^{o}C]. It is conducted in a 10 [%] H_2 in N_2 atmosphere. This adds extra H_2 atoms can diffuse into the c-Si bulk and passivate impurities [68]. In this thesis the hydrogenation step was conducted for 30 [min] at 400 [^{o}C] using a *Tempress Systems* tube furnace. This step was applied to all samples and solar cells.

Magnetron Sputtering

Magnetron sputtering was used for the deposition of the transparent conductive oxide (TCO) layer in the FBC cells. This was done to enhance the performance of the poly-Si layers deposited from *AMOR*, as these have poorer conductivity as compared with the LPCVD poly-Si. This method uses physical vapor deposition (PVD) technique known as sputtering to develop TCO layers.

nIn PVD, Argon gas particles are given high energy to bombard the TCO source material. This releases the source atoms which then diffuse towards the wafer. One major disadvantage of this process is the damage caused during sputtering [69]. This is balanced by an enhancement in optical properties, as the TCO also acts as an anti-reflective coating (ARC). The tool used for these depositions was the *Zorro* produced by *Polyteknik*. Figure.1.9 shows a schematic of the deposition process.

Commonly used TCOs include Boron-doped Zinc Oxide (ZnO:B), Fluor-doped Tin Oxide (SnO:F), Aluminium-doped Zinc Oxide (ZnO:A) and Hydrogen-doped (hydrogenated) Indium Oxide (InO:H) [9]. In this thesis Indium Tin Oxide (ITO) was used for the TCO material. This layer was 90 [%] In_2O_3 and 10 [%] SnO_2. The thickness was 75 [nm] on the front surface and 120 [nm] on the rear.

Metalisation

To complete the solar cell devices metal contacts must be added. The chosen process for

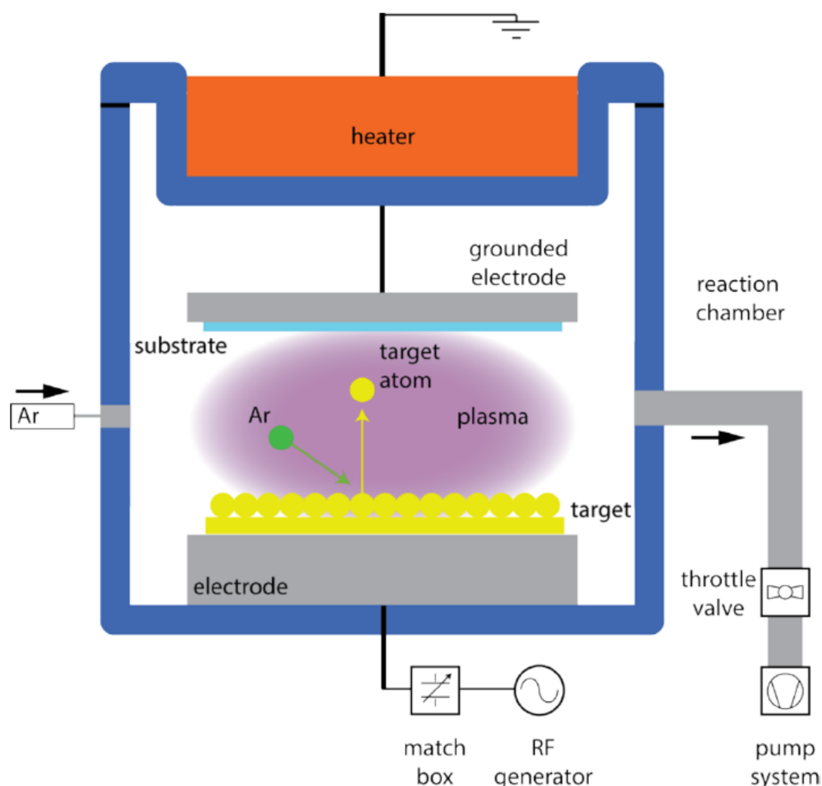

Figure 2.7: Schematic of magnetron sputtering process [58]

this differed between the IBC and FBC cells due to the sensitivity of the IBC front surface. As such, metal was deposited on the FBCs via screen-printing and on the IBCs via metal evaporation. Both of these processes are described below.

Screen-printing
When screen-printing the metal pattern is added to the cell by pushing Silver paste through a screen. This is done using a squeegee which sweeps the paste along the screen, falling through any gaps onto the cell below. Once this step is completed an annealing step is performed at 170 [^{o}C] for 60 [min] in air. The Silver paste used in this thesis was a low temperature Silver polymer paste from *DuPont*.

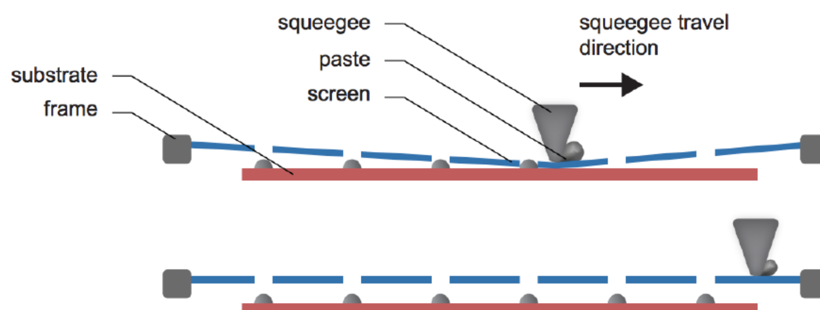

Figure 2.8: Schematic of screen-printing process [58]

Metal evaporation
In metal evaporation metal ingots of the required material are heated to above their melting

point and evaporated before deposition on the target wafer. This is done at high vacuum (10^{-5} Pa) to easily control the oxidation level and deposition thickness [70]. Once deposited the metal condenses back to a solid due to the lower temperature of the target. A schematic of this process is shown in figure.2.9.

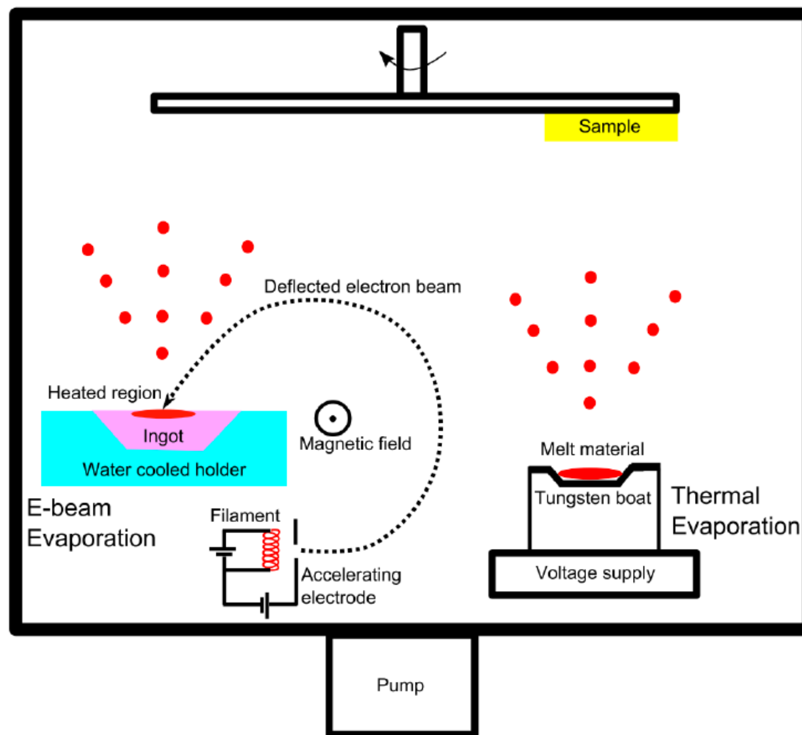

Figure 2.9: Schematic of metal evaporation process [70]

In this thesis the *Provac PRO500S* tool was used to deposit 2 [μm] Aluminium layers on the IBC cells.

2.2. Characterisation

Photoconductance lifetime tester

The photoconductance lifetime tester was used throughout experimentation to measure the quality of devices and samples throughout the fabrication process. By exposing samples to a short pulse of light, 1/64 [s], the photoconductance caused by the recombination of excess generated carriers can be measured [71]. Analysing this data allows for the lifetime, τ_{eff}, implied V_{oc}, iV_{oc} and recombination current, J_0, to be calculated. For this measurement the *Sinton WCT-120* available from *Sinton Instruments* was used. A schematic of this process is shown in figure.2.10.

Ellipsometry

When designing solar cells knowing the correct thickness of the applied layers is paramount. To measure these values ellipsometry was used. Ellipsometry is a technique that measures the difference between incident and scattered light to determine the properties of a material surface [72]. In this thesis it was used to confirm the thickness of all layers used in the fabricated devices and samples. In particular, it was used to determine the thickness of the plasma oxide layers in Chapter.6. For this process the *M-2000DI* from *J.A. Woollam Co.* was used. A

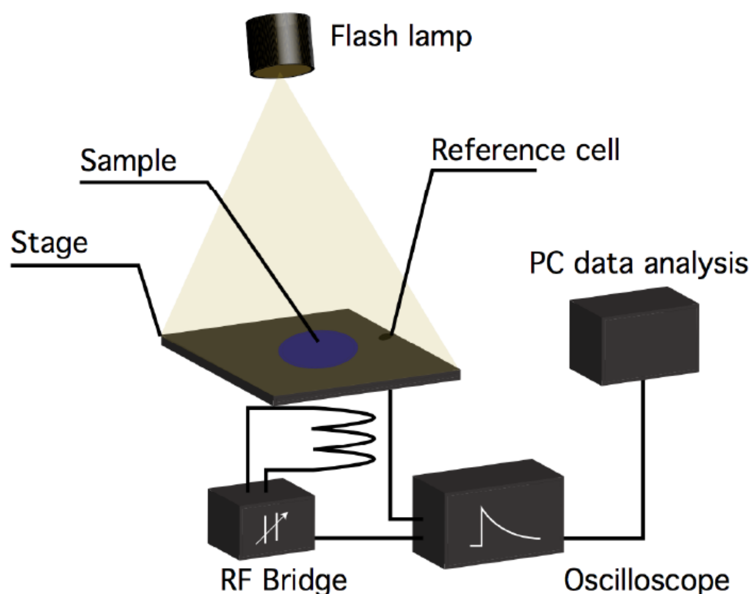

Figure 2.10: Schematic of photoconductance lifetime tester [58]

schematic of this process is shown in figure.2.11.

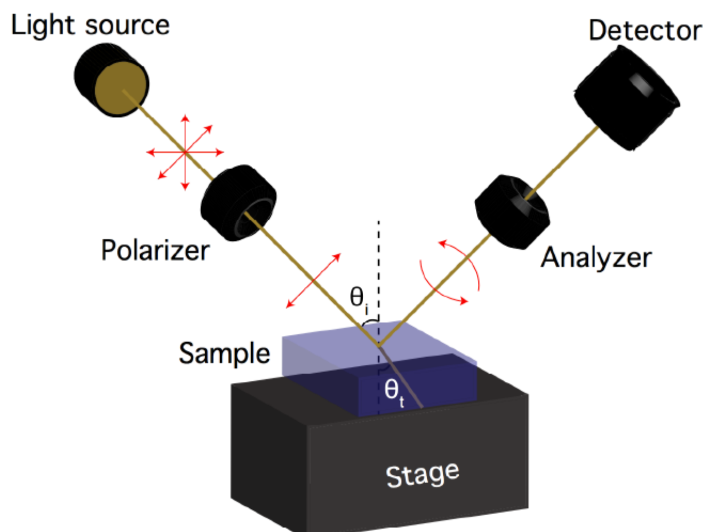

Figure 2.11: Schematic of ellipsometry procedure [58]

Suns-Voc

The Suns-Voc measurement is an IV curve measurement in which two separate cells are used. On one cell the V_{oc} is measured and on the other the light intensity. The experiment is conducted by flashing cells with a Xenon lamp. The advantages are that the measurements are quick so there is little heating of the cell and there is no series resistance effect. Because of this it is often used to check cell properties before metalisation has been added. The disadvantages are that Xenon is not a good representation of the AM1.5 spectrum. The light is not spatially uniform [73]. In this thesis it was used for the measurement of the FBC cells.

Tranmission line measurement
The Transmission line measuremen was used to measure the contact resistance of the plasma oxide layers. This technique involves measuring the resistance across a layer with varying distance between the measured points. Plotting these results allows analysis of the contact and sheet resistance of the desired layer from the y-intercept and gradient respectively, as shown in figure.2.12.

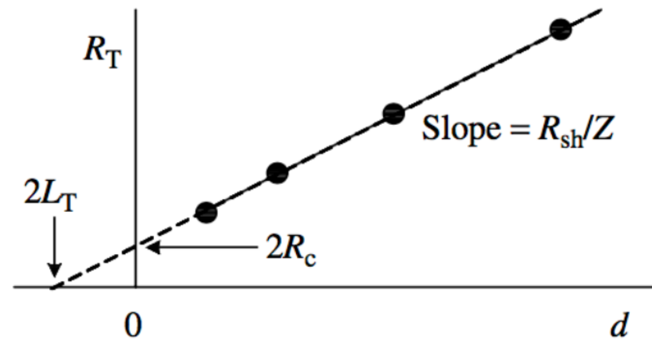

Figure 2.12: Calculation of contact and sheet resistance via TLM method [74]

Current-voltage measurement
To determine the current and voltage characteristics of the IBC cells the *Wacom WXS-156S-L2* solar simulator was used. This simulates standard test conditions for solar cell measurements: 1000 [Wm^{-2}], 25 [^{o}C] and the AM1.5 spectrum. The spectrum is represented using a combination of halogen and xenon lamps, whilst the temperature is regulated via the stage. Making a sweep across a desired voltage range an IV curve is generated. The setup for this instrument is shown in figure.2.13.

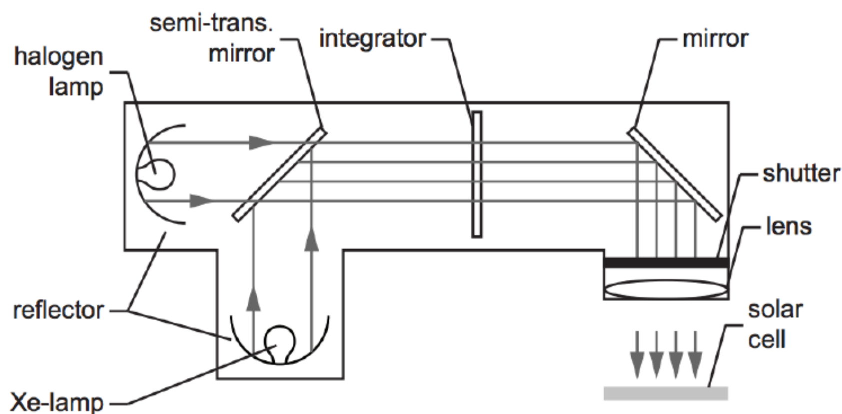

Figure 2.13: Wacom current-voltage measurement set up [58]

3

Front surface field and rear hydrogenation for IBC cells

In this chapter different options for the front surface (FS) passivation and rear hydrogenation of the IBC solar cells are investigated. For the FS, 4 passivation stacks are chosen and their quality is compared under different forming gas annealing (FGA) conditions. The best candidate is then tested against varying doping levels for the front surface field (FSF). For the rear, 4 material stacks are again chosen. These are all tested with the same FGA step. The chapter begins by introducing the FS passivation materials, and the process taken to prepare the samples. Next, the results after different FGA times and FSF doping levels are presented. The rear hydrogenation materials are then introduced and their sample preparation explained. This is followed by a performance analysis of each of the layers. Finally, the chapter concludes with a summary of the findings and the selection of the optimal conditions for the poly-Si IBC solar cells.

3.1. Front surface field

Before discussing the materials tested it is important to note the motivation for this particular research. The left image of figure.3.1 shows the simulated external quantum efficiency (EQE) for the former poly-Si IBC cell design [75]. On the right of this figure, the cell design is shown for reference. In this case a-Si:H/SiN$_x$:H was used for FS passivation. Looking at the plot it is clear that there is a significant amount of absorption for the a-Si:H layer. This is parasitic absorption and is particularly harmful as it is in the short wavelength, high energy, photon range. It is the aim of this section to reduce this parasitic absorption by finding a material stack which is transparent in the c-Si absorption range. The effect of the rear hydrogenation step on the FS passivation is also studied. This is done to understand whether this should be performed before or after the FS passivation is applied to the poly-Si IBC cells.

3.1.1. Materials

In this work, four different passivation stacks were tested. These stacks and test structures are shown in figure.3.2. First, SiO_2/SiN$_x$:H of thickness 10 and 75 [nm] respectively. The SiO_2 is the passivation layer whilst the SiN$_x$:H layer acts as an antireflective coating - as in each of the tested stacks. It also provides hydrogenation to the c-Si interface. Second, SiO_2/AlO$_x$:H/SiN$_x$:H of thickness 10, 10 and 75 [nm] respectively. Here the SiO_2 and AlO$_x$:H are used as primary and secondary passivation layers. The AlO$_x$:H layer will also be used

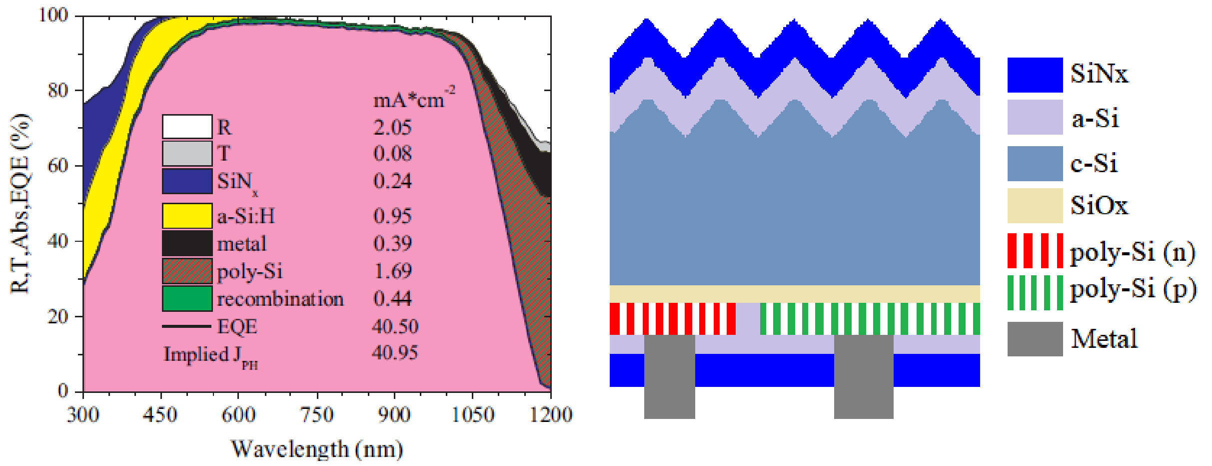

Figure 3.1: Left: Simulated EQE of former poly-Si IBC cell. a-Si:H front surface passivation shows significant absorption of high energy photons within the range of c-Si, lowering device performance [75]. Right: Design of simulated poly-Si IBC cell.

to provide hydrogenation. The third stack was AlO_x:H/SiN_x:H of thickness 10 and 75 [nm] respectively. Each of these 3 stacks is chosen as they effectively optically transparent in the range of c-Si light absorption [14][15][18][19]. As such, they will show minimal parasitic absorption as compared with the former device - offering the possibility for higher cell performance. The final stack tested was a-Si/SiN_x:H of thickness 18 and 75 [nm] respectively. This is slightly lower than the thickness used in figure.3.1 [40] which was 22 [nm] with a view to lowering the parasitic absorption.

Table 3.1: Passivation materials and layer thicknesses

Wafer	Material 1	Thickness [nm]	Material 2	Thickness [nm]	Material 3	Thickness [nm]
1	SiO_2	10	SiN_x:H	75	-	-
2	SiO_2	10	AlO_x:H	10	SiN_x:H	75
3	AlO_x:H	10	SiN_x:H	75	-	-
4	a-Si	18	SiN_x:H	75	-	-

3.1.2. Sample Preparation

Starting from n-type floatzone <100> oriented wafers, samples must first be textured to replicate the structure of the cell FS. This is done by immersing the wafers in TMAH solution at 80 [^{o}C] and 300 [RPM] for approximately 10 [min]. The solution etches in the <100> direction faster than the <111> such that <111> is the new lattice that is formed [9].Next, a 10 [nm] SiO_2 layer is grown via thermal oxidation at 950 [^{o}C].

For the SiO_2/SiN_x:H wafer, next the 75 [nm] SiN_x:H deposition is made using plasma enhanced chemical vapor deposition (PECVD) at 400 [^{o}C]. For the SiO_2/AlO_x:H/SiN_x:H wafer, 10 [nm] AlO_x:H is deposited via plasma atomic layer deposition (ALD) at 250 [^{o}C], before the SiN_x:H deposition. The AlO_x:H/SiN_x:H followed the same procedure, but in this case the SiO_2 was removed with HF 0.55 [%] before the AlO_x:H deposition. The SiO_2 layer was also removed for the a-Si/SiN_x:H wafer. Here, the a-Si layer was deposited using PECVD at 250

[^{o}C]. More specific details about these depositions are given in Chapter. 2. The flowchart for each wafer is shown in figure.3.2.

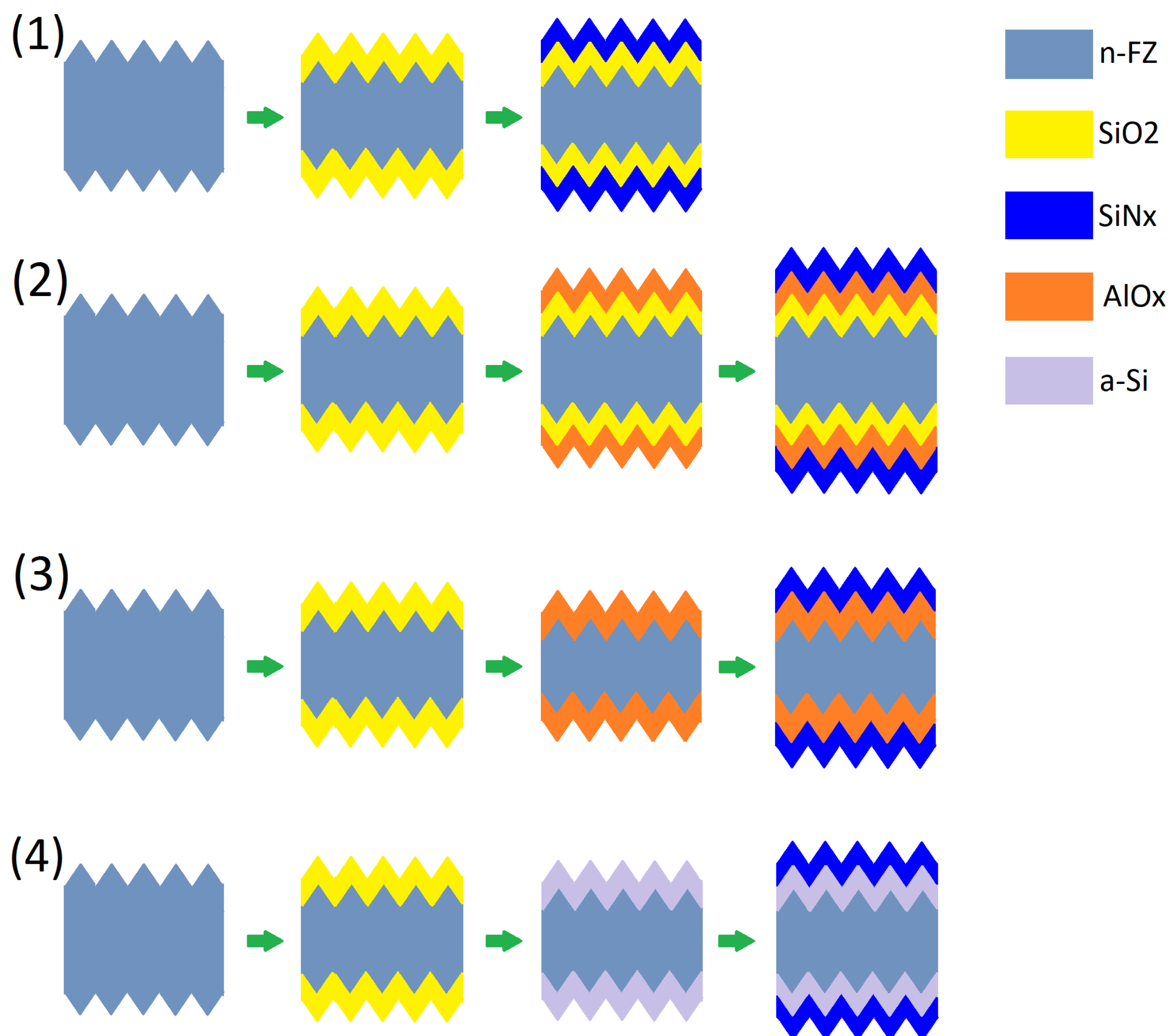

Figure 3.2: FS passivation flowchart. All wafers started from n-type <111> oriented wafers with 10 [nm] SiO_2 from thermal oxidation at 950 [^{o}C]. Sample (1) - SiO_2/SiN_x:H: 75 [nm] SiN_x:H added from PECVD at 400 [^{o}C]. Sample (2) - SiO_2/AlO_x:H/SiN_x:H: 10 [nm] AlO_x:H added from ALD at 250 [^{o}C] and 75 [nm] SiN_x:H from PECVD at 400 [^{o}C]. Sample (3) - AlO_x:H/SiN_x:H: SiO_2 layer removed using HF 0.55 [%]. 10 [nm] AlO_x:H applied from ALD at 250 [^{o}C] and 75 [nm] SiN_x:H from PECVD at 400 [^{o}C]. Sample (4) - a-Si/SiN_x:H: SiO_2 removed using HF 0.55 [%]. 18 [nm] a-Si and 75 [nm] SiN_x:H deposited from PECVD at 250 and 400 [^{o}C] respectively.

Once the wafers were prepared they were cut into quarters and subjected to following FGA times; 0, 10, 20 and 30 [min]. In each case the annealing temperature was 450 [^{o}C]. This was chosen as it was slightly above the temperature for the SiN_x:H deposition and also above the typical 400 [^{o}C] to observe the impact on layer stability. Finally the rear hydrogenation step of 400 [^{o}C] for 30 [min] was applied samples. This was conducted using 10 [%] H_2 ratio in N_2.

For the doped passivation tests, ion implantation is performed after the texturing step. To activate and drive in these dopants annealing was performed at 950 [^{o}C] for 3 [min] in O_2 atmosphere. A 4 [min] HF 0.55 [%] dip was then performed to remove the thermal oxide grown during annealing. Five dopant doses were studied; no doping, 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}]. These equate to doping concentrations at a depth of 10 [nm] of 0, 2e19,

4e19, 7e19 and 1e20 [atoms-cm^{-3}] respectively.

3.1.3. Undoped front surface passivation

In this section the results for the passivation test after varying FGA times are presented. The times selected were; 0, 10, 20 and 30 [min]. The 0 [min] condition should be taken as 400 [^{o}C] from the SiN$_x$:H. For all other times the temperature was 450 [^{o}C]. The effect of the rear hydrogenation step on these samples is also discussed. This was a 30 [min] FGA at 400 [^{o}C] in a 10 [%] H_2 in N_2. The results for both tests are shown in figure.3.3.

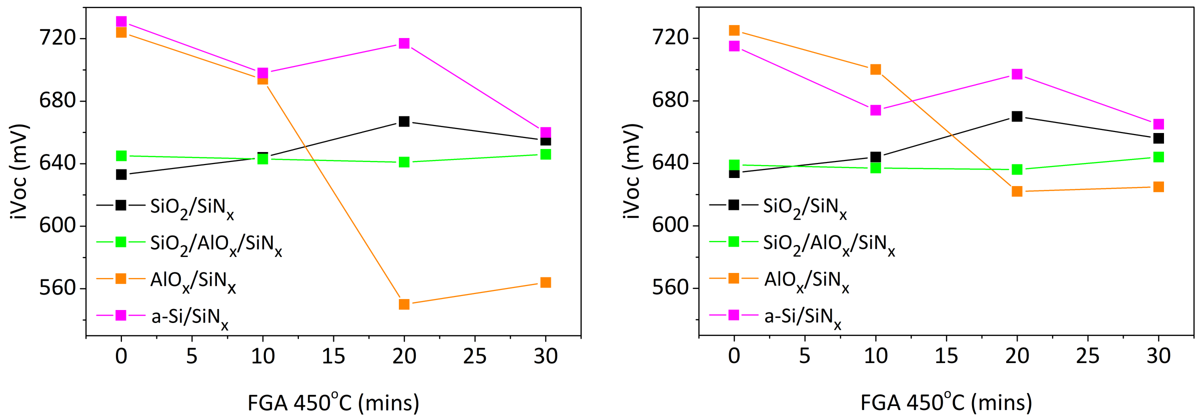

Figure 3.3: Left: Passivation quality of symmetrical samples against FGA time at 450 [^{o}C]. Right: Passivation quality of the same samples after applying the rear hydrogenation step for the cell. This was a 400 [^{o}C] FGA for 30 [min]

Starting with wafer 1, SiO$_2$/SiN$_x$:H, in the left plot a trend of slight improvement can be seen for longer annealing. This effect saturates at 20 [min] with a peak iV_{oc} of 667 [mV] and a J_0 of 19.8 [fAcm^{-2}]. The improvement is thus coming from the additional chemical passivation coming from the H_2 atoms during FGA at 450 [^{o}C]. At 30 [min] this effect is no longer seen. The sheet resistance for each of the samples is consistent at 142 [Ω-sq^{-1}] so the performance drop will be coming from H_2 effusion as opposed to changes in the integrity of the c-Si/passivation interface. Especially given that the SiO_2 deposition was made at 950 [^{o}C], so will be stable under these conditions. Overall, the passivation quality of this layer is quite low owing to the fact that there almost no field effect passivation occurring due to the low density of fixed charge in the SiO_2 layer.

The application of the rear hydrogenation step has almost no effect on the passivation quality. There is a slight increases in the peak value which goes up from 667 to 670 [mV], but this is so small that it can probably be attributed to a variation in the measurement output from the equipment. At this temperature the H_2 is unable to penetrate through the SiO_2 layer to impact the chemical passivation.

Moving on to wafer 2, SiO$_2$/AlO$_x$:H/SiN$_x$:H, it is clear that the 450 [^{o}C] FGA is having no effect on the samples here. The best performing condition comes after 30 [min] annealing with an iV_{oc} of 646 [mV] and a J_0 of 12.7 [fAcm^{-2}]. This is only 5 [mV] higher than the worst performing sample, which is after 20 [min] annealing. It would appear that this combination of layers is inhibiting the flow H_2 atoms towards the surface and the chemical passivation is limited by the quality of SiO_2 layer. Indeed, comparing the case for no annealing with the best sample it can be seen that the iV_{oc} values are almost the same. Again there is almost no field effect

passivation here, which adds to the poor passivation quality. The negative field effect from the AlO_x:H is also not seen. The thickness of the SiO_2 layer is enough to mitigate this.

This wafer shows approximately a 5 [mV] drop across each of the samples after the rear hydrogenation. Based on the fact that this step had almost no impact on the SiO_2/SiN_x:H sample this can be attributed to a reduction of in the H_2 density of the AlO_x:H layer. Overall, it can be said that the rear hydrogenation is having little impact, however. Once again the SiO_2 layer is inhibiting the diffusion of H_2 under FGA at 400 [^{o}C].

Wafer 3, AlO_x:H/SiN_x:H, shows very promising results and has a peak value of 724 [mV] and a J_0 of 5 [fAcm^{-2}] for the 400 [^{o}C] as deposited condition. This layer is providing very effective chemical passivation as compared with wafers 1 and 2. The hydrogen content of the AlO_x:H is able to reduce the density of defects at the c-Si/AlO_x:H/SiN_x:H interface. After 450 [^{o}C] FGA the quality drops dramatically. Annealing at this temperature is already too high and is causing a breakdown of the AlO_x:H layer. It is true that the ideal annealing window for AlO_x:H is between 150-250 [^{o}C], and already at 300 [^{o}C] the passivation quality begins to fall [76]. After FGA there will also be some diffusion of the negative corona charges in the AlO_x:H layer leading to a detrimental field effect. Under no FGA this field effect is not so significant due to the formation of a thin SiO_2 layer upon deposition [76] which is able to mitigate these charges. Considering possible implementation into IBCs, as stated previous, this layer is optically transparent within the absorption range of c-Si so the 0 [min] condition would be a very strong candidate as a front surface passivation material.

This wafer was unaffected by the hydrogenation for the best performing samples, but shows a significant increase for the poorer performing ones. This gives some extra insight into how annealing at 450 [^{o}C] was degrading the passivation quality. At the higher temperature there must be some H_2 effusion from the samples. By subjecting them to a second hydrogenation step, some of these atoms are replaced and the chemical passivation improves. Crucially this is done at a lower temperature which aids the stability.

Wafer 4, a-Si/SiN_x:H, shows the best passivation quality with an iV_{oc} of 731 [mV] and a J_0 of 4 [fAcm^{-2}], for the as deposited 400 [^{o}C] condition. As there are very weak corona charges this passivation is coming entirely from the H_2 content within the a-Si/SiN_x:H layers during deposition. The quality drops significantly after FGA at 450 [^{o}C]. The temperature is too high for the stability of the a-Si:H layer which peaks at 400 [^{o}C] [77]. Thus there may be some H_2 effusion that has lowered performance.

Applying the rear hydrogenation has a negative effect on all of the samples except the lowest performing 30 [min] case. Keeping the samples at this temperature for so long is obviously also affecting the stability of the a-Si:H layer. This wafer was already exposed to this temperature during the SiN_x:H deposition, but this is for a shorter period of 10 [min] (including loading/unloading and pumping).

In summary, it is clear that the 2 most interesting passivation stacks are wafer 3, AlO_x:H/SiN_x:H, and wafer 4, a-Si:H/SiN_x:H. Both of these performed best under 0 [min] FGA, or rather the 400 [^{o}C] as deposited annealing from the SiN_x:H layer. The iV_{oc} values for these samples were 725 and 731 [mV] respectively. For wafer 3, the quality was unaffected by hydrogenation, whilst wafer 4 saw a significant drop. In principle the preferred layer for further investigation would be wafer 3 due to the parasitic absorption in associated with a-Si:H. However, due to

problems with this machine this research could not be continued. To replace this, a second plasma ALD tool was used to replicate this layer. The results of this deposition are investigated in the next section.

AlO_x:H at 300°C

In this section the results are given for the second ALD tool working at 300 [^{o}C] as opposed to 250 [^{o}C]. Here the samples are tested under no annealing and then subjected to a range of different FGA conditions in pursuit of similar passivation quality. Finally, they are again subjected to the rear hydrogenation step of 400 [^{o}C] for 30 [min].

The FGA temperatures used vary from 300-700 [^{o}C], as well as a no FGA condition. The time for each annealing was 5 [min], except for in two of the 600 [^{o}C] cases where 10 and 15 [min] were used. Temperatures selected were based on the limit of the stability window and also research from Kersten et al [78], which demonstrated the gains in performance after annealing at high temperature for short periods. The results are shown in in figure.3.4.

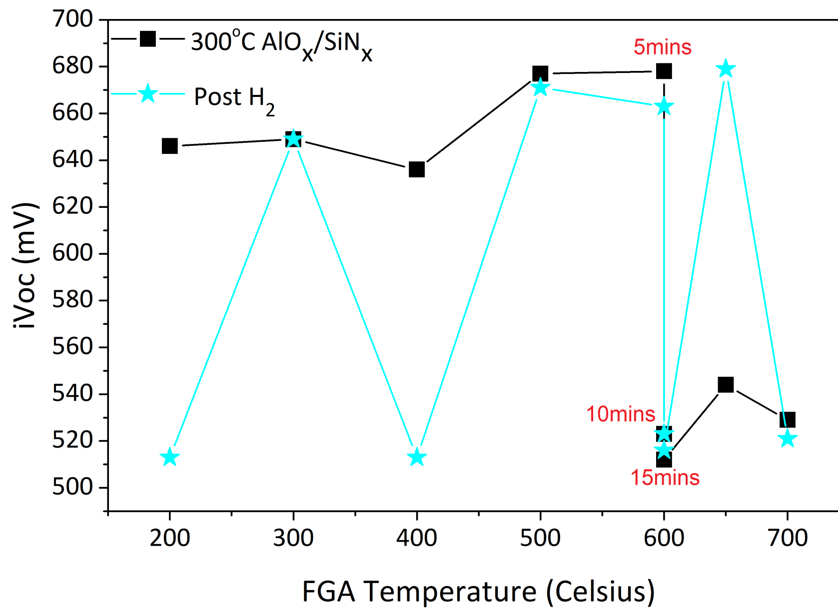

Figure 3.4: Passivation quality of AlO_x:H from ALD at 300 [^{o}C]. All samples annealed for 5 [min] except the indicated samples at 600 [^{o}C]. The black line shows the results before the rear hydrogenation step was applied. The blue shows the results after. The rear hydrogenation consisted of a 400 [^{o}C] FGA in 10 [%] H_2 in N_2 atmosphere for 30 [min].

Unfortunately this new tool was unable to achieve similar passivation quality for the as deposited condition and is in fact significantly worse. As mentioned above, the ideal temperature window for AlO_x:H ALD depositions is 150-250 [^{o}C] so it is unsurprising that this layer does not achieve the same performance. Looking at the black curve on the graph, the effect of the different FGA temperatures before the rear hydrogenation can be seen. It is clear that none of the applied FGA conditions is capable of achieving the same passivation quality as the deposition at 250 [^{o}C]. The 500 [^{o}C] and 600 [^{o}C] 5 [min] tests show the highest improvement. This is related to a decrease in interface state density [78]. The effect saturates above 600 [^{o}C], or for times longer than 5 [min] at this temperature. After the rear hydrogenation is applied the results are somewhat similar. The only major changes are in the 400 [^{o}C] and 650 [^{o}C]

samples. The first of which sees a massive drop in performance

Based on these results, the structure for wafer 3 can no longer be implemented into the poly-Si IBC cells. As such, a-Si:H/SiN$_x$:H was selected as the material stack to passivate the front surface. To reduce the effect of parasitic absorption, this layer was tested with different thicknesses alongside the varying doping levels for the FSF. This procedure is described in the next section. The findings from these tests also show that the rear hydrogenation step should be performed before the FS passivation, to preserve the quality of the a-Si:H layer.

3.1.4. Doping of front surface field

In this section the results are presented for the investigation of the passivation layer against doping for the front surface field. The selected layer was a-Si:H/SiN$_x$:H of thicknesses 18 and 75 [nm] respectively. This replicates the FS passivation of the previous device structure [40] but with a slightly decreased thickness. The original was 22 [nm]. To minimise the effect of parasitic absorption, different a-Si:H layer thicknesses are investigated. The selected thicknesses were; 4.5, 9, 13.5 and 18 [nm]. The chosen dopant doses for the front surface field were; No doping (No FSF), 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}]. These equate to doping concentrations at a depth of 10 [nm] of 0, 2e19, 4e19, 7e19 and 1e20 [atoms-cm^{-3}] respectively. The results of these tests are shown in figure.3.5

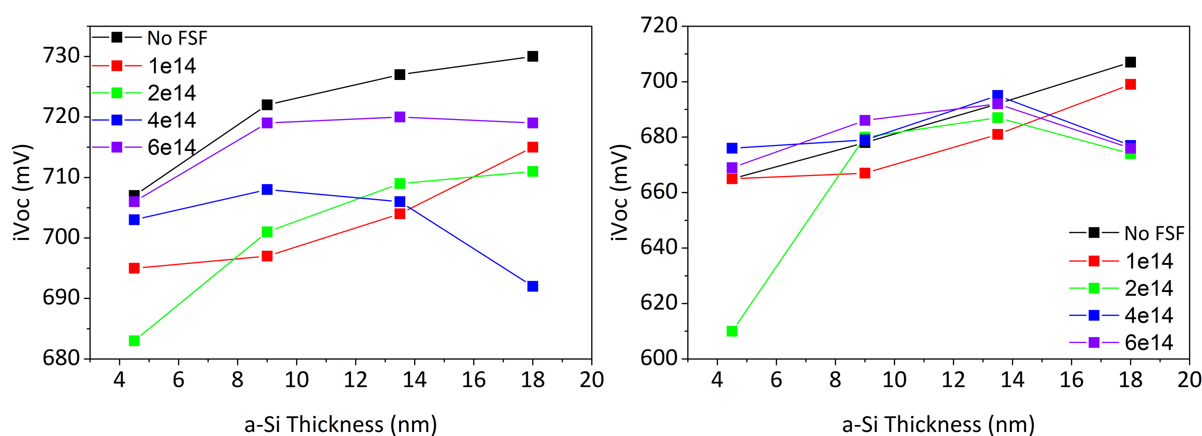

Figure 3.5: Passivation quality of a-Si:H/SiN$_x$:H with varied thickness, against dopant dose for front surface field in [ionscm^{-2}]. Left: Passivation quality before the application of the rear hydrogenation step. Right: Passivation after rear hydrogenation applied. Please note the y-axis scale is different on each graph.

Looking at the case before rear hydrogenation, it is clear that the best results are seen for the samples with no front surface field. The best value comes for the a-Si:H 18 [nm] thickness with an iV_{oc} of 730 [mV] and a J_0 of 13.5 [fAcm^{-2}]. This reproduces the performance of the initial passivation test which obtained 731 [mV] and a J_0 of 4 [fAcm^{-2}]. The increase in J_0 probably comes from a slight difference in the wafer quality, or perhaps damage during handling. Moving along the No FSF curve shows there is a correlation between decreasing thickness and poorer performance. This trend is seen for almost all of the samples. Reducing the thickness, despite lowering the parasitic absorption, is also reducing the chemical passivation. This is caused by a decrease in the available H_2 within the a-Si:H/SiN$_x$ layer to passivate the c-Si/a-Si:H/SiN$_x$ interface.

Analysing the doped samples shows that these are significantly worse than the case with No FSF. The only FSF able to come close to the No FSF values is the 6e14 curve, which peaks at 720 [mV] with a J_0 of 13.2 [fAcm^{-2}] for a thickness of 13.5 [nm]. Ion-implantation

introduces defects during the bombardment of the c-Si surface that lowers the performance. Furthermore, adding extra majority carriers will have contributed to the Auger recombination. In fact, at a dose of 6e14 [ions-cm^{-2}] the FSF can be considered an n-type layer, and so this will also exhibit some parasitic losses due to the free carrier absorption [9].

Analysing the effect of doping shows a second trend in the data. Increased doping leads to better passivation quality. This reveals a relationship between the field effect passivation introduced by the dopants, versus the extra Auger and surface recombination introduced by ion-implantation. At a dose of 6e14 [ionscm^{-2}] the field effect is almost strong enough to compensate this extra recombination, and so is very close to the No FSF curve.

The 4e14 wafer is the only curve which does not show a trend of increasing performance with thickness. Here the iV_{oc} saturates at a value of 708 [mV] for a thickness of 9 [nm]. At 18 [nm] this has dropped to 692 [mV]. It is not entirely clear why this is the case. It could be that the combination of parasitic absorption from the a-Si:H, and the introduced defects/Auger recombination from the ion-implantation, becomes too large for effective passivation and so the quality begins to drop.

After applying the rear hydrogenation step the passivation of all samples drops significantly. This is to be expected, as discussed previously, exposing the wafers to 400 [^{o}C] for 30 [min] leads to H_2 effusion from the a-Si:H layer. The effect is most extreme on the 18 [nm] doped samples, but all of the samples tend towards iV_{oc} values of 670-680 [mV]. This seems to be limit of the passivation due the balance between the introduced defects from ion implantation and the extra field effect passivation.

The No FSF and 1e14 curves are the only ones which manage to maintain the original trend of increased performance with thickness after the rear hydrogenation. This can again be used as evidence that the ion implantation is introducing extra recombination as these are still able maintain good values after the H_2 effusion from the a-Si:H layer. In this case the degradation of this a-Si:H layer does not lead to such a plateau in results, showing that even with poorer passivation quality there is still some value in having the layer present. It is still providing a noticeable amount of chemical passivation. This hydrogenation step also reveals that the 2e14 sample of thickness 4.5 [nm] is a real outlier for this data. After this process there is almost an 80 [mV] drop in performance which is much larger than any of the other samples. There is clearly some other issue impacting performance, perhaps contamination or damage during handling.

As determined earlier, when implementing this layer in IBCs, the rear hydrogenation step should be performed before the front surface passivation in order to preserve the quality. Concerning the a-Si:H layer thickness it is of more interest to measure the effect of thinner layers with respect to the device presented in [40]. In this way the parasitic absorption can be reduced and perhaps better efficiencies can be achieved. With this in mind it seems that 9 [nm] layer is the best option. Here there are still reasonably high values of 722 and 719 [mV] for the No FSF and 6e14 cases respectively. The 4.5 [nm] layer would be too thin, and presents too high a risk of damage during handling. To further investigate the effect of the FSF doping each of the tested doses will also be implemented into the poly-Si IBCs. This means there will be in total 5 IBCs each with the 9 [nm] a-Si:H and 75 [nm] SiN_x:H passivation layers.

3.2. Hydrogenation of rear structure

The aim of this section is to find the optimum hydrogenation condition for the rear cell structure. This is done to improve the quality of the poly-Si/tunnel oxide passivating contact. To understand the performance on both the emitter and BSF layers symmetrical samples are prepared with each of these structures.

3.2.1. Materials

As in the previous section, 4 material stacks were chosen for the rear hydrogenation tests. The first was a SiN_x:H layer of thickness 75 [nm]. SiN_x:H is very good at hydrogenating n-type layers thanks to its high H_2 content [16][17]. It should also well hydrogenate the p-type poly-Si layer but the performance will be lower due to the detrimental field effect from the positive corona charges. Second was SiO_2/SiN_x:H of thickness 100 and 75 [nm] respectively. PECVD SiO_2 has high H_2 content [13] and should therefore hydrogenate both the p- and n-type poly-Si layers and their interfaces effectively. The third stack was AlO_x:H/SiN_x:H of thickness 20 and 75 [nm] respectively. As previously mentioned, AlO_x:H also contains H_2 [19] so should demonstrate strong hydrogen passivation on both the n- and p-type layers. Its high density of fixed negative charge, should make the overall performance slightly better on p-type layers generally [13]. Finally, the fourth sample was a-Si:H/SiN_x:H of thickness 6 and 75 [nm] respectively. Much like the SiN_x:H layer, a-Si:H has a very high H_2 content [22][23], so this should well hydrogenate both the n- and p-type layers effectively.

3.2.2. Sample preparation

The successful candidate for rear hydrogenation will be implemented at the back of the device which is flat so n-type $<$100$>$ wafers were used. All of the following steps are applied to both sides of the wafer to create symmetrical samples. The hydrogenation layer comes after the poly-Si passivation layer, so the first step was to grow the NAOS tunnel oxide, and then use LPCVD to deposit a-Si:H. The NAOS deposition was via wet chemical oxidation in 69.5 [%] HNO_3 solution for 60 [min]. This leads to a layer thickness of 1.4 [nm] [79]. The a-Si:H deposition is at a temperature of 580 [^{o}C] and had a thickness of 250 [nm].

Hydrogenation quality needed to be tested for both the p-type emitter and the n-type back surface field (BSF) of the IBC. To do this, separate symmetrical samples were made with the appropriate implantation dose for the emitter, 5e15 [ionscm^{-2}], or BSF, 6e15 [ionscm^{-2}]. To crystallise the poly-Si layer, and activate and drive in the dopants, a high temperature annealing was conducted at 950 [^{o}C] in O_2 atmosphere. During this step a 10 [nm] native oxide layer is formed which must be removed before contacting. This was done by immersion in HF 0.55 [%]. Finally, the hydrogenation materials are deposited.

All layers were deposited using PECVD except the AlO_x:H layer which was via plasma ALD at 300 [^{o}C]. For SiN_x:H this was at 400 [^{o}C]. For SiO_2 and a-Si:H, at 300 [^{o}C] and 250 [^{o}C] respectively. The materials and thicknesses for each wafer are outlined in table.3.2. After these depositions forming gas annealing (FGA) at 400 [^{o}C] for 30 [min] was conducted. The gas ratio was 10 [%] H_2 in N_2. This is done to add extra H_2 to the poly-Si interface and release H_2 from the materials. The flowchart for this process is shown in figure.3.6.

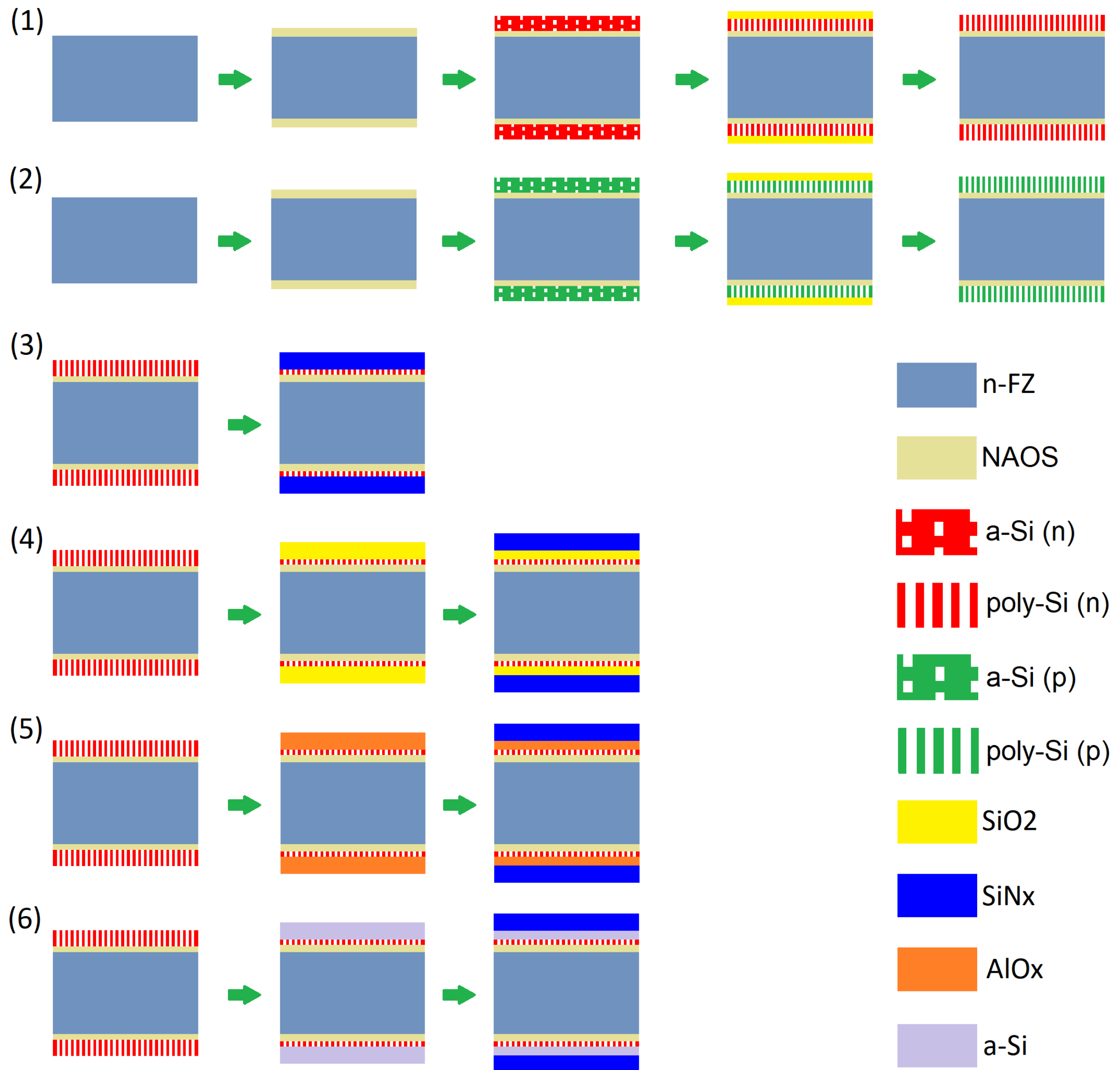

Figure 3.6: Sample for hydrogenation samples. All samples started from n-type floatzone <100> wafers with 1.4 [nm] NAOS oxide and 250 [nm] a-Si:H from LPCVD at 580 [^{o}C].(1) n-type poly-Si sample: Wafers ion implanted with P at dose 6e15 [ionscm^{-2}] to become n-type a-Si:H. Annealing at 950 [^{o}C] for 3 [min] forms n-poly-Si. Annealing causes the formation of native oxide which is removed using HF 0.55 [%]. (2) Fabrication of p-type poly-Si sample: all steps the same as (1) but with B implantation at a dose of 5e15 [ionscm^{-2}] to form the p-type poly-Si layers. (3) n-type SiN$_x$:H sample: 75 [nm] SiN$_x$:H deposited using PECVD at 400 [^{o}C]. (4) n-type SiO$_2$/SiN$_x$:H sample: 100 [nm] SiO$_2$ and 75 [nm] SiN$_x$:H deposited using PECVD at 300 and 400 [^{o}C] respectively. (5) n-type AlO$_x$:H/SiN$_x$:H sample: 20 [nm] SiO$_2$ and 75 [nm] SiN$_x$:H deposited using ALD at 300 [^{o}C] and PECVD at 400 [^{o}C] respectively. (4) n-type a-Si:H/SiN$_x$:H sample:6 [nm] SiO$_2$ and 75 [nm] SiN$_x$:H deposited using PECVD at 250 and 400 [^{o}C] respectively. The same deposition process was also used to fabricate the p-type samples.

3.2.3. P-type and n-type hydrogenation

In this section the results of the hydrogenation tests are presented.

Starting with SiN$_x$:H, as expected this layer performs much better on the n-type BSF. Here there is an iV_{oc} of 710 [mV] and a J_0 of 18.6 [fAcm^{-2}]. This is considerably better than the 686 [mV] and 49.3 [fAcm^{-2}] achieved on the p-type emitter. This is due to the detrimental field effect caused by the positive corona charges within the SiN$_x$:H. And also the properites

Table 3.2: Hydrogenation materials and layer thicknesses for p-type and n-type symmetrical tests

Doping	1	Thickness [nm]	Material 2	Thickness [nm]
p-type	SiN_x:H	75	-	-
p-type	SiO_2	100	SiN_x:H	75
p-type	AlO_x:H	20	SiN_x:H	75
p-type	a-Si:H	6	SiN_x:H	75
n-type	SiN_x:H	75	-	-
n-type	SiO_2	100	SiN_x:H	75
n-type	AlO_x:H	20	SiN_x:H	75
n-type	a-Si:H	6	SiN_x:H	75

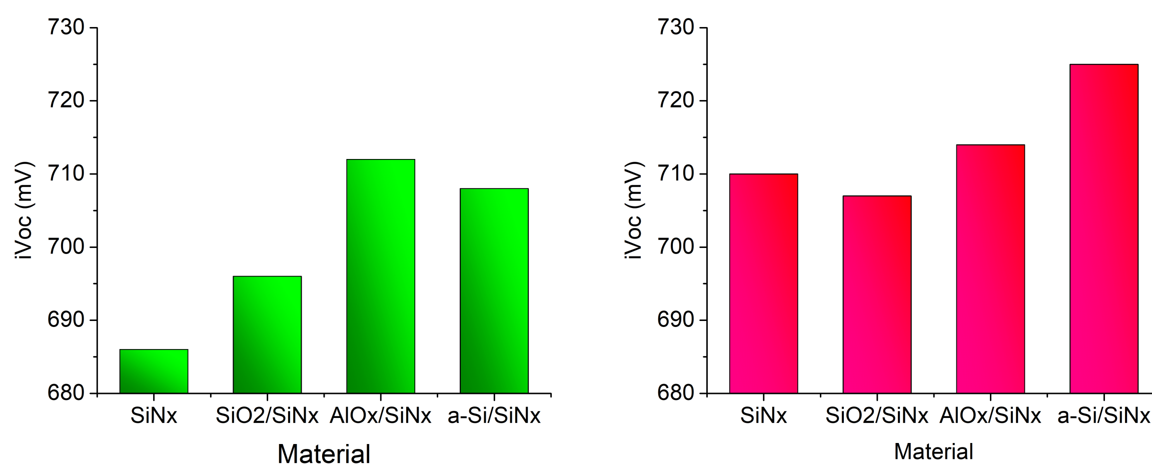

Figure 3.7: Hydrogenation quality of different material stacks on emitter and BSF layers. Left: Effect of hydrogenation of the p-type poly-Si on its passivation of the c-Si interface. Right: Effect of hydrogenation of the n-type poly-Si on its passivation of the c-Si interface.

of p-type poly-Si materials which are much more defective [41]. The number of holes is thus reduced in the p-type layer decreasing the likelihood of collection. The same effect obviously helps achieve better results on the n-type poly-Si by aiding the collection of electrons.

The SiO_2/SiN_x:H stack shows slightly better results on p-type with 696 [mV] and 29.4 [fAcm^{-2}], and slightly worse on n-type with 707 [mV] and 20.5 [fAcm^{-2}], as compared with the SiN_x:H samples. The drop on the p-type poly-Si can again be attributed to positive fixed charge density. However, this is less pronounced due to the weaker field effect compared with SiN_x:H. For the n-type sample, the combination of field effect and hydrogen passivation does lead to reasonable results, but this is not enough for really excellent performance.

Looking at the AlO_x:H/SiN_x:H samples very good values can be seen for both tests. The n-type values of 714 [mV] and 10.4 [fAcm^{-2}] are both higher than the previous material stacks. The same is true for the p-type wafer which has values of 712 [mV] and 15.4 [fAcm^{-2}]. As in the front surface passivation tests, the AlO_x:H layer is able to effectively hydrogenate the n-type layer due to its H_2 content. It is actually more effective than the hydrogenation of the p-

type poly-Si. The field effect from the n-type layer, combined with the small SiO_x layer formed during the AlO_x:H deposition [78], is able to mitigate the effect of the negative corona charges in the AlO_x:H. Again, the stronger n-type performance is also in part due to the inferior quality of the p-type poly-Si.

Lastly the a-Si:H layer shows excellent hydrogenation passivation on the n-type layer with an iV_{oc} of 725 [mV] and J_0 of 6.9 [fAcm^{-2}]. It also well hydrogenates the p-type layer achieving 708 [mV] and 37.5 [fAcm^{-2}]. This is owing to the high H_2 content in this layer and the lack of a detrimental field effect. However, the lack of the positive corona charges means it is less effective than the AlO_x:H layer.

Regarding the hydrogenation of the poly-Si IBCs, the a-Si:H/SiN_x:H layer was determined to be the best for this purpose. This is due to the excellent performance on the n-type BSF samples, achieving an iV_{oc} of 725 [mV]. And also the strong performance on the p-type emitter, achieving an iV_{oc} of 708 [mV].

3.3. Conclusion

In this chapter options for the front surface passivation and field were explored. Four material stacks were investigated: SiO_x/SiN_x:H, SiO_x/AlO_x:H/SiN_x:H, AlO_x:H/SiN_x:H and a-Si:H/SiN_x:H. In the first stage of experimentation samples were tested on undoped symmetrical samples. Both the AlO_x:H/SiN_x:H and a-Si:H/SiN_x:H highlighted themselves as strong candidates for passivation with iV_{oc} values of 724 and 731 [mV]. The AlO_x:H/SiN_x:H stack was of particular interest considering its optical transparency within the c-Si absorption range. Unfortunately this research could not be pursued due to the loss of the machine, so instead the a-Si:H/SiN_x:H stack was chosen. This layer had a-Si:H and SiN_x:H thicknesses of 18 and 75 [nm] respectively.

This was then applied to wafers with varying dopant doses for the front surface field. Namely; no FSF, 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}]. These equate to doping concentrations at a depth of 10 [nm] of 0, 2e19, 4e19, 7e19 and 1e20 [atoms-cm^{-3}] respectively. The thickness of the a-Si:H was also reduced to minimise parasitic absorption. Thicknesses of 4.5, 9, 13.5 and 18 [nm] were chosen. These tests highlighted that the No FSF case was the best performer but also that the 6e14 case was also a strong candidate. These layers achieved 730 and 720 [mV] with the 18 [nm] a-Si:H layer. Moving forward it was determined that a thickness of 9 [nm] would be best for the poly-Si IBCs. This is lower than the 22 [nm] value used in [40] for the previous device, so will exhibit less parasitic absorption, but still thick enough to provide effective passivation. This will be implemented on each of the FSF field doping doses: 0e14 (No FSF), 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}] leading to 5 poly-Si IBCs.

Next the rear hydrogenation for the poly-Si IBC cells was optimised. Again 4 material stacks were investigated: SiN_x:H, SiO_x/SiN_x:H, AlO_x:H/SiN_x:H and a-Si:H/SiN_x:H. These were deposited on n- and p-type poly-Si samples with the same doping concentrations as the BSF and emitter in the IBCs. For each of the samples FGA was applied at a temperature of 400 [^{o}C] for 30 [min].

Comparing the quality of the different materials it was clear that the AlO_x:H/SiN_x:H and a-Si:H/SiN_x:H again samples showed the most promising results. The AlO_x:H/SiN_x:H samples obtained 714 [mV] and 712 [mV] on the n- and p-type poly-Si respectively. The a-Si:H/SiN_x:H

achieved 725 [mV] on the n-type poly-Si and 708 [mV] on the p-type poly-Si. Despite the performance on p-type being slightly less than the AlO_x:H/SiN_x:H layer this was determined to be the strongest candidate for rear hydrogenation. Going forward it was thus decided that the a-Si:H/SiN_x:H stack would be implemented into the IBCs to hydrogenate the poly-Si BSF and emitter.

4

Interdigitated back contacted solar cells

In this chapter the front surface (FS) passivation and rear hydrogenation processes optimised in Chapter.3 are implemented into poly-Si IBC solar cells. The chapter begins with a discussion of the key parameters within the design, and continues with the methods of fabrication. Next, an analysis of the performance of the cells is made. Finally, the chapter ends with a summary of the findings and recommendations for further work.

After the investigation of the FS passivation it was found that the a-Si:H/SiN_x:H stack was the highest performing structure. The thickness of these layers was 9 and 75 [nm] respectively. For the front surface field (FSF) doping it was found that the case with no doping, No FSF, had the highest performance. Despite this, it was decided to investigate a range of different doping levels to see if the same trend would be visible. As such devices with dopant doses of No FSF, 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}] were developed. At the rear of the device the optimal hydrogenation came again from the a-Si:H/SiN_x:H stack. In this case the layer thicknesses were 6 and 75 [nm] respectively. The fabrication process for these solar cells is outlined below. The IBC cell design is shown in figure.4.1.

4.1. Fabrication

Starting from n-type $<100>$ oriented wafers first a standard cleaning step was performed. This was followed by immersion in 0.55 [%] HF for 4 [min] to remove any native oxide. After this the tunnel oxide layer was grown via wet chemical oxidation in 69.5 [%] HNO_3 for 60 [min]. This led to a SiO_x layer of 1.4 [nm] on both sides of the wafer [48][80]. A 250 [nm] a-Si deposition was made on both sides using an LPCVD furnace at 580 [^{o}C]. Photolithography was then used on the rear of the cell to define the emitter and back surface field (BSF) areas before ion implantation. The emitter/BSF ratio was 60:40. For the BSF the Phosphorous (P) dopants were used at a dose of 6e15 [ions-cm^{-2}] and an ion energy of 20 [keV]. For the emitter the dopant atom was Boron (B) with a dose of 5e15 [ions-cm^{-2}] and an ion energy of 5 [keV]. Standard cleaning was performed after each implantation to remove any unwanted particles.

Next, the rear of the device was protected so that the FS could be textured. A 500 [nm] SiN_x deposition was made as a capping layer using PECVD at 400 [^{o}C]. Texturing of the FS was done using TMAH solution at 80 [^{o}C] and 300 [RPM] for approximately 10 [min]. This leads to a $<111>$ oriented surface. An etching step was made on the rear to isolate the emitter and

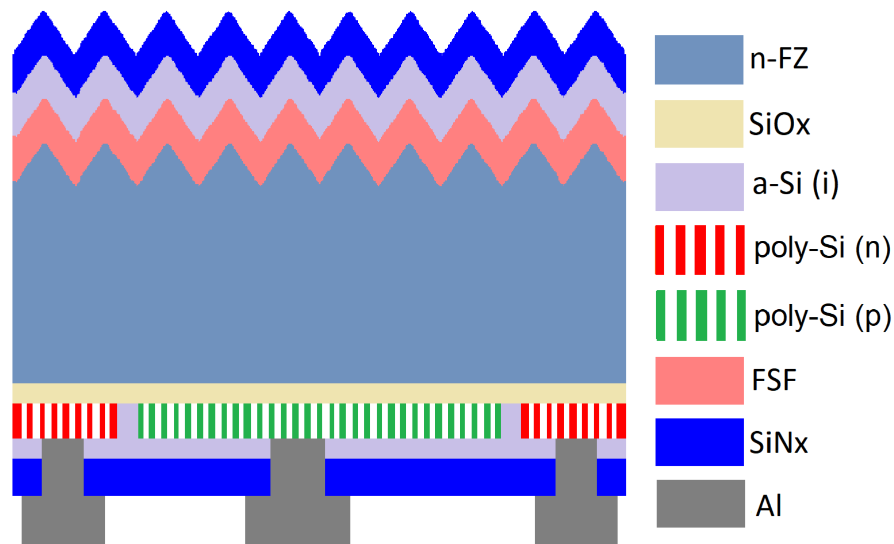

Figure 4.1: Poly-Si IBC solar cell architecture. n-type bulk c-Si with 1.4 [nm] NAOS tunnel oxide, 250 [nm] doped emitter and BSF regions on rear of ratio 60:40. FS passivation stack a-Si:H/SiN$_x$:H of 9 and 75 [nm] respectively. Rear hydrogenation stack a-Si:H/SiN$_x$:H of 6 and 75 [nm] respectively. Al metal contacts 2 [μm].

BSF areas, removing a possible shunt path. Photolithography was used to define the isolation regions before the SiN$_x$/a-Si layers were etched. This was performed using dry-etching with plasma. After this step, the remaining SiN$_x$ was removed from the rear using BHF 1:7 solution for 26 [min]. Ion implantation using P dopants with an ion energy of 10 [keV] was performed on the FS to form the FSF. The doses were 0 (No FSF), 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}]. These equate to doping concentrations at a depth of 10 [nm] of 0, 2e19, 4e19, 7e19 and 1e20 [atoms-cm^{-3}] respectively. Standard cleaning was again performed. To activate and drive in the dopants a high temperature annealing was performed at 950 [^{o}C] in an O_2 atmosphere for 3 [min]. This leads to the growth of a thin SiO$_x$ layer which was subsequently removed via immersion in HF 0.55 [%] for 4 [min].

With the poly-Si passivating contacts fabricated, the rear hydrogenation was applied. This was a-Si:H/SiN$_x$:H of 6 and 75 [nm] respectively. The a-Si:H layer was deposited using PECVD at 250 [^oC]. The SiN$_x$:H layer was deposited using PECVD at 400 [^oC]. FGA was then applied at 400 [^oC] for 30 [min]. This furnace had a 10 [%] H_2 in N_2 ratio. Standard cleaning was then performed, followed by another 0.55 [%] HF dip for 4 [min]. This HF dip slightly etches the rear SiN$_x$:H to <40 [nm]. Next, the a-Si:H/SiN$_x$:H for the FS passivation was applied. These layers were 9 and 75 [nm] respectively and used the same PECVD parameters as the rear hydrogenation.

At the rear of the device the SiN$_x$:H layer was opened so the metal could make direct contact with the poly-Si layers. Photolithography was used to define the contact opening pattern and BHF 1:7 was used for 2 [min] to etch the SiN$_x$:H. Standard cleaning was then performed to remove any unwanted particles from this process. Photolithography is again used to define the metalisation before its deposition via metal evaporation. The material for this step was Al and a thickness of 2 [μm] was used. The unwanted Al material was removed in a lift-off using acetone. A final post-metalisation FGA step was made for the Al to break through the a-Si:H and contact the poly-Si layers. This was done at temperatures ranging from 300-400 [^oC] for different time intervals. The flowchart for this process is shown in figure.4.2.

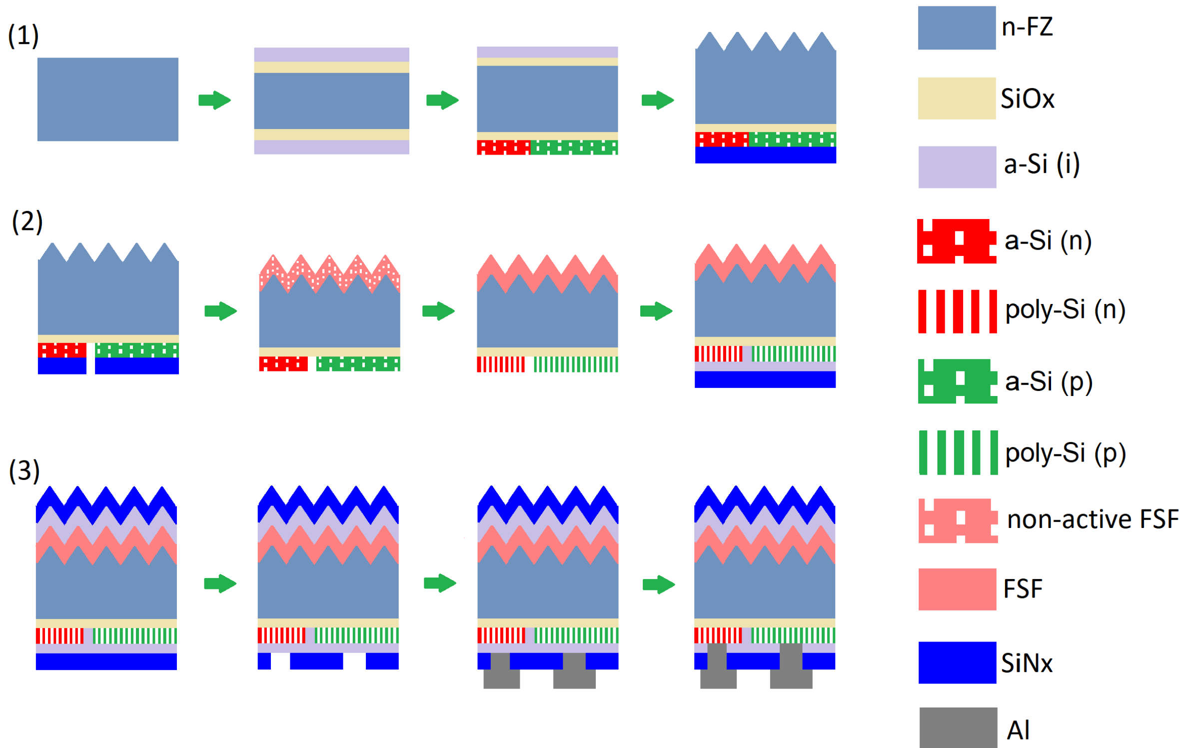

Figure 4.2: IBC fabrication process. n-type <100> oriented wafers used. (1) 1.4 [nm] NAOS oxide grown from 69.5 [%] HNO_3 for 60 [min] and 250 [nm] a-Si deposition from LPCVD. Ion-implantation of emitter/BSF regions on device rear. 500 [nm] SiN_x capping layer on rear, whilst front surface (FS) is textured using TMAH solution for 10 [min]. (2) Etching gap between emitter/BSF regions to remove shunt path. Ion implantation of FSF. Annealing at 950 [^{o}C] to form poly-Si layers and activate/drive in dopants. Application of rear hydrogenation a-Si:H/SiN_x:H stack of 6 and 75 [nm] respectively. Deposited using PECVD at 250 and 400 [^{o}C] respectively. (3) Application of FS passivation a-Si:H/SiN_x:H stack of 9 and 75 [nm] respectively. Deposited using PECVD at 250 and 400 [^{o}C] respectively. Etching contact openings for metallisation. Application of Al contacts via metal evaporation. FGA step to break Al contacts through a-Si:H layer.

4.2. Results

In this section the results of the poly-Si IBC cells are discussed. Unfortunately the cell fabrication was unsuccessful and the post-metalisation annealing step was unable to make good contact with the poly-Si layers. As such, only the cell with the 2e14 [ions-cm^{-2}] FSF is presented here to illustrate the results. An analysis is made of the effect of the different annealing times and temperatures for the post-metalisation step. Each of the measured cells had an area of 2 [cm^2]. The results after the final forming gas annealing step are shown table.4.1.

The results in table.4.1 show that after annealing at 350 [^oC] for 20 [s] the current density is high but the V_{oc} is quite low. These show 32.2 [mA-cm^{-2}] and 100 [mV] respectively. The fact that there is current flow shows that the device is not shunted which is also seen in the high R_{shunt} value of 370 [$k\Omega$] [81][82][83]. The performance is limited by the metal/a-Si:H interface which will have recombination.

For the longer annealing at the higher temperature of 400 [^oC] this relationship is reversed. In these cases, the metal is indeed breaking through the a-Si:H layer, but this is in fact leading to a more severe shunt path in the device. As seen from the very low R_{shunt} values. This was likely due to the reduced thickness of the SiN_x:H layer in the HF step after hydrogenation. HF etches non-uniformly and so will have led to some very thin areas of SiN_x:H and others where

Table 4.1: Performance of poly-Si IBC solar cells after different post-metalisation annealing times and temperatures

Temperature .[^oC]	Time [s]	V_{oc} [mV]	J_{sc} [mAcm^{-2}]	FF [%]	η [%]	R_{shunt} [Ω]
350	10	100	32.2	98.5	3.17	37e4
350	20	368	2.8	27.0	0.28	150
400	30	588	11.4	47.3	0.07	110
400	60	596	6.9	38.8	1.59	70
400	90	559	9.1	47.5	2.42	90
400	120	609	18.0	65.9	7.22	180
400	150	290	3.2	28.4	0.26	40

it was completely removed. These thin or non-existent layers would provide poor isolation of the emitter BSF regions during the post-metalisation step. The metal was then able to contact both the emitter and BSF regions destroying the performance of the device. This effect is shown in (c) of figure.4.3. In the ideal case shown in (b), the SiN$_x$:H layer is thick enough to hold back the metal during this step.

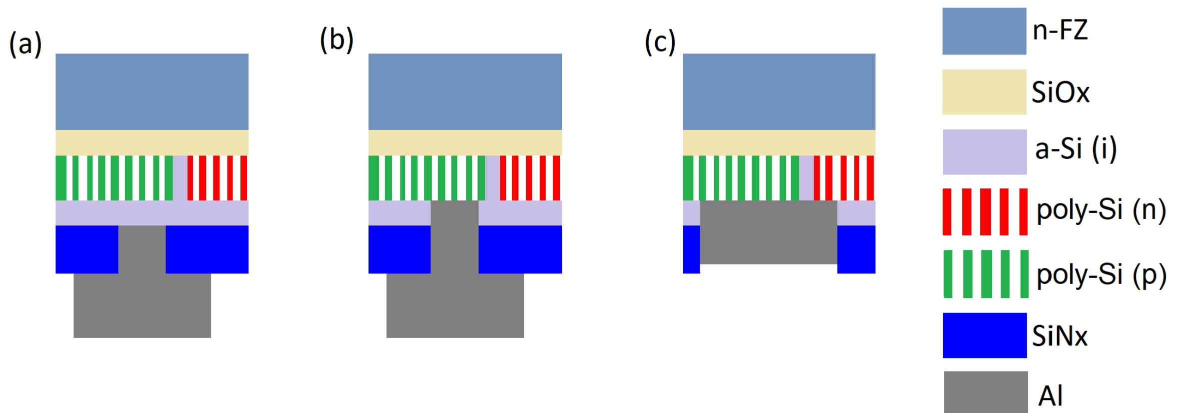

Figure 4.3: Post-metalisation annealing. (a) Schematic of cell before post-metalisation annealing shows a-Si:H present between Al contact and p-poly-Si emitter layer. (b) Successful breakthrough of Al contact after post-metalisation annealing. Al directly contacts emitter with no pathway for shunting. (c) Unsuccessful breakthrough of metal contact after annealing. Al contacts both emitter and BSF (n-poly-Si) regions providing a shunt path in the cell.

The efficiency, η, for each of the cells is also incredibly poor. The best value comes from the 400 [^oC] cells after 120 [s] annealing with a V_{oc} of 609 [mV] and η of 7.22 [%]. This appears to be the optimal condition in order to break through a-Si:H layer, but needs a thicker SiN$_x$:H layer to avoid shunting. For the longer annealing time of 150 [s] there is saturation.

4.3. Conclusion

Unfortunately the fabrication process of the IBCs was unsuccessful and did not lead to any good performing solar cells. The best condition came after a post-metalisation annealing at 400 [^oC] for 120 [s]. This led to a V_{oc} of 609 [mV] and an efficiency of 7.22 [%].

The poor quality of these cells can be attributed to the SiN_x:H layer on the rear of the device being too thin. The HF dip before the front surface passivation was applied etched this layer to a thickness of <40 [nm]. The non-uniform etch rate will also have caused some areas to have little to no SiN_x. This was therefore unable to sustain to the post-metalisation step for the Al contacts and so the both the emitter and BSF were connected. The resulting shunt path destroyed the performance of the cells. In future work a thicker SiN_x:H layer should implemented in order to withstand this process.

5 PECVD Tunnel oxide for FBC cells

In this chapter a new approach for the formation of the tunnel oxide is presented. Instead of using wet chemical oxidation, plasma enhanced chemical vapor deposition (PECVD) is used. The chapter begins with a description of the oxidation process and the thicknesses obtained for different reaction times. Next, measurements of the passivation quality for each of the thicknesses are made on n-type flat symmetrical samples. From this 3 oxides are selected to be used in further configurations. These include; p-type flat and n-type textured symmetrical samples, n-type flat/p-type flat asymmetrical samples, and n-type textured/p-type flat asymmetrical samples. The chapter concludes with the selection of the best oxide layer for implementation into front back contacted (FBC) cells.

The motivation for this research is to achieve better performance from the tunnel oxide layer in the IBC cells. After the current NAOS layer is implemented, the next step is the deposition of a thick a-Si layer via LPCVD. Unfortunately there is unavoidable contamination associated with the transport of the wafers between these two processes. Growing this layer via PECVD eliminates this problem as it can be immediately capped with a-SiO$_x$ without breaking the vacuum [79]. Furthermore, using PECVD allows much greater control over the thickness and stoichiometry of the tunnel oxide as compared with wet chemistry. Thirdly, the PECVD process forms a poly-SiO$_x$ passivating contact as opposed to the current poly-Si layer. This has the advantage of lower parasitic absorption [79].

5.1. Developing the PECVD oxide layer

Similar to the formation of the tunnel oxide via NAOS, when using PECVD to form the oxide layer it is a reaction and not a deposition. This means that the c-Si bulk is being consumed to form SiO$_x$ [44]. Within the PECVD chamber it is an N_2O plasma that reacts with the silicon surface to create the tunnel oxide layer. Following from the work of S. Sandeep [84] it is evident that the important parameters are the time of exposure to the plasma, which dictates the layer thickness and stoichiometry, and the mixture of gases, which also affects the layer stoichiometry. In [84] both N_2O and N_2O + Ar plasmas are investigated as shown in figure.5.1.

5.2. Measuring layer thickness

When forming a tunnel oxide the normalised thickness is 1.5 [nm] [46][40][44]. In figure.5.1 it can be seen that for a reaction time of 5 [min], an oxide thickness of 2.3 [nm] is obtained. In

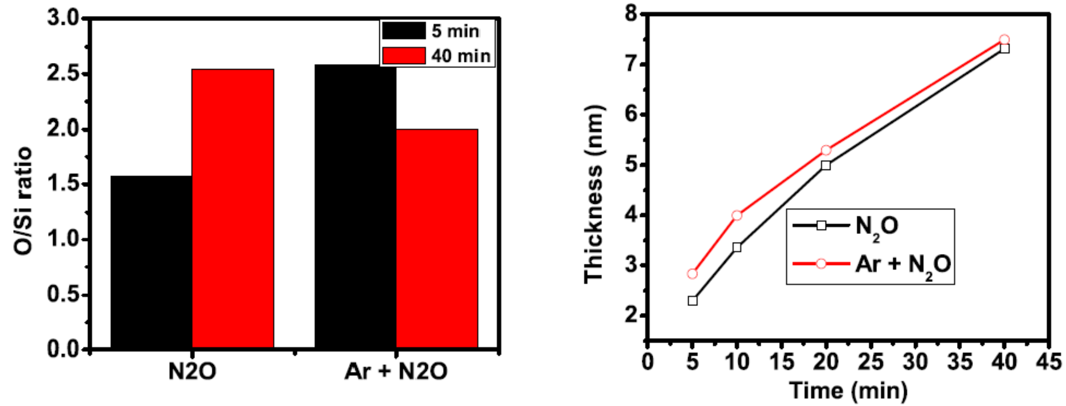

Figure 5.1: Left: Stoichiometry of layer formed is affected by time exposed to plasma as well as mixture of gases. Right: Layer thickness is related to time exposed to plasma [84].

an attempt to reach a value of 1.5 [nm] reaction times of 3, 6, 9, 12, 15, 18 and 21 [min] were measured.

Layers were grown on <100> n-type floatzone (FZ) wafers after a 4 [min] HF 0.55 [%] dip to remove the native oxide. The wafers were then placed in a PECVD tool for oxide growth at 300 [^{o}C]. The N_2O flow rate for reactions was 71 [sccm]. No other gases were used. The RF power was 5 [W] and the pressure 1.33 [mbar], as in [84]. The load and tune were 17 and 15. The plasma oxide thicknesses were then measured using ellipsometry and the results of this are shown in figure.5.2.

Figure.5.2 shows a clear correlation between reaction time and plasma oxide thickness. The 9 [min] oxide comes closest to the NAOS layer with a value of 1.46 [nm]. The graph also shows the presence of two different reaction rates. The initial rate from 3-12 [min] follows an exponential trend. Beyond this point the growth saturates. Here already the formed oxide is covering the c-Si bulk, making it harder for the reaction to continue.

With the layer thicknesses determined, the passivation quality can be compared with the NAOS layer. The preparation of samples for these tests is described in the next section.

5.3. Sample preparation

To test the passivation quality of the plasma oxides, symmetrical test samples were prepared with poly-SiO_x passivating contacts. Three strucures were investigated; n-type flat, p-type flat and n-type textured, as shown in figure.5.3. This was done to understand the performance of this layer in an IBC, where there are both p- and n-type flat layers, and also for FBCs, where there is a p-type flat layer at the rear, and an n-type textured layer at the front, figure.5.3. Finally, to further inform these combinations, n-type flat/p-type flat and n-type textured/p-type flat asymmetrical samples were prepared.

Starting from a polished <100> oriented c-Si wafer, first the plasma oxide was formed using PECVD at 300 [^{o}C]. Next a 10 [nm] intrinsic a-SiO_x layer was added followed by an n-type a-SiO_x layer of 20 [nm] using the same PECVD tool. The deposition parameters for these layers is outlined in detail in Chapter.2. All three layers were deposited on both sides, thus creating

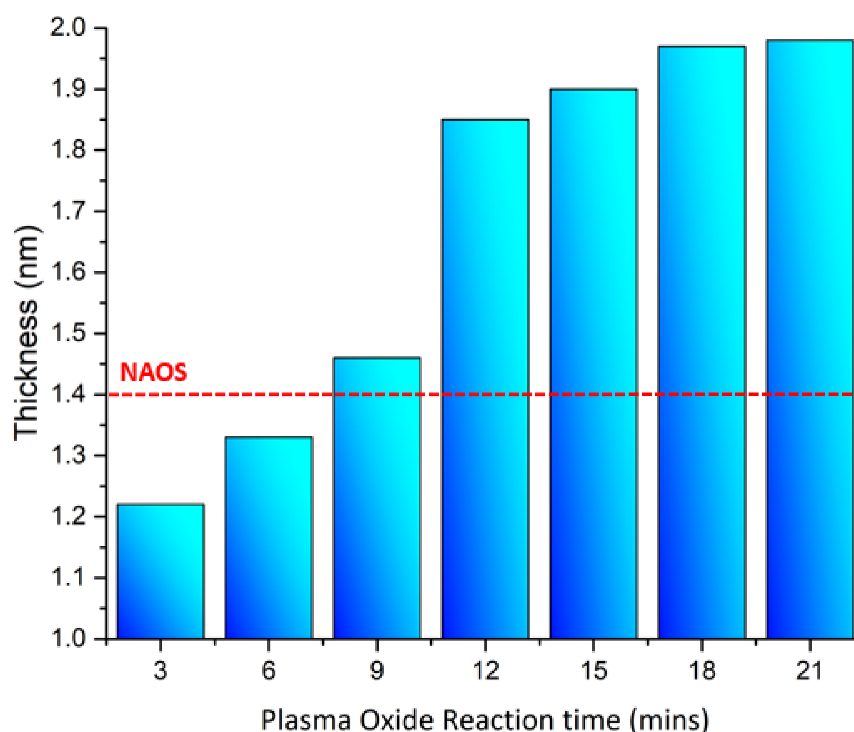

Figure 5.2: Thickness of PECVD tunnel oxide layer with increasing reaction time. Dotted line shows the of 1.4 [nm] thickness from the former NAOS oxide [80]

the symmetrical sample. Samples were prepared with each of the plasma oxide thicknesses mentioned above: 3, 6, 9, 12, 15, 18 and 21 [min]. After these depositions samples were annealed at 850 [^{o}C] to crystallise the a-SiO$_x$ into poly-SiO$_x$, completing the poly-SiO$_x$/plasma oxide passivating contact. Different annealing times were performed in search of the optimal condition. First times of 10, 45 and 60 [min] were tested. Finally a sample with an annealing time of 90 [min] was also measured. The samples were then deposited with 75 [nm] of SiN$_x$:H and subjected to a 30 [min] forming gas annealing at 400 [^{o}C]. In this furnace a ratio of 10 [%] H_2 in N_2 was used. The SiN$_x$:H layer was deposited using PECVD at 400 [^{o}C]. Measurements of the passivation quality were taken before and after this SiN$_x$:H/hydrogenation step. The flowchart for the process is shown in figure.5.3.

For the n-type textured wafers, the same procedure was followed except that at the start of the process textured <111> oriented wafers were used. For the p-type flat samples, the intrinsic layer remained 10 [nm] and a 10 [nm] p-type layer was used in place of the n-type layer. Finally, for the asymmetrical samples, the same procedure was followed but with one side n- and another p-type for the flat/flat samples, and one side n-type textured and the other p-type flat for the flat/textured samples.

5.4. n-type flat

In this section the results are given for the n-type flat samples. First a discussion of the results before hydrogenation is given. A discussion is then made for the results after this step is applied. At the end of the section the 3 most promising n-polySiOx/plasma oxide layers are selected for testing with the remaining configurations.

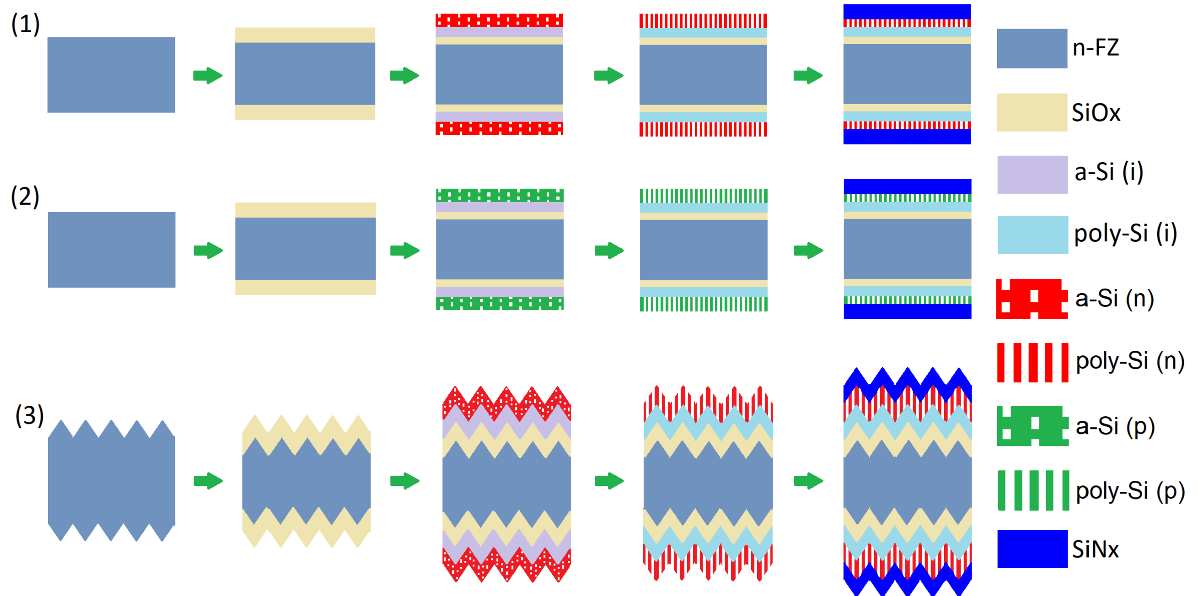

Figure 5.3: Flowchart showing preparation of symmetrical samples for measurement of poly-SiO$_x$/plasma oxide passivation quality. (1) n-type flat: Starting from <100> oriented floatzone wafers first the tunnel oxide is grown. This is done via a c-Si reaction with N_2O plasma using PECVD at 300 [^{o}C]. Next, the i- and n-type a-SiO$_x$ layers are added using the same PECVD tool. These layers are 10 and 20 [nm] respectively. Annealing causes the crystallisation of the a-SiO$_x$ layers into poly-SiO$_x$. 75 [nm] SiN$_x$:H is added using PECVD at 400 [^{o}C]. Finally, hydrogenation is performed at 400 [^{o}C] in an FGA furnace for 30 [min]. (2) p-type flat: this follows the same process as the n-type flat samples except that a p-type a-SiO$_x$ layer is now deposited instead of the n-type. This layer is 10 [nm]. (3) n-type textured: this follows the same procedure as the n-type flat samples, but now the layers are deposited on a <111> oriented textured surface.

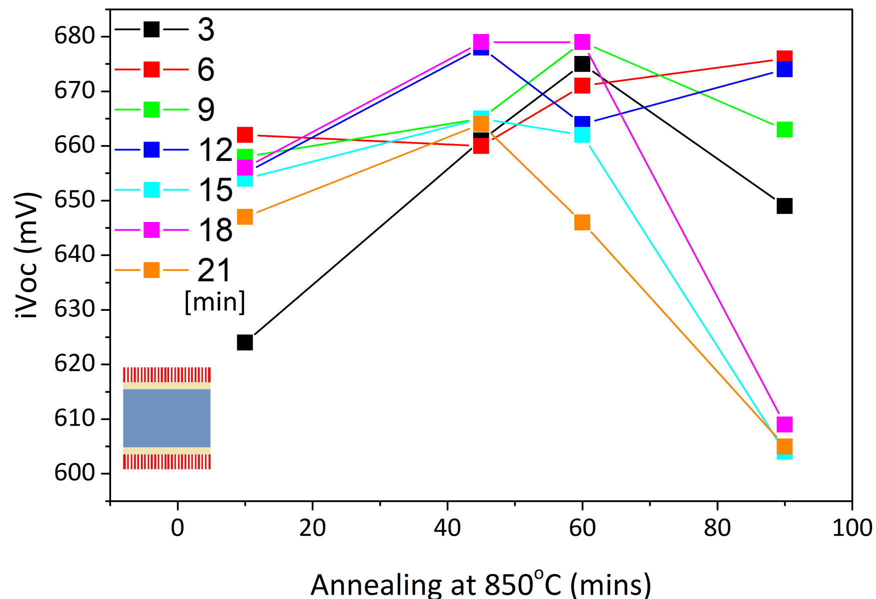

Figure 5.4: Passivation quality of n-poly-SiOx/plasma oxide passivating contacts on n-type flat symmetrical samples. Samples annealed for different times at 850 [^{o}C]. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

In figure.5.4 the results of the passivation tests after annealing are shown. As mentioned in section.1.7.2, the annealing time affects the doping profile which creates the field effect passivation in the n-poly-SiO$_x$/plasma oxide layer. It also affects the integrity of the plasma oxide layer by forming pinholes which aid the tunneling of charge carriers. In the extreme case it can lead to the breakdown of the tunnel oxide layer.

Analysing the results shows that the 10 [min] annealing time is too short for the development of this layer. After this time the n-a-SiO$_x$ has not fully crystallised and the doping profile has not been correctly developed. Conversely, 90 [min] is too long for many of the samples, and results in the lowest values. The doping profile is again not well developed. The best results come after 45 and 60 [min], indicating the presence of the optimum. The maximum value is 679 [mV] which is achieved by the samples using plasma oxide 9, after 60 [min] annealing, and oxide 18 after 45 and 60 [min]. The J_0 values for these samples are 23, 26.8 and 25 [fAcm^{-2}] respectively.

Analysing the sheet resistance of the oxide 18 samples gives insight into what is happening with this layer. After 10 [min] the value is 101 [Ω-sq^{-1}]. This increases to 103 [Ω-sq^{-1}] after 45 [min], but again decreases to 101 [Ω-sq^{-1}] after 60 [min]. After 90 [min] this jumps up to 105 [Ω-sq^{-1}]. For this oxide the n-poly-SiO$_x$ crystallisation appears to happen quite quickly as the variation in the sheet resistance is small. The variation in performance must therefore come mainly from changes in the dopant diffusion. Above 60 [min] annealing the P atoms in the n-type poly-SiO$_x$/plasma oxide have diffused to form a less favourable doping profile. The samples using oxides 15 and 21 show the same dramatic drop. It appears that layers with a thickness above 1.9 [nm] are too thick for the diffusion of P-dopants. The build up of these dopants at the n-poly-SiO$_x$/plasma oxide interface leads to poorer field effect passivation. Some diffusion into the c-Si bulk is needed to create the right field effect for the selection of charge carriers [44].

In contrast, plasma oxide 3 represents the lower bound for performance. This oxide had a thickness of 1.22 [nm]. This is too thin to provide an effective barrier for the dopants and so too many are entering c-Si bulk. Analysing the sheet resistance of this sample shows that it is decreasing with longer annealing. After 10 [min] the value is 145 [Ω-sq^{-1}], while after 45 and 60 [min] this drops to 140 [Ω-sq^{-1}]. After 90 [min] the sheet resistance again drops to 130 [Ω-sq^{-1}] indicating the formation of pinholes in the plasma oxide. The optimum is found at 60 [min]. Here the doping profile has developed such that the best field effect passivation is seen.

In figure.5.5 the results after SiN$_x$:H and hydrogenation are shown. A greater variation in performance is now seen. The sample using oxide 18 remains the best performer and achieves a passivation quality of 723 [mV] and 4.9 [fAcm^{-2}] after 45 [min] annealing. This is close to the optimum value for NAOS which was 727 [mV] after 30 [min] at 850 [^{o}C] [80]. The samples with this oxide are relatively stable across all annealing times. The hydrogenation step has succesfully added H_2 to the lattice which has improved the passivation of the interfaces, raising them all to a similar quality.

The thickness of this layer was 1.97 [nm] which is equivalent to the thickness of oxide 21 (1.98 [nm]). By contrast the samples using oxide 21 have much lower passivation quality. The longer N_2O reaction time leads to an increased plasma oxide density that is hindering the performance [84]. This is likely due to a greater build of P-dopants at this interface and thus a poorer field effect from n-poly-SiO$_x$/plasma oxide passivating contact. Longer annealing only

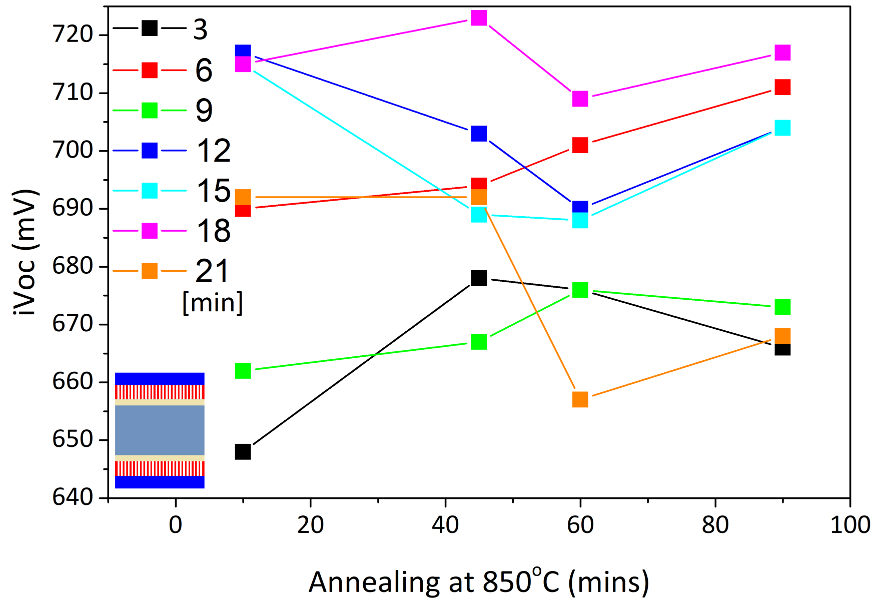

Figure 5.5: Passivation quality of n-poly-SiOx/plasma oxide passivating contacts on n-type flat symmetrical samples. Samples annealed for different times at 850 [^{o}C] and then subjected to hydrogenation. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

adds to this process as more dopants are concentrated at this point. The hydrogenation does raise the quality of the samples, but it is limited by this effect.

The samples with oxides 6 and 12 also show high values of 711 and 717 [mV] and 6.5 and 4.1 [fAcm^{-2}] respectively. These are both quite stable across different annealing times but not to the same degree as the samples using oxide 18. As these 3 oxides showed the best results they were selected for the subsequent tests.

5.5. p-type flat

In this section the results are shown for the p-type flat symmetrical samples. First the results before the hydrogenation step are discussed. Then the results after this step was performed.

Figure.5.6 shows the results of the different annealing times for the p-poly-SiOx/plasma oxide samples with 6, 12 and 18 [min] oxides. The maximum is achieved with oxide 6 after 90 [min] annealing. This gives an iV_{oc} of 638 [mV] and J_0 of 100 [fAcm^{-2}]. This is much poorer than the value obtained on the n-type flat samples. The sheet resistance was fairly constant for each of the samples, ranging from around 104-106 [Ω-sq^{-1}], showing that the integrity of the layer is preserved [80]. The difference in quality can then be attributed to the diffusion of the B dopants. These are smaller than the P atoms used for the n-type layer and so can penetrate the plasma oxide creating defects in the c-Si bulk. This will lower the overall performance and cause the larger J_0 value.

There is a correlation seen between annealing time and passivation quality. Especially for the samples using oxides 6 and 12. Longer annealing leads to a more favourable doping profile which aids the passivation. This effect saturates for the samples with oxide 18 after 45 [min]

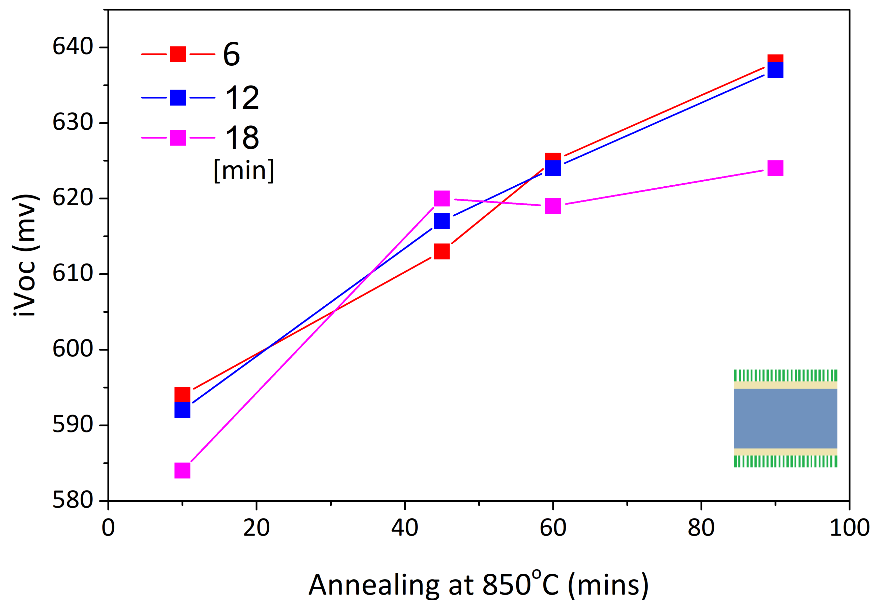

Figure 5.6: Passivation quality of p-poly-SiOx/plasma oxide passivating contacts on p-type flat symmetrical samples. Samples annealed for different times at 850 [^{o}C]. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

annealing. As in the n-type flat samples, the comparative thickness of this layer will make it harder for dopants to diffuse so after the initial crystallisation of the p-poly-SiOx layer, little improvement in the passivation is seen.

In the work of [80], p-poly-SiO$_x$ passivating contacts using the NAOS oxide obtained an iV_{oc} of 679 [mV] and a J_0 of 29 [fAcm^{-2}]. This was after 60 [min] annealing at 850 [^{o}C]. This is far superior to the results achieved here. The tunnel oxide layer grown using wet chemical oxidation obviously creates a more effective doping profile compared with this PECVD oxide.

In figure.5.7 the effect of hydrogenation can be seen. The best value is now on the p-poly-SiOx/plasma oxide passivating contact using oxide 12. This achieves an iV_{oc} of 668 [mV] and a J_0 of 28 [fAcm^{-2}] after 90 [min] annealing. This is again much lower than the value obtained for NAOS which was of 709 [mV] and 13.9 [fAcm^{-2}]. The hydrogenation has improved results, but these are still hindered by the doping profile. The hydrogenation step has also had a large impact on the J_0 values. This indicates that the p-poly-SiOx/plasma oxide was also not chemically passivating the c-Si interface well.

5.6. n-type textured

In this section the results of the tests on n-type textured samples are presented. First the results before the SiN$_x$ and hydrogenation step are presented. Then the results after this step was performed.

The results of the different annealing conditions are shown in figure.5.8. The best passivation comes from the n-poly-SiOx/plasma oxide sample with oxide 18. After 30 [min] annealing this shows an iV_{oc} of 643 [mV] and a J_0 of 133 [fAcm^{-2}]. This is slightly higher than the optimal

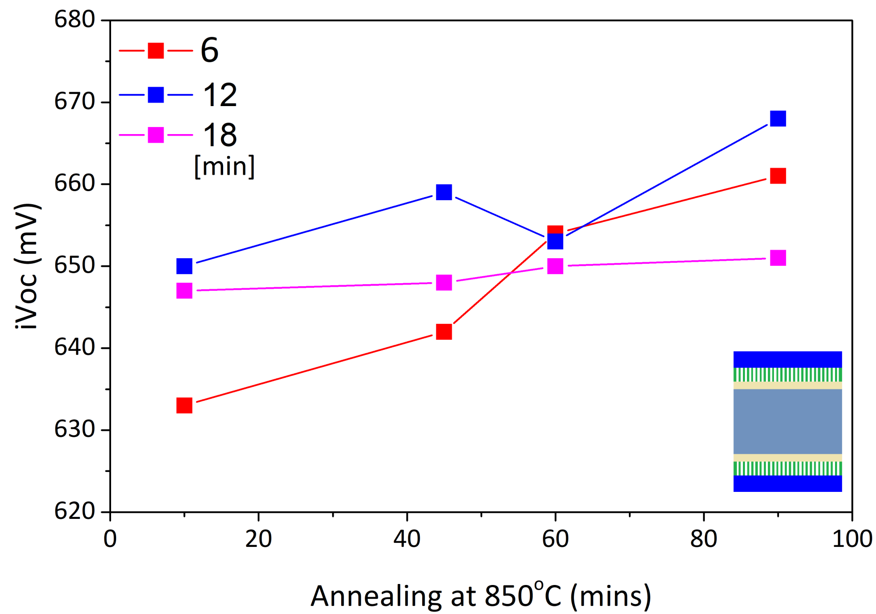

Figure 5.7: Passivation quality of p-poly-SiOx/plasma oxide passivating contacts on p-type flat symmetrical samples. Samples annealed for different times at 850 [^{o}C] and then subjected to hydrogenation. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

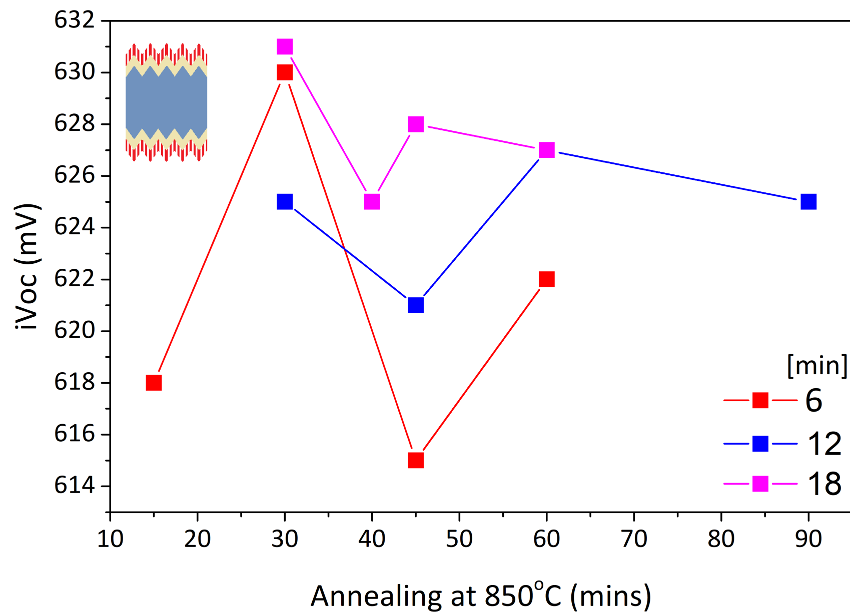

Figure 5.8: Passivation quality of n-poly-SiOx/plasma oxide passivating contacts on n-type textured symmetrical samples. Samples annealed for different times at 850 [^{o}C]. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

result on the p-type flat wafer, which was 638 [mV], but much lower than the n-type flat which achieved 679 [mV]. The growth of the oxide will proceed differently on the textured surface than flat leading to a different layer quality [85]. This has resulted in a poorer passivation of the c-Si interface which is impacting the performance of n-poly-SiOx/plasma oxide. Compar-

ing with the NAOS oxide, the same optimum annealing is found after 30 [min] at 850 [^{o}C], but with a higher iV_{oc} of 683 [mV]. Analysing the sheet resistance of the samples with oxide 18, the layer is consistent across different annealing at 109 [Ω-sq^{-1}] indicating consistent layer integrity [80]. The variation in performance can again be attributed to the varying dopant profile.

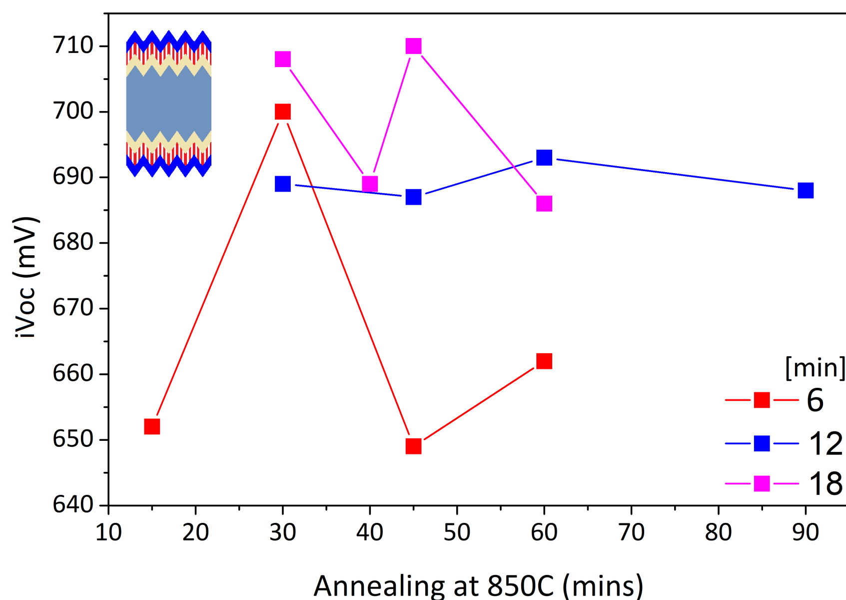

Figure 5.9: Passivation quality of n-poly-SiOx/plasma oxide passivating contacts on n-type textured symmetrical samples. Samples annealed for different times at 850 [^{o}C] and then subjected to hydrogenation. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

Figure.5.9 shows the results for the n-type textured samples after hydrogenation. The trend in each of the curves has remained the same but with increased passivation quality for each sample. Many of the defects associated with these layers and interfaces have been successfully hydrogenated. The n-poly-SiO$_x$/plasma oxide passivating contact with oxide 18 now shows the best result after 45 [min] annealing. An iV_{oc} of 710 [mV] and J_0 of 133 [fAcm^{-2}] is obtained for this condition. This is a much better result than before the hydrogenation step is performed. It is, however, still significantly less than the quality achieved by NAOS under the same conditions. This had an iV_{oc} of 723 [mV] and J_0 of 6.9 [fAcm^{-2}].

5.7. n-type flat/p-type flat

In this section the results of the n-type flat/p-type flat asymmetrical samples are given. This is done to understand how the poly-SiO$_x$/plasma oxide would perform on the IBC structure as here there are both p- and n-type poly-Si layers. Only the performance after the SiN$_x$ plus hydrogenation step is discussed.

Figure.5.10 shows the performance after hydrogenation. In this case the optimum annealing time is found to be 60 [min]. Initially for the n-type samples it was 90 [min] for oxide 6, 10 [min] for oxide 12 and 45 [min] for oxide 18. For the p-type samples 90 [min] was the optimum for all layers. This change can be attributed to the interplay between the two doping profiles leading

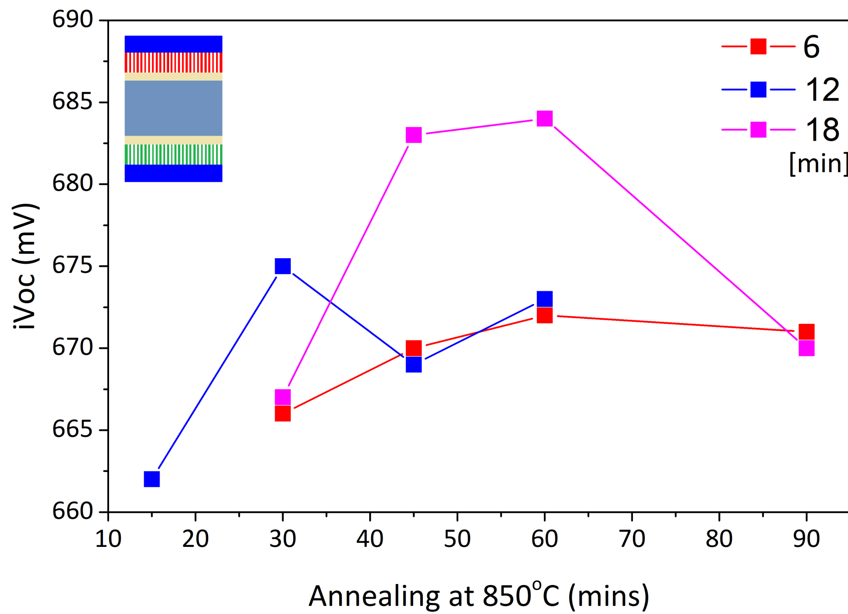

Figure 5.10: Passivation quality of poly-SiOx/plasma oxide passivating contacts on n-type flat/p-type flat asymmetrical samples. Samples annealed for different times at 850 [^{o}C] and then subjected to hydrogenation. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

to a new optimum.

The poly-SiOx/plasma oxide passivating contacts with oxide 18 are by far the best performers. The best of these comes after 60 [min] annealing with an iV_{oc} of 684 [mV] and a J_0 of 65.4 [fAcm^{-2}]. This is still quite low, however, as performance is limited the p-type layer. The sheet resistance of these samples remains constant at a value of 105 [Ω-sq^{-1}] regardless of annealing. The variation in performance is thus coming from the interplay between the doping profiles.

5.8. n-type textured/p-type flat

In this section the results of the n-type textured/p-type flat asymmetrical samples are described after the SiN$_x$ plus hydrogenation step. This combination is used as precursor to the design of the FBC cells.

Looking at figure.5.11 we see a trend of increased performance with longer annealing. The best values for each sample come after 90 [min] annealing. Beyond this point saturation occurs and the passivation quality drops. This is the same optimum annealing condition as the original p-type samples suggesting that this really leads to the ideal doping profile for this layer.

The poly-SiOx/plasma oxide sample using oxide 6 now shows the best performance. An iV_{oc} of 693 [mV] and a J_0 of 39.3 [fAcm^{-2}] is achieved after 90 [min] annealing. On the original textured samples the p-poly-SiOx/plasma oxide using oxide 6 saturated after 45 [min] annealing. The performance dropped to 649 [mV]. On the p-type samples it achieved an iV_{oc} of only 661 [mV] after 90 [min] annealing. Based on these preliminary results it is not entirely clear why this high performance is now seen.

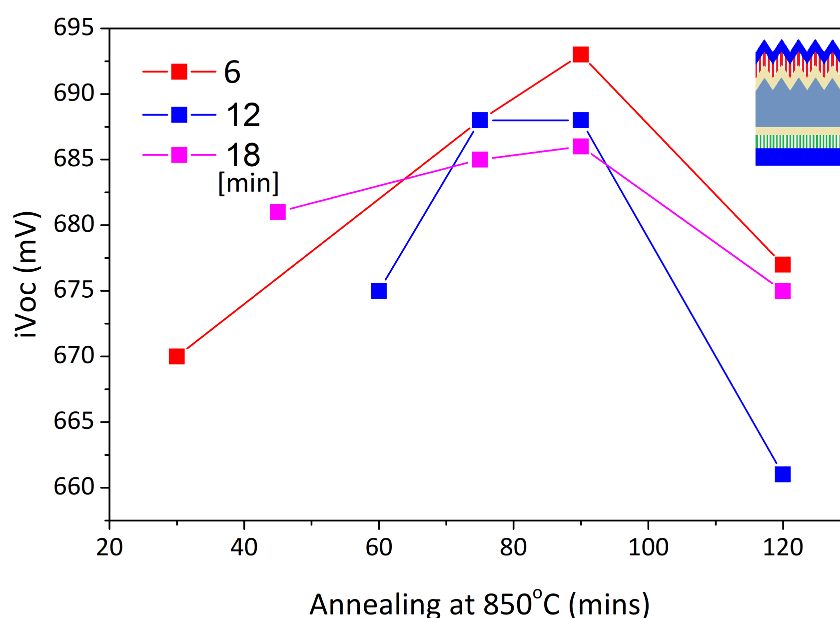

Figure 5.11: Passivation quality of poly-SiOx/plasma oxide passivating contacts on n-type textured/p-type flat asymmetrical samples. Samples annealed for different times at 850 [^{o}C] and then subjected to hydrogenation. Different curves represent plasma oxide reaction time in [min] which is directly correlated with the layer thickness.

Based on these results a selection can be made for the FBC cell design. Oxide 18 showed the best performance on the n-type symmetrical samples, but was the worst performer on p-type. This led to the poorest results on the flat/textured samples making it the wrong choice for the FBC cell. Oxide 6 performed well on n-type textured and reasonably well on p-type, and also showed the best result on the flat/textured samples. However, this result was still not particularly high due to the limitations of the p-type layer. Because of this it was decided that the poly-SiOx/plasma oxide passivating contacts with oxide 12 would be best for the FBC cells based on the high performance on the p-type samples. However, before implementation into the final devices an attempt to improve the passivation of this layer using thicker p-poly-Ox was made. P-type layers of 20 and 30 [nm] were chosen. The results of these tests are given in the next section.

5.9. p-type 20nm, 30nm

In this section an investigation is made of the passivation quality of the poly-SiOx/plasma oxide passivating contact with 12 [min] oxide on thicker p-type layers. Two thicknesses were tested; 20 and 30 [nm], with the aim of achieving higher passivation quality before implementation into an FBC cell. It should be noted that after the crystallisation these layers in fact form 30 and 40 [nm] p-poly-SiO$_x$ layers as the intrinsic poly-SiO$_x$ becomes doped. The results of these tests are shown in figure.5.12.

The figure shows the optimum annealing time has now shifted to 75 [min] with an iV_{oc} of 680 [mV] and a J_0 of 24.1 [fAcm^{-2}]. This is significantly higher than the value achieved on the 10 [nm] p-type samples which was 668 [mV]. The extra p-type material has improved the doping profile for the poly-SiOx/plasma oxide. This has led to an improved field effect passivation,

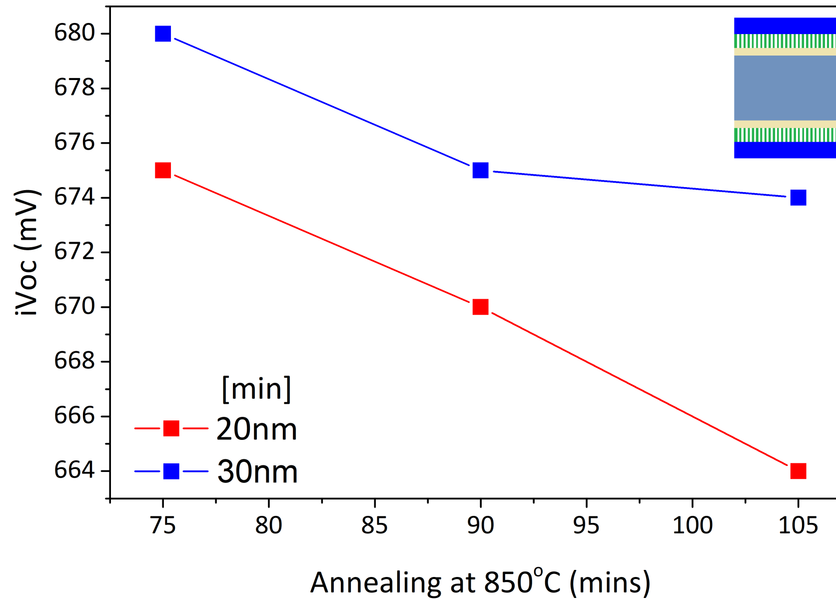

Figure 5.12: Passivation quality of p-poly-SiOx/plasma oxide passivating contacts on p-type flat symmetrical samples. The plasma oxide reaction time was 12 [min]. Samples annealed for different times at 850 [^{o}C] and then subjected to hydrogenation. Different curves represent the thickness of the p-type layer.

raising the overall quality. Now that this layer has been optimised it can be implemented into the FBC cells.

5.10. Conclusion

In the first stage of experimentation the thickness of the tunnel oxide for different reaction times was measured. It was found that the growth rate initially increases exponentially up to around 12 [min] with a thickness of 1.85 [nm]. Beyond this point growth proceeds much more slowly. Growth saturates at 21 [min] with a value of 1.98 [nm]. The thickness closest to the NAOS oxide of 1.4 [nm] was after 9 [min] giving 1.46 [nm].

The passivation quality of these layers was then tested on n-type symmetrical samples. n-poly-SiOx/plasma oxide passivating contact samples were developed for each of the oxide thicknesses. These were annealed at 850 [^{o}C] for a range of times and then hydrogrenated. The best performing samples were those with the 6, 12 and 18 [min] oxide reaction times. The n-poly-SiOx/plasma oxide with oxide 18 was the highest of these, achieving an iV_{oc} of 723 [mV] after 45 [min] annealing.

These 3 oxides were then tested on p-type flat and n-type textured symmetrical samples, and n-type flat/p-type flat and n-type textured/p-type flat asymmetrical samples. Here the same procedure of annealing and hydrogenation was employed. For the p-type flat p-poly-SiOx/plasma oxide samples oxide 12 showed the best passivation of 668 [mV] after 90 [min] annealing. On n-type textured, oxide 18 was again best with an iV_{oc} of 710 [mV] after 45 [min] annealing. On the flat/flat samples the same annealing led to the best value of 683 [mV] for oxide 18. Finally, on the flat/textured poly-SiOx/plasma oxide samples, oxide 6 achieved the best result with an iV_{oc} of 693 [mV], after 90 [min] annealing.

As the p-type layer was limiting sample performance, in an effort to increase the passivation quality before implementation into FBCs, p-poly-SiOx thicknesses of 20 and 30 [nm] were tested. This was done using the best performing 10 [nm] p-poly-SiOx/plasma oxide layer, which was the 12 [min] oxide. This raised the iV_{oc} to 680 [mV] using the 30 [nm] layer. This configuration was thus chosen for implementation into FBC solar cells.

6 Front back contacted solar cells

In this chapter the PECVD tunnel oxide investigated in Chapter 5 is implemented into front back contacted (FBC) solar cells. The chapter begins by introducing the cell design and continues with the processes for fabrication. Next, an analysis is made of the performance of the devices. The chapter ends with a summary of the findings and conclusions.

The FBC cell design studied in this chapter features an n-type bulk, p-type rear emitter and an n-type textured front surface field (FSF), as shown in figure.6.1. This is chosen based on the high quality results achieved with this design using the NAOS oxide [80]. As such, it provides a good reference for the quality of the poly-SiO$_x$/plasma oxide passivating contacts studied here.

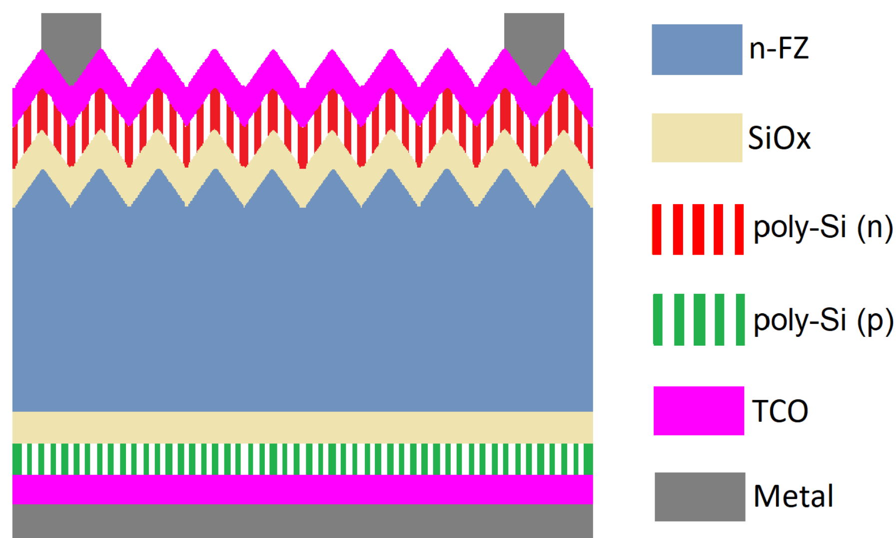

Figure 6.1: FBC solar cell structure. n-type c-Si bulk with 1.85 [nm] PECVD tunnel oxide implemented on front and rear surfaces. Oxide is capped on both sides by a 30 [nm] n-poly-SiO$_x$ on the front and 20 [nm] poly-Si p-poly-SiO$_x$ on the rear. A transparent conductive oxide (TCO) is implemented after these layers to improve conductivity. The rear is fully metalised, whilst the front features cells of 6 and 11 [%] metal coverage.

In Chapter 5 it was found that when implementing the plasma oxide in an n-type textured/p-type flat asymmetrical samples, the p-type layer is limiting. The best p-poly-SiO$_x$ sample was with the plasma oxide grown for 12 [min]. This achieved an iV_{oc} of 668 [mV] on the samples

with a 10 [nm] p-a-SiO$_x$ layer. And achieved 680 [mV] for the samples with a 30 [nm] p-a-SiO$_x$ layer. Thus oxide 12 was selected for implementation into the FBC cells.

The best performance on the n-type textured samples for this layer came after 60 [min] annealing, whilst the best condition for the p-type 30 [nm] samples came after 75 [min]. It was thus decided that in order to maintain the optimum for the n-type layer, a two-step annealing should be implemented. This allowed the p-poly-SiO$_x$ layer to be annealed for a longer total time. To do this the p-a-SiO$_x$ layers were deposited first and annealed for periods of 0 (no initial annealing), 5 or 10 [min], before the n-a-SiO$_x$ layers were added. Once these were deposited, the complete device would undergo a second annealing of 60 [min]. However, this process turned out to produce very low quality passivation and so a second set of FBCs were also tested. These FBCs used the original 10 [nm] p-a-SiO$_x$ layer and were subjected to 1 annealing of 60, 75 or 90 [min] - 90 [min] was the optimal condition found for these samples. The processes to fabricate both sets of cells is outlined in the next section.

6.1. Fabrication

For the fabrication of the FBC solar cells <100> oriented n-type wafers were used for the bulk absorber layer. The cell design required that the front surface be textured whilst the back remained flat. The first step was to apply a protective layer to the rear so the front could be etched. A 500 [nm] capping layer of SiN$_x$ was deposited using PECVD at 400 [^{o}C]. Texturing was done using TMAH solution at 80 [^{o}C] and 300 [RPM] for approximately 10 [min]. Once completed the SiN$_x$ capping layer was removed using BHF 1:7 solution for 26 [min]. Wafers were then cleaned using the standard cleaning process outlined in Chapter. 2, before a 4 [min] 0.55 [%] HF dip to remove any native oxide. Next the wafers were placed in PECVD *AMOR* for the growth of the tunnel oxide and deposition of the i-, n- and p-type a-SiO$_x$ layers. This was at a temperature of 300 [^{o}C].

p-type 30nm

Starting with the rear, first the tunnel oxide reaction is performed. This was done using N$_2$O plasma for 12 [min] leading to an oxide thickness of 1.85 [nm]. This was followed by the 10 [nm] and 30 [nm] a-SiO$_x$ i- and p-layers. Samples were then subjected to the first annealing step of 0, 5 or 10 [min] at 850 [^{o}C]. It should be noted that the 0 [min] condition actually means the front and back are fabricated without leaving *AMOR*. The 5 and 10 [min] wafers were then immersed HF 0.55 [%] for 4 [min]. This removed the native oxide grown during annealing before depositing onto the textured front surface. The front tunnel oxide layer was grown for 20.4 [min]. A factor of 1.7 was added to compensate the slower layer growth on textured surfaces [85]. This was followed by the 10 [nm] a-SiO$_x$ i-layer and 20 [nm] a-SiO$_x$ n-layer. Samples were then annealed for the second time of 60 [min] at the same temperature. After annealing a hydrogenation step was performed by depositing 75 [nm] Si$_x$ on both sides of the cells, and then subjecting them to 30 [min] FGA at 400 [^{o}C]. This furnace had a 10 [%] H$_2$ in N$_2$ ratio of gases. The SiN$_x$:H layer was then removed using BHF 1:7 for 4 [min].

p-type 10nm

The FBCs with a 10 [nm] p-layer were developed in much the same way as the 30 [nm] wafers. Starting from <100> oriented n-type wafers, first the front side texturing procedure was conducted. Next, the wafers were cleaned and the native oxide removed using HF 0.55 [%] for 4 [min]. After this, the tunnel oxide was grown on the front side for 20.4 [min], followed by the 10 [nm] a-SiO$_x$ i-layer and 20 [nm] a-SiO$_x$ n-layer. On the rear side the tunnel oxide is

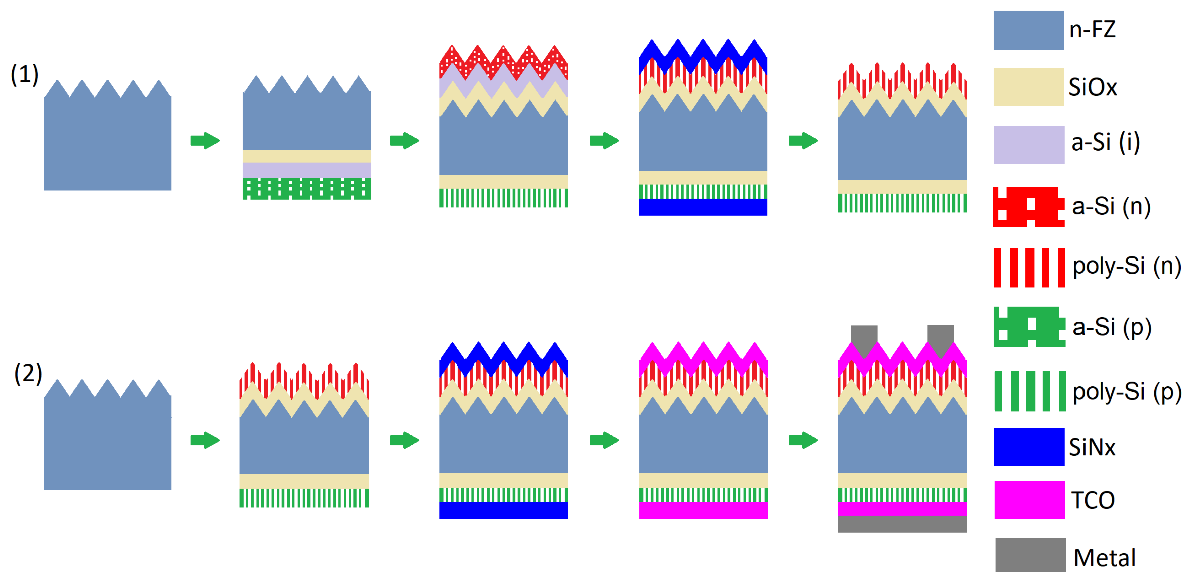

Figure 6.2: FBC fabrication process. n-type textured/flat asymmetrical samples used. (1) p-type 30 [nm] FBC: Tunnel oxide layer of 1.85 [nm] and a-SiO$_x$ i-, p-type layers of 10 and 30 [nm] deposited via PECVD at 300 [^{o}C]. p-poly-SiO$_x$ layers formed after initial annealing at 850 [^{o}C] for 0, 5 or 10 [min]. Removal of native oxide using HF 0.55 [%] before deposition of front surface layers. Tunnel oxide, a-SiO$_x$ i- and n-layers deposited with 1.85, 10 and 20 [nm] respectively. Second annealing of 60 [min] at 850 [^{o}C] performed. 75 [nm] of SiN$_x$:H deposited using PECVD at 400 [^{o}C] and hydrogenation performed for 30 [min] in an FGA furnace at 400 [^{o}C]. Removal of SiN$_x$:H layer using BHF for 4 [min]. (2) p-type 10 [nm] FBC: 1.85 [nm] PECVD oxide, 10 [nm] a-SiO$_x$ i-layer and 20 [nm] a-SiO$_x$ n-layer deposited on front. 1.85 [nm] PECVD oxide, 10 [nm] a-SiO$_x$ i-layer and 10 [nm] a-SiO$_x$ p-layer deposited on rear. Cells annealed for 60, 75 and 90 [min] at 850 [^{o}C]. 75 [nm] of SiN$_x$:H deposited from PECVD at 400 [^{o}C] and hydrogenation performed for 30 [min] in an FGA furnace at 400 [^{o}C]. SiN$_x$:H removed using BHF for 2 [min] 30 [s] and HF 0.55 [%] for 10 [min]. TCO added and Ag metallisation applied via screen-printing.

grown for 12 [min] before the 10 [nm] i- and 10 [nm] p-type a-SiO$_x$ was deposited. 75 [nm] of SiN$_x$:H was added on both sides before FGA at 400 [^{o}C] for 30 [min]. SiN$_x$:H layer then removed using BHF 1:7 for 2 [min] 30 [s], followed by HF 0.55 [%] for another 10 [min]. This was changed from the p-type 30 [nm] process, as the 4 [min] BHF time was thought to be harmful to the p-a-SiO$_x$ layer. Finally, a transparent conductive oxide (TCO) was added at the front and rear of the cell and the metalisation applied via screen printing. The metal on the front was Aluminium and on the rear was silver.

Figure.6.2 shows the flow diagram for these processes and figure.6.3 shows the completed FBC solar cells.

6.2. Results

In this section the performance of the developed FBC cells is discussed. First, the passivation quality of the cells with 30 [nm] p-a-SiO$_x$ layer cells is given. It should be noted that after the crystallisation this in fact forms a 40 [nm] p-poly-SiO$_x$ layer as the intrinsic poly-SiO$_x$ becomes doped. Next, the passivation quality for the cells with the 10 [nm] p-a-SiO$_x$ layers are discussed. The results of the Suns-V$_{oc}$ and EQE measurements of these cells are presented. Finally, to gain a deeper insight into the performance of tunnel oxide layer a transition line method (TLM) measurement is made.

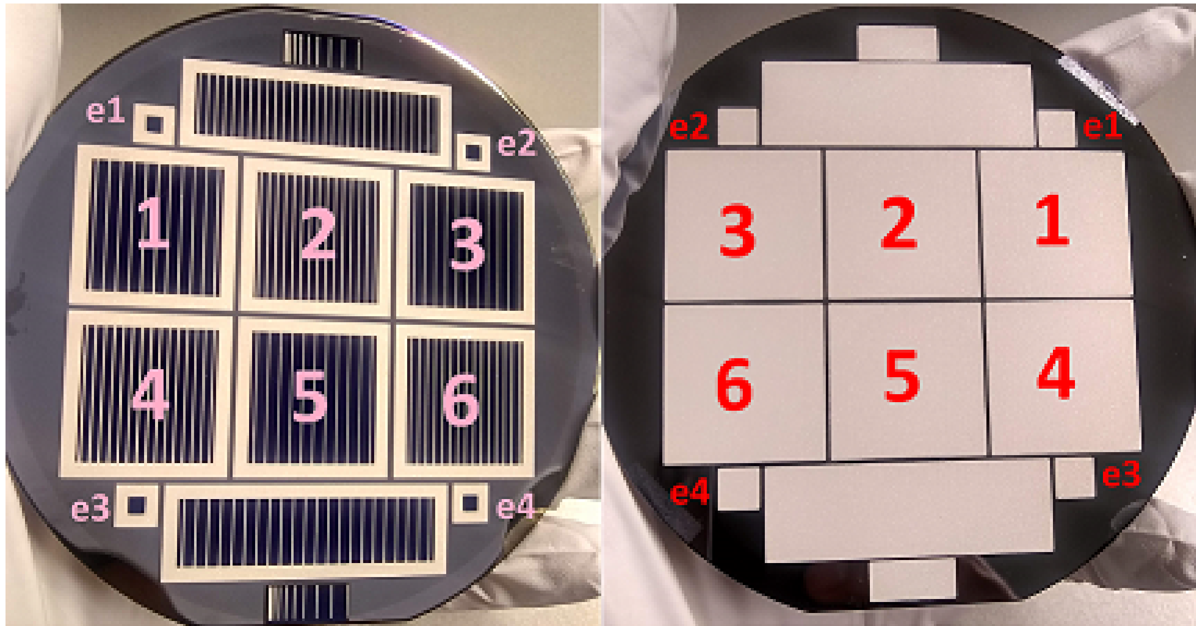

Figure 6.3: Fabricated FBC cells. Left: Front metalisation pattern. Cells 1, 3 and 5 have 6 [%] metal coverage whilst cells 2, 4 and 6 have 11 [%]. Both sets have a cell area of 4 [cm^2]. Cells e1-4 were used to measure the EQE. Right: Rear of FBC cell with full area metalisation.

6.2.1. FBCs with p-type 30nm

In table.6.1 the passivation quality of the p-type 30 [nm] samples is shown. These measurements were made before metalisation so can be considered asymmetrical samples. It is clear that the passivation quality here is very low. The p-type layer used is too thick and this is detrimentally affecting the doping profile across the c-Si/poly-SiO$_x$ interface. The concentration of Boron (B) dopants from this layer is too high and therefore the field effect passivation is no longer optimal. There will also be much more B diffusion into the bulk, causing defects.

Table 6.1: Passivation quality of FBC cells with 30 [nm] p-a-SiO$_x$ layers at different stages in the fabrication process

Cell	Annealing [min]	Hydrogenation [mV]	SiN$_x$:H removed [mV]
11	60	591	594
21	5 + 60	580	581
22	5 + 60	572	566
31	10 + 60	624	625
32	10 + 60	566	571

What is also evident is that the 2 step annealing process is harming the cell quality. Cell 11 was the only cell to be fabricated in one step and this shows the best performance - excluding cell 31 which is an outlier. The annealing step is performed at another lab so all the twice annealed cells will have experienced extra contamination before the deposition of the front side layers. This has probably affected the cell performance despite the cleaning and HF steps. As well as this, the total annealing time will have been much longer when considering the ramping time of the furnace. This will have caused greater B diffusion, further reducing the passivation.

Cell 31 is the only cell able to achieve an iV_{oc} above 600 [mV], but this does not fit the trend of the data. Inspection of this wafer showed the presence of small bubbles on the p-type surface. This indicates blistering had occurred during annealing. It is likely that the B diffusion was unsuccessful in these areas and so the detrimental field effect/defects seen on the other wafers was not so extreme here.

6.2.2. FBCs with p-type 10nm

Table.6.2 shows the passivation quality of the p-type 10 [nm] FBCs at various stages of the fabrication process.

Table 6.2: Passivation quality of FBC cells with 10 [nm] p-a-SiO$_x$ layers at different stages in the fabrication process

Cell	Annealing [min]	Hydrogenation [mV]	SiN$_x$:H removed [mV]	TCO [mV]
1	60	686	689	648
2	60	682	686	643
3	75	682	687	624
4	75	687	690	638
5	90	689	689	656

For these cells the passivation quality is fairly consistent after hydrogenation and after the removal of the SiN$_x$:H. However, there is a large drop after the application of the TCO layer. This can be attributed to the damage caused to the surface from the bombardment of the TCO molecules [69]. The best value at this stage comes from cell 5 with an iV_{oc} of 656 [mV].

In table.6.3 the results of the Suns-V$_{oc}$ measurements are shown. The 6 and 11 [%] cells were averaged for each wafer.

Table 6.3: Results of Suns-V$_{oc}$ measurements of of 10 [nm] p-type FBC cells

Cell	Metal [%]	Suns-V$_{oc}$ [mV]	pFF [%]
1	6	464	91
	11	481	91
2	6	516	91
	11	517	89
3	6	510	85
	11	504	85
4	6	486	95
	11	496	93
5	6	177	59
	11	5	3

After the screen-printing process the performance of the cells again drops. The best performing cells come from the 60 [min] annealing series with a metal coverage of 11 [%]. Here a

Suns-V_{oc} of 517 [mV] is achieved. This is much lower than the NAOS equivalent of 706 [mV] so further optimisation of the plasma oxide is required. The psuedo fill-factor (pFF) values are much higher than the NAOS equivalent of 84 [%]. The average pFF value for the cells with 6 [%] metal coverage is 91 [%]. For those with 11 [%] coverage it is 90 [%]. This indicates that the series resistance from the plasma oxide is much higher than the NAOS oxide. The oxide layer is thus inhibiting the flow of current and decreasing the overall cell performance. Cell 5 is by far the worst performer. Unfortunately this was due to an issue during screen-printing which meant that the metal coverage was not uniform on the rear.

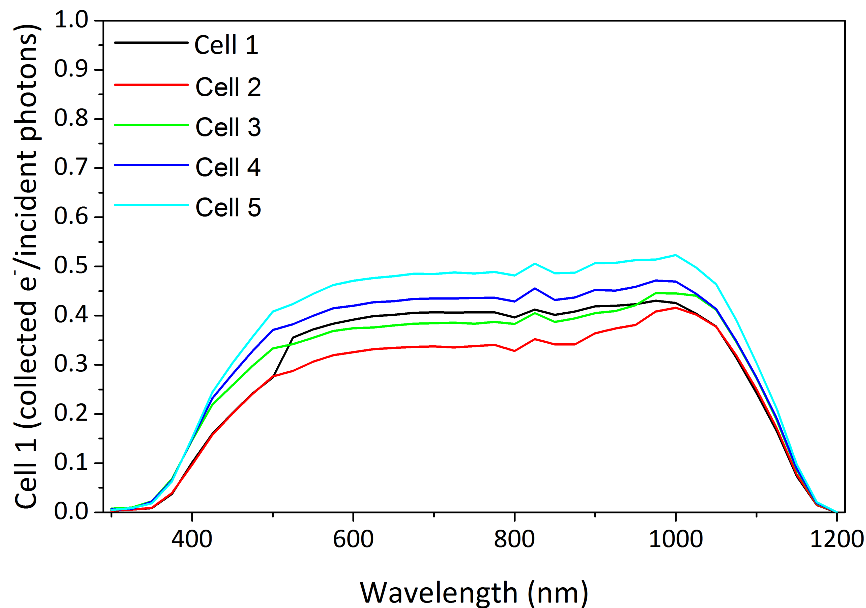

Figure 6.4: EQE of different FBC cells

figure.6.4 shows the external quantum efficiency (EQE) measurements for each of the different cells. The plot shows that there is some current and they are indeed performing as solar cells. However, this current is being blocked by the plasma oxide layer due to the high series resistance. The plot also shows that light absorption improves with longer annealing. This can be attributed to the formation of pinholes in the oxide layer that faciliate carrier transport in the cell [48]. A longer annealing, or higher temperature annealing, may be required to further break up the oxide layer. Alternatively, a different set of parameters could be used for the growth of the oxide. For example a lower N_2O flow, or higher pressure. This might allow the development of thinner oxides with better passivation.

6.3. Measuring $R_{contact}$ of plasma oxides

To better understand the performance of the FBC cells the contact resistance of the PECVD tunnel oxides was measured. This was done via the Transition Line Method (TLM) [86]. The 6, 9, 12, 15 and 18 [min] oxides were selected. The oxides were grown on n-type <100> wafers and annealed for 45 [min] at 850 [^{o}C]. A 1 [μm] deposition of Al in the pattern shown in figure.6.5 was then deposited using metal evaporation. The results of the tests are shown in figure.6.6 and table.6.4.

Looking at the left plot of figure.6.6 the different TLM measurements for each of the layers is

Figure 6.5: TLM pattern used to measure contact resistance of 6, 9, 12, 15 and 18 [min] tunnel oxides on n-type flat wafers. Highlighted in red are the 1 [μm] Al fingers used for the measurements.

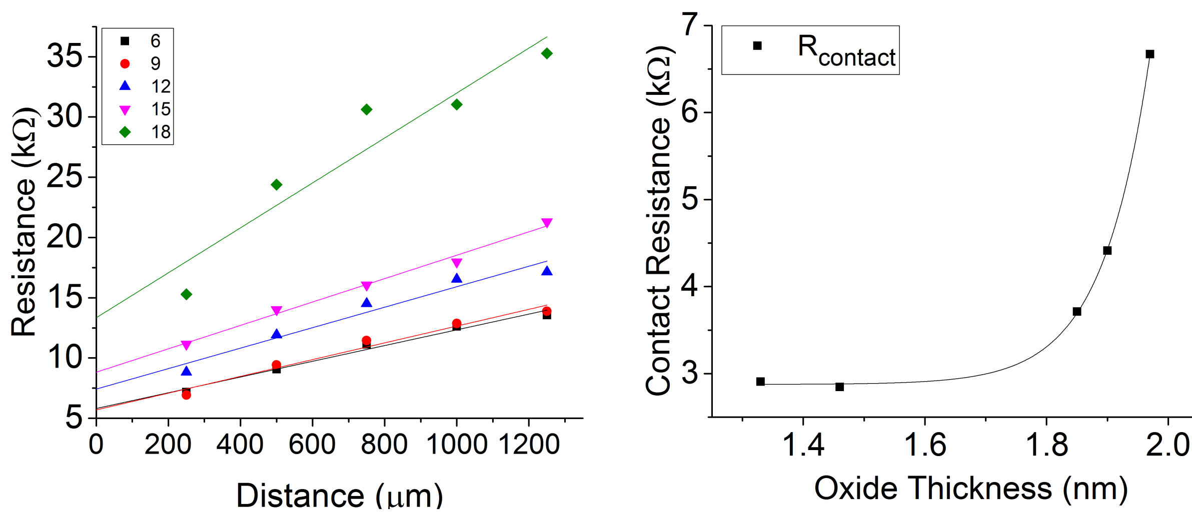

Figure 6.6: Left: TLM measurements of layer resistance against finger spacing distance for 6, 9, 12, 15 and 18 [min] plasma oxides. Right: Plot of $R_{contact}$ against increasing plasma oxide thickness

seen. The y-intercept gives the value of twice the contact resistance, $R_{contact}$, while the slope is related to the sheet resistance, R_{sheet}. Both values increase with greater oxide thickness. This trend increases with reaction time such that the values for the oxide 18 are much higher than the others. On the right hand graph the $R_{contact}$ values are plotted against the layer thickness and an exponential relationship is revealed. In Chapter.5 it was found that after a reaction time of 12 [min] the oxide growth rate begins to saturate and the effect of this is seen here. Beyond this point the reaction is predominantly changing the layer density which is leading to much larger $R_{contact}$ values.

Table.6.4 shows the data used in figure.6.6. The $R_{contact}$ value for oxide 12 is 3.71 [$k\Omega$]. This is incredibly high. This is typically on the order of [mΩ] [80] so explains why the FBCs were unable to produce good values. All of the oxide layers are restricting the flow of current and so provide good passivation but poor quality solar cells. To combat this a higher annealing temperature must be investigated in order to break up this layer and reduce the resistance value. Conversely, thinner plasma oxides could also be developed using different reaction

Table 6.4: $R_{contact}$ and thickness values for plasma oxides 6, 9, 12, 15 and 18 [min]

Oxide .[min]	Thickness [nm]	$R_{contact}$ [$k\Omega$]
6	1.33	2.91
9	1.46	2.85
12	1.85	3.71
15	1.90	4.41
18	1.97	6.67

parameters.

6.4. Conclusion

In this chapter the tunnel oxide investigated in Chapter.5 was implemented into front back contacted solar cells. The chosen oxide was 12 [min] based on the performance on the p-type symmetrical samples, which were limiting. FBCs with a 30 [nm] and 10 [nm] p-type a-SiO$_x$ layer were tested. The 30 [nm] layer was found to be too thick, adding too much Boron to the bulk, detrimentally affecting the cell quality. An iV_{oc} of only 594 [mV] was achieved for the sample with 60 [min] annealing.

The 10 [nm] FBCs performed much better achieving a maximum iV_{oc} of 690 [mV] after 75 [min] annealing. All cells saw a large drop in passivation quality due the damage in the application of the TCO layer. The best cell after this step came after 90 [min] annealing with an iV_{oc} of 656 [mV]. The Suns-Voc measurements taken once the metal was applied showed that the performance had again dropped. The best cell now came from 60 [min] annealing with a front metal coverage of 11 [%]. This had an iV_{oc} of 517 [mV]. These measurements also revealed extremely high pFF values of above 90 [%] suggesting the oxide layer was restricting current flow in the cells. An EQE measurement showed that light absorption/successful carrier collection improved with longer annealing. Increased annealing caused the formation of more pinholes in the oxide layer, aiding the current flow.

Finally, TLM measurements were made for the 6, 9, 12, 15 and 18 [min] oxides which revealed that the contact resistance for each of these layers was incredibly high. Oxide 12 had an $R_{contact}$ of [$k\Omega$] leading to the very high pFF values and low current flow in the FBC cells. It was proposed that a higher annealing temperature should be investigated in order to break up the oxide layer, and facilitate better current flow for future devices. Another option would be the development of thinner tunnel oxides using different parameters for the PECVD reaction.

7 Conclusions

The goal of this thesis was to enhance the passivation quality of poly-Si IBC cells and investigate the performance of PECVD tunnel oxides in poly-SiO_x FBC cells. To do this 3 key areas were studied: the passivation of the front surface field (FSF), the application of an optimised rear hydrogenation and the investigation of an alternative PECVD oxide and poly-SiO_x passivating contact. The findings of the first two studies were implemented into poly-Si IBC cells whilst the third was used in poly-SiO_x FBC cells. The outcomes of each stage of this research, as well the recommendations for further work, are given below.

In Chapter.3 different options for the front surface field were examined. The aim of this research was to find an optically transparent layer for the front surface (FS) passivation. The former a-Si:H/SiN_x:H layer had exhibited parasitic absorption fromt the a-Si:H. Four materials were first tested on undoped <111> n-type symmetrical samples: SiO_2/SiN_x:H, 10/75 [nm], SiO_2/AlO_x:H/SiN_x:H, 10/10/75 [nm], AlO_x:H/SiN_x:H, 10/75 [nm], and a-Si:H/SiN_x:H, 18/75 [nm]. The best performers were the AlO_x:H/SiN_x:H and a-Si:H/SiN_x:H layers which achieved iV_{oc} values of 724 and 731 [mV] and J_0 values of 4 and 5 [fAcm^{-2}] respectively. These excellent results were owing to the high hydrogen content of these layers, providing effective passivation of the c-Si interface. Unfortunately the tool for the AlO_x:H was no longer usable, so this research could not be pursued. As such the a-Si:H/SiN_x:H layer was chosen for further tests. The 18 [nm] a-Si:H layer was slightly thinner than the 22 [nm] thickness used in the former poly-Si IBC.

The a-Si:H/SiN_x:H was then tested with varying thicknesses, with a view to reducing the effect of parasitic absorption, and varying doping doses for the FSF. The thicknesses tested were: 4.5, 9, 13.5 and 18 [nm]. The dopant doses were: No FSF, 1e14, 2e14, 4e14 and 6e14 [ions-cm^{-2}]. These equate to doping concentrations at a depth of 10 [nm] of 0, 2e19, 4e19, 7e19 and 1e20 [atoms-cm^{-3}] respectively. The results of these tests showed that the best condition was with the No FSF/18 [nm] a-Si:H - as in the undoped passivation tests. This achieved 730 [mV] and 13.2 [fAcm^{-2}]. Despite this it was decided that the 9 [nm] a-Si:H layer should be implemented in the IBCs as this would lead to a larger drop in parasitic absorption. With this layer the best passivation of 722 [mV] and 7.3 [fAcm^{-2}] was again achieved with No FSF. It was also decided that each of the doping levels be implemented into IBCs so that the effect of FSF doping in complete devices could be investigated.

The main recommendation for this research would be the further investigation of the AlO_x:H/SiN_x:H passivation stack. This achieved excellent passivation of the c-Si interface and was an opti-

cally transparent alternative to the a-Si:H layer FS passivation layer.

The optimisation of the rear hydrogenation was also investigated in Chapter.3. Here again four material stacks were tested but in this case on <100> oriented n-type wafers. To imitate the structure of the poly-Si emitter and BSF that this hydrogenation would be applied to, two symmetrical samples were developed. One with the NAOS tunnel oxide and p-poly-Si layer for the emitter. And another with the NAOS tunnel oxide and n-poly-Si layer for the BSF. The tested materials were: SiN_x:H, 75 [nm], SiO_2/SiN_x:H, 100/75 [nm], AlO_x:H/SiN_x:H, 20/75 [nm], and a-Si:H/SiN_x:H, 6/75 [nm]. After the deposition of these layers a forming gas annealing was performed at 400 [^{o}C] for 30 [min]. The optimal condition was found using the a-Si:H/SiN_x:H stack and this process was selected for implementation in the poly-Si IBC cells. It achieved 725 [mV] and 6.9 [fAcm^{-2}] on the BSF and 709 [mV] and 37.5 [fAcm^{-2}] on the emitter.

Both the optimised FSF passivation and rear hydrogentation were applied to poly-IBC cells in Chapter.4. Unfortunately this did not lead to good results due to an issue in the fabrication process. The 75 [nm] SiN_x on the rear of the device was found to be too small to withstand the final post-metalisation annealing step. The Al contacts were thus able to connect both the BSF and emitter regions. This formed a shunt path that destroyed the performance of the devices. As such only the IBC with FSF doping 2e14 was presented. This achieved an efficiency of 7.22 [%] after a post-metalisation FGA of 120 [s] at 400 [^{o}C]. The R_{shunt} value for this layer was very low at 180 [Ω] indicating the presence of the shunt path.

Further work on these devices should focus on optimising the final fabrication process. A thicker SiN_x layer should be applied to be more robust against the final annealing step.

In Chapter.5 the investigation of PECVD tunnel oxide on poly-SiO_x passivating contact samples was made. First the thickness was measured for different reaction times in N_2O plasma. After 3 [min] a thickness of 1.22 [nm] was achieved. After 21 [min] growth saturated at 1.98 [nm]. The closest sample to the 1.4 [nm] NAOS oxide currently implemented in the IBCs came after 9 [min]. This had a thickness of 1.46 [nm].

Implementing the plasma oxides into flat n-poly-SiO_x symmetrical samples showed that the passivating contacts with the 18 [min] oxide performed best. The thickness of oxide 18 was 1.98 [nm]. This sample achieved 723 [mV] and 4.9 [fAcm^{-2}]. This was after 45 [min] annealing at 850 [^{o}C] and hydrogenation from 75 [nm] SiN_x and FGA for 30 [min] at 400 [^{o}C]. On flat p-poly-SiO_x symmetrical samples the best value came from the 12 [min] oxide, with thickness 1.85 [nm]. This achieved 668 [mV] and 28 [fAcm^{-2}] after 90 [min] at 850 [^{o}C] and the same hydrogenation step. Oxide 18 again performed best in the textured n-poly-SiO_x samples. Here it obtained 710 [mV] and 8.8 [fAcm^{-2}] after 45 [min] annealing at 850 [^{o}C] and hydrogenation. In each of these tests, the diffusion of dopants was found to be of major importance to the passivation quality. The optimum annealing needed to be applied to get the best doping profile.

Next the plasma oxides were implemented into asymmetrical samples. Namely flat n-poly-SiO_x/flat p-poly-SiO_x and textured n-poly-SiO_x/flat p-poly-SiO_x. On the flat/flat samples oxide 18 was the best after 60 [min] plus hydrogenation. It achieved 684 [mV] and 65.4 [fAcm^{-2}]. On the textured/flat samples poly-SiO_x passivating contacts using the 6 [min] oxide, with a thickness of 1.33 [nm] performed best. This sample obtained 693 [mV] 39.3 [fAcm^{-2}] after 90 [min] annealing plus hydrogenation. These results showed that the p-type layer was limiting,

so in an attempt to improve performance flat p-poly-SiO$_x$ symmetrical with thicker p-a-SiO$_x$ depositions were tested. The chosen thicknesses were 20 and 30 [nm]. The chosen oxide was oxide 12 as this performed best on the former p-poly-SiO$_x$ samples. This resulted in 680 [mV] and 24.1 [fAcm^{-2}] for the 30 [nm] p-a-SiO$_x$ case. The optimal annealing condition was 75 [min] with the same hydrogenation step as the other samples.

The passivating contacts using plasma oxide 12 were implemented into the FBC cells in Chapter.6. This was first tested with the 30 [nm] p-a-SiO$_x$ layer. Unfortunately this was found to be unsuccessful due to the presence of too much Boron which affected the field effect passivation. A peak value of 594 [mV] was obtained before the application of the TCO and metalisation.

Another set of FBCs was prepared with the original 10 [nm] p-a-SiO$_x$ layer. These were tested with annealing times of 60, 75 and 90 [min] at 850 [^{o}C] and the same hydrogenation step. The best iV_{oc} of 689 [mV] came from the sample with the 90 [min] annealing. After this step the SiN$_x$:H was removed which had almost no impact on the results. However, once the TCO was applied the performance dropped significantly. The 90 [min] annealed sample remained the best but with a much lower value of 656 [mV]. This was determined to be the effect of surface bombardment during the TCO deposition.

Finally the metalisation was applied and the Suns-V$_{oc}$ measured. Two metalisation patterns were tested: one with 6 [%] front metal coverage and another with 11 [%]. This step led to a major drop in the V_{oc}. The best value now came from the 60 [min] annealing sample with 11 [%] coverage. This achieved 517 [mV]. The cells also had very high pseudo-fill factor values of 90 [%] indicating there was a high contact resistance in the plasma oxide layer. An EQE analysis was made which showed that the light absorption improved with longer annealing suggesting the formation of pinholes in the plasma oxide. These were facilitating better transport of charge carriers improving electron collection.

Finally a TLM measurement of the 6, 9, 12, 15 and 18 [min] plasma oxides was made. The results showed incredibly high $R_contact$ values on the [kΩ] scale. Oxide 12 had a value of 3.71 [kΩ] explaining the poor performance of the FBC cells. This value was too high for good current flow.

Further work should thus be done on reducing the contact resistance of the PECVD tunnel oxide. To do this higher annealing temperatures should be tested to break up the oxide layer. Alternatively, new parameters should be tested to form thinner, better quality layers.

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