An Alternative ADC for MPPT Applications in a PV-PMIC System

A current sampling low power ADC with Non-Linearity Canceling Time-to-Digital Converter

MSc Thesis

Rui Mao

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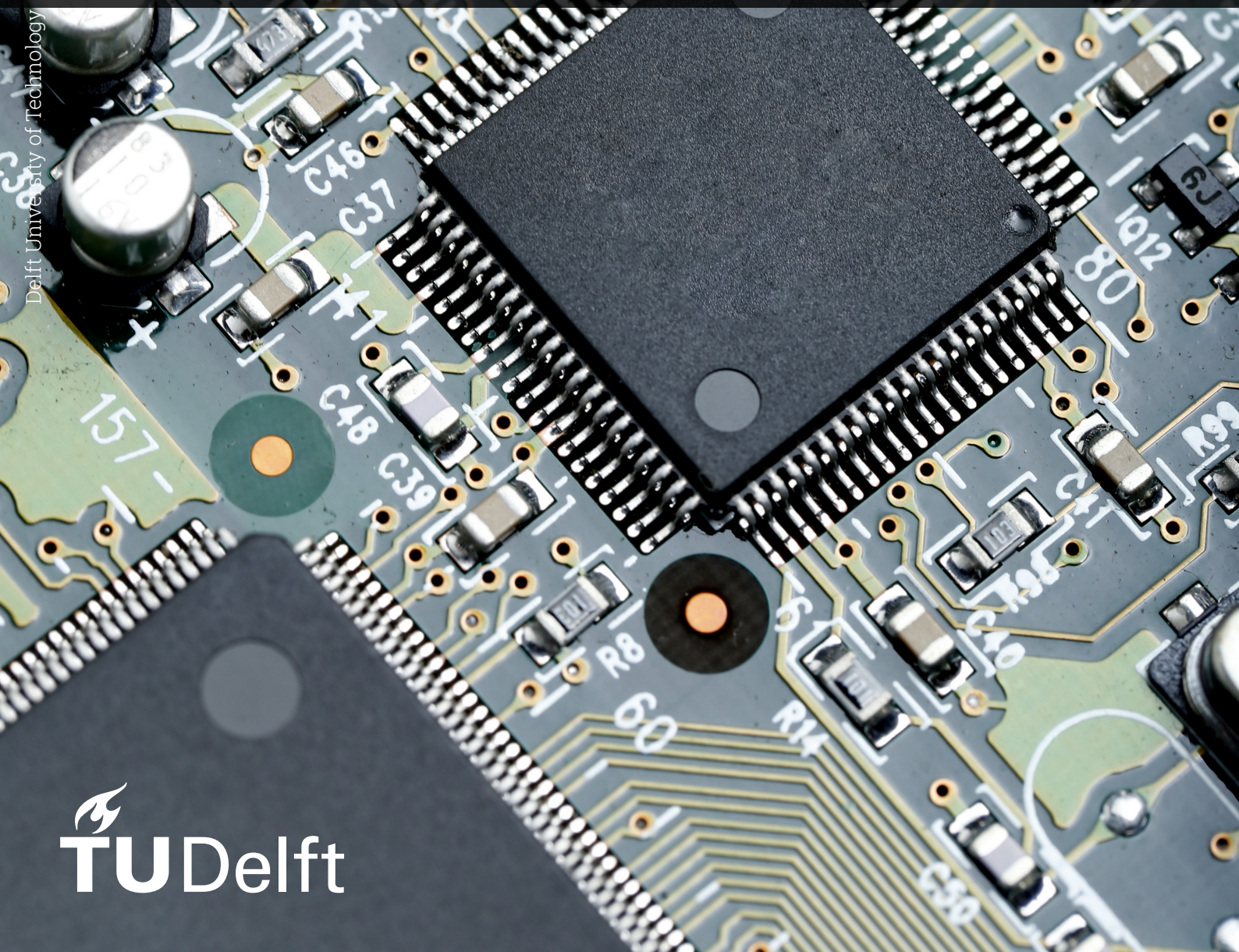

TU Delft

An Alternative ADC for MPPT Applications in a PV-PMIC System

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by

Rui Mao

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TU Delft

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Abstract

The globe is being challenged by growing population and accelerated urbanization, which demands sustainable usage and sharing of resources to create more livable and smarter environments at all scales. To answer those demands, the Internet of Things (IoT) is ultimately a powerful enabler to share resources on a large scale. IoT requires pervasive sensing, which demands a large number of distributed nodes with integrated circuits to collect information. Therefore, Photovoltaic Energy Harvesters (PVEH) have been widely chosen to power IoT nodes, which minimize the maintenance costs. PVEHs are usually managed by Power Management Integrated Circuits (PMIC), also referred to as Photovoltaic cell based PMIC (PV-PMIC). One of the most important feature of PV-PMIC is Maximum Power Point Tracking (MPPT), which ensures the system can output power at Maximum Power Point (MPP). Among various MPPT algorithms, Perturb and Observe (P&O) is the most popular, which requires measurements of a combination of current and voltage of different nodes or branches, which are analog signals and need to be converted into digital signals. To achieve this analog-to-digital conversion, many ADC and TDC architectures have been proposed, but they are all challenged by power limitation and mismatch and Process, Voltage, and Temperature (PVT) variation. This thesis aims to present the design procedure of a new type of ADC for MPPT structure in a PV-PMIC system. To achieve the objectives, a literature research is carried out, with the research question being 'Which Analog-to-Digital Conversion techniques are suitable for MPPT in a low-power, small-area chip?'. After the literature research, a set of requirements are established and an alternative ADC design is proposed and tested. The proposed design combines capacitive current sampling and a Non-Linearity Canceling TDC. The proposed design is further verified at different levels, including the system level and the circuit level. The final verification includes three tests, namely the Linear Time Response, the Static Response and the Frequency Response. The obtained results show that the proposed system at the circuit level achieves ENOB=3.97, FoM=4.17 pJ/conv-step, DNL bounded to ±0.8 LSB, and INL bounded to 2.5 LSB. It is further concluded that the proposed system generally meets the requirements. Moreover, the proposed system has unique advantages compared to conventional ADCs for the dedicated MPPT application. Possible future improvements include further improving linearities, designing calibration and trimming methods, and replacing the hard-coded logic with a storage component.

Nomenclature

Abbreviations

Abbreviation	Definition
ADC	Analog to Digital Converter
CSA-TDC	Cyclic Successive Approximation TDC
DAC	Digital to Analog Converter
DC	Direct Current
DLL	Delay Locked Loop
DL-TDC	Delay Line TDC
DNL	Differential Non-Linearity
DR	Dynamic Range
DTC	Digital to Time Converter
EH	Energy Harvesting (Harvester)
ENOB	Effective Number of Bits
FOCV	Fractional Open Circuit Voltage
FoM	Figure of Merit
FS	Full Scale
FSM	Finite State Machine
FSSC	Fractional Short Circuit Current
GRO	Gated Ring Oscillator
IC	Integrated Circuit
IC	(As an algorithm) Incremental Conductance
INL	Integral Non-Linearity
IoT	Internet of Things
LSA-TDC	Linear Succesive Approximation TDC
LSB	Least Significant Bit
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSB	Most Significant Bit
OTA	Operational Transconductance Amplifier
PH	Photovoltaic Harvester
PMIC	Power Management Integrated Circuit
P&O	Perturb and Observe
PV	Photovoltaic
PVEH	PV Energy Harvesting (Harvester)
PV-PMIC	PV cell based PMIC
PVT	Process, Voltage and Temperature
RO	Ring Oscillator
SAR-ADC	Successive Approximation Register based ADC
SA-TDC	Successive Approximation TDC
SNDR	Signal to Noise and Distortion Ratio
TDC	Time to Digital Converter
VCO	Voltage Controlled Oscillator
VCO-ADC	VCO based ADC
VEH	Vibration Energy Harvesting (Harvester)
ΣΔ-ADC	Sigma Delta ADC

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1 Introduction

1.1. Problem Definition

The globe is being challenged by growing population and accelerated urbanization, which demands sustainable usage and sharing of resources to create more livable and smarter environments at all scales. This aim can be broken down into several aspects. One aspect is increasingly relieving humans from routine tasks, repetitive labour, and recently data-driven decision making. Relevant applications are automation in factories, robotics, and smart driving aids. Another aspect is creating healthy environments where humans can be happy and productive. Relevant applications are geosocializaiton and participatory sensing, which involve not only individuals but also objects to support human activities. In a general sense, all those applications require pervasive and continuous sensing. Pervasive sensing means the sensing nodes are distributed massively into different places where the collection of physical information is required. Continuous sensing means the collection of information is performed repetitively and routinely in the lifecycle of a node. For all applications mentioned above, the Internet of Things (IoT) is ultimately a powerful enabler to share resources on a large scale [1].

The need of pervasive sensing demands a large number of distributed nodes with integrated circuits (IC) to collect information. Such nodes usually sample the dedicated physical information in different places and communicate with the control system. Because the number of nodes is large, the costs of each node should be reduced to meet the budget. The cost requirement further breaks down to manufacturing costs and maintenance costs. The former requirement usually translates to the need for chip sizes to shrink in order to reduce silicon costs. The latter translates to self-powering, robustness, and requiring less frequent maintenance or even free from maintenance.

1.1.1. PV Energy Harvesting

To reduce the need for maintenance, Energy Harvesters (EH) have been widely chosen to power IoT nodes [2]. Such EHs are demanded to be compact in area or space, have low self-power consumption, and provide stable supply to the system [1]. These requirements restrict the usable energy sources. So far, the most popular sources are photovoltaic (PV) energy [2] and vibration energy [3]. Vibration Energy Harvesting (VEH) has also been studied but is less applied than PV Energy Harvesting (PVEH). The reason includes its drawbacks, such as a limited life cycle due to moving parts and low power density [3]. VEH is therefore not discussed in this thesis.

PV energy sources include solar energy and other ambient light sources. Solar energy has been widely and increasingly used on buildings and in solar parks. The quick expansion of the PV energy market is due to several advantages of the PV cells. For example, they do not contain moving parts and do not require maintenance in their life cycles [4]. Besides, it is scalable from as small as thumbnail sizes to as large as power plant sizes. Moreover, although the biggest ambient light source is the sun, small PV-boards can also harvest indoor lighting for electricity. As a result, the IoT nodes powered by PV cells are not limited to day time outdoor scenes, but also indoor scenes or wherever illumination exists.

PV cells have environment dependent characteristics, which refer to the output power changes with irradiation and ambient temperature [2]. Therefore, PV cell control should be applied to PV cell circuits for maximum power point tracking (MPPT). The control is performed by a power management

integrated circuit (PMIC), which is also referred to as PV cell based PMIC (PV-PMIC). PV-PMIC usually contains a DC-DC converter because of the DC-like nature of PV cells as electrical energy sources. By switching the conversion ratio, the PV cells match different load voltages so that the system can output power at Maximum Power Point (MPP).

The MPPT algorithms include Incremental Conductance (IC), Perturb and Observe (P&O), Fractional Open Circuit Voltage (FOCV), and so on. All these algorithms have their advantages and disadvantages. So far, the most popular algorithms in commercial designs are P&O and FOCV [4] due to their simple algorithm and applicability in ICs.

The input of the MPPT structure is the digitized information about the performance of the EH circuit. The information can be provided by different measurements such as voltages, currents, ambient temperature, ambient irradiance, and so on. Such information is acquired from a data processing chain.

1.1.2. Data Processing Chain (ADCs)

The mentioned algorithms require physical data reading and conversion. For some algorithms, such as the Perturbe and Observe (P&O) algorithm and the Fractional Open Circuit Voltage (FOCV) algorithm, the physical data set is defined as a combination of current and voltage of different nodes or branches, which are analog signals. A current or voltage reading chain includes three blocks, namely an analog front-end, an ADC block, and a digital back-end. Taking the requirements of P&O as an example, the analog front-end includes a perturbation circuit and a pre-amplifier. The ADC further converts analog information into the digital domain. Then, the digital back-end stores the digital results and forwards them to the control logic. Among these three blocks, the ADC is the most important block to design. Many choices should be made by considering the power consumption, area usage, accuracy, speed, and other specifications.

The ADC architectures include Flash ADC, Sucessive Approximation Register based ADC (SAR-ADC), Sigma-Delta ADC ($\Sigma\Delta$-ADC), Level Crossing ADC and so on. These architectures have been thoroughly discussed in all different aspects, and each architecture fits a set of applications. SAR-ADCs are the most popular architecture in low power designs thanks to their scalability that makes them compatible with small chip area, and their low power consumption when performing low speed measurements.

Besides conventional ADCs that convert the input quantities to digital codes directly, there are also alternatives by converting input voltage or current first to the time domain and then the digital domain. Such structure borrows the TDC for its high accuracy, high dynamic range (DR), and highly digital nature.

1.1.3. Challenges

One of the challenges of designing such an IoT node is power limitation. On the one hand, the node should be compact, which means the powering structure should not occupy too much area or space. Combining small PV cell area with limited power density per unit PV cell area, the total available power of an IoT node can be estimated to stay at the level of milliwatts (mW) or even microwatts (μW). On the other hand, the power reduction creates circuit design challenges in analog circuits. To reduce power, supply voltage and branch current often need reduction, damaging the signal swing or stage gain.

Besides, reducing the sizes of the CMOS components also face hazards created by mismatch and Process, Voltage and Temperature (PVT) variation. As the component size shrinks, the impact of mismatch will increase accordingly. Taking SAR-ADC as an example, the mismatch in component sizes not only translates to the offset voltage in the comparator, but also errors in reference voltages. When the impact of the mismatch becomes too large, the circuit structures need to adopt compensation techniques, by either increasing capacitor area or increasing power. Either compensation technique is going to leverage the benefits of size shrinking.

To overcome the limits of size shrinking in IoT applications, one solution may be moving to time domain and borrow the highly digital nature of TDC or voltage controlled oscillators (VCO) to resolve analog design hazards. That solves the low supply voltage problem, but also introduces extra conversion structures, which can introduce non-linearity to the system.

1.2. Objectives

This thesis aims to present the design procedure of a new type of ADC for MPPT structure in a PV-PMIC system. The whole PV-PMIC system and the scope of the project is shown in Fig. 1.1. The whole PHEV system consists of a PV-cell, a Charge Pump controlled by the MPPT logic as the DC-DC converter, and a battery that can usually be considered a constant voltage source. The scope of this project is restricted to the design of an ADC that measures the charging current and presents the results to the MPPT logic as digital codes.

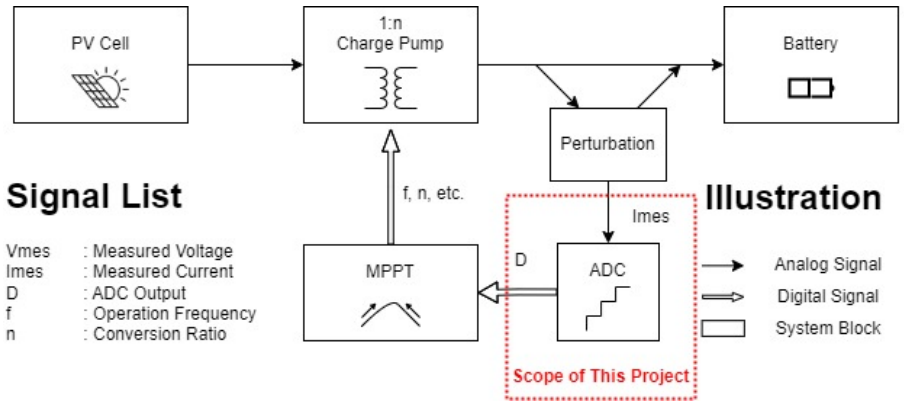


Figure 1.1: System structure and scope of this project.

To achieve the objectives, a literature research should be carried out. The research question is 'Which Analog-to-Digital Conversion techniques are suitable for MPPT in a low-power, small-area chip?'. The expected output of the literature research is the suggestion to the architectures that may be useful to answer the demands. This research will then focus on the key features of the previously proposed architectures instead of the comparison among the architectures.

After the literature research, the design requirements will be introduced and a design will be proposed. The design should take the conclusion of the literature research into account. The design is also expected to bring innovative and applicable thoughts to the required application.

1.3. About this Thesis

This thesis includes several chapters: Chapter 2 will present the results of the literature research. Chapter 3 will present the proposed system and the design methods. Chapter 4 will present the implemented circuits of the proposed system and the simulation results. Finally, Chapter 5 will present the conclusions and discussions.

2

Literature Review

This Literature Review is conducted to answer the research question 'Which Analog-to-Digital Conversion techniques are suitable for MPPT in a low-power, small-area chip?'. The Literature Review will focus on different ADC techniques, including TDC techniques as they are considered special types of ADC in some applications. The major keywords for this literature review are 'ADC' and 'TDC'. The minor keywords are 'Energy Harvester', 'MPPT', 'Low Power', 'Ultra-Low power', 'IoT', and 'PV' to filter low-power and small-area designs. The publication date of the papers found is restricted to the most recent 20 years, except for some design guidelines that explain commonly adopted methodology.

This chapter is divided into four sections: Section 1 provides the necessary background, including the PV cell characteristics and the MPPT algorithms. Section 2 discusses the ADC techniques. Section 3 outlines the TDC techniques. Section 4 compares the properties of the mentioned designs and presents the conclusions.

2.1. Background

To understand the requirements for a measurement structure of PV-PMICs with MPPT algorithms, some background information on PV cell characteristics and MPPT algorithms is necessary. This section is divided into two subsections, explaining the PV cell characteristics and the MPPT algorithms respectively.

2.1.1. PV System Characteristics

The output characteristics of a PV cell can be described as a circuit model shown in Fig. 2.1. The PV cell is also referred to as a photovoltaic harvester (PH). In this circuit, current source $I_{PH,SC}$ represents the short circuit current (SC) that is generated by the PH from the irradiance of the light sources. Rp and Rs represent the shunt and series resistance and model the non-ideality of the PV board. The diode D_{PV} represents the PN junction that forms the base of the PV cell. By solving the circuit, the system characteristics can be derived as follows [5]:

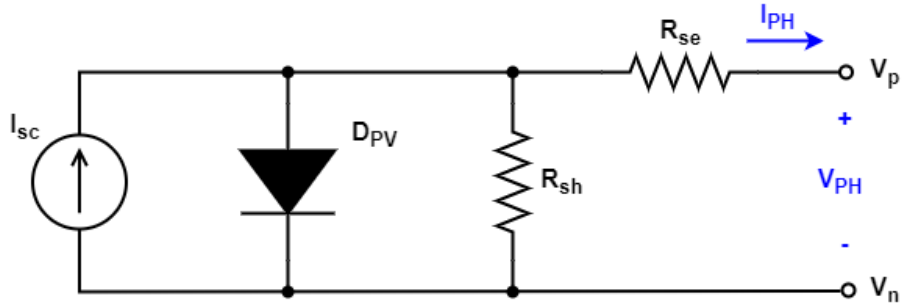


Figure 2.1: Equivalent circuit of PV cell.

$$I_{PH} = I_{PH,SC} - I_{SAT}\{e^{\frac{q}{AKT}(V_{PH}+I_{PH}R_{SE}-1)} - \frac{V_{PH}+I_{PH}R_{SE}}{R_{SH}}\}, \tag{2.1}$$

$$P_{PH} = I_{PH}V_{PH}, \tag{2.2}$$

where q is the unit charge, K is the Boltzmann constant, T is the temperature, R_{SH} and R_{SE} are respectively the shunt and series resistance, and P_{PH}, V_{PH}, and I_{PH} are respectively the output power, output voltage, and output current of the PH. The relationship between P_{PH} or I_{PH} and V_{PH} are respectively shown in Fig. 2.2.

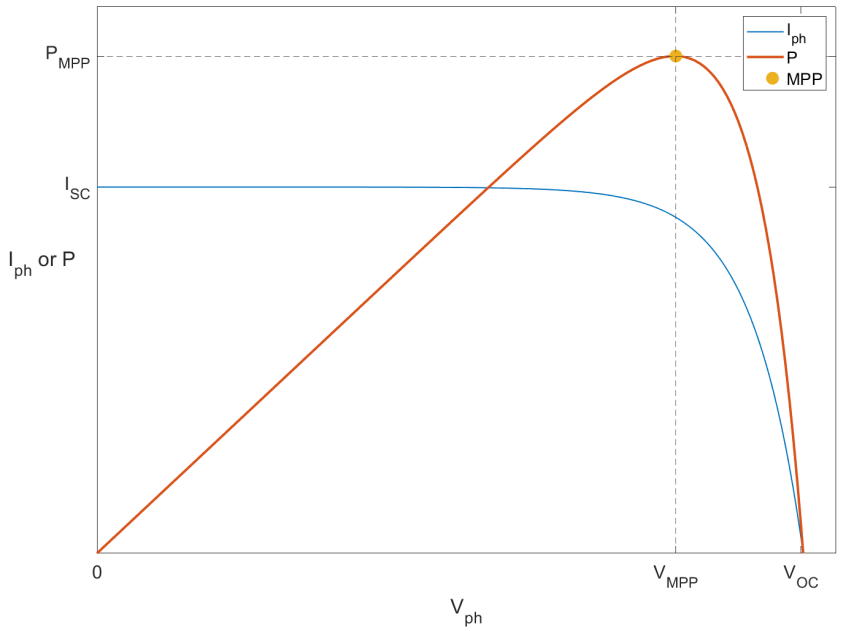


Figure 2.2: PV cell V-I and V-P characteristics.

If the solar irradiance level varies, I_{SC} will increase or decrease accordingly [4], and the power curves will change as shown in Fig. 2.3. It can be observed that the MPP changes, but the relative relationship between the MPP and the irradiance level remains largely the same.

2.1.2. MPPT Algorithms

An MPP exists for a PV cell under certain environmental conditions. For simplicity, we assume that the load does not require protection, so the load current is not expected to have an upper limit. The load is then expected to be charged at the MPP for maximum power efficiency. Due to the different voltages of the loads, the voltage at the PV nodes does not always guarantee the maximum power transfer. To adjust the equivalent voltage of the load seen by the PV cell, a DC-DC converter is inserted between the actual load and the PV cell. The MPPT block is designed to control that DC-DC converter [6].

Fig. 2.4 shows a common equivalent circuit model of a PVEH system. In this circuit model, the PV cells adopt the circuit model shown in Section 2.1.1. The DC-DC converter adopts its equivalent transformer model with a series resistance, which suffices in the quasi-static condition. The DC-DC converter allows digital control to toggle its conversion ratio n and its equivalent resistance Req, The MPPT algorithms include Perturb and Observe (P&O), Incremental Capacitance (IC), Fractional Open Circuit Voltage (FOCV), Fractional Short Circuit Current (FSCC), and so on. The most popular algorithms are P&O and FOCV algorithms. Both require measurement of the system voltage or current, so they both need an ADC as the analog front end.

This section is further divided into two subsections. One subsection covers the P&O algorithm and the other covers the FOCV algorithm.

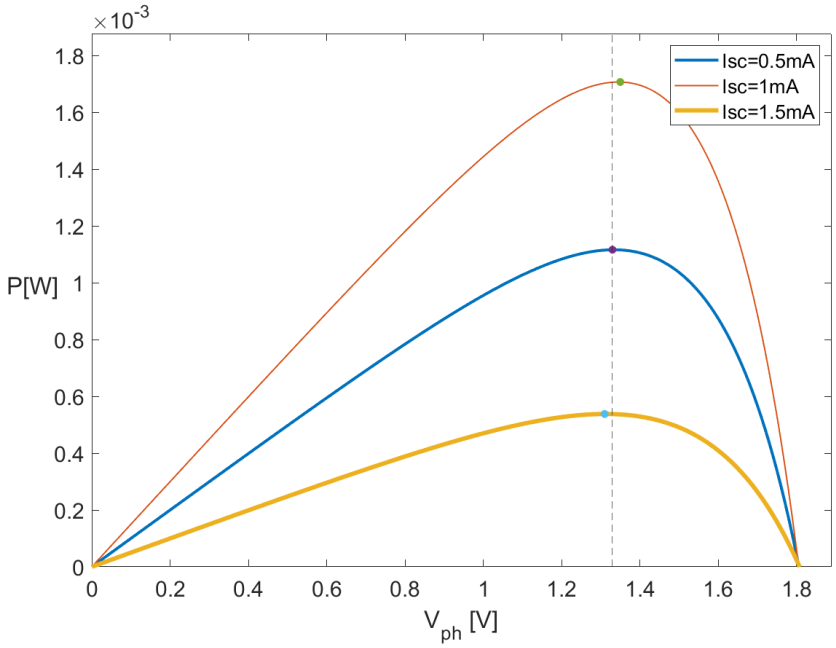


Figure 2.3: P-V curve when irradiance level change.

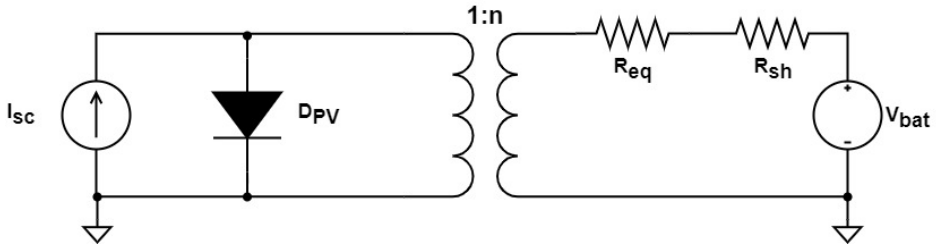


Figure 2.4: Equivalent circuit of power chain.

Perturb and Observe
P&O is a popular MPPT algorithm thanks to the simplicity of the working principle [2]. It works by continuously perturbing the system and acting according to the measurements. The perturbations imply whether the power state at the moment lies on the left side or the right side of the MPP. This decides in which direction the system should move.

In Fig. 2.5, a simple P&O solution is illustrated as an example. This simple algorithm is comparable to the gradient descent algorithm. The perturbation measures $\Delta P/\Delta V$ as an approximation to $\mathrm{d}P/\mathrm{d}V$. To do so, the circuit takes two successive measurements before and after an action to the system, for example, switching the conversion factor of the DC-DC converter. If the action drives the system towards the MPP, the measured power should see an increase and the algorithm continues the previous operation. Otherwise, the measured power should see a decrease and the reverse of the previous action should be taken. When the measured power remains the same, the system reaches the MPP with some degree of confidence and accuracy.

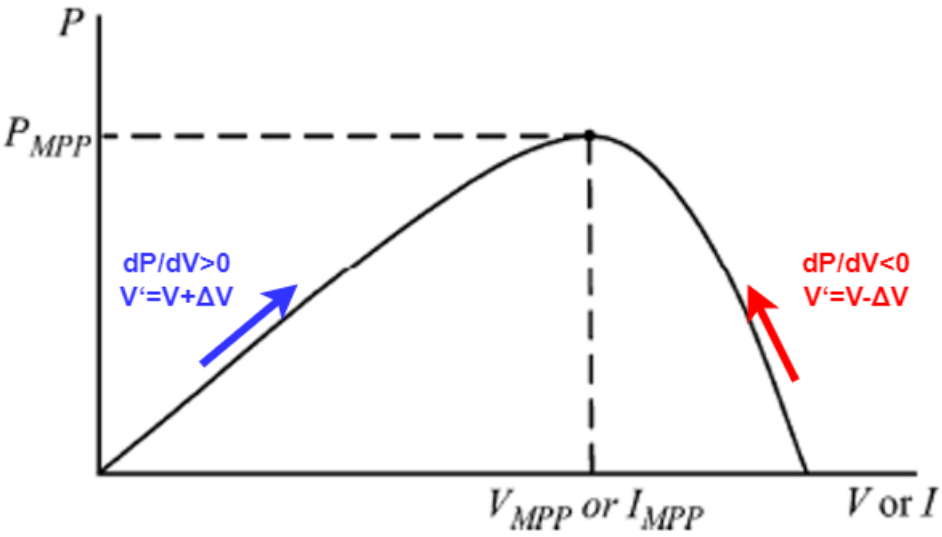


Figure 2.5: P&O algorithm illustrated on a P-V curve.

Fractional Open Circuit Voltage
The FOCV algorithm is based on pre-defined information indicating that the MPP occurs at around a fixed ratio of the open circuit voltage at the PV cell output. Open circuit voltage, or open voltage (OV), is the voltage present when the PV cell nodes are open. According to this algorithm, OV needs to be measured by shortly disconnecting the load from the PV. After that, the load will be reconnected and the PV cell voltage will then be measured. The FOCV algorithm then controls the DC-DC converter so that the PV cell voltage moves towards a pre-defined ratio of the OV. An illustration of this algorithm can be found in Fig. 2.6.

2.1.3. ADC and TDC
MPPT blocks require information about the current or voltage from the PV system. A sensing structure is needed to sense and process current or voltage signals into digital signals. Such structures are called Analog-to-Digital Converters (ADCs). Traditionally, ADC refers only to current- or voltage- to digital converter. In a broad sense, circuits that convert arbitrary time delays into digital codes, known as "Time-to-Digital Converters (TDCs)", are also a type of ADC. In this paper, the former definition will be adopted. An ADC with TDC functioning as a subcircuit will be referred to as an ADC but will be discussed in the TDC chapters regarding its TDC concepts.

Both ADCs and TDCs bridge the analog domain and the digital domain; therefore, they both contain analog components and digital components. Their essential analog components include reference generators and comparators. The reference generator generates discrete references, which can be currents, voltages, or time delays. The comparator(s) compare(s) the input signal with the generated references. The digital circuits include control logic, output code storage, and, if necessary, calibration

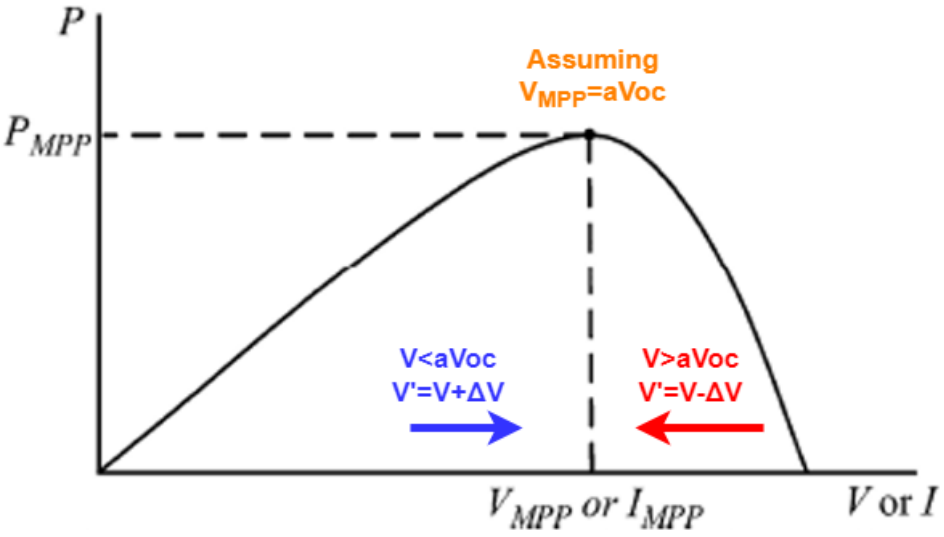


Figure 2.6: FOCV algorithm illustrated on a P-V curve.

logic. Different types of ADCs are distinguished from one another by their comparison logic and the associated analog circuits.

An ADC can operate in the voltage domain, current domain, or time domain. If an ADC operates in the voltage domain, the input signal is converted into a voltage signal and compared against voltage references. The same principle applies to the current domain and time domain. Note that current signals and voltage signals are often converted to each other in circuits, but most designs compare in the voltage domain.

2.2. ADC Architectures

ADCs are used in measurement systems to digitize analog input signals. For MPPT application on small systems, ADCs with small area usage, and low power consumption that operate on demand are favorable [2, 4, 5, 6]. These requirements also overlap with IoT applications [1].

When designing low-power small-area ADC circuits, several challenges arise [1]. First, to reduce the power consumption, either the current or supply voltage needs to be reduced, sometimes both. Reducing current typically decreases the stage gain and reducing supply voltage generally reduces the output swing. Second, to minimize area usage, components in the signal chain, such as resistors and capacitors, need to shrink in size, which results in increased power consumption. Third, in signal processing circuits, smaller components result in larger mismatches. This introduces a larger dynamic offset in the system.

In IoT and MPPT applications, the ADC with a moderate speed and resolution can cover most IoT applications [1]. Therefore, ADC techniques that allow trading conversion speed and resolution for other system specs are favorable. This results in most ADC for IoT applications being Successive Approximation ADCs (SAR-ADC) [1], Flash ADC, and $\Sigma\Delta$-ADC are less applicable because Flash ADC consumes more power and $\Sigma\Delta$-ADC has bad reconfigurability to accomplish low speed, low power demands. They can be used as an enhancement of SAR-ADC, which becomes a mixed type of ADC or pipelined ADC.

Besides traditional types of ADC, new types of ADC such as VCO-based ADC have also been reported [7, 8, 9, 10, 11]. VCO-based ADC introduces oscillator frequency as the middle stage between input voltage or current and output digital codes. Although it toggles the gate delay of the oscillator, its characteristics differ from TDC-based ADC, as the voltage is converted to the pulse frequency instead of a piece of delay. Besides, most VCO-ADC designs adopt analog calibration or noise cancellation to solve design problems such as nonlinearity. Therefore it is discussed separately from TDC designs in this literature research.

This section further discusses popular ADC techniques in low-power small-area applications such as IoT applications. These techniques are SAR-ADC and VCO ADC. After that, a short summary will

present some important conclusions about the SAR-ADC.

2.2.1. SAR-ADC

SAR-ADC is a type of Nyquist rate data converter [1]. The typical structure includes a Digital to Analog Converter (DAC), a comparator, and a logical control, as shown in Fig. 2.7. The DAC creates reference voltage or current, usually voltage. Adding up some of the references can make an approximation of different levels. The comparator will compare the approximation to the input. Successively comparing it to gradually adjusted approximations can make the final approximation close to the input signal, which becomes the digitized result.

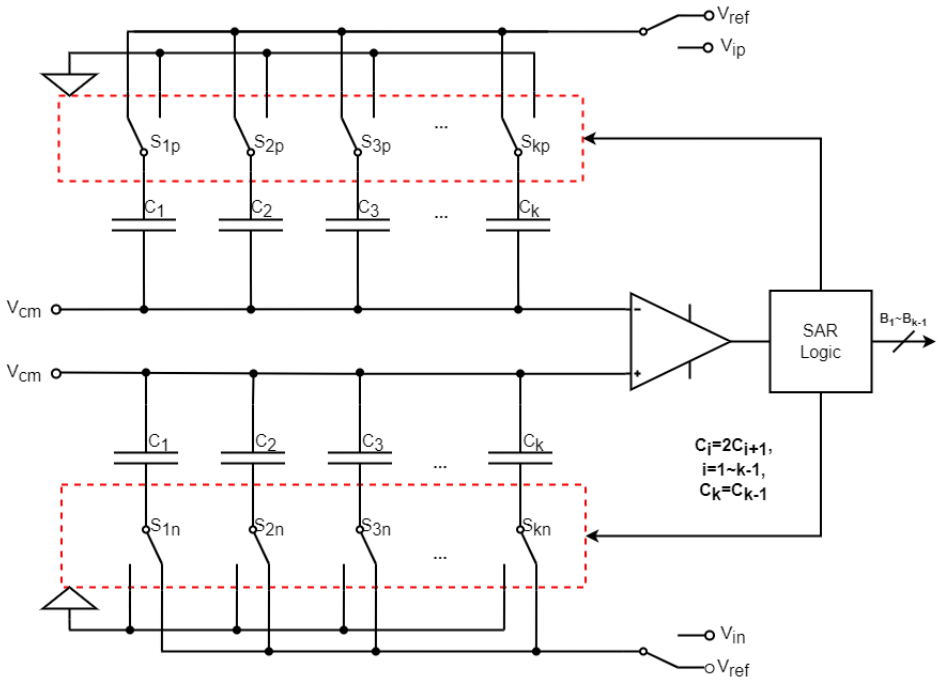


Figure 2.7: Conventional $(k-1)$-bit SAR-ADC. k is a positive integer larger than 2.

SAR-ADC is the most popular ADC architecture thanks to the trade-off between speed and accuracy [1]. The easiness of switching down speed by using components of larger sizes and larger capacitors. From 2014 on, many μW-level SAR-ADC designs have been proposed targeting IoT applications. The improvements include monotonic switching schemes [12, 13, 14, 15, 16], comparators with higher power efficiency, and adjusted weights [17].

The major power loss in SAR-ADC is caused by charging and discharging capacitors. [13] presents a switching scheme that saves up to 87.54% of charging power compared to the conventional switching scheme by monotonic switching scheme. The monotonic switching scheme aims to reuse the charge on large capacitors to charge smaller capacitors. After that, many other designs with improved switching schemes have been proposed targeting power reduction [12, 15, 16]. One of the recent developments is the switching scheme proposed by [14], which further reduces the sampling power loss to 99.22%. This result is near the theoretical maximal power reduction by changing switching schemes [14].

Binary weighting schemes without redundancy make each comparison step critical to digitize correctly. In the presence of PVT variations, the correctness of the Least Significant Bit (LSB) can be severely challenged. One solution is to add redundant bits so that the error rate of that step reduces. Another possible way is by adjusting the weighting to create overlaps between two adjacent steps [17]. This way increases the tolerance of SAR-ADC to the PVT variations.

2.2.2. VCO based ADC

VCO-based ADC has a Voltage Controlled Oscillator (VCO) as the integrator to sample the continuous analog input into time, and then convert the sampled signal to the digital domain [7, 8, 9, 10, 11]. The circuit diagram and the timing diagram are respectively shown in Fig. 2.8 and 2.9. The VCO is made

by a ring of current-starved inverters. The input voltage is connected to the gate of the bias stages so that it can continuously toggle the oscillation frequency of the oscillator. By quantizing the oscillation frequency, the output digital code represents the oscillation frequency and indirectly represents the voltage level during the sampling period. The structure is comparable with a Delay Locked Loop (DLL). DLL structure aims to control the oscillation frequency by controlling the bias voltage of the current source stage with feedback. In VCO-ADC, instead of stabilizing the oscillator frequency, the oscillation frequency is designed to vary to reflect the bias voltage level.

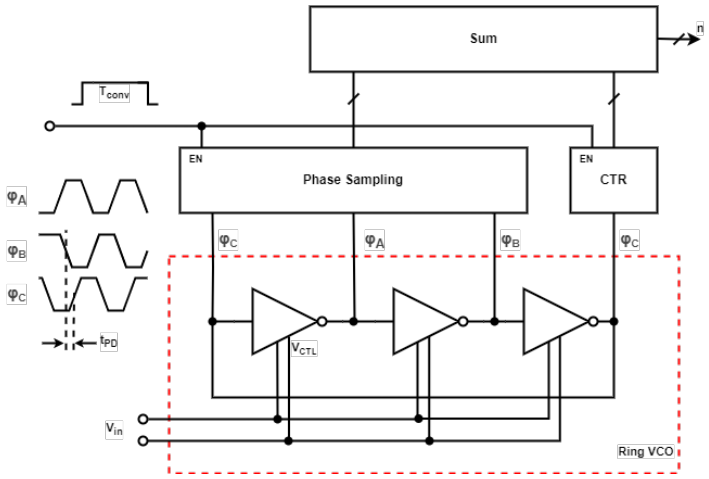


Figure 2.8: Circuit diagram of a VCO ADC [11].

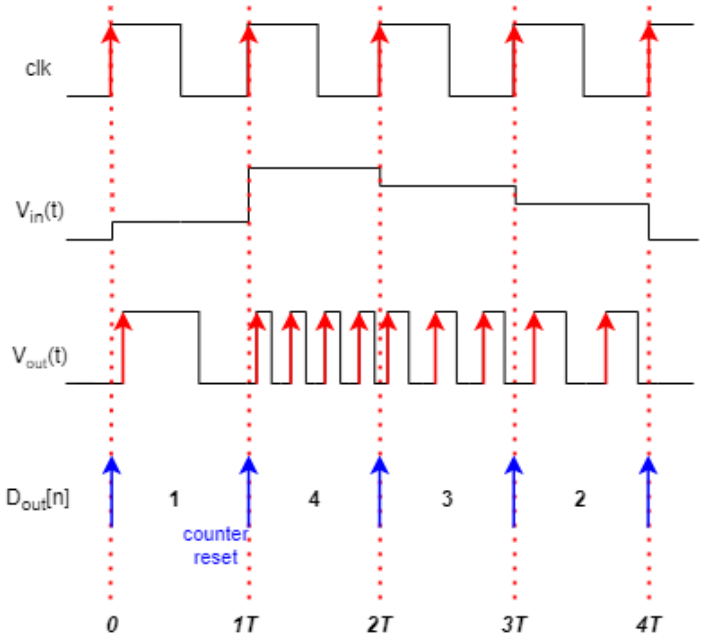


Figure 2.9: Timing diagram of a VCO ADC [7].

The motivation for adopting VCO as a core includes inherent input low-pass filtering, digital nature, and higher reconfigurability than other structures [11]. The inherent low-pass filtering is provided by the continuous input sampling at the input stage, which provides anti-aliasing features. The digital nature refers to the VCO's property, that the voltage at each node is either Vdd or Vgnd. The VCO can enjoy power reduction in advanced CMOS technologies without suffering from analog non-idealities.

The disadvantage of VCO-ADC is nonlinearity [7, 11]. The nonlinearity originates from the nonlinear V-f characteristics, which can be further traced back to the non-linear relationship between the branch

current and the threshold voltage. The system Integral Non-Linearity (INL) depends on the linearity of the VCO core. Therefore, many VCO-ADCs focus on correction using background calibration. Another possible way of correction is noise shaping by sigma-delta modulation.

2.2.3. Summary

The common properties of VCO-ADC and SAR-ADC are taking advantage of longer conversion times to save power in digitization with moderate accuracy. The difference is, SAR-ADC faces the trade-off challenge between area and power while VCO-ADC faces the challenge of linearization.

2.3. TDC Architectures

Thanks to its highly digital nature, TDC benefits more from advancing CMOS technologies than ADC in the voltage or current domain, making it suitable for IoT applications [18]. Besides, the digital nature also has advantages such as a large dynamic range, being low voltage friendly, and the potential for low power consumption.

TDC digitizes a piece of delay time as the input signal, marked by the start and stop event [18, 19, 20]. By converting the voltage or current signal to a delay duration, TDC can also be used to digitize voltage or current signals indirectly. For example, the dual-slope voltage or current measurements are done by sampling voltage on the measurement capacitor or integrating input current on the measurement capacitor, then discharging the capacitor with a fixed current [21]. In this way, the voltage or current is converted into the time duration, which is further digitized into the final result, as shown in Fig. 2.10. In an alternate view, we can consider this system as a TDC with a resolution equal to the clock cycle. This is an example of a trivial solution to digitize the time, but the resolution can be improved. More advanced TDC architecture usually aims at a resolution of the gate delay level or sub-gate delay level [18, 19, 20, 22].

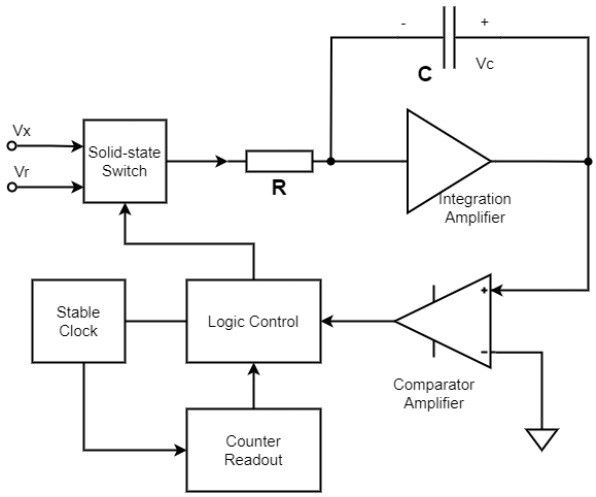


Figure 2.10: Circuit diagram of Dual Slope ADC [21].

There are several reasons that TDC becomes favorable in IoT applications [18, 19, 20]. First, the reference in the time domain is usually generated by delay cells, which are not limited by analog circuits' big enemies such as low supply voltages or insufficient gain.

Second, the operations in the time domain, including comparison, addition, and subtraction, are fully digital. For example, comparing an arbitrary delay (as the input signal) with the reference delay only requires two event detectors, as shown in Fig. 2.11. The input delay is presented by a leading signal edge 'A' in one wire as the start, and a lagging signal edge in another wire 'B' as the end. To compare the input delay and the reference delay, the circuit makes the starting edge go through the reference delay, and observes if it arrives before the ending edge, which does not go through any delay. If the delayed starting edge wins, it can be said that the reference delay is shorter than the input delay. Otherwise, if the ending edge wins, the reference delay is longer. Additionally, addition or subtraction by an amount of time can also be performed by adding an extra reference delay to the branch 'B' or 'A,' respectively. The accuracy of the resulting signal delay only depends on the accuracy of the signal

propagation delays, which are characterized by digital properties. Therefore, the analog non-idealities such as non-linearity caused by low supply voltage or current can be reduced, which makes it potentially suitable for low-power designs. However, the resolution is challenged by digital uncertainties, such as unwanted delays and jitters.

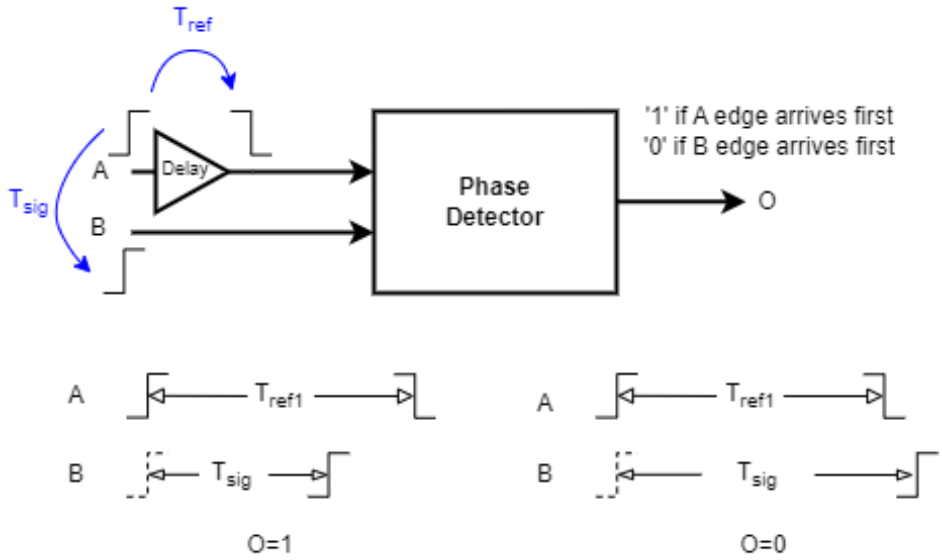


Figure 2.11: Comparison mechanism in TDC.

Third, the dynamic range of TDC is high and free from power consumption limits. In any circuit, the voltage of a node or current in a branch has an upper limit due to material properties. Besides, the voltage or current resolution is limited by the noise in the circuits. But in the time domain, waiting for a time as long as possible does not cause any circuit failure, and the resolution is fine enough compared to the long waiting time. Therefore, the upper limit of the TDC is only set by the circuit, such as the maximum of the counter or the number of delay cells in the delay line. What's more, if the TDC is designed with a delay ring, the limits created by the number of delay cells also disappear (see Section 2.3.3). The negative side effect of waiting for a long time is the increased sampling period or reduced sampling rate. Therefore, TDC is more beneficial for applications with large DR requirements and low sampling rate requirements.

The TDC Architectures include Delay-Line TDC (DL-TDC), Vernier TDC (Vernier TDC), Gated Ring-Oscillator Based TDC (GRO-TDC) [23], Vernier Ring Oscillator based TDC (Vernier RO-TDC) [24], Successive Approximation TDC (SA-TDC), Sigma Delta TDC ($\Sigma\Delta$-TDC), and Stochastic TDC [18, 19, 20]. Among these architectures, Delay-Line-based TDC is usually referred to as the comparison reference, and other architectures are compared in terms of resolution and dependency on mismatches due to PVT. It is not possible to introduce all the structures exhaustively. In this literature research, the TDC architectures with moderate accuracy and relatively simple structure are selected, which are DL-TDC, Vernier TDC, GRO-TDC, and SA-TDC.

For the rest of this section, different TDC architectures will be introduced and discussed. First, Delay Line TDC and general design considerations will be introduced and discussed. After that, three more advanced architectures, namely Vernier TDC, GRO-TDC, and SA-TDC will be introduced by three different. Finally, a summary of TDC architectures will be drawn.

2.3.1. Delay Line TDC

Delay Line TDC (DL-TDC) is also called Flash TDC because it compares the input delay with different references in a single iteration [18]. As shown in Fig. 2.12. The structure contains a delay line and a series of registers. The start signal is sent to the delay line and passes through each delay cell sequentially, and passed delay cells are recorded by the registers. After a certain duration of time, the end signal freezes the state of all registers and the readout starts. The output of all registers forms a thermometer code. After a thermometer to binary converter, the binary output is ready and measurement is complete [18,

19].

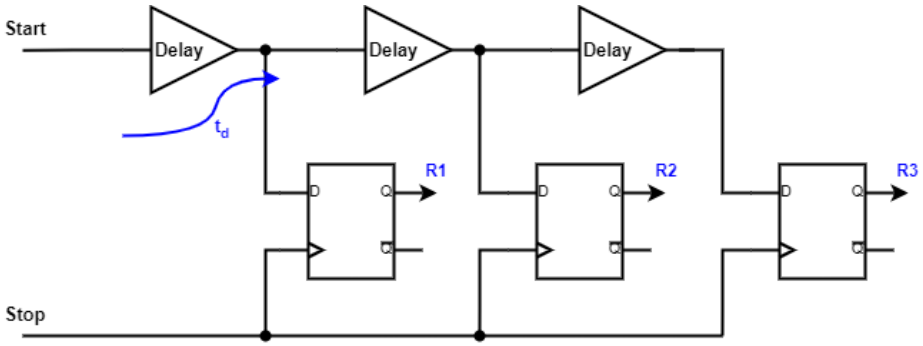


Figure 2.12: Circuit diagram of DL-TDC [19].

The resolution limit of DL-TDC is the gate delay, which is decided by the CMOS technology [18, 19]. Besides, the matching among the gates is another limit factor of the resolution, because the influence of mismatch increases as the device size shrinks. The resolution and mismatch are typical trade-off considerations of all TDC structures [18, 19].

Another point of design is the choice between the sequential structure and the ring structure. To reach a higher dynamic range, the delay line can be connected head to tail as a ring, causing the signal to keep circulating in the ring before the end event arrives. Such a structure is also called a Ring Oscillator-based TDC (RO-TDC). Forming a ring introduces the risk of cumulative jitters because the same delay element is reused in each cycle [22].

2.3.2. Vernier TDC

Vernier TDC is a TDC type with two delay chains, one of which is faster than the other [18]. At the beginning of a measurement, the start signal is sent to the slower chain. The general structure is shown in Fig. 2.13. After a certain duration of time, the end signal is sent to the faster chain. When the end signal passes through each stage, it gradually catches up with the starting signal and causes a phase flip. The final result is generated in a similar way to DL-TDC, which represents the number of stages before the flip happens.

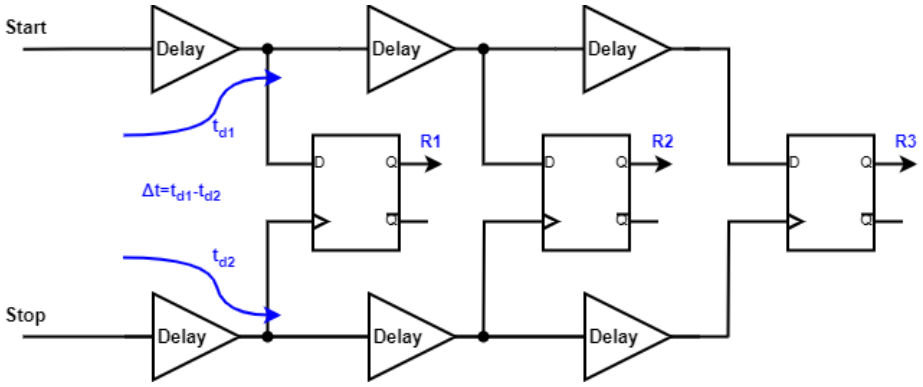


Figure 2.13: Circuit diagram of Vernier TDC [19].

As an improvement compared with DL-TDC, Vernier TDC has a higher resolution than DL-TDC because Vernier TDC's quantization unit is the difference between the fast and slow gate delay [18, 19]. The resolution surpasses the gate delay limit.

The additional delay line also causes side effects. First, compared to DL-TDC, Vernier TDC is more prone to mismatch [18, 19]. One reason is the resolution is higher than DL-TDC. Since there are two delay lines, the required matching between each delay cell becomes the matching between the difference of each stage of two delay cells, which is more challenging. Second, Venier TDC consumes more power compared to DL-TDC due to the additional delay line.

Vernier TDC can also use the ring structure. The benefits and challenges of doing so are similar to DL-TDC.

2.3.3. Gated Ring Oscillator based TDC

Gated Ring Oscillator-based TDC contains a Gated Ring Oscillator as the digitization core. The start event will circulate in the GRO waiting for the end signal, as shown in Fig. 2.14. When the end event comes, the gate will turn down the GRO so that the state in GRO freezes. The result is then the number of cycles the start signal has passed plus the residual represented by the phase in GRO. After one measurement, the next measurement can start by de-freezing the GRO so that the signal further circulates in the GRO [25]. Similarly, GRO-based TDC can also have either a single delay loop or a Vernier structure [24].

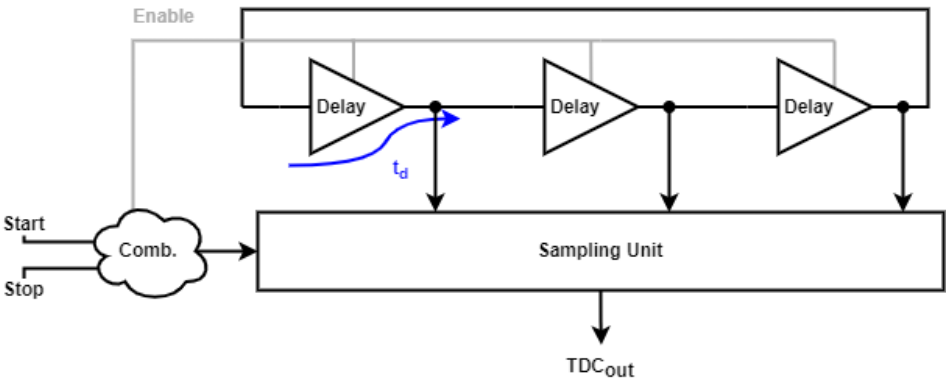


Figure 2.14: Circuit diagram of GRO-TDC [19].

One advantage of GRO-TDC is that the DR is no longer limited by the number of delay elements. If the GROTDC starts to operate and the stop signal does not come, the oscillation in the delay ring will not naturally stop, unlike in DL-TDC. Therefore, the DR of such a system is only limited by the counter capability. However, the counting logic is also more complex compared to DL-TDC because of the recurring transitions.

Besides the advantage in DR, the biggest advantage of GRO-based TDC is the inherent noise cancellation [25]. This is because, in a set of successive measurements, the starting node is randomly decided by the duration and the starting node of the last measurement. Therefore, the delay sequence that will be used is sufficiently random, which avoids a fixed sequence of delay cells creating offset errors in the measurement. As a result, GRO-TDC does not require calibration of each delay cell to achieve high linearity and resolution but only demands the calibration of the overall gain [18]. Another advantage compared to DL-TDC is the reduced number of phases during read-out. In DL-TDC or Vernier TDC, reading out requires each gate to pass through the decoder, while for GRO-TDC, the rough result is already stored in the cycle counter and the fine result contains fewer bits.

One disadvantage of GRO-TDC is that it requires several successive measurements to profit from the operation [22]. After a long freezing time, the phase information may be lost due to quiescent leakage. To restart the measurement, the system needs to start with a dedicated start pin, which causes the inherent noise cancellation to disappear.

2.3.4. Successive Approximation TDC

SA-TDC is a new TDC architecture compared to other architectures [20]. SA-TDC has a similar working principle to SAR-ADC, which approximates the input time duration with different reference delays. Just as SAR-ADC compares and swaps the reference correspondingly, SA-TDC also requires a time comparator and time reference. It can be further divided into Cyclic Successive Approximation TDC (CSA-TDC) and Linear Successive Approximation TDC (LSA-TDC). However, they share the same algorithm, therefore it can be explained with a single timing diagram.

Fig. 2.15 illustrates the concepts in CSA-TDC. The CSA-TDC circuits can be described in Fig. 2.15a, and the algorithms can be described in Fig. 2.15b. The two ports, 'Start' and 'Stop' are the inputs for the

starting signal and the ending signal. The starting signal will first arrive at node A, then go to the Digital to Time Converter (DTC), which creates reference delays and is controlled by the logic block 'Arbiter and Selector'. When arrived at node A', it will be forwarded back to the input port and start another cycle. The same applies to the ending signal, which follows B and B', and then goes back to the input port.

Fig. 2.15c explains how results are generated with the cycling of two signals. In Fig. 2.15c, t_{sig} represents the input delay signal and $t_{sig} = (9/32)FS$, where FS represents the full scale of the TDC. A, B, A' and B' are the ports where the event happens and the bracket with a number represents how many times an event has occurred in those ports. t_{ref1},...,t_{ref4} represent the reference delays created by the DTC. LSB is the Least Significant Bit, and $LSB = t_{ref4}$ in this case. t_{ref} should follow a binary distribution, which means

$$t_{ref,k} = \frac{1}{2^k} FS, \tag{2.3}$$

where $k = 1, 2, ..., n$ and $t_{ref,k}$ is the k-th largest reference delay. As time passes, the signals will arrive in B, A', and B' ports, and those arrivals indicate the relationship between the combination of delays to be compared. For example, at the moment of an event in B, the algorithm can tell that t_{sig} must be shorter than t_{ref1}, otherwise A' would have arrived first. Therefore it decides $D[0] = 0$, which is the most siginificant bit (MSB). Similar decisions happen when A' and B' receive events. The comparison results form the second column in Fig. 2.15c. By applying Equation 2.3 to the second column, we can obtain the third column 'Bineary Implication', which motivates the results of each output bit. Finally, the output $D = 01000$ is obtained, or in decimal $D = 16$.

The same algorithm can be made in sequential form to reduce timing violation and power consumption by optimizing each stage [26]. The structure is referred to as SA-TDC, but to distinguish it from CSA-TDC, it can also be called LSA-TDC. The word 'linear' in LSA-TDC indicates that the blocks are connected in a line. Fig. 2.16 shows the general structure. In LSA-TDC, the reference delay of each stage is fixed to $t_{ref,k} = (1/2^k)FS$, where k is the order number of the stage. The phase detector detects whether A or B arrives first. When A arrives first, the stage will make the decision $D[k] = 1$, and forward the combination A' and B to the next stage. Otherwise, it will decide $D[k] = 0$ and forward B' and A. In either case, the leading edge will be delayed by an amount of $t_{ref,k}$ while the lagging edge remains, which is equivalent to adding $t_{ref,k}$ to the opposite side of the compared quantities as in Fig. 2.15c. Therefore, its algorithm and operations are equivalent to those shown in Fig. 2.15c.

As for disadvantages, SA-TDC shares a similar matching problem with other techniques. Besides, as a property of successive approximation algorithms, the decisions of MSBs are critical because a wrong bit can shadow all bits with smaller weights, creating quantization errors that are more than 1 LSB. However, SA-TDC and CSA-TDC have unique advantages, which include the possibility of creating redundancy by non-linear segmentation. Besides, the SA-TDC and CSA-TDC accept various time reference generation mechanisms [18], therefore they are more suitable for taking advantage of new delay generation techniques or integrating with other techniques. For example, to achieve better resolution, Cyclic Vernier TDC can be added to the CSA-TDC structure without adding more delay lines [27].

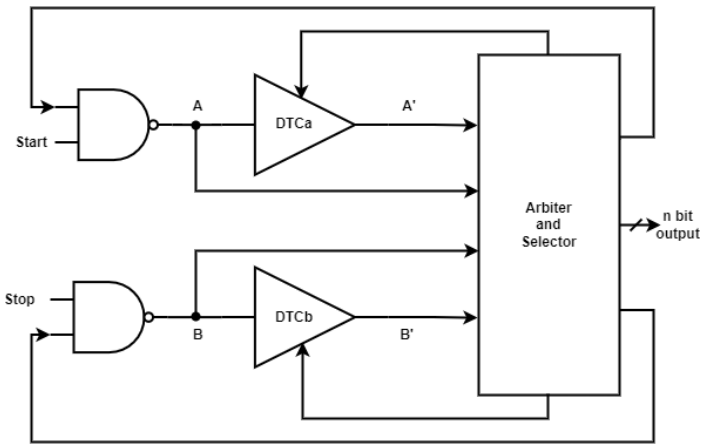
2.3.5. Summary

The TDC architectures are suitable for IoT applications thanks to the highly digital properties of time digitization. The reference generator in general can be characterized into two types: single delay lines, or vernier structure. The other differences lie in ring forming, gated cells, and algorithms.

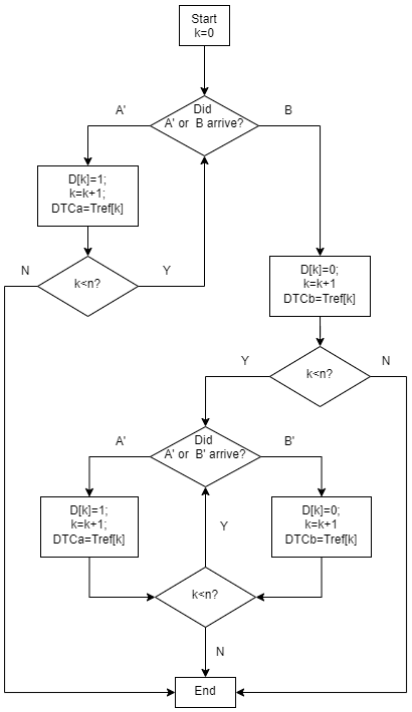
The most important trade-off in TDC is the area/power vs sensitivity to mismatches. When the resolution becomes smaller than the gate delay, the sensitivity to mismatch naturally increases. To meet the system performance demands, a balance should be found between mismatch compensation and power consumption. Because the gate delay is strongly dependent on PVT, calibration is usually required for TDC.

2.4. Conclusion

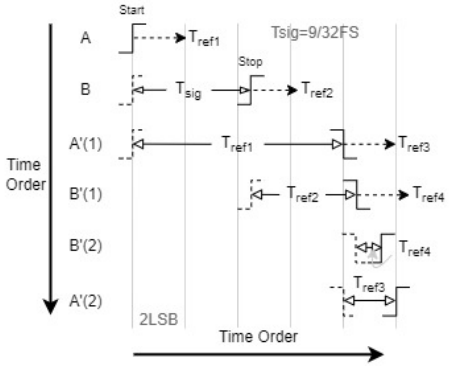
The literature research reviews different ADC techniques including TDC-based techniques. Given the requirements of low bandwidth, small area, and low power consumption, SAR-ADC, VCO-ADC, and TDC each address these requirements in different ways. For techniques that do not involve time-domain signaling, SAR-ADC is the most suitable. Additionally, VCO-ADC and TDC techniques are gaining



(a) Circuit diagram of CSA-TDC [20].



(b) Algorithm of CSA-TDC.



Event	Comparison Result	Binary Implication	Output
B arrived	Tsig<Tref1	Tsig<1/2 FS	D[0]=0
Ad arrived	Tsig+Tref2>Tref1	Tsig>1/4 FS (and Tsig<2/4FS)	D[1]=1
Bd arrived	Tsig+Tref2<Tref1+Tref3	Tsig<3/8 FS (and Tsig>2/8FS)	D[2]=0
Bd arrived	Tsig+Tref2+Tref4<Tref1+Tref3	Tsig<5/16 FS (and Tsig>4/16FS)	D[3]=0

Ad arrived, but the operation was terminated after obtaining D[3].

(c) Timing diagram of 4-bit CSA-TDC. D[0] is the MSB.

Figure 2.15: CSA-TDC principles.

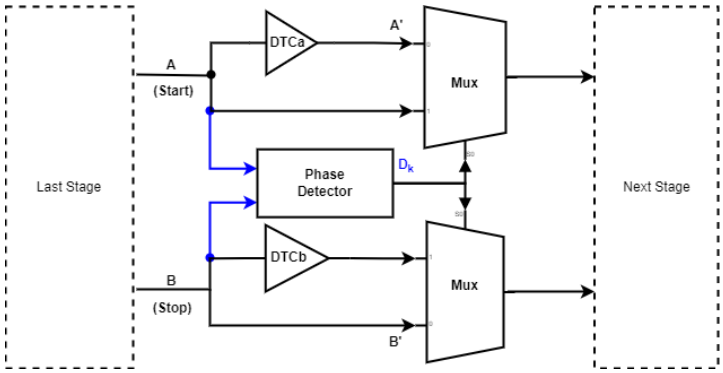


Figure 2.16: Circuit diagram of LSA-TDC [26].

attention due to the ease of referencing and comparing in the time domain. VCO-ADC reduces power consumption and does not require an additional conversion structure, but it suffers from nonlinearity issues. TDC has good accuracy and high DR but needs an additional conversion structure to measure voltage or current. Among TDC techniques, the major consideration is the trade-off between resolution and power consumption due to mismatch compensation, which can be achieved in moderate resolution design.

3

System Design

In this chapter, the proposed design is presented at the system level, including the design process and some considerations at the circuit level design. The reasoning follows the order of the design workflow. First, the definition of each part of the proposed system will be detailed. Then, the system level design of each part will be proposed and discussed. Finally, the proposed system will be implemented with MatLab coding to verify its behavior. Each section below corresponds to one of these topics.

3.1. System Definition

The scope of this project is defined as an ADC for MPPT application in a PV-PMIC system. To avoid being overwhelmed by possibilities, it is necessary to define the input and output at an early stage. By defining the input and output, several choices can already be made. This section will present the adopted choices.

3.1.1. Input Signal

In the given PV-PMIC system, the MPPT application requires information about the average charging power in a fixed duration of time after the start signal of a measurement. The average charging power is determined by $P_{charge} = V_{load}I_{load}$. Because V_{load} has a DC-like nature and remains relatively stable, it can be considered constant. The indicator of power is then I_{load}, which is the average current of the measurement duration. I_{load} is defined as the input signal of the whole chain.

The input I_{load} range is defined to be from 1.5 µA to 15 mA, including the boundaries. In practice, for a single device, the required range for the measurement is only a small part of the whole system. Therefore, the resolution requirements are not uniformly defined for the whole input range because MPPT senses changes relative to the input current level. Instead, the input range can be divided into different segments, and each segment needs to achieve a pre-defined resolution. The resolution requirements are introduced in Table 3.1, which are derived from the ENOB requirements introduced later. In other words, the ADC gain depends on in which zone I_{load} lies, and within each zone, the resolution needs to be uniform, and the system will be compared against conventional ADCs.

Table 3.1: Table of resolution requirements.

Input Range Number	Range	Resolution
1	1.5 µA – 15 µA	0.84 µA
2	15 µA – 150 µA	8.4 µA
3	150 µA – 1.5 mA	84 µA
4	1.5 mA – 15 mA	0.84 mA

3.1.2. Output Signal

The output signal is a digital code q_{out} that represents I_{load}. q_{out} is a binary quantity but can be expressed as an integer.

q_{out} needs to meet several accuracy requirements: First, the whole system needs to achieve 6-bit accuracy. This accuracy requirement is not the Effective Number of Bits (ENOB) because the logrithmic sub-range division scheme makes each range having different scales with each other. However, as the whole range is subdivided into 4 regions and coded using 2 bits, the resolution requirement becomes ENOB=4 for each sub-range. Table 3.1 lists the corresponding resolution requirement in each range.

To ensure ENOB=4, a common practice is to overdesign the ADC with one or two additional bits. In this thesis, the actual number of bits is chosen to be 5-bit.

In addition, the system needs to present in which range the current is at the moment. This only requires the range selector to report its state, which is not difficult to implement.

3.1.3. Other Specifications

There are several specifications for the ADC structure, namely minimum sampling frequency, area usage, and power consumption. These will be explained in the next chapter, which covers the implementation details. In general, both area usage and power consumption need to be minimized. In parallel with that, designs with a higher proportion of digital circuits are preferred.

3.2. Proposed System

The proposed system consists of the Current Sampler and the Non-Linearity Canceling TDC (NLCTDC). This section introduces the design choices around each sub-circuit.

3.2.1. Current Sampler

The system shown in Fig. 3.1 is the proposed current sampler. To simplify the design, the input current is assumed to be a 1:1 copy of the actual load current modeled by a DC current source. The input current I_{load} is sampled with a capacitor C_{samp}. The capacitor will then be charged to a reference voltage V_{ref}, and the charging duration T_{sig} varies with the time-based average value of I_{load}. T_{sig} is then marked by two events in the digital domain. One is the start signal from the integration control, and the other is the stop signal from the comparator. The transfer function from I_{load} and T_{sig} is as follows:

$$T_{sig} = \frac{C_{samp} V_{ref}}{I_{load}}. \tag{3.1}$$

The system requires a division scheme to address the very large input range. The implementation of the division scheme shown in Tab. 3.1 is also shown in Fig. 3.1. It contains a capacitor array with 4 capacitors and several switches. The 4 capacitors have different sizes. The three larger capacitors, namely $C1$, $C2$, and $C3$, are respectively 900, 90, and 9 times as large as the smallest capacitor, $C0$. For the smallest subrange, the smallest capacitor is switched on and the others are switched off. To switch to the next subrange, the next smallest is also switched on so that the total capacitance is $(9 + 1) = 10$ times the smallest one, making the detection range 10 times that of the smallest range. More details about the circuit implementation can be found in Chapter 4.

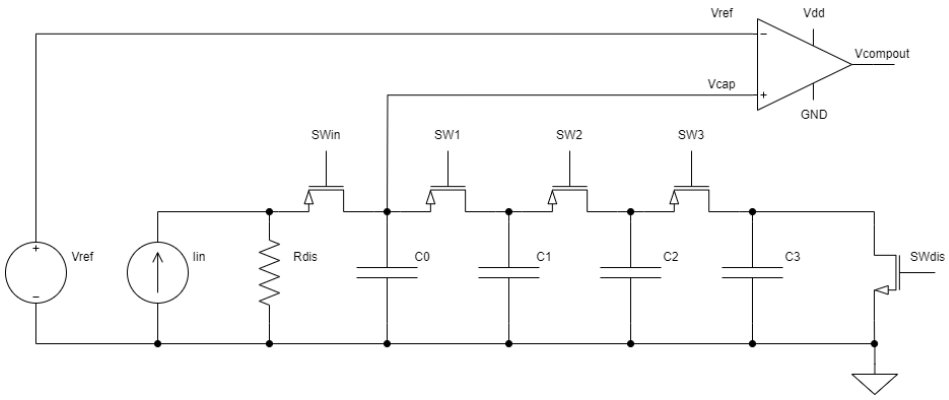


Figure 3.1: Circuit diagram of current sampler.

The major benefit of this implementation is that the capacitor works as an integrator to the input

current, which inherently provides a first-order noise-shaping effect. The averaging effect also reduces the impact of high frequency noise in DC measurement.

This implementation also brings some disadvantages. One disadvantage is the long conversion time, which is acceptable according to the system requirements. Another disadvantage is the non-linear mapping between T_{sig} and I_{load}, as can bee seen from Equation 3.1. The non-linearity is further elaborated in Subscetion 3.2.2.

3.2.2. Non-Linearity Canceling TDC

As mentioned in Subsection 3.2.1, the *i-t* mapping shows an inversely proportional relationship or hyperbolic relationship. This is considered the fundamental non-linearity, which is the main factor preventing the use of a linear TDC in the proposed application. To solve this problem, this project aims to use a special type of TDC to fit this application.

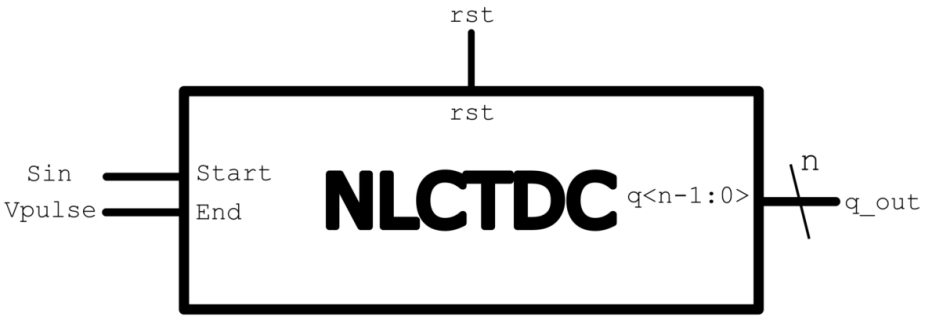


Figure 3.2: NLCTDC model.

The proposed TDC is named Non-Linearity Canceling TDC (NLC-TDC) represented by the black box model shown in Fig. 3.2. As a general requirement, the logic is connected to the reset signal 'rst'. The input of the NLCTDC is the delay signal T_{sig} represented by the delay between two rising edges, T_{start} and T_{end}. The two signals are sent to the ports 'Start' and 'End', respectively. T_{start} is the moment that the switch 'Sin' is connected and T_{end} is the moment that the voltage at the V_{pulse} port reaches 'high'. The output of NLCTDC is the binary quantity q_{out} from ports q<n:0> that reflects the input signal I_{load} in a linear way. Besides, the NLCTDC is also supposed to communicate with the current sampler control logic to share the necessary signals. The current sampler control logic is omitted for now and will be discussed in Chapter 4.

The NLCTDC is a non-linear TDC by itself, but its behavior is the inverse function to the non-linear behavior of the sampler so that the input current is converted to final codes in a linear manner. Moreover, it is a highly digital circuit that contains no analog circuits. This is the most important part of this thesis, which requires a detailed explanation of various aspects, such as the aim of the structure, the expected behavior, and then the circuit implementation. Therefore, Section 3.3 will introduce the aim and the expected behavior, and Section 3.4 will present the verification results of the effectiveness of the introduced behaviour.

3.3. Explanation to NLCTDC

The NLCTDC is designed to compensate for the non-linearity of the current sampler. To design the NLCTDC properly, the non-linearity of the current sampler needs to be analyzed. This section will begin with a short mathematical analysis of the non-linearity. Then, the non-linearity will be illustrated in three hypothetical systems. Finally, the pattern of the non-linearity will be concluded.

3.3.1. Non-linearity Analysis

To help with the discussion around the non-linearity in the Current Sampler, let's define some terms regarding the relevant concepts as listed below.

The first list contains definitions in $i - t$ space, which closely relates to the current sampler curve.

- i: The current variable, equivalent to the numerical value of I_{load}, and $i \in [0, \infty) \cap \mathbb{R}$.

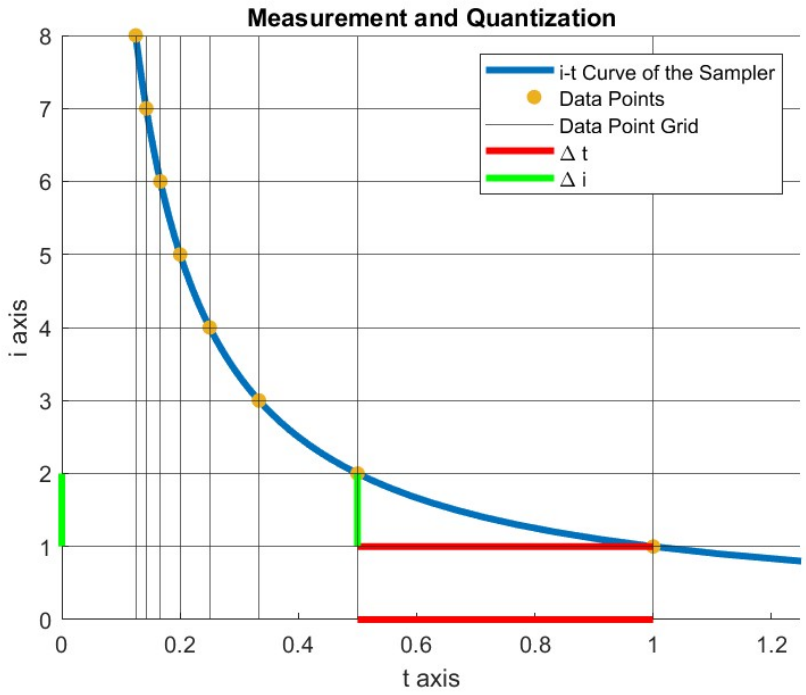


Figure 3.3: Concept illustration. The 'Data Points' represent the decision boundaries of the quantizer. The grid density illustrates the uniformity of Δi and Δt.

- t: The time variable, equivalent to the numerical value of T_{sig}, and $t \in [0, \infty) \cap \mathbb{R}$.
- $i = f(t)$: The characteristic curve representing the Current Sampler. f is the mapping between i and t and is defined as $f(t) = k_1/t$, where k_1 is constant, equivalent to the numerical value of $C_{samp}V_{ref}$, and $k_1 \in [0, \infty) \cap \mathbb{R}$.

The second list contains definitions related to quantization concepts in $i - t$ space.

- p: the decision boundary points in $i - t$ plane. $p = (i, t)$.
- N: The number of bits of the current quantizer, which is a constant. It decides how many boundary points will be needed.
- M: The number of quantization steps. $M = 2^N$. Note the number of decision boundaries is $M - 1$ instead of M. Therefore, k is bounded as $k \in [0, (M-1) - 1]$ or $k \in [0, M - 2]$.
- Δi: The quantization step in I axis, which is constant. $\Delta i = i_k - i_{k+1}$.
- Δt_k The quantization step in T axis, which is dependent on k. $\Delta t_k = t_{k+1} - t_k$. Note Δt adopts the opposite step direction to Δi in order to keep both quantities positive.

The third list contains definitions related to quantization results.

- q: The final quantization result of i, a non-negative integer. Ideally, $q = [i/\Delta i]$, where '[]' represents rounding to the nearest integer.
- p_q: The decision boundary points in $i - q$ plane. $p = (i, q)$.
- q_t: The quantization result of t, a non-negative integer. For later narrates, there are both situations where $q_t = q$ and situations where $q_t \neq q$ but q_t is mapped to q. But q_t strictly follows $q_t = [\frac{t}{\Delta t}]$.
- $q = f_q(t)$: The quantization curve that maps t and q.
- $q = f(q_t)$: The mapping between q and q_t. This function is an equivalent but alternative representation of $q = f_q(t)$.

In the following subsections, three hypothetical systems will be presented as examples to illustrate problems caused by the mentioned non-linearity and the motivation of the proposed method.

3.3.2. The First Hypothetical System

To study non-linearity of the current sampler, linearity needs to be studied first. According to the definition, the decision boundaries of a linear ADC are equally spaced at both the input side and the output side. If those boundaries are plotted in $i - q$ plane, as shown in Fig. 3.4, it can be observed that all boundary points $p_q = (i, q)$ are well aligned in a line. In that case, all the distances between two adjacent i values of those p are equal, or we can say Δi is constant.

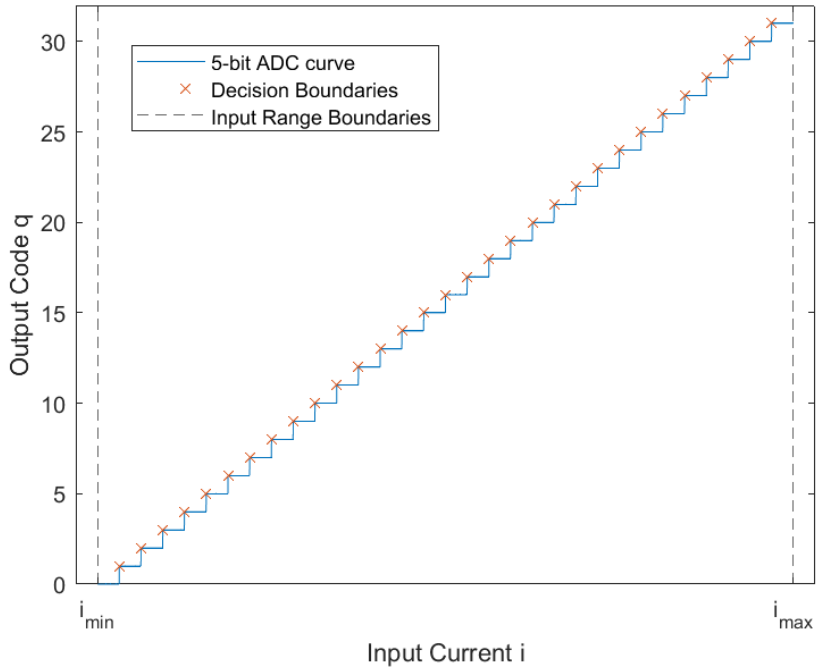


Figure 3.4: Ideal 5-bit ADC.

It can be seen that the decision boundaries can be used as a linearity indicator. This conclusion also applies to the system with a current sampler in different domains. The current sampler converts current into time delays, and therefore, it is a conversion from i domain to t domain. Fig. 3.3 shows the decision boundaries with Δi is constant and mapped to t domain with the non-linear sampler curve. The time steps Δt between two adjacent t points are not uniform. The mapping from uniform i to non-uniform t is a property of a non-linear curve, in this case,

$$i = f(t) = k_1/t. \tag{3.2}$$

One idea to compensate for the non-linearity can be overdesigning the TDC with extra bits, so $q = f_q(t) = [t/\Delta t]$, where Δt is defined by the number of bits of the TDC. In that case, a linear $t - q$ mapping is created similar to an ideal ADC with extra bits. To verify this idea, a hypothetical N-bit linear TDC can be applied to the proposed non-linear current sampler system, where N is larger than 5. The system is successful if it is comparable to a conventional 5-bit ADC with current input.

To showcase this idea, the input current is set to $i \in [1/32, 1]$, where '[]' represents an interval including both boundaries, and the quantization step Δi of the ideal 5-bit ADC is set as $1/32$. For the TDC system, the corresponding t range can be calculated with $t = k_1/i$. For simlicity, we set $k_1 = 1$, resulting in $t \in [1, 32]$. To enable enough time resolution, we use a 9-bit TDC. The quantization step of the TDC system is then $\Delta t = (1/2^9) \times 32 = 1/2^4 = 1/16$. After time quantization, the system outputs $q = q_t$ directly. The result is represented by the $i - q$ plot of the two systems, as shown in Fig. 3.5.

The $i - q$ plot in Fig. 3.5 shows that the hypothetical system with a TDC is unusable because of the resolution loss in its largest i step. Meanwhile, it is also non-linear because the shown shape of a hyperbole differs too much from a line. Therefore, this method is not a good solution to the problem.

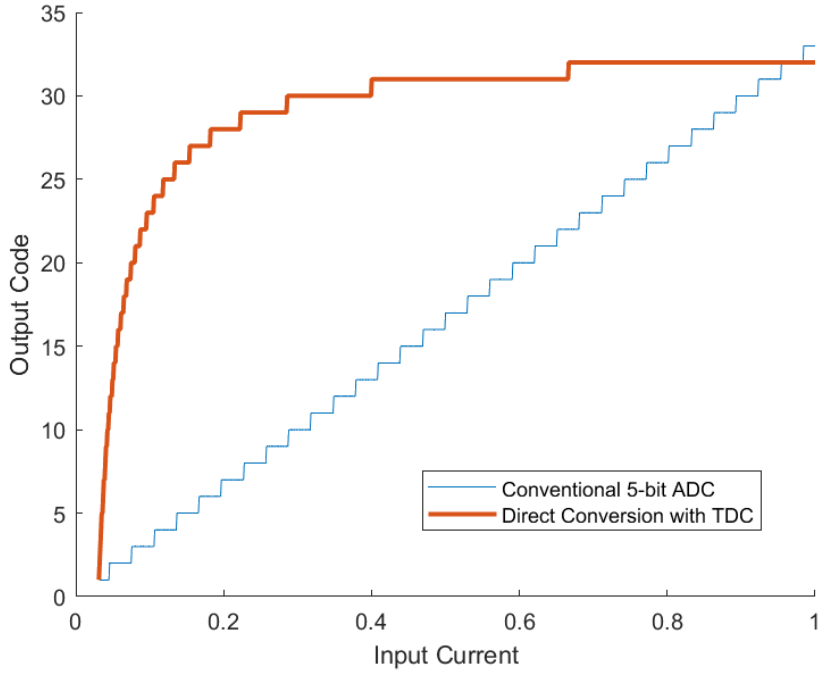


Figure 3.5: Direct TDC quantization. The TDC curve has a hyperbolic shape. The linearity is completely lost.

3.3.3. The Second Hypothetical System

To restore the linearity, adding a divider after the 9-bit linear TDC may be suggested. Then, all the properties mentioned above still hold, but the obtained t_q will be further processed with a hypothetical ideal divider with N_d bit output, where N_d is an arbitrary number to our choice. For now, we can assume that the number of bits exceeds our need, so the division can be made very fine. The divider takes $k_2 = 1$ as the dividend to match the previous choice of $k_1 = 1$, q_t as the divisor and the quotient is q, so that $i_q = [k_2/q_t]$. Note that the value of k_2 does not decide the division resolution. Instead, the number of bits of q, denoted as N_d, decides the division resolution, so we need to suppose N_d is very large to simplify the discussion. In practice, the divider output has finite resolution because the quotient needs to be presented in a finite number of bits, so the divider will output a quotient with N_d bits and a remainder. The remainder can then be stored or discarded. But later, we will see ignoring the remainder and letting N_d be very large, such as $N_d = 20$, will not harm the conclusion.

A testbench is set up to verify such a system. The input remains the same as the last testbench, where $i \in [1/32, 1]$, and the ideal 5-b ADC also remains the same as a benchmark. For the system with a TDC, Δt still follows that of a 9-bit TDC, and the quantization results of time are still $q_t = [t/\Delta t]$. At this step, the resulting graph will not differ from Fig. 3.5. But now q_t will be sent to the divider, and the quotient will become the output q for the whole system. The curve of the quotient is shown in Fig. 3.6.

It can be seen that the $q - i$ curve is brought back to linear, yet the larger i side forms a big 'head' with large errors, and the other side forms a fine 'tail' with small errors. The cause is similar to that of Fig. 3.5. This is because the time quantization reduces the resolution at the right-hand side of Fig.3.5. Although the divider can straighten the curve, it cannot restore the resolution loss, as the same dividend and divisor can only produce the same quotient. As a result, the 'head' sees a large quantization error, which is not removable unless introducing other quantities, such as the quantization remainder of the TDC. However, extracting the quantization remainder also requires quantization, which causes increased system complexity. Moreover, the remainder is also non-uniform. As we can see, the quantization remainder of the 'head' part in Fig. 3.5 is up to half the largest step, but the remainder of the 'tail' part is as fine as those small steps. Therefore, this is not a good solution for this project.

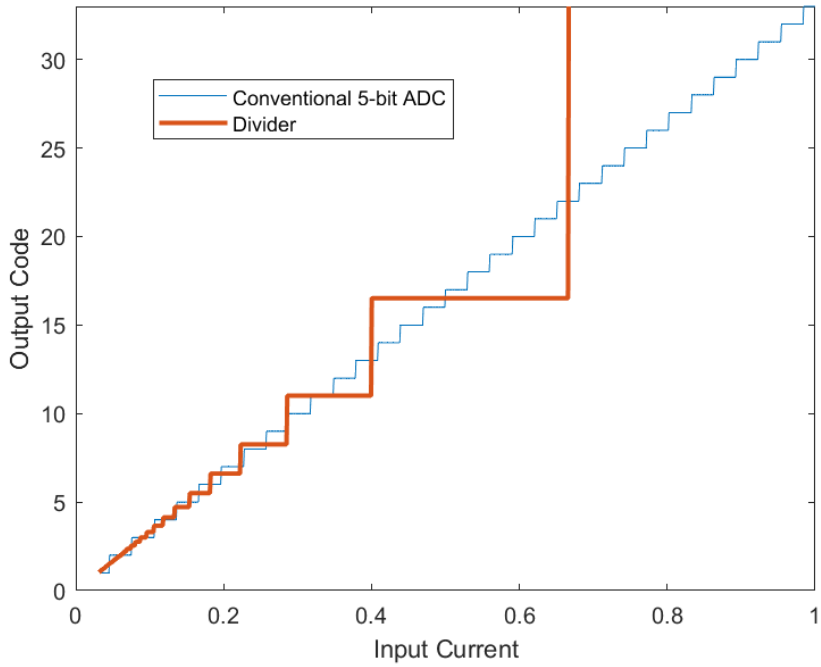


Figure 3.6: System with division after TDC. The output of the divider is scaled to [1, 32] Although the linearity is restored, the large steps with large quantization errors still exist.

3.3.4. The Third Hypothetical System

The third idea would suggest increasing the resolution in the time quantization. Then, the resolution loss at the TDC part will reduce, and the resolution of the output of the divider will also increase. To verify this, we need to replace only the 9-bit TDC with an 11-bit TDC and repeat the process. All other parts need to remain the same. The outcome is shown in Fig. 3.7. It can be seen that although the largest step matches the resolution of a conventional 5-bit ADC, the smaller steps will be unnecessarily fine. In a later design stage, the overdesigned resolution will cost more system budgets, such as chip area and power. Therefore, this method is not a good solution for the system.

3.3.5. Conclusion

After the analysis above, the pattern of the non-linear current sampler can be found. The whole curve can be roughly divided into three parts, as shown in Fig. 3.8: the Head, the Body, and the Tail. The three parts require different quantization resolutions: the 'head' requires the finest quantization to avoid resolution loss, but for the 'tail' part and the 'body' part, the resolution requirements vary but are less stringent. This pattern causes the conventional uniform quantization scheme to fail because a fine TDC will exceed the requirements of the 'tail,' but a rough TDC will not suffice the requirements of the 'head.' Therefore, a way needs to be found to bias the quantization resolution.

It can be further concluded that the requirement of biasing different parts is unavoidable regardless of the system parameters and design parameters. That is because those system parameters and design parameters only perform linear transformations to the curve. For example, if V_{ref} changes due to mismatch or PVT, or C has to change due to insufficient silicon area, the characteristic equation becomes

$$T'_{sig} = \frac{(C + \Delta C)(V_{ref} + \Delta V_{ref})}{I_{load}}. \tag{3.3}$$

If both ΔC and V_{ref} are constant, they can be expressed as a ratio of C and V_{ref}, respectively, as follows:

$$\Delta C = \alpha C, \tag{3.4}$$

$$\Delta V_{ref} = \beta V_{ref}. \tag{3.5}$$

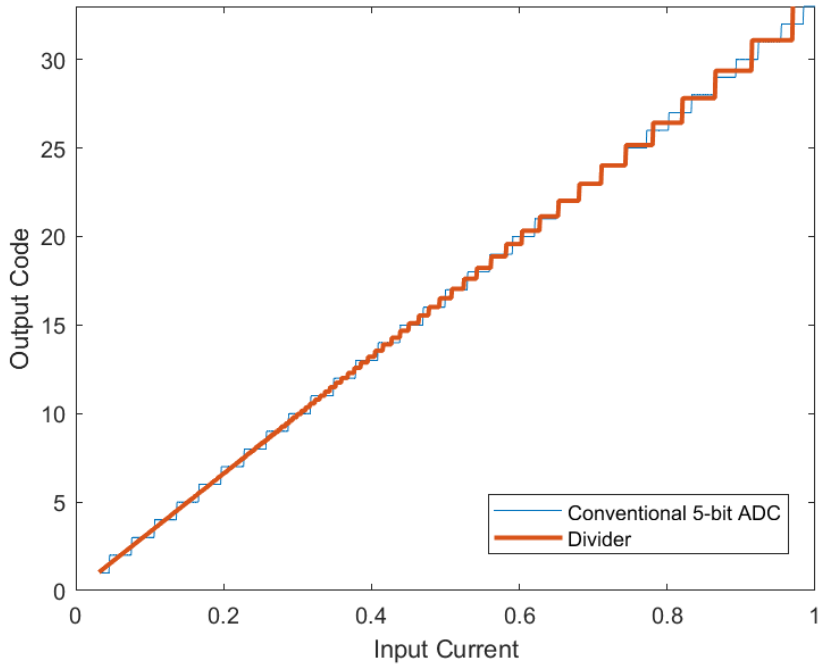


Figure 3.7: Division After TDC Quantization with Finer Resolution.

The original equation then becomes

$$T'_{sig} = \frac{(1+\alpha)(1+\beta)CV_{ref}}{I_{load}} = (1+\alpha)(1+\beta)T_{sig}. \tag{3.6}$$

It can then be observed that T'_{sig} preserves the property of T_{sig} with a different scale. Moreover, the property of the curve will not change after adding an offset to either I_{load} or T_{sig}, because the offsets only shift the position of the curve in the i-t plane. In Fig. 3.9a-3.9d, several situations that apply a linear transformation to the original current sampler curve are presented. These situations include scaling in i direction, scaling in t direction, introducing a t offset, and cropping curve. Such transformations cause the new curve to shift position from the original curve or become a subset of the original curve. However, it can be clearly observed that the transformations keep the relative positions of the three zones on the curve.

Therefore, the need of biasing different parts with different resolutions will not disappear. A counterargument is that the linear transformation changes the scale of the required gain of the curve so that the quantizer can quantize the 'head' with enough precision and the 'tail' in a better way. However, doing so will only reproduce the problems shown in Fig. 3.6, as the relative relationship between the quantizer and the curve still exists but with a different scale.

3.3.6. Solution

From the analysis above, we can find out there are two prerequisites for the possible solution, namely:

- The TDC needs to linearize $i - q$ curve.
- The TDC needs to select gains in order to give precise quantization in the 'head' zone and not cause unnecessary quantization in the 'tail' zone.

The combination of these two conditions and the problem analysis shows that a dedicated non-linear TDC performs better than a linear TDC to complete this task. For the first requirement, it is easy to find out the required TDC characteristic function as follows:

$$f_{q,ideal}(t) = \frac{K}{t_{sig}}, \tag{3.7}$$

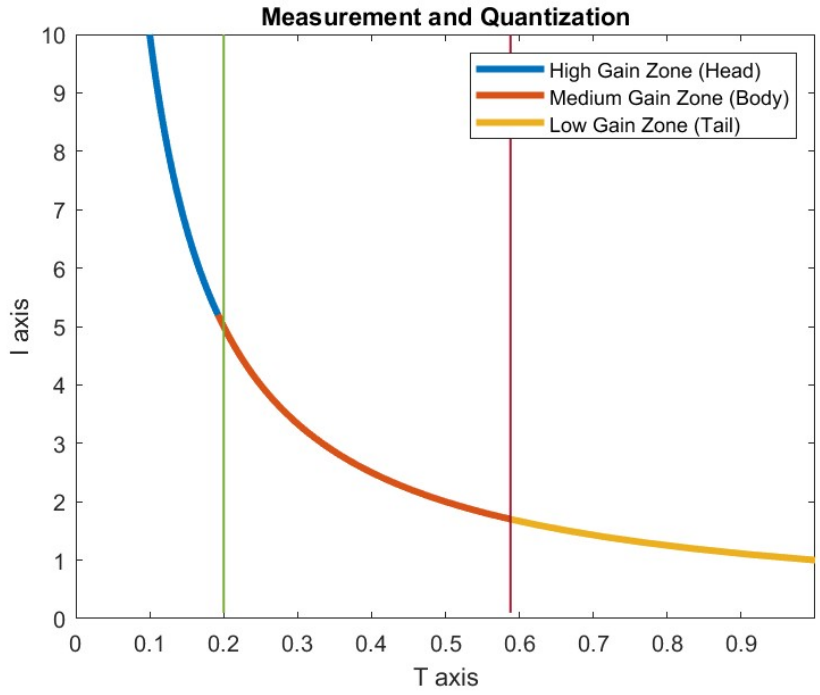
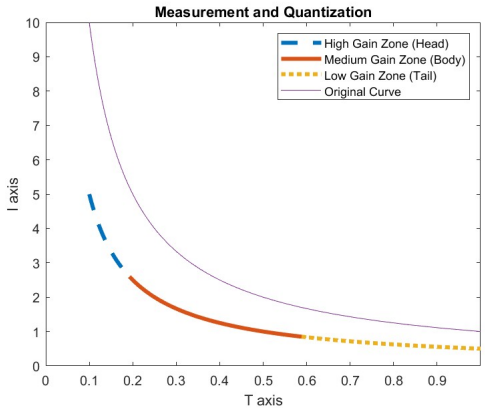
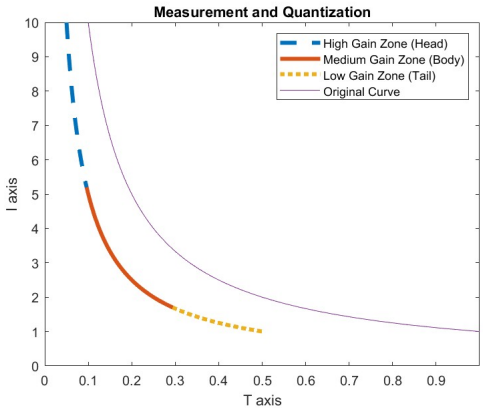


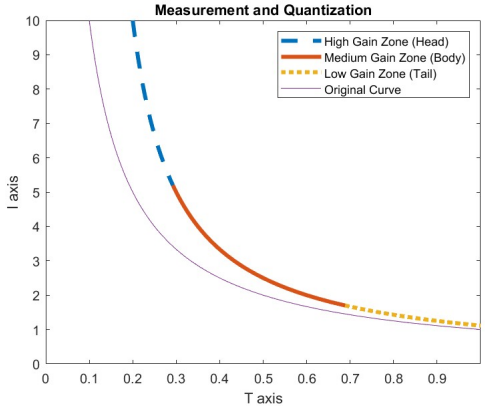
Figure 3.8: Three Subranges.



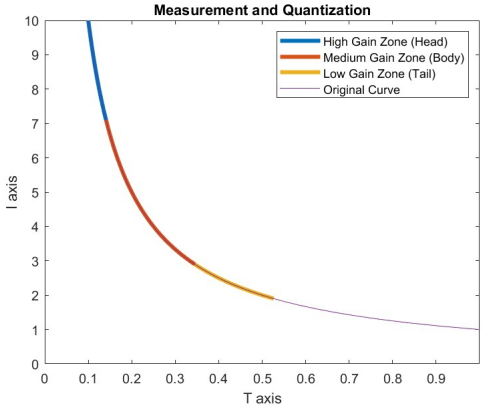
(a) Scaled i.



(b) Scaled t.



(c) Offset in t.



(d) Cropped curve.

Figure 3.9: Effect of linear transformation.

$$q = f_{q,ideal}(t) = \frac{K}{t_{sig}} = \frac{K}{\frac{C_{samp}V_{ref}}{I_{load}}} = \frac{K}{C_{samp}V_{ref}} I_{load}, \tag{3.8}$$

where K is the scaling factor that is an arbitrary constant.

The second requirement is the most tricky because an input-dependent behavior is required. The analog feedback method is not applicable, as finding a component with a dedicated non-linear property is challenging. Once the input current is converted to voltage, there will be no components with hyperbolic characteristics that can convert the voltage to another quantity. However, as the whole system is in a small number of bits with countable steps, we can use a look-up table to map each step size of the curve back to a linear code.

The look-up table shows that each quantization step is made into different lengths depending on the momentary system input. In this way, a digitized inverse function is created, as shown in Fig. 3.10. In the implementation, the $i - t$ mapping is unchanged compared to the hypothetical systems, but after t is obtained, it will be mapped to q with the predetermined look-up table. Notice the mapping can be done in two equivalent ways, either a direct $t - q$ conversion or first obtaining q_t then converting q_t to q. As the expectation, the output code q will be the linear representation of I_{load} in the digital domain, with well-defined small non-linearity and without too much over-quantization.

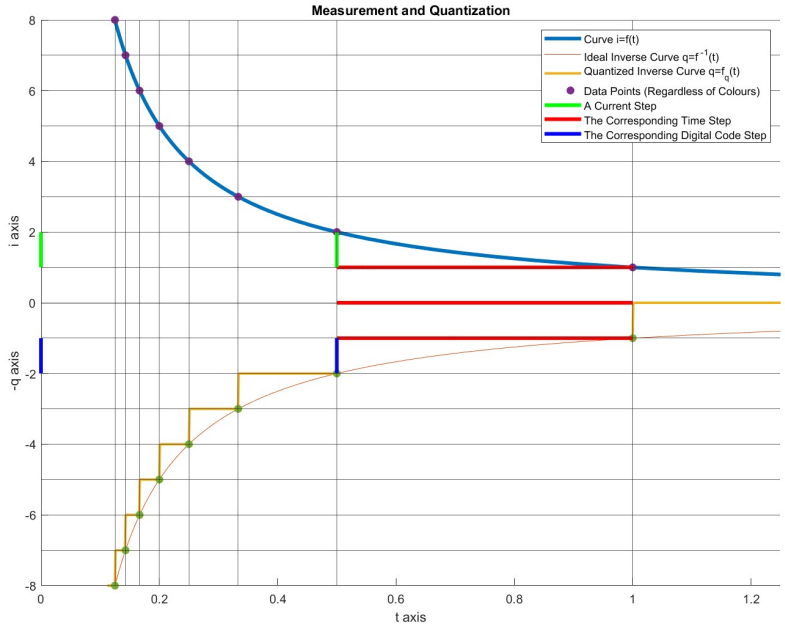
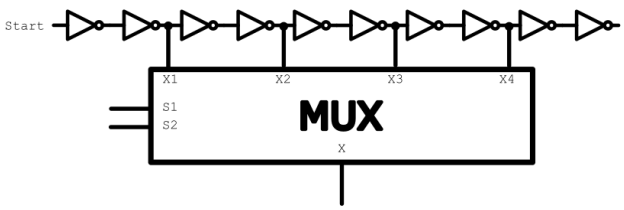


Figure 3.10: Illustration of quantization in three axes. Note the q-axis is presented as $-q$ for clear plotting. The green, red, and blue bar marks a process of transforming i step to t and q domains to restore the linearity.

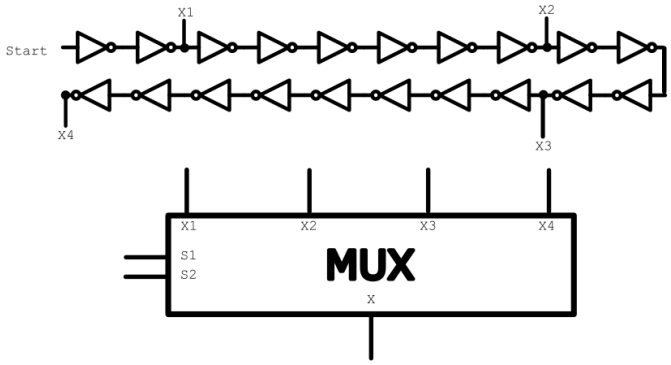
To calculate the desired look-up table, we first need to depict the design parameters. There are several tunable design parameters in this model, namely C, V_{ref}, and T_{res}. These parameters form the gain factor by $K = (CV_{ref})/T_{res}$, so they can be scaled to compensate each other without damaging the behavior. For example, in a later design stage, if T_{res} should be larger than the desired value by a factor of $T'_{res} = 1.2T_{res}$, C or V can compensate that by either $C' = (1/1.2)C$ or $V' = (1/1.2)V$. However, after the parameters are depicted, the look-up table will become unique.

The look-up table is obtained by following calculation steps: First, the set t_k is obtained by elementwise division $t_k = (C_{samp}V_{ref})/i_k$ for each k. Then, by calculating $\Delta t_k = t_k - t_{k-1}$ for each $k > 1$, the length of each step can also be obtained. It can already be seen that when trying to calculate Δt_0, the required t_{-1} will be missing. Therefore, Δt_0 is specially defined as $\Delta t_0 = t_0$, marking the step of $q = 0$ has $t_{-1} = 0$ as the natual boundary. The final step is to round each step to the multiple of a chosen resolution unit t_{res}, resulting in the quantized step set $\Delta t_{q,k} = [(\Delta t_k)/t_{res}]$. The rounding step aims to help with the implementation of TDC.

One concern about this method is the circuit implementation. However, this method has a rather simple implementation method in the time domain. Two types of reference delay generators are shown in Fig. 3.11. Fig. 3.11a shows a linear reference delay, and Fig. 3.11b shows an altered DL-TDC. The two delay references create different delay properties by changing the number of delay buffers in between. The structure shown in Fig. 3.11b forms the fundamental element for the implementation in the later chapters. More implementation details will be discussed in the next chapter.



(a) Linear delay reference. The delay from the start to four inputs are 1, 2, 3, and 4 buffer delays, respectively.



(b) Delay reference with varied step size. The delay from start to four inputs are 1, 4, 6, 10 buffer delays, respectively.

Figure 3.11: Two types of delay references. Note two inverters form a delay buffer.

Moving back to the analysis of the system that is not working well, it can be seen the key to the problem is to adjust the resolution according to the needs, which changes with the input current at the moment. The required minimum resolution depends on the smallest step in the 'head,' so that the resolution requirement needs to be met regardless of the structures or the algorithms. However, by applying the greatest resolution to the 'tail,' overquantizing still happens, so the algorithm needs to filter out excess information, resulting in the phenomenon described by Fig. 3.7. That's why using variable step sizes in the TDC structure is a proper approach.

So far, we have obtained a mathematical model for the proposed system. Before continuing with the design workflow, the model needs to be verified by MatLab. After passing the Mathematical model verification, the whole system will be implemented and verified in the simulation software Cadence.

3.4. Mathematical Verification

The mathematical verification aims to describe the ideal behavior of the proposed model as an ADC and assess this method under the given requirements. These goals will be achieved in three steps: First, the system requirements will be translated to a set of test goals that define an acceptable ADC. Second, the mathematical model will be built to generate results. Third, the results will be discussed in combination with the test goals, and a conclusion will be drawn. Each step mentioned here will be addressed in a subsection below.

3.4.1. Test Goals

The goal of testing at this design phase is to check the linearity between i and q when applying the quantization method mentioned above. The first goal is to verify if the DNL and INL are bounded in a safe region.

Moreover, the test also aims to describe the distribution of its remaining non-linearity among the whole data range, so that the effect of this curve in later implementation steps can be estimated.

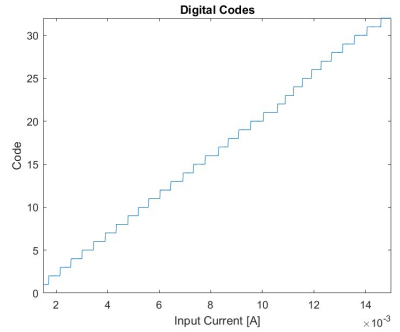
3.4.2. Modeling and Testing Methods

First, the input step count M and the input current range i_0, i_{M-1} are chosen to be $M = 2^5 = 32$, $i_0 = 1.5$ mA, $i_{M-1} = 15$ mA. The step count M is chosen based on $N = 5$ as mentioned in Section 3.1.2 and i_0, i_{M-1} are chosen to fit the largest subrange. The other subranges have the same curve shape but with different multipliers, so the model of one range covers all ranges. Also, the parameters C and V_{ref} are chosen to be 20 pF and 1 V respectively. After that, the calculations follow the method described in the previous section, and the sequences $t_1, ..., t_M$ and $\Delta t_1, ..., \Delta t_M$ are obtained. The Δt sequence is further rounded to multiples of $t_{res} = 50$ ps to obtain the Δt_q sequence. Finally, the model reconstructs the sequence Δt_q into sequence i_q, which are the quantization boundaries in the current domain.

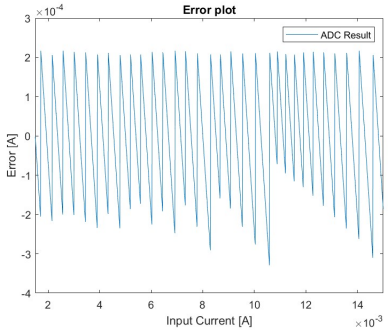
After the model calculation, the testing tasks include generating characteristic curves and calculating associated performance indicators. The characteristic curves include the $i - t$ curve, $t - q$ curve, and $i - q$ curve. The performance graphs include error plots, INL, and DNL graphs. As the $i - t$ graph and $t - q$ graph are both non-linear, only the $i - q$ graph is valid for traditional performance assessment. Therefore, only $i - q$ will be assessed with performance indicators.

The model is constructed with MatLab codes shown in Appendix A. The codes include three parts, namely curve construction, fine plot testing, and results generation. Some of the codes serve for necessary calculation in later steps and will be introduced in the following chapters.

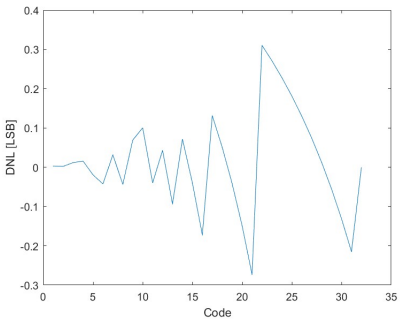
3.4.3. Results



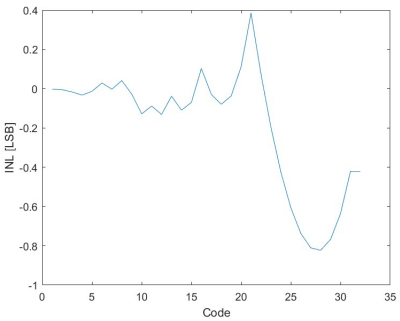
(a) $i - q$ Characteristic Curve.



(b) Error Plot with Current.



(c) DNL Plot.



(d) INL Plot.

Figure 3.12: Test Results of Non-Linearity Canceling TDC in MatLab.

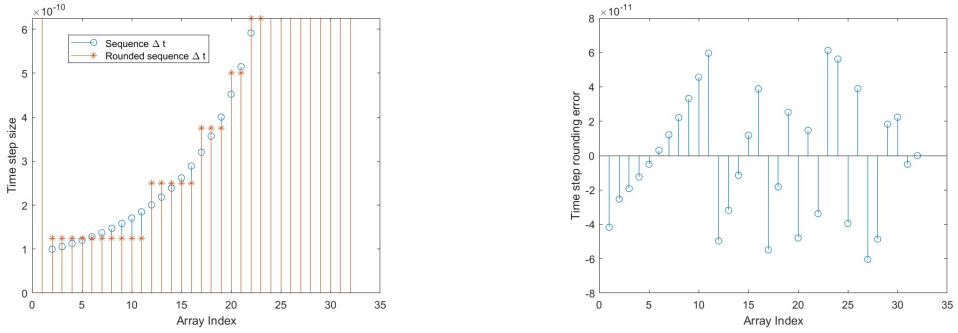
Fig. 3.12 shows the obtained graphs, including the $i - q$ characteristic plot, the quantization error plot, the DNL plot, and the INL plot. The $i - q$ plot (Fig. 3.12a) shows that this method with a given parameter set can produce a input-output response comparable to conventional ADC. Fig. 3.12b illustrates the distribution of quantization error, which is non-uniform but bounded to a certain region.

INL and DNL plots (Fig. 3.12d and Fig. 3.12c) provide more details about how the quantization error distributes across the whole range. We see a larger error takes place in the larger current part

described as the highly demanding 'head'. The maximum absolute value of DNL is below 0.5 LSB, and that of INL is below 0.8 LSB. These results show that this algorithm can meet the requirements.

The distribution of the DNL is caused by rounding effects in different regions. Fig. 3.13 illustrates the rounding effects, where Fig. 3.13a shows Δt and rounded Δt respectively, and Fig. 3.13b shows their absolute difference, which is the rounding error. Although all rounding errors are below 0.5 LSB for all steps, the impact is different because Δt is varied. In a large step such as Δt_{20}, which has the length $\Delta t_{20} = 3$ LSB, a rounding error of 0.5 LSB only makes $0.5/3 = 1/6$ relative error. However, in a small step such as $\Delta t_{11} = 1$ LSB, a 0.5 LSB error can make up to 50% relative error. That's why they cause the largest DNL steps.

Another partial conclusion is the INL in the 'head' region is the largest. That comes from the cumulative error of the 'head' region. As the rounding of the smaller step is single-sided, the cumulation enlarges the INL. However, the INL is less problematic because the sampling rate is going to be low, and distortion to the high frequency signal is not a concern for this application.



(a) Time Steps Before and After Rounding.

(b) Rounding Error of Each Time Step.

Figure 3.13: Time Steps and Rounding Effects.

3.4.4. Conclusions

The results show that the NLCTDC behavior fits the proposed application. The DNL and INL have a well-defined upper limit within the requirements. Therefore, it can be concluded that the described method is a potentially good solution. The next step is to implement this method appropriately in circuits and evaluate the performance of the resulting circuit system.

4

Circuit Implementation

In this chapter, the implementation of the proposed system will be discussed. First, all circuit blocks in the proposed system are discussed respectively. Then, the test plan and the corresponding test results are presented. Finally, a conclusion is drawn.

4.1. System Block Implementation

The top-level block diagram of the implemented system is shown in Fig. 4.1. It consists of two major blocks: the Current Sampler and the Non-Linearity Canceling Time to Digital Converter (NLCTDC). The details are further elaborated in the corresponding subsections.

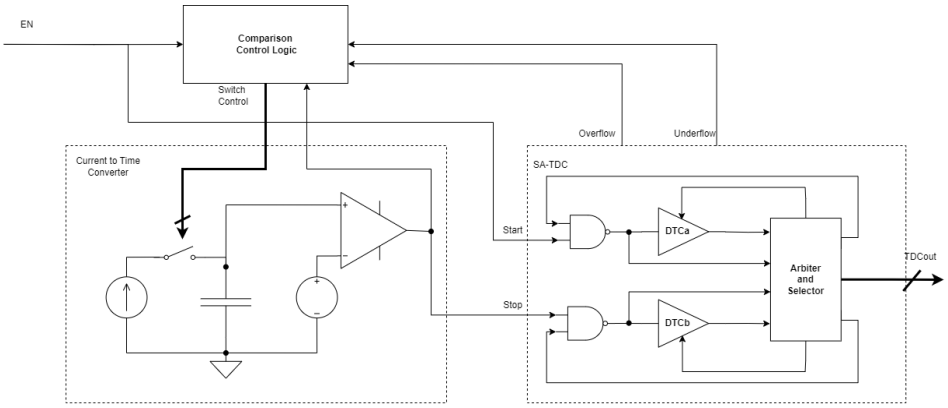


Figure 4.1: Top-level block diagram of proposed MPPT scheme.

4.1.1. Current Sampler

The Current Sampler consists of a circuit that produces a reliable copy of the input current, a switched capacitor bus, a comparator, and a control block, as shown in Fig. 4.2.

Switched Capacitor Bus

The structure of the switched capacitor bus is shown in Fig. 4.2. The current source 'Iin' represents the current created by the current copying structure, which is a 1:1 copy of the actual charging current. The resistor 'Rdis' represents a discharge path of the input current, and the resistance is set large enough (10 $G\Omega$) that it does not influence the current flowing to the sampling capacitors when the switch 'SWin' is connected. Note that the input current model created by 'Iin' and 'Rdis' is not the actual input structure but an equivalent representation.

Other components in Fig. 4.2 include five switches ('SWin', 'SWdis', 'SW1', 'SW2' and 'SW3') and four capacitors ('C0', 'C1', 'C2', 'C3'). The switches are controlled by the comparison logic to perform actions such as sampling the input current, discharging the capacitors, and changing the total effective

capacitance. The capacitors follow the capacitance distribution as described in the previous chapter ($C_k = 9C_{k-1}, k = 3, 2, 1$). The three larger capacitors are all dependent on 'C0', which forms a design parameter of the system.

The control scheme of the switches is explained in Section 4.1.1.

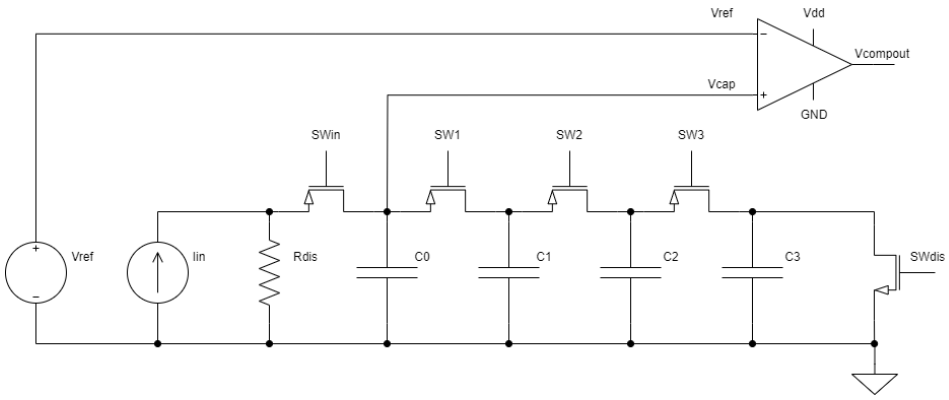


Figure 4.2: Circuit diagram of current sampler.

Comparator

The comparator is a five-stage Operational Transconductance Amplifier (OTA) structure with a simple output stage, as shown in Fig. 4.3. The bias current is provided by current mirrors. As the comparator compares input voltages against a fixed reference voltage, the bias current of the comparator only influences the output delay. Therefore, the comparator can be biased against a low current to reduce the current consumption.

From experience, the Strong Arm Latch structure performs better than the OTA as a comparator because it consumes less power per comparison. However, the Strong Arm Latch cannot be deployed because it is a clocked comparator. If a Strong Arm Latch is used as the comparator, it will require a clock with $T_{clk} = 500$ ps at most or $f_{clk} = 2$ GHz, which is not available from the application. Therefore, a continuous time comparator is used. The power consumption is expected to be controlled by shutting down the comparator during the time that a measurement is not required. In the presented version, the shutting-down mechanism is not implemented for simplicity.

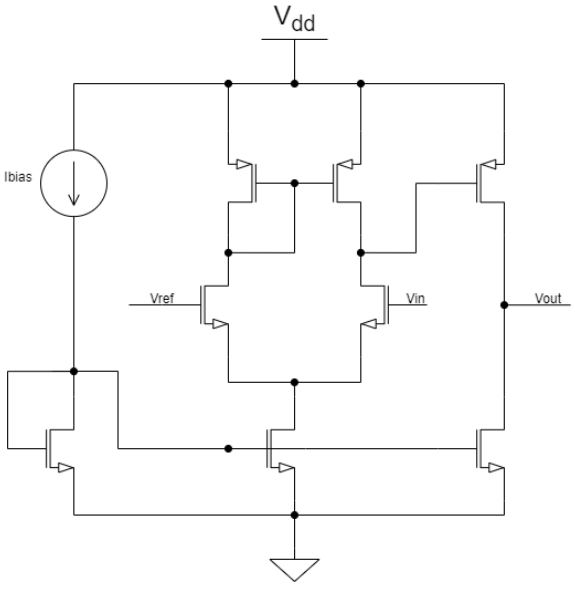


Figure 4.3: Adopted comparator.

Comparison Control Logic

The comparison control logic aims to control the charging and discharging of the sampling capacitors. It is implemented with an asynchronous Finite State Machine (FSM) shown in Fig. 4.4.

The FSM consists of two states, the discharge state ('DISC') and the integration state ('INTE'), represented by a single bit number '0' and '1,' respectively. At the 'DISC' state, the input port will be disconnected from the capacitor bus, and all capacitors are connected to the ground (GND) to discharge. At the 'INTE' state, the capacitor bus will connect to the input port, and the gain is toggled by interconnecting switches (SW1..SW3), which changes the effective total capacitances.

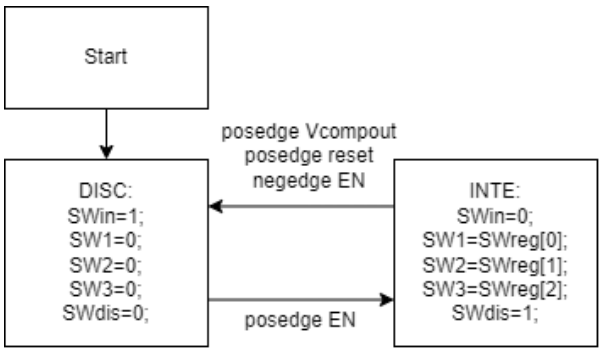


Figure 4.4: Comparison Control logic. 'Posedge {Signal}' in this figure represents 'the positive edge of {Signal}', 'Negedge {Signal} represents 'the negative edge of {Signal}'. The same applies to other figures.

When 'reset' is high, the FSM enters and stays at the 'DISC' state. When 'reset' is low, the FSM will enter the 'INTE' state at the positive edge of 'EN' to start sampling. The FSM will exit the 'INTE' state in either of the three conditions:

- At the rising edge of 'Vcompout,' marking the sampling is complete;
- At the falling edge of 'EN,' marking a Time-Out;
- At the rising edge of 'reset,' marking a forced reset.

It can be seen that the measurement will be synchronized with the rising edge of 'EN,' and the length of the 'EN' pulse indicates the maximum measurement time because a longer measurement is forced to end by the Time-Out condition.

In parallel with the main FSM, the states of 'SW1', 'SW2,' and 'SW3' during the 'INTE' state are toggled by three registers ('SWreg[1:3]'). The registers are reset at the positive edge of 'reset', and are updated at the negative edge of EN according to whether the 'Overflow' or 'Underflow' pin has been pulled up, as illustrated in Fig. 4.5.

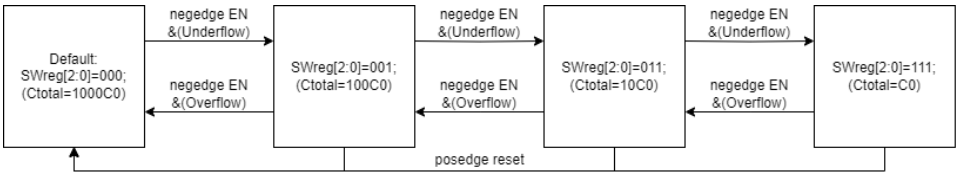


Figure 4.5: Control logic.

4.1.2. NLC-TDC

The required behaviour of the NLC-TDC is described in Chapter 3. In this project, the architecture of Cyclic Successive Approximation Time to Digital Converter (CSA-TDC) is chosen to enable easy reconfiguration of the step sizes and reduce the number of delay stages.

The basic structure and the algorithm of the implemented CSA-TDC follow the general architecture described in Fig. 4.6. However, there are two differences. First, the control logic needs to send out 'Overflow' and 'Underflow' flags for the comparison control. Second, the reference generation scheme is changed completely to create the Non-Linearity Canceling feature.

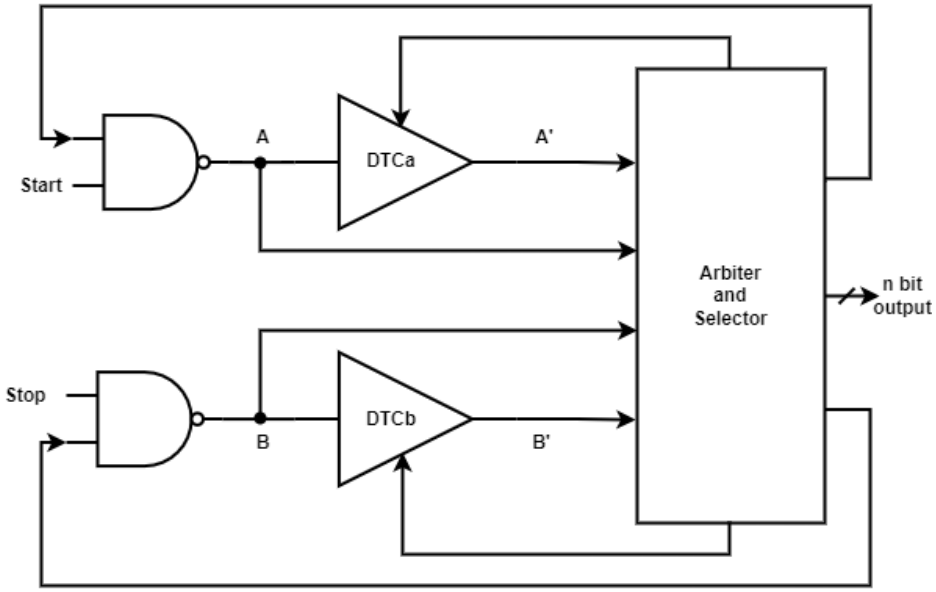


Figure 4.6: CSA-TDC structure.

Reference Scheme

In a conventional N-bit Successive Approximation TDC (SA-TDC), the references are generated according to a balanced binary distribution scheme, as shown in Fig. 4.7. The node represents the equivalent reference $T_{ref,total}$, and the branches represent the decision $D[k]$ and required T_{ref} of each step. $D[N-k+1]$ is decided between -1 and $+1$. For the k-th iteration, which decides the k-th largest bit, the following equations apply:

$$T_{ref}(k) = \frac{1}{2^k} FS = (2^{N-k+1}) T_u, \tag{4.1}$$

$$T_{ref,total}(k) = \sum_{i=k}^{N} (D[N-i+1] T_{ref}(i)), \tag{4.2}$$

where T_u is the unit time reference and T_{ref} is a multiple of it. $T_{ref}(k)$ is independent from the previous decisions $D[N:k-1]$, due to the balanced reference distribution. However, to create the required non-linear characteristic curve, $D[N:k-1]$ should influence T_{ref}, as shown in Fig. 4.8 and 4.9. It can be expressed as

$$T_{ref}(k, D[N:(N-k+1)]) = T_u * n(k, D[N:(N-k+1)]), \tag{4.3}$$

where n is the number of required delay stages. For $k = N$, there is no previous decision and n will become n_N, which is the initial reference. The table of $n(k, D[N:(N-k+1)])$ can be generated by a short piece of code shown in Appendix A, and is hard-coded into the SA-TDC logic for simplicity. The complete table for a 5-bit scenario ($N = 5$) is shown in Table 4.1, which contains 17 unique n values as follows:

$$n \in \{1, 2, 3, 4, 5, 7, 9, 12, 13, 20, 26, 27, 33, 38, 44, 45, 47\}. \tag{4.4}$$

For this project, as explained in Section 3.1.2, a 5-bit ADC is needed. Therefore, the scenario shown above can be used in the reference design. As a result, the DTCs need to create 17 different lengths, and they are controlled by two 5-bit signals.

TDC Control Logic

The proposed TDC algorithm is shown in Fig. 4.10, similar to the general algorithm but specifies some important control signals. At the positive edge of EN, the main loop initiates the operation. The signal 'bit' is a binary quantity that notes the next to-be-decided bit and decrements from 5 to 0. The two loops are 'A->Ad->A->...' and 'B->Bd->B->...'. At either a positive edge or a negative edge of 'Ad,' a

Table 4.1: Table of $n(k, D[N : (N-k+1)])$. The last two rows omit the value of $D[N : (N-k+1)]$, which still follows starting with 0 and incrementing with 1 for each n value from left to right.

k	n values
1	$n(1)$=47
2	$n(2,0)$=13 $n(2,1)$=33
3	$n(3,00)$=4 $n(3,01)$=5 $n(3,10)$=20 $n(3,11)$=44
4	2 2 3 4 7 9 27 45
5	1 1 1 1 1 1 2 2 3 3 5 5 9 12 26 38

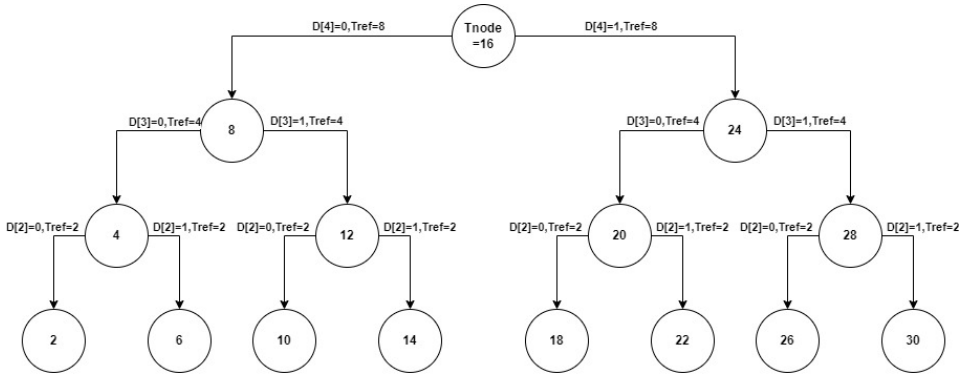


Figure 4.7: Balanced binary reference distribution.

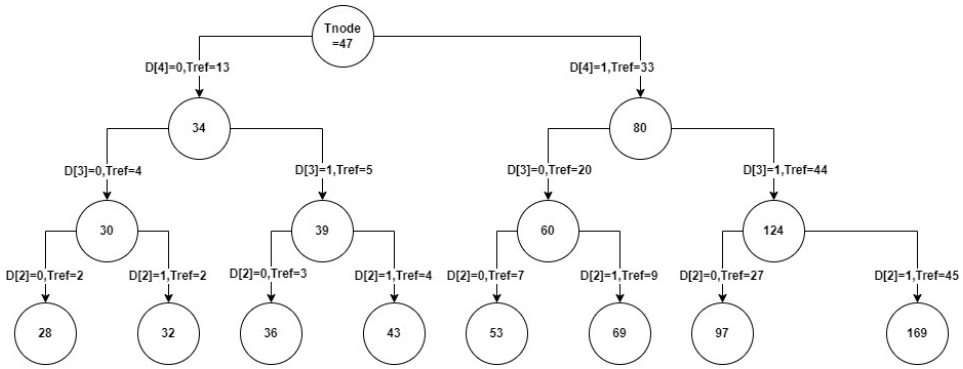


Figure 4.8: Non-balanced binary reference distribution.

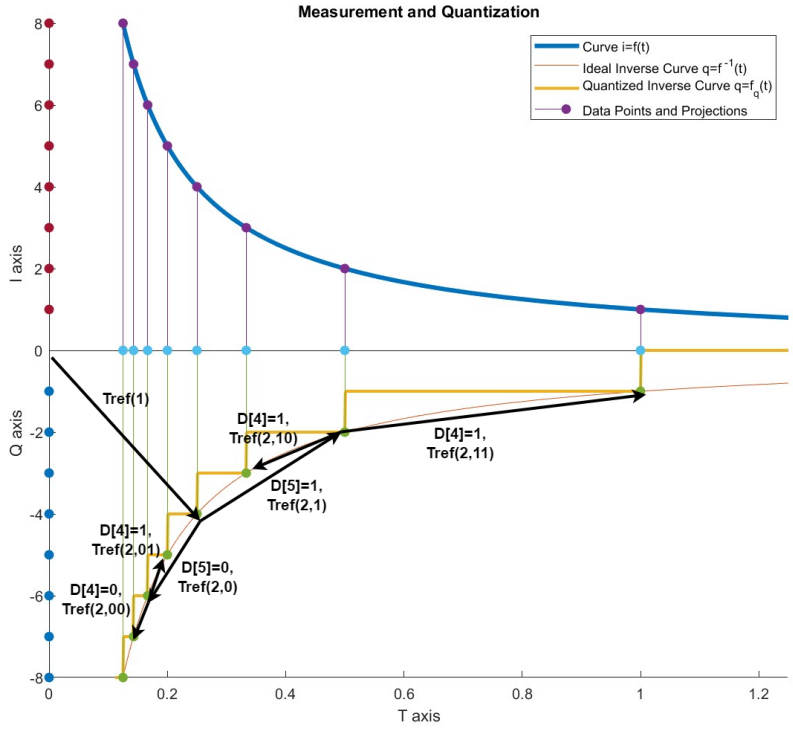


Figure 4.9: Non-balanced binary reference distribution on quantizer curve.

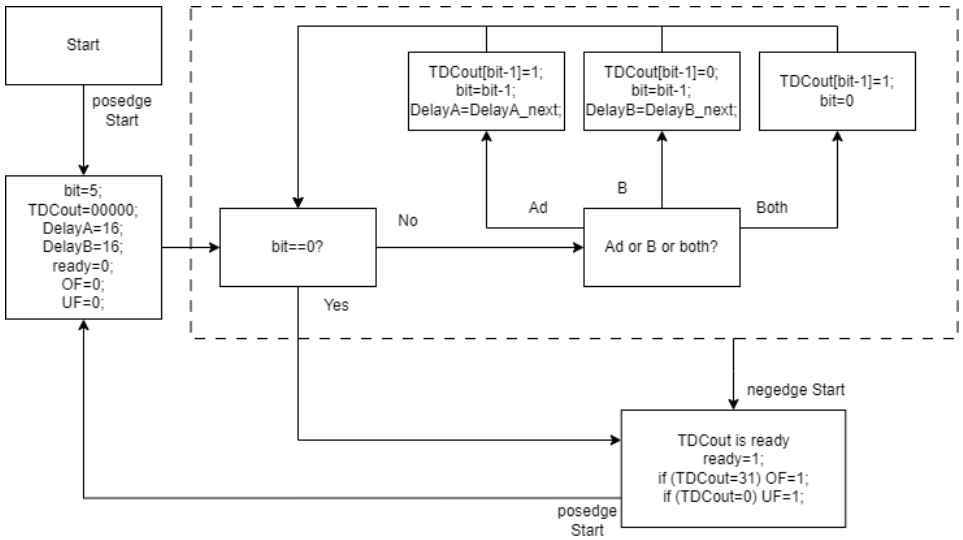


Figure 4.10: Proposed algorithm for TDC control.

pulse will created at 'TDCone', the same is true for 'B' and 'TDCzero.' Whenever one of the 'TDCone' and 'TDCzero' pulses is sent to the input ports, the following assignments will happen (the case for 'TDCzero' is in brackets):

1. The output code 'TDCout[bit-1]' is set to '1'('0');
2. The loop control 'DelayA'('DelayB') is set to $n_{k,D[N:(N-k+1)]}$;
3. The 'DTCreadyA'('DTCreadyB') signal is toggled to create an edge.

To clarify some possible confusion between the quantities in circuit implementation and the ones represented by mathematical signs, two notes need to be taken. The first note is that if we want to express the quantity 'bit' with N and k, it should be $bit = N - k + 1$. The algorithm starts with 'bit'=5, or equivalently $k = 1$. Because of the negative sign in front of k, each decrement of 'bit' represents an increment of k. When the loop continues to the moment just before the last decision is made, 'bit' will become 1 and k will become 5. Then, after the last decision is made, bit will become '0' and mark the measurement has ended. The second note is that 'TDCout[4:0]' corresponds to $D[5:1]$ as the digital counts usually start with 0 instead of 1. Therefore, when 'bit'=5, the next reference should be assigned to $D[5]$ or 'TDCout[4]', and the next reference should be chosen to $n_{2,D[5]}$ to decide $D[4]$.

The looping process repeats until one of the following conditions occurs:

1. bit becomes 0 after 5 iterations
2. Both 'TDCone' and 'TDCzero' flags detected within 1 iteration.
3. At the negative edge of EN
4. $reset$ flag is raised

Condition 1 marks a successful measurement. Condition 2 marks that the current comparison reaches a state where the input is too close to the combination of the references that the one and zero are detected at the same time. Therefore, the measurement can also be stopped. Condition 3 marks the time-out of the measurement. Condition 4 is the forced reset operation. When any of these conditions is met, the system will go back to the starting state and wait for the start of the next measurement.

Digital to Time Converter

The Digital to Time Converter (DTC) is the combination of a delay chain and a mux, as shown in Fig.4.11. The structure of the delay chain can be found in Fig. 4.11a, and the concept of the mux can be found in Fig. 4.11b. As for function, the DTC needs to create the following reference set for the algorithm:

$$n = \frac{T_{ref}}{T_u} \in \{1, 2, 3, 4, 5, 7, 9, 12, 13, 20, 26, 27, 33, 38, 44, 45, 47\}. \tag{4.5}$$

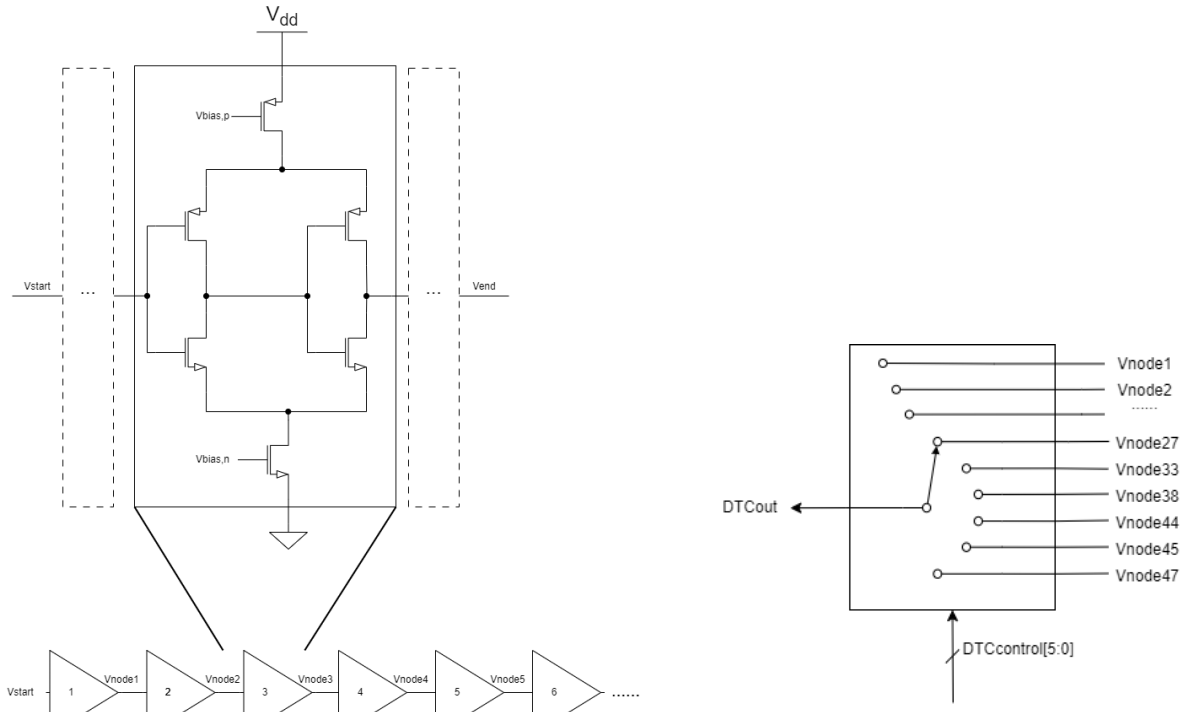
This set consists of 17 elements, and the largest element is 47. Therefore, the delay chain circuit contains 48 stages, with 1 extra stage ensuring all gates have similar loads. Each delay stage consists of two not gates that share the same bias current on both PMOS and NMOS branches to ensure a similar slew rate at the rising edges and the falling edges. The stage capacitor toggles the stage delay t_u, which is a design parameter of the system. All the stages are designed to be identical.

Which node among the 17 dedicated nodes is connected to the output is controlled by a 17-1 mux. At the rising edge of the signal $ready$, the mux will load the D_c to its internal registers. The mux will forward the node in position $n(k, D[k-1])$ to the output, which can be expressed as follows:

$$t_d = t_u * n(k, D[N - k + 1]). \tag{4.6}$$

4.1.3. Decoder

The Decoder is the extended part of the system, which converts the binary codes into decimals to provide convenience for testing. The decoder is selected to invert the polarity of the code with $q_{out} = 32 - q$ to ensure the positive gain of $\mathrm{d}I/\mathrm{d}q_{out}$ so that the increase in q_{out} corresponds to the increase in I. A more detailed explanation can be found in Appendix. B.1.



(a) Delay chain circuit.

(b) 17-to-1 mux. The mux connects to specific nodes in Fig. 4.11a according to Equation 4.5

Figure 4.11: Circuit implementation of DTC.

4.2. Test Methods

The input of the system includes the to-be-measured current source, the reset signal, and the EN signal. The output of the system is the digital code representing the measured current. The first two bits represent the equivalent size of the sampling capacitor, and the last five bits are the output of the TDC. At each falling edge of 'EN,' the 7-bit digital code is converted to an equivalent decimal number for more illustrative representation.

Because the proposed design contains two valid Designs Under Test (DUTs), which are the SA-TDC and the current input ADC as a whole, the two conversion structures should be verified with different tests. For this system, three types of responses are defined, namely the Linear Input Response, the Static Response, and the Frequency Response.

The simulation will be carried out in the Cadence environment. After obtaining simulation results, the curves will be transferred to MatLab for analysis and result presentation.

4.2.1. Benchmark

Because of the difficulty of characterizing the proposed system as a conventional ADC, a version of the system with ideal DTCs is designed as the benchmark for the proposed system. The benchmark version is identical to the proposed system except that the DTC is replaced with an ideal DTC, where the delay is defined by Verilog codes.

The benchmark is designed to extract the performance upper bound of the proposed system. In the test procedure, the benchmark and the circuit implementation will be compared against each other. The comparison between the two versions reflects the performance degradation after real circuit implementation.

4.2.2. Linear Time Response

The linear time response describes the system output pattern when T_{in} increases linearly. The expectation is that the output q follows a hyperbolic pattern. To complete this test, the current sampler needs a special setup, as shown in Fig. 4.12. The NLCTDC part remains the same.

The way of ensuring input delay is linearly decreasing is by applying the same sample current and

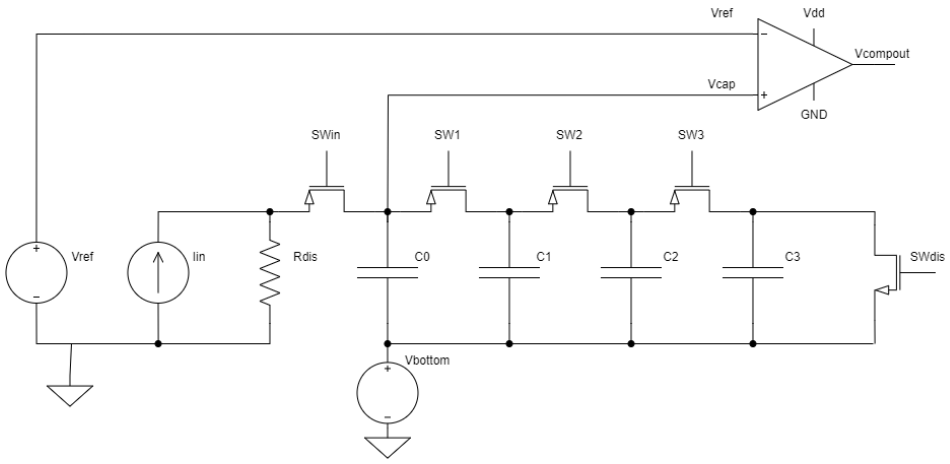


Figure 4.12: Setup for linear time response test.

period but gradually decreasing the bottom plate voltage V_{bottom} of the sampling capacitor. In the configuration shown in Fig. 4.12, in one sample period, the actual voltage ramp V_{ramp} in the presence of input current is,

$$V_{ramp} = V_{ref} - V_{bottom}. \tag{4.7}$$

Then, if V_{bottom} is slowly linearly toggled from V_{ref} to V_{GND} over the total simulation time t_{sim}, V_{ramp} will be toggled from V_{GND} to V_{ref} and will also linearly distribute among t_{sim}. Then input delay t_{in} of the TDC will become,

$$t_{d,in}(t) = \frac{C_{samp}}{I} V_{ramp}(t), \tag{4.8}$$

where $V_{ramp}(t)$ is slowly changing from V_{GND} to V_{ref} as time t passes, and $t_{d,in}(t)$ is slowly changing from $t_{d,in,min} = (C_{samp}V_{GND})/I = 0$ to $t_{d,in,max} = (C_{samp}V_{ref}(t))/I$ as a result. In this way, a gradually increasing input $t_{d,in}$ within one measurement range is created, and the periodic sampling will extract the shape of the TDC curve.

The best way to examine the shape of a curve is to fit the dataset to the target curve and then observe the relative error. However, fitting a dataset directly to a hyperbolic curve is challenging. To get an accurate fitted curve, two operations can convert the problem of fitting a hyperbolic curve to fitting a linear curve.

The first operation is to reduce the original dataset. The reason is that the resulting curve can be foreseen as ununiform. To avoid different step sizes providing different weights to the fitting algorithm, the center point of each step is extracted as the data points for fitting. The center points are a valid indicator of the curve and also ensure the equal weights of all steps.

The second operation is to transform one of the axes, in this case, the t_d axis. As the simulation time t_{sim} is proportional to t_d, it is also valid to transform t_{sim} instead. In details, this means transforming t_{sim} to $1/t_{sim}$, denoted as $a = 1/t_{sim} = 1/(kt_d)$ or $t_d = 1/(ka)$. After transformation, the relationship $q = f(t_d) = [k/t_d]$ is inverted into a linear relationship as follows,

$$q = [\frac{k}{t_d}] = [k_1 k_2 a]. \tag{4.9}$$

Therefore, after the axis transformation, the data points are expected to exhibit a linear relationship. Then, using linear fitting, the error will show the likelihood between the transformed dataset to a line, or between the original dataset and a standard hyperbole. For this test, the regression error e is used for the fitting accuracy indicator. It is defined as the vertical differences between each data point and the regression line. Because this test only aims to check the shape instead of extracting the actual quantization accuracy, the test standard does not need to meet a stringent standard. Therefore, the test target is that the absolute regression error, $|e|$, is bounded to $2LSB$. The actual system accuracy can be extracted by other tests.

4.2.3. Static Response

The static response test considers the proposed system as a current-based ADC and aims to generate the input-to-output relationship when the I_{in} changes linearly and slowly over a long time. This test is further divided into two partial tests.

The first test is the single range test, where the system only receives a linear ramp of currents over the largest measurement range. In detail, the ramp starts from 1.5 mA and will reach 15 mA within 80 µs, and the sampling period is 350 ns. The obtained response is examined as a static response of a 5-bit ADC.

The second test is the all-ranges test, where the system receives a ramp across all four ranges. Because the 4-range division of this system is not linear, the input current and simulation time arrangements follow Table. 4.2. After this division, the obtained response is examined as a static response of a 7-bit ADC.

After collecting two responses, the performance indicators DNL and INL will be calculated with the following equations:

$$DNL(k) = \frac{H(k) - H_{avg}}{H_{avg}}, H_{avg} = \frac{\sum_0^M H(k)}{M}, \tag{4.10}$$

$$INL(k) = \sum_0^k DNL(k), \tag{4.11}$$

where $DNL(k)$ and $INL(k)$ are the DNL and INL of the k-th step, respectively, $H(k)$ is the step size of the k-th step and is equivalent to ΔI_{in}, H_{avg} is the average step size of all steps, and M is the total number of steps. Because the simulation time t_{sim} is linearly correlated to I_{in}, it can be derived that $\Delta t_{sim} \propto \Delta I_{in}$. Therefore, Δt_{sim} can be substituted as an equivalent of ΔI_{in} in INL and DNL calculation. After calculation, the system is concluded to pass the test if DNL is bounded with ±1 LSB and INL is bounded with ±2.5 LSB. The adopted DNL requirement arises from the need to ensure monotonicity, while the INL requirement is based on a commercial ADC chip with a similar wide input range [28].

Table 4.2: Table of full range ramp setup.

Input Range Number	Range	Simulation Duration
1	1.5 µA – 15 µA	0–80 µs
2	15 µA – 150 µA	80–160 µs
3	150 µA – 1.5 mA	160–240 µs
4	1.5 mA – 15 mA	240–320 µs

4.2.4. Frequency Response

This test aims to extract the SNDR and ENOB of the proposed system. For simplicity, this test will only be done in the largest input range, which is [1.5 mA, 15 mA]. To extract the best SNDR, the input current is chosen to vary from 2 mA to 14 mA, which means the offset and the amplitude of the current are 8 mA and 6 mA, respectively. The frequency range of the input is usually chosen as [0, $f_s/2$], where f_s is the sampling frequency. The maximum sampling frequency of the proposed system is 2.86 MHz, which is decided by the duration of the longest measurement plus the resetting time. For simplicity, the test will be carried out in 4 input frequencies, which are 10 kHz, 100 kHz, 1 MHz, and 1.3 MHz. With these tests, the frequency response of the whole frequency range can be estimated. The sampled curve will be resampled with a much higher frequency (250 MHz) in the simulator, which is a large frequency excess but ensures the output waveform is fully preserved. The output waveform is further analyzed by applying FFT transformation and calculating the Signal to Noise and Distortion Ratio (SNDR) and Effective Number of Bits (ENOB). When calculating SNDR, the noise band is chosen as [0, $f_s/2$], and SNDR is calculated as

$$SNDR = \frac{P_S}{P_{N+D}}, \tag{4.12}$$

where P_S is the signal power and P_{N+D} is the sum of noise and distortion power in the noise band. After that, ENOB is calculated as

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02}, \tag{4.13}$$

where $SNDR_{dB}$ is the SNDR in dB. Then, it will be compared to the requirement specified in Section 3.1.2, which is $ENOB \geq 4$. After obtaining the ENOB, the Walden Figure of Merit (FoM) will be calculated. The formula for the Walden FoM is

$$FoM = \frac{P}{2^{ENOB} f_s}, \tag{4.14}$$

where FoM is the Walden FoM, P is the power consumption of the ADC. In this project, P is estimated with the power consumption of the comparator and the DTCs during the simulation. The power consumption of the control logic is not included. Therefore, the estimated power consumption is expected to be lower than the actual power consumption. A more accurate estimation is only possible after the synthesis and the layout design are complete, which still needs to be done.

4.3. Results

This section presents the obtained test results and briefly explains each of them. The test target of each test is summarized in Tab. 4.3.

Table 4.3: Table of test targets.

Test Name	Target
Linear Time Response	$\|e_{regression}\|$<2LSB
Static Response	DNL<1LSB, INL<2.5LSB
Frequency Response	ENOB>4

4.3.1. Linear Time Response

The linear time response describes the system output pattern when t_{in} increases linearly. The expectation is that q_{out} follows a hyperbolic pattern. During this test, some polarity changes are applied to the obtained data curve, and the details can be found in the Appendix B.1. The polarity changes do not change the conclusion.

The results are plotted in Fig. 4.13. Fig. 4.13a-4.13d respectively show the obtained original curves, the extracted data points, the transformed curves with fitted lines, and the regression error plots. After processing, the transformed data set is eventually fitted to a regression line with the absolute error bounded to 1.5 LSB. It can be concluded that the TDC has a hyperbolic pattern.

4.3.2. Static Response

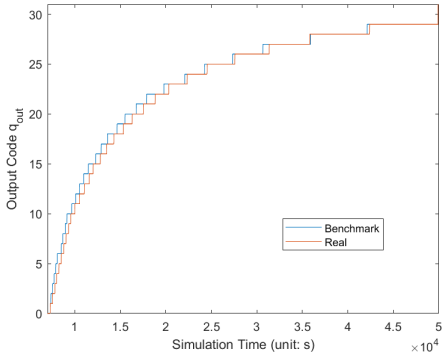
The static response aims to extract DNL and INL as linearity indicators. The obtained results are shown in Fig. 4.14. The three figures on the left, namely Fig. 4.14a, 4.14c, and 4.14e, respectively show the quantization curve, the DNL plot and the INL plot of a single range as a 5-bit ADC. Similarly, the three figures on the right, namely Fig. 4.14b, 4.14d, and 4.14f, respectively show the same items of the full range as a 7-bit ADC. The extreme values of INL and DNL are summarized in Table 4.4.

In Fig. 4.14b, due to the overlap between two adjacent subranges, three missing codes occur at the position of these overlaps. The missing codes are excluded from the DNL calculation because the overlap is not considered a flaw in the subranges.

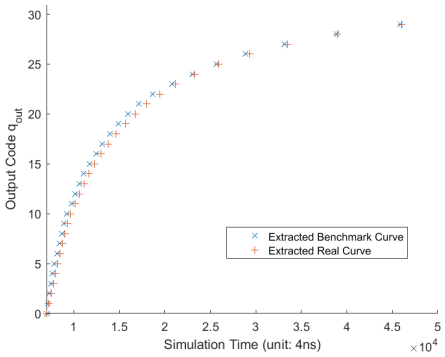
From the mostly positive INL values in Fig. 4.14e and Fig. 4.14f it can be concluded that the quantization curve is convex. The impact of the convex curve can be seen from the frequency response later. Besides, both DNL and INL extreme values are larger for the real curves compared to the benchmark curves, which relates to the non-idealities of the analog delay chain. This phenomenon is elaborately discussed in Appendix B.2. Moreover, the DNL and INL of the full range tests are larger than the single range tests, which relates to the missing codes when the input jumps between subranges. However, the extreme values all meet the test targets, which concludes that the proposed system passes the static response test.

4.3.3. Frequency Response

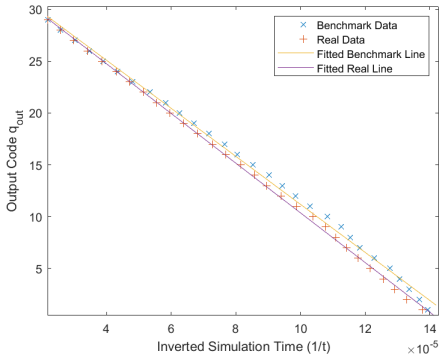
The spectra of relevance, defined as the spectra below $f_s/2$, are presented in Fig. 4.15. Fig. 4.15a-4.15d respectively show the frequency response of the 10 kHz, 100 kHz, 1 MHz and 1.3 MHz inputs. In these



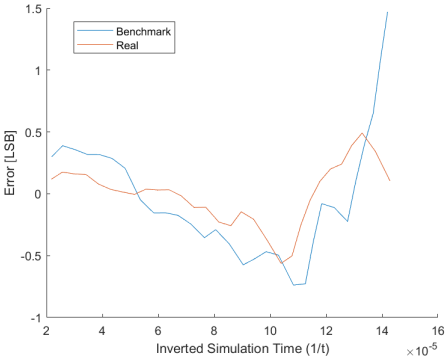
(a) Obtained curve.



(b) Reduced curve.



(c) Reduced curve after axis transformation.

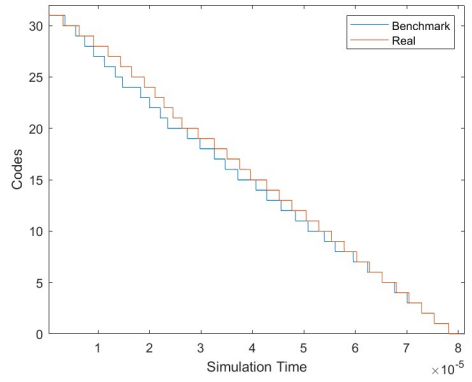


(d) Regression error.

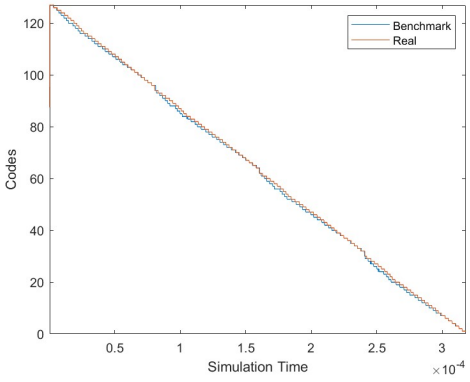
Figure 4.13: Linear input response.

Table 4.4: Test results of the static response (unit: LSB). 'Single' and 'Full' represent the single range test and full range test, respectively. '-' and '+' represent the negative and positive extreme values respectively.

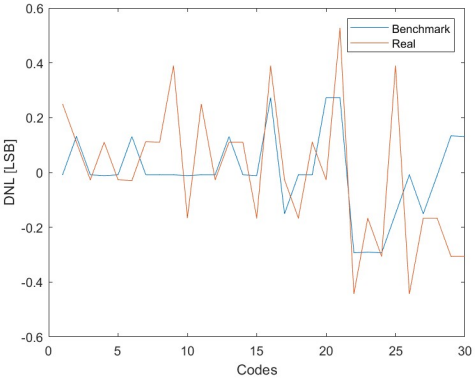
		Benchmark	Real
DNL	Single	-0.29/+0.27	-0.44/+0.52
	Full	-0.45/+0.36	-0.72/+0.64
INL	Single	-0.26/+0.93	-0/+1.91
	Full	-0.51/+1.26	-0.23/+2.49



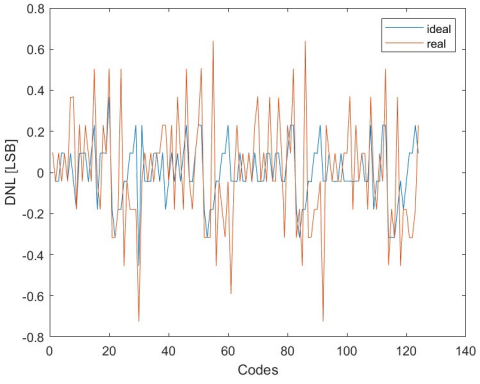
(a) Single Range Response.



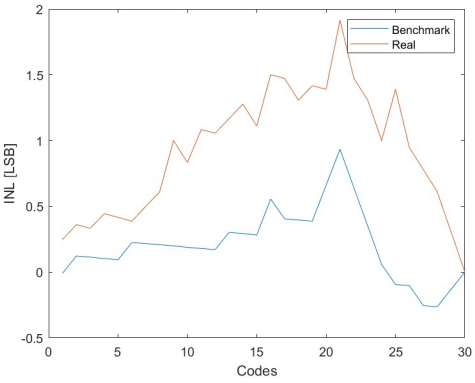
(b) Full Range Response.



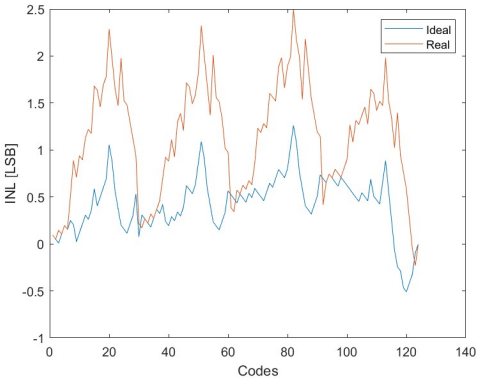
(c) Single Range DNL.



(d) Full Range DNL.



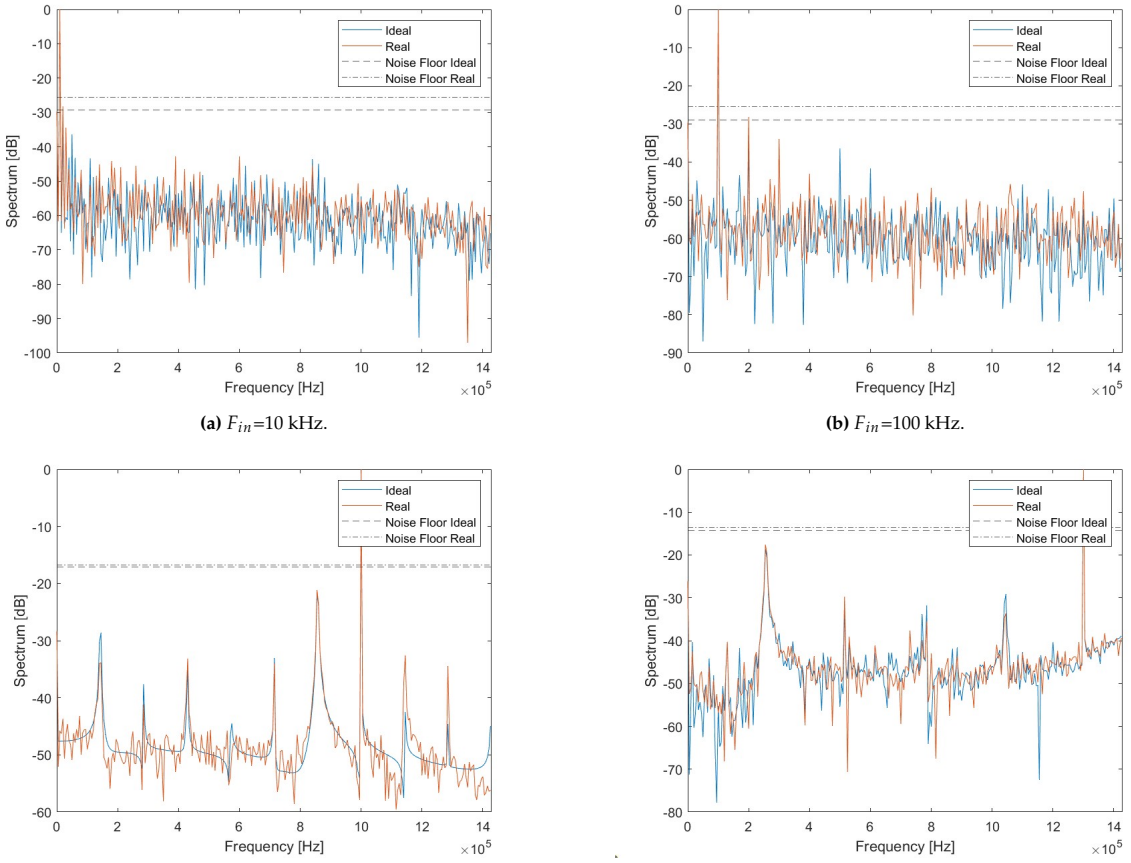
(e) Single Range INL.



(f) Full Range INL.

Figure 4.14: Static Response.

figures, the effects of non-linearities are illustrated by the large harmonic components. The spectra of F_{in} = 1 MHz and F_{in} = 1.3 MHz both have large harmonic distortion components, which show that this ADC is not suitable for high-frequency measurements. On the other hand, the two low-frequency spectra are rather reliable but also suffer from linearity problems.



(a) F_{in}=10 kHz.

(b) F_{in}=100 kHz.

(c) F_{in}=1 MHz.

(d) F_{in}=1.3 MHz.

Figure 4.15: Spectra of Frequency Response.

The SNDR and ENOB figures are summarized in Table. 4.5. The figures show that the Benchmark system achieved $ENOB$ = 4.5 when the input frequency is 10 kHz. This outperforms the requirement of $ENOB$ = 4. After applying analog delay components, ENOB will degrade to $ENOB$ = 3.96, which slightly underperforms the requirement.

Table 4.5: Table of ENOB and SNDR.

F_{in}	SNDR [dB]		ENOB	
	Benchmark	Real	Benchmark	Real
10 kHz	29.23	25.64	4.56	3.97
100 kHz	28.90	25.46	4.51	3.94
1 MHz	17.06	16.74	2.54	2.49
1.3 MHz	14.22	13.61	2.07	1.97

The estimated power consumption from the simulation is 187 µW, without the power consumed by the digital blocks. By substituting $ENOB$ = 3.97, P = 187 µW, and F_S = 2.86 MHz into Equation 4.14, FoM is found to be 4.17 pJ/conv-step.

4.4. Conclusion

It can be concluded from the test results above that the system achieved the design targets. First, the TDC exhibits a hyperbolic pattern with acceptable errors. Second, at low sampling frequencies such as 10 kHz and 100 kHz, the benchmark system achieves ENOB=4.5, DNL bounded to ±0.5 LSB, and INL bounded to ±1.5 LSB. The system with analog DTC achieves ENOB=3.97, FoM=4.17 pJ/conv-step, DNL bounded to ±0.8 LSB, and INL bounded to 2.5 LSB. Considering the dedicated application majorly takes DC input and a small number of measurements, the system can be concluded as usable for the application. However, the system with an analog DTC slightly underperforms the ENOB and INL requirements. The problems have clear causes and can be improved in future versions. The causes of degradations will be discussed in Chapter 5.

5 Conclusion

In this thesis, an alternative ADC solution for an MPPT application in a PV-PMIC system has been proposed. The proposed solution adopts capacitive current sampling and an alternative SA-TDC to cancel the non-linearity of the current sampler. The system parameters and obtained results are summarized in Tab. 5.1.

Table 5.1: System parameters/results.

System Parameters/Results		Value	Units
Current Sampler	Total Sampling Capacitance	460	μF
	Input Range	1.5-15000	μA
	Maximum Sample Rate	2.86	MHz
	Minimum Sample Period	350	ns
	#Input Subranges	4	
	Subrange 1	1.5-15	μA
	Subrange 2	15-150	μA
	Subrange 3	150-1500	μA
	Subrange 4	1500-15000	μA
SA-TDC	Stage Delay	1.3	ns
	# of Delay Stages	96	
	Supply Voltage	1.8	V
Benchmark ADC Performance	Resolution	5	bits
	ENOB	4.5	bits
	DNL	-0.45/+0.36	LSB
	INL	-0.51/+1.26	LSB
ADC Performance	Resolution	5	bits
	ENOB	4	bits
	DNL	-0.72/+0.64	LSB
	INL	-0.23/+2.49	LSB
	Power Consumption (Estimate)	187.2	μW
	Walden Figure-of-Merit (FoM)	4.17	pJ/conv-step

The proposed system has several unique advantages compared to SAR-ADCs. First, the proposed design reduces the requirements for analog components. For example, in SAR-ADCs, a low comparator offset voltage is a key requirement for most of the designs. However, in the proposed design, the comparator offset can be compensated by trimming the time reference generator. Second, the proposed design avoids using large capacitors as the reference generator. Instead, the capacitor is used as the sampling component, and quantization is completed in the time domain with delay references. As a result, the large sampling capacitance in the proposed circuit is more flexible in size. Methods to reduce the size of the sampling capacitance can be found in Appendix B.4. Moreover, the proposed circuit is more compatible with more advanced CMOS technologies, as the lower source voltages and reduced

analog gains are not a limiting factor for the proposed TDC solution.

5.1. Contributions

This work proposed a new solution to the problem of preserving system linearity despite existing non-linearities in some components. As shown in Chapter 3, strong non-linearity usually forms a hindering factor preventing the use of linear components in the measurement system. However, the proposed work illustrates that for some well-known non-linearities, the negative effects can be compensated in low accuracy measurement systems. To the best of the author's knowledge, the proposed solution to the $1/x$ non-linearity is so far unique. Although nonlinearity cancellation techniques, or similar nonlinearity digitization techniques, were also mentioned in other works [29], those solutions are not capable of solving the particular problem in this thesis because they do not target the $1/x$ non-linearity.

Besides, this work elaborated on the possibility of using TDC as the measurement component in low power MPPT application. Due to the stringent area and power requirements, most designs for such application adopts SAR-ADC architecture. In those designs, voltages are usually the conversion quantity for digitization. However, this work illustrates the possibility of using time delay as the conversion quantity. Moreover, when being applied in an MPPT algorithm, the sampling frequency is usually much lower, and the power consumption of the proposed system would also reduce. An example of power estimation in an MPPT algorithm can be found in Appendix B.3.

5.2. Features

The features of the proposed system include high proportion of digital circuits, being clock-free and supporting responses on demand.

The high proportion of digital circuits results from the fact that the proposed system includes only two types of analog components, the current sampler and the delay chain. The delay chain can be designed as digital component without damaging the performance, therefore the only component that requires analog design is the current sampler. The advantage of the high ratio of digital circuits is the performance will improve with advancing CMOS technology. The more advanced CMOS technologies can result in reduced loop delay and increased TDC accuracy, which directly result in higher performance.

The clock-free feature comes from the adopted control scheme. As the system only needs to respond to either of a 'TDCone' event or a 'TDCzero' event, the clock signal is in principle not necessary. Generally, TDCs require clock signal to provide synchronocity. However, the clock frequency needs to match the TDC resolution in order to operate properly. Therefore, if the proposed system with t_d = 1.3 ns were to adopt a clock signal, it would require a clock signal with $F_{clk} = 1/(1.3ns) = 760$ MHz. This frequency is too high for the application as low clock frequency is required to reduce power consumption. Therefore, the system is deliberately made without clock signal. This has negative impact on comparator power consumption, because the low power comparitor solution such as Strong Arm Latchs cannot be used, and a 5-transisitor OTA, which is a continious time comparator, is used instead. The absence of the clock signal introduces uncertainty to loop control logic. However, for the 5-bit SA-TDC in the required application, the pulse swallowing can be handeled in a separate scenario in the loop control circuit. The benefit of not using a clock is that the TDC resolution is no longer limited by clock signal, which enables the low power application to adopt TDC structure.

The response-on-demand feature is the desired property of the low power application. The proposed system starts a measurement at the positive edge of 'EN' pin, and after a measurement, it will suspend until another positive edge of 'EN' pin. Although the continuous time components such as the comparator will dissipate power during suspension, they can be designed as a controlled comparator to reduce the static power during the suspension. Therefore this system can be designed suitable for an IoT application that requires the response-on-demand feature.

5.3. Future Work

The first limitation of the proposed system is the linearity. Although it fulfills the requirements and can be tolerated by the application, improving it is still beneficial as the reading of the charging current would become more accurate. A more accuracte measurement can serve other purposes. Moreover, the trade-offs of the power consumption and area occupation can also be improved. A detailed discussion

of performance limiting factors can be found in Appendix B.4.

Besides, the proposed system requires calibration or trimming to reduce the remaining non-linearity. Usually, TDC architectures require calibration structure to reduce the impact of mismatches and PVT variation [20]. The calibration method required by the proposed system only needs to address some additional considerations regarding the specialties of the proposed algorithm.

It is also helpful to improve the hard-coded reference scheme by using a storage element. The storage elements store the reference weights as numbers. When the SA-TDC control logic request the next reference weight, the storage presents the stored number according to the proposed reference scheme. The improvement compared to the current version is that the numbers in the storage can be updated, which offers some freedom for adjusting the curve. The adjustment can be used for calibration purposes or creating inverse for other non-linear functions. This also shows that the proposed system is not limited to solve the dedicated problem, but can also be extended to solve other similar problems.

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A

Source Codes

A.1. Reference Scheme Calculation and Evaluation

```
%% This code generates and assesses the Non-Linearity Canceling TDC. Simple schematic
    parameters are included for convenience.
clear all; clf; close all;
%Part I: Obtain the TDC curve
V=1;    %Threshold voltage. Adjustable
C=20e-12; %Sampling capacitor. Adjustable
Imin=1.5e-3;
Imax=15e-3;
Istep=(Imax-Imin)/31;   %Calculate step size base on minimum or maximum current
Irange=   Imax:-Istep:Imin;  %Get each datapoint in I range
n=length(Irange);          %the number of data points.
nStage=32;                     %The number of stages in TDC. Not important

x=zeros([1 n]);
Diff=x;                         %The TDC array, unit = second
Diff(1)=C*V/Irange(1);          %Set the first element in Diff to offset
for ind =1:length(Irange)        %Calculate the rest of Diff
   I=Irange(ind);
   x(ind)=C*V/I;
   Diff(ind)=x(ind)-x(max(ind-1,1));
end
Tclk=0.05e-9;                %quantization step

VCO=(randn([1 nStage])*0+1)*Tclk;
for ind=1:8
VCO=[VCO,VCO];
end
Diff(1)=x(1);
ClockDiff=(Diff-Tclk)./Tclk;
stem(((ClockDiff(1:n))));


D=(round(Diff/Tclk));             %Round to multiples of Tclk
% for ind=2:length(D)
%     if D(ind)>6
%        D(ind)=round(D(ind)/4)*4
%     end
% end
%end

%Customized D curve
%D=[22     1     1     1     1     1     1     1     1     2     2     2     2     2
    2     2     2     3     3     4     4     5     5    16*ones([1 10])];


%Part II: Testing the obtained Curve
Ttotal=sum(D);
InputCurrent=Imin:(Imax-Imin)/1000:Imax;
```

```
    Result=zeros([1 length(InputCurrent)]);
    Code=Result;
    DigitizedTime=cumsum(D);
    for ind=1:length(DigitizedTime)
        DigitizedTime(ind)=sum(VCO(1:DigitizedTime(ind)));
    end
    %DigitizedTime=DigitizedTime(length(DigitizedTime):-1:1);
    error=1; %Error in C*V, 1 is no error
    DigitizedCurrent=C*V*error./(DigitizedTime);
    for ind=InputCurrent
      current=ind-0e-6*randn;
     if isempty(max(DigitizedCurrent(current>DigitizedCurrent-0.5*Istep)))
       Result(InputCurrent==ind)=min(DigitizedCurrent);
       Code(InputCurrent==ind)=0;
    else
      Result(InputCurrent==ind)=max(DigitizedCurrent(current>DigitizedCurrent-0.5*Istep));
      Code(InputCurrent==ind)=find(DigitizedCurrent==Result(InputCurrent==ind));
    end
    end

    %Part III: Generate and plot results

    %Calculate DNL
      avg_width=-Istep;
      Widths=[avg_width,DigitizedCurrent(2:end)-DigitizedCurrent(1:end-1)];
      Widths=Widths(end:-1:1);
      DNL=(Widths-avg_width)./avg_width;

    %Calculate INL
      avg_width=-Istep;
      INL=(DigitizedCurrent-(Imin:Istep:Imax))./avg_width;
      INL=INL(end:-1:1);

    %Calculate ENOB
    TotalNoise=mean((Result-InputCurrent).^2);
    Power=0.5*Imax^2;
    SQNR=10*log10(Power/TotalNoise);
    ENOB=(SQNR-1.76)/6.02;

    % Convert D to SA-TDC delays (implementation support)
    SA_D=zeros([5 16]);
    index=[];
    Dcopy=D;
    Nbegin=1;
    for ind=1:5
         for ind2=1:2^(ind-1)
            Nbegin=1+(ind2-1)*32/(2^(ind-1));
           Nend=Nbegin+32/2^(ind)-1;
           SA_D(ind,ind2)=sum(D(1:Nend));
           index=[index;Nbegin,Nend];

        end
    end

    SA_D2=SA_D;
    for ind1=5:-1:2
        for ind2=2^(ind1-1)-1:-2:1
                SA_D2(ind1,ind2)=SA_D(ind1-1,fix(ind2/2)+1)-SA_D(ind1,ind2);
        end
        for ind2=2^(ind1-1):-2:2
            if (rem(ind2,2)==0)
                SA_D2(ind1,ind2)=SA_D(ind1,ind2)-SA_D(ind1-1,fix(ind2/2));
            end
        end
    end
    TDCelements=unique(SA_D2)
    %Plot Results

    plot(InputCurrent,Result);
    hold on;
    plot(InputCurrent,InputCurrent);
```

```
118     %title("With Input Error, Tstep=1/16 Tclk");
119     xlabel("Input Current [A]");
120     ylabel("Measured Current [A]");
121     legend(["ADC Result","Reference"]);
122     xlim([Imin,Imax]);
123     ylim([Imin,Imax]);
124     figure(2);
125     plot(InputCurrent,(Result-InputCurrent));
126     title("Error plot");
127     xlabel("Input Current [A]");
128     ylabel("Error [A]");
129     legend(["ADC Result"]);
130     xlim([Imin,Imax]);
131
132     hold on;
133     figure(3);
134     plot(InputCurrent,33-Code);
135     title("Digital Codes");
136     xlabel("Input Current [A]");
137     ylabel("Code");
138
139     xlim([Imin,Imax]);
140     ylim([0 32]);
141     figure(4);
142     plot(-DNL);
143     xlabel("Code")
144     ylabel("DNL [LSB]");
145     figure(5);
146     plot(cumsum(DNL));
147     xlabel("Code")
148     ylabel("INL [LSB]");
149
150
151     figure(6);
152     stem(Diff(1:n));
153     hold on;
154     stem(D*Tclk,"*");
155     xlabel("Array Index");
156     ylabel("Time step size");
157     legend(["Sequence \Delta t","Rounded sequence \Delta t"]);
158     ylim([0 5*Tclk]);
159     figure(7);
160     stem(Diff(1:n)-D*Tclk);
161     hold on;
162
163     D %The normalized clock counts based on the stage delay
```

B

Additional Information

This chapter aims to present detailed discussions that are too long for the body. Section B.1 will explain the polarities in the proposed system. Section B.4 will explain some performance-related factors in the proposed system to detailize the potential improvements.

B.1. Polarities in the Proposed System

This section aims to clarify the potential confusion caused by statements in Section 4.1.3 and Section 4.3.1. Those statements wrote, 'The decoder is selected to inverse the polarity of the code with $q_{sampled} = 32 - q_{out}$ to ensure the positive gain of $\mathrm{d}I/\mathrm{d}q$ so that the increase in q_{out} corresponds to the increase in I.' and 'During this test, some polarity changes are applied to the obtained data curve, ...'. In these statements, the polarity of the system is mentioned. Here is an elaborate clarification of the two statements.

B.1.1. Polarity Choice of the Proposed System

The proposed ADC system is designed to carry out current-to-digital conversion, which connects three quantities, the input current i, the delay t, and the digital code q. The polarity of the proposed system refers to the plus or minus sign of the gain $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}t/\mathrm{d}q$. Polarity is important because it decides when an increase is seen in i, whether a decrease will be seen in t or q. This is usually not a problem in conventional ADC because $q - i$ usually has positive polarity.

The problem is caused by $i - t$ conversion of the system because the delay has the opposite polarity as the current as follows,

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}\frac{C_{samp}V_{ref}}{t} = -\frac{C_{samp}V_{ref}}{t^2} < 0. \tag{B.1}$$

Once t is directly digitized without the reverse polarity, the output q will have the same polarity with t but then opposite to i. This is not a desired property because the larger code refers to the smaller current.

Therefore, the polarity is chosen as $i, t, q, q_{out} = +, -, -, +$, which means that t takes the reverse polarity as q but q_{out} reverses the polarity once more. As a result, the transfer function regarding the first three quantities are

$$t = \frac{C_{samp}V_{ref}}{i}, C, V > 0, \frac{\mathrm{d}t}{\mathrm{d}i} < 0, \tag{B.2}$$

$$q = f(t) = f_q([\frac{t}{\Delta t}]), \frac{\mathrm{d}f_q(t)}{\mathrm{d}t} > 0. \tag{B.3}$$

The last quantity needs a reverse polarity, so $q_{out} = -q$ is applied. Because the eventual output codes are better to be positive, an offset needs to be added so that $q_{out} = 2^N - q$. For our 5-bit ADC, $N = 5$ is substituted in and $q_{out} = 32 - q$.

The explanations above are believed to have clarified the statement: 'The decoder is selected to inverse the polarity of the code with $q_{sampled} = 32 - q_{out}$ to ensure the positive gain of $\mathrm{d}I/\mathrm{d}q$ so that the increase in q_{out} corresponds to the increase in I.'

B.1.2. Problem and Solution in Linear Time Response

The Linear Time Response extracts the curve shape by applying gradually changing bottom plate voltage, which toggles the time delay linearly. This test creates a new scenario of polarity matching among V_{ref}, t_{sim}, t, and q. Note that t_{sim} is the simulation time, which is different from t.

The expectation is $t_{sim} = kt, k > 0$ so that the operation $a = 1/t$ that needs to apply to t can be directly applied to t_{sim} as $a' = 1/t_{sim}$, where a and a' are two quantities that help with linear fitting but have no meaning. But if the polarity is reversed, the transfer function will become

$$t_{sim} = b - kt, k, b > 0. \tag{B.4}$$

The presence of b is because t_{sim} is always positive due to the feature of the simulator. As a result, the attempt to calculate a' will create

$$a' = \frac{1}{b - kt}. \tag{B.5}$$

The linear fitting will certainly fail because a' is not proportional to q.

Many solutions can solve the problem. However, the simplest solution may be as follows: if the inverse a' is not proportional to q, then reverse the polarity of t_{sim} by

$$t_{sim,2} = max(t_{sim}) + \delta - t_{sim}, \tag{B.6}$$

where $max(t_{sim})$ refers to the largest t_{sim} data point, and δ is a small quantity to avoid $t_{sim,2} = 0$ that would hinder the inverse step. After this, $t_{sim,2}$ would regain the linear relationship with t so that $a' = 1/t_{sim}$ is proportional to q. The only undecided parameter is δ, which can be found by rough manual tuning. Moreover, fine-tuning δ is capable of finding the curve that has the minimum regression error. However, since minimizing the regression error is not the main goal, there is no need to fine-tune δ.

The explanations above are believed to have clarified the statement: 'During this test, some polarity changes were applied to the obtained data curve.'

B.2. Explanations of DNL and INL Patterns in Simulation

In Section 4.3.2, the DNL and INL performance of the real system is found to degrade compared to the benchmark system. The causes suggested by the author are outlined below.

First, consider the identical factors and differences between the two systems. Both systems adopt the same algorithm and reference scheme. However, the major difference between the benchmark system and the real system is the ELD. In the circuit simulation, the delay to time converters (DTCs) of the benchmark system are implemented with logic block delay codes but those of the real system are with a delay chain circuit. Therefore, the real system suffers from a larger ELD than the benchmark system. The larger ELD is believed to cause both DNL and INL degradation.

As explained in Appendix B.4.2, the ELD creates errors for the references. If the reference scheme is balanced, the error pattern would be symmetrical for two complementary codes. For example, '0000' and '1111' both suffer from an error of $3t_{eld}$ at the last bit but '0101' and '1010' both suffer an error of $1t_{eld}$. Because the reference of the last decision t_{LSB} is the same for all codes. Then, if the relative error is calculated, the following formula would apply:

$$e = \frac{nt_{eld}}{t_{LSB}}, \tag{B.7}$$

where e is the error ratio and n is the accumulated number of t_{eld}.

However, it can be noticed that the reference scheme of this project, shown in Table B.1, has different values for the t_{LSB}. The reference scheme is not symmetrical and has smaller reference values at the smaller codes. As a result, when symmetrical ELD errors take place, the smaller codes suffer from larger error, which shares the same reasoning as Section 3.4.3. Note that the ELD errors not only impact the last decision but also in the decision of every bit according to the reference taken on each of them.

Combining the factors mentioned above, the phenomenon that the DNL and the INL of the real system become larger than those of the benchmark system can be explained. While other factors may have some influence, their impact is expected to be less significant.

Table B.1: Table of TDC reference scheme.

k	n values															
1	$n(1)$=47															
2	$n(2,0)$=13								$n(2,1)$=33							
3	$n(3,00)$=4				$n(3,01)$=5				$n(3,10)$=20				$n(3,11)$=44			
4	2		2		3		4		7		9		27		45	
5	1	1	1	1	1	1	2	2	3	3	5	5	9	12	26	38

B.3. Power estimation of an MPPT system with the proposed ADC

This section aims to present an example of the actual power consumption of the proposed ADC in an commercially available MPPT system [31]. The proposed system has a power consumption of 187 μW and a sampling duration of 350 ns as discussed in Chapter 5. According to the product datasheet [31], the MPPT cycle varies between 0.5 s and 64 s. It is assumed that during each MPPT cycle, the ADC takes one sample and remains powered off for the rest of the cycle, consuming negligible power.

With these quantities and assumptions, the average power of the proposed system with these MPPT cycles P_{avg} can be calculated as follows:

$$P_{avg} = \frac{P_{ADC} T_{sample}}{T_{MPPT}}, \tag{B.8}$$

where P_{ADC} is the power during the sampling time, T_{sample} is the sampling duration, and T_{MPPT} is the MPPT cycle. The calculation results shows that the actual power consumption P_{MPPT} is 0.13 nW for a 0.5 s MPPT cycle, and 1.02 pW for a 64 s MPPT cycle. These values are six and nine orders of magnitude smaller than P_{ADC}, respectively.

This estimation method has some limitations, as it does not account for the power consumption of digital blocks, and the quiescent power of the ADC is not exactly zero in a chip. However, these results suggest that the actual power consumption in the given MPPT algorithm can be significantly reduced. Therefore, the proposed system largely meets the low power consumption requirement.

B.4. Factors Related to System Performance

This section aims to discuss the potential improvements to the proposed circuits. Before the discussion starts, the reader is recommended to briefly refresh Chapter 3 or recall the governing transfer functions listed below. The transfer function of the proposed ADC is

$$q_{out} = [\frac{I_{in}}{\Delta i}]. \tag{B.9}$$

The result involves the sampling and quantization part. Their transfer functions are respectively

$$t_{in} = \frac{C_{samp} V_{ref}}{I_{in}}, \tag{B.10}$$

$$q_{out} = [f(\frac{t_{in}}{t_d})] \approx [\frac{k}{t_{in}}]. \tag{B.11}$$

B.4.1. Large Sampling Capacitors

As reducing area is the primary goal, the total capacitance should be minimized. The dominating capacitance is the sampling capacitor C_{samp}, which is a fixed factor of C_0. The minimal size of the sampling capacitor directly relates to the TDC stage delay t_d.

In practice, t_d needs to be selected based on the processing delay of the control logic. An estimated processing delay is 4-5 gate delays. Therefore t_d usually needs to be selected as $t_d = 10 \times 50$ ps= 500 ps, which is 10 times the estimated gate delay of 50 ps. The factor 10 is chosen based on the principle of leaving room for adjustments. In that case, C_0 will become 500 fF, and $C_{total} = 1000C_0 = 500$ pF.

The total capacitance is large and an area stringent design with this architecture may need to use one or more external capacitors. There are several techniques to reduce the area of the sampling capacitance.

One way is to use more advanced CMOS technologies, as mentioned in Chapter 5. More advanced technologies can produce smaller t_d and therefore the sampling capacitance can be reduced accordingly. Another method is to scale the time delay t_{in} up to match the desired t_d value. This can be implemented by a current shrinking structure such as a current mirror. Equivalently, a time amplifier that amplifies the input delay can also complete the task [30].

In any way above, the required current-to-time gain is distributed and thus the sampling capacitance can be smaller.

B.4.2. External Loop Delay

The external loop delay (ELD) will cause the delay references to be inaccurate. The biggest problem is that ELD will accumulate and cause input-dependent reference errors. Consider two cases where the first 4 bits are respectively 0101 and 0000, the decision of the fifth bit is based on the following comparisons:

$$t_{in} + t_{ref,2} + t_{ref,4} ? t_{ref,1} + t_{ref,3}, \tag{B.12}$$

$$t_{in} + t_{ref,2} + t_{ref,3} + t_{ref,4} ? t_{ref,1}, \tag{B.13}$$

where the symbol ? represents a comparison between the left side and the right side, as if $>$, $<$ or $=$ needs to be filled in. In case of $>$ is filled in ?, $D[5] = 1$, otherwise $D[5] = 0$.

However, when the signal passes through the logic gates in the loops, some additional delays will be added. The total additional delay of the loops A and B can be denoted as $t_{eld,a}$ and $t_{eld,b}$ respectively. After adding the ELDs, their comparisons become

$$t_{sig} + (t_{ref,2} + t_{eld,b}) + (t_{ref,4} + t_{eld,b}) ? (t_{ref,1} + t_{eld,a}) + (t_{ref,3} + t_{eld,a}) + (t_{ref,5} + t_{eld,a}), \tag{B.14}$$

$$t_{sig} + (t_{ref,2} + t_{eld,b}) + (t_{ref,3} + t_{eld,b}) + (t_{ref,4} + t_{eld,b}) + (t_{ref,5} + t_{eld,b}) ? (t_{ref,1} + t_{eld,a}). \tag{B.15}$$

One note is that $t_{ref,1}$ will always associate with $t_{eld,a}$, because in the proposed system the signal 'Start' always arrives before the signal 'Stop' and $t_{ref,1}$ will always be assigned in the loop 'A'. Further, if $t_{eld,a} = t_{eld,b}$ and both are denoted as t_{eld}, we can see that in the 0101 case, the t_{eld} of the two loops balances each other with only one t_{eld} remaining on the right side. However, in the 0000 case, the t_{eld} will accumulate on the left side and cause the fifth comparison more in favor of a '1' than a '0'. In general, the introduced error for a bit whose previous codes count n_1 '1's and n_0 '0's can be expressed by

$$t_e = (n_1 + 1)t_{eld,a} - (n_0)t_{eld,b} \approx (n_1 - n_0 + 1)t_{eld}, \tag{B.16}$$

where the 1 in $n_1 + 1$ is for $t_{ref,1}$ which is always at the right side. The positive side of this inaccuracy is that the impact depends on the length of the corresponding delay references. If the corresponding delay reference is larger, the ratio $t_{eld}/(kt_d)$ will become smaller. Because of the chosen delay distribution, t_d is large when i_{in} is small, making the results influenced in a smaller scale. On the other hand, t_d is small when I_{in} is large, making the larger error caused by t_{eld} less impacted. This feature makes the system error tolerable for the MPPT application with P&O algorithm because in a real case, MPPT operations on a large charging current require less measurement accuracy to make the correct decision. However, as stated earlier, improving the accuracy is still beneficial to enable applications that require higher accuracy.

In case this needs to be improved, the problem can potentially be solved by a calibration structure. The calibration structure adopts fine delay chains and can balance the two loop branches by adding additional delay on a single side. When one of the A and B loop branches is looped more than the other, the other loop can receive an extra delay to compensate for ELDs.

B.4.3. Edge Detection Hazards

The proposed system adopts dual edge detection, which is usually difficult to implement for synthesizable logic. The dual edge detection problem can be solved by adding a dual-edge-to-pulse converter as shown in Fig. B.1, which has the disadvantage of increasing the gate delay. Besides, the competition between the two channels would also increase the system uncertainty after synthesis. In synthesizable logic, the output registers need to be updated by one combinatorial logic block, which creates the problem that the logic block needs to detect two independent channels. This hazard will occur when the

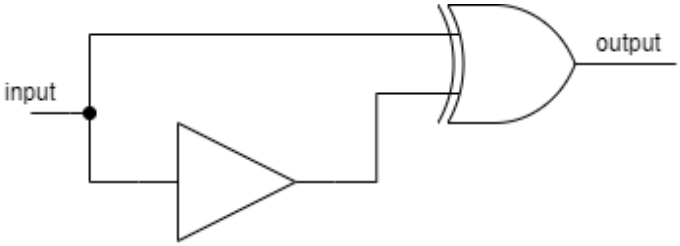

Figure B.1: The dual-edge-to-pulse converter. Whenever the input has a rising or falling edge, the output will create a pulse with a width equal to the buffer delay.

A and B loops create signals 'one' and 'zero' simultaneously, which is comparable with the metastability in SAR-ADC. Although this hazard can be handled as a third case in the SA-TDC logic, named 'one and zero', this solution further creates the difference between 'one and zero' and 'one' after 'zero'. In future work, it needs to be checked whether the accuracy degradation is acceptable for the whole system.

B.4.4. Summary

Above all, the dominating factor to the ADC resolution is the accuracy of t_d and the delay offset t_o. During the simulation, several limiting factors of resolution are found. They are the large sampling capacitors, the ELD, and the edge detection hazards. The sampling capacitors can be reduced in size by using more advanced technologies, a current shrinking structure, or a time amplifier. The ELD can be solved by calibration techniques. The edge detection hazards can be solved by introducing a dual-edge detector or reducing its impact.