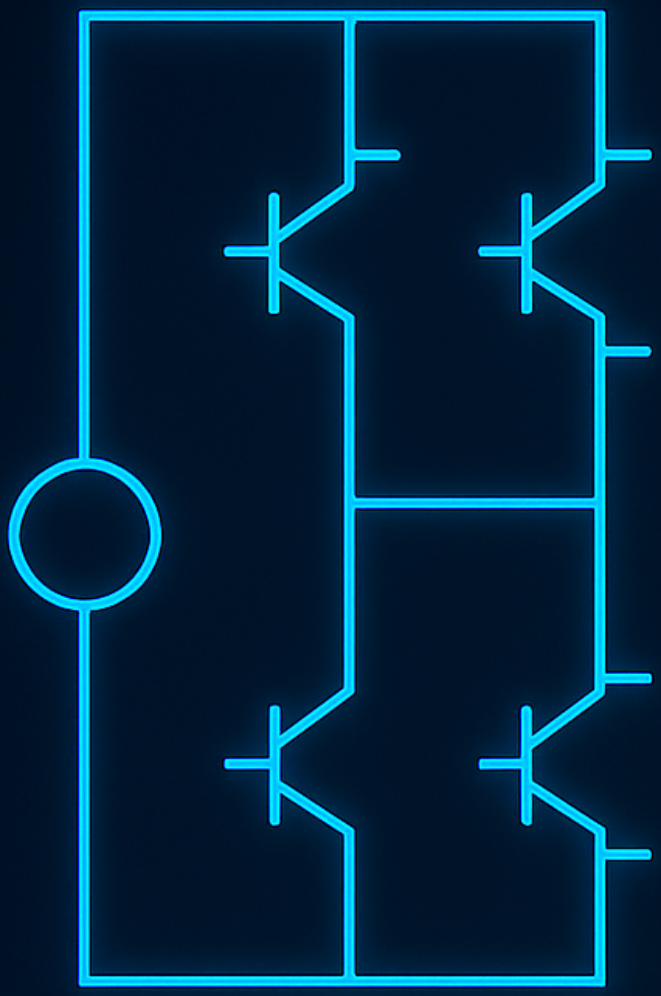

High-frequency switching

Driving circuity for high-frequency transformers

EE3L11: Bachelor Graduation Project

Fimme de Vreeze
Jort Kuiper
Rutger Mevissen

Delft University of Technology

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by
BAP group L
Subgroup switching

Fimme de Vreeze
Jort Kuiper
Rutger Mevissen

Thesis committee members

Dr. ir. Nick van der Meijs
and
Dr. ir. Mohamad Ghaffarian Niasar

Supervisor:	Dr. ir. Mohamad Ghaffarian Niasar
Advisor:	Dr. ir. Hani Vahedi
Project Duration:	April, 2025 - June, 2025
Faculty:	Electrical Engineering, Delft

TU Delft

Abstract

This thesis delves deeper into the design and implementation of a high-frequency DC to DC converter, focusing on the driving circuitry of a transformer based power conversion system operating at MHz frequencies. Because of more demand for smaller, lighter and more energy efficient designs, high-frequency transformers have become an interesting and promising alternative to the standard lower frequency topologies. The project investigates two different topologies, namely: a self oscillating circuit and a GaN based full-bridge inverter. Each of these accompanied by a rectifier stage.

The final prototype successfully operates at a frequency of at least 1 MHz, generating a sinusoidal waveform at the output of the transformer. The system also meet the requirements for achieving an efficiency of 80%, and design criteria such as load independence, compact size and a minimum input voltage of 50 V DC. However, the output power has not reached the desired level of 50 V at 2 A.

The project stresses the importance of precise timing and dead time control in high-frequency switching. While the self oscillating circuit showed promise in LTSpice simulations, it was not pursued due to its dependency on the load connected. Future work should be done to explore an improved component integration, and more advanced control strategies to reach the full 100 W output capability.

Contents

Nomenclature

Abbreviations

Abbreviation	Definition
AC	Alternating current
DC	Direct current
FET	Field effect transistor
FFT	Fast Fourier Transform
GaN	Gallium Nitride
HEMT	High electron mobility transistor
IGBT	Insulated gate bipolar transistor
LLC	Inductor-Inductor-Capacitor
MOSFET	Metal oxide semiconductor field effect transistor
PCB	Printed circuit board
PWM	Pulse width modulation
RMS	Root mean squared
Si	Silicon
SiC	Silicon Carbide
SOC	Self-oscillating Circuit
WBG	Wide-bandgap
ZVS	Zero Voltage Switching

Symbols

Symbol	Definition	Unit
C	Capacitance	[Farad]
f	Frequency	[Hertz]
I	Current	[Ampere]
K	Gain	[-]
L	Inductance	[Henry]
N	Turns	[-]
P	Power	[Watt]
Q	Charge	[Coulomb]
R	Resistance	[Ohm]
t	Time	[Seconds]
V	Voltage	[Volt]
Z	Impedance	[Ohm]

1 Introduction

1.1. Problem definition

In the modern world of power electronics, transformers are used everywhere and play a crucial role in efficiently transferring, converting and isolating electrical energy. From industrial to consumer electronics, transformers play a big role in energy conversion processes. Normally, these transformers operate at frequencies close to the grid, most commonly 50-60 Hz. These kinds of transformers make use of large magnetic cores and bulky windings in order to handle the energy transfer required. However, the increasing need for lighter, smaller and more energy-efficient systems are pushing the limits of low-frequency transformers and call for alternatives that better meet these requirements [6].

To meet these demands, research has turned to high-frequency transformers. Operating at frequencies typically in the range of hundreds of kilohertz and going as high as multiple megahertz allows these transformers to be substantially reduced in size [7]. This reduction automatically translates to an additional reduction of weight of the magnetic component. This can be explained by the fact that higher frequencies allow transformers to utilise smaller core sizes and decreased winding inductances as the energy transfer per cycle becomes more efficient.

It is advantages like these that make high-frequency transformers so interesting in fields like switch-mode power supplies, electric vehicles, solar inverters, and other renewable energy systems where size, weight and efficiency play a crucial role in the design procedure and the performance of the system.

However, high-frequency does come with its own challenges. When increasing the switching frequency, the electromagnetic interference, switching losses and design complexity increase with it [8]. These challenges require the designer, and so also this project group, to pay attention to the entire system, including the design of the switching circuitry, gate drive signals, transformer construction, and the rectification stage.

1.1.1. The project

This thesis investigates the implementation and performance of high-frequency transformers by designing and building a complete DC to DC converter. The project aimes to realize a compact and efficient power converter able to deliver 100 W of output power.

There are three stages which make up the project as a whole. Firstly the driving circuit, this circuit creates the initial waveform from a DC input source. Secondly, connected to the driving circuit, is the transformer. It transfers energy between its input and output, and in the mean time provides isolation. Thirdly, the output rectifier. In order to get back to a stable DC signal from the AC waveform generated by the driving circuit, a rectifier will be used. These components should be carefully chosen in order for the efficiency to be as high as possible and have the most reliable system.

When all of these elements are integrated this projects aims to demonstrate the benefits and reproducibility of high-frequency power conversion.

1.2. Thesis synopsis

This thesis will dive deeper on the driving circuitry of these high-frequency transformers. Specifically topologies like self oscillating circuits and full-bridge drivers utilising GaN transistors will be explored and evaluated while keeping an eye on drawbacks like electromagnetic interference and thermal losses.

1.3. Thesis composition

Six students from TU Delft carried out this project as part of the EE3L11 bachelor's graduation project. This project requires a clearly defined division of labour. Consequently, the team was divided into two subgroups of three: one responsible for the design and implementation of the high-frequency transformer and the other focused on the development of the driving switching circuit as well as the rectifier. Each subgroup produced their own thesis document, both of which can be read as a stand-alone thesis. However for a more comprehensive understanding of the overall project, both documents should be consulted. The focus of this thesis is highlighted dark-blue in Figure 1.1.

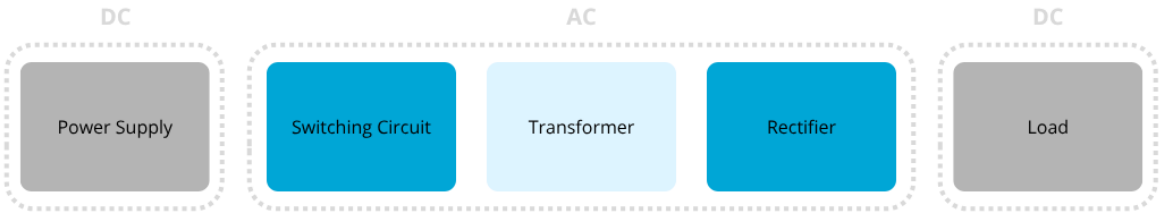


Figure 1.1: Overall project outline.

2

State-of-the-art analysis

This section presents a comprehensive overview of the state-of-the-art technologies in high-frequency switching circuits, including the latest developments in semiconductor devices, converter topologies, control strategies, and integration techniques.

2.1. Semiconductor technology

Traditionally, power converters were built using silicon MOSFETs and IGBTs. However, these are unsuitable for use in high-frequency operation due to high switching losses and relatively slow rise and fall times [4]. Fortunately, these limitations have been overcome by the emergence of wide-bandgap semiconductor technologies, like gallium nitride and silicon carbide devices.

GaN-FET exhibit low on-resistance as well as a small junction capacitance and has a negligible reverse recovery time, enabling it to have turn-on and turn-off speed of several nanosecond. Qualifying this WBG for efficient switching at frequencies well beyond 1 MHz. However during the switching process, the rapid changes in voltage and current can lead to overshoot. Therefore, control parameters should be carefully considered to ensure balance and improve the output performance [9]. Still, GaN surpasses Si and SiC in efficiency for low- to mid-power applications. Meanwhile, SiC, though generally not as fast as GaN, excels in managing higher voltages and maintaining superior thermal stability, making it particularly suitable for high-power systems [19].

SiC is well suited for high-power applications, including automotive and locomotive traction inverters, large-scale solar farms, and three-phase grid converters. In contrast, GaN finds its use in consumer electronics, server and telecom power supplies, as well as industrial systems such as servo drivers, onboard chargers for electric vehicles, and DC/DC converters [5].

2.2. Converter topologies

DC-to-AC conversion can be achieved using three primary topologies: the half-bridge, full-bridge, and class E converters. The full-bridge configuration allows bidirectional transformer operation, utilising both halves of the switching cycle to enhance core efficiency and effectively double power capacity by distributing the load current across two transistors at any given moment. The half-bridge topology, consisting of two transistors, offers a simpler design but applies only half the voltage to the transformer, making it better suited for moderate power applications [17].

On the other hand, class E converters employ a single active switch and a resonant network to enable zero-voltage switching, which practically eliminates switching losses and allows efficient operation at very high switching frequencies. This resonant soft-switching mechanism ensures high efficiency, particularly when using GaN transistors. However, class E designs are generally constrained to lower output power and subject transistors to significantly higher voltage stress [16]. In contrast, half-bridge and full-bridge configurations are more appropriate for handling higher power levels.

2.3. Switching efficiency

Transistor bridge topologies are commonly used to invert the power of a DC supply. These transistors have several losses, namely: gate-, conduction- and switching losses.

2.3.1. Conduction losses

The conduction losses originate from the drain-source current in the transistor in the ON-state. By Ohm's law:

$$P_{conduction} = I_{DS}^2 \cdot R_{DS} \tag{2.1}$$

The current I_{ds} is the RMS-value of the AC current. Reducing the resistance in the channel leads to reduced conduction losses, however this will often lead to a larger channel and thus, more gate charge required.

2.3.2. Gate- and switching losses

The gate- and switching losses increase with frequency. For instance, the losses due to the charging of the gate of a transistor are described in Equation 2.2.

$$P_{gate} = Q_g \cdot V_{DD} \cdot f_s = C_i \cdot V_{DD}^2 \cdot f_s \tag{2.2}$$

Here, P_{gate} is the power loss associated with charging the gate. It depends on the total gate charge Q_g, the gate drive voltage V_{DD}, and the switching frequency f_s. Alternatively, it can be expressed using the input capacitance C_i of the gate. As the switching frequency increases, this loss becomes more significant.

The switching losses are described in Equation 2.3, where $Q_{GD} + Q_{GS}$ are the gate t

$$P_{switch} = \frac{V_{in} \cdot I_{DS} \cdot f_s (Q_{GD} + Q_{GS})}{I_G} \tag{2.3}$$

In this expression, P_{switch} is the power dissipated during switching transitions. It depends on the input voltage V_{in} across the transistor, the drain-to-source current I_{DS}, and the switching frequency f_s. The terms Q_{GD} and Q_{GS} represent the gate-to-drain and gate-to-source charges respectively, while I_G is the gate current. These parameters characterize how much charge is moved during switching and how quickly it occurs.

Resonance circuits can help decrease these losses. For instance, a resonance tank enables efficient gate charging by temporarily storing energy in the resonant components. Switching losses, on the other hand, are caused mainly by power dissipation in the direct current path during transitions. An LLC resonant tank cascaded after the transistor bridge can enable Zero Voltage Switching (ZVS), where the transistor switches when the voltage across it is near zero, thereby minimizing switching losses. For further details, refer to subsection 2.3.3 and section 6.4 [21][18].

2.3.3. Zero voltage switching

ZVS is a widely adopted soft-switching technique in high-frequency power converters that helps minimize switching losses and electromagnetic interference (EMI). Unlike hard-switching, where transistors turn on while a voltage is still present across them, leading to significant power dissipation, ZVS ensures that the switch is activated precisely when its drain-source voltage has naturally resonated to zero. This is typically achieved using an LC resonant network formed by circuit parasitics or intentionally added components, which shapes the voltage waveform so that switching transitions occur under ideal conditions. ZVS not only improves converter efficiency, especially in MHz-range designs, but also reduces thermal stress on switching devices like GaN FETs [10].

In a half-bridge circuit implementing Zero Voltage Switching (ZVS), two distinct operational modes are present. In the first mode, one field-effect transistor (FET) is closed while the other remains open,

allowing power to be transferred to the transformer. The second mode, known as freewheeling, occurs when both FETs are open. In this state, current flows through the body diode of the previously open transistor, causing the voltage across that transistor to decrease until it reaches the forward voltage of the body diode. As a result, the transistor experiences an almost zero drain-to-source voltage (V_{DS}) at the moment it is turned on again. This principle can be seen in Figure 2.1 [14].

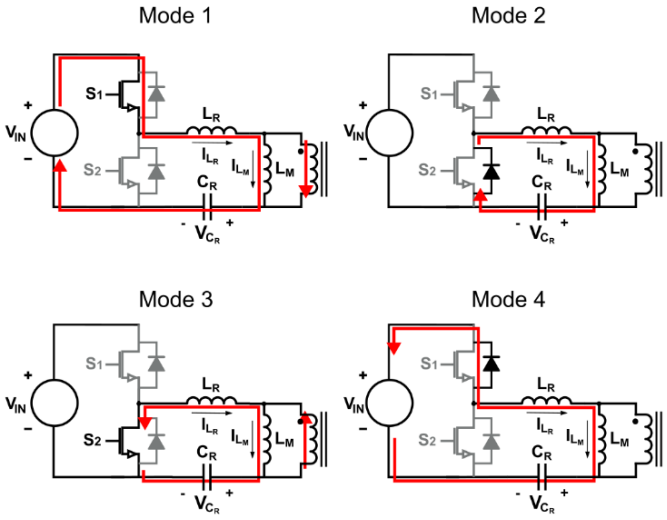


Figure 2.1: ZVS by using an LLC-resonance tank[13].

2.3.4. LLC-resonance tank

Resonant circuits shape the square output into sine-waves as shown below. Moreover if the resonant tank behaves inductive, the current lags voltage. The result is that the transistor will be turned off before the current reverses direction. The current will flow trough the body diode, decreasing V_{DS} and resulting in only a very small forward voltage drop. In capacitive operation the current will switch direction before the transistor is off, the body diode will conduct and when the other transistor starts conducting the diode will have reverse-recovery losses. Inductive operation is achieved by switching at higher frequencies than the resonance frequency

The LLC-tank contains two resonances: L_r with C_r and also Lm with $L_r + Cr$. The performance of the system is thus closely related to the switching frequency. The series resonance (L_r with C_r) will lead to a large gain at the resonance frequency, the parallel resonance will reduce the gain, however if L_m is relatively large then this will occur at low frequencies, which are outside of the frequency range of interest [13].

The paragraphs above indicate that LLC-resonant circuits should be designed such that the switching frequency is higher than the resonance frequency and moreover, the switching frequency is close enough to the resonance frequency that the circuit provides sufficient gain as can be seen in Figure 2.2

Harmonic filtering

The hard switching action in the transistor bridge results in a square-wave voltage output that contains both a DC component and a spectrum of odd harmonics. The resonant capacitor in the circuit blocks the DC component, while the remaining elements of the LLC tank filter out the higher-order harmonics, effectively allowing only the fundamental switching frequency component to pass through. In the case of a half-bridge topology, the amplitude of the fundamental component can be approximated by the following expression:

$$V_{fund} = \frac{4}{\pi} \cdot \frac{V_{in}}{2} \tag{2.4}$$

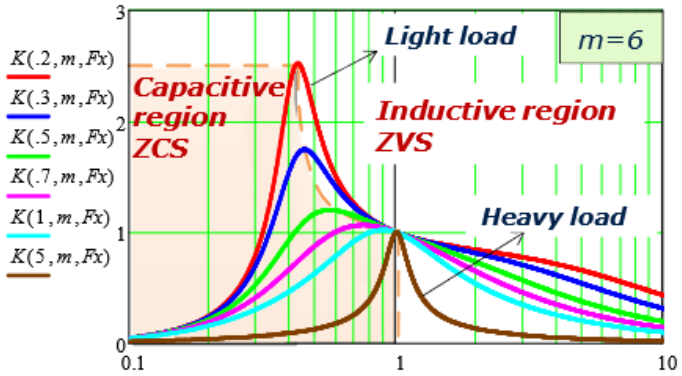


Figure 2.2: LLC-tank gain plot [2].

In this equation, V_{fund} represents the amplitude of the fundamental component of the output voltage, and V_{in} is the input DC voltage supplied to the half-bridge.

The transformer in the circuit is not ideal and exhibits parasitic elements that must be taken into account. Specifically, the primary winding can be modeled as an ideal transformer in parallel with a magnetizing inductance L_m, which represents the inductance required to establish the magnetic field in the transformer core. Additionally, the series leakage inductance models the imperfect magnetic coupling between the primary and secondary windings. At high frequencies, this leakage inductance becomes significant and can be effectively utilized as the resonant inductance L_r in the circuit. Together with an appropriately selected resonant capacitor C_r, the inductances L_r and L_m form the LLC tank circuit.

2.4. Rectification

Rectifying high-frequency AC signals presents unique challenges compared to conventional 50-60 Hz systems. Conventional diode rectifiers exhibit significant reverse recovery losses and constrained switching speeds at high frequencies, leading to reduced efficiency in such applications. To mitigate these drawbacks, ultrafast recovery diodes and Schottky diodes are widely employed due to their low junction capacitance and minimal to negligible reverse recovery time, enabling improved performance in high-frequency power conversion systems.

2.5. Recent trends and challenges

The state-of-the-art in high-frequency switching circuits is rapidly advancing, driven by innovations in WBG semiconductors and resonant topologies. GaN-based full-bridge converters, combined with LLC resonant networks and high-frequency transformers, provide exceptional efficiency and compact designs. However, critical engineering challenges such as electromagnetic interference (EMI), thermal management, and long-term reliability still need to be addressed.

This project aims to contribute to this field by designing, implementing, and evaluating a high-frequency full-bridge GaN switching circuit integrated with a transformer and resonant network. The goal is to experimentally validate performance under real-world conditions and explore trade-offs in design optimization.

3

Programme of requirements

3.1. Subgroup requirements

This BAP project is split in two different subgroups, namely a group that focusses on the transformer part, and a group that focusses on the driving circuit. In this paper the driving circuit will be the main subject. When starting a project like this, it is important to first look at what expectations can be set in order for the final project to be deemed satisfactory. These requirements act as a fall back during the design procedure and make sure that the project does not stray from the original plan.

The requirements are set up by adhering to NASA's product verification model [1].

3.1.1. System requirements

Even though the two subgroups deliver their own respected thesis's and are graded separately. It is still one project, meaning that there are certain requirements which are shared among both the groups. These are called system requirements.

Table 3.1: Whole system requirements and their corresponding validation methods.

System requirements			Validation			
Req. ID	**Statement**	**Value**	**Ana.**	**Insp.**	**Demo**	**Test**
HFT_SW_S_1	The input voltage shall be able to handle a minimum value	50 V	✓	✓	✗	✓
HFT_SW_S_2	The output voltage shall have a fixed value	50 V	✓	✓	✗	✓
HFT_SW_S_3	The output current shall have a minimum value	2 A	✓	✗	✗	✓
HFT_SW_S_4	The system shall have a minimum frequency	1 MHz	✓	✗	✓	✓
HFT_SW_S_5	The system shall fit within a box of specified size	8x8x8 cm	✗	✓	✓	✗
HFT_SW_S_6	The system shall have a minimum efficiency	80 %	✓	✗	✓	✓
HFT_SW_F_1	The system shall function as a DC-DC converter	-	✓	✓	✓	✓
HFT_SW_F_2	The system shall be load independent	-	✓	✗	✓	✓

3.1.2. Driving circuit requirements.

After setting the requirements for the whole system, it is possible (and necessary) to look at specific parts of the project. This is where the subgroups become more isolated. However, it is important to note that many requirements are set up by discussing with the other group to ensure an easier integration process of both systems together.
Below, the requirements of the driving circuit can be found. This circuit will ultimately be connected to the DC input source and at the output to the transformer.

Table 3.2: Driving circuit requirements and their corresponding validation methods.

Driving circuit requirements			Validation			
Req. ID	**Statement**	**Value**	**Ana.**	**Insp.**	**Demo**	**Test**
HFT_SW_S_7	The driving circuit shall take a DC input of at least	50 V	✓	✗	✗	✓
HFT_SW_S_8	The driving circuit shall generate an AC output	50 V_{RMS}	✓	✗	✓	✓
HFT_SW_S_9	The driving circuit shall output a minimum current	2 A	✓	✗	✗	✓
HFT_SW_S_10	The driving circuit shall fit within a box of specified size	8x8x5 cm	✗	✓	✗	✗
HFT_SW_F_3	The driving circuit shall not need cooling	-	✗	✓	✗	✓
HFT_SW_F_4	The driving circuit shall utilize ZVS	-	✓	✗	✗	✓
HFT_SW_F_5	The output of the driving circuit shall be connected to a transformer	-	✓	✗	✗	✓

3.1.3. Microcontroller requirements

Depending on the topology chosen for the driving circuit, the system might need an external PWM generator to drive the switching of a full-bridge inverter. This signal is generated by means of a microcontroller. For a full-bridge inverter this would mean two PWM signals.

Table 3.3: Microcontroller requirements and their corresponding validation methods.

Microcontroller requirements			Validation			
Req. ID	**Statement**	**Value**	**Ana.**	**Insp.**	**Demo**	**Test**
HFT_SW_S_11	The microcontroller shall generate PWM signals of minimum frequency	1 MHz	✓	✗	✗	✓
HFT_SW_S_12	The microcontroller shall create an exact phase shift	180°	✓	✗	✗	✓
HFT_SW_S_13	The microcontroller shall run on a set minimum voltage	5 V	✓	✓	✗	✓
HFT_SW_S_14	The microcontroller shall have a changeable duty cycle	25% - 50%	✓	✗	✓	✓
HFT_SW_F_6	The microcontroller shall be programmable	-	✓	✓	✓	✗
HFT_SW_F_7	The microcontroller shall not need any cooling	-	✗	✓	✗	✓
HFT_SW_F_8	The microcontroller shall generate two PWM signals	-	✗	✗	✓	✓
HFT_SW_F_9	The microcontroller shall operate independently	-	✓	✗	✓	✓

3.1.4. Rectifier requirements

After the transformer, the signal is of AC, sine-like, nature. However to truly become a DC to DC converter, the AC output of the transformer has to be rectified.

Table 3.4: Rectifier requirements and corresponding validation methods.

Rectifier requirements			Validation			
Req. ID	**Statement**	**Value**	**Ana.**	**Insp.**	**Demo**	**Test**
HFT_SW_S_15	The rectifier shall have a maximum reverse recovery time	5 ns	✓	✗	✗	✓
HFT_SW_S_16	The rectifier shall allow a minimum current	2 A	✓	✗	✗	✓
HFT_SW_S_17	The rectifier shall allow a minimum voltage	50 V	✓	✗	✗	✓
HFT_SW_S_18	The rectifier shall not exceed a certain forward voltage drop	2.5 V	✓	✗	✗	✓
HFT_SW_S_19	The rectifier shall be connected to a known resistive load	-	✓	✓	✓	✗
HFT_SW_F_10	The rectifier shall include a smoothening capacitor	-	✗	✓	✓	✗
HFT_SW_F_11	The rectifier shall output a DC voltage	-	✓	✗	✓	✓
HFT_SW_F_112	The rectifier shall take an AC input	-	✓	✗	✓	✓

4

Topology 1: self oscillating circuit

The first topology researched is the principle of a self oscillating circuit. For this instance a standard low voltage module for induction heating was used.

4.1. Self oscillating circuit

4.1.1. Working principles

The self oscillating circuit (SOC) consists of two MOSFETs, two resistive dividers for supplying voltage to the gate, two schottkydiodes connecting the gate of the MOSFET to the drain of the other MOSFET. Additionally the circuit contains an LLC-tank, connected to the drain of each FET and moreover, to the load. This can be seen in Figure 4.1. The physical board is realized by putting two capacitors in parallel, therefore the capacitor in the schematic is denoted as C_1+C_2.

Theoretically the resistive dividers would turn both FETs on and would thus turn off both FETs, by pulling each others gate to ground. In practice, however, parasitic differences in the MOSFETs will cause one FET to trigger earlier than the other. This FET makes sure the other FET is not on, because the gate is pulled to ground via the schottkydiodes. The LLC-circuit, so V_{DS} as well, will charge and then discharge slowly. The gate of the MOSFET that is turned ON is connected to this voltage and as it drops, the gate voltage drops below the threshold voltage. This FET will now turn off and the other one on: the behaviour has flipped. The circuit keeps oscillating this way.

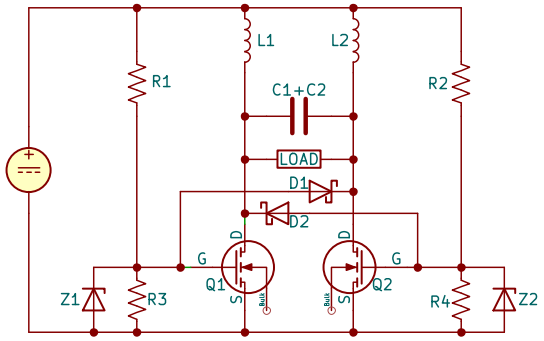


Figure 4.1: Self oscillating circuit.

4.1.2. Resonance frequency under open load conditions

The resonance frequency of the circuit can be analytically derived by examining its behavior during operation. When one of the FETs in the half-bridge is turned on and the other is turned off, the topology of the circuit simplifies significantly. Under this condition, the circuit can be approximated as a basic series LC circuit, as illustrated in Figure 4.2. This simplification allows the use of classical resonance analysis methods.

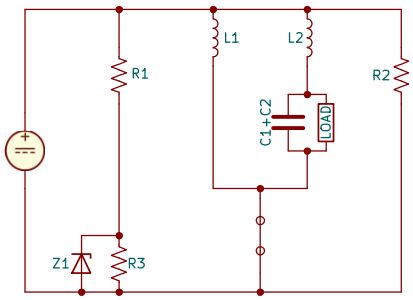


Figure 4.2: Self-oscillating circuit when Q1 is closed.

The corresponding voltage over the load can now be calculated using the circuit in Figure 4.3, where the load is open. The voltage transfer function for the series LC configuration is given in Equation 4.1. This expression is derived based on the impedance division principle, where the voltage across the capacitor V_{out} is computed using the ratio of the impedance of the capacitor $Z_2 = 1/(sC)$ to the total series impedance $Z_1 + Z_2 = sL + 1/(sC)$, multiplied by the Laplace-transformed input voltage V_{DC}/s:

$$V_{out}(s) = \frac{Z_2}{Z_1 + Z_2} \cdot \frac{V_{DC}}{s} = \frac{\frac{1}{sC}}{sL + \frac{1}{sC}} \cdot \frac{V_{DC}}{s} = \frac{1}{s^2LC + 1} \cdot \frac{V_{DC}}{s} \tag{4.1}$$

This transfer function represents a second-order low-pass filter with a resonant peak at the natural frequency of the LC circuit. The circuit's resonance frequency, which is the frequency at which the impedance of the inductor and capacitor cancel each other out, can be determined using the standard formula:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{4.2}$$

In this equation, f_r is the resonance frequency in Hertz, L is the inductance in Henrys, and C is the capacitance in Farads. At this frequency, the reactive components of the inductor and capacitor are equal in magnitude but opposite in phase, resulting in a purely resistive impedance and maximum energy transfer.

This analysis assumes an open-load condition at the output, meaning there is no significant current drawn from the circuit. This simplifies the analysis by removing load-dependent damping effects and allows for clear identification of the resonant behavior inherent to the LC tank itself.

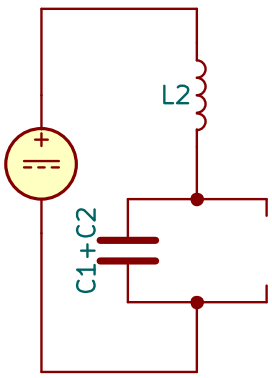


Figure 4.3: Simplified version of self-oscillating circuit when Q1 is closed.

4.1.3. Resonance frequency for loaded output

The resonance frequency of the SOC under a loaded condition, as shown in Figure 4.4, can also be analytically determined. Although the analysis becomes more complex than the open-load case, it can still be approached using established small-signal models [22].

In this configuration, the load is no longer purely capacitive or inductive, but a combination of inductance (L_{load}) and resistance (R_{load}), which interacts with the capacitors $C_1 + C_2$ in the resonant tank. As a result, the transfer function exhibits two distinct resonances: One due to the LC tank formed by the series inductor L_2 and capacitors $C_1 + C_2$. Another arising from the interaction between the load inductance L_{load} and the same capacitors $C_1 + C_2$.

Moreover, the resistor R_{load} introduces damping into the system, represented mathematically by a second-order term involving R_{load} and $C_1 + C_2$. The voltage transfer function is given by:

$$V_{out}(s) = \frac{Z_2}{Z_1 + Z_2} \cdot \frac{V_{DC}}{s} = \frac{\frac{1}{L_2 C}}{\left(s + \frac{1}{2RC}\right)^2 + \frac{1}{L_{load}C} + \frac{1}{L_2 C} - \frac{1}{4R^2C^2}} \cdot \frac{V_{DC}}{s} \tag{4.3}$$

This equation shows that the circuit behaves like a second-order low-pass filter with complex pole dynamics. Here $C_1 + C_2$ is given by one combined C. The denominator is in the form of a damped second-order system, where the damping term is $\frac{1}{2RC}$ and the effective squared angular frequency ω_0^2 is:

$$\omega_0^2 = \frac{1}{L_{load}C} + \frac{1}{L_2 C} - \frac{1}{4R^2C^2} \tag{7}$$

Here, ω_0 represents the angular resonance frequency of the system. This expression includes three contributing components:

- The term $\frac{1}{L_{load}C}$ reflects the resonant effect of the load's inductance with the capacitor.
- The term $\frac{1}{L_2 C}$ comes from the intrinsic LC tank of the circuit.
- The subtraction term $-\frac{1}{4R^2C^2}$ accounts for energy losses due to the resistive load.

For the system to remain stable and oscillatory, the value of ω_0^2 must remain positive, implying that the resistive term must not dominate the combined inductive contributions. If the damping becomes too strong , when R_{load} becomes too small, the expression under the square root may become negative, leading to instability or an overdamped response where no sustained oscillation occurs.

In essence, this formulation provides insight into how the load characteristics directly influence the resonance behavior of the SOC. Designing for a target resonance frequency under load requires careful balancing of L_{load}, L_2, C, and R_{load} to ensure desired performance and avoid instability.

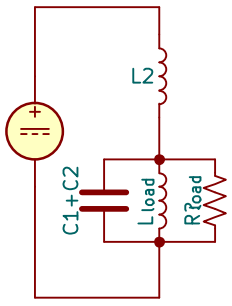


Figure 4.4: Simplified version of self-oscillating circuit when Q1 is closed, with specified load.

5

Topology 2: GaN full-bridge module

The second topology explored is the GaN full-bridge module. To implement a high-frequency full-bridge switching circuit, two Texas Instruments LMG5200EVM-02 GaN half-bridge power stage evaluation boards were used [20]. These boards are rated for a 80 V input and can draw a current of 10 A. First, the operating principles of a single evaluation module are presented; then the interconnection of two such modules to form a complete full-bridge topology is described in detail.

5.1. Half-bridge power module

5.1.1. Working principle

Half-bridge topologies are common in power electronics. They are composed of two switches, each in the form of a transistor. These transistors are connected in series with each other, one side is connected to the voltage supply and the other side to ground. At the midpoint of these transistors, a load is connected. This load is in parallel with the ground transistor. The working principle involves alternating the conduction states of the high-side and low-side switches. This controls the voltage that is applied to the load. Figure 5.1 illustrates how there are three different key switching stages: when the high-side switch is on and the low-side off, when both switches are off, and when the high-side switch is off and the low-side switch is on. The state where both switches are off allows for a controlled dead time between the two other stages. Dead time is essential to prevent shoot-through. Proper timing of the switches is crucial to ensure that this phenomenon is not occuring.

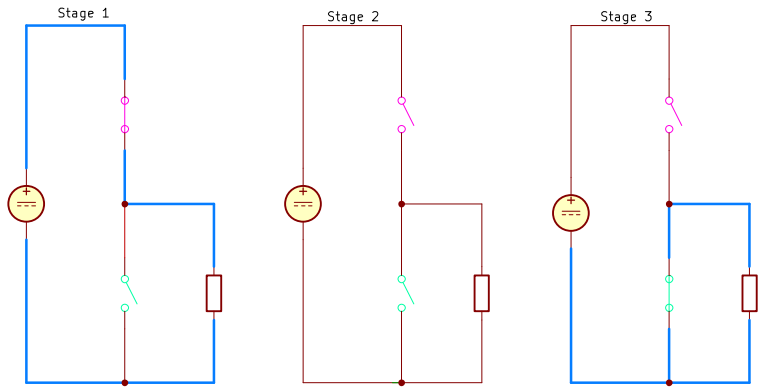


Figure 5.1: Switching stages of the half-bridge circuit.

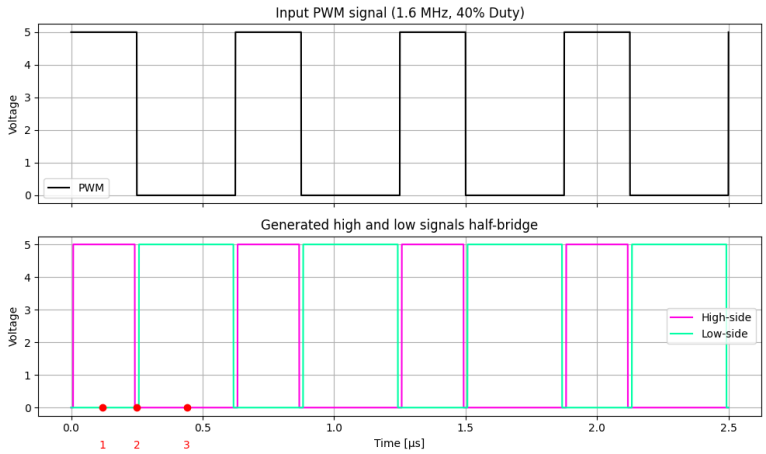


Figure 5.2: PWM signal for the high- and low-side, generated by the board.

5.1.2. Shoot-through

A shoot-through is a faulty stage that occurs when both the high-side and low-side switches are conducting at the same time. The moment this happens, the load is short-circuited, and current can directly flow from the source to ground. This current is often so large that it damages components like the transistors.

In order to minimise the chance of shoot-through, these topologies utilise a specified dead time between the switching of stages. This dead time can be observed in Figure 5.2 and Figure 5.1, where stage two is the dead time stage. One can easily see how making sure that both switches are not conducting can prevent any short circuit from occurring.

Even though dead time is a necessity, excessive dead time can reduce system efficiency due to extended periods where none of the switches are conducting and no power is provided to the load. It is clear that dead time must be calibrated carefully and accurately, depending on the switching characteristics of the transistors used.

5.1.3. Dead time generator

Nowadays many modern development boards which are used for driving half bridge circuits include built-in dead time generator circuits as part of their gate driver circuitry. These generators are hardware based and automatically restrict the PWM pulses driving the switches to not have any overlap between the high-side and low-side signals. This ensures that no matter the PWM duty cycle provided to the board, there is no chance for shoot-through to happen.

By utilising this mechanism, the board will be limited to a maximum duty cycle, as the fixed dead time is enforced even when the user-provided PWM duty cycle exceeds the maximum switching speed that the transistors can achieve. This feature significantly enhances the overall system reliability.

Figure 5.3 shows the dead time generating circuit of the Texas Instruments LMG5200EVM-02 GaN half-bridge power stage evaluation board. The PWM control signal is provided on pin 4 of J5; the rest of the pins are connected to ground. It also shows how the pwm signal gets split into a high and a low signal which is passed through to the gate driver of the GaN transistors.

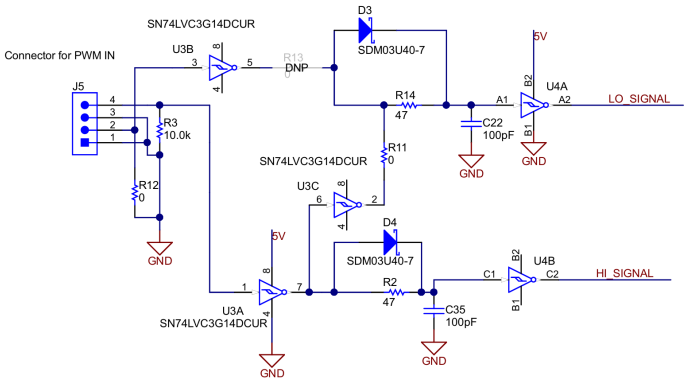


Figure 5.3: Dead time generating circuit [20].

5.2. Full-bridge power module

5.2.1. Working principle

The inner workings of a full-bridge inverter, also known as an H-bridge, extends on the concept of a half-bridge topology. However, in a full-bridge configuration, there are four transistors connected in an H-shaped arrangement, as shown in Figure 5.5. The load is connected between two midpoints of the legs of the bridge. By alternating which pairs of transistors conduct current, the inverter can apply both positive and negative voltages to the load. Meaning that the voltage swing of the H-bridge is twice that of the half-bridge, and utilises more of the power supply.

The operation of the H-bridge involves switching the diagonally opposite transistors together. Stages 1 and 5 shown in Figure 5.5 illustrate the two conduction stages which exist for a full-bridge under normal operation. By setting either one of the high side switches and the opposite low side switch to the conduction mode, a current can flow through the load. The inverter produces a square wave AC output, which fluctuates around zero in both the positive and negative values when observing from the load. As for the half-bridge the full bridge is controlled by two PWM signals, one per board. The second PWM signal is ultimately phase shifted by 180°, such two signals are shown in Figure 5.4. Here two signals with a deliberate exaggerated non-ideal phase shift are shown for worst case scenario analysis in subsection 5.2.2.

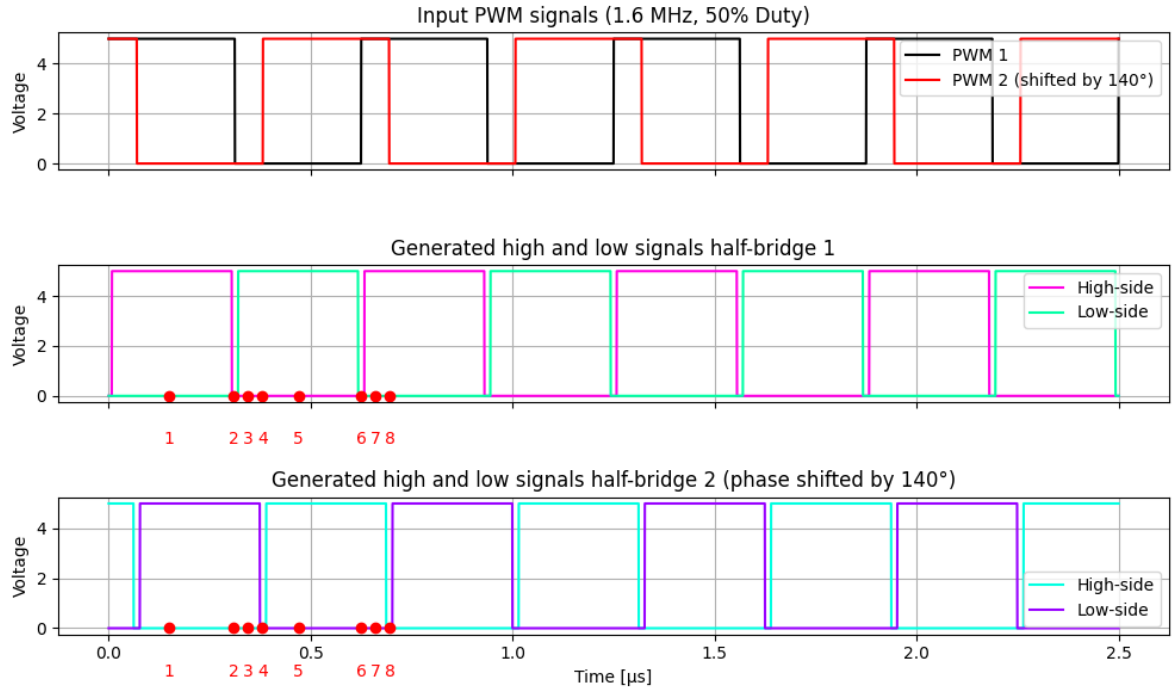


Figure 5.4: PWM signal for both boards for the high and low side, generated by the board.

5.2.2. Shoot-through

In the same manor as with the half-bridge, shoot-through can occur when there is a straight path from source to ground. This occurs when both the high-side and low-side switches of the same leg conduct simultaneously, most likely damaging them in the process.

Knowing that a full-bridge consists of two legs, each with a pair of switches, it can be easily seen that the risk of shoot-through exists in both sides. This means that the timing of the signals driving the transistors must be very precise. However, the risk of shoot-through only determined by one leg. Thus, connecting two half-bridges to form a full-bridge does not lead to a higher chance of shoot-through. This can be clearly seen in Figure 5.4 and Figure 5.5. The highest possible number of switching stages that is eight and this can only be reached when using to PWM signals which are not perfectly aligned, resulting in overlap high-side with high-side instead of solely overlap in low-side with high-side. When

using a lower duty cycle or a better phase shift, the number of different stages will decrease, as less overlaps are created. The timing of all the possible different stages are indicated in Figure 5.4 and in Figure 5.5 the circuits paths are illustrated respectively. It is visible that there exist a closed loop only in stages 1 and 5. More importantly it is visible that there exist no stage where there is a direct path from source to ground. Even when both top and bottom switches are on, no shoot-through will occur. This is again because shoot-through only occurs when two switches in one leg are closed simultaneously, and the built-in dead time generator mitigates this risk.

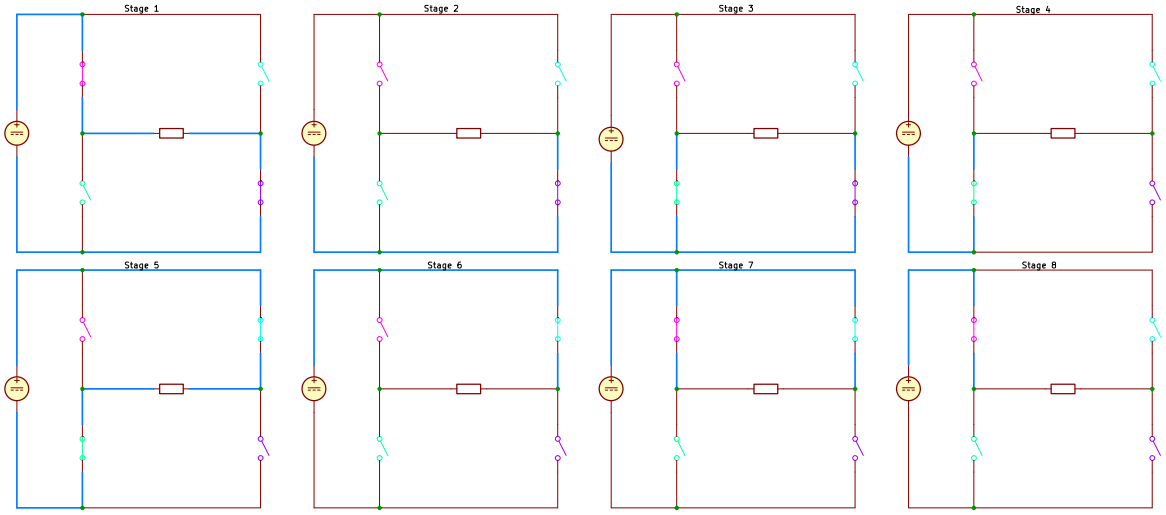


Figure 5.5: Switching stages full-bridge circuit.

5.2.3. Dead time

Dead time, much like shoot-though, works by the same principles in a full-bridge as in a half-bridge. Maintaining a period of non-conduction minimises the chance for shoot-through to occur. However, as stated before in subsection 5.1.3 the development board used in this project maintains a maximum dead time. This means that shoot-through will not occur, even when providing a PWM signal that does not incorporate dead time. When the connecting two of these boards together and looking at the different stages that it can take in Figure 5.5 and Figure 5.4, it can be seen that the only stages which conduct current are the ones that place a voltage over the load. However, this being said, there are more stages where no current is flowing. Even though these stages will not damage the components, it still effects the efficiency of the whole system.

5.2.4. Combined power

Given the connected full-bridge now the full swing of the DC power supply can be used. When supplying a voltage of 52 V, the voltage across the load will now switch between +52 V and -52 V, resulting in a total voltage swing of 104 V. This creates a higher power density compared to when only voltage is applied for half of the time. The total output voltage can be adjusted by varying the duty cycle. The total V_{rms} is defined by the area under the graph, and as the duty cycle increases, leading to a longer on-time, this area will increase as well, resulting in a higher V_{rms} on the output. Ideally the V_{rms} will be as close as possible as the input voltage to reach the highest efficiency. Thus, the PWM needs to be set as close as possible to the maximum of 50 percent. As stated in subsection 5.2.2, this will not increase the chance of shoot-through since the boards have a built-in dead-time generator.

5.2.5. Overshoot

Due to the extremely fast switching transitions, the resulting voltage overshoot must be carefully considered to ensure that it does not exceed the voltage and current limitations of the circuit board. When switching signals at high frequencies, such as 1.6 MHz, and relatively high voltages, the presence of parasitic inductance in the circuit layout, particularly in wires and PCB traces, becomes a significant concern. According to the fundamental voltage–current relationship of an inductor, as shown in Equation 5.1, a rapid change in current leads to a substantial voltage across the inductive elements. Consequently, during fast switching events, the abrupt variation in current induces voltage spikes, resulting in overshoot or oscillatory ringing at the switching node.

To mitigate the risk of damaging the circuit, it is essential to minimise parasitic inductance, for example, by reducing the length of current paths immediately after the switching elements. However, layout optimisation alone is often insufficient to guarantee safe operation. An additional current path must be provided to safely absorb or redirect transient energy. This can be achieved through the implementation of a snubber circuit or a resonant LLC circuit. Given that one of the project's objectives was to achieve soft-switching, an LLC resonant circuit was designed and implemented to effectively reduce voltage overshoot while improving switching efficiency.

$$V_L(t) = L\frac{di(t)}{dt} \tag{5.1}$$

5.3. Control

In order to drive a half- or full-bridge inverter, one or more PWM signals have to be generated. In this section the focus will be mostly on the implementation of control on the full-bridge topology, as this is ultimately what will be used for the remainder of the project, and utilizes the same working principles as a half-bridge with a few additions.

5.3.1. Signals

Driving the two connected half-bridges independently requires two PWM signals which are 180° out of phase. This phase shift ensures a clean transition between the stages described in subsection 5.2.3. Not only the phase shift has influence on the efficiency of the system, the duty cycle and dead time also play a major role. In general, to get the highest efficiency possible, the system should spend as little time as possible in the non-conducting stages.

In this project these signals were generated using an Arduino UNO. This board is easy to configure, capable of reaching speeds in the megahertz range, and does not require additional cooling or an external signal to function.

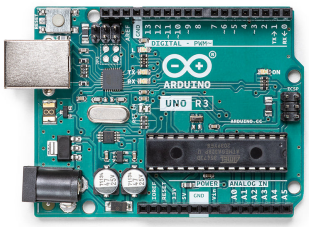


Figure 5.6: Arduino UNO microcontroller [3].

5.3.2. Achieving MHz frequencies

To generate PWM signals with frequencies in the MHz range, the code used has to refrain avoid delays caused by high-level functions and operate only close to the hardware itself. The complete code can be found in appendix [A].

Normally when writing to a pin using Arduino, the command DigitalWrite() would be used. However, this command can not be used in MHz operations as it simply takes too many clock cycles to complete. Another, much faster, way of setting a pin high or low, is by means of PORTD. Directly writing to the pin in just a couple cycles.

In order to create a square wave signal the Arduino has to wait a set amount of time before moving on to the next instruction. In slower applications this can be done by means of the sleep() instruction, but this, again, is too slow for this projects use case, and does not provide the amount of freedom in generating signals of different lengths as wanted. Instead a "nop", or no-operation, instruction is used. This instruction stalls the program for once clock cycle at a time which means 62.5 ns on a 16 MHz Arduino UNO.

6

Implementation

6.1. Topology 1: self oscillating circuit

6.2. Test setup

To evaluate the performance of the self-oscillating circuit, the experimental test setup shown in Figure 6.1 was utilized. Several custom-wound inductors with different inductance values were fabricated to test the circuit under various loading conditions. The test setup consisted of the following equipment:

- A Delta Elektronika M52-30 power supply, used to provide an input voltage in the range of 12–30 V to the self-oscillating circuit.
- A Rigol MSO5354 digital oscilloscope for monitoring the system's dynamic performance and waveform analysis.
- One Pico TA057 differential probe for precise voltage measurements at the circuit output.
- A set of self-fabricated inductive loads with varying inductance values to evaluate the circuit's oscillation behavior under different conditions.
- A selection of resistive loads for characterizing performance across a range of load impedances.

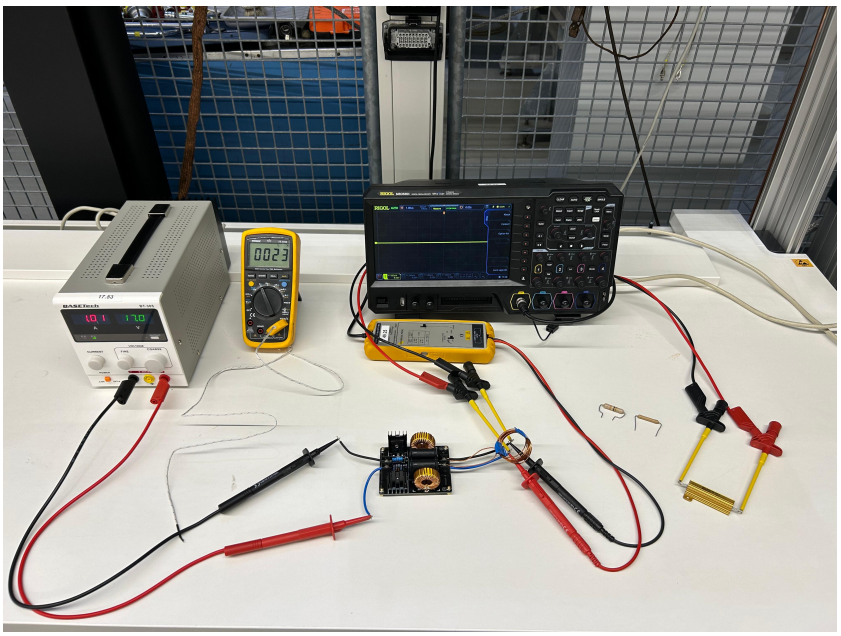


Figure 6.1: Test setup for the self-oscillating circuit.

6.3. Topology 2: GaN full-bridge module

6.3.1. Assembly and inspection of the full-bridge driver boards

In order to implement a full-bridge inverter topology, two development boards, both containing a half-bridge, were assembled and connected. Surface mount components were soldered using solder paste applied using a stencil.

After carefully placing the components manually in the desired locations, the board was placed in a temperature-controlled oven to ensure that the solder paste would be heated up uniformly and form a strong solder joint. Once this first side of the board was completed, the second side was soldered using the same principle. However, in order to prevent direct contact with the oven floor, metal stand-offs had to be used, as seen in Figure 6.2. This to ensure that the components of the already soldered side, which now finds itself upside down in the oven, do not come off during the second reflow process. This method works since the solder paste does not flow as easily after already being soldered once, keeping all components secured to the board.

Figure 6.2: Evaluation board in the oven with metal stand-offs.

Prior to connecting the two half-bridge boards to form a full-bridge circuit, a small modification was needed. An onboard inductor, which was part of the original rectification stage, was removed to disable the rectifier functionality. The pad that was left behind could then be repurposed as a convenient electrical connection point to link the outputs of the two half-bridges, thereby completing the full-bridge configuration

Post soldering, an inspection had to be conducted in multiple stages to ensure the proper functionality of the PCB. These stages include a visual inspection to verify alignment and solder quality, electrical continuity testing using a multimeter, and to conclude, a full functional test of the assembled circuit. During the testing phase it became clear that component U4, partly responsible for maintaining a 5 volt bias voltage, was not seated correctly. However, after using a hot air soldering station, the chip was re-soldered to ensure a good connection.

After observing the failure rate of these development boards, it was determined that maintaining an excess of spare assemblies would be favourable due to the fragility of certain components. This resulted in two different previously soldered but non-functional boards to be selected for analysis and to attempt a repair.

By utilizing the different test points located across the board, and systematically going over these, it became apparent that there was no signal on TP9 and TP10. This could only mean that component U3 was defective. The location of these points and chips are highlighted in Figure 6.3. Coincidentally this was the case for both boards. This chip is part of the dead-time generating circuitry, meaning that the PWM signal was not being passed through and no switching was occurring.

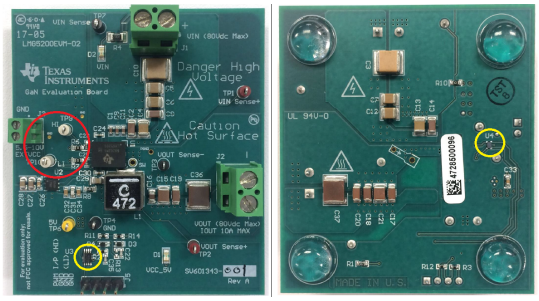


Figure 6.3: Top (left) and bottom (right) view of the development board, where red indicates TP9 and TP10 and yellow chips U3 and U4.

In order to restore functionality to both boards, component U3 was de-soldered and replaced with a new one by making use of a soldering iron, hot air station, and soldering flux to ensure good flow of the solder itself. This, in combination of a digital microscope camera meant the chip could be placed correctly and tested in the same manor as before. This process ensured four driver boards to be confirmed fully operational.

6.4. Method for LLC calculation

6.4.1. Parameters

The design-steps taken in this project have been based on [2] and [13]. For optimal LLC-tank design, several equations should be taken into account:

Quality factor

The quality factor gives insight in the gain of the system regarding the load. For heavy loads, so a high Q, the peak of the system will shift towards the resonance frequency and becomes narrower. Low quality factors have more gain over a broader bandwidth. However, this also leads to less filtering of the harmonics and thus a less sinusoidal waveform. Therefore a compromise should be made in the design of the LLC-tank. In this project the quality factor is chosen as a value between 0.5 and 0.8, because this provides sufficient gain, but also filters enough of the harmonics.

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \tag{6.1}$$

Reflected load

The equation for the reflected load gives insight in how the load at the output R_o is reflected to the primary, accounting for the rectifier and the transformer.

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot R_o = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot \frac{V_o^2}{P_o} \tag{6.2}$$

Normalized frequency

The normalized frequency (F_x) gives insight into the inductive/capacitive regions in Figure 2.2.

$$F_x = \frac{f_s}{f_r} \tag{6.3}$$

Resonance frequency

The equation for resonance frequency (f_r) 6.4 is used in this research for determining the value of C_r that results in a frequency of 1 MHz.

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \tag{6.4}$$

The inductive ratio 'm'

The value of m shapes the gain plot of the system. Higher values of m will flatten the curve. Lower m leads to higher ripple current and circulating magnetizing current, thus conduction losses and so a lower efficiency compared to a higher m with the same Q-factor. Since the peak is higher for low values of m higher gains can be realized.

$$m = \frac{L_r + L_m}{L_r} \tag{6.5}$$

6.4.2. LLC-tank gain function

Finally, the gain of the LLC-tank contains all these parameters. The gain equation is shown below in Equation 6.6.

$$K = \frac{F_x^2(m-1)}{\sqrt{(mF_x^2-1)^2 + F_x^2(F_x^2-1)^2(m-1)^2Q^2}} \tag{6.6}$$

Since a lot of parameters come into play for the design of an LLC-resonant tank, leading to a complex and iterative process. At first, this process was done by hand, see Appendix B, but has been implemented with Python scripts to make it easier, quicker and better visible. This has led to precise fine-tuning of the LLC-tank. See Appendix A for the Python code.

6.4.3. Rectifier circuit

6.4.4. Ideal diode properties

Due to constraints in availability and time, three diode candidates were examined for potential use in the rectifier circuit: the Onsemi MBR1100 axial lead rectifier [15], the Diotec DB25-12 three-phase diode bridge rectifier [11], and the Diotec SB5100 Schottky barrier rectifier diode [12]. Given the requirement to achieve a 50 V, 2 A output, several critical parameters must be considered when selecting an appropriate diode.

Firstly, to enable signal rectification in the MHz frequency range, the diode should exhibit a minimal, ideally negligible, reverse recovery time (t_{rr}). At a frequency of 1.6 MHz, a single clock cycle lasts 625 ns, necessitating a reverse recovery time significantly below this threshold. As the DB25-12 diode has a t_{rr} of 1500 ns, it is deemed unsuitable and consequently excluded from further consideration.

Secondly, the peak repetitive reverse voltage and peak repetitive forward current must be sufficiently high. To ensure the diode can accommodate the target output V_{rms}, it must withstand a peak voltage of at least 70.7 V, excluding transient voltage spikes and ringing effects. To maintain operational safety, the diode should be rated at approximately 1.5 times the peak voltage, equating to a minimum of 106 V. Additionally, the diode's current rating must exceed 2 A. As the Onsemi MBR1100 is rated precisely at 2 A, no safety margin is available, rendering it unsuitable for this application.

Thirdly, minimising losses necessitates selecting a diode with a low forward voltage and junction capacitance. The associated power losses can be determined using Equation 6.7 and Equation 6.8. The Diotec SB5100, with a forward voltage of 0.79 V at 5 A and a junction capacitance of 210 pF, is expected to incur power losses of 1.58 W due to conduction and 0.84 W due to junction capacitance effects, totalling 2.42 W per diode. As two diodes conduct simultaneously in the full-bridge configuration, a nominal power loss of 4.82 W is anticipated.

$$P_{\text{cond}} = V_F \cdot I_{\text{avg}} \tag{6.7}$$

$$P_{\text{cap}} = \frac{1}{2} C_j V^2 f \tag{6.8}$$

6.4.5. Smoothing capacitor

To stabilise the rectified DC output, a capacitor is integrated into the rectifier circuit. The appropriate capacitor value can be determined using Equation 6.9. To enhance efficiency, the desired voltage ripple is minimised and set to 0.5 V, resulting in a 1% ripple on 50 V. The ripple frequency is twice the switching frequency, as the diodes invert the lower half of the waveform. Consequently, the minimum required capacitance is 1.25 μF. Considering safety margins, a capacitor within the range of 2-5 μF should be utilized. Furthermore, the capacitor must exhibit low equivalent series resistance (ESR) to ensure proper functionality at this frequency. In the implemented setup, two parallel 1 μF capacitors were employed.

$$C = \frac{I_{\text{load}}}{f_{\text{ripple}} \cdot \Delta V} \tag{6.9}$$

6.5. Prototype

6.5.1. Circuit design

A prototype was developed to implement the complete system. The prototype comprised the following components, as presented in Figure 6.4:

- A full-bridge converter, constructed using two LMG5200EVM-02 boards [20].
- A capacitor of 10 nF for the LLC-resonant circuit, tailored to the transformer parameters defined by the Transformer subgroup, as outlined in section 1.3.
- A rectifier circuit incorporating a smoothing capacitor of 2 μF.
- A resistive load for system testing.

The prototype employed large, high-voltage metallised polypropylene film capacitors for both the LLC resonant tank and the rectifier smoothing stage. Additionally, it was assembled using relatively wide and long conductor paths to accommodate the large components and facilitate measurement access.

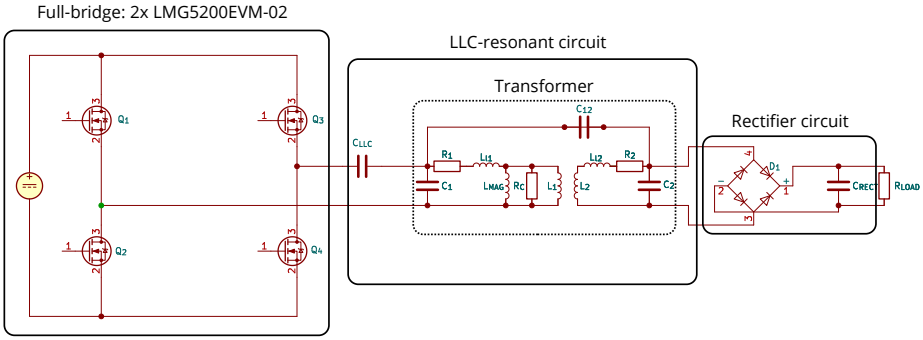


Figure 6.4: Complete circuit design for the GaN full-bridge module.

6.5.2. Test setup

After assembling the circuit as shown in Figure 6.4, the system was prepared for experimental evaluation. The test setup, depicted in Figure 6.5, consisted of the following equipment:

- A Delta Elektronika M52-30 power supply, used to provide a variable input voltage in the range of 25–50 V.
- A Basetech BT-305 power supply, used to supply a bias voltage of 5–10 V for the LMG5200EVM-02 boards.
- An additional Basetech BT-305 power supply, used to drive a cooling fan (5–12 V) for thermal management of the transformer core and load.
- A Rigol MSO5354 digital oscilloscope for analyzing system performance.
- Three Pico TA057 differential probes for voltage measurements at various points in the circuit.
- One pigtail probe for capturing high-frequency signals at the output of one of the LMG5200EVM-02 boards.
- A Fluke 177 True RMS digital multimeter, used to measure the current through the load (only after the rectifier stage).
- A Tenma 72-7780 digital multimeter to monitor the temperature of both the load and the transformer core.
- A laptop to power the Arduino Uno microcontroller and to record measurement data.

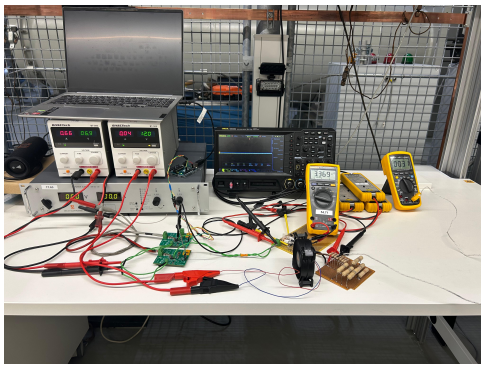


Figure 6.5: Used test setup for the GaN full-bridge module.

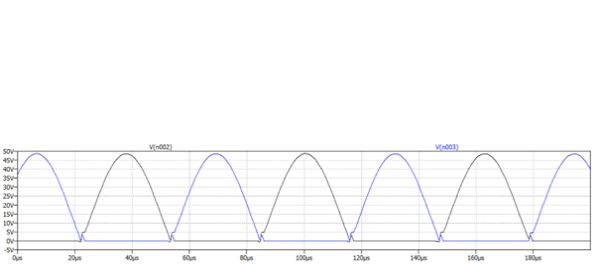
7

Results

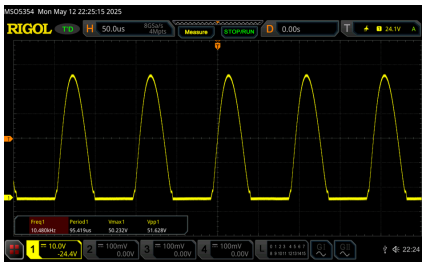
7.1. Topology 1: self oscillating circuit

7.1.1. Model - versus physical results

The accuracy of the LTSpice model was validated by comparing its simulated results with experimental measurements under the default configuration and open-load conditions. The LTSpice-generated waveform, presented in Figure 7.1a, exhibits an operating frequency of 15.8 kHz. Conversely, the corresponding physical measurement, conducted under identical conditions, is depicted in Figure 7.1b, demonstrating a frequency of 10.5 kHz.



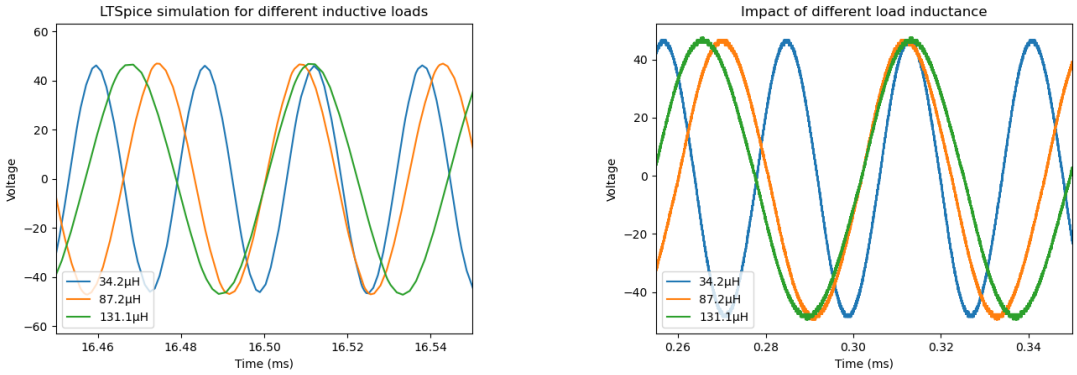
(a) LTSpice result



(b) Physical result

Figure 7.1: Open load in the self oscillating circuit.

Additional configurations were examined to analyze the discrepancies between the simulated model further and observed physical behavior. Specifically, multiple inductive load scenarios were evaluated, including 32.7 μH, 87.2 μH, and 131.1 μH. The corresponding results are presented in Figure 7.2. Both the simulation and experimental measurements exhibit similar frequency values of 36 kHz, 24 kHz, and 21 kHz, respectively. Furthermore, the peak voltage in the simulation plot is measured at 46 V, while the physical measurement shows a slightly higher value of 46.8 V. Overall, the comparison indicates strong alignment between the modeled and experimental results.



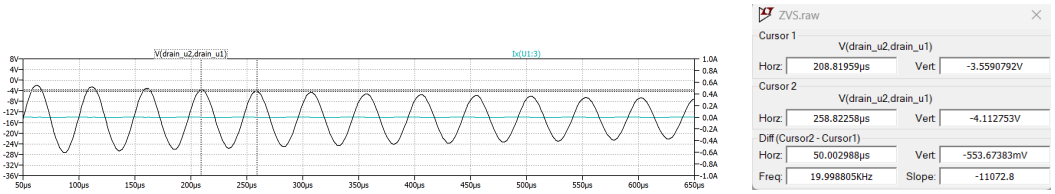
(a) LTSpice result **(b)** Physical result

Figure 7.2: Several inductive loads connected to the self oscillating circuit.

The deviation between the model and physical results mentioned above might have several causes. Moreover, the results shown also don't align with the analytical derived frequency.

A likely cause for this difference is the MOSFET parasitics, which are ignored in the analytical derivation. Moreover, the LTSpice model accounts for a part of the parasitic, but is likely incomplete. This explains why the simulated frequency is in between the analytical derived value and the measured value of the physical device.

One argument for this hypothesis stems from the LTSpice simulation (see Figure 7.3a). In the early transient, it can be seen that the frequency of oscillation is very close to what is expected from the analytical result. In this early transient the MOSFETs are not conducting, so the oscillations at the output stem only from the LC-tank. Right after one of the FETs reaches its threshold voltage and start conducting, the output frequency drops. This behaviour argues that the FETs parasitics are indeed not neglectable and most likely account for the difference in expected- and measured frequency.



(a) 20kHz sine-wave **(b)** Corresponding frequency

Figure 7.3: Output of the default SOC before MOSFETs are conducting.

The second argument for the hypothesis is that this deviating behaviour only occurs with open load. It is known that the load affects the oscillating frequency and if these values become large enough, they will likely dominate. The effect of the transistor's parasitics diminishes.

7.1.2. ZVS in the Self Oscillating Circuit

The LTSpice simulations show that for open load and default configuration of the SOC-board, it functions under ZVS conditions. The current in the channel starts flowing, when there is no voltage V_{DS} as can be seen in Figure 7.4:

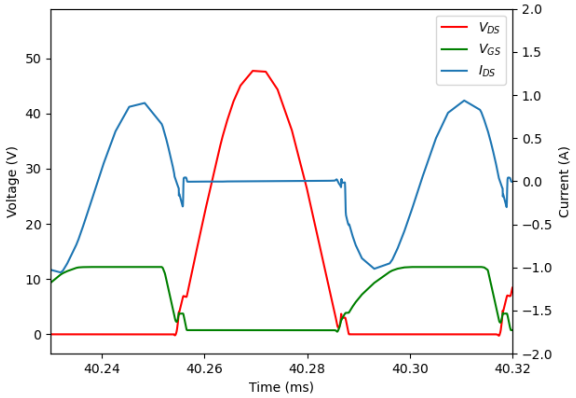
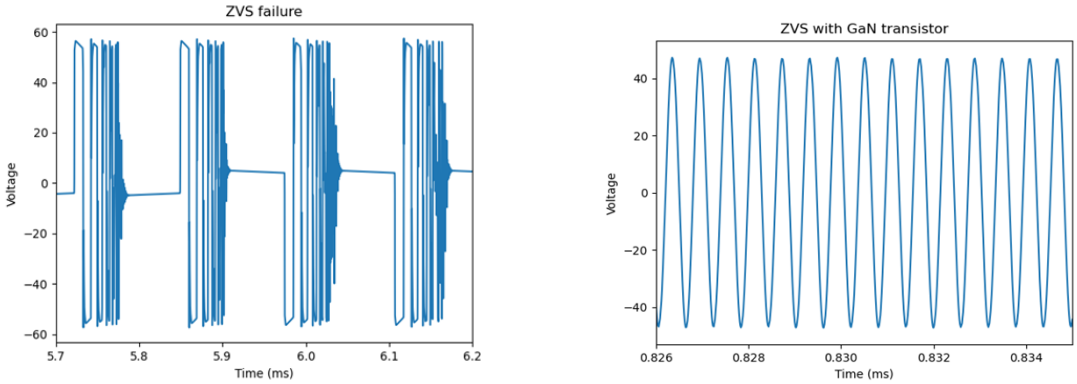


Figure 7.4: LTSpice result of ZVS in the Self Oscillating Circuit.

7.1.3. LTSpice GAN versus MOSFET

The MOSFETs in the self-oscillating circuit struggle to maintain performance at high switching frequencies, which becomes evident in the LTSpice simulation shown in Figure 7.5a. Replacing the MOSFETs with an arbitrarily selected GaN field-effect transistor (EPC2007 GaN FET) yields a remarkable improvement. The output voltage remains sinusoidal even at an increased frequency of approximately 1.25 MHz, as illustrated in Figure 7.5b. A detailed comparison of frequency measurements and FFT results for both simulations is provided in Appendix C.2.



(a) MOSFET result

(b) GaN FET result

Figure 7.5: LTSpice simulation comparing the output voltage.

This difference is likely due to superior characteristics of GaN regarding high frequency operation, such as high electron mobility and a smaller gate capacitance.

7.2. Topology 2: GaN full-bridge module

7.2.1. PWM control

Using the commands mentioned in subsection 5.3.2, the Arduino was configured to a frequency of 1.6 MHz and a duty cycle of 40%. These values were used for most tests regarding the half- and full-bridge systems. The output of the Arduino can be seen in Figure 7.6. When looking at this plot it can be seen that it has the desired frequency and duty cycle. Also interesting to note is the overshoot which can be seen at every change of state. Even though this overshoot is 20% of the total voltage, this is not the overshoot which can be seen at the output of the inverter. This can be explained by the fact that the PWM signal is first passed through the dead time generating circuit explained in subsection 5.1.3 and then fed to the gates of the GaN transistors, never coming in direct contact with the output.

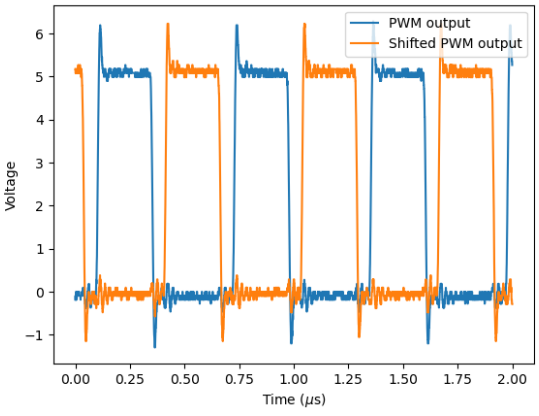


Figure 7.6: PWM signal generated by an Arduino UNO.

7.2.2. Simulation results

In subsection 6.4.2 the methodology for obtaining the LLC-tank values were elaborated. Several designs have been simulated, which have lead to the final design presented in this section. The simulated result will be compared to the results on the oscilloscope. The requirements specified in chapter 3 result in the following values for L_r and C_r, given a resonance frequency of 1.5 MHz:

Table 7.1: Table showing L_r and C_r for several values of Q.

Q	L_r	C_r
0.2	4.30e-07	2.62e-08
0.3	6.45e-07	1.75e-08
0.4	8.60e-07	1.31e-08
0.5	1.08e-06	1.05e-08
0.6	1.29e-06	8.73e-09
0.7	1.51e-06	7.48e-09
0.8	1.72e-06	6.54e-09
0.9	1.94e-06	5.82e-09

These values can be used to find the gain of the LLC-tank for all these different quality factors, plotted against the normalized resonance frequency.

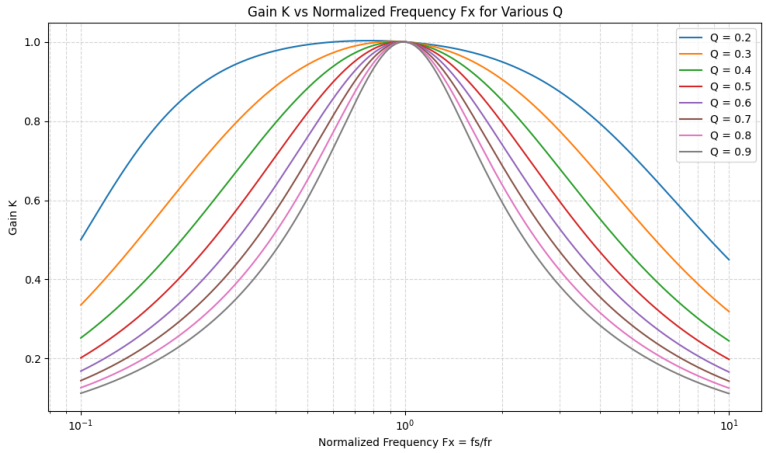


Figure 7.7: Gain-Frequency plots for several values of Q.

The combination of the quality factor range specified in subsection 6.4.1 and the transformer parasitics from the other group lead to a specific design. Their transformer has a leakage inductance of $1.18\mu H$, which leads to the specifications in Table 7.1 and the gain plot in Figure 7.8.

Table 7.2: Table showing the parameters of the LLC-tank.

Q	f_r MHz	$L_r/L_{leak}(H)$	$C_r(F)$	$R_{ac}(\Omega)$	Gain (K) at f_s
0.54	1.47	1.18e-6	10e-9	20.3	0.99

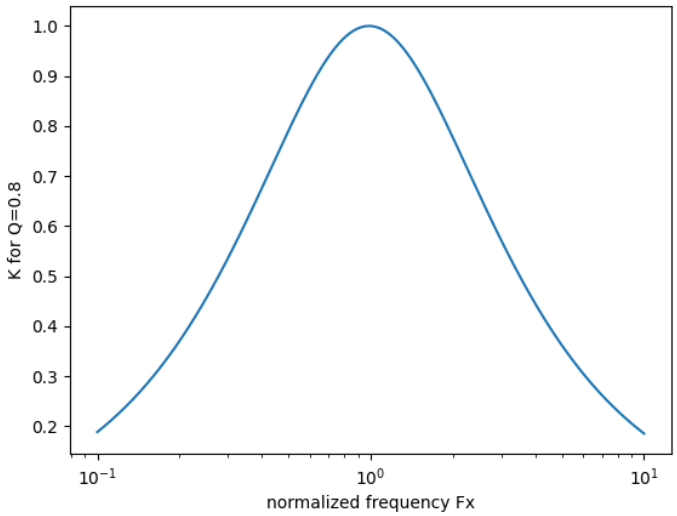


Figure 7.8: Gain-frequency plot of the LLC-design.

7.2.3. Physical results

Switching circuit

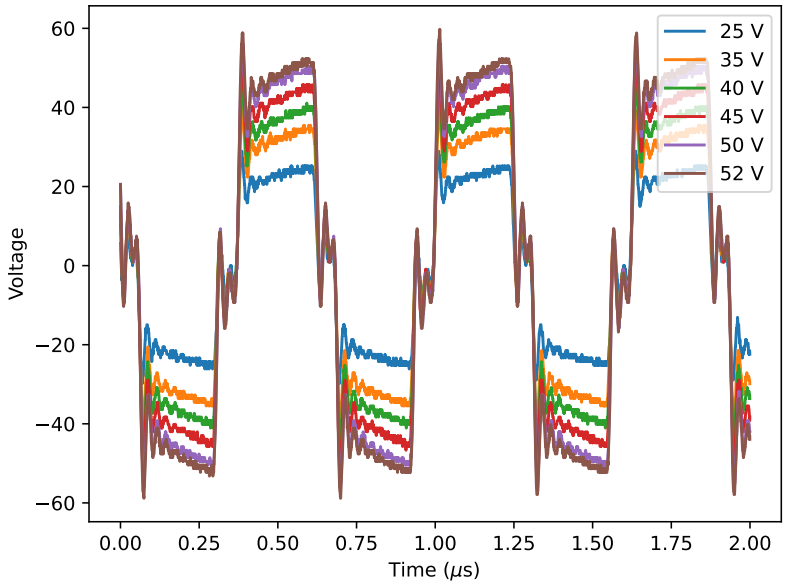


Figure 7.9: Output of H-bridge, which is connected to just the transformer and a 25 Ω resistive load, without C_{LLC} and the rectifier circuit from Figure 6.4.

The output of the implemented full-bridge converter is presented in Figure 7.9, demonstrating the successful attainment of a peak-to-peak voltage of 104 V. Additionally, the presence of adequate dead time is observable, though it may be slightly excessive. The residual ringing and overshoot will be mitigated through the LLC resonant tank, ensuring improved waveform stability and overall system efficiency.

LLC-resonance tank

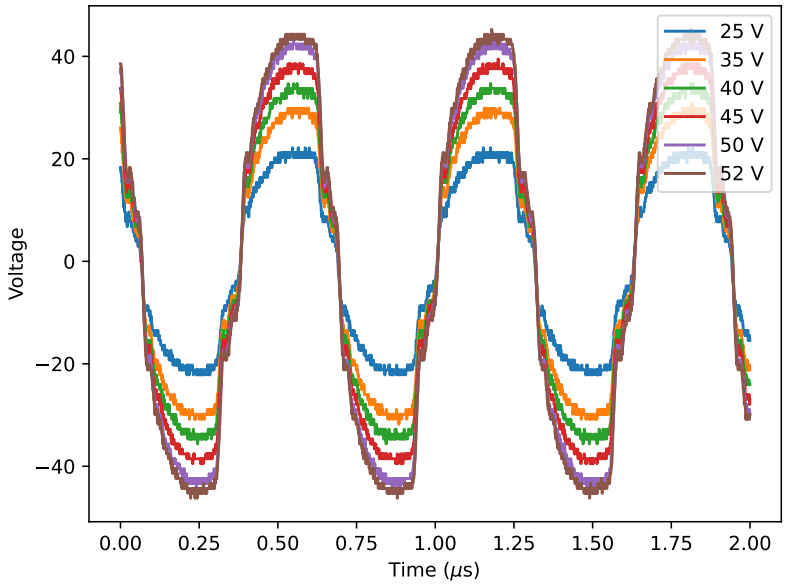


Figure 7.10: Output of transformer connected to the full-bridge and a 25 Ω resistive load, without the rectifier circuit from Figure 6.4.

The LLC resonant tank, comprising a capacitor and a transformer, plays a crucial role in shaping the output waveform. As illustrated in Figure 7.10, the initially distorted square wave observed in Figure 7.9 has been effectively smoothed. The removal of overshoot and ringing has resulted in the formation of a well-defined sinusoidal waveform. With a 52 V input supply, the generated sine wave achieves an output of 34 V_{rms}. However, this value is slightly lower than anticipated.

The efficiency measurements of the system obtained thus far are presented in **??**. Efficiency was determined based on the output V_{rms} and the resistive value of the load, as direct current measurements were not feasible due to the high-frequency nature of the waveform. The efficiency of the system was evaluated both with and without accounting for the bias power consumption. As only a negligible portion of the bias power is transferred to the output, including it in the efficiency calculation slightly distorts the representation of power losses within the main conversion path. Nevertheless, the bias power does constitute a component of the system's total energy consumption and therefore influences the overall system efficiency. However, both resulting efficiency values are unrealistically high, indicating that this calculation method may be inadequate for this particular case. This discrepancy is likely attributed to the inductive characteristics of the resistors, which makes the use of V^2/R to calculate power not correct and can thus not be used to find the efficiency.

Table 7.3: Efficiency Table.

Input				**Output**			**Efficiency**	
V_{in}	W_{Bias}	W_{Input}	W_{Total}	V_{rms}	Ω_{Load}	W	$\eta_{Without-W_{Bias}}$	$\eta_{With-W_{bias}}$
25	0.3	10.0	**10.3**	16.3	25.1	**10.6**	**106**	**102**
35	0.3	21.0	**21.3**	22.7	25.1	**20.6**	**98**	**97**
40	0.5	24.0	**24.5**	26.1	25.1	**27.0**	**113**	**110**
45	0.4	31.5	**31.9**	29.4	25.1	**34.4**	**109**	**108**
50	0.5	40.0	**40.5**	32.8	25.1	**42.8**	**107**	**106**
52	0.7	41.6	**42.3**	34.1	25.1	**46.2**	**111**	**109**

Rectifier

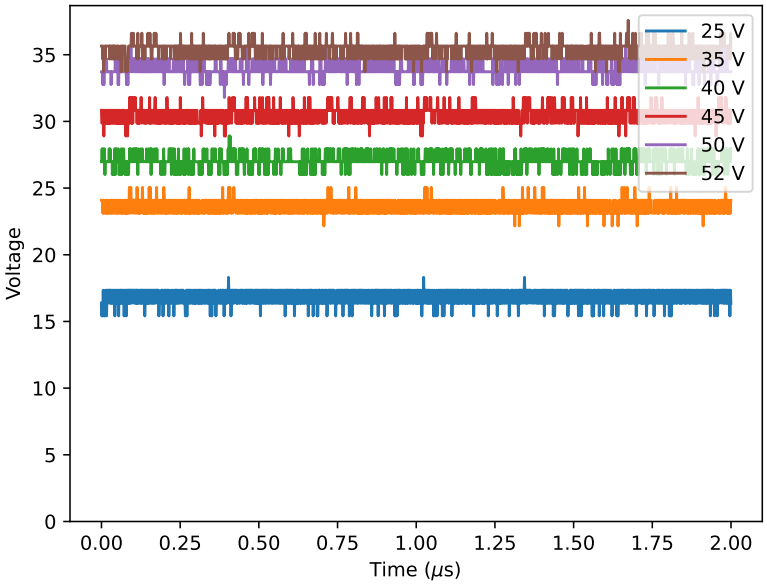


Figure 7.11: Output of the rectifier connected to the total system from Figure 6.4 and a load of 25 Ω.

The rectified output voltage is presented in Figure 7.11, demonstrating the successful conversion of the sinusoidal waveform into a smooth DC signal. The observed spikes are likely attributed to measurement timing inaccuracies. Under a 52 V input load condition, the measured output voltage was 35.5 V.

Again two corresponding efficiency values of the system up to this stage are depicted in Table 7.4. As the rectifier effectively eliminates the frequency component of the signal, the calculated efficiency values now exhibit improved accuracy when employing the same computational approach. An overall efficiency of 79% has been achieved, aligning with the intended target. However, the system has not successfully reached the 100 W power output objective.

Table 7.4: System efficiency up to the output of the rectifier.

Input				**Output**			**Efficiency**	
V_{in}	W_{Bias}	W_{Input}	W_{Total}	V_{rms}	Ω_{Load}	W	$\eta_{Without-W_{Bias}}$	$\eta_{With-W_{bias}}$
25	0.4	15.0	**15.4**	16.8	25.1	**11.2**	**75**	73
35	0.5	28.0	**28.5**	23.6	25.1	**22.2**	**80**	78
40	0.5	36.0	**36.5**	27.1	25.1	**29.2**	**81**	80
45	0.6	45.0	**45.6**	30.6	25.1	**37.2**	**83**	82
50	0.7	55.0	**55.7**	33.9	25.1	**45.8**	**83**	82
52	0.7	62.4	**63.1**	35.5	25.1	**50.1**	**80**	79

7.2.4. Comparing the results

The experimental results deviate from the simulated predictions, with a notably lower gain than anticipated. Consequently, the target output voltage has not yet been achieved, preventing the expected current draw from the calculated load. This discrepancy suggests that further investigation is required to identify potential factors influencing the observed performance and to refine the model accordingly.

7.2.5. Spectrum Analysis

In this paragraph the spectrum of the system will be analysed at different sections of the circuit. First the Fast Fourier Transform (FFT) will be done on the output of the H-bridge, then on the LLC-tank output

and lastly the output of the rectifier will be verified.

FFT: H-Bridge and LLC-tank

In Figure 7.12 it can be seen that the signal contains most of its power around the switching frequency. Moreover, the odd harmonics appear in the graph and the even harmonics are not present as is expected. The output of the LLC-tank has a slightly lower peak at the fundamental than the H-bridge, but the higher harmonics are also more damped. This results in a more sine-wave shaped signal, verifying a good LLC-design.

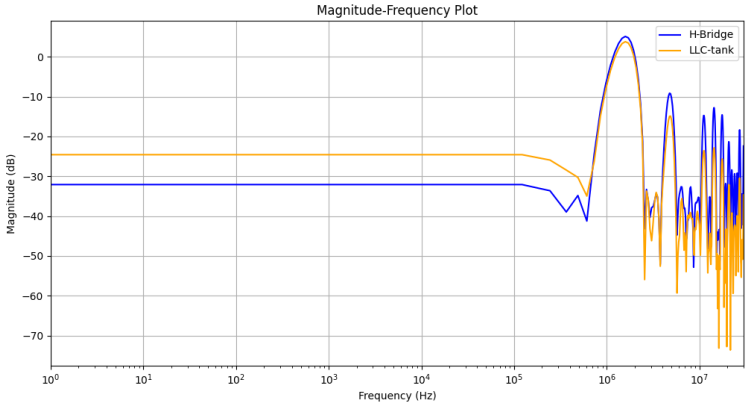


Figure 7.12: Output of the rectifier connected to the system and a load of 25 Ω.

FFT: Rectifier

Initially, the FFT was calculated to verify the output of the rectifier, which in theory should be DC (0 Hz). In Figure 7.13, it can be seen that the majority of the spectral power of the rectifier is contained around 0 Hz. This becomes even more evident when comparing the output of the rectifier to the output of the H-Bridge. Nevertheless, during measurements, unexpected results were found. The wounded-wire resister seemed to have a larger impedance, which could be explained by inductive behaviour of the wounded-wire resistor at higher frequencies. However, the FFT in Figure 7.13 weakens this explanation.

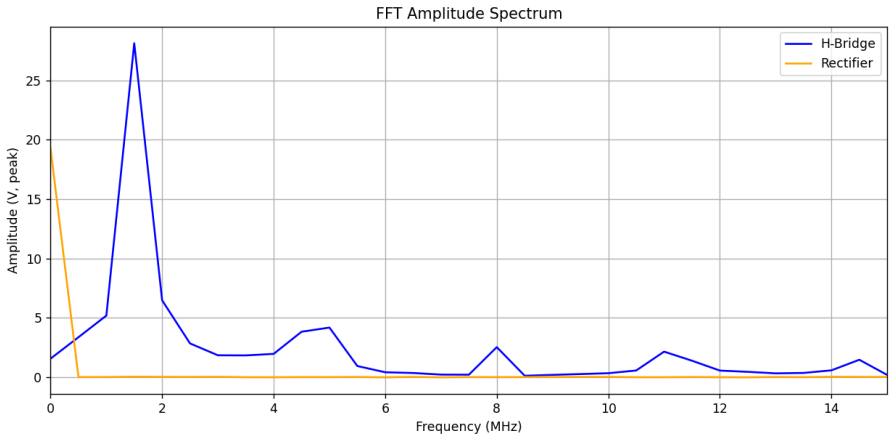


Figure 7.13: FFT comparison of the rectifier output with the output of the H-bridge.

8

Discussion and Conclusion

8.1. Conclusion

This project aims to demonstrate the benefits and reproducibility of high-frequency power conversion. The self-oscillating circuit shows potential at first, due to its simplicity. This simplicity allowed for an LTSpice model to simulate quite accurately the behaviour of the circuit. Although the self-oscillating circuit itself has not reached over a megahertz in frequency, the model has shown that it is likely possible if the silicon transistors are replaced by their GaN substitutes. Unfortunately the self-oscillating circuit is load dependent, so it does not meet the requirements specified.

The GaN full-bridge module is a more sophisticated design. This research has shown that it is possible to integrate two half-bridge modules into one full-bridge module, operating at frequencies above megahertz. However, it has the intrinsic disadvantage that it is less efficient due to the its inert hard-switching behaviour. Therefore an LLC-resonant circuit is successfully integrated between the module's output and the transformer. Finally the output after the transformer was rectified and DC-DC conversion at megahertz frequency was successfully achieved.

The GaN full-bridge module has shown to not only be able of operating at megahertz frequency, it also did so with efficiencies above 90% without rectification and around 80% measured after the rectifier. It has met all of the requirements, with exception of the minimum voltage and the minimum delivered power. However, the power supply utilized in this project did not allow for higher input voltages, so it could not be tested. The module is likely able to deliver these higher output voltages when supplied by a sufficient power supply, but this should be confirmed in further research. The delivered power requirement can in further research be satisfied by using a heavier load (lower impedance), so more current is drawn and thus, a higher delivered wattage can be reached without the need of increasing the voltage.

8.2. Discussion

This project set out to design and implement a high-frequency DC–DC converter, targeting compactness, high efficiency, and MHz-range operation. Unfortunately, due to time constraints not everything is done and a couple of improvements can be made. First of all: The self oscillating circuit should be physically researched after the silicon transistors are substituted by GaN transistors. Moreover, the GaN full-bridge module should be tested with a power supply that allows for higher input voltage. Also its dead time and duty cycle should be investigated further to achieve the required 100 W output power. In addition more attention towards thermal management would be useful, since this also helps understanding the efficiency and losses better. Finally, smaller adjacent components should be used in the future, otherwise the size reduction in transformer might get compensated by the adjacent components.

Throughout the course of the project, a deeper understanding of the complexities in high-frequency power electronics was obtained among all members. Skills regarding the design of dead-time circuits and shoot-through mitigation, but also the programming of microcontrollers for high frequency pulses were learned. This hands-on experienced has lead to a lot of theoretical- and practical insight.

Additionally, the team demonstrated strong collaboration. A fair distribution of tasks was made and communication within the team was effective and contributed positively most of the time. This allowed the project to progress steadily and reduced bottlenecks when unforeseen challenges arose.

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A

Python Code

The self-written python scripts used for designing the LLC resonance tank are shown in this Appendix

The code below shows a python script for calculating the LLC values, also for multiple scenario's.

```
import numpy as np
import matplotlib.pyplot as plt

#Dit script is om de Lr en Cr (leakage/resonant inductance) en resonant capacitance  te berekenen

#(maximum) load values underneath
Vo=50
Po=100
Ro=5
n=1     #transformer turn ratio

Q=np.arange(0.2,1,0.1)
fr=1.5e6                #resonance frequency, dus minimale switching frequency!
print("fr ",fr)
Rac=(8/((np.pi)**2))*n*(Vo**2/Po)                    #reflected load

# print("Rac", Rac)

Cr =  np.sqrt(1/(((2*np.pi*fr)**2)*((Q*Rac)**2)))
Lr = ((Q*Rac)**2)*Cr                                 #Quality factor
fr = 1/(2*np.pi*np.sqrt(Lr*Cr))


##################
#prints
print("Lr, Cr = ", Lr,Cr)
print("fr = ", fr)

####################
#plots
fig, (ax1, ax2) = plt.subplots(1, 2)
fig.suptitle('Lr and Cr against Q')
ax1.plot(Q, Lr)
ax1.set_title('Lr against Q')
ax2.plot(Q, Cr, 'tab:orange')
ax2.set_title('Cr against Q')
plt.show()
```

The code below shows a gain versus normalized frequency plot for validating the designed system, it also calculates and prints several values like the Q-factor.

```
import numpy as np
import matplotlib.pyplot as plt

######################
#Dit script is voor één specifieke plot en om de Q factor enzo te vinden.
######################

#LLC values
Lm=152e-6  #magnetizing inductance
Lr=(1.18e-6)  #leakage/resonance inductance
Cr=10e-9    #resonance capacitance

#############
#Hier moet je ff de switching frequency invullen, dus van de arduino basically
# fs=2e6

fs=1.6e6
fr=1/(2*np.pi*np.sqrt(Lr*Cr))
n=1

#Maximum load values
#####
Vo=50
Po=100
Ro=25

#Een van de twee hieronder moet gecomment zijn
# Rac=(8/((np.pi)**2))*n*(Vo**2/Po)     # Requirement van Mohammad
Rac=(8/((np.pi)**2))*n*(Ro)             # Om verschillende loads te testen

#################
#Q factor and m function
Q=(np.sqrt(Lr/Cr))/Rac                  #Quality factor
Fx=fs/fr                                #normalized frequency
m=(Lr+Lm)/Lr                            #ratio of total priary to resonant, grotere m =
    plattere curve = minder gain

##########
#K formula
numerator=((Fx**2)*(m-1))
denomenator=(np.sqrt((m*(Fx**2)-1)**2+Fx**2*(Fx**2-1)**2*(m-1)**2*Q**2))
K=numerator/denomenator

print("K=",K)

fs=np.arange(0.1*fr,10*fr,10)
Fx=fs/fr

numerator=((Fx**2)*(m-1))
denomenator=(np.sqrt((m*(Fx**2)-1)**2+Fx**2*(Fx**2-1)**2*(m-1)**2*Q**2))
K=numerator/denomenator

############
#prints
print("Resonance frequency = ",fr)
print("Rac = ", Rac)
print("m = ",m)
print("Q = ",Q)
print("Higher Q means peak closer to resonance \n")
print("Higher Q means smaller peak")
# print("numerator", numerator, "and denomenator", denomenator)
# print(Fx)
# print("K=",K)

############
#plot
plt.plot(Fx,K)
plt.xscale('log')
```

```
68 plt.title(label= "Gain␣K␣against␣Normalized␣Frequency")
69 plt.xlabel("normalized␣frequency␣Fx")
70 plt.ylabel("K␣for␣Q=0.8")
71 plt.show()
```

The result of the earlier mentioned LLC value calculation script, provides multiple L_r and C_r values for a single resonance frequency. This script plots the gain of all of them against the normalized frequency including their Q-factor for a specific load value.

```
import numpy as np
import matplotlib.pyplot as plt

######################
#LLC values
Lm=150.e-6  #magnetizing inductance
# Lr=0.93e-6  #leakage/resonance inductance
# Cr=100e-9    #resonance capacitance

########################
#800Khz
# Lr =  [1.58451512e-05, 2.37677268e-05, 3.16903024e-05, 3.96128780e-05,
#  4.75354536e-05, 5.54580292e-05, 6.33806048e-05, 7.13031804e-05]
# Cr = [1.56943658e-08, 1.04629105e-08, 7.84718289e-09, 6.27774631e-09,
#  5.23145526e-09, 4.48410451e-09, 3.92359144e-09, 3.48763684e-09]


########################
# 1Meg, 150V=Vo
# Lr = [5.05704060e-06, 7.58556090e-06, 1.01140812e-05, 1.26426015e-05,
#  1.51711218e-05, 1.76996421e-05, 2.02281624e-05, 2.27566827e-05]

# Cr = [5.00891686e-09, 3.33927791e-09, 2.50445843e-09, 2.00356674e-09,
#  1.66963895e-09, 1.43111910e-09, 1.25222921e-09, 1.11309264e-09]

#vo=50V
# Lr = [6.45030689e-07, 9.67546033e-07, 1.29006138e-06, 1.61257672e-06,
#  1.93509207e-06, 2.25760741e-06, 2.58012275e-06, 2.90263810e-06]

# Cr = [3.92699082e-08, 2.61799388e-08, 1.96349541e-08, 1.57079633e-08,
#  1.30899694e-08, 1.12199738e-08, 9.81747704e-09, 8.72664626e-09]




#Vul hier de waardes in die je uit de value calculation script krijgt
##############
#Bewaar deze aub, dit is de huidige haha
#1.5 Meg 50V=Vo
Lr= [4.30020459e-07, 6.45030689e-07, 8.60040918e-07, 1.07505115e-06,
 1.29006138e-06, 1.50507161e-06, 1.72008184e-06, 1.93509207e-06]

Cr= [2.61799388e-08, 1.74532925e-08, 1.30899694e-08, 1.04719755e-08,
 8.72664626e-09, 7.47998251e-09, 6.54498469e-09, 5.81776417e-09]
################

#frequency formulas
# fs=2e6

fs=1.5e6
Vo=50
Po=100
Ro=5
n=1
Q_list=[]


for i in range(len(Lr)):
    fr=1/(2*np.pi*np.sqrt(Lr[i]*Cr[i]))
    fs=np.arange(0.1*fr,10*fr,10)
    #Maximum load values
    #####

    # Rac=(8/((np.pi)**2))*n*(Vo**2/Po)     #reflected load
    Rac=(8/((np.pi)**2))*n*(Ro)             #reflected load

    ##################
```

```
    #Q factor and m function
    Q=(np.sqrt(Lr[i]/Cr[i]))/Rac                    #Quality factor
    Fx=fs/fr                                #normalized frequency
    m=(Lr[i]+Lm)/Lr[i]                          #ratio of total priary to resonant

    ##########
    #K formula
    numerator=((Fx**2)*(m-1))
    denomenator=(np.sqrt((m*(Fx**2)-1)**2+Fx**2*(Fx**2-1)**2*(m-1)**2*Q**2))
    K=numerator/denomenator

    Q_list.append(Q)
    # print("K=",K)
    # print("Q = ", Q)

# print("Q_list = ",Q_list)

plt.figure(figsize=(10, 6))
for Q in Q_list:
    numerator = (Fx**2) * (m - 1)
    denominator = np.sqrt((m * Fx**2 - 1)**2 + Fx**2 * (Fx**2 - 1)**2 * (m - 1)**2 * Q**2)
    K = numerator / denominator
    plt.plot(Fx, K, label=f"Q = {Q:.1f}")

# Plot formatting
plt.xscale('log')
plt.xlabel("Normalized Frequency Fx = fs/fr")
plt.ylabel("Gain K")
plt.title("Gain K vs Normalized Frequency Fx for Various Q")
plt.grid(True, which='both', linestyle='--', alpha=0.5)
plt.legend()
plt.tight_layout()
plt.show()
```

Code to create plots of oscilloscope data (or any data in csv format). And calculate frequencies in different manors depending on what is needed.

```
import pandas as pd
import matplotlib.pyplot as plt
import numpy as np
from scipy.signal import find_peaks

# Load the CSV file into a DataFrame
dataHigh = pd.read_csv("131-1.csv")
dataNoLoad = pd.read_csv("noLoad15V0.csv")

# plt.plot(data["time"], data["V"])
# data["CH1"] = data["CH1"] * 20  # Convert CH1 to 20x attenuation


dataHigh["time"] = dataHigh["time"] * 1000  # Convert time to milliseconds
dataNoLoad["Time"] = dataNoLoad["Time"] * 1000  # Convert time to milliseconds

# plot data
plt.plot(dataHigh["time"], dataHigh["V"])
plt.plot(dataNoLoad["Time"], dataNoLoad["CH1"])


# Function to calculate frequency using peaks
def calculate_frequency_from_peaks(time, signal):
    peaks, _ = find_peaks(signal)
    peak_times = time.iloc[peaks]
    time_differences = np.diff(peak_times)
    average_period = np.mean(time_differences)
    frequency = 1 / average_period
    print("frequency", frequency)
    return frequency


# Function to calculate frequency using zero crossings (only for sinusoidal signals around
    zero)
```

```
def calculate_frequency_from_zeros(time, signal):
    mid_point = abs(max(signal)) - abs(min(signal))
    print("mid points", mid_point)
    i = int(len(signal) / 2 + 1)
    while i > len(signal) / 2 and i < len(signal) - 1:
        print(i)
        if signal[i] * signal[i + 1] <= 0:
            print(signal[i], signal[i + 1])
            zero_crossing1 = (time.iloc[i] + time.iloc[i + 1]) / 2
            x = signal[i:]
            peaks, _ = find_peaks(x, width=1000)
            print(zero_crossing1)
            while i < len(signal) - 1:
                if signal[i] >= 10 or signal[i] <= -10:
                    while i < len(signal) - 1:
                        if signal[i] * signal[i + 1] <= 0:
                            zero_crossing2 = (time.iloc[i] + time.iloc[i + 1]) / 2
                            print("zero crossings", zero_crossing1, zero_crossing2)
                            time_difference = zero_crossing2 - zero_crossing1
                            print("time difference", time_difference)
                            frequency = 1 / (2 * time_difference)
                            print("frequency", frequency)
                            plt.plot(zero_crossing1, 0, "x")
                            plt.plot(zero_crossing2, 0, "x")
                            break
                        i += 1
                    break
                i += 1
            break
        i += 1

    return


# Function to calculate frequency using midpoints
def calculate_frequency_from_midpoints(time, signal):

    mid_point = abs(max(signal)) - abs(min(signal))
    print("mid points", mid_point)
    i = int(len(signal) / 2 + 1)
    while i < len(signal) - 1:
        if (
            (signal[i] < mid_point and signal[i + 1] > mid_point)
            or (signal[i] > mid_point and signal[i + 1] < mid_point)
            or signal[i] == mid_point
        ):
            zero_crossing1 = (time.iloc[i] + time.iloc[i + 1]) / 2

            while i < len(signal) - 1:
                if signal[i] >= 10 or signal[i] <= -10:
                    while i < len(signal) - 1:
                        if (
                            (signal[i] < mid_point and signal[i + 1] > mid_point)
                            or (signal[i] > mid_point and signal[i + 1] < mid_point)
                            or signal[i] == mid_point
                        ):
                            print(signal[i], signal[i + 1])
                            zero_crossing2 = (time.iloc[i] + time.iloc[i + 1]) / 2
                            time_difference = zero_crossing2 - zero_crossing1
                            print("time difference", time_difference)
                            frequency = 1 / (2 * time_difference)
                            print("frequency", frequency)

                            # plt.plot(
                            #     zero_crossing2, (signal[i] + signal[i + 1]) / 2, "x"
                            # )
                            break
                        i += 1
                    break
                i += 1
            break
```

```
        i += 1

    return


calculate_frequency_from_midpoints(dataHigh["time"], dataHigh["V"])
calculate_frequency_from_peaks(dataNoLoad["Time"], dataNoLoad["CH1"])

# Add labels, title, and legend
# plt.xlim(0.0049 * 1000, 0.0057 * 1000)
# plt.ylim(
#     0,
# )
plt.xlabel("Time (ms)")
plt.ylabel("Voltage")
plt.title("Title")
plt.legend()

# Show the plot
plt.show()
```

Code for just creating plots. No more, no less.

```
import pandas as pd
import matplotlib.pyplot as plt
import numpy as np

# Load the CSV file into a DataFrame
data = pd.read_csv("data0.csv")
data_2 = pd.read_csv("data0.csv")
# data_3 = pd.read_csv("ZVS_151_6u.csv")

data["Time"] = data["Time"] * 1000000
data_2["Time"] = data_2["Time"] * 1000000
# data_3["Time"] = data_3["Time"] * 1000

plt.plot(data["Time"], data["CH2"])
plt.plot(data_2["Time"], data_2["CH3"])
# plt.plot(data_3["Time"], data_3["V"], label="131.1µH")


# Add labels, title, and legend
# plt.xlim(5.7, 6)
plt.xlabel("Time (us)")
plt.ylabel("Voltage")
plt.title("ZVS Full bridge GaN driver attempt 10 ohm")
# plt.legend()

# Show the plot
plt.show()
```

Code to convert .txt files to .csv files. For example useful when wanting to create python plots, or do calculations on data coming from LTSpice.

```
import pandas as pd
import matplotlib.pyplot as plt
import numpy as np

# Load text file
input_file = "ZVS4.txt"
output_file = "ZVS4.csv"

# Read the tab-separated data (assumes first row contains headers)
data = pd.read_csv(input_file, sep="\t")

# Write to CSV
data.to_csv(output_file, index=False)

print(f"File converted and saved as '{output_file}'")
```

This code is used to generate two PWM signals 180 degrees out of phase with each other using an Arduino Uno/

```
 int i=10;
void setup() {
  DDRD = B00111000; // Set pins 3 (PD3) and 4 (PD4) as outputs
  noInterrupts();
}

void loop() {
  while (i >0) {
  PORTD = B00000000;
  PORTD = B00010000;


__asm__("nop");
__asm__("nop");
__asm__("nop");
 PORTD = B00000000;
 PORTD = B00001000;


__asm__("nop");

}
}

//__asm__("nop");
//__asm__("nop\n\t");
```

B

Calculations by hand

B.0.1. Calculation for LLC tank

In 3 the required output voltage is stated as 50 V and the maximum power as 100 W. Equation 6.2 leads approximately to $R_{ac} = 20.3\ \Omega$ if the winding ratio is 1.

For the quality factor we want to be in a range between 0.5 and 1. Since lower results in a higher ZVS range, but higher means more efficiency and higher load robustness. Substituting this in the equation for the Q-factor 6.1 results in approximately $65.9 = \frac{L_r}{C_r}$ for Q=0.4 and for Q=0.8 this is 264
Preferable the system has both ZVS and working frequencies above 1 MHz. The system will operate at ZVS if the LLC-tank behaves inductive, which means switching frequencies above the resonance frequency. Therefore the resonance frequency f_r is chosen as 1 MHz. Equation 6.4 results in $L_r C_r = 2.54 \cdot 10^{-14}$

Substituting $\frac{L_r}{C_r} = 65.9$ into $L_r C_r = 2.54 \cdot 10^{-14}$ results in $C_r = \sqrt{\frac{2.53 \cdot 10^{-14}}{65.9}} = 19.6nF$ for Q=0.4 and $C_r = \sqrt{\frac{2.53 \cdot 10^{-14}}{264}} = 9.79nF$. And $L_r = 1.29\mu H$ and $L_r = 2.58\mu H$

C

LTSpice

C.1. SOC

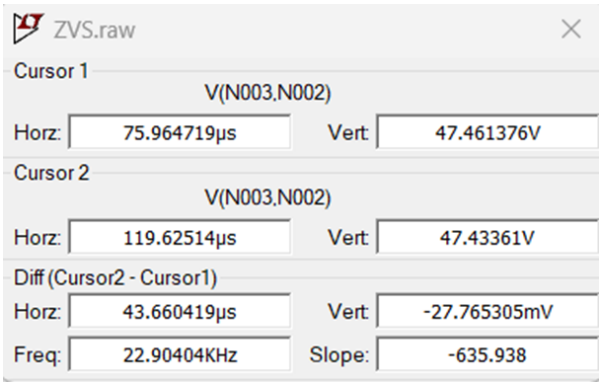


Figure C.1: Frequency of SOC for 151.6 micro Henry load

C.2. MOSFET versus GaN FET

The frequency between two sequential peaks is measured and results in the frequency of 1.26 MHz as can be seen in the figure below.

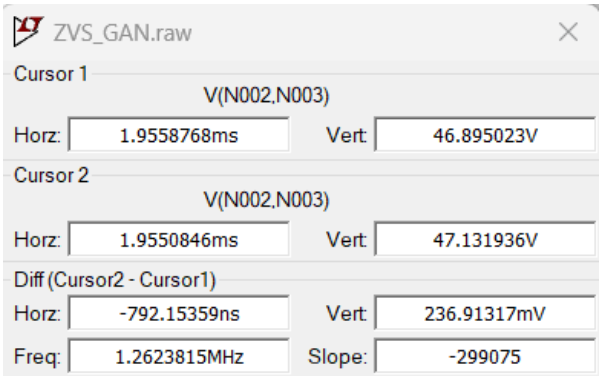
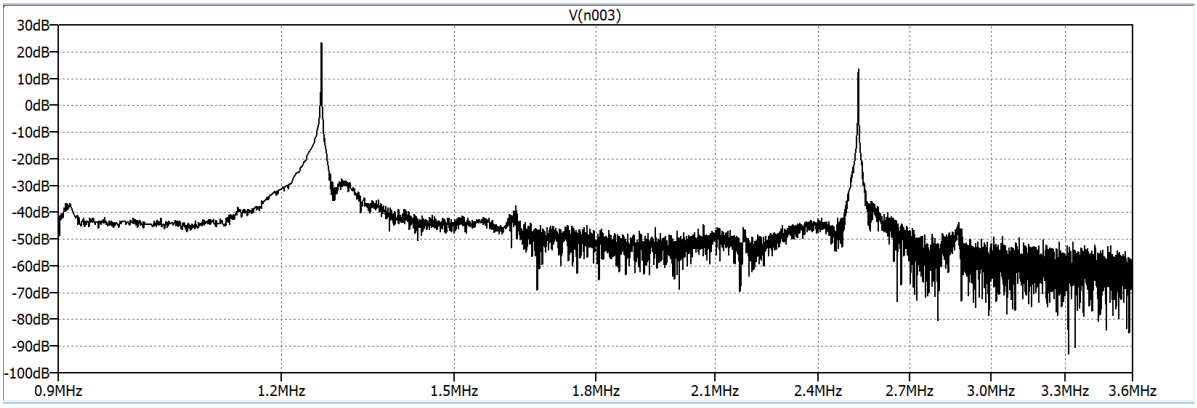
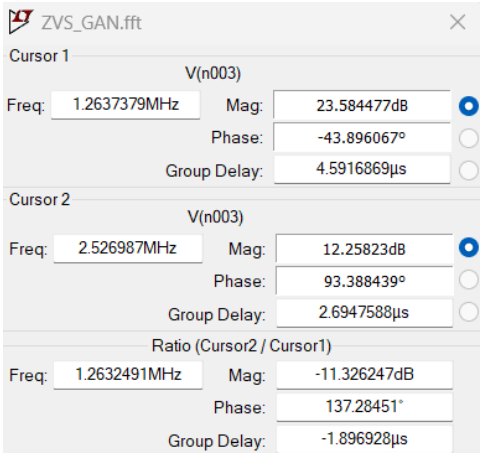


Figure C.2: The frequency of the circuit with GaN transistors



(a) FFT of the output voltage simulated with GaN FETs



(b) Fundamental and second harmonic Frequency

Figure C.3: GaN FFT