Bachelor Graduation Project Thesis

Switched-Device Power Amplifier using Bias Control

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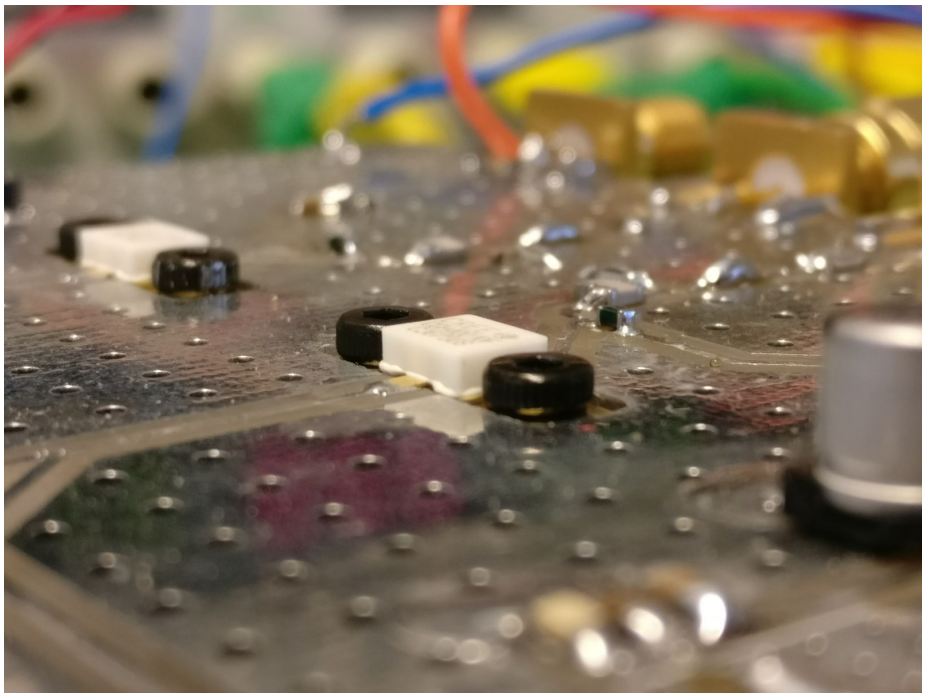

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Challenge the future

Abstract

In this work, a switched-device power amplifier using bias control is designed and realized. The PA operates at a frequency of $100\,\mathrm{MHz}$. Test results show that the PA achieves a PAE of $63\,\%$ at $-6\,\mathrm{dB}$ power back-off and $60\,\%$ at the peak output power of $40\,\mathrm{dBm}$.

First, an overview of the state-of-the-art PA technology and performance in high PAPR applications is given. The state-of-the-art analysis is then used to set up the requirements of the PA and to compare the results to in the end. The design of the PA is explained in detail, followed by an evaluation of the simulated and measured results. Notable observations of the performance measurements are also discussed. After the concluding remarks regarding this work are given, recommendations on how to improve the performance and to extend the concept of the proposed switched-device PA are presented.

Contents

1

Introduction

Over the last decades, the demand for increased wireless networking capacity is steadily rising. Worldwide, mobile data traffic increased from 7 EB to 11 EB (exa bytes) per month and is predicted to increase to 49 EB in 2021 [1]. Current 4G networks, digital radio and television transmission and other applications employ OFDM and/or QAM modulation/transmission techniques resulting in a high peak to average power ratio (PAPR) [2]. Similar modulation schemes are also considered for future 5G networks [3]. The choice for high PAPR transmission methods leads to operation of power amplifiers (PA's) at lower efficiency, as conventional (simple class A, AB, B) PA designs operate worse at back-off than at peak power due to the presence of bias currents. This chapter will explain some state-of-the-art PA designs that alleviate this inherent handicap.
The combination of current, mediocre efficient, complex PA's and the expected large increase of wireless data transport founds the obligation to design more efficient PA's, in order to reduce the relative power consumption.
The goal of this Bachelor graduation project is to conduct a proof-of-concept for a new, relatively simple PA topology promising 70 % drain efficiency which also enables operation in high PAPR applications. This concept could fill in a gap in the demanding efficiency problem that current RF PA technologies experience.

1.1 Thesis Outline

This thesis will describe the design process of the proposed PA, realization of the design and simulation and test results. In this chapter, the problem and its boundaries will be described. Also a brief investigation of the state-of-the-art will be given to complement the problem context given in the previous section, to define reasonable performance requirements of the proposed PA and to place the realized PA performance in perspective after testing.
In the next chapter, an overview of the requirements of the PA will be given. This chapter explains how the PA must function and gives quantitative design constraints

and specifications.
In chapter 3 an in-depth explanation of the functionality and design problems of the PA will be provided. The chapter will discuss for each design problem the methodology used to solve the problem and will also give the designed solutions.
In chapter 4, the simulation results will be presented, as well as the process of realizing the prototype and its test results.
Finally, chapter 5 will discuss the achieved results and will point out the differences between the test results and the performance predicted in the simulations.
In the last two chapters, a conclusion for this project and recommendations for improving the PA and ideas future projects will be given.

1.2 Project Overview

The objective of the entire project is to perform a proof-of-concept of a new PA topology that switches the operation from one transistor to another to realize increased efficiency at power back-off. The transistors have different supply voltages, this makes one device more efficient at back-off (lower supply voltage), while the other is more efficient at peak power.
The full project is split into three smaller projects, for three teams, each team with two persons each. One team is responsible for the design of a system that drives the designed PA's and is able to perform the required measurements. The other two teams each design a slightly different implementation of the proposed switched-device PA The implementations differ in the mode of operation: in the first implementation, the mode of the PA is switched by controlling the input signals to the two different branches in the PA. In the other implementation, the mode of operation is switched by controlling the gate bias of the transistors in the different branches. The exact functionality of the switching and the use of different branches will be explained in the following sections and chapters. This thesis concerns the design of the of the PA that uses control of the gate bias.

1.3 Problem Scope

As stated before, the goal of this project is to perform a proof-of-concept of a new PA topology promising $70\,\%$ efficiency at peak power operation. The efficiency at power back-off is also enhanced. This is achieved by the combination of two PA's whose modes of operation are controlled. Until power back-off, the main PA is active and the peak PA is in cut-off, while it is the other way around from power back-off until peak power. The optimal power level at which the modes change is determined by the power probability density function of the signal envelope. The switching is implemented by modifying the gate bias of the transistors such that a device is either in cutoff or active. Throughout this thesis, the term 'switched device' is used to indicate the bias controlled operation.
The most dominant design challenges of the switched device implementation are qualitatively summarized below:

- Choosing gate and drain (supply) bias voltage values conform with linearity specifications and that optimizes drain efficiency
- Adequate (de)coupling of supplies and the signal path
- Guaranteeing stability of the amplifier
- PCB design

A more quantitative description of the challenges will be given in chapter 2.
(Digital) predistortion to compensate for non-linearity and harmonic distortion falls outside the scope of this project, as it was considered too time-consuming. Therefore it would have left little time to optimize for the primary goals.
Furthermore, examining the dynamic distortion of the device (e.g. intermodulation distortion, distortion due to switching) was considered a secondary goal and optimizing for possible consequences from these effects was regarded out of the scope of the project.

1.4 State-of-the-Art Analysis

Several technologies exist to enhance the efficiency of PA's used in high PAPR applications. These include newly developed technologies such as envelope tracking (ET), but also a technique like the Doherty amplifier [4] that has been used for a long time and proves to be very effective for modern transmission applications.
This section gives an overview of the state-of-the-art techniques for more efficient high PAPR transmission. First, class G PA's will be discussed due to their similarity to the switched device PA operation. Second, the Doherty PA's will be examined because of their similar efficiency characteristic [5]. Third, the performance of ET PA's will be briefly evaluated, because this principle is the 'continuous-mode' version of the previously mentioned class G PA. The technique of outphasing will be discussed to conclude the state-of-the-art analysis regarding high PAPR amplification techniques. Finally, the main features of GaN HEMT devices will be summarized.

1.4.1 Class G PA

The principle behind class G PA's is very similar to that of the switched-device PA. A simple class G PA has a two transistors of which their supplies are switched on/off, while the simple switched-device PA has two transistors of which the input (either the bias or the signal) is controlled to switch the device on/off.
Current class G PA's can achieve PAE's over $50\,\%$ [6], but more often have maximum PAE's between $40\,\%$ and $50\,\%$ [7], [8].
Class G are known to suffer from linearity and distortion problems associated with the switching [6]. Therefore, many class G PA's rely on DPD to enhance the linearity of the PA. However, the distortion caused by the transients from the switches is hard to compensate for. Also, energy losses are associated with the switching technique performed by class G PA's [9]. This becomes especially problematic for applications in future wireless networks that require large bandwidths and thus a high frequency of

supply switching.
Because the switched-device PA will control the switching from the input, it is less complex to compensate for switching distortion or to switch using a profile that minimizes distortion. This is possible because a high degree of control is available for input signals. The complexity for class G PA's to compensate for switching distortion lies in the fact that the switching is performed using a special part of the PA, that is separately controlled.

1.4.2 Doherty PA

Because the Doherty efficiency-output power characteristic closely resembles that of the switched-device simulations and the fact that this technique will probably extensively be used in future (5G) applications [10], this technique is overviewed. Also, due to its similarity, the performance of this technique is compared with the realized switched-device technique in chapter 4.
Table 1.1 gives a summary of the current state-of-the-art in Doherty PA's. The performance of Doherty PA's is strongly dependent on the matching networks needed to enable load modulation between the peak and main amplifier sections. When fabricated on-chip, the quarter-wavelength transmission lines (TL's) needed for this matching can lead to significant losses [10]. Another noticeable fact Table 1.1 shows is the difference between the efficiencies of the lower frequency PA's. Using other impedance transformers for matching and modulation at the output, the power-added efficiency (PAE) can become significantly higher [11]. Also, the use of DPD makes it possible to correct for nonlinear gain. This allows to operate at bias levels which result in higher efficiency at the cost of transistor linearity, without compromising the linearity of the whole amplifier.
Finally, the used transistor technology can greatly influence the efficiency due to differences in parasitics which can lower the efficiency of the device.

Table 1.1: Overview of state-of-the-art performance of Doherty PA's. Power backoff is at $-6\,\mathrm{dB}$.

Reference	PAE @ backoff	PAE @ $\mathbf{P_{MAX}}$	$\mathbf{P_{MAX}}$	Gain	Frequency	Technology
[12] 2017	$16.6\,\%$	$22.6\,\%$	$17.1\,\mathrm{dBm}$	$17.1\,\mathrm{dB}$	$37\,\mathrm{GHz}$	$130\,\mathrm{nm}$ SiGe
[13] 2013	$17\,\%$	$23\,\%$	$18\,\mathrm{dBm}$	$7\,\mathrm{dB}$	$42\,\mathrm{GHz}$	$150\,\mathrm{nm}$ GaAs
[11] 2016	$63\,\%$	$72\,\%$	$43.7\,\mathrm{dBm}$	$10.5\,\mathrm{dB}$	$1.8\,\mathrm{GHz}$	GaN HEMT
[14] 2016	$55\,\%$	$60\,\%$	$44\,\mathrm{dBm}$	$10\,\mathrm{dB}$	$1.95\,\mathrm{GHz}$	GaN HEMT
[15] 2015	$38\,\%$	$64\,\%$	$47.34\,\mathrm{dBm}$	$43\,\mathrm{dB}$	$2.45\,\mathrm{GHz}$	GaN HEMT
[16] 2015	$53.4\,\%$	$64\,\%$	$44\,\mathrm{dBm}$	$9.1\,\mathrm{dB}$	$1.94\,\mathrm{GHz}$	GaN HEMT

1.4.3 Envelope Tracking

Envelope tracking PA's track the signal envelope and vary the drain supply voltage continuously, this improves the efficiency compared to conventional PA's. This class of PA's can also rely on DPD. In [17] the performance of a DPD and non-DPD envelope tracking amplifier is compared. The article contains a table comparing the results from

other studies, and is also shown in Table 1.2. The main drawback of ET is that it becomes increasingly harder to track envelopes as the bandwidth increases. This gives ET a disadvantage in the development of PA's for future wireless networks, which will operate at high frequencies and large bandwidths.

Table 1.2: Comparison of different ET tracking PA studies, from [17]

Reference	PAE @ P_{MAX}	P_{MAX}	Gain	Frequency	DPD
[18] 2012	57.3 %	43.6 dBm	13.57 dB	0.78 GHz	yes
[19] 2013	32.4 %	30.2 dBm	7.4 dB	9.23 GHz	no
[20] 2011	57.2 %	40.2 dBm	18 dB	0.89 GHz	yes
[21] 2013	48 %	28.3 dBm	-	2.54 GHz	no
[22] 2013	47 %	46.3 dBm	6.5 dB	2.60 GHz	yes
[17] 2016	54.4 %	39.2 dBm	16.5 dB	0.88 GHz	no
[17] 2016	52.8 %	38.7 dBm	15.3 dB	0.88 GHz	yes

1.4.4 Outphasing

Outphasing PA's exploit the conversion of amplitude modulation to differential phase modulation. This allows the two PA's to operate at peak saturation power at peak efficiency. In [23] a multi-level outphasing PA is studied, the drain supply for the two amplifiers is varied here, which allows for a smaller outphasing angle. The PA's can operate at increased efficiency and the power combiner has less constraining design requirements because of the smaller outphasing angle. This paper shows the combination of a high PAPR PA technology, with the concept of drain supply modulation to increase the efficiency. The average total efficiency attains 48 %, at a frequency of 9.7 GHz.

1.4.5 GaN HEMT technology

This section will give a brief overview of the properties of gallium-nitride high electron mobility (GaN HEMT) devices and discusses some of the properties that make this type of semiconductor specifically interesting for this application.
GaN is a semiconductor material very suitable for RF applications. GaN technology outperforms Si LDMOS in efficiency and power density in most applications [24] while also being applicable for operation up to several 100 GHz. Useful material properties of GaN are its hardness, mechanical stability, heat capacity and thermal conductivity. It also has very low sensitivity to ionizing radiation [25]. This makes the technology interesting for the aerospace industry. At the moment, GaN technology still has several times the price of LDMOS per die. As a result, it is not popular on the low frequency market. When the frequency increases, packaging and assembly become more expensive than die cost. This is where GaN HEMT technology comes in.

2

Programme of Requirements

The switched device PA implements a method to achieve higher efficiency at back-off than traditional (class A, AB, B) amplifiers. The efficiency-power relation should be similar to that of a Doherty PA.
This chapter covers the behaviour the PA should exhibit, as well as the quantitative performance specifications.

2.1 Functional Requirements

This section describes the functions the switched device PA must be able to perform. As the principles behind the functionality of this PA are quite simple, the amount of functional requirements will be concise.

2.1.1 PCB

The simulated PA has to be implemented on a PCB, which should be usable as a prototype. The PCB should therefore allow for a basic implementation of the designed circuit and provide room for modifications.

2.1.2 Linearity

Both branches (peak and main) of the PA must be able to amplify a single-tone input signal according to the linearity requirements given in the next section. This is the most straightforward requirement, as this proves basic operation of the branches. The primary goal of the proof-of-concept is to show the efficiency potential of a single-tone operation. The amplifier will be optimized for this operation, meaning no extra measures (e.g. DPD) will be taken to optimize the performance for multi-tone operation.

2.1.3 Switching

The most distinctive functional requirement is the switching of operation between the branches. At the chosen threshold ($-6\,\mathrm{dB}$ backoff), the operation must switch from one device to the other. This must be realized by controlling the gate bias of both devices such that one device will become biased in cut-off, while the other will bias such that it can amplify the signal.
For this proof-of-concept, it is of minor importance to suppress anomalies that arise from the switching itself. As suppressing these anomalies requires digital predistortion (DPD) and/or a custom gate bias voltage switching profile, designing effective solutions to this problem is considered to be out of the scope of this project. It suffices to show that the steady-state behaviour of the PA is as required.

2.1.4 Coupling

The PA must be designed such that the (input/output) signals will not interfere with the bias/supply voltages of both device sections. To achieve this, coupling networks have to be designed which, besides from AC/DC (de)coupling, take care of shorting harmonic components that arise from the signal transfer.

2.1.5 Stability

Another, important aspect is guaranteeing stable operation of the devices. At frequencies where the devices provide higher than unity gain, the devices must be stable to avoid oscillations. This is a critical requirement, because if this is not guaranteed, noise or switching on/off the gate bias or signal could result in oscillations blocking functional signal transfer.

2.2 System Requirements

As the goal of the project is to prove the efficiency potential of the switched device amplifier, the efficiency specification is the most important to strive for. The efficiency targets are to be at least similar to that of the current state-of-the-art of Doherty PA's, as this PA architecture has the same profile of its efficiency on input power characteristic [5].
Consulting Table 1.1, an indication of the efficiency requirement can be given. Given that the switched-device PA must operate at $100\,\mathrm{MHz}$ at a maximum output power of $40\,\mathrm{dBm}$ without using DPD, it is reasonable to aim for efficiencies similar to the low frequency PA's from Table 1.1. The operation at lower frequencies makes it easier to achieve higher efficiencies, while not using DPD gives lower feasible efficiency levels. This is because bias levels providing more efficient but nonlinear transistor operation cannot be chosen as the non-linearity cannot be corrected for. A reasonable minimum efficiency specification was, using these considerations, chosen to be $55\,\%$ for the $-6\,\mathrm{dB}$ back-off power and $65\,\%$ for maximum power operation.
As the maximum output power was given to be at a maximum gain compression level of $-1\,\mathrm{dB}$, this compression level value was also set to be the maximum allowed gain

ripple level, as no DPD will be used. Obviously, it is preferred to achieve a lower ripple without compromising the efficiency specifications and vice versa.
Finally, the transistor devices for the PA were already provided. The used devices are the CREE GaN HEMT CGH40010 transistors [26]. The GaN devices manufactured by CREE are proven to be very reliable and effective, as all references in Table 1.1 using GaN technology also used devices produced by CREE.

Table 2.1: System requirements specifications

Parameter	**Value**
P_{max} @ $-1\,\mathrm{dB}$ compression	$40\,\mathrm{dBm}$
Carrier frequency	$100\,\mathrm{MHz}$
PAE @ P_{max}	$>65\,\%$
PAE @ $-6\,\mathrm{dB}$ backoff	$>55\,\%$
Gain ripple	$<-1\,\mathrm{dB}$
Technology	GaN HEMT (CREE CGH40010)

3

Design Description

In this chapter, the design of the circuit and the bias and supply voltages will be explained. A schematic of the resulting, full PA circuit is included in Appendix A. The next section will give an overview of the PA and its different building blocks. This is to make clear what the relation is of all designed blocks, which are discussed in the other sections, with respect to the complete PA system.

3.1 Amplifier Topology

Fig. 3.1 shows an overview of the switched-device PA. This is a block schematic version of the circuit in the proposal [5]. Also, blocks for stability compensation and supply/bias (de)coupling were added.

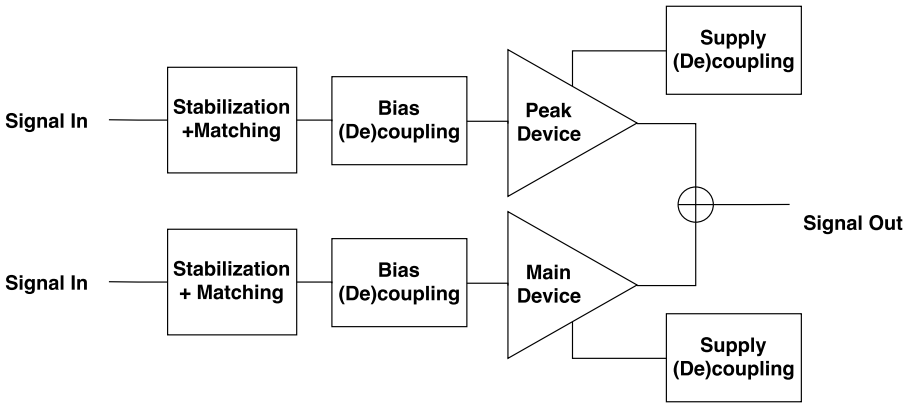


Figure 3.1: Block Diagram of PA system, subdivided in blocks used to split the design in different sections.

When the output power is between P_{MAX} and $-6\,\mathrm{dB}$ back-off, the upper branch is active and the lower branch is biased in cut-off. For output powers lower than $-6\,\mathrm{dB}$, the situation is reversed. Using this technique, only one of the transistors is active for each output power level. In Fig. 3.2 it is shown how the DC current varies along the output power for both devices. The effect of switching the device is clearly visible.

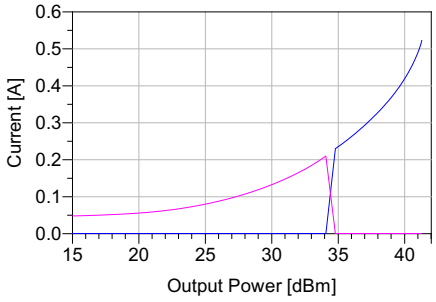


Figure 3.2: Current of main PA (purple) and current of peak PA (blue) along the output power range. At $P_{out} = 34\,\mathrm{dBm}$, the branches switch between their operation modes.

This switching of an active device allows for a simple output power coupling topology, as will be explained in Section 3.5. Also, as the main branch (or PA) will have approximately half the supply voltage of the peak PA. This allows for efficiencies at back-off close to efficiencies at P_{MAX}.
The system design is split in the parts seen in the block schematic. In the next sections, the design choices of each individual type of block will be discussed. For every block, examples of just one of the branches will be given, as design examples of the other branch yield very similar results and the design is performed using an identical approach.

3.2 Bias and Supply

This section discusses the choice of gate bias and supply voltages needed for the peak/-main devices in Fig. 3.1. The section is split in two parts: the gate bias and the supply voltage.

3.2.1 Gate Bias

The choice of the gate bias depended on two factors: maximum efficiency of the PA class and the linearity of the transfer.
The gate bias voltage corresponding to class A operation of the devices yields a theoretical maximum efficiency of $50\,\%$ [27] at optimal linearity. Due to the low efficiency, this bias was not an option. Devices biased at lower gate voltages can achieve higher efficiency at the cost of reduced linearity and worse distortion behaviour, as a result of the sub-2π conduction angle [27].
Lower bias voltage operations (class AB to class B) were investigated. In these classes,

second-order harmonics are the dominant source of distortion and for class B the even-order harmonics are, ideally, the only source of harmonic distortion [27]. The threshold voltage of the used GaN HEMT was checked by simulation. Fig. 3.3 shows that this threshold voltage V_T is near $-3.40\,\mathrm{V}$ for V_{DS} between $15\,\mathrm{V}$ and $35\,\mathrm{V}$. As this threshold could differ per device, it is important to consider the drain-source current I_{DS} rather than the gate-source voltage V_{GS}. Therefore, the current data provided by sweeps such as the ones showed in Fig. 3.3 was also used to set the correct gate bias for the real devices in the testing phase of the project.

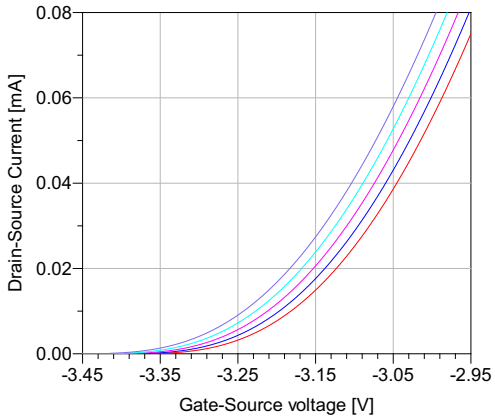
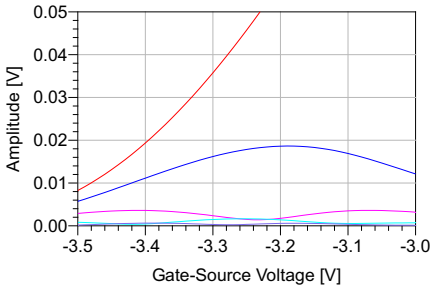
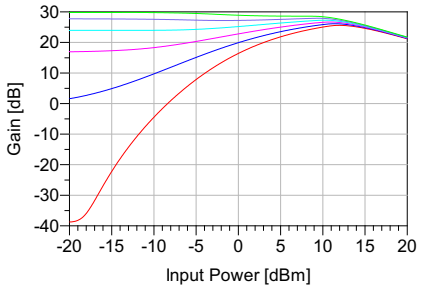


Figure 3.3: Plot for checking the threshold for the GaN HEMT for different drain-source voltages (V_{DS}). From left to right: $V_{DS} = 35\,\mathrm{V}$, $30\,\mathrm{V}$, $25\,\mathrm{V}$, $20\,\mathrm{V}$ and $15\,\mathrm{V}$.



(a) Voltage amplitudes of harmonic components at PA output for gate voltage sweep. Harmonics are the first harmonic (red), the second (blue), the third (purple) the fourth (cyan) and the fifth (grey). Simulation conditions: $V_{DS} = 32V$, input power: $-5\,\mathrm{dBm}$



(b) Gain over input power sweep for different gate biases V_{GS}. From up to down: $V_{GS} = -2.9\,\mathrm{V}$, $-3.00\,\mathrm{V}$, $-3.10\,\mathrm{V}$, $-3.20\,\mathrm{V}$, $-3.30\,\mathrm{V}$, $-3.40\,\mathrm{V}$ and $-3.50\,\mathrm{V}$.

Figure 3.4: Standalone device test for harmonics and linearity

As will be explained in Section 3.3, the second(/even)-order harmonics can eas-

ily be removed from the output spectrum. This leaves the odd-order harmonics as a source for distortion. Fig. 3.4a shows that a deep class AB bias operation at $V_{GS} = -3.23\,\mathrm{V}$ would therefore be optimal in terms of harmonic distortion, due to the minimum in odd-order harmonics. The class B operation (near $V_{GS} = -3.45\,\mathrm{V}$) introduces nonzero odd-order harmonics, which can be explained by the device being very nonlinear at this bias level (Fig. 3.3). However, for a more linear transfer, $-3.0\,\mathrm{V}$ for V_{GS} would be preferable (Fig. 3.4b). Therefore, a V_{GS} of $-3.0\,\mathrm{V}$ was chosen as bias voltage for the simulated transistor. The bias current I_{DS} is then further determined by the drain supply voltages.
The DC (de)coupling is implemented using a capacitor for the DC block and an inductor for the DC feed. A resistor could also have been used to couple the bias voltage to the gate, but simulations predicted a non-constant voltage transfer to the gate when using resistive coupling. This can be explained by the (non-constant) resistance present in the device/package itself, resulting in a voltage division. For the sake of simplicity, an inductor was therefore used. Because the impedance of the gate bias source is not accurately known, a shunt capacitor, chosen to have a very low impedance at $100\,\mathrm{MHz}$ is also included to short AC to ground at the source-side of the inductor. This guarantees correct decoupling of the input signal, as the detected impedance at the gate is then just the (large) impedance of the inductor.

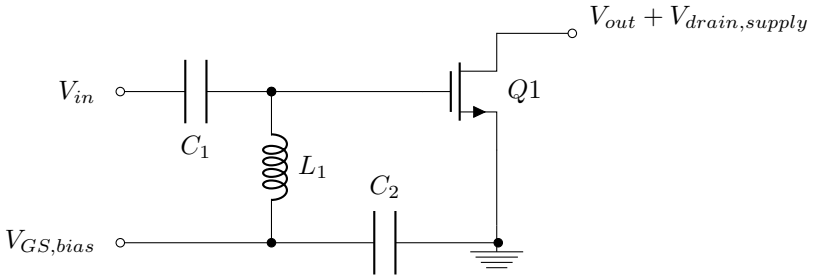


Figure 3.5: Bias (de)coupling circuit section

3.2.2 Drain Voltage

For the switching threshold, $-6\,\mathrm{dB}$ power back-off was chosen as a suitable point, as this is a very common back-off level for Doherty PA's. Other back-off power levels could be chosen as well, dependent on the PAPR level of the signal envelope. For the sake of simplicity for comparing the result to Doherty PA's (Table 1.1), the $-6\,\mathrm{dBm}$ back-off level was chosen. Also an optimization can be done on the average efficiency of the PA, depending on switching threshhold.

The peak device supply DC voltage is dictated by the maximum power requirement ($40\,\mathrm{dBm}$). The main drain device supply voltage on the other hand, is dependent on the back-off power level, which is $34\,\mathrm{dBm}$. The minimal needed voltage levels are given in Eq. 3.1. In reality, somewhat higher voltages are needed as a result of hard compression of the PA. This happens when the drain-source voltage, as a result of the

output signal voltage level, passes beyond the knee voltage V_{knee} of the devices.

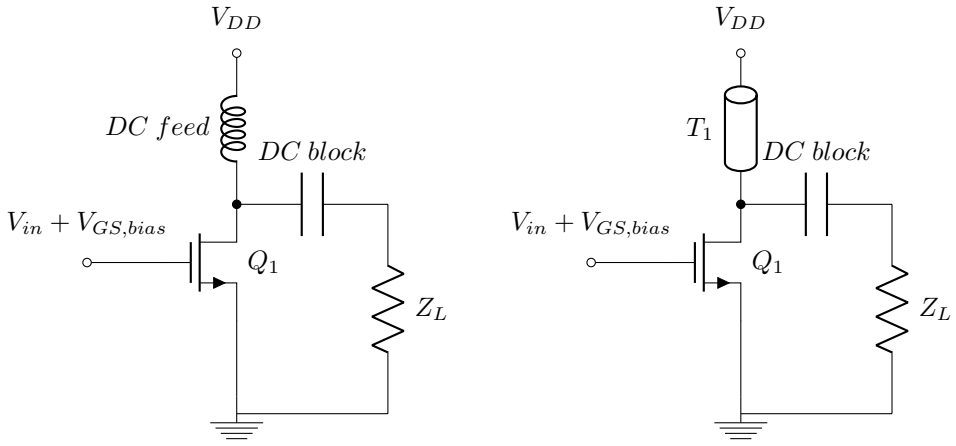
$$V_{supply,peak} = \sqrt{2R_{load}P_{MAX}} \approx 32\,\mathrm{V} \tag{3.1}$$

$$V_{supply,main} = \sqrt{2R_{load}P_{Backoff}} \approx 16\,\mathrm{V} \tag{3.2}$$

Using the chosen supply and gate bias voltage levels, the I_{DS} levels were determined using the I_{DS}/V_{GS} characteristics of the devices at the chosen supply voltages.

3.3 Power Supply Coupling

At the drain supply, no AC signal must be present, as this node should only have a DC voltage. A large inductance inductor (DC feed) between the supply and the drain would be appropriate, as it shorts DC and blocks AC. This is practically not feasible, since the inductor would have an extremely large inductance. Additionally, this would not filter out the prevailing second-order harmonic components in the output signal introduced by the near-class B operation of the device [27]. An alternative that also decouples the signal from the supply is a $\lambda/4$-transmission line (TL). A drawback of this implementation is the relatively large cable length required at $f = 100\,\mathrm{MHz}$. The schematic for using both options is shown in Fig. 3.6.



(a) Decoupling circuit using a large inductor (DC feed)

(b) Decoupling circuit using a $\lambda/4$-transformer

Figure 3.6: Power supply decoupling implementations, the supply (de)coupling block from Fig. 3.1 is implemented by the inductor or the TL connected to the drains, respectively

The $\lambda/4$-transformer can be tuned to the system frequency ($100\,\mathrm{MHz}$). In order to adequately decouple the fundamental signal from the supply, the drain must 'see' an

open circuit at the input of the TL (characterized by an antinode of the electric wave). In order to realize this, the supply-end of the TL must be grounded for the fundamental AC component. As a result of the $\lambda/4$ length of the TL, this ground is detected as an antinode at the drain-end of the TL (see Fig. 3.7) and thus decouples the fundamental frequency from the drain. For the second-order harmonic (and all higher-order, even harmonics), the TL directly connects the drain to the ground, such that this component is shorted and will not be transferred to the load.

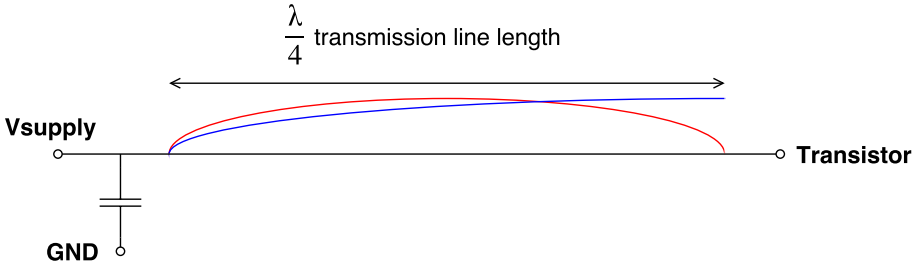


Figure 3.7: Visualisation of how a $\lambda/4$ TL decouples the fundamental while shorting the second-order harmonic. The blue wave indicates fundamental signal, the red wave the second-order harmonic. At the transistor-side, an antinode is observed at the fundamental frequency (open circuit), while a short is detected at the second-order harmonic

As the impedance of the power supply is unknown, grounding of the fundamental and the harmonics must be implemented by connecting capacitors to the supply-end of the TL. To improve the decoupling of AC to the supply, a wide range of frequencies should be shorted to ground at the supply. Therefore a range of different capacitances should be connected at the supply. Capacitors were chosen for their resonance frequency, originating from parasitic inductances. These parasitics are inherent to the packaging and are in the order of $1\,\mathrm{nH}$ for the 0805 package [28]. The different harmonic filter capacitors are shown in Fig. 3.8.
To conclude this part of the design, the implemented supply (de)coupling block from Fig. 3.1 is shown in Fig. 3.8, consisting of the TL and the decoupling capacitors.

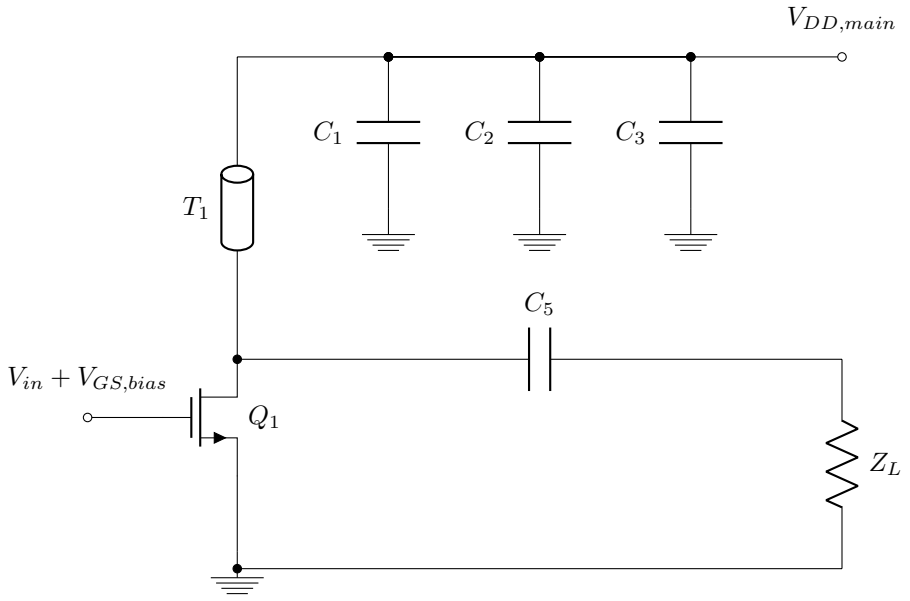


Figure 3.8: Power supply decoupling circuit, with harmonic filters, the values of the harmonic filter capacitances are $C_1 = 10\,\mu\text{F}$, $C_2 = 680\,\text{pF}$ and $C_3 = 2.7\,\text{nF}$

3.4 Stability

Ensuring stability of devices in the PA is critical for correct operation. Using devices under unstable conditions can trigger oscillations to be produced by the device (due to poles present in right half-plane). This troubles linear amplification of input signals.
Evaluating the stability was done using an alternative format [29] of the Rollett stability factor equation [30] that employs S-parameters instead of Y-parameters. Eq. 3.3 shows the used equation for evaluating the stability. The device is unconditionally stable (i.e. stable for all passive input/load impedances) when $K > 1$ and $\Delta < 1$ for all frequencies in which the device has more than unity gain.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{21}|} \tag{3.3}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.4}$$

According to [26], the device has $K < 1$ at a higher than unity Maximum Available Gain (MAG) at least between $0.5\,\text{GHz}$ and $3.4\,\text{GHz}$, therefore stability compensation is needed.
Evaluation and compensation for the stability properties of the GaN device was performed in the following steps:

1. Evaluating stability using idealized circuitry under designed bias conditions

2. Simple input impedance matching using a shunt resistor, evaluate stability again
3. Estimating stability compensation using stability circles
4. Changing ideal biasing circuitry (RF choke, DC block) for real components (TL, capacitors, inductors)
5. Optimization for input impedance, gain and stability using the ADS optimization function.

The following section will explain the first step, the standalone stability characteristics of the device and show the urge for stability compensation. Section 3.4.2 will explain the other steps, considerations and methodology in ensuring the stability of the device.

3.4.1 Uncompensated Stability Characteristics

Using the device biased using ideal (de)coupling as shown in Fig. 3.9, the standalone stability characteristics of the GaN device was determined. The value of K is important at all frequencies below approximately $10\,\mathrm{GHz}$ (near the frequency at which the GaN device has unity gain), and not just $100\,\mathrm{MHz}$. 'RF' chockes or DC feeds were used instead of $\lambda/4$ TL's. This minimizes the influence of all components but the transistor on the stability and gain behaviour of the circuit.
The results of these simulations are shown in Fig. 3.10.

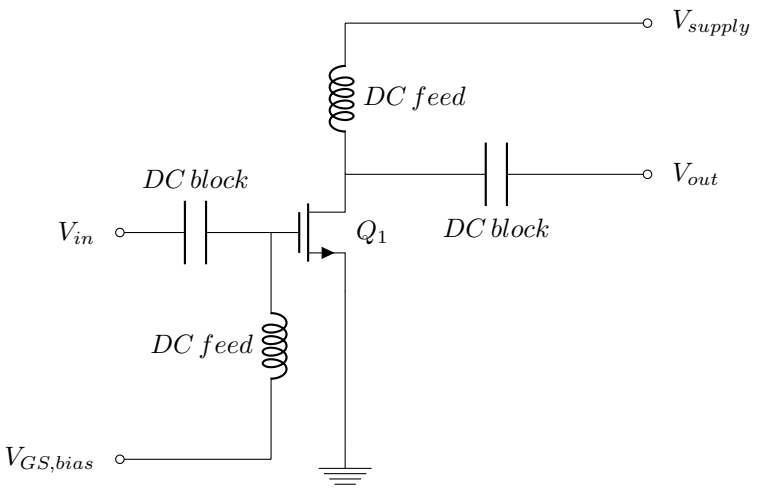
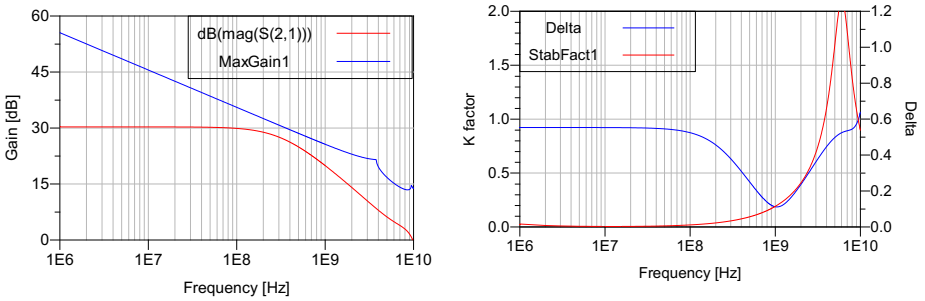


Figure 3.9: Circuit used to determine stability of standalone device. Biasing performed using ideal DC and AC blocks.



(a) Maximum available gain (G_{MAX}) and forward transmission (gain) parameter $S_{2,1}$

(b) Stability factor K and Δ

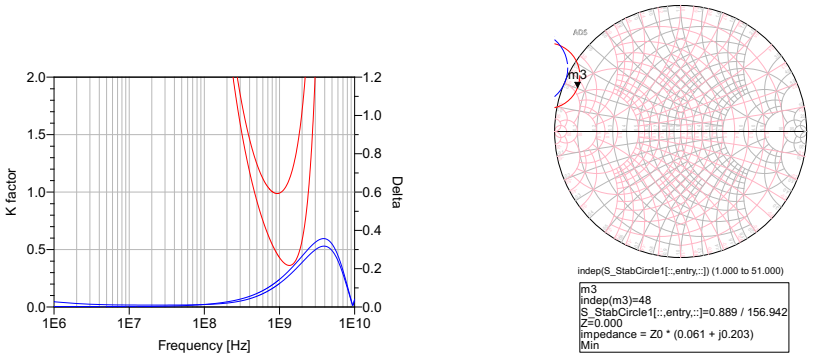
Figure 3.10: Results of standalone stability analysis using S-parameter simulation

Fig. 3.10 shows that the device is not unconditionally stable. The results are very similar to the data given in [26]. Also, due to input mismatch, the actual gain of the device is far below G_{MAX}. The first step after this observation was to place a shunt resistor at the input of the devices.

3.4.2 Compensated Design

After a shunt resistor (R_2 in Fig. 3.12) of $50\,\Omega$ was added to the input of the devices to match the input to the signal generator output impedance, K became larger than 1 at lower frequencies ($f < 400\,\text{MHz}$). Between $400\,\text{MHz} < f > 3\,\text{GHz}$, K was still smaller than 1 (red curve in Fig. 3.11a). Therefore another stability compensating resistor is needed.
The effectiveness of the shunt resistor can be explained by the reduction of the S_{11} (input reflection S-parameter) and thus causing the division in Eq. 3.3 to become larger. Another explanation can be given by using stability circles [29] drawn in a Smith Chart. The boundaries of these circles indicate input/loading reflection coefficients at which the device is on the brink of unstable operation. Areas enclosed by the circles indicate reflection coefficients (and thus input/load impedances) at which the device behaves in an unstable way. As long as the circles do not enclose parts of the unit circle (positive resistance at load/input) in the Smith chart at all frequencies lower than the frequency of unity gain, the device is considered unconditionally stable.
These circles were used to perform an estimation of the needed series resistor used to compensate for the conditional stability between $400\,\text{MHz} < f > 3\,\text{GHz}$. This series resistor was placed directly after the input, before the shunt resistor. A resistor in the order of $3\,\Omega$ or higher appeared to be sufficient. This method and the result of the estimation is visualized in Fig. 3.11.
The red circle in Fig. 3.11b indicates the stability circle at approximately $880\,\text{MHz}$, which has a K below 1 (Fig. 3.11a). Using the marker in the stability circle, the required resistance to shift the stability circle out of the unit circle can be estimated. The shifted circle is shown in blue in Fig. 3.11b. The series resistor assures that the

GaN device can never 'see' an impedance lower than the minimum impedance required for stability.



(a) Stability factor K and Δ with and without series resistor compensation

(b) Stability circle at $880\,\mathrm{MHz}$ with (blue) and without (red) a series resistor compensation.

Figure 3.11: Results of stability analysis using with (blue) and without extra series resistor of $Z_0 * 0.061 \approx 3\,\Omega$ placed before the shunt resistor of $50\,\Omega$

An extra series resistance increases K but at the same time decreases (due to voltage division) the gain of the PA. Also the combination of a series resistor at the input and the $50\,\Omega$ shunt resistor behind it changes the input impedance. After replacing the ideal DC blocks and AC blocks with practical capacitors, inductors and a $\lambda/4$ TL at the drain supply, this trade-off was solved using the ADS optimization function. This resulted in slightly larger values for the series resistor (around $10\,\Omega$) to give headroom for the K factor and slightly smaller values for the shunt resistor ($40\,\Omega$ to $45\,\Omega$) to compensate for the change in input resistance. The circuit used to evaluate stability of this practical implementation is shown in Fig. 3.12. The stability compensation and matching is thus implemented by the series and shunt resistor combination placed directly after the input. Optimization of the input reactance was not considered necessary as the input reactance was already relatively low (approximately $8\,\Omega$) compared to the input resistance.

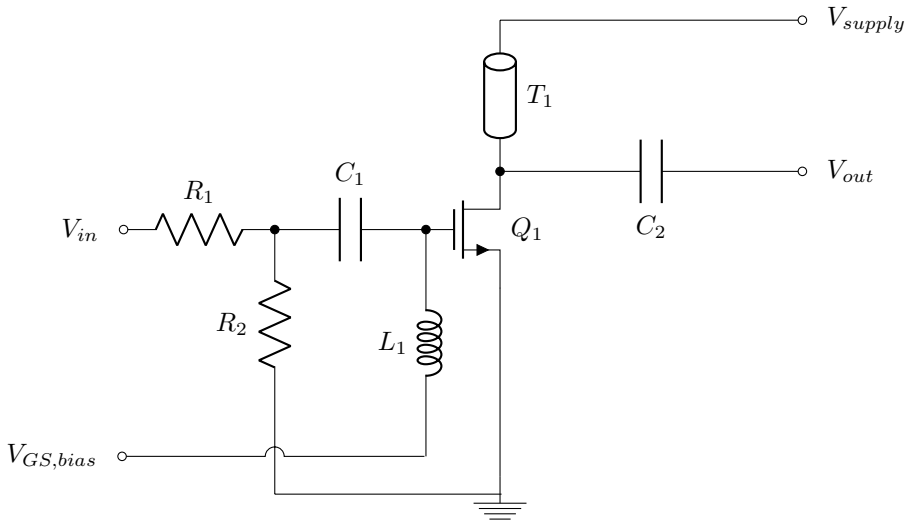
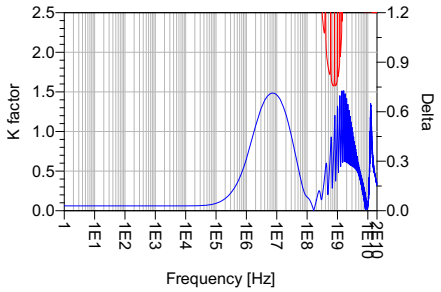
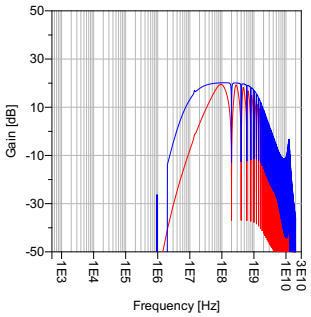


Figure 3.12: Designed stability compensated circuit. Connected to the gate are the components stabilizing the device ($R_{1,2}$) and the ones (de)coupling the sources (C_1, L_1, T_1)

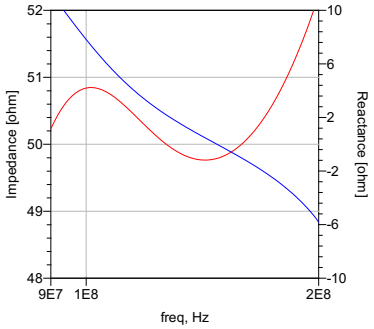
The results of the optimization and the parameters of interest are shown in Fig. 3.13. This figure show the result of the S-parameter analysis using the available component values, being close to the values determined by the optimization.
Evident from Fig. 3.13 is the close approximation of the gain to G_{MAX}, compared to the standalone gain, as now the input matching is adequate.



(a) Stability factor K (red) and Δ parameter (blue) curve for resulting topology



(b) Gain (red) and G_{MAX} (blue) for resulting topology



(c) Input impedance, i.e. resistance (red) and reactance (blue), for resulting topology

Figure 3.13: Results of resulting stability analysis using S-parameter simulation. Lobes and perturbations in characteristics are a result of the $\lambda/4$ TL, shorting even harmonics of the 100 MHz signal.

3.5 Output Power Coupling

The output signals of the two amplifiers have to be combined at the (single) output port. There is a good amount of research done on this topic, providing various methods for power combining [31], [32], these methods achieve high isolation of the divider ports, and proper matching of those ports. This is particularly useful when combining power from two simultaneously active sources. It is unnecessary for this amplifier topology, since for only a small period of time of the signal envelope (during a switch), both amplifiers are (to a certain extent) on.

The most simple solution is to directly connect the two outputs. However, a DC voltage is always present on both amplifiers, so DC decoupling is required. Two capacitors can solve for this problem. As these capacitors (0805 package used) suffer from the same parasitic inductance as the capacitors from Fig. 3.8, the capacitances for the output combining should be chosen such that the LC-combination resonates at 100 MHz.

An alternative approach can be found in [33], where multiple primary coils on a transformer are used to combine signals. This method also DC decouples the amplifiers from the output. For this design, capacitors where chosen for their availability, ease of use and reliability.
This implements the last block of Fig. 3.1 and concludes the circuit design.

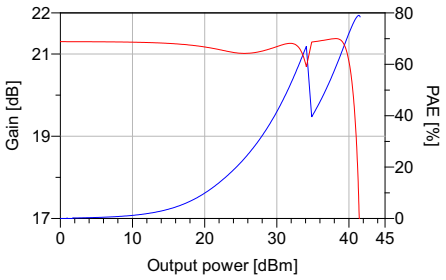
4

Evaluation

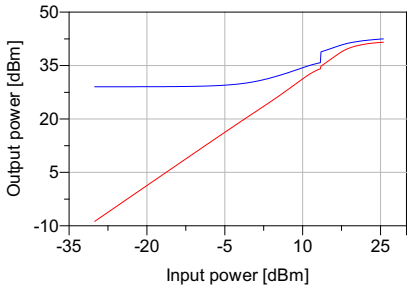
This chapter will present the results of the PA simulation (PAE, gain), the process of realizing the design and the test results of the PA realized on the PCB.

4.1 Simulation Results

This section presents the simulated PA performance regarding efficiency, linearity and distortion over the input power sweep. The simulation was performed using the circuit that resulted after combining all subcircuits described in chapter 3. Fig. 4.1 gives the resulting gain and PAE of the switched-device PA. The PA gives a gain of $20.9\,\mathrm{dB}$ at a ripple below $0.3\,\mathrm{dB}$ (before entering the region of hard compression). The $-1\,\mathrm{dB}$ compression point lies at an output power of $40.2\,\mathrm{dBm}$.
According to the simulations, the PA has a PAE of $67.0\,\%$ at $-6\,\mathrm{dB}$ output power backoff and $71.9\,\%$ at P_{MAX}.



(a) Simulated gain (red) and PAE (blue) vs. output power of switched-device PA



(b) Output (red) and DC (blue) power vs. Input power of PA

Figure 4.1: Simulated output power vs. input power of switched-device PA

The distortion behaviour of the PA was also investigated. Simulation predicts that the 3rd-order output intercept point (OIP3) is located at an output power of $41\,\mathrm{dBm}$. Fig. 4.2 shows the output powers and the tangents used to find the OIP3.

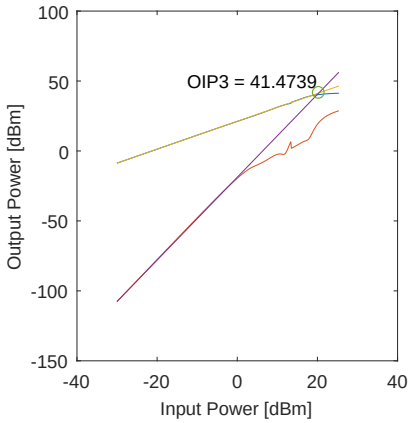


Figure 4.2: Simulated third harmonic, fundamental power vs. output power of PA. OIP3 is also indicated

4.2 Prototype Realization

A prototype is realized to verify the simulations and to observe the non-idealities that are introduced in practice. In Fig. 4.3 the full layout of the PA can be seen. In this section important considerations regarding the realization are discussed.
The PCB is based on $1\,\mathrm{mm}$ thick FR4 material. Several concepts where used to guide the design, based partially on [34]:

- Use the bottom copper as a ground plane.
- Use the top copper for traces, and fill up the remaining space with a ground plane, connected to the bottom copper through many vias. This provides a low impedance path for decoupling.
- Minimize distance between gate connector and device gate, providing low impedance, to minimize the possibility on oscillations.
- Decouple power supply as close as possible to the connector, to minimize current loops.

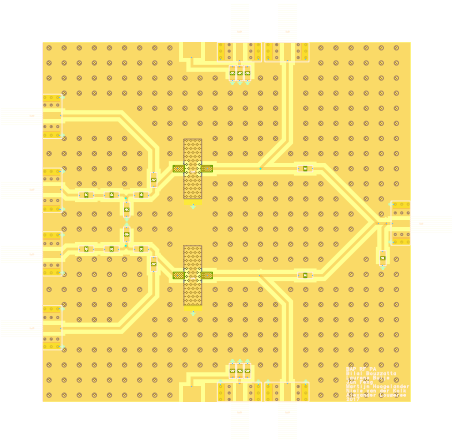


Figure 4.3: PA prototype PCB layout

For accurately calculating the length of the coaxial TL, the microstrip TL length on the PCB has to be taken into account. The 'line impedance calculator' utility in ADS was used to calculate the electrical length of the microstrip.

The length of the microstrip between the supply node and the transistor drain was approximately $4\,\mathrm{cm}$ ($1590\,\mathrm{mil}$). Using the ADS utility, an electrical length of $8.64°$ at $100\,\mathrm{MHz}$ was found.
The required electrical length from the coaxial transmission line was calculated as follows:

$$E = 90 - 8.64 = 81.36° \tag{4.1}$$

The length of the coaxial part of the TL, given the velocity factor $v_f = 0.695$ of the cable (found here [35]) is calculated using Eq. 4.2 and Eq. 4.3.

$$\lambda = \frac{cv_f}{f} \tag{4.2}$$

$$l = \frac{\lambda E}{360} = \frac{cv_f E}{360 f} = 0.47\,\mathrm{m} \tag{4.3}$$

The prototype was fabricated and is shown in Fig. 4.4

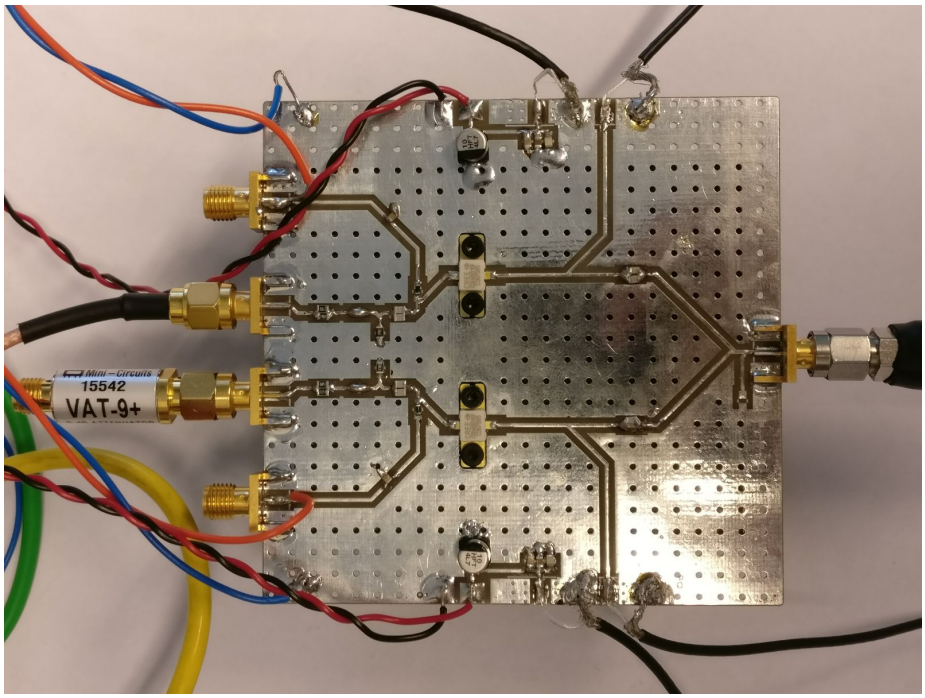


Figure 4.4: Photograph of prototype

4.3 Prototype Results

The PAE has been obtained from the prototype by performing an input power sweep at the chosen supply voltages and I_{DS} currents. The measurement system was provided by the measurement section of the project group and its schematic is shown in Fig. 4.5 [36]. A single-tone, steady state test was conducted for this sweep. The result is shown in Fig. 5.2.

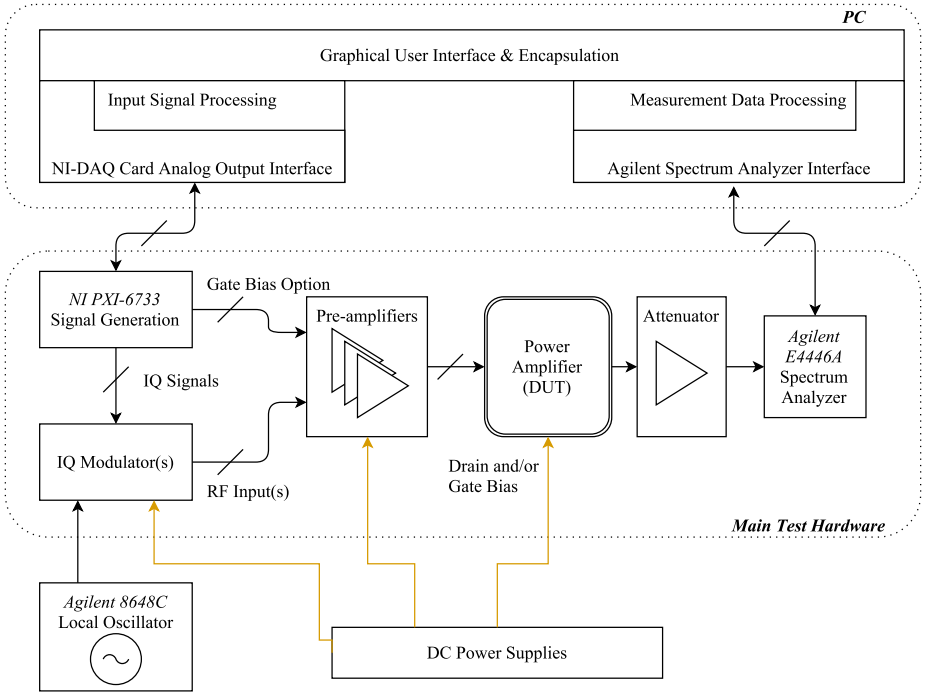


Figure 4.5: Schematic of used setup to test the prototype. Schematic was provided by the project subgroup responsible for the test setup and PA drives

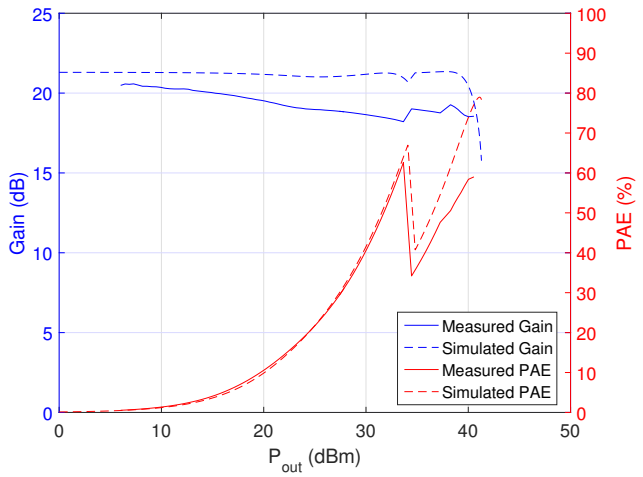


Figure 4.6: Gain and PAE vs. output power, $V_D = 32\,\mathrm{V}$

The main PA very closely matches its simulated counterpart (PAE $\approx 63\,\%$ @ $-6\,\mathrm{dB}$ power backoff instead of $67\,\%$). The peak PA however, gives a PAE of $60\,\%$ instead of the simulated $72\,\%$ and thus has a considerably lower efficiency than simulated. Possible origins of this lack of performance are discussed in chapter 5.
The gain of the PA has a mean value of $18.5\,\mathrm{dB}$, has a maximum value of $19.80\,\mathrm{dB}$ and a minimum value of $17.15\,\mathrm{dB}$. The ripple is thus larger than the specified $-1\,\mathrm{dB}$.
Table 4.1 shows the studies from Table 1.1 again in addition to the results of this work.

Table 4.1: Comparison between state-of-the-art Doherty PA's and this work. Power backoff is at $-6\,\mathrm{dB}$.

Reference	PAE @ backoff	PAE @ $\mathrm{P_{MAX}}$	$\mathrm{P_{MAX}}$	Gain	Frequency	Technology
[13] 2013	$17\,\%$	$23\,\%$	$18\,\mathrm{dBm}$	$7\,\mathrm{dB}$	$42\,\mathrm{GHz}$	$150\,\mathrm{nm}$ GaAs
[11] 2016	$63\,\%$	$72\,\%$	$43.7\,\mathrm{dBm}$	$10.5\,\mathrm{dB}$	$1.8\,\mathrm{GHz}$	GaN HEMT
[14] 2016	$55\,\%$	$60\,\%$	$44\,\mathrm{dBm}$	$10\,\mathrm{dB}$	$1.95\,\mathrm{GHz}$	GaN HEMT
[15] 2015	$38\,\%$	$64\,\%$	$47.34\,\mathrm{dBm}$	$43\,\mathrm{dB}$	$2.45\,\mathrm{GHz}$	GaN HEMT
[16] 2015	$53.4\,\%$	$64\,\%$	$44\,\mathrm{dBm}$	$9.1\,\mathrm{dB}$	$1.94\,\mathrm{GHz}$	GaN HEMT
This work 2015	$63\,\%$	$60\,\%$	$40.25\,\mathrm{dBm}$	$19\,\mathrm{dB}$	$0.1\,\mathrm{GHz}$	GaN HEMT

In addition to gain and PAE measurements, OIP3 has also been calculated using an input power sweep. The linear amplification region was extrapolated for both 1st and 3rd order harmonics, yielding the OIP3 (see Fig. 4.7). The OIP3 was found at $P_{out} = 53.82\,\mathrm{dBm}$.

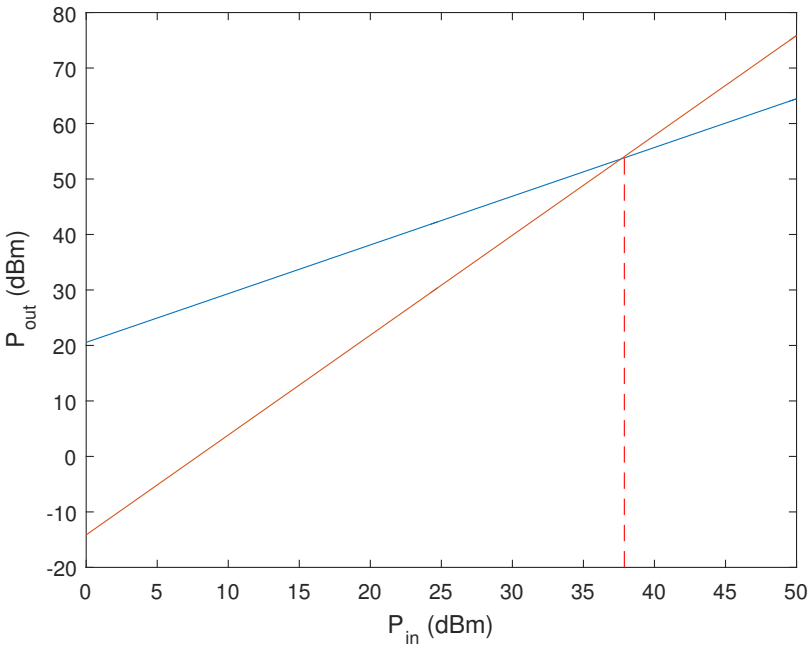


Figure 4.7: Measured OIP3, the blue line is the fundamental harmonic, the orange line the 3rd order harmonic

5

Discussion

The realization of the switched-design PA proved to be fully operational. However, not all specifications are met. The PAE of the peak PA does not reach the specified $65\,\%$ level. Surprisingly, the PAE of the main device does approach the specified peak efficiency level.
Also the ripple specification is not met. The ripple level exceeds the $-1\,\mathrm{dB}$ ripple with a maximum of $1.3\,\mathrm{dB}$ from the main gain level. Although the ripple specification is not exceeded by a large amount, the simulations predicted a ripple that was not larger than $0.6\,\mathrm{dB}$ before the beginning of hard compression near $40\,\mathrm{dBm}$. This gives a significant difference between the calculated and measured values.
In the following sections, the origins of these deviations from the simulated design are discussed. In the next chapter, chapter 7, steps to further investigate and solve these problems are discussed.

5.1 Additional Losses

Definite origins of the lowered gain level are the losses associated with the traces and connectors and (other) parasitics on the PCB. Those losses were not included in the simulation and thus automatically resulted in a lower gain level than expected.
These losses also result in lower efficiency levels and thus can also be used to explain the $2\,\%$ deviation of the actual main PA efficiency level from the efficiency level predicted by simulation.
However, for the $10\,\%$ error in the peak PA efficiency level, this explanation does not suffice on its own, as this error is significantly larger than the error from the predicted main PA efficiency.

5.2 Supply Voltage Headroom

As explained in Section 3.2.2, headroom in the drain supply voltage is needed in order to prevent the GaN devices going into the hard compression region at input power levels

which still need to be correctly amplified. This headroom was estimated by checking if simulations results still gave sufficient performance at the chosen supply voltage. It can be argued that, due to deviations between fabricated devices, not each device needs the same level of headroom in the supply voltages (V_{knee} may differ per device).
The gain characteristic in Fig. 5.2 from the test results does not show a clear hard compression shape compared to the simulated gain characteristic. This could mean that the drain supply of the peak PA is 'too high', i.e. the $-1\,\mathrm{dB}$ compression level lies beyond $40\,\mathrm{dBm}$ output power. If this is the case, then the supply level may be lowered, increasing the efficiency of the (peak) PA. This could explain the difference between the test results and the simulations regarding the peak PA efficiency, as the degree of impact of this factor can differ per device and thus per PA branch. Testing this hypothesis in ADS by lowering the peak supply voltage by $2\,\mathrm{V}$ resulted in an increase of efficiency of $5\,\%$ (Fig. 5.1) with respect to the previous simulation. This increase in efficiency resulted in the device being farther in compression at $40\,\mathrm{dBm}$ in the new simulation. However, in the prototype test, the compression was not yet observed at the simulated supply value of $32\,\mathrm{V}$. This means that the drain voltage could be lowered until the compression is observed.

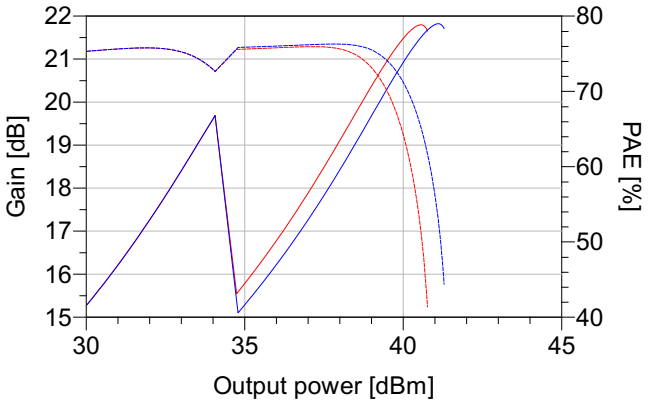


Figure 5.1: Parameters sweep of drain supply voltage. Hard compression starts at lower output power for a lower supply voltage. The red curves indicate the simulation using a lower V_{DS} than the initial design

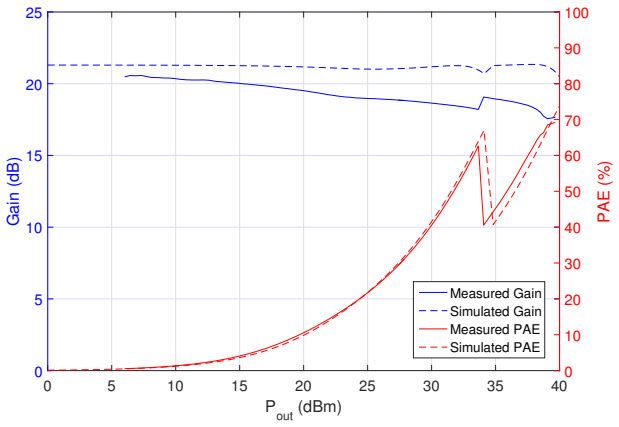


Figure 5.2: Gain and PAE vs. output power, $V_D = 26\,\mathrm{V}$

5.3 Transmission Line Length Mismatch

A mismatch in the length of the produced TL's also reduces the gain and the efficiency. This originates from inadequate transformation of the supply-side impedance (this should be near zero, due to capacitors) at the signal frequency. The transistor gain then does not observe an open circuit at $100\,\mathrm{MHz}$ and thus a portion of the signal power will flow to ground through the TL. This increases the lost signal power, reducing the gain and the efficiency. A mismatch in TL length at either branch of the PA will reduce the performance, even if the branch at which there is a mismatch is inactive is never active. The reason for this is that the branches are not isolated from each other at the signal frequency and thus the output signal from at the active branch could flow towards the inactive branch and through the TL which has a mismatch. Therefore, this component error affects the gain and efficiency of both branches and therefore does not explain the large error observed at the peaking PA. This hypothesis was verified by simulation. The results of this simulation are shown in Fig. 5.3 and show that mismatch in electrical length of a single TL affects the performance of both branches equally.

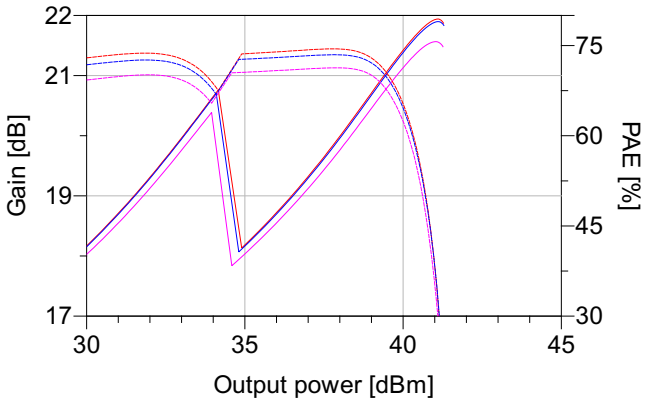


Figure 5.3: Testing the impact of peak PA TL length mismatch on the performance. dashed lines indicate the gain, solid lines the PAE. TL electrical lengths are, respectvely, $80°$ (red), $90°$ (blue) and $100°$ (purple)

5.4 Leakage Currents

During the test sweeps of the prototype, currents flowing from the drain supply of the device in cutoff were observed. These leakage currents at the main supply were, at most, $8\,\%$ of the total current provided by the power supply. As the PAE was calculated using the voltages and currents delivered at both drain supplies, this also reduces the efficiency. The origin of these leakage currents is the increasing gate bias that the input signal causes at increasing input power levels. This increases the channel leakage current in the inactive transistor.

5.5 Component Tolerances

The used GaN transistors have a wide range of variable parameters [26]. For example, the threshold voltage of the devices can vary between $-2.3\,\mathrm{V}$ and $-3.8\,\mathrm{V}$. The small signal gain can also vary (approximately $2\,\mathrm{dB}$) between devices. The many parameters prone to fabrication tolerances can thus easily affect the performance of the PA.
The temperature of the devices also plays a role. This was not taken into account in the initial design and in the simulations, but, when testing the PA, the peaking PA heated significantly. The temperature mainly affects the gain of the PA. This was observed using a parameter sweep in ADS, Fig. 5.4 shows the results. As can be seen, the efficiency is hardly affected (in the threshold region, the PAE jumps to different efficiency values due to the difference in gain) while the gain becomes lower at higher temperatures.
The gain of the peak PA shows an almost constant error with respect to the simulated gain. Because of the high output powers at which the peak PA operates, the temperature

of the device at these output powers is a realistic factor in the observed gain reduction. The increasing temperature with output power could explain why the error between the simulated gain of the main PA increases as the output power becomes larger.

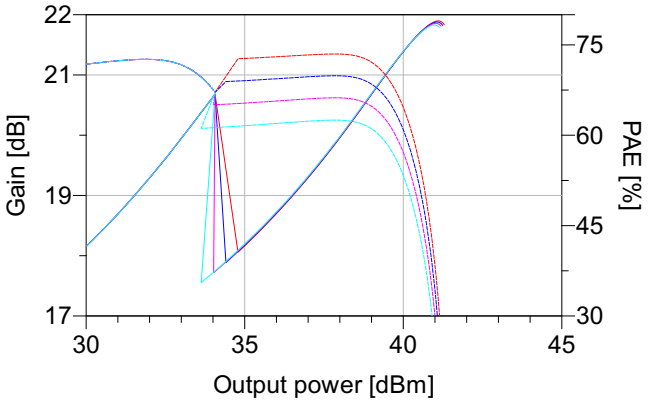


Figure 5.4: Parameter sweep of the temperature of the peak PA. The device was simulated at 25 °C (red), 50 °C (blue), 75 °C (pink) and 100 °C (cyan)

6

Conclusion

A switched-device PA was designed, simulated, realized and tested. This type of PA is designed for efficient operation in high PAPR modulation schemes. The high efficiency is achieved by switching between two different power modes. At P_{MAX}, one GaN HEMT amplifies the signal. This transistor is supplied with the voltage needed to provide P_{MAX} to the load. At power back-off ($-6\,\mathrm{dB}$ and lower), another GaN HEMT supplied with approximately half the supply voltage of the other transistor amplifies the signal. When the mode of operation is switched, the device that was active before is switched of and vice versa.
The PA achieved a PAE of $63\,\%$ at $-6\,\mathrm{dB}$ back-off and $60\,\%$ at P_{MAX} ($40\,\mathrm{dBm}$). The designed PA operates at a frequency of $100\,\mathrm{MHz}$. The attained PAE characteristic and levels are comparable to the efficiencies achieved by state-of-the-art Doherty PA's. Also, the topology of the switched-device is much simpler than Doherty PA's due to its simple output power coupling.
The peak PA branch suffered from a significantly lower PAE than was simulated. A number of explanations for this flaw were presented and are to be investigated.

7

Recommendations

This chapter is divided into two part: Section 7.1 will focus on the steps that are recommended for improving the performance of the prototype, without adding extensive new techniques, such as predistortion.
The second part, Section 7.2 will discuss some ideas (for future projects) on improving the performance or functionality of the prototype, using techniques that are not used for designing the current prototype.

7.1 Improving the Performance

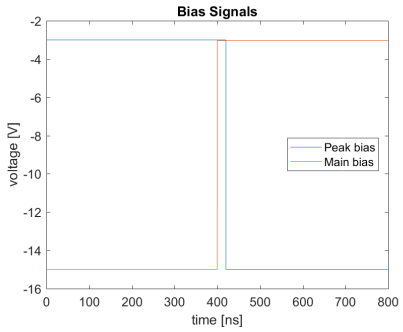
The hypotheses of chapter 5 are to be investigated. Tests at lower peak supply levels should be performed to check when hard compression is observed near the $40\,\mathrm{dBm}$ (@ $-1\,\mathrm{dB}$ compression), as was simulated. It should be checked to what extent this improves the PAE of the peak PA.
Additionally, produced TL's should be examined more accurate on their electrical length. This should preferably be done on the PCB, such that the electrical length of the traces on the PCB is included in the test as well. Accurately knowing this parameter allows to produce TL's that get as close to an ideal $\lambda/4$ TL, to improve gain and efficiency.
Finally, the presence of leakage currents on the PCB should be investigated.
The most important problem to be studies is the origin of the peak PA efficiency and gain being lower than predicted. When considering possible causes, it is important to inspect whether the cause dominantly affects only the peak PA, as the performance of the main PA closely resembles the predicted performance.

7.2 Future Work

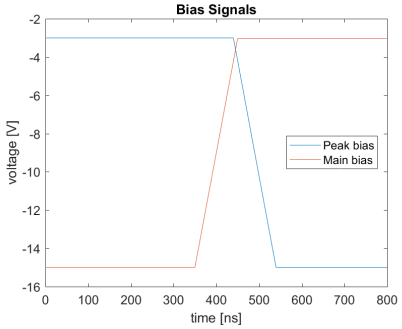
This section proposes ideas for future projects to improve and extend the functionality of the prototype realized in this project.

7.2.1 Time Domain Analysis

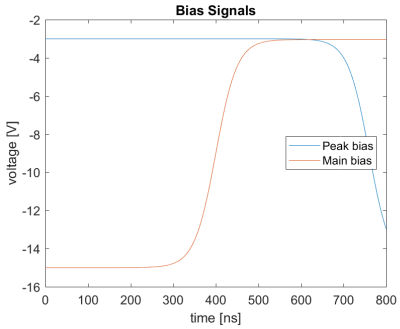
Because the switched-device PA must suffer from distortion originating from switching transients, an extensive time domain analysis is important. A start can be the investigation of anomalies arising from step inputs to both transistor branches. To minimize for transient distortion, DPD can be utilized (as recommended in Section 7.2.2), but custom switching 'profiles' can be used as well. These switching profiles are fed to the transistor gate to turn on/off the transistor.
Some first basic simulations showed some parameters influencing the transient distortion. These were the shape of the profile, the slope of the profile, and the overlap between the gate bias signals of the two branches (i.e. the time the other gate bias will start changing after the other has started). The switching profile shapes used to perform these first tests are shown in Fig. 7.1. Although the performed simulation are useful to investigate which parameters can be optimized, they were not sufficient to draw any useful conclusions on how to optimize the profiles.



(a) Step profile with 10 ns overlap



(b) Linear profile, 100 ns duration with 90 ns overlap



(c) Logistic profile, 200 ns duration with 190 ns overlap

Figure 7.1: Three different gate bias switching profiles

7.2.2 Minimizing the Distortion

A valuable extension of the current PA design would be the addition of (digital) pre-distortion. DPD adds (a little) distortion at the input of the PA. This distortion is tuned such that it cancels out the distortion introduced by the PA itself, thus linearizing the PA. A widely used DPD technique in Doherty PA's is vector-switched DPD [37], but there are also plenty techniques utilizing lookup-tables that are also known to perform well, for example [38].
DPD relaxes the linearity requirements of the PA hardware, as the PA can, using DPD, operate at bias levels that yield a stronger nonlinear transfer. Using DPD, this nonlinear transfer can be compensated for. The relaxation of this specification helps to achieve higher efficiencies (i.e. by operating at higher output powers, in compression).
Many Doherty PA's use DPD to increase their linearity. In Table 1.1 for example, [11], [16], [14] all use DPD. The switched-device PA can achieve a higher efficiency when it can operate at a higher output power at the same supply voltage level (even in compression). The nonlinear transfer at these high output power levels can be compensated for by using DPD. Therefore, implementing this technique would be very profitable for optimizing the performance of the switched-device PA.

7.2.3 Increasing Frequency and Bandwidth

In order to be usable for future wireless networks, such as 5G, the frequency of the system must be increased by a large amount. Current 4G network bands are allocated roughly between $500\,\mathrm{MHz}$ and $3500\,\mathrm{MHz}$. Future 5G bands on the other hand, are allocated between $28\,\mathrm{GHz}$ and $60\,\mathrm{GHz}$. The current implementation of the switched-device PA is not applicable for the current generation of wireless networks and therefore upscaling of the frequency of the PA is critical to develop of a switched-device PA suited for future wireless networks. As stated in Section 1.4, high frequency operation brings several other challenges with it, reduced gain being one of the most prominent. Additionally, because future communications demand for high data rates, this technique must be optimized for wide-bandwidth communications.

7.2.4 Multi-Switched-Device

Theoretically the concept of a two transistor switched device PA can be extended to multiple devices. The main advantage of the PA: high efficiency for a larger set of input powers than with one or two transistors. This can be extended to many devices, which may all be at peak efficiency at a specific input power. The average efficiency can be increased drastically. A disadvantage of such an implementation is the cost of the PA when many transistors are used. Also, when the amount of devices increase, the frequency of switches increases. This introduces additional switching distortion. Additionally, all transistors but one are off, which can be regarded as a waste of PCB space and components.
An improvement for multi-switched-device PAs could be to incorporate some envelope tracking on the drain supplies as well. The multiple devices give the drain envelope tracking more time to adjust to a different level, which increases the frequency up to

which envelope tracking is feasible.

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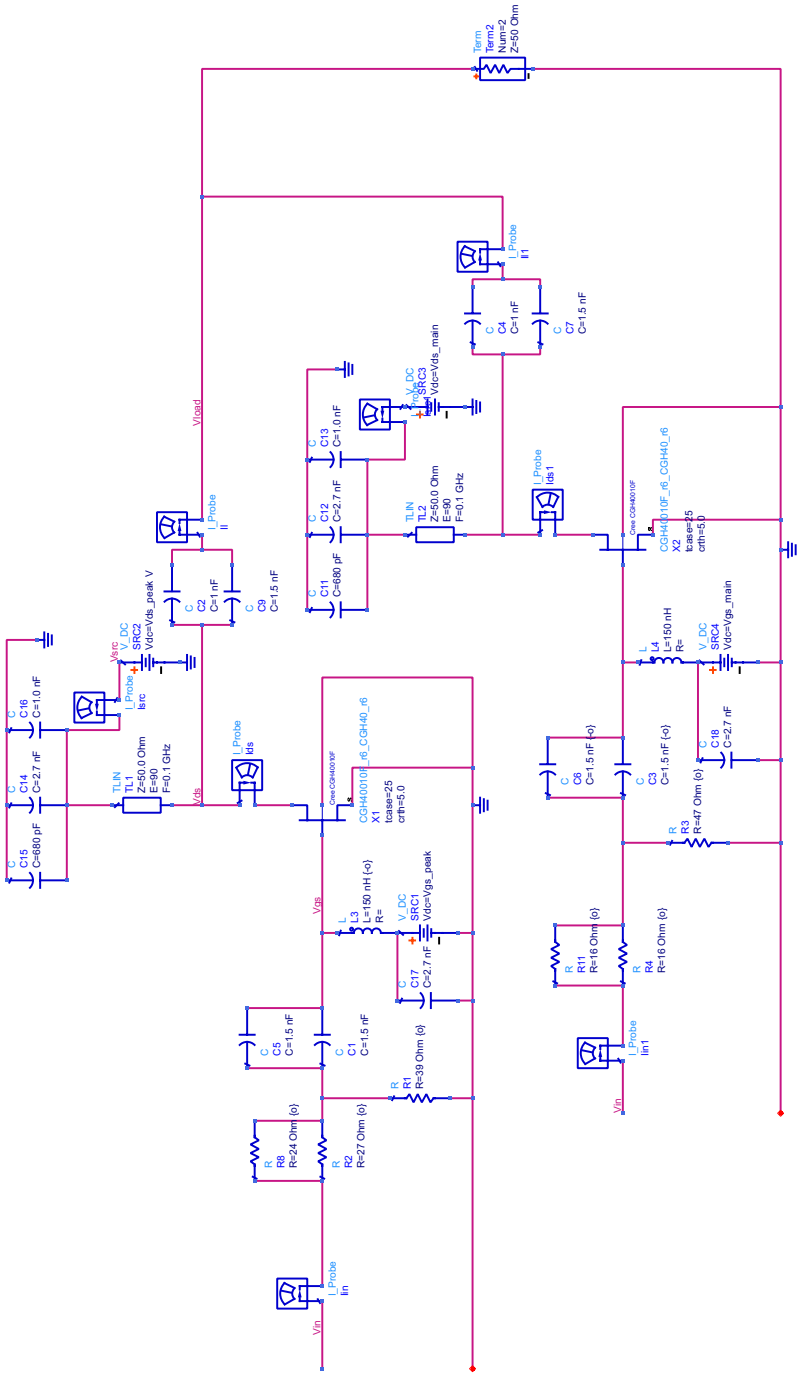
Appendices

A

Schematics



(a) Circuit designed to implement switched-device PA. parallel components used to approximate values determined by design process