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Circuit Design for Highly Sensitive RF-Powered Wireless Sensor Nodes

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Proefschrift

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CONTENTS

List of Abbreviations

ADC	Analog-to-Digital Converter
CP	Charge Pump
DLL	Delay Locked Loop
DSP	Digital Signal Processor
EIRP	Equivalent Isotropic Radiated Power
EM	Electromagnetic
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
GE	Global Efficiency
IC	Integrated Circuit
IoT	Internet of Things
ISM	Industrial, Scientific and Medical
LDO	Low-Dropout Regulator
LHP	Left-Half Plane
LNA	Low Noise Amplifier
LPF	Low Pass Filter
MEMS	Microelectromechanical System
MIM	Metal-insulator-metal

MPPT Maximum Power Point Tracking

NF Noise Figure

OOK On-Off Keying

PA Power Amplifier

PCE Power Conversion Efficiency

PLL Phase-Locked Loop

PM Phase Margin

PSRR Power Supply Rejection Ratio

PVT Process-Voltage-Temperature

RF Radio Frequency

RX Receiver

SNR Signal-to-Noise Ratio

TX Transmitter

UGBW Unity Gain Bandwidth

VCDL Voltage Controlled Delay Line

WSN Wireless Sensor Node

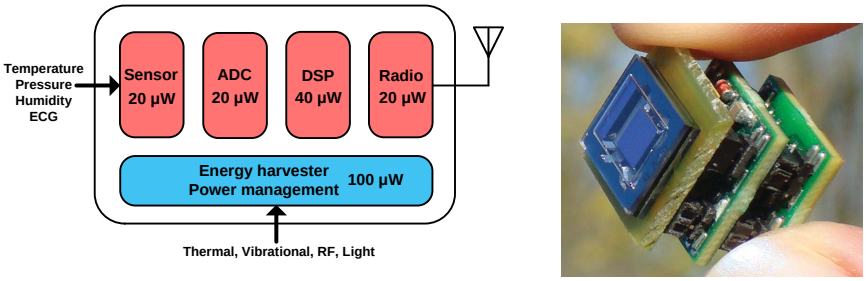
CHAPTER 1

INTRODUCTION

1.1 Energy Scavenged Wireless Sensor Nodes

The vision of realizing a network of wireless sensor nodes (WSNs) attracted much attention over the years as it can serve a wide range of applications [1]. These WSNs can sense, process and wirelessly transmit information within the network such as temperature, humidity, location and sensor identification. This eliminates the need for wiring each individual sensor and thus can considerably reduce installation costs when deploying a large number of sensors. The targeted average power consumption of a WSN has been estimated by various authors to be in the order of 10 to 100 μW [2–4], but strongly depends on the type of sensor and application. If this power is supplied by a battery, the maintenance costs can be relatively high compared to the initial purchase costs. For example, a network of 1500 WSNs with a battery lifetime of 4 years each will on average require one battery replacement per day. Although a network with 1500 connected devices may seem like a lot today, it is foreseen by various leading companies like NXP, Huawei, Qualcomm, Google, Cisco and Intel that the numbers of WSNs will exponentially grow over the coming years [5]. The market forecast of WSNs will be discussed further in Section 1.2.

Providing the required power by means of an energy harvester makes the WSN truly autonomous and eliminates the need for battery replacement. Figure 1.1(a) shows a schematic representation of a typical energy scavenged WSN. The energy is supplied by an energy harvester that converts energy from one domain (for example thermal, mechanical or electromagnetic) into the electrical domain. A power management circuit subsequently distributes the harvested energy to the various circuit blocks such as a sensor, an Analog-



(a) (b)

Figure 1.1: (a) Schematic representation of a typical energy scavenged WSN [2]. (b) A 1 cm^3 cube shaped WSN powered from a vibrational energy harvester [6].

to-Digital Converter (ADC), a Digital Signal Processor (DSP) and a radio. Figure 1.1(b) shows an example of a 1 cm^3 cube shaped WSN powered only from a vibrational energy harvester [6].
The majority of today's WSNs however are still battery powered due to the many technological challenges of designing energy scavenged WSNs. First of all, the dependency of the available power on the surrounding environment is an important limitation as will be discussed more in Chapter 2. Another key reason why energy scavenged WSNs are not yet widely commercialized into products is the unequal balance between the power consumption of the WSN and the power generated by the energy harvester. As a consequence, the WSN is required to be heavily duty cycled and therefore spends the majority of its time in standby and harvesting mode, which limits the functionality and performance considerably. Moreover, the non-zero standby current consumption further limits the performance and becomes an important design factor. Innovations in both the energy harvester as well as the WSN circuit implementation are therefore required.

1.2 Market Forecast

Accurately predicting the market value of WSNs over a ten year span is extremely difficult, if not impossible. Still, a range of reports and market forecasts have been published by independent research companies that all forecast substantial growth for the worldwide WSN market. This is a consequence of the progress made in affordable mass production and improved functionality which results in more applications and customer demands. Today's WSNs

unit prices are targeted at around $10-$15 and expected to decrease to $9.80 in 2019 and $0.40 in 2029 [7]. Eventually, WSNs will be small and cheap enough to for example be sprayed on floors, walls, buildings and roads.
IDTechEx forecasts that the total WSN market increases to $1.8 billion by 2024 [7] whereas BCC Research estimates the global WSN market to reach $4.3 billion by 2019 [8]. The wearable electronics market (medical, healthcare, fitness, wellness sector), according to IDTechEx, will grow from over $14 billion today to over $70 billion in 2024 [9] due to the development investments of big companies such as Adidas, Nike, Philips, Samsung and Apple.
These forecasts all indicate that there is a huge number of potential applications for WSNs in the near future. Some of the target applications used for this thesis will be discussed next.

1.3 Target Applications

There are various potential applications that have inspired many research institutions and industry companies to explore WSNs. Some examples are industrial manufacturing, healthcare monitoring, agriculture, logistics, electronic shelf labeling, structural maintenance and the military [2, 10].
A more broadly described application is the 'Internet of Things', which was first coined by Kevin Ashton in 1999 [11] and describes the wireless connectivity between devices, systems and services via the internet. This includes everything from cell phones to cars, lighting, coffee makers, law enforcement agencies and wearable/implantable devices. These 'things' can share their data via the internet and have the ability to for example learn, memorize, monitor and notify their users and therefore extend the connectivity beyond traditional (local) machine-to-machine (M2M) communication. The company Cao Gadgets LLC for example developed a wireless sensor tag that monitors and records motion events and notifies its user in real-time via a phone or tablet with internet access [12]. Cisco estimates that 50 billion devices and objects will be connected to the internet by 2020, meaning that each person world wide will on average have six connected devices [13]. These kind of applications usually require a WSN with a low update rate (often less than one hertz) and a limited wireless range of several meters [14], which may be realizable with duty cycled energy scavenged WSNs.
In the remainder of this section, the main target applications for this thesis are discussed in more detail, which are smart buildings and warehouse inventory management.

Figure 1.2: Illustration of various wireless sensor nodes in a smart building (courtesy of Eyes Above Security Systems Inc.).

Smart Buildings

The number of commercial buildings (i.e. office buildings, shopping malls and warehouses) in the United States alone sums up to approximately 5.6 million with a total of 8.11 billion m^2 of total floorspace [15]. The energy consumption of these buildings account for approximately 40% of total fossil fuel energy use [16]. With the rise of the world's most populous and fastest-growing countries such as China and India, it is expected that the energy consumed by these buildings will rise substantially in the near future. The impact on the environment is therefore high and long due to the building's long life cycle. This means that a huge opportunity exists to significantly reduce the net energy consumption. This is one of the driving forces behind so-called "smart buildings".

A smart building is a promising initiative and typical example of an IoT application. These intelligent systems require a large deployment of WSNs that for example monitor mechanical devices, temperature, light and the presence or absence of human beings as illustrated in Fig. 1.2. This allows to for example switch on the heating and lighting only in areas where they are needed. A network of WSNs consuming a few watt in total may thus enable total energy savings in the order of 10 to 30%, which can potentially lower the total

building power consumption by several kW [2]. The EnOcean Alliance for example develops energy harvesting wireless switches and sensors and claim 40% potential energy savings with 15% cost savings in new constructions and 70% cost savings in retrofits [17]. GreenPeak is another company that develops battery-powered radio chips for smart home applications like home security, lighting control and fire detection [18].
Besides reducing the net energy consumption, smart buildings can also provide intelligent monitoring of for example empty parking spaces, printers, waste bins, coffee machines and access control. Smart buildings thus have the potential to realize highly automated and efficient buildings with reduced energy consumption.

Warehouse Inventory Management

The average warehouse has a floor area of approximately 1000 m^2 [15]. In order to find a specific item in such a large area, an inventory list is required with the location of each item. Besides knowing the exact location, the food industry for example also benefits from knowing important conditions like the temperature, humidity and travel history of each item. Attaching a WSN with an unique identification number to each item thus allows the user to efficiently find remote items and view its conditions. In this scenario, it is important that the WSN costs need to be a fraction of the costs of the corresponding item and also relatively small in size.

1.4 Design Challenges and Objectives

The underlying objective of this thesis is to investigate, design and demonstrate an autonomous wireless sensor node powered solely by an energy harvester. One of the main challenges is to optimize the interface between the energy harvester and the WSN electronics for maximum sensitivity, efficiency and output power. This enables the possibility to use autonomous WSNs in new applications that previously where considered to be out of reach. The fundamental and practical limitations of various energy harvesters for the targeted application therefore first must be identified. The harvested energy should be utilized and distributed efficiently to each part of the WSN and thus requires efficient power management. Moreover, a suitable wireless communication system architecture is required that can be implemented with low power consumption and low cost. Hence, innovations at both the energy harvester as well as the power management and wireless communication system archi-

tecture are needed in order to improve the overall functionality and power efficiency, size, cost and reliability,

1.5 Organization of the Thesis

The work presented in this thesis is organized as follows.

In **Chapter 2** a general overview is given of micropower energy harvesting related to WSN applications. Four different energy harvesting approaches will be explored: vibrational, thermal, photovoltaic and RF. For each approach, the pros and cons are evaluated with respect to the potentially generated power, reliability, size and design challenges.

In **Chapter 3**, a system level description is given of an RF-powered transmitter to be used for WSN applications. Several design aspects, challenges and requirements are discussed in this chapter, thereby providing a framework for the following chapters.

Chapter 4 first treats some basic antenna and wave propagation fundamentals that lead to a general antenna equivalent circuit model. Subsequently, the co-design of antenna-electronics interfaces in the receiving mode is investigated, which includes optimum reception of wireless information and wireless power.

Chapter 5 uses the conclusions from the previous chapter and discusses the design procedure of a compact self-calibrating and highly sensitive RF energy harvester in 90 nm CMOS technology. First the design challenges and the proposed solution are discussed, followed by the circuit design of an RF rectifier. Then, the co-design with a custom designed antenna is presented and the experimental results in an anechoic chamber are discussed.

In **Chapter 6,** the theory and circuit design of a high efficient 2.4 GHz tuned switching power amplifier (PA) with <0 dBm output power is presented. An on-chip duty cycle calibration loop is proposed to enhance drain efficiency while the PA driver is optimized for high global efficiency. The experimental results of a 40 nm fabricated prototype are discussed and compared to the state-of-the-art.

Chapter 7 combines the work of the previous chapters and presents a compact RF-powered 2.4 GHz transmitter in 40 nm CMOS. First the circuit design of various blocks is described such as RF energy harvesting, power management, RF extraction, frequency divider, delay locked loop and a frequency multiplier. Subsequently, the experimental results of the prototype TX are extensively reported.

Finally, conclusions and recommendations for future research are presented in **Chapter 8**.

CHAPTER 2

MICROPOWER ENERGY HARVESTING FOR WSNS

People have been using nature's energy sources for hundreds of years by constructing various kinds of watermills and windmills. Today, large-scale wind turbines and solar power plants are developed to meet the 20% renewable energy target by the year 2020 set by the European Union [19].
The driving force for *micropower* energy harvesting is the desire to realize maintenance-free autonomous WSNs. In this chapter, first an overview is given of micropower energy harvesting in general related to WSN applications. Subsequently, four different energy harvesting approaches will be discussed: vibrational, thermal, photovoltaic and RF. For each approach, the pros and cons are evaluated with respect to potentially generated power, reliability, size and design challenges.

2.1 The Power Balance

The Achilles' Heel of today's energy scavenged WSNs is the unequal balance between the power *consumption* of the WSN and the power *generated* by the energy harvester. This is shown graphically in Fig. 2.1. On one side of the scale, the power consumption of integrated circuits decreases over time with more advanced CMOS technologies and circuit designs. The energy harvester on the other side of the scale also benefits from these improvements and thus becomes more efficient in converting energy from other domains into electrical energy. Of course, these curves are highly speculative as they depend on many factors such as sensor functionality, type of harvester, the available power of the energy source and the application.

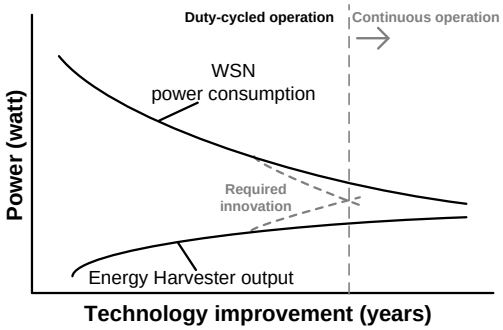


Figure 2.1: General power balance between energy harvester output and power consumption of a WSN.

It may be argued that the intersection of these two curves may be inevitable due to technology improvements. This however, may not be the case for a number of reasons. Firstly, the difference between the required power and the available power to the harvester may simply be too large for a specific application. A second reason is that the scaling of CMOS devices may not be beneficial for the performance of analog circuits. With a lower supply voltage, the performances at some point are limited by the circuit noise. If the signal-to-noise ratio and dynamic range are required to remain the same, then lowering the supply voltage can actually *increase* the power consumption. Hence, innovations at both the energy harvester and the WSN are needed in order to equalize the power balance. Once this can be realized, it will create the possibility to use autonomous WSNs in new applications that previously where out of reach.

At the point where these curves intersect, the energy harvester provides enough power to continuously operate the WSN. For the majority of today's WSN applications, this point has not been reached yet, meaning that the WSN needs to be duty-cycled. With duty-cycled operation, the energy harvester output first is locally stored in a battery or (super)capacitor. When enough energy is accumulated over time, the WSN can be powered for a short period. This way, a mW power budget can be realized when harvesting at μW power levels.

A typical power profile of a duty-cycled energy scavenged WSN is sketched in Fig. 2.2. The peak power consumption during transmitting and receiving typically is significantly higher than the energy harvester output, but is only required for a short time. Between reception and transmission, the

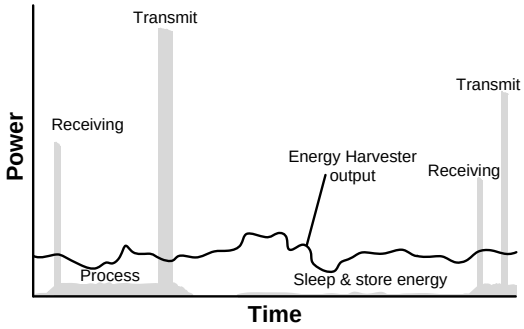


Figure 2.2: Typical power profile of a duty-cycle energy scavenged WSN.

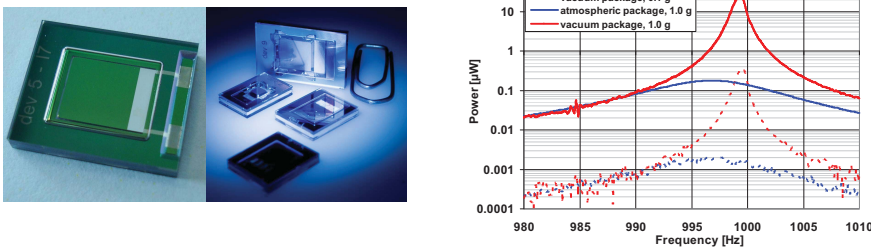
WSN measures and processes the sensor input. For the rest of the time, it is in energy harvesting mode. Low-power and adaptive power management is thus required for optimum performance.

The power generated by the energy harvester can fluctuate strongly over time and depends on the type of energy harvester and its environment. To determine the potentially generated output power, first different types of energy harvesters need to be investigated and compared on aspects such as output power, reliability, size, costs and possible applications. The energy harvesters that will be briefly discussed in the following sections are vibrational, thermal, photovoltaic and RF energy harvesters.

2.2 Vibrational Energy Harvesting

Vibrational energy harvesters are well studied in the energy harvesting literature. Basically, there are three ways of converting vibrations into energy [20]:

- Electrostatic: A pre-charged capacitor with two opposing metal structures where one metal plate is displaced due to an external force. This external force changes the capacitance and voltage (assuming constant charge mode) and converts the mechanical motion in electrical energy.
- Piezoelectric: Vibration or movement causes the deformation of a piezoelectric material, thereby generating a charge.
- Electromagnetic: The displacement of a magnetic mass with respect to a coil produces a change in the magnetic flux. The change in flux generates a voltage.



(a) (b)

Figure 2.3: (a) Piezoelectric MEMS energy harvester and (b) measured generated power for an atmospheric and vacuum packaged device with acceleration of 0.1 g and 1.0 g (picture courtesy of Imec/Holst centre [6]).

Figure 2.3(a) shows a piezoelectric energy harvester that utilizes a vacuum-packaged microelectromechanical system (MEMS) to reduce the air damping, thereby improving the power output at all frequencies. The output power depends on the acceleration and the frequency of the vibration. Typically, vibrational energy harvesters are most sensitive to vibrations that are close to their natural frequency. The harvester thus needs to be designed for a specific frequency range that corresponds to the vibrations found in the targeted application.

Typical usage for vibrational energy harvesters are applications with moving parts such as machines, engines and other industrial devices. An intelligent car tire with built-in pressure sensors can for example be powered by means of a vibrational energy harvester. Each time when the tire with the embedded harvester contacts the road, a high amplitude shock of up to a few hundred g is generated for velocities above 80 km/h [21]. Each shock will cause the harvester to ring down at its natural resonance frequency and convert mechanical energy into electrical energy. Peak output powers of 489 μW have been reported with an average output power of 42 μW at 70km/h [21]. This power allows the wireless pressure sensor to communicate with the vehicle computer and indicate the driver when the tires are under-inflated. This not only prevents unneeded fuel pollution, but also makes the vehicle safer to drive.

Another well studied target application is energy harvesting from human motion to power wearable electronics. When running at 10 km/h, accelerations around 3 g with peaks up to 7 g can be expected [22]. This large potential source of energy has been used to develop energy harvesting shoes [23–25]

and backpacks [26] which can provide an average output power between 0.4-2 mW while walking at a frequency of roughly 1 Hz to 10 Hz. Although this output power is larger than that of the harvester example shown in Fig. 2.3(b), this energy harvester is also significantly larger in size (~200 cm^2), which may be too big for many applications.

The open-circuit AC voltage of vibrational harvesters is relatively high compared to other harvesters and varies roughly between 0.8 and 10 V at a frequency of a few kHz at most. An AC/DC converter with these specifications can for example be implemented with active diodes combined with a DC-DC boost converter, resulting in very high power conversion efficiencies above 90% [27].

A major disadvantage of vibrational energy harvesters is that the number of applications that provide a reliable and constant source of energy near the resonant frequency is limited as the vibrations are often unpredictable. A more complete overview of energy harvesting from human and machine motions can be found in [28].

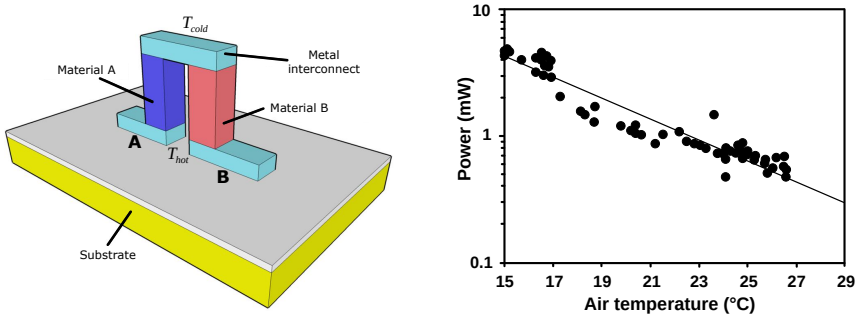
2.3 Thermal Energy Harvesting

Thermal energy harvesters are based on the Seebeck effect. When a temperature difference is established between two sides of dissimilar materials as illustrated in Fig. 2.4(a), a voltage develops between point A and B as described by

$$V_{AB} = -(\alpha_A - \alpha_B)(T_{hot} - T_{cold}) \tag{2.1}$$

where V_{AB} is the potential difference [V], α_A and α_B are the Seebeck coefficients of materials A and B respectively [V/K] and $(T_{hot} - T_{cold})$ is the temperature difference between the hot and the cold source [K] [20]. The output voltage of a single thermocouple is very small as the Seebeck coefficient is only in the order of 0.2 mV/K for semiconductor material. Either a very large temperature difference is thus required, or a large number of thermocouples (called a thermopile) connected thermally in parallel and electrically in series is needed.

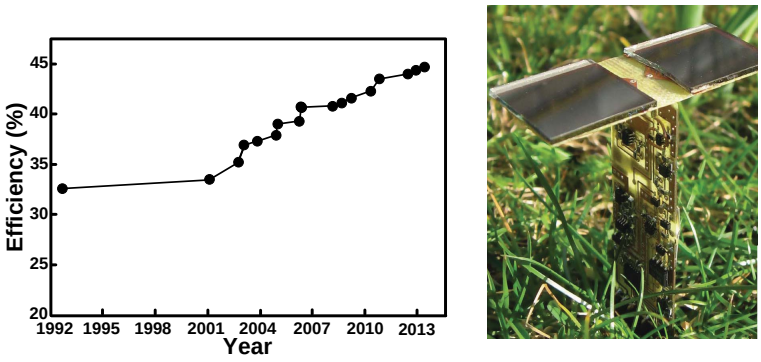
A recent development in the area of wearable energy harvesters is a thermoelectric shirt with 16 thermopiles integrated between two textile layers of the shirt [29]. A temperature difference is created by placing the hot plate in contact with the skin under the textile, which is at a temperature of approximately 37 $^{\circ}C$. The cold plate is placed about 4 mm from the cotton layer such that it is cooled by ambient air flow. When combining the harvested power of all



(a) (b)

Figure 2.4: (a) Single thermocouple and (b) the measured generated power of a human subject wearing a thermoelectric shirt with multiple thermocouples (picture courtesy of Imec/Holst centre [29]).

16 thermopiles, an average output power between 0.5–5 mW was measured for ambient air temperatures between 27 and 15 $^{\circ}C$ as shown in Figure 2.4(b). Smaller sized thermal harvesters have also been mounted in a wrist-watch and generate an average power of about 250 μW at 22 $^{\circ}C$ air temperature [30]. Another field of interest is the aerospace industry as aircrafts are exposed to large thermal gradients. Depending on the location of the harvester, peak generated power levels between 5-35 mW may be feasible [31].
The advantage of thermal energy harvesters is that there are no moving parts in contrast to the vibrational harvester, which allows reliable and long continuous operation. But unfortunately, thermal harvesters are inefficient for low temperature differences and require a large number of thermocouples to generate a sufficiently high voltage, making them expensive to fabricate. Alternatively, a smaller amount of thermocouples may be used in combination with a DC-DC converter that boosts the generated voltage to useful levels. The challenge then is to design a highly efficient converter that can operate at very low input voltages and is powered by the harvested energy itself. This has been the subject of many studies on inductive boost converters [32, 33] and charge pumps [34, 35]. The reported efficiencies are ranging between 46-92%, depending on the input voltage, and can be used for input voltages as low as 20 mV [36].



(a) (b)

Figure 2.5: (a) Efficiency records of photovoltaic cells under solar spectra [38] and (b) a prototype of a solar powered WSN (picture courtesy of Mina Danesh [39]).

2.4 Photovoltaic Energy Harvesting

When a photon is absorbed by a photovoltaic cell, an electron-hole pair is generated provided that the incident photon has an energy greater than that of the material's bandgap. The presence of the internal electric field inside the p-n junction of the solar cell facilitates the separation of the photon generated electron-hole pairs and forces an electric current to flow through an external load. This process however is not 100% efficient as the sunlight spectrum consists of photons with different energy levels. Photons with energy less than the material's bandgap are not able to generate an electron-hole pair and thus do not contribute to the output current. A photon with more energy than the required bandgap energy loses its extra energy in the form of heat (unless the photon has exactly enough energy to create two or more electron-hole pairs). To prevent this loss mechanism, multi-junction cells with multiple bandgaps have been proposed over the years to absorb a broader range of photon energy levels. The record conversion efficiency of the last 20 years is illustrated in Fig. 2.5(a), showing an increased performance towards the current record efficiency of 44.7% [37]. Commercially (and cheaper) available photovoltaic cells however typically have a lower efficiency of about 20% or less.

For outdoor applications, the power density of solar radiation on the earth's surface is about 100 mW/cm^2 at noon on a clear day and roughly 30 mW/cm^2 or less for a cloudy day [20, 40]. Thus, a harvested power of about 6-20

mW/cm^2 can be expected when using commercially available photovoltaic cells. For indoor applications however, the situation is much different since the light intensity of artificial lighting conditions found in office buildings are typically below 100 μW/cm^2 [41]. This limits the harvested power to about 10 μW/cm^2 as a lower light intensity also corresponds to a lower conversion efficiency.

The challenge for small-scale solar harvesting is to generate sufficient power with limited area. Figure 2.5(b) shows an example of a WSN powered by a flexible photovoltaic cell that generates 20 mW under ideal outside conditions [40]. To minimize the WSN size, this prototype uses an antenna that is integrated on the back of the photovoltaic cell together with a radio transmitter, power management and a super capacitor. A maximum power point tracking (MPPT) circuit is required as a photovoltaic cell can operate over a wide range of voltages and currents for irregular light exposures [42].
In 2011, the university of Michigan presented a cubic-millimiter sized energy-autonomous wireless intraocular pressure monitor that is powered by a 0.07 mm^2 integrated solar cell [43]. Due to the extremely small size, the solar cell can only generate 80.6 nW of power. In this case, the circuit power consumption and its leakage current becomes very important to the overall performance of the WSN.
The disadvantage of photovoltaic energy harvesting is that the available power of the photovoltaic energy harvester is strongly dependent on the application and location. Solar energy harvesting is a very good candidate for outdoor applications with direct sunlight like greenhouses and farms, but may fall short compared to other type of energy harvesters for indoor applications.

2.5 RF Energy Harvesting

The transfer of wireless energy by means of electromagnetic waves can be categorized into non-radiative and radiative energy transfer. Near-field inductive coupling belongs to the non-radiative category and is based on two magnetically coupled coils in resonance. This energy transfer method has been extensively studied for wireless powering and is widely used for example to power implantable devices [44, 45]. For near-field coupling, the coils need to be in close proximity, typically within the same dimension as the coil. The coil dimension in turn is determined by the operating frequency, which often is in the order of a few MHz. Recently, Stanford University showed that significantly higher efficiencies can be obtained in the electromagnetic mid-field (a region between the near-field and far-field) when for example wirelessly

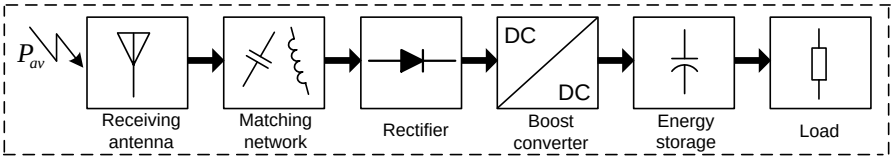


Figure 2.6: General receiving far-field RF energy harvesting system with power management [48].

transferring power to implantable devices [46]. Although this operating region extends the wireless range compared to near-field coupling, it is limited to about 3-10 times the coil radius [47], which may still be too short for WSN applications.
To further increase the wireless range, far-field power transfer needs to be used. Unlike inductively coupled systems, far-field systems radiate and receive in all directions when assuming an isotropic radiator and receiver. Although this can be conceived as a disadvantage as power is 'lost' in directions other than the desired one, it can be turned into an advantage for applications that require multiple targets spread out over a large area that need to be powered.

A far-field RF energy harvesting system generally consists of a receiving antenna, matching network, rectifier and power management (DC-DC converter) as illustrated in Fig. 2.6. The antenna converts the electromagnetic signals to electrical voltages and currents, which are related to the available power P_{av}, antenna impedance and the rectifier input impedance. The available power can originate from ambient or dedicated RF energy sources, which are briefly discussed below.

Ambient RF Energy

Ambient RF energy sources such as TV, GSM and WLAN base stations are omnipresent in most of today's societies. It thus sounds very promising to 're-use' these signals to realize truly autonomous wireless sensors. In [49], an experiment was conducted to measure the received signal strength and probability in urban and suburban areas between 800 and 900 MHz. In an urban area, the received signal strength was most likely to be around -20 to -40 dBm with a peak probability of 31% around -33 dBm. In a less dense populated environment, this peak was around -37dBm with a probability of 27%. Similar results have been found in [50], where the ambient RF power density at a distance between 25-100 meters from a 900 MHz GSM base station was

found to be between 0.01-0.1 μW/cm^2 (around -30 to -20 dBm).

Whether or not these power levels are high enough to be used for RF energy harvesting, can be determined by calculating the rectifier startup power threshold. As practical components used for rectification need a minimum voltage in order to conduct current, the RF energy harvester is limited by the rectifier startup threshold voltage[1] $V_{rec,threshold}$. The startup power threshold $P_{startup}$ then is given by

$$P_{startup} = \frac{V_{rec,threshold}^2}{2\eta_A R_{rec,p}} \tag{2.2}$$

where η_A is the receiving antenna radiation efficiency and $R_{rec,p}$ is the equivalent parallel input resistance of the rectifier [51]. For a single Schottky rectifier implementation with $R_{rec,p}$ =1 kΩ, $V_{rec,threshold} = 0.3$ V and $\eta_A = 0.8$, the minimum required power for rectification equals 56.25 μW (-12.5 dBm). The power conversion efficiency will likely be low around this startup threshold as the diode is just barely forward biased. Typically, the rectifier becomes more efficient for larger input power levels. If $V_{rec,threshold}$ for example can be reduced to 0.1V, the startup threshold is lowered to -22 dBm, giving a sensitivity improvement of 9.5 dB. Harvesting from ambient RF energy sources thus requires a very sensitive rectifier. In general, ambient RF power levels are considered to be too low to be used for RF energy harvesting as they are often around or below the power startup threshold of the rectifier.

There are however some scenarios with higher ambient RF power levels such as in high-density locations like public transport and festivals [52]. Another approach to is to simultaneously harvest from multiple frequency bands as demonstrated in [53].

Dedicated RF Energy

Alternatively, a more powerful and reliable *dedicated* RF energy source can be used in the vicinity of the devices that need to be powered wirelessly. The available power[2] P_{av} to the receiving antenna in free space using a perfectly aligned and conjugate matched antenna is described by the Friis transmission equation

$$P_{av} = \left(\frac{\lambda}{4\pi d}\right)^2 G_{RX} P_{EIRP} \tag{2.3}$$

[1] The startup threshold voltage does not necessarily equal the diode or transistor threshold voltage, it is also a function of the number of rectifying stages and the rectifier circuit topology.

[2] The concept of available power and other antenna fundamentals will be discussed in more detail in Chapter 4.

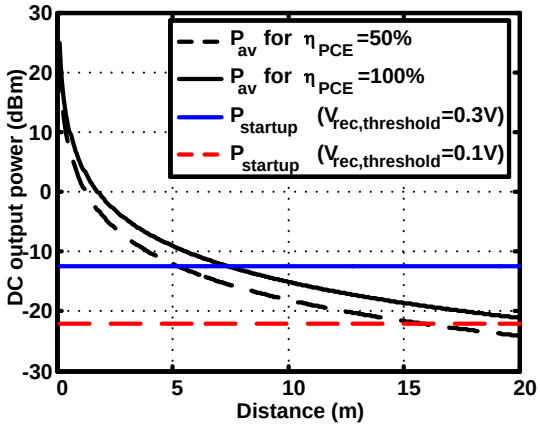


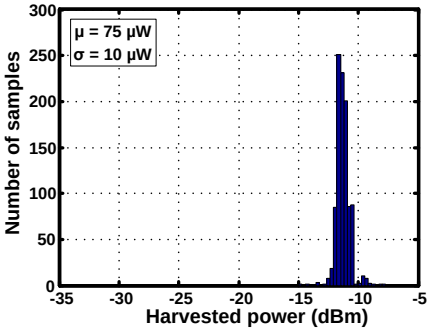
Figure 2.7: Calculated DC output power vs. distance with startup power threshold limit for P_{EIRP}=3.28 W, λ=0.345 m and G_{RX}=1.25.

where P_{EIRP} is defined as the Equivalent Isotropic Radiated Power (EIRP) of the RF source, G_{RX} is the receiving antenna gain of the RF harvester, d is the distance between the RF source and the receiving antenna and λ is the wavelength [54]. The maximum available power at a given distance from the RF source is thus limited by the frequency, antenna gain and the maximum allowed P_{EIRP}, which is defined by international regulations. The license-free Industrial, Scientific and Medical (ISM) frequency bands are often used for dedicated RF harvesting applications since they allow for a high P_{EIRP} with acceptable antenna sizes. The European Radio communications Commission (ERC) limits the maximum P_{EIRP} at 868 MHz to 3.28 W and to 4 W at 2.45 GHz [55]. The U.S. Federal Communications Commission (FCC) limits both the power levels at the 915 MHz and 2.45 GHz bands to 4 W EIRP [56].
As a practical example, Fig. 2.7 shows the harvested DC output power versus distance for the case of a rectifier power conversion efficiency η_{PCE} of 50% and 100%. A line-of-sight scenario is assumed with P_{EIRP}=3.28 W, λ=0.345 m (868 MHz) and G_{RX}=1.25. For η_{PCE}=50%, a DC output power of about 61.8 μW can be achieved at a distance of 5 meter and 6.87 μW at 15 meter. When calculating the power transfer efficiency to a single WSN at 5 meter, the efficiency is only 0.0019% as the power of the RF source is also radiated in other directions and does not contribute to the received power of the WSN. This approach is thus only cost efficient if a large multiple of WSNs is employed that are all powered by the same RF source. However, if an intelligent RF source is used that tracks the sensor node and steers a highly

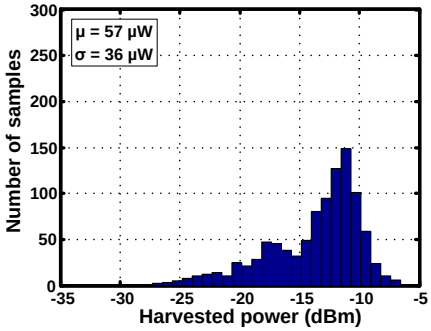
directive beam towards the WSN when it requests charging, it is possible to improve the overal system efficiency.
The maximum wireless range however is limited by the startup power threshold as indicated by the horizontal lines in Fig. 2.7. In this example, a reduction in rectifier threshold voltage from 0.3V to 0.1V increases the maximum achievable distance from 5 meters to 15.7 meters for η_{PCE}=50%. This indicates the importance of minimizing $P_{startup}$ in case the regulations do not allow to increase the radiated power any further.

Distribution of RF Harvested Power in an Office Environment

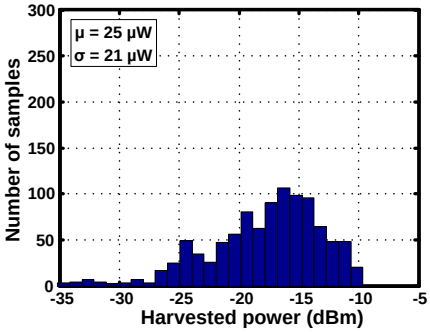
Even with a dedicated RF source, the harvested power can vary significantly in a realistic environment due to the many unknown variables in the propagation channel. To get a better understanding of the distribution of RF harvested power in various scenarios, an experiment was conducted.
Fig. 2.8 shows the measured harvested RF power in an office room (~24 m^2) at 915 MHz for three different scenarios using a Powercast P2110-EVAL-02 RF energy harvester [57] with 1 dBi receiving antenna gain at 3.5 meter distance from a single 3 W EIRP dedicated RF source. In each scenario, the harvested RF power is measured using 1000 samples taken over a period of 30 minutes.
The first figure shows a static office environment with line-of-sight and aligned antenna. The mean harvested power (μ) is 75 μW with a standard deviation (σ) of 10 μW. The scenario shown in Fig. 2.8(b) shows the harvested power in case of a line-of-sight and random angular and lateral misaligned antenna. Here, a mean value of 57 μW was measured with a standard deviation of 36 μW. The last scenario is non-line-of-sight with random misaligned antennas in a highly dynamic office room with people walking in between the transmitter and RF harvester. The mean harvested power in this case was 25 μW with a standard deviation of 21 μW.
As expected, the average harvested power not only decreases in a more dynamic scenario, but also the standard deviation becomes relatively larger. Although these measurements strongly depend on the environment and the RF energy harvester being used, they demonstrate that the RF energy harvester needs to be designed for high sensitivity when used in a dynamic environment. These fluctuations therefore need to be considered at system level and again demonstrate the need for an intelligent RF source.



(a) Line-of-sight and aligned antenna.



(b) Line-of-sight random angular and lateral misaligned antenna.



(c) Non-line-of-sight with random angular and lateral misaligned antenna.

Figure 2.8: Measured distribution of RF harvested power in an office room (~24 m^2) for different scenarios taken over a 30 minutes period.

Since the open-circuit AC antenna voltage of RF energy harvesters usually is relatively small (<0.5V) compared to vibrational energy harvesters, it poses a challenge for the rectifier design. Also the relatively high operating frequency in the ISM bands (GHz range) does not allow for a low-power active diode rectifier implementation. A complete and thorough study of the antenna-rectifier interface is thus required in order to optimize the overall system performance.

The advantage of RF energy harvesting is that it can be used in applications where vibrations, light and temperature gradients are not always available or unpredictable such as in warehouses and smart buildings. Moreover, besides delivering energy, the RF source can also serve as a communication hub and provide a system clock by modulating the RF carrier wave [58]. This unique

advantage can greatly reduce the radio power consumption of the WSN as it eliminates an on-chip signal generator.

2.6 Comparison

A choice needs to be made which harvester is most suited for the target application (warehouse and smart buildings). To compare the four different energy harvesters, an overview is given in Table 2.1. The potential harvested power is compared per cm^2, which gives a fair and good indication of the desired harvested power and required size.
When comparing only on harvested power density, it follows that outdoor photovoltaic and thermal industrial harvesting outperform other harvesters. However, these energy sources are likely not to be available for the target application. Also energy from human vibrations and ambient RF energy is considered not to be a reliable and useful source for the target application. This leaves indoor photovoltaic, thermal and dedicated RF energy harvesting as potential candidates, which have comparable power density levels. Dedicated RF energy harvesting however can serve a large variety of applications, even in thermally constant, dark and static environments. Moreover, additional possibilities such as using the RF energy source as a data and clock distribution hub greatly reduces the power consumption of the WSN. Also the fabrication costs of an RF antenna are much lower than that of a photovoltaic cell. With the advances in flexible electronics, the WSN and antenna can even be integrated on the same flexible substrate. With this reasoning, it is decided that RF energy harvesting is the most suited energy harvester for the target application.

Table 2.1: Overview of potentially available and harvested power of various energy harvesters (based on data from [20]).

	Power Source	**Harvested Power Density**
Vibrational		
Human	0.5 m at 1 Hz 1 m/s^2 at 50 Hz	4 μW/cm^2
Industrial	1 m at 5Hz 10 m/s^2 at 1 kHz	100 μW/cm^2
Photovoltaic		
Indoor	<0.1 mW/cm^2	<10 μW/cm^2
Outdoor	30-100 mW/cm^2	6-10 mW/cm^2
Thermal Energy		
Human	20 mW/cm^2	30 μW/cm^2
Industrial	100 mW/cm^2	1-10 mW/cm^2
RF		
Ambient	0.01-0.1 μW/cm^2	<0.03 μW/cm^2
Dedicated	0.5-50 μW/cm^2	0.15-20 μW/cm^2

2.7 Conclusions

An overview has been given of micropower energy harvesting for autonomous WSN applications. The unequal balance between the power consumption of the WSN and the power generated by the energy harvester requires most autonomous WSNs to be duty-cycled. When enough energy is harvested over time, the WSN can be powered for a short period. This way, a mW power budget can be realized when harvesting at μW power levels.
Four different energy harvesting approaches where discussed: vibrational, thermal, photovoltaic and RF. Outdoor photovoltaic and thermal industrial energy harvesters are able to generate more power than other harvesters, but do not match the target application (warehouse and smart buildings). Also the energy from ambient RF, human vibrations and human thermal sources are considered to be too low, not reliable and not available for the target application.
Dedicated RF energy harvesting however can offer a large variety of applications, even in thermally constant, dark and static environments. Moreover, additional possibilities such as using the RF energy source as a data and clock distribution hub greatly reduces the power consumption of the WSN. Also the fabrication costs of an RF antenna is relatively low. The design challenge for RF energy harvesting is the relatively small (<0.5V) open-circuit voltage of the receiving antenna at relatively high operating frequency in the ISM

bands (GHz range). Especially for low input power levels (i.e., a long wireless range), a very sensitive rectifier is required. A complete and thorough study of the antenna-rectifier interface is thus required in order to optimize the overall system performance.

The conclusions drawn in this chapter are used as input for the following chapter, in which a system level description is given and several design aspects are discussed for an RF-powered transmitter.

CHAPTER 3

SYSTEM LEVEL DESIGN

In the previous chapter it was concluded that RF-powered WSNs have the distinct advantage over other energy harvesting systems that they can operate wirelessly in a large variety of applications, even in thermally constant, dark and static environments. This chapter discusses several system aspects, challenges and requirements for the design of RF-powered WSNs.

3.1 System Level Description

The absence of a stable reference frequency in low cost and power efficient WSNs makes it very challenging to implement a low power wireless communication architecture. Passive RFID backscattering therefore has been a popular choice because of its simplicity and low power consumption [59, 60]. By simply altering the input impedance of the RFID tag, the incoming RF wave is backscattered from the RFID antenna with different amplitude and phase and thus can be used to encode information. Since this process re-uses the energy from the incoming RF wave for wireless transmission, it is not required to *generate* an RF carrier and thus can be implemented with minimum power consumption. The functionality and operating range however are limited and the system can suffer from reader self-jamming as the backscattered signal is at the same frequency as the signal transmitted by the RFID reader [61]. Other solutions have been proposed that utilize a local oscillator for RF carrier generation [62]. This not only requires significant power, but also is very challenging to realize with sufficient accuracy over process-voltage-temperature (PVT) variations.
Surface acoustic wave (SAW) and film bulk acoustic resonators (FBARs) can provide a high Q and extremely accurate reference frequency and therefore

have been used to generate RF carriers in low power transmitters [63, 64]. These resonators however are relatively bulky and often cannot be integrated on chip, thereby increasing the fabrication costs of the WSN even further.
In [65] a crystal-less RF-powered transceiver has been proposed. By using the 915 MHz received carrier frequency as reference frequency in a Phase-Locked Loop (PLL), an accurate 2.4 GHz signal could be realized to be used for wireless data transmission. These frequencies are conveniently located in the license-free Industrial, Scientific and Medical (ISM) bands [56] and thus can be used for frequency synthesis in order to realize a compact, frequency stable and power efficient solution. A similar architecture has been proposed in [66], where the received signal is fed into an injection-locked frequency multiplier to generate a 402 MHz carrier. Another architecture in [67] has been proposed for an RF-powered RFID tag with on-chip antennas. In this architecture, a 5.8 GHz dedicated RF source supplies both energy and a frequency reference that is used as clock for 3.1-10.6 GHz impulse radio ultra-wideband (IR-UWB) transmission. Although the sensitivity of the tag itself is -14.22 dBm, the on-chip antennas greatly limit the wireless operating range to 7 cm.

Both the 902-928 MHz as the 2.405-2.47 GHz ISM bands are well established and widely used for various wireless communication standards. The combination of the two frequency bands therefore can be used in many RF-powered WSN applications. Since the limiting factor for maximum wireless range is likely to be the RF energy harvester and not the transmitter (TX), it is advantageous to use the lower 915 MHz ISM band for RF energy harvesting and the 2.4 GHz ISM band for wireless transmission. This is because antennas operating at lower frequencies have a larger effective area and therefore are more effective to capture energy from the incoming wave [1]. This translates into a longer wireless range but also requires a larger physical antenna area. The Effective Isotropic Radiated Power (EIRP) in the 915 MHz ISM band is limited to 4 watt (+36 dBm) by the Federal Communications Commission (FCC) [56], which enables a long wireless range.

A system level description of the proposed RF-powered transmitter is illustrated in Fig. 3.1. The system consists of an RF energy harvester, power management unit, frequency synthesizer and an RF power amplifier. In this work, a dedicated RF source is assumed within the vicinity of the WSN that provides strong and reliable power in the 902-928 MHz ISM band. An RF energy harvester converts the captured electromagnetic (EM) energy by the

[1] The concept of effective area and other antenna fundamentals will be discussed in more detail in Chapter 4.

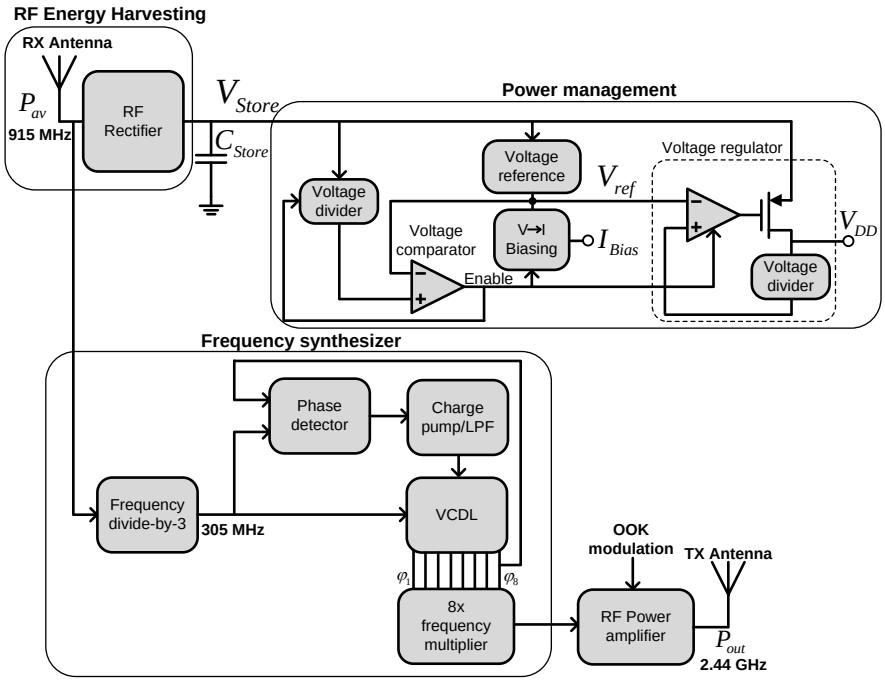


Figure 3.1: Proposed RF-powered DLL-based transmitter.

antenna into electrical DC power. The harvested energy is first locally stored in an external capacitor until enough energy is accumulated to initiate wireless data transmission. The challenges and requirements for each block will be briefly discussed in the following sections.

3.2 RF Energy Harvesting

Apart from being designed for efficient power transfer, the RF energy harvester needs to be designed for superior sensitivity (i.e., minimize the required available power at the antenna to activate the TX). This leads to an increased area and distance that can be covered by the dedicated RF source.

Some other design challenges for RF energy harvesters have already been briefly introduced in Section 2.5 and will be extensively discussed in Chapters 4 and 5.

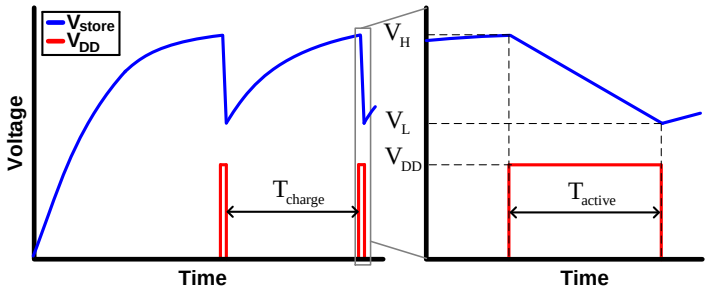


Figure 3.2: Power management time-domain waveforms. On the left an impression of the storage capacitor voltage and on the right a zoomed in figure illustrating the active period during wireless transmission.

3.3 Power Management

The power management unit illustrated in Fig. 3.1 consist of a voltage reference, voltage comparator, V-I converter and a voltage regulator. The voltage waveform across the storage capacitor C_{store} and supply voltage V_{DD} are sketched in Fig. 3.2 to illustrate the power management functionality. Here, V_L and V_H are defined as the low and high voltages that together with C_{store} determine the amount of stored energy available to the system.
When the system is in harvesting mode, the rectifier charges C_{store} to V_H while only the voltage reference and voltage comparator are enabled. When $V_{store} \geq V_H$, the voltage comparator enables the voltage regulator and V-I converter which provide a stable V_{DD} and reference current I_{ref} for the various circuit blocks while C_{store} is discharged from V_H to V_L due to the current drawn by the transmitter. The active time T_{active} is determined by C_{store}, V_H, V_L, V_{DD} and the total current drawn by the system. Once $V_{store} \leq V_L$, the comparator disables the voltage regulator and the system returns to harvesting mode. The charging time T_{charge} is determined by the available RF power at the antenna, the RF rectifier efficiency, the storage capacitor and the power consumption of the voltage reference and comparator. To determine the system design variables, we first consider the voltage regulator efficiency of this system.

The energy efficiency of an ideal linear voltage regulator (neglecting its bias current) with a constant input and output voltage is simply given by $\eta = V_{DD}/V_H$. However, in this system the input voltage of the voltage regulator decreases linearly with time when assuming a constant current sink I_{load} as load. The energy at the input of the voltage regulator for $V_{DD} \leq V_L \leq V_H$ is thus given by

$$E_{in} = \int_{t}^{t+T_{active}} I_{load} V_{store} dt \tag{3.1}$$

$$= I_{load} T_{Active} \frac{V_H + V_L}{2} \tag{3.2}$$

The energy delivered to the regulator load is simply given by

$$E_{out} = I_{load} V_{DD} T_{active} \tag{3.3}$$

The voltage regulator energy efficiency $\eta_{regulator} = E_{out}/E_{in}$ then can be expressed as

$$\eta_{regulator} = \frac{2V_{DD}}{V_H + V_L} \tag{3.4}$$

$$= \frac{V_{DD}}{V_H} \frac{2}{1 + \frac{V_L}{V_H}} \tag{3.5}$$

Note that the second term in (3.5) indicates the relative improvement in efficiency compared to a voltage regulator with constant input and output voltage. To obtain a high efficiency, the differences between V_H, V_L, and V_{DD} need to be as small as possible. The required values for V_{DD} and V_L are determined by the circuit's minimum supply voltage and the voltage regulator implementation. The value of V_H on the other hand depends on system parameters like total power consumption of the system, the amount of data that needs to be transmitted, type of modulation and the value of C_{store}.

To relate these design variables, first the required energy for wireless operation is calculated. In this work, the power amplifier (PA) input signal is modulated in order to realize On-Off Keying (i.e., the PA is switched on and off) while the remaining TX core circuits are always on during modulation to minimize the startup time. Hence, the average DC power consumed by the transmitter during transmission in this case can be written as

$$P_{DC,Tx} = mP_{DC,PA} + P_{DC,core} \tag{3.6}$$

where m is the probability of transmitting a '0' and '1' data bit, $P_{DC,PA}$ is the DC power consumption of the PA and $P_{DC,core}$ is the DC power consumption of the remaining core circuits during transmission. Note that in this case $P_{DC,Tx}$ and $P_{DC,core}$ are calculated with respect to V_{DD} since the power loss due to the regulator voltage drop is included in $\eta_{regulator}$.

The required energy for wireless transmission is found by relating the amount of data to be sent, $Data$ [bit], to the $Bitrate$ [bit/s] and the regulator efficiency:

$$E_{req} = \frac{mP_{DC,PA} + P_{DC,core}}{\eta_{regulator}} \frac{Data}{Bitrate} \tag{3.7}$$

The energy available from the storage capacitor is given by

$$E_{av} = \frac{1}{2} C_{store} \left(V_H^2 - V_L^2 \right) \tag{3.8}$$

The design variables of the system then can be related to the design specifications by substituting (3.5) into (3.7) and equating this with (3.8). Rearranging the terms gives

$$\left(mP_{DC,PA} + P_{DC,core} \right) \frac{Data}{Bitrate} = C_{store} V_{DD} (V_H - V_L) \tag{3.9}$$

The system specifications are given on the left-hand side of (3.9) while on the right-hand side the design variables are found. In order to achieve high efficiency, a small difference between V_{DD}, V_H and V_L is required as evident from (3.5). This increases the required C_{store}, which also simultaneously improves the system sensitivity (i.e., the minimum available power to reach V_H) since the rectifier now requires less power at the antenna to charge C_{store} to V_H. For a given value of C_{store}, the minimum V_H is found by calculating

$$V_H = \frac{mP_{DC,PA} + P_{DC,core}}{C_{store} V_{DD}} \frac{Data}{Bitrate} + V_L \tag{3.10}$$

The active transmision time T_{active} is given by

$$T_{active} = \frac{C_{store} V_{DD} (V_H - V_L)}{mP_{DC,PA} + P_{DC,core}} \tag{3.11}$$

As an example, a simple WSN containing 128 bits of information with a 1 μF storage capacitor, 500 kbps data rate, $P_{DC,PA}$=1.5 mW, $P_{DC,core}$=0.5 mW, m=0.5 (On-off keying modulation with equal probability of transmitting a '0' and '1' data bit), V_{DD}=1V and V_L=1.1V requires a minimum V_H of 1.42 V and allows for a transmission time of T_{active}=256 μs. Using (3.5), a theoretical voltage regulator efficiency (neglecting bias currents) of 79.3% is found. With such a high efficiency, this voltage regulator actually approaches the efficiency of switching regulators, but with less ripple, area, noise and complexity [68].

Higher efficiencies can be achieved by for example increasing C_{store} such that the required V_H becomes lower. Although this increases the initial start-up charging time, it simultaneously improves the system sensitivity (i.e., the

minimum available power to reach V_H) since the rectifier now requires less power at the antenna to charge C_{store} to V_H. A practical upper limit for the capacitor selection is set by the leakage current. Large (super)capacitors tend to have relatively high leakage current compared to the current output of the RF energy harvester. Although the leakage current decays over time, the initial leakage current of typical supercapacitors can be in the order of 10-30 μA [69]. For the low power levels discussed in this thesis, the RF energy harvester is not able to supply this current and even if it can, a large portion of the harvested power will be wasted due to this leakage. Therefore the capacitor type should also be selected for relatively low leakage current. More details on loading effects can be found in Appendix A.

3.4 Frequency Synthesizer

The transmitter RF carrier is derived from the received continuous RF wave at the input of the RF energy harvester in the 902-928 MHz ISM band. The interface between the antenna, RF energy harvester and the frequency divider needs to be optimized in order not to degrade the performance of each circuit block. By extracting the input frequency and applying a frequency multiplication of ratio 8/3, a transmitter RF carrier between 2.405-2.47 GHz can be realized that covers almost the entire license-free 2.4 GHz ISM band [56]. The 8/3 architecture has been proposed first in [65] and has been implemented using a frequency divider and PLL. In the proposed RF-powered transmitter shown Fig. 3.1, the RF input signal frequency first is divided by three and subsequently used as Delay Locked Loop (DLL) reference signal. The DLL consists of a phase detector, charge pump with Low Pass Filter (LPF) and a Voltage Controlled Delay Line (VCDL) that produces eight evenly spaced signals that are fed to an eight-times frequency multiplier. For a 915 MHz input, the majority of the circuits thus operates at 305 MHz while only the PA operates at 2.44 GHz. Since the DLL mainly consists of logic gates and does not require any inductors, it allows for a compact and area efficient solution. The DLL also is a single-pole system and thus inherently stable [70]. The implementation details of each block are discussed in Chapter 7.

3.5 RF Power Amplifier

The limited power budget and short-range application of a WSN usually requires a Power Amplifier (PA) with small output power (<0 dBm). These so called 'medium' PAs are very challenging to design with high global effi-

ciency ($P_{out}/P_{DC,total}$) because the output power becomes comparable to the total power consumption of the WSN. Since the number of scientific publications on 2.4 GHz PAs with <0 dBm output power is very limited, Chapter 6 of this thesis is devoted to this topic.

The wireless transmitted information is encoded using On-Off Keying (OOK) modulation since it can be implemented with low complexity and low power consumption. This is achieved by simply enabling and disabling the PA. The power management and frequency synthesizer circuits are always on during modulation to minimize the startup time.

When following the previous WSN scenario example in Section 3.3 and assuming a PA efficiency of 50%, then a 1 mW (0dBm) power budget is available for wireless transmission. A possible receiving device might be an RFID reader, but can for example also be a smart phone or another (energy scavenged) WSN with a very strict power budget. Typically in these scenarios, it is foreseen that these WSNs use an ultra-low power wake-up receiver with limited data rate (<1 Mbps) and short wireless range. The wireless range depends on many different factors such as operating frequency, transmitter power, antenna gain, environment conditions and receiver sensitivity. Wake-up OOK receivers consuming sub-100μW operating at 2.4 GHz are reported with a sensitivity of around -72 dBm at 100 kbps [71–74]. Assuming this scenario with a 0 dBm Tx output power at 2.4 GHz and -72 dBm receiver sensitivity, in its simplest form, allows for a theoretical wireless transmission distance of approximately 39 m.

3.6 Conclusions

In this chapter a system level overview has been given of the challenges and requirements for RF-powered WSNs. The funcionality of the proposed RF-powered DLL-based transmitter has been briefly described. Furthermore, the relations between the design variables for the voltage regulator and power management have been derived and provide a framework for the circuit implementation. The design procedure and circuit implementation of highly-sensitive RF energy harvesters will be extensively discussed in Chapters 4 and 5, respectively. The power amplifier and frequency synthesizer circuit design will be discussed in detail in Chapter 6.

CHAPTER 4

ANTENNA-ELECTRONICS INTERFACES IN THE RECEIVING MODE

In this chapter, first the antenna and wave propagation fundamentals are discussed which leads to a general antenna equivalent circuit model. Subsequently, the co-design principles of antenna-electronics interfaces are presented for antenna systems in the receiving mode, which includes reception of wireless information and wireless power. Finally, two examples are treated to demonstrate the antenna-electronics co-design for the reception of wireless information (low noise amplifiers) and wireless power (RF energy harvesting).

4.1 Fundamental Antenna Parameters

Antennas close the interface gap between the electronics and the electromagnetic (EM) radiating fields. They are therefore of great significance in any wireless system and can even be a performance-limiting factor in terms of size, bandwidth and efficiency. In order to optimize this interface for a desired performance, a firm understanding of both domains is essential. Therefore, the fundamental antenna parameters are defined first.

Antenna Definition An antenna is a *transducer* designed to transmit or receive EM waves. In other words, antennas convert electrical energy into electromagnetic energy and vice versa. The radiation mechanism of any antenna is based on the acceleration of electric *charge*. This creates a time-varying electric field which again gives rise to a magnetic field and both fields propagate away from the antenna at the speed of light in case of free space. Thus, time-varying *currents* produce radiation and incoming radiation can produce time-varying currents. Antenna design is all about influencing the current distribution of a certain structure so that radiation properties such as efficiency, directivity, bandwidth and radiation pattern are met.

Radiation Pattern The relative distribution of the radiated power as a function of the direction in space is defined as the radiation pattern. A hypothetical *isotropic* radiator radiates equally well in all directions such that the power uniformly spreads out across the surface of an imaginary sphere. The power density S [W/m^2] at a distance d from a radiating isotropic RF source therefore equals the total radiated power by the transmitter divided by the surface area of a sphere:

$$S_{rad} = \frac{P_{rad}}{4\pi d^2} \tag{4.1}$$

The radiation intensity U in a given direction is defined as the power radiated from an antenna per unit solid angle and is defined as:

$$U = d^2 S_{rad} \tag{4.2}$$

Directivity Isotropic antennas do not exist in practice but are used to define the directivity of an antenna. When assuming a non-isotropic lossless antenna, then by the law of energy conservation this antenna should radiate or receive more effectively in some directions than in others. The directivity D is the ratio between the radiation intensity in a given direction to the radiation intensity of an isotropic antenna:

$$D = \frac{U_{Antenna}}{U_{Isotropic}} = \frac{4\pi U_{Antenna}}{P_{rad}} \tag{4.3}$$

Note that if the direction is not specified, it usually implies the direction of maximum radiation intensity, indicated by D_0.

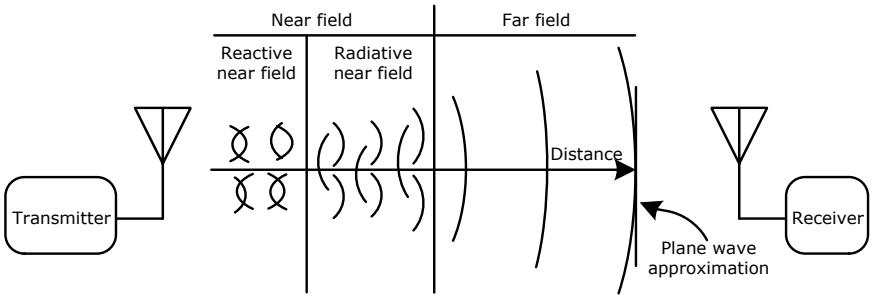


Figure 4.1: Radiation field regions with plane-wave approximation in the far-field.

Radiation Fields Near-and far-field can mean different things in different contexts. Defining the boundary between them is depending on the designers perspective and tolerances. There is not a definite boundary, but rather a transition from regions where either the reactive or the real power dominates [75]. For example, the boundary between the near and far-field can be defined as the distance from the antenna where the 1/d and $1/d^2$ terms (distance) of the field components are equal. This boundary definition is commonly used and is given by $d = \lambda/2\pi$. Another boundary given by $d = 2D^2/\lambda$ includes the size of the antenna and is valid for electrically large antennas [76, 77]. Setting the boundary through the wave impedance involves determining at what distance from the antenna the EM wave impedance becomes 'constant'. An excellent paper is available which goes through the various definitions and boundaries of the near-field [78].

In general, the reactive near-field of an antenna is the field region where the reactive power dominates the total complex power. This reactive power is not radiated but stored inside the electromagnetic field near the antenna. The angular field distribution is dependent upon the distance from the antenna and often is too complex to predict. In the radiative near-field, the real power dominates the total complex power but the angular field distribution still is dependent upon the distance from the antenna. In the far-field, the real power dominates the total complex power and the angular field distribution in this field is essentially independent of the distance from the antenna. When a receiving antenna is located in the far-field of the radiating source as depicted in Fig. 4.1, the wave can be approximated as a plane wave.

Antenna Radiation Efficiency The antenna radiation efficiency relates the radiated power to the power accepted by the antenna[1]:

$$\eta_A = \frac{P_{rad}}{P_{accepted}} \tag{4.4}$$

The radiated power P_{rad} is found by integrating the power density over an closed surface with radius d (distance) enclosing the radiating structure. The power accepted by the antenna $P_{accepted}$ is the actual power delivered to the antenna after taking any interface impedance matching losses into account (to be discussed in Section 4.2).
The antenna radiation efficiency can be subdivided into conductivity efficiency and dielectric efficiency

$$\eta_A = \eta_{cond} \cdot \eta_{dielectric} \tag{4.5}$$

The conductivity efficiency η_{cond} can be modeled using the concept of the antenna radiation resistance R_{rad} and loss resistance R_{loss}. The radiation resistance is not associated with any resistance in the antenna structure, but represents the power 'dissipated' or 'radiated' into free space. The power dissipated in R_{loss} represents the conduction losses due to the finite conductivity of the antenna material. When the antenna loss mechanism can be modeled as a series connection of resistances, then the conductivity efficiency is then given by

$$\eta_{cond} = \frac{R_{rad}}{R_{loss} + R_{rad}} \tag{4.6}$$

The total antenna resistance is thus defined as $R_A = R_{rad} + R_{loss}$ and can be found analytically or numerically for simple antenna geometries. For more complex geometries, η_{cond} can be determined by using the Wheeler Cap Method [75]. In this measurement, the test antenna is placed on a ground plane and its input impedance is measured at the resonant frequency of the antenna. The real part of the antenna impedance in this case corresponds to $R_{rad} + R_{loss}$. Then, the impedance is measured with a conducting sphere enclosing the antenna and ground plane with radius $\lambda/2\pi$. By surrounding the antenna with a conducting sphere, the radiating field is effectively removed without affecting the near-field energy of the antenna. As the input power is the sum of the radiated power and power loss, only the loss resistance R_{loss}

[1]The radiation efficiency for a given antenna is the same in the receiving mode as in the transmitting mode.

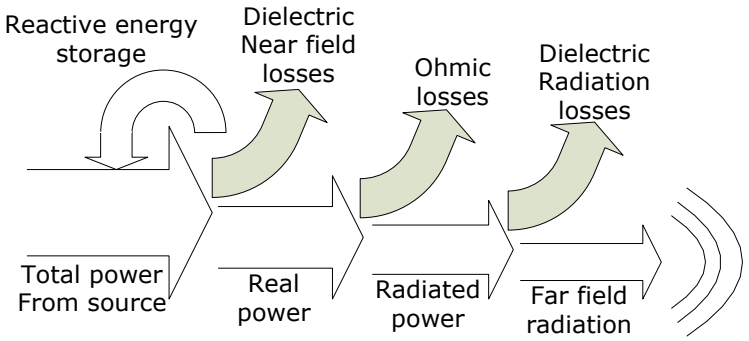


Figure 4.2: Power distribution of a lossy antenna in a conducting medium.

remains. The separation of R_{loss} and R_{rad} then allows to compute the antenna conductivity efficiency according to (4.6). Note that this method may not be valid when the antenna and its loss mechanism cannot be modeled by either a simple series RLC or a parallel RCL circuit [79].
An alternative way to measure η_{cond} is to determine the directivity from the radiation pattern in an anechoic chamber and subsequently calculate the efficiency using the concept of antenna gain. The antenna gain in this case is determined by placing two identical antennas with known directivity at a known distance. Subsequently, the power loss between them is measured, which allows to calculate the radiation efficiency.

The dielectric efficiency $\eta_{dielectric}$ is more difficult to compute and is usually measured as it strongly depends on the surrounding medium of the antenna. The dielectric efficiency is related to the reactive energy stored in the antenna's near-field. If the antenna is placed in a conductive medium, the reactive power will become partly real and doesn't contribute to the radiation from the antenna and is therefore lost in the near-field. This effect is illustrated in the power distribution diagram of a lossy antenna in a lossy medium shown in Figure 4.2. The lossy dielectric medium also causes dielectric radiation loss, but note that this is not included in the definition of the dielectric efficiency. The dielectric radiation loss corresponds to the propagation loss of the lossy medium and can be viewed as additional loss. In this thesis, it is assumed that the antenna is located in free space ($\eta_{dielectric} = 1$), such that the total antenna efficiency becomes $\eta_A = \eta_{cond}$.

Gain The gain G of an antenna is closely related to the directivity, but also takes the antenna efficiency into account.

$$G = \eta_A D \tag{4.7}$$

Bandwidth The bandwidth of an antenna can be considered to be the range of frequencies around a center frequency where the antenna characteristics such as input impedance, radiation pattern, directivity or efficiency are within an acceptable value. In this thesis, the bandwidth is related to the input impedance of the antenna.

Polarization Polarization of a radiated *wave* is defined as the property of an EM wave describing the time varying direction and relative magnitude of the electric field vector [54]. The polarization of an *antenna* in a given direction is defined as the polarization of the wave radiated by the antenna. An antenna or wave can be linear, circular or elliptically polarized. If the antenna and the wave do not have the same polarization, the amount of power extracted by the antenna will not be maximized due to the polarization loss factor $PLF = |\cos\Psi|^2$. This factor depends on the polarization angle Ψ between the transmitting and receiving antenna.

Input Impedance The input impedance of an antenna is defined as the ratio of voltage to current seen at the feedpoint terminal, also known as the feedpoint impedance. This impedance can be modeled as $Z_A = R_A + jX_A$ and is dependent on frequency, antenna shape and the surrounding environment. The sign of the input reactance depends on the near-field predominance of field type: electric (capacitive) or magnetic (inductive). At resonance (zero reactance) the stored energies due to the near-fields are equal.

Dependence on the Surrounding Environment All antenna parameters are dependent on the wavelength λ and thus are also dependent on the medium in which the antenna is located. The wavelength dependence on the medium can be described by

$$\lambda(j\omega) = \frac{\lambda_0}{\sqrt{\varepsilon_r(\omega) + \frac{\sigma(\omega)}{j\omega\varepsilon_0}}} \tag{4.8}$$

where λ_0 is the wavelength in free space [m], $\varepsilon_r(\omega)$ is the relative permittivity, $\varepsilon_0 = 8.854 \cdot 10^{-12}$ is the permittivity of free space [F/m], $\sigma(\omega)$ is the conductivity of the medium [S/m] and ω is the angular frequency [rad/s]. By

placing an antenna in a theoretical non-conducting and high permittivity environment extending to infinity, the antenna effectively becomes a factor $\sqrt{\varepsilon_r}$ electrically larger compared to the same antenna in free space. This property is widely used to scale down the antennas physical size.

4.2 Wave Propagation and Available Power

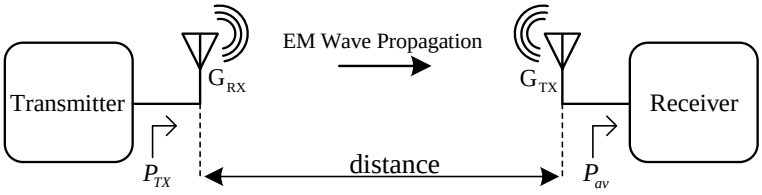


Figure 4.3: Wireless power transfer in the far-field region using a transmitting and receiving antenna.

To understand how the terminal voltage and current of a receiving antenna relate to the radiated power from a transmitting antenna, the available power at the receiving antenna needs to be determined. When a signal generator at the transmitter side forces a time-varying current through an antenna structure, electromagnetic radiation is produced and distributed in space according to the antenna radiation pattern. Following the definitions of antenna gain and isotropic radiators in Section 4.1, the power density S [W/m^2] at a distance d from a transmitting antenna with gain G_{TX} and transmitter power P_{TX} is written as

$$S = \frac{P_{TX}}{4\pi d^2} G_{TX} = \frac{P_{EIRP}}{4\pi d^2} \tag{4.9}$$

where $P_{EIRP} = P_{TX} G_{TX}$ is defined as the Equivalent Isotropic Radiated Power (EIRP). The amount of power collected by a receiving antenna located in the far-field region of the transmitter can be found by using the concept of antenna effective area. The antenna effective area A_{eff} is defined as the ratio of the available power P_{av} to the power density of a plane wave incident on the antenna.

$$A_{eff} = \frac{P_{av}}{S} \tag{4.10}$$

The available power is defined as the maximum power that can be extracted from an antenna and can be delivered to the load (i.e., power at the

input of the RF energy harvester or receiver). The actual dissipated power in the antenna load only equals P_{av} in case of a lossless and perfectly impedance matched antenna-electronics interface.

For any receiving antenna, it can be proven that the effective antenna area is closely related to its gain G_{RX} [54]:

$$A_{eff} = \frac{\lambda^2}{4\pi} G_{RX} \tag{4.11}$$

The available power to a lossless and perfectly aligned receiving antenna in free space is then given by

$$P_{av} = A_{eff} S = \left(\frac{\lambda}{4\pi d}\right)^2 G_{RX} P_{EIRP} \tag{4.12}$$

This equation known as the 'Friis transmission equation' [80] gives a fundamental limit to the available power as a function of distance, power, frequency and antenna gain. The $(\lambda/4\pi d)^2$ term is often referred to as 'free space path loss'. This expression, however, suggests that free space somehow attenuates a propagating electromagnetic wave with decreasing wavelength and increasing distance. This is a misconception. Firstly, the radiated power is not lost over distance, but merely spreads out across the surface area. Therefore, only a portion of this spherical wavefront is captured by the receiving antenna. Secondly, the wavelength enters the equation because of the effective antenna area. A shorter wavelength corresponds to a smaller effective antenna area and therefore is less effective to capture energy from the incoming wave. In order to capture the same power at a shorter wavelength, the physical area of the antenna needs to be increased.

It is important to emphasize that (4.12) is only valid if the receiving antenna is located in the far-field of the transmitting antenna. For closer distances, the incoming wave can no longer be approximated as a plane wave and thus gives inaccurate predictions.

Practical Limitations

There are several practical limitations that can strongly influence the available RF power at a given distance from the RF energy source. The theoretical line-of-sight available power of (4.12) can be extended to a more practical form

$$P_{av} = \left(\frac{\lambda}{4\pi d}\right)^n G_{RX}(\theta,\varphi) P_{EIRP} \left(1-|\Gamma|^2\right) |\cos\Psi|^2 \tag{4.13}$$

where

- n is the wave propagation exponent which can range between 0.8 to 1.8 in a (highly) reflective line-of-sight environment and can get as high as 8.6 for non-line-of-sight environments [48];
- $G_{RX}(\theta,\varphi)$ is the receiving antenna gain and is a function of the azimuth angle θ and the elevation angle ψ and depends on the type of antenna being used;
- $\left(1-|\Gamma|^2\right)$is the interface impedance mismatch efficiency at the receiver, where $\Gamma = (Z_L - Z_A^*)/(Z_L + Z_A)$ is the power wave reflection coefficient, Z_A is the antenna impedance and Z_L is the antenna load impedance [81];
- $|\cos\Psi|^2$is the polarization loss factor and depends on the angle Ψ between the transmitting and receiving antenna and their polarization.

4.3 Antenna Equivalent Circuit Model

An antenna relates the terminal voltage, current and impedance of the antenna to the incident electromagnetic field power. From the point of view of the antenna load, the antenna behaves as a generator with an internal impedance. Hence, an equivalent circuit model needs to be found that correctly describes the antenna characteristics.
From an electronic design perspective we are interested in a simple equivalent circuit model consisting of a voltage or current source combined with resistances, capacitances and inductances to represent the available power, efficiency and frequency dependence. Other antenna parameters such as radiation pattern, directivity and polarization are *not* included as these are already included in the definition of the available power P_{av}.

To relate the antenna terminal voltage to the available power P_{av} as calculated from 4.12, the antenna-electronics interface model as depicted in Fig.

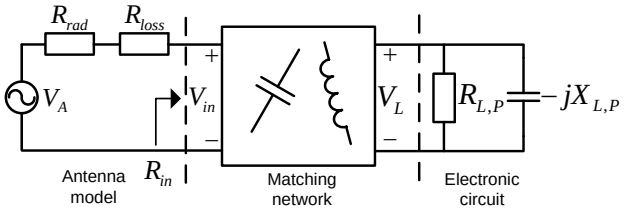


Figure 4.4: Antenna-electronics interface model.

4.4 may be used. For now, the antenna impedance is assumed to be purely real for convenience. However, it is also valid to assume that the imaginary part of the antenna impedance is absorbed into the matching network; it does not make a difference for the following analysis. The voltage induced by the electric field is represented by a Thévenin equivalent antenna voltage source V_A. The total antenna series resistance amounts to $R_A = R_{rad} + R_{loss}$.

The electronic circuit load is modeled as a parallel combination of resistance $R_{L,P}$ and reactance $X_{L,P}$. To relate V_A to P_{av}, a lossless and conjugate impedance matched network is assumed. In this scenario, it follows that $V_{in} = \frac{1}{2}V_A$ as $R_{in} = R_{rad} + R_{loss}$. Hence, the power balance for a lossy antenna with a conjugate impedance matched interface is written as

$$P_{av} = \frac{(V_A/2)^2}{2\,(R_{rad} + R_{loss})} \tag{4.14}$$

Note that the left-hand side of (4.14) also includes the antenna radiation efficiency η_A because of the way P_{av} is defined in (4.12). Using $R_A = R_{rad} + R_{loss}$, it follows that

$$V_A = \sqrt{8R_A P_{av}} \tag{4.15}$$

It is noteworthy that P_{av} reduces linear with a decrease in η_A, while $R_A = R_{rad}/\eta_A$. The equivalent antenna source voltage thus does not depend on η_A, therefore it can also be written as

$$V_A = \sqrt{8R_{Rad} P_{av,ideal}} \tag{4.16}$$

where $P_{av,ideal}$ represents the 'ideal' received available power of a lossless antenna. The reduction in P_{av} at the antenna load due to a decrease in η_A comes from the additional loss resistance R_{loss} that limits the current flow through the antenna and hence power in its load. For example, Equation (4.16) quickly reveals that a 50 Ω antenna with $P_{av,ideal}$=-20 dBm (10 μW) has a

63.2 mV antenna equivalent circuit voltage[2]. When η_A decreases to 90%, a loss resistance of $R_{loss} = R_{rad}(1-\eta_A)/\eta_A \approx 5.56\ \Omega$ is added to the equivalent antenna model, which reduces the available power in the antenna load to 9 μW, as evident from (4.14).

The relationship between V_A, R_{rad} and other system design parameters is found by substituting (4.12) into (4.15):

$$V_A = \sqrt{\frac{R_A G_{RX} P_{EIRP}}{2}} \frac{\lambda}{\pi d} \tag{4.17}$$

The relations between the antenna equivalent circuit elements are summarized in Table 4.1.

Table 4.1: Antenna equivalent circuit elements.

Antenna resistance	$R_A = R_{rad} + R_{loss}$
Radiation efficiency	$\eta_A = \frac{R_{rad}}{R_{rad}+R_{loss}}$
Radiation resistance	$R_{rad} = R_A \eta_A$
Conduction loss resistance	$R_{loss} = R_{rad}\left(\frac{1-\eta_A}{\eta_A}\right)$
Thévenin equivalent voltage	$V_A = \sqrt{8R_A P_{av}} = \sqrt{8R_{Rad} P_{av,ideal}}$

Frequency Dependence

The frequency dependence of the antenna impedance over a given frequency range is modeled using inductances and capacitances and depends on the type of antenna. Fig. 4.5 shows the typical impedance versus frequency of a center fed electric dipole antenna. For frequencies below the first resonance frequency ($X_A(\omega) \ll 0$), the electric dipole antenna behaves as an RC series circuit. Around the first natural resonant frequency ($X_A(\omega) = 0$ and $\frac{\partial X_A(\omega)}{\partial \omega} > 0$), it behaves as a series RLC circuit. When moving towards the natural anti-resonant frequency ($X_A(\omega) = 0$ and $\frac{\partial X_A(\omega)}{\partial \omega} < 0$), the antenna behaves as a parallel RLC circuit [82]. The modeling accuracy and frequency range therefore determine the complexity of the antenna equivalent circuit model. Loop antennas on the other hand behave as an RL series circuit for frequencies below the first anti-resonance frequency. Designers thus need to choose the correct antenna type to realize a specific antenna impedance. In many narrowband systems, a simple antenna model consisting of a resistance and a reactance is

[2]In general, the equivalent antenna voltage V_A is *not* the voltage swing at the load. The load voltage can be smaller or larger than V_A, depending on the interface impedance.

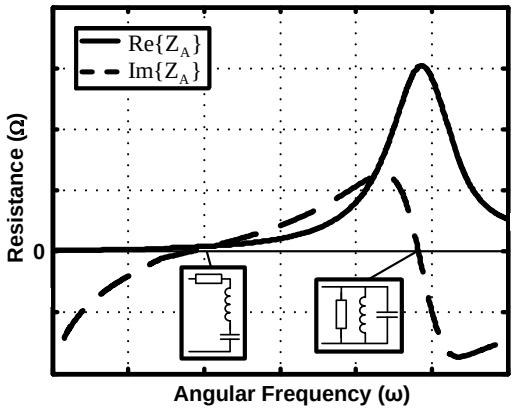


Figure 4.5: Typical impedance vs. frequency plot for a center fed electric dipole antenna. The appropriate circuit models are identified near resonance points

sufficient to correctly model the terminal I-V characteristics for a given frequency range.

Other Model Limitations

It is worth mentioning other limitations of this antenna model besides the limited frequency range. First of all, the dielectric losses cannot be represented by simply adding another series resistance to this model. The dielectric losses can be determined using EM simulation tools of the antenna inside the lossy medium. Another limitation of the receiving antenna model arises when the power dissipated in R_A is referred to as the re-radiated (scattered) power of the antenna, which is very common in many antenna textbooks [54, 83, 84]. In this case, the Norton and Thévenin equivalent circuits do *not* provide the same re-radiated power for the same conditions. This apparent paradox has been recognized by some antenna engineers and has been heavily debated for decades between several authors. More details can be found in Appendix B.

4.4 Wave Impedance and Impedance Matching

The transition from an incoming EM wave to the electronics can be viewed as two transitions; one from the EM field to the antenna and another transition from the antenna to the electronics. The latter can be optimized for maximum power by using conjugate matching ($Z_L = Z_A^*$). One can extend this reasoning

and ask if there exists a similar impedance matching requirement for the first transition. As the wave impedance is the ratio of the strength of the electric and magnetic fields ($Z_0 = \sqrt{\mu_0/\varepsilon_0} \approx 377\ \Omega$ in free space conditions), should the antenna impedance be matched to 377 Ω in order to optimize reception?

First of all, it is worth to emphasize that the impedance of free space in the far-field is 377 Ω regardless of the feedpoint antenna impedance. For smaller distances however, the E/H ratio becomes dependent on the distance from the antenna and can become larger or smaller than 377 Ω, depending on antenna and its near-field predominance of field type: electric (capacitive) or magnetic (inductive) [78].
Secondly, consider a lossless antenna driven by a conjugate matched generator. As there is no power loss at this interface, the antenna must radiate 100% of its energy into free space as there is no power reflected back from the antenna. A 10 Ω or 400 Ω antenna therefore does not radiate less efficiently than a 377 Ω antenna. In a way, the antenna acts as a 2-port transducer that converts the voltage [V] and current [A] at its terminals to electromagnetic fields [V/m] and [A/m] and guides the fields towards free space with a characteristic impedance of 377 Ω.

The reason why the majority of antenna interfaces are 50 Ω comes from historic standardization and goes back to the development of coaxial cables for high power radio waves. The cable characterisic impedance determines the power handling (maximum at 30 Ω) and loss (minimum at 77 Ω) [85]. A characteristic impedance of 50 Ω is thus a compromise between power handling and signal loss. Furthermore, the widely used half-wavelength dipole antenna has an input resistance of 73 Ω, which presents a good match to 50 Ω interfaces.

4.5 Co-Design of Antenna-Electronics Interfaces

During the design process of a wireless system, the antenna and electronic circuit designers sometimes are operating independently from each other and are considered to belong to separate disciplines. Both designers agree upon a common characteristic impedance (Z_0) of the antenna-electronics interface and subsequently optimize their part of the system. The electronic circuit often requires an impedance transformation network while the antenna usually is directly matched to the characteristic impedance of a transmission line (Fig. 4.6(a)) to avoid propagation effects in the interface. Traditionally, this characteristic impedance is commonly assumed to be 50 Ω, without any further discussion. Although this standardization may be convenient from a mea-

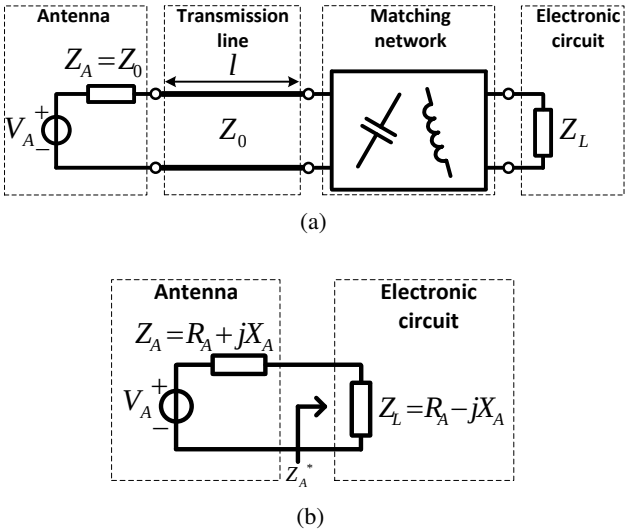


Figure 4.6: (a) Conventional and (b) co-designed antenna-electronics interface in the receiving mode.

surement point of view, it is a rather uncomfortable assumption to make as it clearly cannot be the optimum impedance for all design challenges when for example considering noise performance, efficiency or antenna size.

4.5.1 Co-Design Principle

By co-designing the antenna-electronics interface, both disciplines share a common optimization target and can agree on an alternative interface impedance to optimize the overall system performance for a specific application. The choice of interface impedance plays a crucial role in the optimization of antenna systems in the receiving mode.

Let's first consider the need of the transmission line in the conventional interface as shown in Fig. 4.6(a). If the length between the antenna and the electronic circuit is electrically short ($l < \lambda/10$), then the propagation effects at the interface can be neglected as the voltage and current can be considered constant along the line [81]. This, for example, may be the case for Integrated Circuits (ICs) with on-chip antennas [86] and ICs that are directly integrated into an off-chip antenna as demonstrated in [87] and [88].
The interconnection between the antenna and electronics then can be modeled as a simple wire or lumped elements instead of distributed elements. In this case there is no fundamental reason to use transmission lines and hence no

need to impedance match to Z_0. This opens up the possibility to directly match the antenna to the electronic circuitry as illustrated in Fig. 4.6(b). The use of the matching network and transmission line is thus avoided, thereby eliminating the loss and noise that would otherwise be introduced by these networks. Although this non-50 Ω interface makes the verification process more complex as it may require an anechoic chamber [88] or non-linear source-pull measurement [89], it also allows to increase the voltage or current at the antenna load (i.e. the electronic circuit equivalent input impedance) for the same available power at the antenna. Before elaborating further on this topic, first a distinction has to be made between wireless power reception and wireless information reception.

4.5.2 Wireless Power Reception

The design goal for wireless power reception is obviously to transfer maximum power from the antenna to the electronics. When DC electric power is required, a rectifier can be directly conjugate matched to the antenna. In practice however, the rectifier is implemented using (Schottky) diodes or MOS transistors, which inherently are *voltage controlled* devices and require a minimum voltage in order to conduct a certain amount of current. This sets the second design condition that a sufficiently large voltage needs to be generated in order to *activate* the rectifier while simultaneously achieving maximum power transfer. This becomes the main design concern for applications with limited available power at the antenna, which is the case for highly sensitive RF energy harvesters and wireless implantable medical devices.

4.5.3 Wireless Information Reception

The reception of wireless information is fundamentally different from wireless power reception in the sense that information processing in principle does not require power transfer from the EM wave to the electronics. Although power is required to propagate information over free space from one antenna to another, this power is not required for the readout of the receiver. From the electronic circuit's point of view, the information in the field strength can be represented by either voltage or current and the designer has to choose which signal quantity represents the information in the most accurate way and which quantity is more favorable to measure with the electronics. The interface then has to be optimized to maximize this preferred signal quantity to for example obtain the highest signal-to-noise ratio or amplitude. The power required for amplification is provided by the receiver's power supply, not the incomming

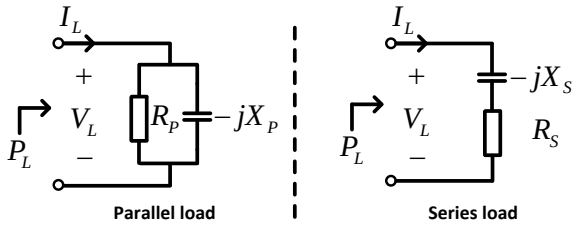


Figure 4.7: Antenna load impedance equivalent model.

EM wave.

4.5.4 Voltage, Current and Interface Impedance

Optimizing the interface for maximum voltage or current is a matter of first optimizing the antenna load impedance. In many cases, the load for a given frequency range can be modeled as either a series or parallel combination of resistance and reactance (Fig. 4.7). Depending on preference and application, one might be more convenient to use than the other, but both provide the same characteristics. In this analysis, an antenna load impedance with capacitive reactance is assumed, which holds for the majority of integrated circuits.

Without making any assumptions about the source, the power in the load can be expressed as

$$P_L = \left(1 - |\Gamma|^2\right) P_{av} \tag{4.18}$$

where $\Gamma = (Z_L - Z_A^*) / (Z_L + Z_A)$ is the power wave reflection coefficient [81], Z_A is the antenna impedance, Z_L is the antenna load impedance and P_{av} denotes the power available to the antenna. The current magnitude through the load then equals

$$|I_L| = \sqrt{\frac{2\left(1 - |\Gamma|^2\right) P_{av}}{R_S}} \tag{4.19}$$

while the voltage magnitude across the load is

$$|V_L| = \sqrt{2\left(1 - |\Gamma|^2\right) P_{av} R_P} \tag{4.20}$$

In both cases, a conjugate matched interface ($Z_A = Z_L^*$) produces the maximum voltage and current at a given antenna load, which is the first condition

to optimize the desired signal quantity. Although this condition relates the *relative* impedance between the antenna and electronic circuit, the key point is that an additional increase in voltage or current can be achieved by correctly choosing at *which* impedance level conjugate matching occurs.

When assuming an ideal conjugate matched interface, the voltage across the parallel load terminals is given by

$$|V_L| = \sqrt{2P_{av}R_P} \tag{4.21}$$

The voltage across the load of the equivalent series impedance is calculated using the parallel-to-series conversion equations

$$R_P = \left(1+Q^2\right)R_S \tag{4.22}$$

and

$$X_P = \left(1+\frac{1}{Q^2}\right)X_S \tag{4.23}$$

where $Q = (X_S/R_S) = (R_P/X_P)$. Note that this impedance conversion is only valid around the resonance frequency. The voltage in terms of the series load is then expressed as

$$|V_L| = \sqrt{2P_{av}R_S}\sqrt{1+Q^2} \tag{4.24}$$

Equation (4.24) indicates that the output voltage can be 'boosted' by increasing the Q-factor of the interface. It should be noted that this also requires a larger parallel load resistance R_P due to the equivalence of (4.21) and (4.24). Hence, when the available power and antenna load are fixed, one cannot increase the load voltage to higher levels by means of antenna design (except using a physically larger antenna with higher directivity). *The designer therefore needs to design the electronic circuit for the largest R_P possible and subsequently co-design the antenna impedance for conjugate matching.* This conclusion is a key point that needs to be considered during the design procedure.

The load current can similarly be found by writing

$$|I_L| = \sqrt{\frac{2P_{av}}{R_S}} \tag{4.25}$$

and thus can only be maximized by minimizing R_S. This is equivalent to the following expression in terms of the parallel load

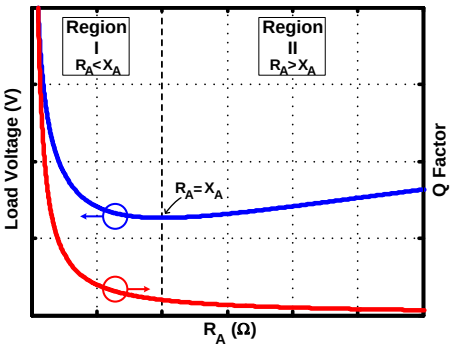


Figure 4.8: Antenna load voltage vs antenna resistance for non-zero antenna reactance.

$$|I_L| = \sqrt{\frac{2P_{av}}{R_P}}\sqrt{1+Q^2} \tag{4.26}$$

Thus, the maximum voltage and current at the interface is set only by the antenna load impedance and the available power. This conclusion is in accordance with the results published in [51], where it was shown that adding a resonant circuit does not help to further increase the load voltage for a fixed load impedance.

The antenna impedance ($Z_A = R_A + jX_A$) is found by determining the required ratio of the real and imaginary part of the load impedance. When considering voltage to be the signal quantity to maximize and assuming a conjugate matched interface ($X_A = X_S$ and $R_A = R_S$), Equation (4.24) can be rewritten as

$$|V_L| = \sqrt{2P_{av}\left(\frac{R_A^2 + X_A^2}{R_A}\right)} \tag{4.27}$$

Equation (4.27) is plotted in Figure 4.8 together with the Q-factor and shows the antenna load voltage versus antenna resistance for a given P_{av} and non-zero X_A. Note that the voltage can be maximized by either decreasing or increasing R_A and is at its minimum when $R_A = X_A$. Two different regions thus can be identified, being Region I for $R_A < X_A$ and Region II for $R_A > X_A$.

When assuming $R_A \ll X_A$ in Region I, (4.27) simplifies to

$$V_L|_{R_A \ll X_A} \approx \sqrt{2P_{av}}\frac{X_A}{\sqrt{R_A}} \tag{4.28}$$

In this region, the output voltage is passively boosted by the presence of the antenna reactance, which forms an LC resonator with the load. Significant improvement for large values of Q can be achieved at the expense of bandwidth.

When assuming $R_A \gg X_A$ in Region II, (4.27) simplifies to

$$V_L|_{R_A \gg X_A} \approx \sqrt{2P_{av}R_A} \tag{4.29}$$

In this region, the antenna impedance can be considered to be purely real. The load voltage is simply determined by the resistive voltage division between the antenna and its load. But since the equivalent Thévenin antenna voltage itself depends on the antenna resistance by $V_A = \sqrt{8P_{av}R_A}$, the load voltage increases, although at a slower rate compared to Region I. On the other hand, Region II has a fundamentally wideband characteristic, which can be exploited in the design of wideband Low Noise Amplifiers (LNA).

4.6 Co-Design Examples

In this section, two examples are treated to demonstrate the antenna-electronics co-design for the reception of wireless information by means of a low-noise amplifier (LNA) and wireless power by means of RF energy harvesting.

4.6.1 Low Noise Amplifier

The co-design of any antenna-electronics interface starts by optimizing the antenna load impedance, which in this example is a 900 MHz narrowband LNA[3]. The well-known inductively degenerated CMOS cascode LNA topology [90] is used as it provides an easy way of adjusting the LNA input impedance. The LNA is directly connected to an inductive antenna as depicted in Fig. 4.9. The information is sensed with a CMOS gate, meaning that voltage is the preferred signal quantity to maximize.

Along with the desired signal V_A, the antenna picks up noise from all points within its radiation pattern and thus depends on how the antenna is directed towards its environment. However, at radio frequencies it is usually assumed that the random noise of an antenna will be as low or lower than the thermal noise corresponding to room temperature [91]. The antenna noise can thus be modeled as $\overline{V_{n,A}^2} = 4kTR_A\Delta f$, where $k = 1.38 \cdot 10^{-23}$ J/K is Boltzmann's constant, $T = 300\,K$ and Δf denotes the unit bandwidth.

[3]The antenna-LNA co-design described in this section is the result of a cooperation with Yao Liu from Delft University of Technology.

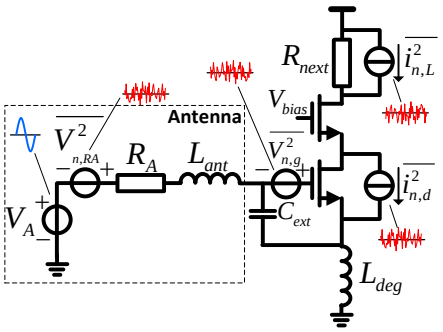
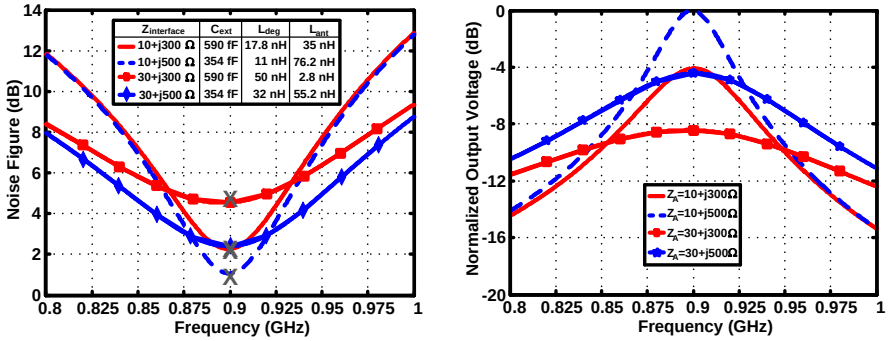


Figure 4.9: Interface model of an inductively degenerated CMOS LNA directly connected to an inductive antenna including relevant noise sources.

Other relevant sources of noise are the channel noise of the transistor $\overline{i_{n,d}^2} = 4kT\gamma g_m \Delta f$, the gate resistance $\overline{v_{n,g}^2} = 4kT\gamma R_g \Delta f$ and the LNA load noise $\overline{i_{n,L}^2} = 4kT\Delta f / R_{next}$. Here, g_m denotes the transconductance of the MOS transistor, R_g the transistor gate resistance and R_{next} is the loading resistance of the next stage. The coefficient γ is often between 2/3 and 2, depending on the transistor size and the technology. Note that the noise contribution of the cascoding transistor is negligible at low and medium frequencies as only a small fraction of its noise is transferred to the output due to its relatively low input impedance.

The performance of the LNA is evaluated using the Noise Factor (F), which is a measure of how much noise is relatively added by the LNA compared to the noise generated by the source. It is worth to emphasize that the noise factor therefore is defined for a specific antenna resistance and thus can be improved by co-design. A larger antenna resistance for example generates more noise, but also equally scales the desired antenna voltage as $V_A = \sqrt{8P_{av}R_A}$. The input Signal-to-Noise Ratio (SNR) therefore does not change. However, the noise of the LNA now appears relatively smaller compared to the antenna noise, resulting in a lower noise factor and therefore better SNR at the output.

For this particular LNA implementation, the interface impedance is defined as $Z_{interface} = R_A + j\omega(L_{ant} + L_{deg}) = R_A + jX_A$ as the total inductance in the interface is the sum of the antenna and the degeneration inductor. As the narrowband LNA operates in Region I, the antenna load voltage is thus approximated by (4.28) for large values of Q. When assuming the interface to be at the resonance frequency with conjugate matching, the minimum noise



(a) (b)

Figure 4.10: (a) Simulated Noise Figure and (b) normalized voltage transfer for narrowband LNA for various interface impedances. The calculated NF_{min} using (4.30) is marked by 'X'.

factor for low and medium frequencies can be approximated as

$$F_{min} \approx 1 + \delta \frac{R_g}{R_A} + \underbrace{\frac{R_A}{X_A^2}}_{co-design} \underbrace{\left(\frac{\gamma}{g_m} + \frac{4}{g_m^2 R_{next}} \right)}_{LNA} \tag{4.30}$$

Notice that the 'LNA' term in (4.30) only depends on the LNA circuit parameters and can be minimized by increasing the MOS transistor's bias current and gate area. The 'co-design' term allows to reduce the noise factor without additional power consumption by using a high-Q impedance interface. The input-referred noise of R_g is suppressed by the interface gain due to the presence of the external capacitor C_{ext}. This is indicated by δ, which scales with $1/Q^2$ when $C_{ext} \gg C_{gs}$.

The LNA is designed in AMS 0.18 μm technology and its design parameters are kept constant during the following circuit simulations ($g_m = 366\,\mu S$, $C_{gs} = 4$ fF, $R_g = 18\ \Omega$, $R_{next} = 10$ kΩ, $\gamma = 1.1$). The LNA input impedance is varied by tuning L_{deg} and C_{ext} while the antenna is subsequently conjugate matched to the LNA input for each case. The inductive antenna is modeled as an inductor L_{ant} in series with a power port with resistance R_A. The difference in noise factor is thus only determined by the difference in interface impedance. As a proof of concept, the antenna and matching components are considered lossless.

The minimum simulated noise factor in dB (i.e., the noise figure, NF) shown in Figure 4.10(a) matches well with the theoretical values obtained

from (4.30) for all interface impedances. Note that the $10 + j300\Omega$ and $30 + j500\Omega$ interface have approximately the same NF_{min}, but the $30 + j500\Omega$ interface has a larger NF bandwidth because this interface has an approximately two-times lower Q-factor.
Figure 4.10(b) shows the normalized voltage transfer and clearly indicates the tradeoff between maximum voltage gain and bandwidth. The LNA -3dB bandwidth with respect to the voltage transfer is simply determined by the RLC antenna-electronics interface and agrees very well with the theoretical $f_{-3dB} = f_0 \frac{2R_A}{X_A}$.

For minimum NF, R_A should be as low and X_A as high as possible. In practice however, this will cause the antenna radiation efficiency to drop considerably when the antenna conduction loss resistance becomes comparable to R_A [92]. In this case, a minimum R_A should be selected during the optimization. The LNA input however, *can* be designed for maximum parallel resistance (i.e., ideally purely capacitive input impedance) and therefore would increase the load voltage by 6 dB when keeping R_A fixed at the minimum value [93]. It is important to point out that a conjugate matched interface in theory would increase the voltage even further, but in this case would require a purely inductive antenna with infinitely small antenna radiation resistance and conduction loss resistance, which of course is not realizable.

4.6.2 RF Energy Harvesting

The co-design of an antenna and a rectifier is slightly more complex compared to the LNA example in the sense that the rectifier is highly nonlinear. An RF energy harvester therefore is usually optimized for a given input power in a narrow frequency band as the interface is hard to conjugate match over a broad input power range. Recalling from Section 4.5, it is critical to generate a sufficiently large voltage to overcome the threshold voltage of the transistors while simultaneously achieving maximum power transfer. Although there are many rectifier implementations to choose from that all have their own advantages and disadvantages, it is essential for the co-design to choose a rectifier topology that provides a high parallel input resistance R_P. In this example, a conventional two-stage diode-connected NMOS rectifier is used as depicted in Fig. 4.11. Each stage consist of a voltage doubler configuration using two capacitors and two NMOS transistors .
The effective input resistance R_P of this rectifier implementation depends on the input voltage, but can also be increased by increasing the transistor threshold voltage V_{TH}, as was proven in [94]. A larger V_{TH} increases the voltage boost but also increases the minimum voltage to activate the rectifier, meaning

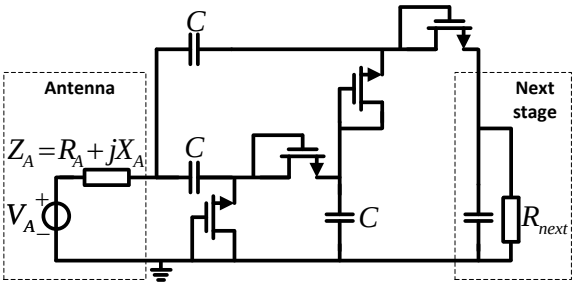


Figure 4.11: Two-stage diode-connected NMOS recitifer connected to an inductive antenna..

that there is a tradeoff to be made for the value of V_{TH}. This can for example be done by adjusting the body voltage or using different V_{TH} transistors.

Two rectifiers are implemented with identical transistor size (W/L=1000), coupling capacitors (C=0.8 pF) and resistive load ($R_{next} = 300$ kΩ). The only difference is that one rectifier is implemented with standard threshold voltage transistors ($V_{TH,standard} = 560$ mV) while the other rectifier uses low threshold transistors ($V_{TH,low} = 440$ mV). The simulated input series resistance of the two rectifiers at -15 dBm input power at 900 MHz is 20 Ω and 15 Ω for the $V_{TH,low}$ and $V_{TH,standard}$ implementation, respectively. The simulated input series reactance is 450 Ω for both implementations. The antenna is subsequently conjugate matched to the rectifier input impedance for both cases.

The simulated power efficiency ($\eta = P_{out}/P_{av}$) and steady state DC output voltage are shown in Fig. 4.12. For input power levels lower than -20 dBm, both interfaces do not generate sufficient input voltage to overcome the threshold voltage of the transistors. However, since the 20 Ω rectifier implementation uses lower threshold voltage transistors than the 15 Ω implementation, it shows slightly better efficiency at low (<-17 dBm) input levels. For input power levels higher than -17 dBm, the 15 Ω rectifier benefits more from the interface voltage boost and thus has a larger transistor overdrive voltage compared to the 20 Ω interface, resulting in a significant efficiency improvement. When looking at the simulated steady state DC output voltage, it is evident that the 15 Ω interface generates a significantly larger output voltage compared to the 20 Ω interface. This can be used to for example increase the maximum energy storage capability ($E_{store} = \frac{1}{2} C_{store} V_{out}^2$) when charging a (super)capacitor for autonomous wireless sensor nodes.

Note that the correct design procedure for both the LNA and the RF energy harvester is to design the antenna according to the electronics, not the

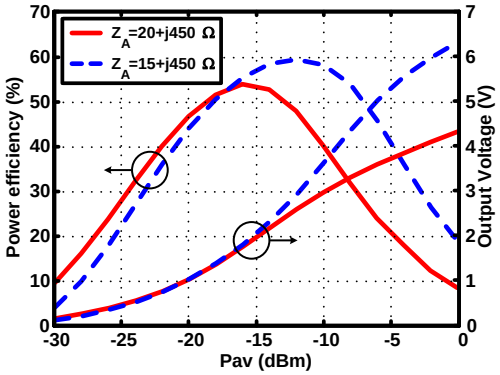


Figure 4.12: Simulated power efficiency and DC output voltage vs. available power for two different rectifier input impedances with $R_{next} = 300$ kΩ.

other way around. This design approach is required since the overall antenna-electronic performance (like NF or efficiency) does not depend only on the choice of interface impedance but also on the circuit implementation. The antenna thus needs to be designed *after* the optimum circuit implementation with corresponding interface impedance is known.

4.7 Conclusions

The fundamental antenna and wave propagation properties have been presented in the first part of this chapter and lead to a general antenna equivalent circuit model with its practical limitations. Subsequently, the co-design principles have been presented for electrically-short antenna-electronics interfaces in the receiving mode. It was argued that power transfer is not the only design objective in these interfaces, but that the interface needs to be optimized for either voltage or current, depending on which is more favorable to measure with the electronics. The first condition is to conjugate match the antenna-electronics interface as this maximizes both the voltage and current at the load. The second condition is to determine at which impedance level conjugate matching should occur in order to further increase the load voltage or current. When following this reasoning, co-design can be used to improve the system performance like noise figure, efficiency and sensitivity without increasing the power consumption. This was demonstrated with a co-design example for the reception of wireless information by means of an antenna and an LNA, and for the reception of wireless power by means of an antenna and a rectifier.

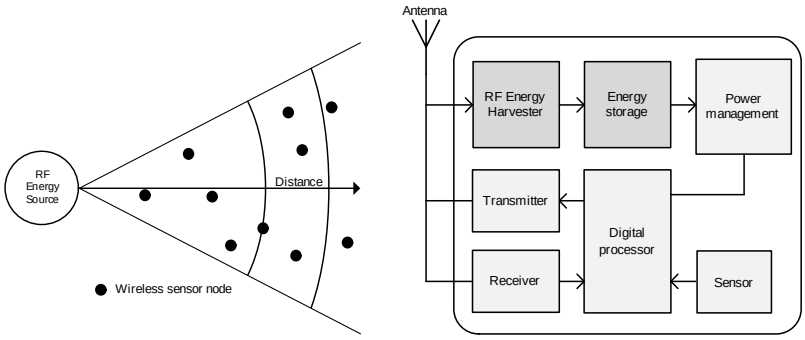
CHAPTER 5

HIGHLY SENSITIVE RF ENERGY HARVESTER DESIGN

Following the antenna-electronics co-design principles presented in the previous chapter, this chapter describes the design of a compact self-calibrating and highly sensitive RF energy harvester in standard CMOS technology. First the design challenges and the proposed solution are discussed in Section 5.1 followed by the circuit design in Section 5.2. The rectifier co-design with the antenna is discussed in Section 5.3 and the experimental results are given in Section 5.4.

5.1 Introduction

In Section 2.6 it was concluded that dedicated RF energy harvesting was the most suited energy harvester for the target application. Figure 5.1(a) illustrates a typical RF scavenged WSN network where each WSN harvests energy from an RF source and converts the captured electromagnetic energy into electrical DC power. This DC power is locally stored in a capacitor or battery and re-used as power supply when required. Besides delivering energy, the RF source can also serve as a communication hub and provide a system clock by modulating the RF carrier wave [58]. This will be discussed in more detail in the next chapter.



(a) (b)

Figure 5.1: (a) RF scavenged sensor network using a dedicated RF energy source and (b) system level block diagram of a wireless sensor node.

Recalling from Section 4.2, the power available to each WSN is ideally described by

$$P_{av} = \left(\frac{\lambda}{4\pi d}\right)^2 G_{RX} P_{EIRP} \tag{5.1}$$

where P_{EIRP} is the Equivalent Isotropic Radiated Power (EIRP), G_{RX} is the gain of the receiving antenna, λ is the wavelength and d is the distance from the radiating energy source. Note that although the available power decreases with the square of the distance, the area covered by the RF source *increases* by the same amount. This can be exploited in high density and heavily duty cycled WSN networks as a single RF source can power a large number of sensor nodes. Hence, apart from designing for efficient power transfer, the harvester must be designed for superior sensitivity which results in a large wireless range. In this work, a dedicated RF source is assumed which provides strong and reliable power at the 868 MHz European Industrial, Scientific and Medical (ISM) band. The maximum allowed radiated power in this band is 3.28 W EIRP [55].

Generating a sufficiently large voltage to activate the rectifier with a few μWs of power is the major design concern for long range RF harvesters as MOS transistors inherently are voltage-controlled devices. For example, the open-circuit terminal voltage of a 50 Ω antenna with -20 dBm available power is only 63.24 mV, much too low to overcome the threshold voltage of a standard CMOS transistor which lies around 400 mV in 90 nm technology.

Some solutions have been proposed to reduce the rectifier turn-on voltage by using (near) zero V_{TH} transistors [95, 96], gate pre-biasing [97] or V_{TH} self-

cancellation schemes [98–101]. However, the high fabrication costs, calibration phase or reverse current leakage make these solutions too expensive and impractical. Moreover, the majority of published CMOS rectifiers designed for long range RF energy harvesters are tested only in the electrical domain by using a signal generator as a well defined input power source with well defined impedance. Although this is a convenient way of measuring, it oversimplifies and neglects many aspects that can have a dominant effect on the end-to-end performance. Antenna characteristics such as impedance, efficiency and radiation pattern are a strong function of wavelength and hence the surrounding environment. By including an antenna in the measurements, the complete energy conversion from the EM domain to the electrical domain can be evaluated over distance and therefore include all performance-limiting effects such as misalignment, radiation efficiency, polarization and impedance mismatch. In addition, this allows for co-designing the antenna and rectifier for maximum performance as their interface is no longer constrained by the traditional 50 Ω characteristic impedance.

5.1.1 Antenna-Rectifier Interface Modeling

The rectifier essentially is a nonlinear circuit, meaning that a full wave nonlinear analysis such as in [95] is required to accurately predict the behavior of the rectifier over a wide range of input powers. Although this method offers an accurate model for the rectifier, it provides less insight in the antenna-rectifier optimization procedure and increases the complexity of the model as intuitive concepts such as impedance and frequency domain by definition can no longer be used. Furthermore, a nonlinear analysis requires knowledge of the implementation of the rectifier, and therefore does not allow for a general analysis that can be used for any antenna-rectifier topology. Therefore, the simplified linear interface model in Figure 5.2 is used in this work as it provides a very useful and intuitive understanding of the fundamental properties at the antenna-rectifier interface.

The interface model shows an equivalent circuit model of a rectifier with capacitive load connected to a loop antenna. The voltage induced by the electric field is represented by a Thévenin equivalent voltage source V_A and is a function of the radiation resistance R_{rad} and the available power P_{av}. The conduction loss resistance R_{loss} is related to the radiation efficiency. The reactive element jX_A represents the energy stored in the near-field and is inductive since the loop antenna is used below its first anti-resonance frequency. The rectifier output is also modeled as a Thévenin equivalent circuit. The input impedance of the rectifier is mainly capacitive where R_{rec} is the real part of

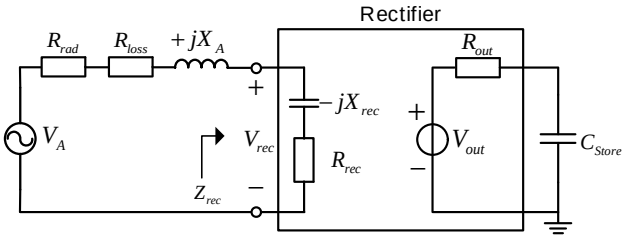


Figure 5.2: Antenna-rectifier interface equivalent circuit model.

the impedance and $X_{rec} = 1/(\omega C_{rec})$ represents the imaginary part. Both R_{rec} and X_{rec} can be assumed constant at low input power levels (i.e., around the power-up threshold) as the rectifier impedance will be dominated by the linear parasitic components [100].

By using an antenna with an inductive reactance, the rectifier capacitance can be compensated for without using other external components. Moreover, this LC combination also provides passive voltage boosting, which effectively increases the rectifier input voltage V_{rec} for the same input power [51]. As the rectifier input voltage V_{rec} determines the sensitivity of the RF energy harvester, an expression that relates V_{rec} to the interface impedance and the available power is derived below.
The input voltage swing at the rectifier can be written as

$$V_{rec} = V_A G_{V,boost} \tag{5.2}$$

where $G_{V,boost}$ is the passive voltage boost obtained from the resonating network. When $X_{rec} \gg R_{rec}$ and the interface is at resonance ($X_{rec} = X_A$), it holds that

$$G_{V,boost} = \left| \frac{V_{rec}}{V_A} \right| \approx \frac{X_{rec}}{R_A + R_{rec}} \tag{5.3}$$

When combining (5.2) and (5.3) and using $V_A = \sqrt{8 R_A P_{av}}$, the minimum required available power for a desired V_{rec} can be written as

$$P_{av} = \left(\frac{R_A + R_{rec}}{X_{rec}} \right)^2 \frac{V_{rec}^2}{8 R_A} \tag{5.4}$$

Equation 5.4 indicates that increasing X_{rec} is a very effective way of improving the sensitivity. The rectifier input resistance R_{rec} and reactance X_{rec} depend on the rectifier implementation. In reality, the input power dependence of R_{rec} and X_{rec} reduces the passive voltage boost at high input powers. This

effect is not included in this linear model but will be taken into account during circuit simulations in Subsection 5.2.3.

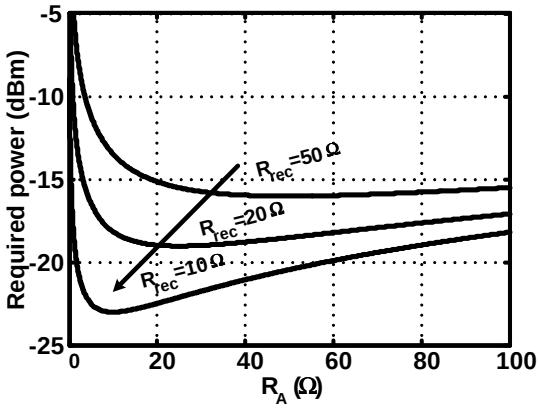


Figure 5.3: Calculated minimum required power to generate $V_{rec} = 0.4$ V vs. antenna resistance for various R_{rec} when $X_{rec} = 400\,\Omega$.

If for example $X_{rec} = 400\,\Omega$, the curves in Fig. 5.3 show the minimum required available power to generate $V_{rec} = 0.4$ V for three different values of R_{rec} as function of the antenna resistance. Evidently, a smaller R_{rec} lowers the required available power as it increases the passive voltage boost at the interface. The minimum point of each curve is when conjugate matching occurs. When $R_A > R_{rec}$, the antenna voltage V_A increases but the passive voltage boost becomes lower. Much more power is required when $R_A < R_{rec}$ as the antenna voltage becomes smaller and no benefit is gained from the passive voltage boost due to the current limiting R_{rec}. In this example, the minimum required available power to generate $V_{rec} = 0.4$ V for a 50 Ω interface equals -16 dBm (25 μW), while only -23 dBm (5 μW) is required for a 10 Ω interface, resulting in a 7 dB sensitivity improvement. This indicates the importance of a low resistive and high-Q antenna-rectifier interface. This design methodology can be applied to any rectifier and loop antenna implementation and can also be extended to rectifiers with a resistive load [102].

5.1.2 Self-Calibrating Impedance Control Loop

All antenna parameters described so far are dependent on wavelength and therefore also the surrounding environment. Moreover, the rectifier nonlinear input impedance also varies with frequency and input power. This makes the high-Q interface very sensitive to any variation caused by process mismatch,

variation in input power level or environment changes of on-body antennas. This has been extensively reported in various articles on printed flexible antennas [103–105]. To compensate for this, a control loop is added to tune the impedance such that a resonance is created with the antenna. The proposed RF energy harvester in Fig. 5.4(a) shows a feedback controlled voltage boosting and tuning network that compensates for variation at the interface that may occur in a realistic environment. As the antenna and rectifier reactances at the interface influence both the resonance frequency and the passive voltage boost at the interface, it is decided to compensate only for reactive variations. Also compensating the real part is less critical but would significantly increase the complexity of the control loop implementation. This way, the loop still improves the RF energy harvester robustness while taking advantage of the passive voltage boost obtained from the high-Q resonator.

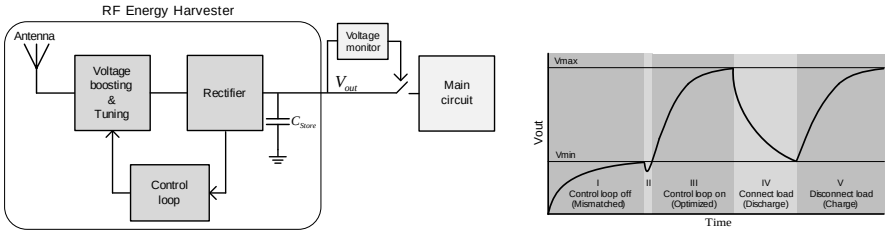


Figure 5.4: (a) System overview of the proposed RF energy harvester with control loop and (b) the output voltage waveform with zero energy initial condition (b).

To determine when enough energy is stored in the off-chip capacitor, a voltage monitor is used that can enable the main circuit. Fig. 5.4(b) illustrates the output voltage as function of time divided into five different regions for a constant input power. In Region I, there is no initial energy available to activate the control loop. The interface is therefore mismatched and the rectified voltage increases slowly with time. In Region II, Vout reaches the minimum voltage to activate the control loop. The output voltage slightly drops due to the power consumption of the control loop itself while optimizing the interface. Once the interface is optimized, the capacitor can be charged to V_{max} as indicated in Region III. In Region IV, the main circuit is connected and discharges the capacitor until V_{min} to reactivate the control loop. The energy available to the main circuit in this region equals $E = \frac{1}{2}C_{store}\left(V_{max}^2 - V_{min}^2\right)$. The load is disconnected again in Region V and the cycle repeats itself. This ensures optimum continuous operation after an initial startup. The additional

power and time required to generate V_{min} in Region I strongly depends on the rectifier and control loop implementation. This practical limitation will be discussed in more detail in Subsection 5.4.1.

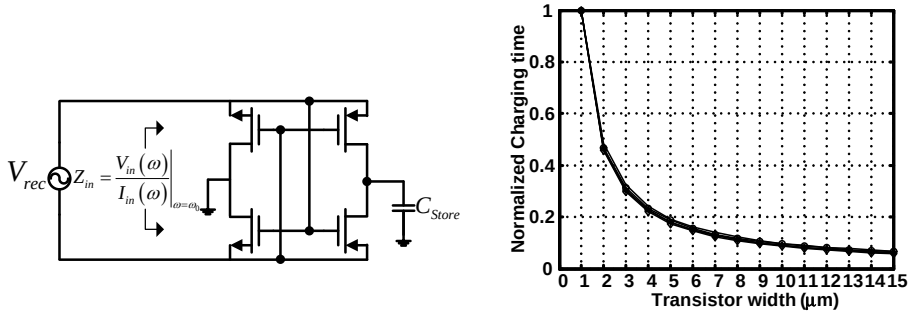
5.2 Rectifier Circuit Design

A rectifier usually is designed for maximum performance in steady state for a given load voltage to current ratio. In this work however, the steady state performance is of little concern as no additional energy can be added to the storage capacitor once the capacitor is charged to the rectifier peak input voltage. Instead, the transient behavior must be optimized to reach steady state as fast as possible. The circuit design of an RF energy harvester in TSMC 90nm CMOS technology is described in this section.

5.2.1 Single Stage Rectifier

The core of the harvester consists of a conventional cross-connected differential rectifier as shown in Fig. 5.5(a) [98, 99]. In this structure, the output voltage and common-mode gate voltage generated during rectification provide additional biasing which effectively reduces the required turn-on voltage. Due to this V_{TH} self-cancellation, the rectifier can be activated at lower input power levels than other similar topologies [106]. Another benefit of the differential rectifier is its symmetry as it cancels all even order harmonic currents. In practice, this implies that it is sufficient to only suppress the 3rd harmonic in order to prevent power loss due to re-radiation. This will be dealt with when discussing the antenna-rectifier co-design in Section 5.3.

When the rectifier operates in the subthreshold region, the steady state output voltage is independent of the threshold voltage and device dimensions. These parameters only affect the input impedance and charging time as noticed in [94]. The charging time however, is mainly determined by the storage capacitance and available power. The required transistor width is determined by analyzing the relative charging curve for different input voltages. In Fig. 5.5(b), the simulated 90% charging time vs. transistor width curves are normalized to the charging time for W=1 μm for a rectifier input voltage of 200-600 mV. Here, the PMOS width is 2.5 times larger than of an NMOS to compensate for the difference in hole and electron mobility. Note that the charging curves are nearly identical for all input voltages. This allows the designer to reduce the charging time by the same amount over a broad input voltage range for a given transistor width. In this work, a total transistor width of 6 μm (10



(a) (b)

Figure 5.5: (a) Rectifier circuit implementation with V_{TH} self-cancellation [98] and (b) simulated normalized charging time vs. transistor width for 200-600 mV input voltage.

fingers) with minimum gate length is chosen. Larger transistors do not significantly improve the charging time but will increase the input capacitance as the transistor capacitances dominate the rectifier impedance for $C_{store} \gg C_{par}$. The simulated voltage efficiency η_v of a single rectifying stage in this case is around 90%. The quasi steady state input impedance is calculated by the ratio of the FFTs of $V_{in}(t)$ and $I_{in}(t)$ at the operating frequency [62]. For an input voltage of 300 mV it is found that $Z_{rec} = 196.6 - j4896\,\Omega$.

5.2.2 Multi-Stage Rectifier

An output voltage higher than that of a single-stage rectifier ($\eta_v V_{rec}$) is achieved by cascading rectifying stages. Coupling capacitors ensure that the AC voltage is added in parallel while the rectified DC voltages of each stage are added in series (Fig. 5.6). The coupling capacitors are chosen to be 800 fF to avoid voltage division with the parasitic capacitors while keeping the chip area small.

Although the voltage gain of a cascade of N rectifiers increases linearly with N, it also linearly decreases the input impedance. Consequently, the antenna resistance R_A needs to be scaled down with N as well to obtain conjugate matching with $R_{rec,single}$, which decreases V_A for the same input power. The output voltage can be mathematically expressed as

$$V_{out} = V_A G_{V,boost} \eta_v N \tag{5.5}$$

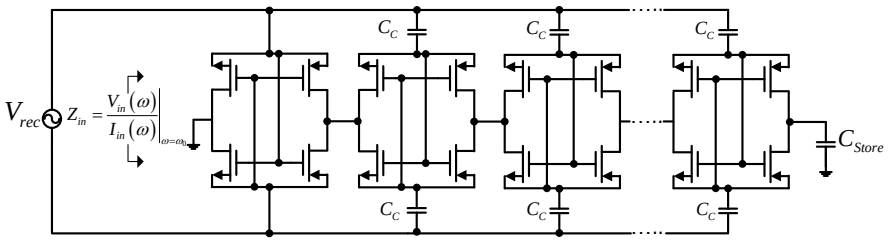


Figure 5.6: Multi-stage RF energy harvester with capacitive load.

Assuming conjugate matching with $X_{rec} \gg R_{rec}$ and using $V_A = \sqrt{8R_A P_{av}}$ leads to

$$V_{out} = \sqrt{8P_{av}\left(R_{rec,single}/N\right)}\,\frac{X_{rec,single}/N}{2R_{rec,single}/N}\,\eta_v N \tag{5.6}$$

The steady state output voltage for an N-stage conjugate matched rectifier with capacitive load can then be written as

$$V_{out} = \sqrt{\frac{2P_{av}N}{R_{rec,single}}}\,X_{rec,single}\,\eta_v \tag{5.7}$$

where $R_{rec,single}$ and $X_{rec,single}$ are the rectifier input resistance and reactance of a single stage, respectively. The output voltage scales with $\sqrt{N}$ when including the interface passive voltage boost. Note that although the rectifier voltage efficiency η_v actually drops with decreasing power, simulations show that $\eta_v \geq$80% when $V_{rec} \geq$0.15 V. Due to the large passive voltage boost, this voltage swing can be generated relatively easy even at power levels down to -30 dBm. Assuming $\eta_v >$80% is therefore a reasonable assumption for the power levels of interest in this work.

Fig. 5.7 shows the calculated output voltage following from (5.7) for an N-stage rectifier at conjugate matching with $P_{av} = -25$ dBm (3.16 μW), $\eta_v = 0.9$ and a total additional capacitance of 350 fF, representing the additional capacitance associated with bondpads, Electrostatic Discharge (ESD) protection and tuning capacitance (to be discussed later). The simulated 90% charging time is normalized to the charging time for N=1 to evaluate the increment with N. Note that the charging time increases rapidly with increasing N, which is mainly the result of the body effect of the NMOS transistors in the latter stages (assuming a standard process with $V_{bs,n} \neq 0V$). The number of stages therefore is highly dependent on the required output voltage and charging time (up-

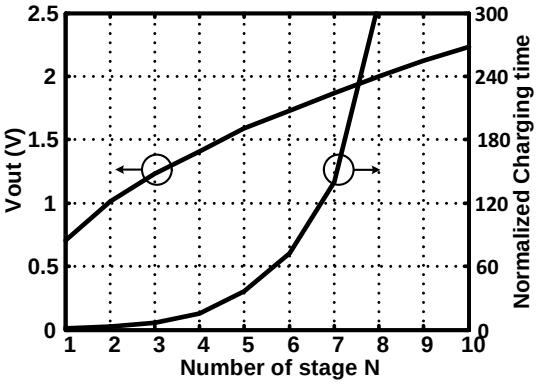


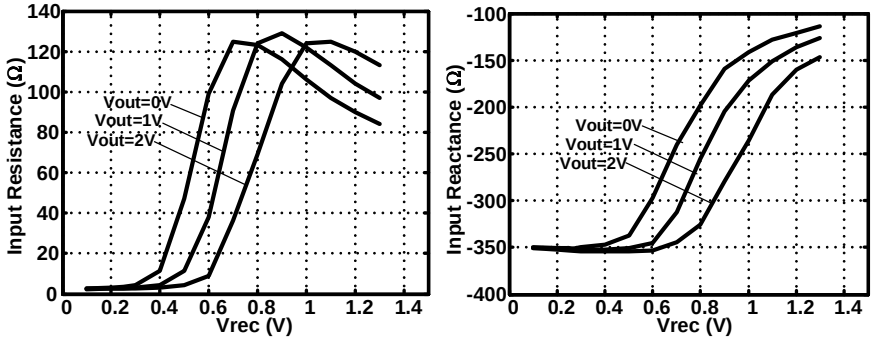
Figure 5.7: Calculated V_{out} and simulated normalized charging time vs. number of stages N for P_{av} =-25 dBm.

date rate) of the application. A single stage rectifier with P_{av} =-25 dBm takes approximately 60 msec to fully charge a 450 nF storage capacitance to 0.7 V. A 7-stage rectifier however, can generate 1.85 V but takes approximately 8.5 seconds. This may be good enough for a simple wireless temperature sensor with low update rate, but is too slow for real-time monitoring of for example an electrocardiographic (ECG) signal. Adding just one more stage (Vout=2V) would increase the charging time to 18.2 seconds. Hence, a high Q-network is preferred rather than using a large number of stages in order to improve performance. In this work, a rectifier structure with 5 stages is chosen to generate 1.5V with reasonable charging time at low power levels around -20 dBm.

5.2.3 Rectifier Input Impedance

The simulated input impedance of the 5-stage rectifier is depicted in Fig 5.8. In the subthreshold region ($V_{rec} < V_{TH}$), the input impedance is dominated by the parasitic capacitance of the MOS transistors. As V_{rec} increases, the magnitude of Z_{rec} decreases as the transistors start to conduct more current. This causes a transformation in the real part of $R_{rec} = \sqrt{|Z|^2 - X_{rec}^2}$ and results in a significant increase of R_{rec}. Nonetheless, an interesting fact is that both curves shift to the right when V_{out} increases due to the body effect and thereby partly compensates the increasing resistance.

Until this point in the design flow, an ideal independent voltage source has been used to simulate the rectifier input impedance. In reality, the inductive antenna limits the change in current and influences the input voltage



(a) Input resistance. (b) Input reactance.

Figure 5.8: Simulated input impedance versus V_{rec} and V_{out}.

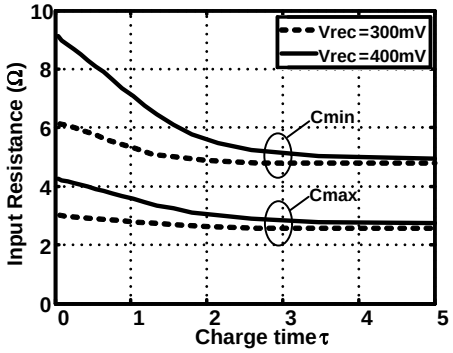


Figure 5.9: Simulated input resistance R_{rec} during a complete charging period for different V_{rec} and tuning capacitance.

during charging. To model this transient behavior, an inductance is added to the voltage source and is set to resonate with the rectifier reactance. Figure 5.9 shows the simulated input resistance during a 5τ charging period for two values of V_{rec} and the minimum and maximum tuning capacitance. Note that R_{rec} slightly decreases and is almost constant for $V_{rec} = 300$ mV. The variation in X_{rec} is only 3%. The interface impedance during charging is therefore relatively well defined at low power levels.

5.2.4 Switched Capacitor Bank

The impedance variations at the interface are compensated for by means of a binary-weighted capacitor bank parallel to the rectifier. The required tuning

capacitance step ΔC_{tune} is determined at low input power levels as the rectifier Q-factor is at its maximum in this region. Simulations show that a ΔC_{tune} of 2 fF is sufficient to maximize performance for power levels down to -30 dBm. As such a small capacitance is not available in this design kit, two custom designed metal-metal capacitors are used in series as illustrated in Fig. 5.10. The capacitor is realized using Metal 6 and Metal 7 stacked together with minimum width and spacing to minimize parasitics. With an area of 2.4x2.5 μm, the post-layout simulated capacitance is found to be 4 fF.

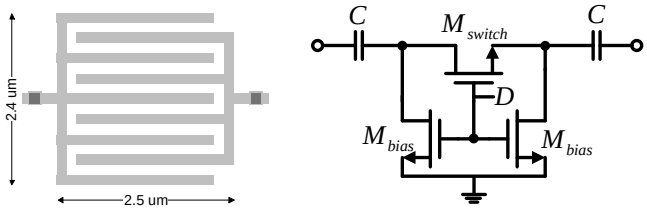


Figure 5.10: Unit capacitance layout and nMOS switch implementation.

Each unit cell consists of two capacitors, a main switching transistor (M_{switch}=1/0.1) and two small biasing transistors (M_{bias}=0.2/0.1) to enhance the Q-factor. With a voltage of 0.7 V as D='1', the post-layout Q-factor is >100 over all process corners. The on-off capacitive tuning ratio C_{on}/C_{off} in this case equals 2.2. The number of bits is determined by the desired tuning range and voltage boost. If too many capacitances are added in parallel to the rectifier, it reduces the available voltage boost at the interface. It was chosen to use a 7-bit capacitor bank consisting of 127 unit capacitor switches where $C_{max} = 256$ fF and $C_{min} = 116$ fF. This results in a tuning range in reactance of $340\,\Omega \leq X \leq 460\,\Omega$ for the rectifier and antenna as $X_{rec} = X_A$.

5.2.5 Reverse Current Leakage Reduction

The harvester's ability to store and hold the energy over a long period of time is another very important aspect that is not discussed often in the literature. This allows a WSN to operate and re-activate the control loop after a long period of time without sufficient power for rectification. To minimize the current leakage of the external storage capacitor itself, a polyester (PET) film capacitor is used with a minimum insulation resistance of 10 GΩ. Transistor leakage current is another form of leakage and is given by the subthreshold current. In case of a pMOS transistor, the subthreshold current is given by:

$$I_{SD,p} = I_0 e^{\frac{-V_{GB}}{nV_T}} \left(e^{\frac{V_{SB}}{V_T}} - e^{\frac{V_{DB}}{V_T}} \right) \tag{5.8}$$

where $I_0 = e^{\frac{|V_{TH}|}{nV_T}} \mu C_{OX} \frac{W}{L} V_t^2$ is the technology related characteristic current, μ is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W and L are the transistor width and length, $V_t = k_B T/q$ is the thermal voltage , V_{TH} is the threshold voltage, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage and n is the subthreshold slope [107].
The dominating leakage mechanism of the rectifier used in this work occurs when the rectifier input voltage swing is much smaller than the DC output voltage ($V_{rec} \ll V_{out}$). This for example can occur when the available input power suddenly drops with several dB. This results in a negative gate-source voltage of the pMOS transistors in the last stage and causes current to flow from the capacitor back into the rectifier. Hence, a solution is required to reduce this effect.

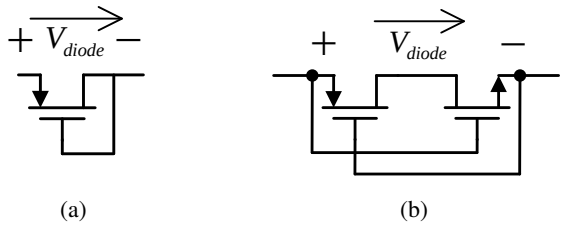


Figure 5.11: Conventional (a) and complementary (b) diode connected MOS transistor.

Conventional Diode-Connected MOS Transistor

By replacing the switching pMOS transistors in Fig. 5.5 with conventional pMOS diode-connected transistors as depicted in Fig. 5.11(a), the reverse current can be significantly reduced. When assuming that $V_{rec} \ll V_{out}$ and V_B=V_S (bulk is connected to source terminal) and using the sign convention in Fig. 5.11(a) (meaning in this case $V_{diode} < 0$ and $I_{diode} = -I_{SD,p}$), then the voltages of the conventional diode connected transistor are found to be $V_{GS,p}$=0 V and $V_{DS,p} = V_{diode}$. Substituting these results in Eq. (5.8) gives the following expression of the reverse current leakage for $V_{diode} < 0$:

$$I_{diode,conv,rev} = I_0 \left(e^{\frac{V_{diode}}{V_t}} - 1 \right) \tag{5.9}$$

For large negative values of V_{diode} , the reverse current leakage is mainly determined by the technology related characteristic current I_0 and the thermal voltage V_t.
For the forward current ($V_{diode} > 0$), the source and drain terminals exchange and thus become $V_{GS,p} = V_{DS,p} = -V_{diode}$ and $I_{diode} = I_{SD,p}$. Calculating I_{diode} then leads to

$$I_{diode,conv,fwd} = I_0 \left(e^{\frac{V_{diode}}{V_t}} - e^{\frac{V_{diode}(1-n)}{nV_t}} \right) \tag{5.10}$$

For $n = 1$, the forward and reversed current are thus given by the same expression.

Improved Complementary Diode MOS Transistor

When again looking at Eq. (5.8), it becomes evident that a much greater current leakage reduction for $V_{diode} < 0$ can be achieved if $V_{GB,p}$ can be made more positive than 0V. This can be realized with the complementary diode structure shown in Fig. 5.11(b). This circuit topology is proposed for memory cell applications [108], but can also be used for high-frequency rectification. For complementary pMOS and nMOS (symmetrical threshold voltages, identical subthreshold slopes and a size ratio between n and p-MOSFETs equal to the inverse of their mobility ratio) it follows for $V_{diode} > 0V$ that $V_{GS,n} = V_{diode}$ and $V_{DS,n} = \frac{1}{2}V_{diode}$. Furthermore, it holds for the pMOS that $V_{GS,p} = -V_{diode}$, $V_{DS,p} = -\frac{1}{2}V_{diode}$ and $I_{diode} = I_{SD,p}$. Since the two transistors are connected in series it holds that $I_{diode} = I_{DS,n} = I_{SD,p}$. As in the previous case, it is assumed that V_B=V_S. When substituting $V_{GS,p} = -V_{diode}$ and $V_{DS,p} = -\frac{1}{2}V_{diode}$ into Eq. (5.8), then the subthreshold current for $V_{diode} > 0V$ of the improved diode structure can be written as

$$I_{diode,comp,fwd} = I_0 \left(e^{\frac{V_{diode}}{nV_t}} - e^{\frac{V_{diode}(2-n)}{2nV_t}} \right) \tag{5.11}$$

For $V_{diode} < 0V$, it follows that $V_{GS,n} = \frac{1}{2}V_{diode}$ and $V_{DS,n} = -\frac{1}{2}V_{diode}$. Furthermore, it also holds that $V_{GS,p} = -\frac{1}{2}V_{diode}$, $V_{DS,p} = \frac{1}{2}V_{diode}$ and $I_{diode} = -I_{SD,p}$, which leads to

$$I_{diode,comp,rev} = I_0 \left(e^{\frac{V_{diode}(1+n)}{2nV_t}} - e^{\frac{V_{diode}}{2nV_t}} \right) \tag{5.12}$$

In order to better compare the current characteristics of the two solutions, we set n=1. It then follows that for both forward and reverse biasing, the subthreshold diode current of the conventional structure equals

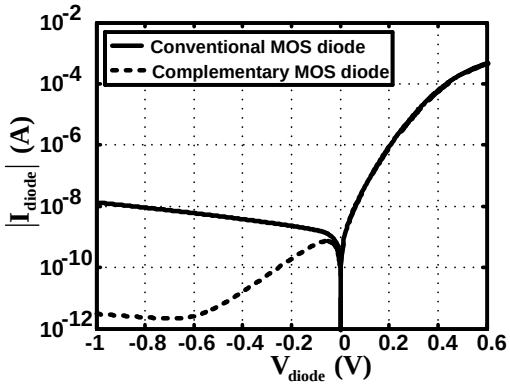


Figure 5.12: Simulated diode characteristics (diode voltage vs. absolute current) for a conventional and complementary MOS diode.

$$I_{diode,conventional} = I_0 \left(e^{\frac{V_{diode}}{V_t}} - 1 \right) \tag{5.13}$$

and for the improved complementary diode

$$I_{diode,complementary} = I_0 \left(e^{\frac{V_{diode}}{V_t}} - e^{\frac{V_{diode}}{2V_t}} \right) \tag{5.14}$$

Note the similarity between (5.13) and (5.14) for $V_{diode} > 0V$. The forward characteristics are almost identical for voltages roughly above $4V_t$ (~100 mV at room temperature) as the last term in (5.14) becomes negligible. To compensate for the slightly reduced current for $V_{diode} < 4V_t$, the transistor width can be made wider. The structure thus behaves as a single diode when forward biased.
For reverse biasing however, the current initially increases due to increasing $V_{DS,p}$ and then strongly decreases as $V_{GS,p}$ becomes more and more positive. Due to the symmetry of the circuit, exactly the opposite holds for the nMOS transistor. This causes the last term in (5.14) to become dominant and hence further reduces the leakage current when V_{diode} becomes more negative.

A combination of ultra-low V_{TH} and low V_{TH} transistors is sized to realize symmetrical devices with $V_{TH} = \pm 0.4$ V. The simulated I-V characteristics of the two diode implementations are shown in Fig. 5.12. The reverse current of the conventional MOS diode actually increases with a larger reverse bias voltage due to the body effect. The complementary diode however, strongly benefits from the exponential current reduction at reverse biasing. The reverse

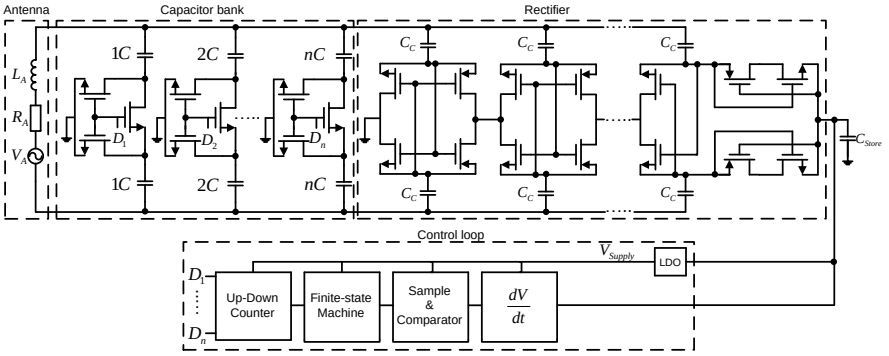


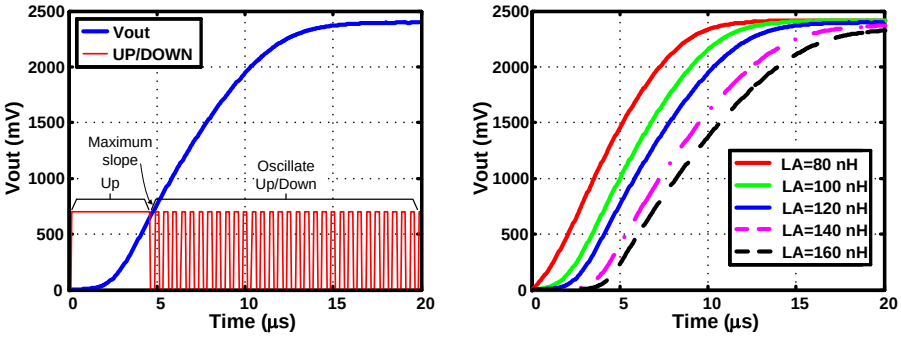
Figure 5.13: Multi-stage RF energy harvester with complementary MOS diode in the last stage and control loop.

current at $V_{diode} = -0.6$ V equals 6 nA for the conventional diode and only 2.6 pA for the complementary diode, providing more than three orders of magnitude in reverse current reduction.

5.2.6 Control Loop Implementation

The calibrating control loop consists of a 7-bit binary-weighted capacitor bank that is controlled by an up-down counter. The harvester initially charges the storage capacitor C_{store} to the turn-on voltage of the loop. Then the energy transfer to the off-chip capacitor is optimized by maximizing the slope of the load voltage. A possible control loop implementation in combination with a multi-stage rectifier including reverse leakage reduction is shown in Fig. 5.13. The slope information is obtained using a differentiating network. Subsequently, a sample & comparator stage compares the slope information with the previous sample and determines if the slope has increased or decreased. This information is fed to a finite-state machine that determines if the up-down counter should keep counting or change count direction. The output of the n-bit up-down counter is used to control a capacitor bank consisting of $(2^n - 1)$ unit capacitor switches at the interface. The number of bits is determined by the required tuning range and accuracy. A Low-Dropout Regulator (LDO) offers a stable supply voltage for the control loop.

The operating principle of the control loop is verified with (pre-layout) simulations. The up-down counter, finite-state machine and differentiator have been implemented at circuit level while the clock generator, LDO (0.7 V output) and sample & comparator are implemented using ideal blocks. The

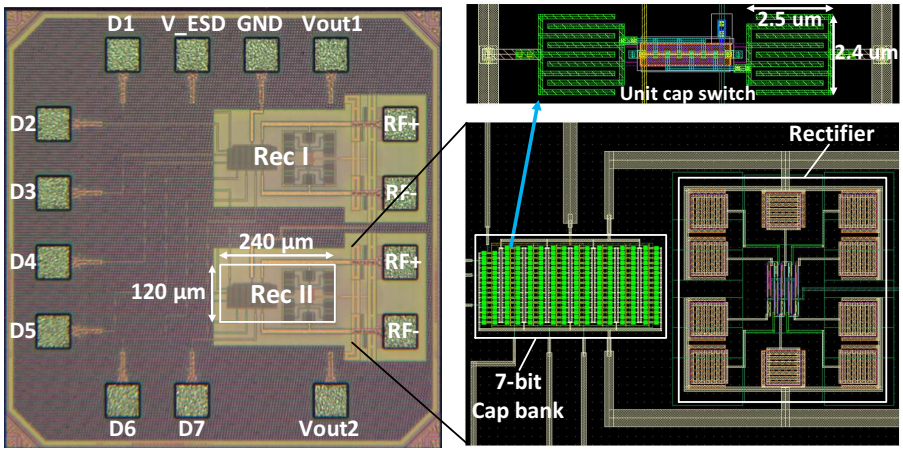


(a) (b)

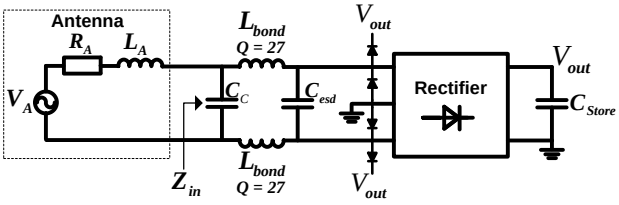
Figure 5.14: Simulated control loop calibration for (a) V_{out} and UP/DOWN count direction and (b) V_{out} for variations in L_A.

simulation results shown in Figure 5.14(a) are for P_{av}=-20 dBm and a relatively small load capacitance of 10 pF in order to reduce simulation time.
The 'UP/DOWN' count direction corresponds to the output signal of the finite-state machine and keeps counting up or down (depending on the initial direction) as long as the slope of V_{out} keeps increasing. The slope decreases when the capacitor bank has passed the optimum capacitance. In this case, 'UP/DOWN' turns from logic '1' to '0' and the loop inverts the counting direction. At the optimum capacitance code, 'UP/DOWN' oscillates between "1" and "0" at the clock frequency. This scheme ensures that small impedance variations, which may occur in a realistic environment, will be compensated for by the control loop, making the RF energy harvester very robust while it benefits from the passive voltage boost obtained from the high-Q antenna. This is demonstrated in Figure 5.14(b), where the antenna inductance is varied between 80 nH $\leq L_A \leq$ 160 nH to mimic antenna environment changes. The control loop is able to cope with these large variations despite the high-Q antenna network and maximizes V_{out} in each scenario.

As a proof of principle, the control loop is implemented off-chip using a micro controller. However, preliminary simulation results show that a similar mainly digital control loop can also be implemented on-chip. When optimizing for low leakage current, the average power of the control loop can be in the order of tenths of nW due to the relaxed requirements on the clock speed and accuracy (~kHz range). Once the loop is calibrated, it can be duty-cycled or turned off so that it is no longer loading the rectifier for very low input power levels.



(a)



(b)

Figure 5.15: (a) Chip microphotograph with layout details and (b) antenna-chip interface model with parasitic components.

5.2.7 Layout Design and Parasitic Components

Two rectifiers with the 7-bit capacitor bank have been implemented in TSMC 90nm CMOS technology. The first implementation (Rec I) uses the conventional differential rectifier shown in Fig. 5.6 while the second implementation (Rec II) includes the complementary diode in the last stage as depicted in Fig. 5.13. Since the input impedance is mainly determined by the rectifier parasitic capacitances, careful layout is essential. The high required quality factor of the IC's input impedance is achieved by optimizing the number of fingers and using sufficiently wide metal connections. A symmetrical and interdigitated layout further improves device matching. The top plate of each metal-insulator-metal (MIM) coupling capacitor is connected to the antenna side to prevent the larger bottom-plate parasitic capacitance from additionally shunting the capacitor bank.

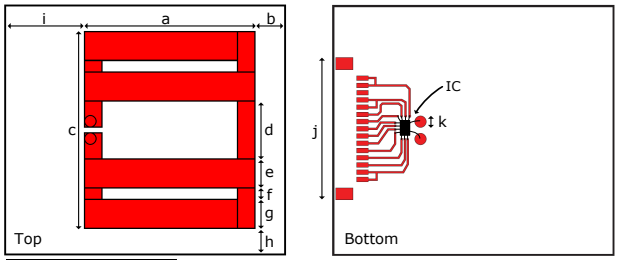
The RF bondpads are custom designed to minimize the parasitic capacitance and include ESD protection. The ESD diodes are biased at the lowest and highest generated voltage in the circuit (GND and V_{out}) as illustrated in Fig. 5.15(b). The extracted bondpad capacitance is 191 fF and is modeled with $C_{ESD} = 95.5$ fF as the two ESD diode capacitances are connected in series via the ground terminal. An external supply is used to bias the ESD control pins D1-D7. The bondwires to the antenna feedpoint are approximately 1.5 mm in length each and are modeled with an inductance of L_{bond} =1.5 nH with 0.3 Ω loss resistance. The bondwire mutual capacitance is modeled with $C_M = 25$ fF. It is important to note that the IC will be directly bondwired to the external antenna RF feed points. The PCB capacitance therefore is already embedded into the antenna input impedance and should not be used again in this model. The post-layout input impedance seen from the antenna feedpoint for V_{rec} = 300 mV is found to be $Z_{in,0} = 7.6 - j418\,\Omega$ for C_{min} and $Z_{in,1} = 4.3 - j310\,\Omega$ for C_{max}.

5.3 Antenna-Rectifier Co-Design

Given the post-layout simulated rectifier input impedance as described in the previous section, the required antenna[1] impedance is set to $Z_A = 4.3 + j350\Omega$ at 868 MHz. The exact value of the reactance is not very critical as the control loop will ensure resonance. The antenna resistance is set to $R_A = 4.3$ Ω in order to prevent that $R_A < R_{rec}$ as discussed in Section 5.1.1. The power loss due to the resistive mismatch at higher input powers is then compensated for by the increased available power.

The proposed antenna structure in Figure 5.16 is a compact rectangular loop antenna with additional short-circuited arms. These arms can provide fine tuning of the antenna impedance by for example varying parameter f. After optimizing all antenna parameters (dimensions, substrate thickness and permittivity), it is decided to use 0.5 mm thick GML 1000 substrate ($\varepsilon_r = 3.05$ and $\tan\delta = 0.003$) for high radiation efficiency. The chip is integrated on the backside of the antenna to minimize its effect on the radiation characteristics. The RF inputs are bond wired to vias (2 mm in diameter) that connect to the antenna feed point.

[1]The antenna-rectifier co-design described in this section is the result of a cooperation between Delft University of Technology, Holst Centre/Imec and Eindhoven University of Technology (TU/e). The antenna is designed by Shady Keyrouz from TU/e. More detailed design aspects can be found in his PhD thesis [109].



Parameter	mm
a	35.25
b	2
c	34
d	10
e	5
f	2
g	5
h	4.5
i	13.75
j	24.6
k	2

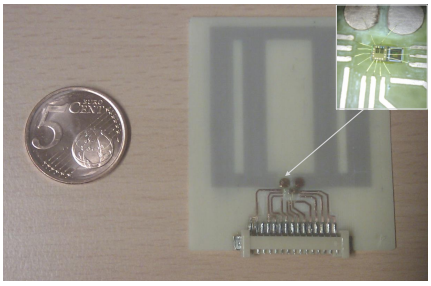
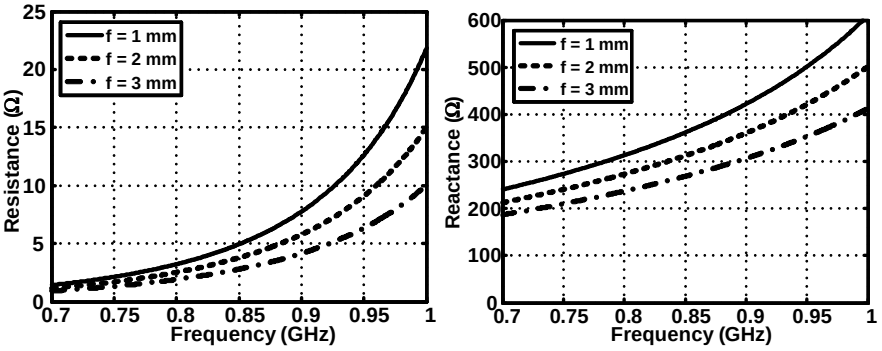


Figure 5.16: Proposed antenna structure and dimensions with integrated chip on the backside.

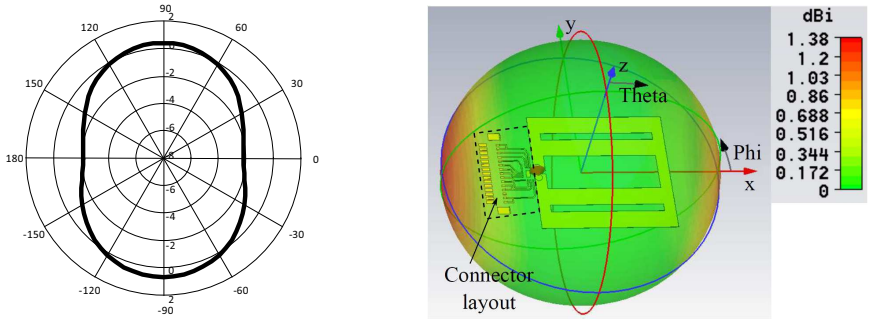


(a) (b)

Figure 5.17: Simulated antenna input impedance for different values of parameter f.

In this prototype, the control and output signals are connected to a measurement board via a connector. Once the control loop is completely integrated on chip and the connector is no longer required, it is expected that the antenna area can be scaled down further without significant performance loss.

The antenna impedance (Fig. 5.17) is simulated in CST Microwave Stu-



(a) (b)

Figure 5.18: (a) Simulated elevation plane radiation pattern (theta vs. antenna gain G_A in dBi) and (b) 3D directivity pattern.

dio using frequency, transient and transmission line solvers and all converge to approximately $Z_A = 4.4 + j328\Omega$, thereby ensuring a high degree of confidence in the simulation results. At the 3rd harmonic (2.604 GHz), the simulated antenna and rectifier impedance are $92.0 + j12.7\Omega$ and $1.78 - j124.5\Omega$, respectively. This causes a highly mismatched interface which attenuates the harmonic currents produced by the rectifier with 15 dB and thereby minimizes power loss due to re-radiation. In addition, the power contained at the 3rd harmonic is relatively small for the power levels discussed in this work.

Fig. 5.18 illustrates the elevation plane radiation pattern (theta vs. antenna gain G_A in dBi) and the 3D directivity to give insight in the directional dependence. The proposed antenna is horizontally polarized and has a maximum antenna gain of 0.659 dBi, corresponding to 84.7% radiation efficiency.

5.4 Experimental Results

The RF energy harvester performance first was measured in an anechoic chamber to mimic free space conditions. Then, the harvester was measured in a realistic office environment. The following measurement results are obtained using the harvester with rectifier II (complementary MOS diode) implementation unless stated otherwise. The RF energy harvester is positioned for optimal directional alignment and polarization with respect to the transmitting antenna. As the control loop is off-chip, its power consumption during calibration is not included in the measurements.

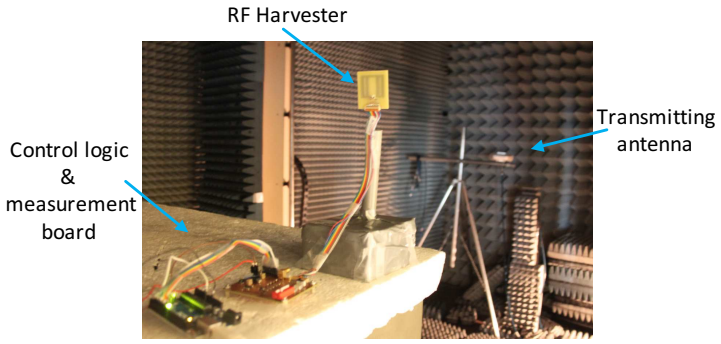
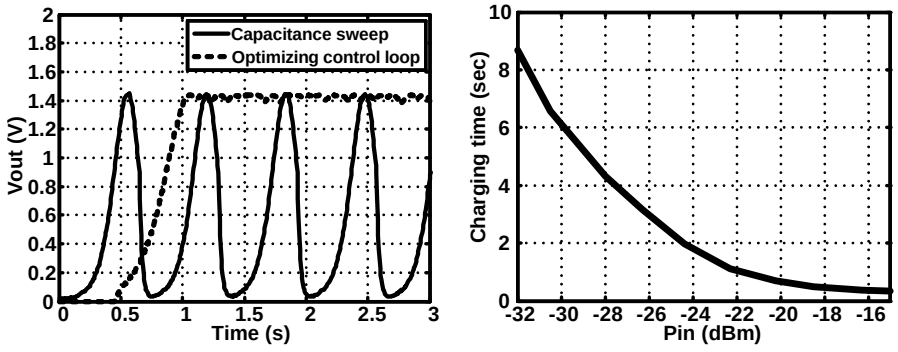


Figure 5.19: Measurement setup in anechoic chamber.

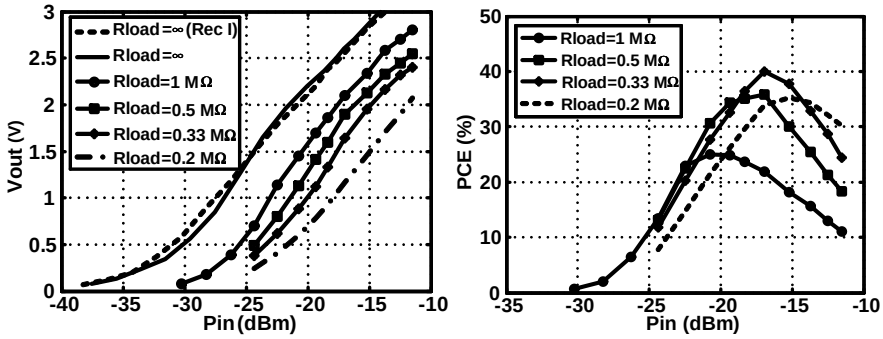


(a) (b)

Figure 5.20: (a) Measured V_{out} for capacitance sweep and optimizing control loop, R_{load}=1 MΩ and P_{in}=-20 dBm, (b) 10-90% charging time vs. P_{in}.

5.4.1 Measurements in Anechoic Chamber

The setup is calibrated at 868 MHz using two identical broadband log periodic antennas (HG824-11LP-NF) separated by 3.6 meter to ensure far-field conditions. Since the harvesting antenna dimensions are much smaller than the wavelength (a= λ/9.8 and c= λ/10.2), the antenna performance is included in the measurements by defining the input power as the maximum power available from an impedance and polarization-matched isotropic antenna (G_A =0 dBi). This power is determined by measuring the received power using the reference antenna at the harvester position and subsequently add the reference antenna gain to obtain $P_{in} = P_{av,iso}$. The measured power is within ±0.5 dB agreement with the theoretical available power calculated from (5.1).



(a) (b)

Figure 5.21: Measured (a) V_{out} and (b) power conversion efficiency for different R_{load} vs. P_{in}.

Fig. 5.20(a) shows the measured output voltage for an optimizing control loop and open-loop scenario (capacitance sweep) for Rload=1 MΩ and Pin=-20 dBm. During a capacitance sweep, the control loop is continuously counting from the minimum to the maximum capacitance value. Clearly, an optimum capacitance exists that corresponds to maximum power in the load. In the second measurements, the loop optimization is activated at 0.5 seconds and maximizes the power dissipation in the load.
The 10-90% charging time vs. Pin for a 450 nF load capacitance is shown in Fig. 5.20(b). Evidently, the charging time increases due to the decreasing input power and hence lower PCE.

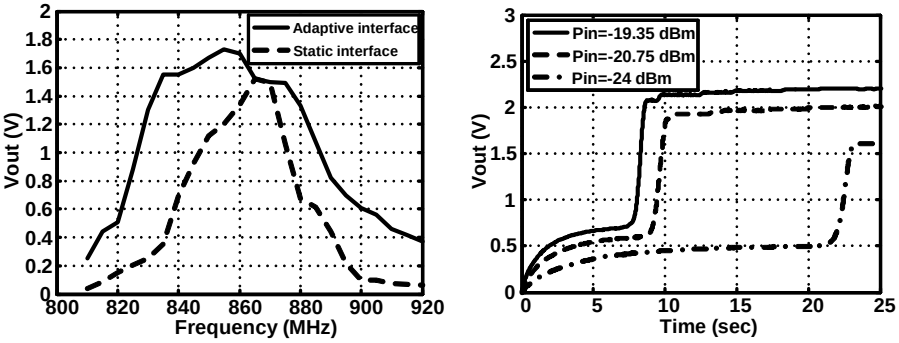
The measured output voltage vs. input power for different load resistances in Fig. 5.21(a) shows excellent sensitivity at low power levels. The unloaded performance of Rec I and Rec II are very similar and both are able to generate 1V with approximately -27 dBm input power. As the charging time scales linearly with capacitor size, Fig. 5.21(a) and 5.20(b) give a good indication of the available energy as a function of input power and time.

The efficiency of the RF energy harvester needs to be defined carefully. When the energy efficiency is defined as the ratio of the stored energy in the capacitor over the integral of the available power, it is required to specify the integration time. Hence, this efficiency definition becomes arbitrary and therefore difficult to compare in a fair way to previous work. Moreover, the energy efficiency approaches 0% for a long integration time as no additional energy can be stored when the capacitor is fully charged.

In this work, the RF-DC power conversion efficiency (PCE) is defined using a resistive load

$$PCE = \frac{P_{load}}{P_{av,iso}} = \frac{V_{out}^2}{R_{load} P_{av,iso}} \tag{5.15}$$

Figure 5.21(b) shows that the PCE peaks around -17 dBm with a maximum of 40% for a load resistance of 0.33 MΩ. This includes all losses of the antenna, interface and rectifier. For more details on the optimum load resistance, the reader is referred to Appendix A.



(a) (b)

Figure 5.22: (a) Measured frequency response for R_{load}=1 MΩ and P_{in}=-20 dBm, (b) minimum P_{in} for zero energy initial condition for V_{min}=0.5, 0.6 and 0.7V.

The harvester frequency response is obtained after calibrating the setup over frequency and is depicted in Fig. 5.22(a) for two scenarios. In the first scenario, the control loop is active and adapts the antenna-rectifier interface. The -3 dB bandwidth in this case is approximately 60 MHz for a 1 MΩ load resistance and -20 dBm input power. The maximum output peaks at 855 MHz, slightly lower than the 868 MHz used for the measurement in this work. To compare this to a static antenna-rectifier interface, a second measurement is performed where the capacitor bank is tuned to maximize the output at the 868 MHz band. Evidently, the control loop more than doubles the bandwidth of the RF energy harvester compared to the static interface scenario.

In order to test the performance with zero initial energy stored in the capacitor (i.e. control loop is off, D='0'), three measurements are carried out to find the required initial startup power and charging time to reach the startup voltage of the control loop for V_{min}=0.5, 0.6 and 0.7 V. When $V_{out} > V_{min}$, the

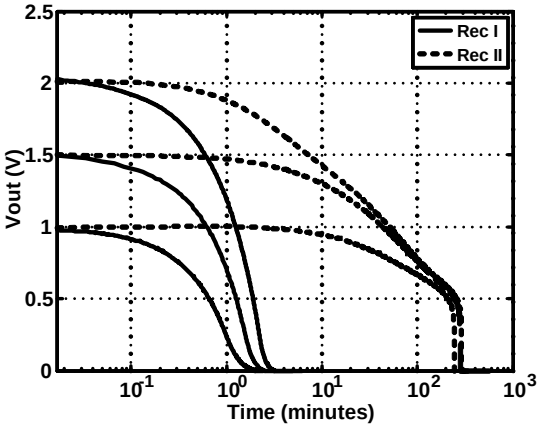


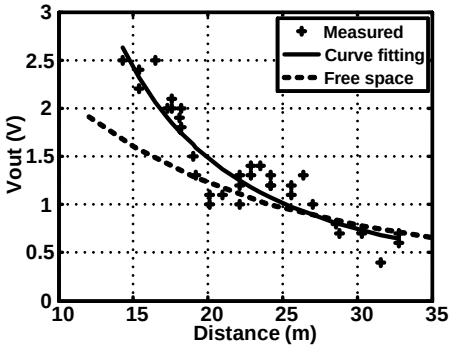
Figure 5.23: Measured discharge time for Rec I & II for $C_{store} = 350$ nF.

off-chip micro controller activates the control loop and optimizes the interface as shown in Figure 5.22(b). When for example V_{min}=0.5 V, the RF energy harvester needs an initial startup power of -24 dBm and 21.5 sec charging time in order reach V_{min} and to activate its control loop. This demonstrates the feasibility and limitations of a WSN under worst case conditions.

To test the energy storage capabilities of the harvester over a long period of time, the two RF harvester implementations with $C_{store} = 350$ nF initially are charged to three different values of V_{out}. Then the signal generator is switched off and V_{out} is measured as a function of time. As an example, the discharge curves in Fig. 5.23 show that for an initially stored voltage of 1.5V, the capacitor is discharged to 0.5V after approximately 75 seconds for Rec I. The harvester implementation with Rec II is able to store the energy significantly longer. The discharge time to 0.5V for the same initial voltage is now more than 4.1 hours, which is nearly 200 times longer than the harvester implementation with Rec I. This greatly improves the functionality and practical use of the RF energy harvester in a WSN and demonstrates the advantage of using the proposed complementary diode.

5.4.2 RF Energy Harvesting in a Realistic Environment

To test the harvester in a realistic environment, a 1.78W EIRP dedicated RF source at 868 MHz was used to measure V_{out} versus line-of-sight distance in an office corridor for a capacitive load. Fig. 5.24(a) illustrates the measured data points with curve fitting and the theoretical V_{out} in free space calculated from the measured sensitivity in Fig. 5.21(a). On average, the performance



(a)

(b)

Figure 5.24: (a) Measured output voltage vs. distance for $P_{EIRP} = 1.78$ W and $C_{store} = 350$ nF and (b) line-of-sight measurement in office corridor.

is better than in free space condition for distances closer than 27 meters from the RF source. This may be explained by the waveguide effect of the corridor, where high power density waves reflect from the walls, floor and ceiling and contribute to the total available power. In this experiment, 1V could be generated at 27 meter distance. Due to limitations of the measurement equipment it was not possible to transmit at the maximum allowed radiated power of 3.28 W in the European ISM band, which would theoretically result in a 1.4x larger range.

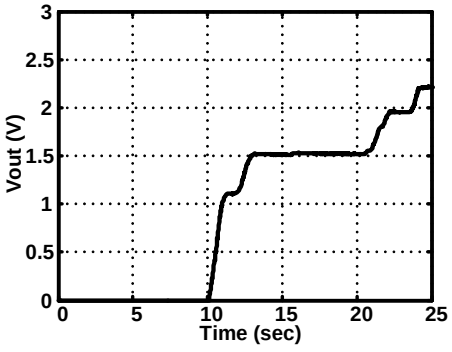


Figure 5.25: Ambient RF energy harvesting from a GSM-900 mobile phone at 2 meter distance.

The energy harvesting from ambient RF sources is demonstrated by measuring the output voltage when using a GSM-900 mobile phone from 2 meter

distance. Although the frequency and power levels varied greatly during a call (peak power levels of -4.6 dBm were measured between 886 MHz and 907 MHz), we observed that it is feasible to charge a capacitor to 2.2 V as demonstrated in Fig. 5.25.

5.4.3 Comparison with Previous Work

Table 5.1 shows a comparison with state-of-the-art CMOS RF energy harvesters. This work shows superior wireless range performance and demonstrates a -27 dBm sensitivity for 1V output in an anechoic chamber and 27 meter range from a 1.78 W RF source in an office corridor. Also a PCE of 40% at -17 dBm is amongst the highest reported in the literature. The rectifier and capacitor bank are implemented in standard CMOS technology, occupying only 0.029 mm^2 and the harvester requires no calibration procedure. Moreover, the proposed antenna is respectively 37% and 70% smaller than the ones used in [97] and [100], even though the operating frequency is lower.

5.5 Conclusions

The co-design of a CMOS rectifier and a small loop antenna for a highly sensitive RF energy harvester has been presented. First, a design methodology is described to optimize the antenna-rectifier interface by using a low resistive and high-Q interface. Subsequently, a 5-stage cross-connected differential rectifier with complementary MOS diode in the last rectifying stage is designed that significantly improves the harvester's ability to store and hold energy over a long period of time. A control loop with 7-bit binary-weighted capacitor bank compensates for variation at the interface while benefiting from the larger passive voltage boost to improve the sensitivity.

The chip is implemented in standard TSMC 90 nm CMOS technology, includes ESD protection and is directly mounted on the backside of the antenna. Measurements in an anechoic chamber at 868 MHz demonstrate an end-to-end maximum PCE of 40% and a sensitivity of -27 dBm to generate 1V across a capacitive load. In an office corridor, 1V could be generated from a 1.78 W RF source at 27 meter distance.

Table 5.1: Performance summary and comparison with previous work.

Parameters	**This work**	**T. Le '08 [97]**	**J. Yi '07 [95]**	**S. Mandal '07 [100]**	**G. Papotto '11 [101]**
Technology	90 nm	0.25 μm	0.18 μm	0.18 μm	90 nm
Die area	0.029 mm^2	0.4 mm^2	0.084 mm^2	n.a.	0.19 mm^2
Antenna area	21.9 cm^2	30 cm^2	n.a.	37.4 cm^2	no antenna
Frequency	868 MHz	906 MHz	900 MHz	970 MHz	915 MHz
Rectifier stages	5	36	24	2	17
Requirement	Control loop	External pre-charge	Zero V_{TH} transistor	-	Deep n-well
Sensitivity ($R_{load} = \infty$)	-27 dBm for 1V	-22.6 dBm for 2V	n.a.	-17.7 dBm for 0.8V	-24 dBm for 1V
Measured distance	27 meter @ 1.78 W	15 meter @ 4 W	1.1 meter @ 0.32 W	n.a.	none
Max PCE	40% @ -17 dBm	30%$^{(a)}$ @ -8 dBm	26.5 % @ -11 dBm	37%$^{(a)}$ @ -18.7 dBm	16.1% @ -15.83 dBm

CHAPTER 6

A 2.4 GHZ POWER AMPLIFIER FOR AUTONOMOUS WSNS

Energy scavenged Wireless Sensor Nodes (WSNs) usually require a small output power (<0 dBm) due to their short-range application and limited power budget. This makes the RF Power Amplifier (PA) design different from that of conventional PAs as the output power becomes comparable to the power consumption of the PA driver. In this chapter, a 2.4 GHz tuned switching PA and PA driver is proposed with an on-chip duty cycle calibration loop to enhance efficiency. A simplified model of the tuned switching PA is analyzed in Section 6.2 and verified with simulations. Then, the circuit design of the PA and its duty cycle calibration loop is described in Section 6.3. The experimental results of the fabricated prototype are discussed in Section 6.4.

6.1 Introduction

The combined power consumption of a PA and the PA driver becomes important for autonomous WSNs with relatively low output power levels. To quantify this, the definition of Global Efficiency (GE) can be used, which relates the fundamental RF output power to the combined DC power consumption of the PA and the PA driver:

$$\text{Global Efficiency} = \frac{P_{RFout}}{P_{PA,DC} + P_{Driver,DC}} \tag{6.1}$$

To show the significance of the PA driver power consumption, consider a 2.4 GHz switching mode PA with 200 fF input capacitance. For a 1.1V nominal supply, a substantial 580 μW of driving power is required when considering

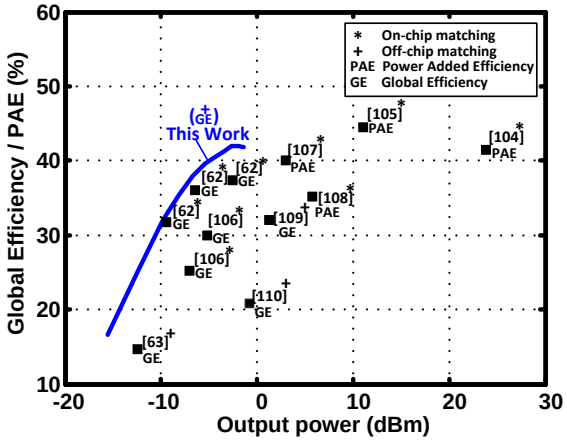


Figure 6.1: Survey of 2.4 GHz CMOS PA global efficiency/power added efficiency vs. output power.

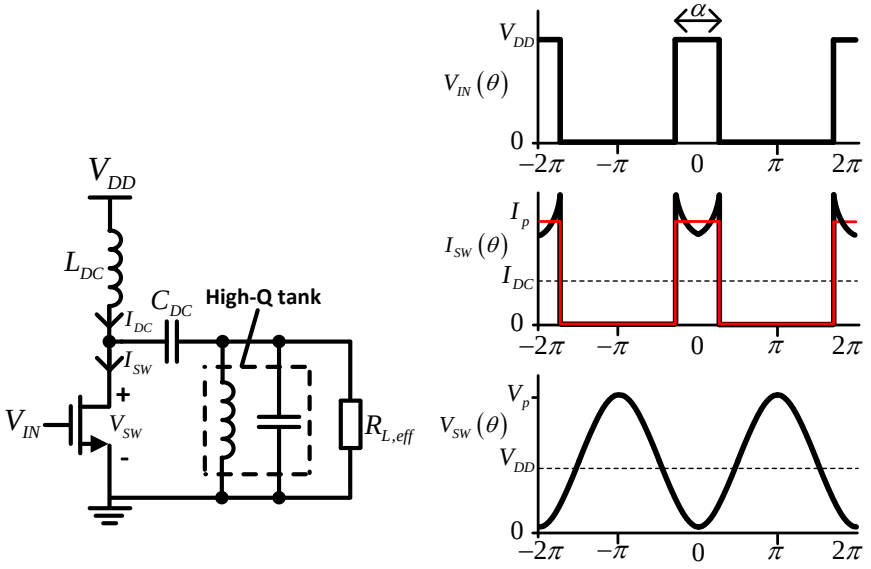
that the switching power of a single CMOS inverter is given by $P_{Driver,DC} = C_{PA}V_{DD,driver}^2 f$. When assuming P_{RFout} =500 μW (-3 dBm), this would result in a maximum global efficiency of only 46.2%, even when assuming a 100% drain efficiency ($P_{RFout}/P_{PA,DC}$). This becomes evident when looking at Figure 6.1, which shows a performance survey of recently published 2.4 GHz CMOS PAs [64, 65, 110–116]. As expected, a clear reduction in global efficiency is observed with decreasing output power.

Some efforts have been made to design low output power PAs for WSN applications. Class-E PAs can have good efficiency at high output power, but are challenging to design for <0 dBm output power due to the impractical matching network component values or low supply requirements [117]. A Class-F PA with 28% global efficiency at -20 dBm has been reported in [118], but is operating at a much lower frequencies (315 MHz) and therefore requires lower driving power. Moreover, the class-F PA requires a large number of passive components for harmonic tuning.
For <0 dBm output power, class-D PAs are frequently used as they ideally can provide 100% drain efficiency, but also require a large driving power which reduces the global efficiency. This issue is addressed in [64], where the authors added an on-chip inductor to resonate with the PA input capacitance at the expense of increased chip area.

This chapter presents an alternative approach to the design of a 2.4 GHz switching PA by introducing an on-chip duty cycle calibration loop to increase the global efficiency at <0 dBm output power.

6.2 Tuned Switching Power Amplifier Modeling

In this section, a feasibility study is done on the tuned switching power amplifier as depicted in Figure 6.2(a). In this topology, the transistor acts as a switch that is controlled by a square wave input signal with a given duty cycle. The DC supply voltage is fed through a choke inductor L_{DC} and the load is DC-blocked with C_{DC}. A high-Q harmonic tank filter at the output filters out the fundamental RF signal. The effective load resistance $R_{L,\text{eff}}$ represents the resistance seen from the PA, which commonly is an impedance transformation network in between the PA and the antenna.
In order to design for a desired global efficiency and output power level, an equivalent circuit model needs to be developed to determine the required duty cycle d and switch resistance R_{SW}. The goal of such a model at this stage of the design is to provide a sufficiently accurate prediction that gives insight into the design tradeoffs and the feasibility. An exact, closed-form solution often requires extensive calculations or numerical analysis, which do not necessarily add to the intuitive understanding [119,120]. Therefore, some approximations are made to simplify the model.



(a) (b)

Figure 6.2: (a) Tuned switching PA and (b) approximated waveforms of the tuned switching PA.

6.2.1 PA Model Simplifications

The tuned switching PA depicted in Figure 6.2(a) includes an NMOS transistor which can be seen as a voltage controlled resistance R_{SW}. Following the analysis and simplifications made in [121], the voltage across the switch is assumed to be a sinusoidal signal due to the high-Q harmonic tank filter. This approximation becomes more accurate at low duty cycles and high loading resistances, which both correspond to a (desired) low output power level. When extending this reasoning, it shows that the current through the switch I_{SW} shows peaks at the edge transitions. This current waveform can be well approximated by a square wave of equal area as indicated in red in Fig. 6.2(b). The range of the model validity will be demonstrated later in Section 6.2.2.

The duty cycle is defined as $d = \frac{\alpha}{2\pi}$ as depicted in Fig. 6.2(b). When the NMOS transistor input voltage is high, then the switch voltage is at its minimum while the current through the transistor is at its maximum. This period is set by the duty cycle and equals $-\pi d \leq \theta \leq \pi d$. The DC current I_{DC} for a given duty cycle is thus given by

$$\begin{aligned} I_{DC} &= \frac{1}{2\pi}\int_{-\pi}^{\pi} i_{sw}(\theta)d\theta && (6.2)\\ &= \frac{1}{\pi}\int_{0}^{\pi d} I_p d\theta && (6.3)\\ &= dI_p && (6.4) \end{aligned}$$

The fundamental current component amplitude is given by

$$\begin{aligned} I_1 &= \frac{1}{\pi}\int_{-\pi}^{\pi} i_{sw}(\theta)\cos(\theta)d\theta && (6.5)\\ &= \frac{2}{\pi}\int_{0}^{\pi d} I_p\cos(\theta)d\theta && (6.6)\\ &= \frac{2\sin(\pi d)}{\pi} I_p && (6.7) \end{aligned}$$

The fundamental voltage component amplitude is simply equal to the supply voltage

$$V_1 = V_{DD} \qquad (6.8)$$

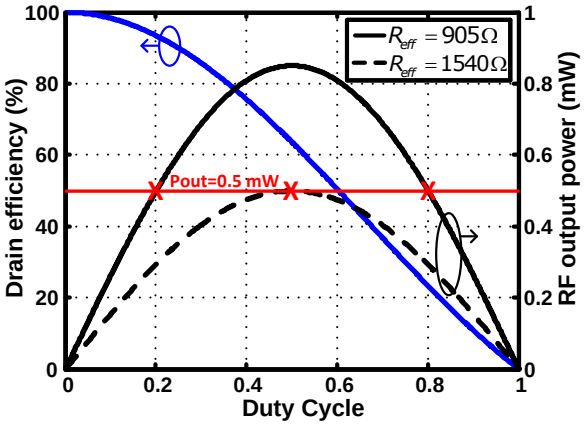


Figure 6.3: Ideal drain efficiency and RF output power for $V_{DD} = 1$V.

The fundamental RF power P_{RFout} then equals

$$P_{RFout} = \frac{V_1 I_1}{\sqrt{2}\sqrt{2}} = V_{DD} I_p \frac{\sin(\pi d)}{\pi} \tag{6.9}$$

When using $I_{DC} = dI_p$, the drain efficiency η_{Ideal} is obtained by writing

$$\eta_{ideal} = \frac{P_{RFout}}{V_{DD} I_{DC}} = \frac{\sin(\pi d)}{\pi d} \tag{6.10}$$

The drain efficiency thus follows a sinc function as depicted in Fig. 6.3 and can be increased by decreasing the duty cycle. The fundamental RF output power in terms of the effective load resistance and supply voltage is found by substituting $I_p = 2V_{DD}/R_{L,\text{eff}}$ into (6.9):

$$P_{RFout} = \frac{V_{DD}^2}{R_{L,\text{eff}}} \frac{2\sin(\pi d)}{\pi} \tag{6.11}$$

Equation (6.11) indicates that the maximum RF output power is obtained at d=0.5 and decreases when the duty cycle is either increased or decreased, assuming that $R_{L,\text{eff}}$ and V_{DD} are fixed. Since the required output power in this work is relatively low, it is acceptable to use low duty cycles in order to enhance the efficiency. A lower duty cycle also allows to use a smaller $R_{L,\text{eff}}$ for the same output power, which has the advantage that the required impedance transformation ratio to the 50 Ω antenna also becomes smaller. An example is depicted in Figure 6.3. When P_{RFout} is desired to be 500 μW (indicated by the red horizontal line) and V_{DD}=1.1V, then a duty cycle of d=0.5

requires an effective load resistance of $R_{L,\text{eff}}$=1540 Ω while only $R_{L,\text{eff}}$=905 Ω is required for d=0.2. Evidently, a duty cycle of 0.8 also corresponds to 500 μW RF power, but with much lower drain efficiency.

6.2.2 PA Switch Losses

The reduction in drain efficiency due to the power loss in the switch resistance R_{SW} can be estimated as described in [119]:

$$\eta_{drain} \approx \eta_{ideal} \frac{P_{RFout}}{P_{RFout} + P_{Switch}} \tag{6.12}$$

Therefore, an expression needs to be found of the average dissipated power in R_{SW} in terms of P_{RFout}. The average dissipated power in the switch resistance is given by

$$P_{Switch} = \frac{1}{\pi} \int_0^{\pi d} I_P^2 R_{SW} d\theta \tag{6.13}$$

while the fundamental RF output power is expressed as

$$P_{RFout} = \frac{1}{2} I_1^2 R_{L,\text{eff}} \tag{6.14}$$

Substituting (6.7) into (6.14) yields

$$P_{RFout} = \frac{2\sin^2(\pi d)}{\pi^2} I_p^2 R_{L,\text{eff}} \tag{6.15}$$

Rewriting for I_p^2 and substituting into (6.13) gives

$$P_{Switch} = \frac{R_{SW}}{R_{L,\text{eff}}} \frac{\pi^2 d}{2\sin^2(\pi d)} P_{RFout} \tag{6.16}$$

Finally, the drain efficiency including switch losses is found by substituting (6.16) and (6.10) into (6.12):

$$\eta_{drain} \approx \frac{\sin(\pi d)}{\pi d} \frac{1}{1 + \frac{R_{SW}}{R_{L,\text{eff}}} \frac{\pi^2 d}{2\sin^2(\pi d)}} \tag{6.17}$$

Figure 6.4 shows a surface plot of (6.17) for an effective load resistance of 1 kΩ where the duty cycle is varied between 0 and 1 and the switch resistance varies between 0 and 500 Ω.

For an ideal switch, this model suggests that the drain efficiency always increases for lower duty cycles. However, this is no longer the case when using a MOS transistor with a non-zero switch resistance. When the duty

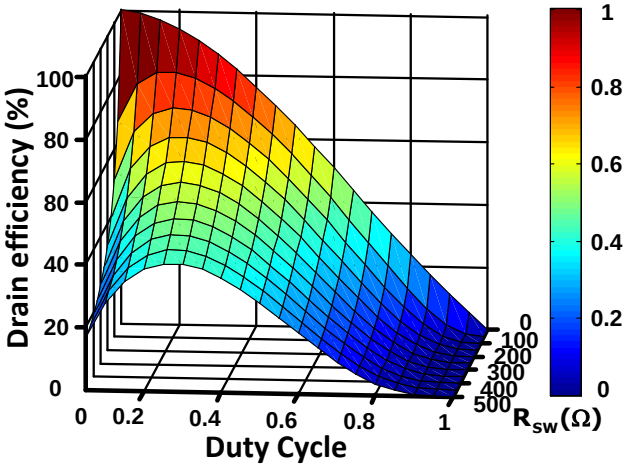


Figure 6.4: Surface plot of the calculated drain efficiency when varying the duty cycle and switch resistance for $R_{L,\text{eff}}$=1 kΩ.

cycle decreases, the power loss due to R_{SW} becomes relatively large because the fundamental RF output power approaches zero as indicated in Figure 6.3[1]. Therefore, the duty cycle should not be decreased too much in practice. For a non-ideal switch, an optimum duty cycle for maximum drain efficiency is found to be roughly between $0.2 \leq d \leq 0.3$, depending on R_{SW} and $R_{L,\text{eff}}$.

The accuracy of this model is verified with simulations using an ideal switch with a series resistance R_{SW} and $R_{L,\text{eff}}$=1 kΩ. Figure 6.5 (a) and (b) show that the model describes the drain efficiency fairly well for duty cycles below 0.5 and provides a more accurate model than presented in [122]. The efficiency for $d = 0.4$ slightly deviates since the sinusoidal drain voltage assumption becomes invalid. When R_{SW} approaches zero, the model predicts a lower efficiency than the values obtained with simulations (especially for duty cycles above 0.3). Also in this case, the voltage and current waveform approximations assumed in the analysis become invalid. Moreover, for an ideal switch there will be no overlap in current and voltage, which is not included in this model. This effect however is less severe at the low power levels and duty cycles discussed in this thesis, but can have a larger impact on the model accuracy for PAs with a significantly higher output power.

Figure 6.5 (c) shows the simulated drain efficiency versus duty cycle when the PA is implemented with a CMOS transistor with $R_{SW} \approx 220\ \Omega$. Note

[1]Note that this effect also decreases the efficiency at high duty cycles since the RF output power also decreases for $d > 0.5$.

that the duty cycle indeed has a rather broad optimum around $0.2 \leq d \leq 0.3$ as predicted by the theory. Hence, this simple model provides an intuitive understanding and is a useful tool for designing tuned switching PAs with a low duty cycle input.

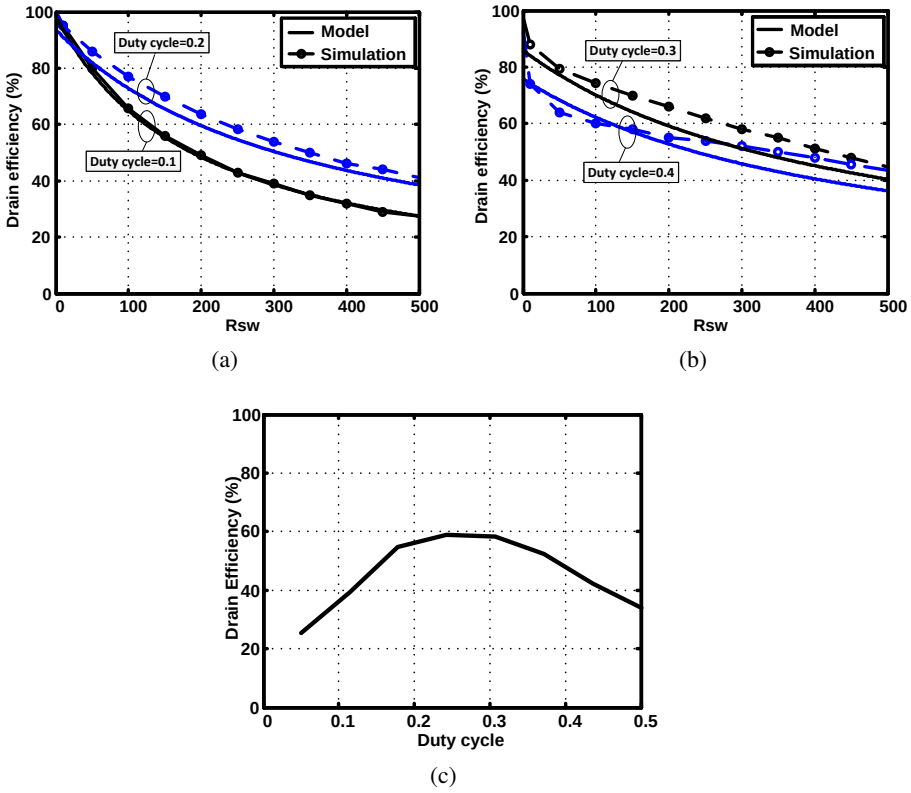


Figure 6.5: Drain efficiency model verification for switch resistances with $R_{L,\text{eff}}$=1 kΩ and (a) d=0.1 and d=0.2 and (b) and d=0.3 and d=0.4. (c) Simulated drain efficiency with CMOS implementation of PA.

6.3 Circuit Design

The circuit design of the tuned switching PA is split into three main parts. First, the PA and its load network are discussed. Subsequently, the PA driver circuit topology including duty cycle calibration is described. Then, the dimensions of the PA and the driver are optimized to obtain maximum global efficiency.

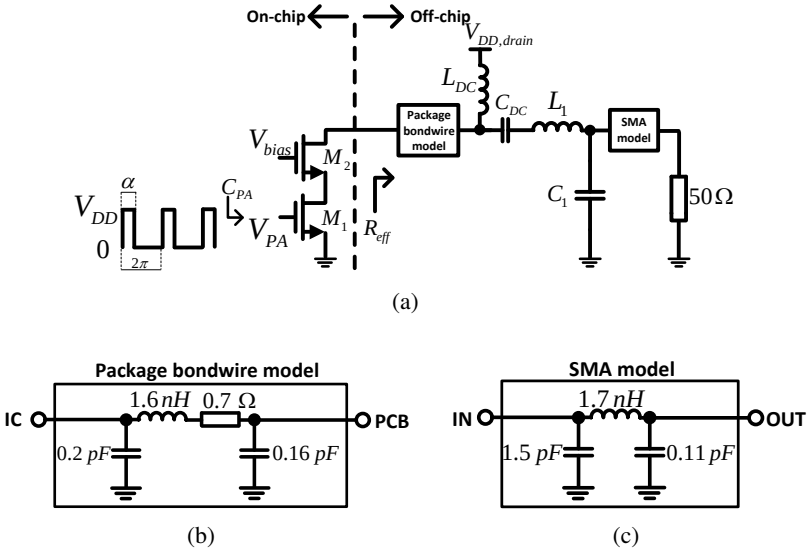


Figure 6.6: (a) CMOS tuned switching power amplifier with cascode transistor, (b) package/bondwire equivalent circuit model and (c) SMA equivalent circuit model.

6.3.1 Tuned Switching Power Amplifier

The core of the PA consists of a single-ended inductively loaded NMOS cascode transistor (see Fig. 6.6(a)). Transistor M1 is strongly driven by a rail-to-rail input voltage with duty cycle d and thus acts as a switch. The cascode transistor M2 limits the maximum voltage swing of M1 to improve reliability and also reduces the effective input capacitance C_{PA} by suppressing the Miller effect [123]. The output matching network provides impedance transformation to the 50 Ω antenna and consists of L_1 and C_1 tuned at the fundamental RF frequency. To minimize the parasitic losses associated with practical components, an off-chip matching network is utilized using high-Q inductors and capacitors. Both RF inductors are from the Coilcraft 0402HP series and SPICE models supplied by Coilcraft are used to simulate the frequency-dependent behavior of the inductors (not shown in schematic). The drain inductor L_{DC} is selected to be self-resonant at the operating frequency to provide maximum impedance. The matching inductor L_1 is selected for a high Q-factor and a high self-resonant frequency.

The package/bondwire equivalent circuit model shown in Fig. 6.6(b) is based on the extracted data from [124–126] for a quad flat no-lead (QFN) package and includes the bondpad and ESD capacitance (in total 150 fF),

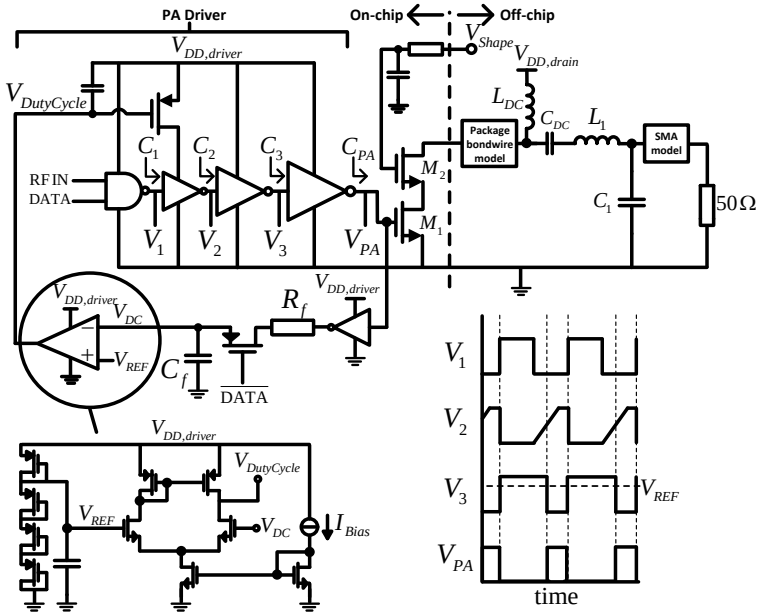


Figure 6.7: Proposed PA and driver with on-chip duty cycle calibration loop.

bondwire, package and PCB pad. The SMA connector equivalent circuit model (Fig. 6.6(c)) is provided by Imec/Holst Centre and includes the SMA footprint with tapering which is used on the test PCB. The 0402 SMD pad capacitance models and the PCB inductance traces are omitted in the schematic.

The effective load resistance $R_{L,\text{eff}}$ seen from the on-chip cascode transistor is used to set the desired output power for a given supply voltage. The combined channel resistance of M1 and M2 equals R_{SW}. The required values of R_{SW} and $R_{L,\text{eff}}$ are found during the global efficiency optimization in Section 6.3.3. To do so, first the PA driver topology and the corresponding C_{PA} needs to be known. This is the topic of the next section.

6.3.2 PA Driver and Duty Cycle Calibration Loop

The RF input duty cycle is set using the proposed duty cycle calibration loop shown in Fig. 6.7. The PA driver consists of a cascade of tapered inverters, where the first inverter has an additional PMOS transistor that controls the inverter's rise time. The second and third inverter act as a comparator and provide sufficient gain to drive the PA transistor. The voltage at the PA input V_{PA} is sensed with a small inverter and is fed to an RC low pass filter to ob-

tain the DC component, which is an indication for the duty cycle. Then, an NMOS differential pair compares the DC voltage to a reference voltage and subsequently controls the gate of the PMOS transistor. The reference voltage is set to $V_{REF} = \beta V_{Driver}$ by means of identical diode-connected PMOS transistors, where βV_{Driver} is a fraction of the PA driver supply voltage. Due to the negative feedback, the duty cycle is calibrated over PVT variations and therefore ensures robust operation.
The RF input is fed through a NAND gate which allows for On-Off Keying (OOK) with near-zero power consumption during a logic '0' transmission (except for the opamp current $I_{opamp} = 5\,\mu A$). A calibration memory is introduced by storing the loop control voltage on filter capacitor C_f during the OFF period in OOK modulation by means of a PMOS switch. This ensures fast startup after a '0'$\rightarrow$'1' transition and therefore allows for a high data rate.

The PA input capacitance C_{PA} consists of the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} of the NMOS switch, of which the latter is amplified by the miller effect. The gate and drain capacitances will change in time due to the switching of the gate and drain voltage, which makes the characterization of C_{PA} rather complex [123]. Nevertheless, the concept of an equivalent gate capacitance can be used that is proportional to the gate width of the NMOS transistor [127]. The effective PA input capacitance C_{PA} for a given PA transistor size can then be determined using circuit simulations and subsequently scaled with the transistor width W_1.
The total power dissipation of the PA driver can be estimated by

$$P_{Driver,DC} = (C_{PA} + C_1 + C_2 + C_3)\, f V_{DD,driver}^2 + I_{opamp} V_{DD,driver} \tag{6.18}$$

The cascade of tapered inverters are scaled for fast transitions and small input capacitance to keep the PA driver power consumption to a minimum. The sum of all PA driver capacitances then approximately equals $2C_{PA}$. Hence, the total power dissipation of the PA driver becomes

$$P_{Driver,DC} \approx 2C_{PA} f V_{DD,driver}^2 + I_{opamp} V_{DD,driver} \tag{6.19}$$

where $C_{PA} \propto W_1$.

6.3.3 Global Efficiency Optimization

The gate width of M1 is a crucial parameter to obtain a high global efficiency, as it involves a tradeoff between the drain efficiency and the PA driver power

consumption. The gate width of M2 however can be increased without increasing C_{PA}, although it also adds parasitic capacitance to the output matching network.

In order to optimize the gate width of M1, the global efficiency definition is slightly rewritten to include the drain efficiency:

$$\text{Global Efficiency} = \frac{P_{RFout}}{\frac{P_{RFout}}{\eta_{drain}} + P_{Driver,DC}} \tag{6.20}$$

Recalling from (6.17), the drain efficiency is given by

$$\eta_{drain} \approx \frac{\sin(\pi d)}{\pi d} \frac{1}{1 + \frac{R_{SW}}{R_{L,\text{eff}}} \frac{\pi^2 d}{2\sin^2(\pi d)}} \tag{6.21}$$

From (6.11), the effective load resistance $R_{L,\text{eff}}$ can be expressed as

$$R_{L,\text{eff}} = \frac{V_{DD,drain}^2}{2P_{RFout}} \frac{4\sin(\pi d)}{\pi} \tag{6.22}$$

while the switch resistance R_{SW} in deep-triode is given by

$$R_{SW} = \frac{1}{\mu_n C_{ox} \frac{W_1}{L_1} (V_{DD,driver} - V_{TH})} \tag{6.23}$$

The PA driver power consumption is given by (6.19) and also scales with W_1 as discussed in the previous section. If minimum length transistors are used with both $V_{DD,driver}$ and $V_{DD,drain}$ set to 1.1V and an RF output power of 500 μW is required, then the global efficiency can be plotted in terms of duty cycle and transistor gate width by substituting (6.23), (6.22), (6.21) and (6.19) into (6.20).

Figure 6.8 shows the surface plot of the calculated global efficiency and indicates that a maximum efficiency of 55% can be achieved when $0.25 \leq d \leq 0.35$ and $15\mu m \leq W_1 \leq 25\mu m$. As a lower duty cycle corresponds to a smaller required $R_{L,\text{eff}}$ and therefore a smaller impedance transformation ratio, it is preferred to set the duty cycle to d=0.25. This sets the required load resistance to $R_{L,\text{eff}}$=1089 Ω. After verifying with simulations, the optimum transistor width is slightly decreased and set to W_1=14 μm. Transistor M2 is made 28 μm wide with minimum length to reduce the effect of M2 on R_{SW} with acceptable parasitic capacitance at the output. This corresponds to $R_{SW} = 220$ Ω. The total post layout simulated gate capacitance of the PA and driver is 36 fF, resulting in 106 μW of switching power and 5.5 μW static power corresponding to the opamp power consumption, After taking

into account all parasitic components introduced by the pads, packaging and PCB parasitics, the matching network component values are given by L_{DC}=47 nH, L_1=3.9 nH, C_{DC} = 33 pF and C_1=2.4 pF.

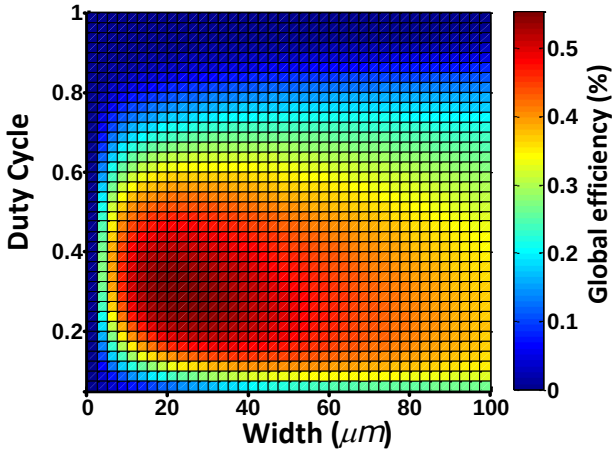


Figure 6.8: Surface plot of calculated global efficiency when varying duty cycle and the PA transistor width of M1 for P_{RFout}=500 μW and 1.1V for both V_{Driver} and $V_{DD,drain}$.

6.3.4 Pulse Shaping

The PA cascode transistor can be utilized to realize pulse shaping by using an off-chip pulse shaping circuit. The pulse shaping circuit is based on a simple integrator combined with two D-type flip flops with clear and preset and two comparators [128]. The circuit generates a triangular voltage which is synchronized with the DATA input and drives the gate of M2. The gate of the PA cascode transistor is decoupled with an on-chip capacitor and a small filter resistor. These components have a negligible effect on the pulse shape, but stabilize the gate voltage when pulse shaping is not used.

6.4 Experimental Results

The proposed PA is fabricated in TSMC 40nm CMOS technology and the layout area of the PA is 75x75 μm^2 as illustrated in Fig. 6.9. Extensive use has been made of power supply mesh unit cells for good current distribution and on-chip supply decoupling.

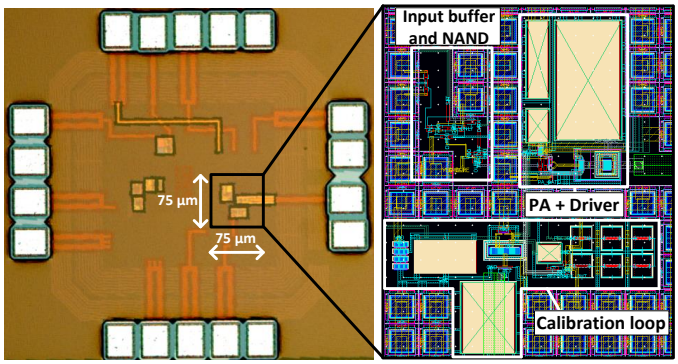


Figure 6.9: Chip microphotograph with layout details

6.4.1 Measurement Setup

The chip is bondwired to a 14-lead QFN package and mounted on a PCB for testing (see Fig. 6.10). The PCB is powered by batteries and has on-board power management with filtering and voltage regulators and contains the pulse shaping circuit. The RF signals are routed to SMA connectors and measured using a Teledyne Lecroy LabMaster 40 GS/s oscilloscope and a Rohde & Schwarz 8 GHz signal & spectrum analyzer.

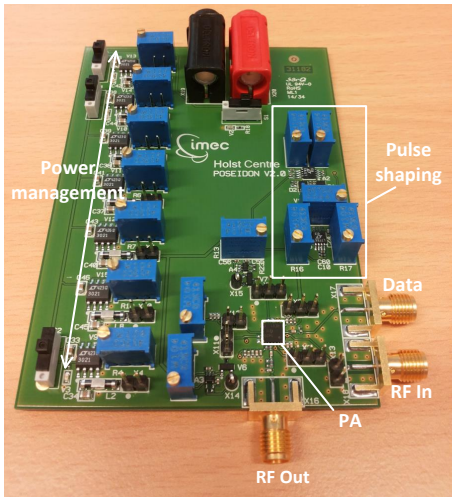


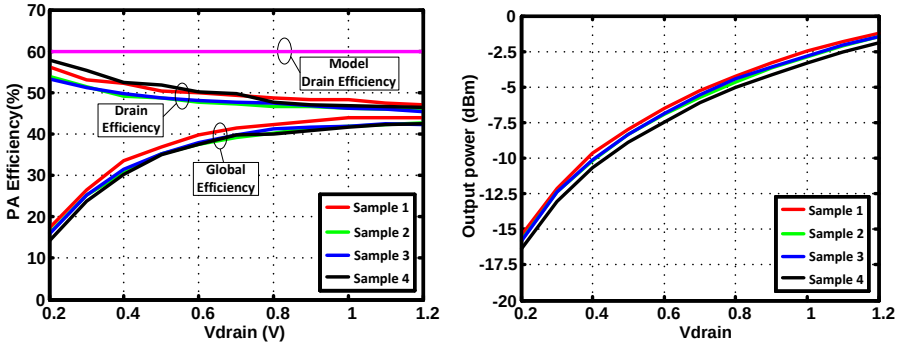
Figure 6.10: Photo of the packaged PA on test PCB.

6.4.2 Efficiency and Output Power

Figure 6.11(a) shows the measured drain and global efficiency versus the PA drain voltage at 2.44 GHz of four PA samples, each mounted on a separate test PCB. The drain efficiency shows a weak dependence on the drain voltage and decreases from approximately 55% to 45%, which indicates slightly better matching at low drain voltage because of the smaller impedance transformation ratio. The theoretical drain efficiency obtained from Eq. (6.21) does not depend on the drain voltage and thus is fixed around 60% for $R_{L,\text{eff}}$=1089 Ω and $R_{SW} = 220$ Ω, which was found in Subsection 6.3.3. This theoretical model assumes an ideal square wave input voltage with ideal matching components and thus does not take additional matching losses into account, which can explain the reduced efficiency found in the measurements. The global efficiency is around 40% at -5 dBm for all samples and increases to about 42% at -1.7 dBm, which compares favorably with other state-of-the-art PAs (see Fig. 6.1). The output power as a function of the drain voltage is depicted in Figure 6.11(b).

The measured power consumption of the PA driver including calibration loop is 110 μW from a 1.1V supply. An output power variation of less than 0.25 dB is observed over the 2.4-2.48 GHz ISM frequency band.

Figure 6.12 shows the measured output spectrum with the 2^{nd} and 3^{rd} harmonic, which are -51 dBc and -50.7 dBc, respectively.



(a) (b)

Figure 6.11: Measured (a) PA efficiency and (b) output power vs. drain voltage ($V_{DD,driver} = 1.1$ V) for four different samples.

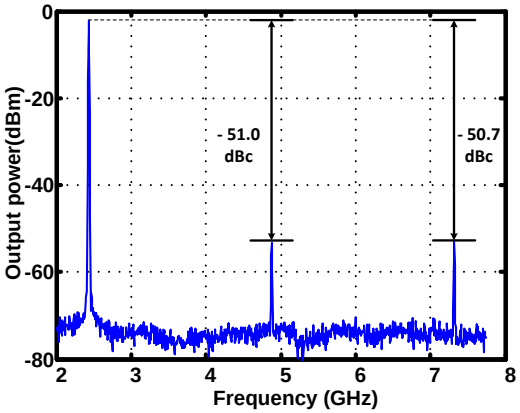


Figure 6.12: Measured output spectrum with 2nd and 3rd harmonic for a 2.44 GHz input

6.4.3 OOK and Pulse Shaping

A consecutive '0101' series is applied to the DATA input of the NAND gate to measure the OOK output in time and frequency domain. The transient waveform of a 40 Mbps OOK output is shown in Fig. 6.13. The 10-90% rise time is only 1.5 ns due to the fast startup calibration memory of the loop, whereas the fall time is 3.3 ns. The measured average power consumption in this case is 646 μW at -2.84 dBm output power.

As WSNs usually have lower data rates, the output spectrum of a 2 Mbps OOK output is shown in Fig. 6.14. Pulse shaping is achieved by driving the PA cascode transistor with an external triangular voltage which is synchronized with the DATA input to smooth the pulse edges. This reduces the -20 dBc bandwidth from 11 MHz to 6 MHz. To keep the output power constant for both the shaped and unshaped output, the shaped pulse width has been slightly increased to 700 ns.

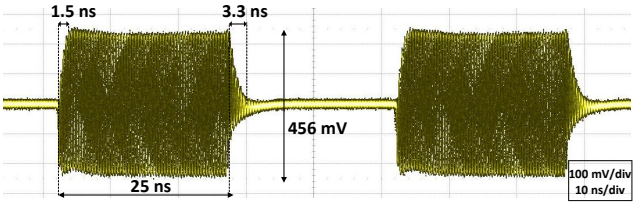
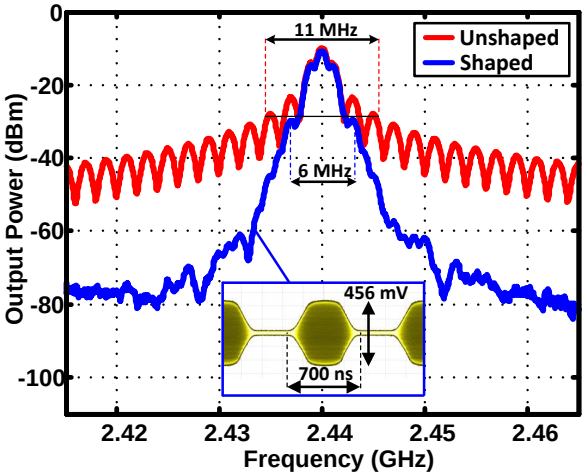


Figure 6.13: Measured transient output of 40 Mbps OOK modulation



(a)

Figure 6.14: Output spectrum of 2 Mbps OOK modulation (RBW=1 MHz).

6.4.4 Comparison with Previous Work

A performance comparison between state-of-the-art 2.4 GHz CMOS power amplifiers for low output power is given in Table 6.1. The proposed PA shows the highest global efficiency for output power levels below 0 dBm. Also the data rate compares favorably due to the short rise and fall time. Furthermore, the die area is significantly smaller than that of its competitors, but an external matching network is required.

6.5 Conclusions

The design of a high-efficiency 2.4 GHz tuned switching PA for <0 dBm output power has been presented to be used in low power autonomous WSN applications. From theoretical analysis it followed that the drain efficiency of an ideal tuned switching PA approaches 100% when he duty cycle approaches zero. When the switch resistance becomes non-zero, an optimum duty cycle needs to be chosen, depending on the effective load resistance and the switch resistance.

The global efficiency is optimized by finding a balance between the capacitive switching losses of the PA driver, the PA switch resistance and the RF input duty cycle. An on-chip duty cycle calibration loop has been proposed to set the duty cycle at 25%.

A PA propotype is implemented in 40nm CMOS technology and supports OOK modulation with pulse shaping capabilities. A global efficiency of 40% is achieved when delivering -5 dBm to a 50 Ω load. Due to the introduced memory in the duty cycle calibration loop, the rise and fall times are kept below 3.3 ns, making high data rate OOK modulation feasible.

Table 6.1: Performance comparison of 2.4 GHz CMOS power amplifiers.

	This work	[64]	[65]	[112]	[113]	[115]
CMOS Process	40 nm	65 nm	90 nm	0.13 μm	65 nm	90 nm
P_{RFout} (dBm)	-5	-2.5	-12.5	-5.2	3	1.2
Drain efficiency (%)	45.4	40	-	-	47	39
GE/PAE (%)	40^{GE}	37.3^{GE}	14.7^{GE}	30^{GE}	40^{PAE}	32^{GE}
Modulation	OOK	OOK BPSK MSK	OOK	FSK	-	OOK
Data rate (Mbps)	40	1	5	-	-	10
Off-chip matching?	Yes	No	Yes	No	No	Yes
Die area (mm^2)	0.0056	0.324	-	-	0.18	0.055

GE: Global Efficiency, PAE: Power Added Efficiency

CHAPTER 7

AN RF-POWERED DLL-BASED 2.4 GHZ TRANSMITTER

This chapter combines the accumulated knowledge and results of the previous chapters for the system integration of a compact RF-powered 2.4 GHz transmitter (TX) in 40 nm CMOS. The proposed transmitter is again depicted in Figure 7.1 for convenience. The TX utilizes the received dedicated RF signal for both energy harvesting as well as frequency synthesis. An RF energy harvester and nanowatt power management circuit captures, stores and monitors the harvested energy until enough energy is available for wireless data transmission. Then, a TX RF carrier is derived from the received RF signal by means of a Delay Locked Loop (DLL) and XOR-based frequency multiplier. The antenna load is subsequently driven by a tuned switching RF power amplifier with reduced duty cycle input for high global efficiency. For more details on the system level design and specifications, the reader is referred to Chapter 3.

The circuit design of each block in Fig. 7.1 is discussed first. Subsequently, the experimental results of the fabricated TX are extensively reported in Section 7.10. Conclusions are drawn at the end of this chapter.

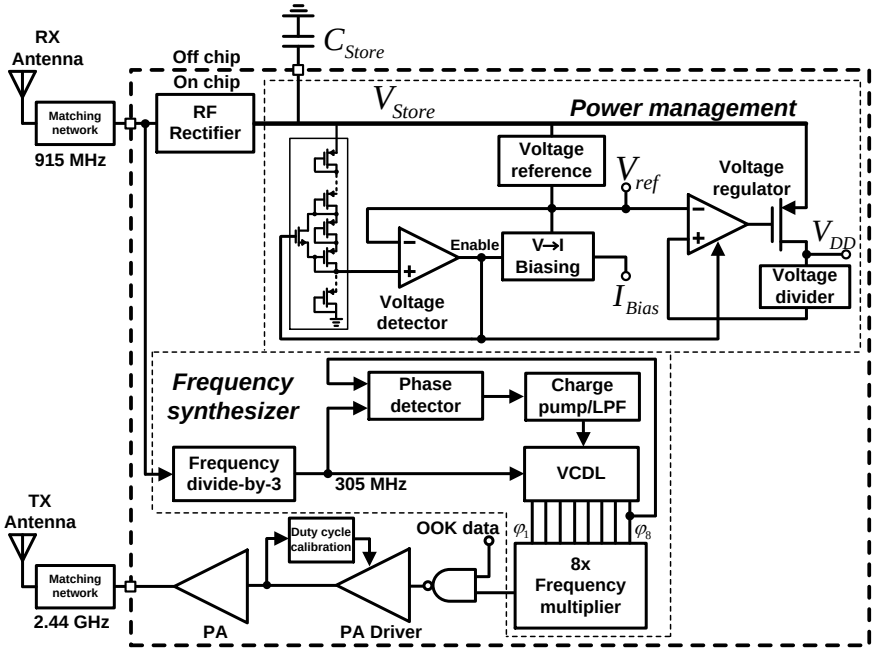


Figure 7.1: Proposed RF-powered DLL-based transmitter.

7.1 RF Energy Harvester

The RF rectifier circuit design is based on the design procedure described in Chapter 5 and consists of a 5-stage cross-connected differential rectifier. In contrast to the RF energy harvester with co-designed antenna described in Chapter 5, this RF rectifier is matched to a 50 Ω signal generator using an off-chip matching network and a single-to-differential converter using a TDK HHM1776B3 50:50 balun as depicted in Fig. 7.2[1]. This greatly simplifies the measurement procedure and calibration of this 40 nm prototype as there is no need for an anechoic chamber to accurately determine the available power. Both RF inductors are from the Coilcraft 0908SQ series and SPICE models supplied by Coilcraft are used to simulate the frequency-dependent behavior of the inductors.

[1]The decision not to implement the proposed control loop and co-designed antenna for the RF energy harvester implementation in 40 nm was made because of time constraints. A proof of principle of the control loop and the antenna-rectifier co-design was already demonstrated in Chapter 5 and thus gives an idication of the expected performance improvements once these features are included into the design.

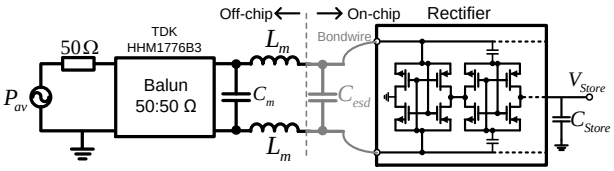


Figure 7.2: RF Rectifier with external matching network, RF balun and 50 Ω signal generator.

7.2 Voltage Reference

When the system is in harvesting mode, only the voltage reference and the voltage detector are enabled and therefore sink a continuous current from the RF energy harvester. These two circuits together with the rectifier therefore determine the overall system sensitivity and must be designed for minimum power consumption. For this reason, the CMOS voltage reference illustrated in Fig. 7.3 is used as all transistors operate in the subthreshold region for low voltage and low current operation.

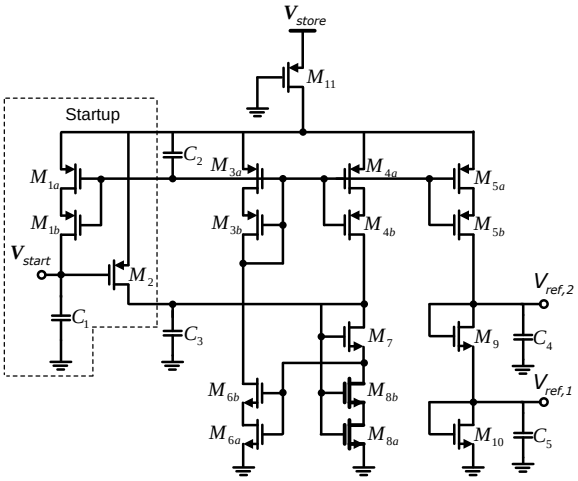
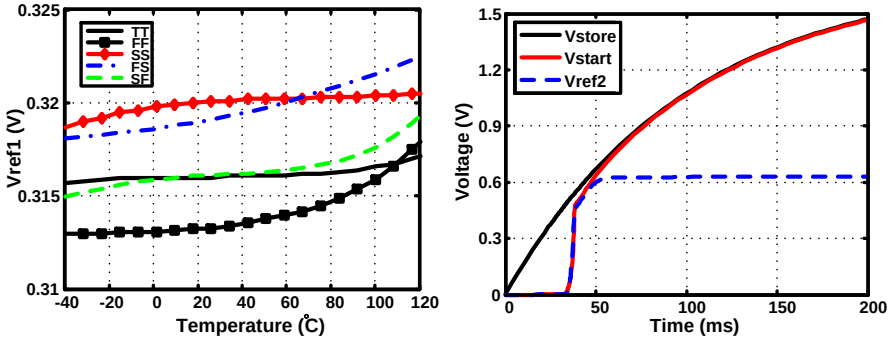


Figure 7.3: Voltage reference circuit implementation.

Self-cascoded transistors (denoted by subscript *a* and *b*) are used to reduce sensitivity to supply voltage variations without requiring additional biasing or increased supply voltage [129]. Temperature compensation is achieved by generating a current that is derived from a linear combination of nMOS V_{GS}



(a) (b)

Figure 7.4: (a) Simulated voltage reference $V_{ref,2}$ vs. temperature for five different process corners and (b) time domain voltage waveforms of V_{store}, V_{start} and $V_{ref,2}$.

voltages ($V_{GS8} = V_{GS7} + V_{GS6}$) and is subsequently mirrored into the diode-connected transistors M_9 and M_{10} to compensate their negative gate-source voltage temperate coefficient. The reference voltage $V_{ref,1}$ can be approximated to the threshold voltage difference between M_8 and M_6 [130]. The accuracy of the reference voltage thus is mainly determined by the matching properties of the transistor threshold voltages, which can be minimized with careful layout techniques. The difference in threshold voltage is increased by using a high threshold voltage transistor for M_8, indicated with a bold transistor symbol. Transistor M_9 is an exact copy of M_{10} with its bulk connected to its source and generates a second voltage of $V_{ref,2}$=2$V_{ref,1}$, which is used for various circuit blocks. A startup circuit is added consisting of M_1, M_2 and C_1 that injects an initial current into the drain of M_7 when V_{store} increases from zero volt. Once C_1 is charged to V_{store}, transistor M_2 is turned off and the startup circuit is switched off.

The simulated voltage reference $V_{ref,1}$ vs. temperature over five process corners is shown in Fig. 7.4(a). In the Typical-Typical (TT) corner around room temperature (20 ° C), a voltage reference is found of $V_{ref,1}$=316 mV. At room temperature, the voltage reference varies between 313.3 mV and 320.1 mV, corresponding to the Fast-Fast (FF) and Slow-Slow (SS) corners, respectively. The temperature coefficient $\left(V_{high} - V_{low}\right) / \left(V_{room}\left(T_{high} - T_{low}\right)\right)$ for the TT corner equals 25.7 ppm/°C for a temperature range of -40 to 125 °C. For other process corners, the temperature compensation is slightly off and thus results in a higher temperature coefficient, e.g., around 90 ppm/°C in the

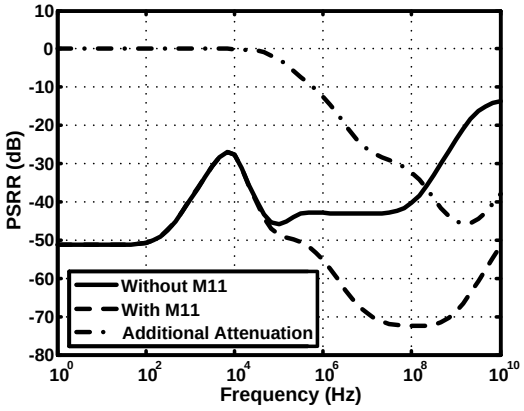


Figure 7.5: Simulated PSRR of the voltage reference with and without transistor M_{11}.

FF corner. Monte Carlo simulations show a mean voltage of $V_{ref,1}$=316 mV with a 3σ deviation of 30 mV over process corners and device mismatch.

Figure 7.4(b) shows the simulated time domain voltage waveforms of V_{store}, V_{start} and $V_{ref,2}$. It shows that $V_{ref,2}$ follows V_{start} until V_{store} is about 510 mV and subsequently settles to a supply independent reference voltage of 632 mV, exactly twice $V_{ref,1}$. The total simulated current consumption at V_{store}=1.2V is around 55 nA.

Transistor M_{11} is biased in the triode region and creates a LPF with the node capacitance at its drain to improve the Power Supply Rejection Ratio (PSRR) at high frequencies. The PSRR is simulated using the transfer function (XF) analysis from V_{store} to $V_{ref,2}$ with and without M_{11} and is depicted in Figure 7.5. There is no noticeable effect of M_{11} at frequencies below approximately 100 kHz. For higher frequencies there is a significant improvement in PSRR due to the additional attenuation of M_{11}. The additional attenuation at 50 MHz and 1.47 GHz is nearly 30 dB and 45.7 dB, respectively. The PSRR improvement comes at almost no cost because M_{11} can be kept small and has a negligible voltage drop due to the low current flowing through it. The bias current in the voltage reference can still self-calibrate when M_{11} is scaled large enough so as not to limit the bias current.

7.3 Voltage detector

The voltage detector needs to provide moderate gain and speed because C_{store} is charged relatively slowly. Therefore the simple open loop amplifier shown

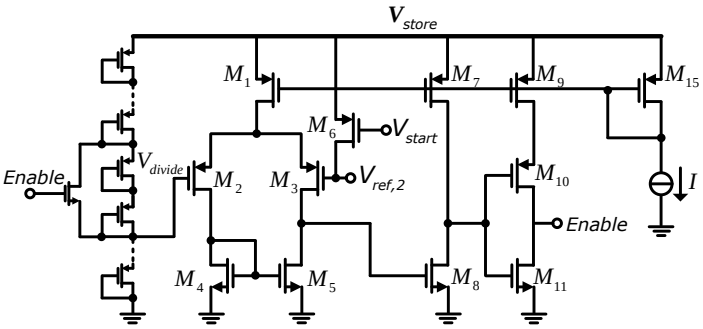


Figure 7.6: Voltage detector circuit implementation.

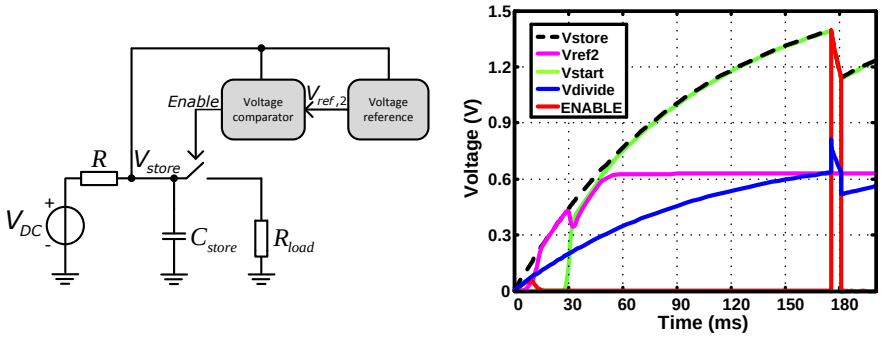
in Fig. 7.6 is used for this purpose. The PMOS input pair (M_2 and M_3) amplifies the voltage difference between $V_{ref,2}$ and V_{divide}, where V_{divide} denotes a scaled version of the storage voltage provided by nine or eleven PMOS diode connected transistors sized for low leakage current. Transistor M_8 provides further gain and drives a current starved inverter (M_9, M_{10} and M_{11}) to generate a binary 'Enable' signal with reduced dynamic power consumption. The following inverter buffers (not shown) are powered directly from V_{store}. When Enable='0', the detector enables the system when $\frac{5}{11}V_{store} > V_{ref,2}$, which corresponds to the maximum storage voltage V_H. When Enable='1', the detector disables the system when $\frac{5}{9}V_{store} < V_{ref,2}$, which corresponds to the minimum storage voltage V_L. To prevent the detector from enabling the system during a cold startup from zero volt, transistor M_6 is added that connects $V_{ref,2}$ to V_{store} to ensure $V_{ref,2} > V_{divide}$ during startup.

To test the combined functionality of the voltage detector and the voltage regulator, the test bench depicted in Figure 7.7(a) is used. An ideal DC voltage source with series resistor R is used to charge C_{store} from zero volt to model the output characteristics of the rectifier. The voltage detector and voltage reference are directly powered from V_{store} during charging. When $V_{store} \geq V_H$, the voltage detector closes the switch such that R_{load} starts to discharge C_{store}. The detector disconnects R_{load} when $V_{store} \leq V_L$ and the system returns to the charging mode.

The simulated time domain voltage waveforms are shown in Figure 7.7(b). Note that $V_{ref,2}$ is now first tracking V_{store} during startup instead of V_{start} as is the case of the stand-alone voltage reference shown in Fig. 7.4(b). However, when combined with the voltage detector, $V_{ref,2}$ is shorted to V_{store} by M_6 to prevent a false positive 'Enable' during startup. This also causes the small 'dip' in $V_{ref,2}$ shown in Figure 7.7(b) at approximately 400 mV because V_{start}

turns off transistor M_6.

Once $V_{divide} \geq V_{ref,2}$ (or equivalently $V_{store} \geq V_H$), the detector output 'Enable' becomes high and subsequently increases the reference level V_{divide} from $\frac{5}{11}V_{store}$ to $\frac{5}{9}V_{store}$ and connects the load resistor. After the lower voltage reference V_L has been reached, the system returns to charging mode as expected. The total simulated current consumption of the voltage detector equals 15 nA.



(a) (b)

Figure 7.7: (a) Test bench of voltage reference and voltage detector and (b) simulated time domain voltage waveforms of the storage capacitor, voltage reference and voltage detector.

7.4 Voltage-to-Current Converter

To generate the required bias currents for each circuit block, the voltage-to-current (V-I) converter depicted in Fig. 7.8 is utilized. The V-I converter is based on a two-stage negative feedback amplifier with resistive feedback. The output current flowing through M_{10} and R_f is ideally given by $\frac{V_{ref,1}}{R_f}$ and thus does not depend on supply voltage variations. The lower voltage reference $V_{ref,1} = 316$ mV is used instead of $V_{ref,2}$ because this requires a smaller R_f and thus saves considerable area. For a 2 μA bias current, the resistor value is set to R_f=158 kΩ and is implemented as a polysilicon resistor for good temperature behavior. As there is no stable current available to bias the V-I converter itself, transistor M_5 copies the current through R_f to adaptively bias the differential pair. A copy of this current is distributed to the various circuit blocks by M_4. Note that this self-biasing scheme creates a second feedback loop and thus should be checked for potential instability issues. In this case, the self-bias current is fed back by transistor M_5 into the common source node

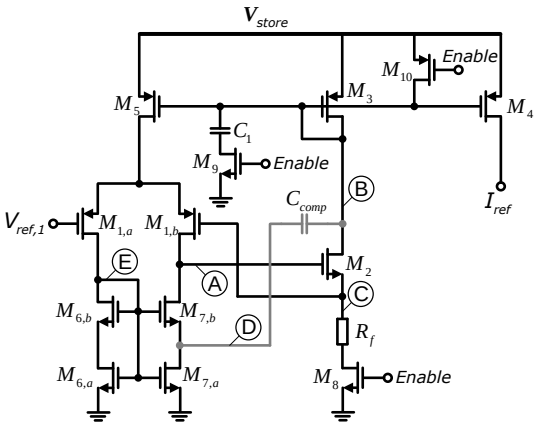


Figure 7.8: Voltage-to-current converter circuit implementation.

of the differential amplifier and thus results in a very low loop gain (<-30 dB over mismatch and process corners). The current is thus regulated by the differential pair that senses and adapts the voltage across R_f.

The current mirror load of the differential pair is implemented using self-cascoded transistors ($M_{6,a}$, $M_{6,b}$, $M_{7,a}$ and $M_{7,b}$). The self-cascoded transistor is a cascode of two transistors with both gates connected (e.g. $M_{6,a}$ and $M_{6,b}$). For the equivalent transistor to work in strong inversion, it is required that the bottom transistor $M_{6,a}$ works in the linear region and the top transistor $M_{6,b}$ works in strong inversion. The bottom transistor therefore acts as a source degeneration resistance that boosts up the output resistance (and thus loop gain). If both transistors have the same channel length and the top transistor is m times wider, the equivalent output resistance is given by $r_{o,eq} = (1+m)r_{o,6b}$ [129]. Although this output resistance is lower than that of a conventional biased cascode structure, the advantage is that $V_{DS,sat}$ is nearly the same as that of a single saturated transistor and therefore is a low-voltage solution. Furthermore, this structure does not require any additional biasing and allows for indirect frequency compensation by connecting C_{comp} from the drain of M_2 to the low impedance intermediate node between $M_{7,a}$ and $M_{7,b}$. Doing so prevents a right-half plane (RHP) zero, allows for a smaller compensation capacitance and also increases the unity gain frequency compared to conventional Miller compensation [131].

Transistors M_8 and M_{10} are used to ensure near-zero current consumption when the system is in harvesting mode (Enable=0). To ensure a fast startup behavior, transistor M_9 is added to initially pull down node B when the circuit

is enabled. Once the circuit is self-biased, M_9 and C_{gs1} have a negligible effect on the pole locations and stability because of the relatively high output impedance of the negative feedback amplifier.

The frequency and stability behavior is analyzed by finding the poles and zeros of the loop gain. The strong interaction however between the input and output voltage of the second stage makes it difficult to associate a pole with each node. For a derivation of all poles and zeros with the corresponding small signal model, the reader is referred to Appendix C. Only the dominant poles are discussed next.

The DC loop gain $L(0)$ is given by

$$L(0) = -\frac{g_{m1}g_{m2}r_{o1}R_f}{g_{m2}R_f + 1} \tag{7.1}$$

and equals -102. The dominant pole is roughly given by

$$p_1 \approx -\frac{1}{2\pi r_{o1}(\frac{C_{gs2}}{R_f g_{m2}+1} + C_{gd2})} \tag{7.2}$$

which equals -1.42 MHz. Notice that the feedback resistance R_f increases the input impedance at the input of the M_2 and thus effectively decreases the capacitance seen from node A with $g_{m2}R_f + 1$. The second pole location is approximately given by

$$p_2 \approx -\frac{C_{gs2} + C_{gd2}(R_f g_{m2} + 1)}{2\pi R_f \left(C_{gs1}C_{gs2} + C_{gd2}C_{gs1} + C_{gd2}C_{gs2}\right)} \tag{7.3}$$

and is located at -127 MHz.

The pole associated with the differential pair current mirror at node E is given by

$$p_3 \approx -\frac{g_{m6}}{2\pi C_E} \tag{7.4}$$

which corresponds to -8 MHz. Furtheremore, a zero is found at approximately

$$z_2 \approx -\frac{2g_{m6}}{2\pi C_E} \tag{7.5}$$

and is located at -16 MHz.

Stability simulations are done by placing a current probe between node A and the gate of M_2 to calculate the loop gain. Placing the probe between these nodes ensures that the influence of both feedback loops is analyzed. Simulations show that the uncompensated V-I converter already has a Phase Margin

Corner	PM (degree)	UGBW (MHz)	DC Gain (dB)	Iref (μA)
TT	60.54	67.01	38.4	1.96
SS	60.15	55.31	38.6	1.65
FF	61.48	82.53	38.2	2.46
FS	61.5	61.49	39.2	1.98
SF	59.89	70.09	35.3	1.92

Table 7.1: Simulated V-I performance over process corners.

(PM) greater than 60 degree because the second stage (M_2) is configured as a source follower and therefore does not further reduce the phase margin. For the final implementation (after layout) a small compensation capacitor of $C_{comp} = 170$ fF is used. Post-layout simulated performances like phase margin , Unity Gain Bandwidth (UGBW), DC gain and output current are shown in Table 7.1 for different process corners. All corners show a PM around 60 degree, a minimum UGBW of 55 MHz and a minimum DC gain of 35.3 dB. The output current I_{ref} is close to 2 μA for the TT, FS and SF corner. The worst case spreading of I_{ref} is about 22% due to the process tolerances of the feedback resistor. Although the various circuits should be able to handle this spreading, a 2-bit selection switch (not shown) has been added to adjust the bias current if necessary.

Figure 7.9 shows the simulated I_{ref} vs. temperature for five different process corners. The simulated temperature coefficient in the TT corner is 54 ppm/°C between -40 and 125 °C. The worst case temperature coefficient is found in the FS corner and equals 144.7 ppm/°C. The total current consumption of the proposed V-I converter equals 3 μA.

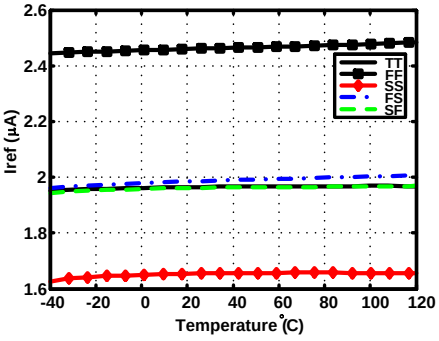


Figure 7.9: Simulated current reference I_{ref} vs. temperature for five different process corners.

7.5 Voltage Regulator

The circuit implementation of the voltage regulator is depicted in Fig 7.10. A two-stage opamp with PMOS input stage (M_6 and M_7) and PMOS pass transistor (M_{12}) is utilized to accommodate the input voltage and to provide a large DC gain. The system load impedance is represented by C_L and R_L. Note that C_L includes the decoupling capacitors of various circuit blocks and needs to be relatively small compared to C_{store} otherwise a significant amount of energy is lost by simply transferring charge from C_{store} to C_L. Frequency compensation is again done by using indirect frequency compensation with C_{comp} from node B to E. This effectively isolates C_{comp} from path A and thus does not load the differential pair. Besides providing pole splitting, an additional left-half plane (LHP) zero is created that can be used to stabilize the regulator [131]. A (phantom) zero [132] can also be created by capacitor C_z in the resistive feedback network, but this is less effective due to the small increase in loop gain that can be achieved. Creating a (phantom) zero at the input or output of the regulator also proved to be inefficient and undesirable. Transistors M_1, M_5 and M_{10} are used to minimize current leakage by defining critical floating nodes when Enable='0' (note that I_{ref} is also switched off in the V-I converter for Enable='0').

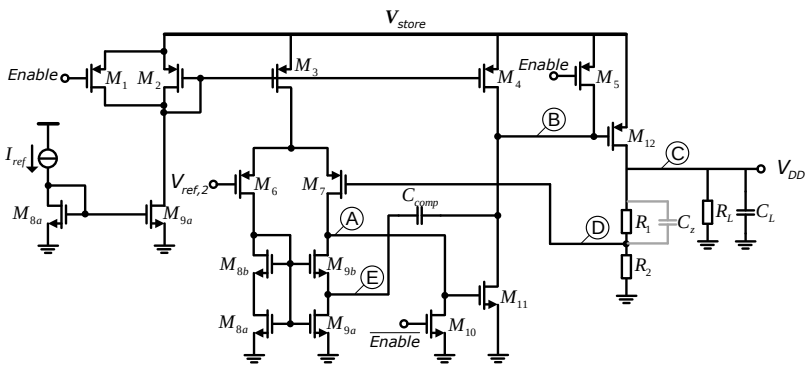


Figure 7.10: Voltage regulator circuit implementation.

The frequency and stability behavior is again analyzed by finding the poles and zeros of the loop gain. Following the analysis outlined in [131, 133], an approximation can be made for the poles and zeros of the proposed voltage regulator with indirect miller compensation. For this analysis, the equivalent circuit elements given in Table 7.2 are used to link the circuit elements to each circuit node shown in Fig. 7.10.

Table 7.2: Circuit elements at each node with their approximate values.

Element	Value	Element	Value
R_A	$r_{o7} \parallel r_{o9}$	C_A	$C_{gs11}+C_{dg9b}+C_{db9b}+C_{db7}+C_{dg7}$
R_B	$r_{o4} \parallel r_{o11}$	C_B	$C_{gs12}+C_{dg12}(1+g_{m12}R_L)$
R_C	$r_{o12} \parallel R_L \parallel (R_1+R_1)$	C_C	C_L
R_D	$R_1 \parallel R_2$	C_D	$C_{gs7}/2+C_{gb7}$
R_E	$r_{db,9a} \parallel g_{m9b}^{-1}$	C_E	$C_{gs9b}+C_{db9a}+C_{dg9a}$

The DC loop gain is given by

$$L(0) \approx -g_{mA}R_A g_{mB}R_B g_{mC}R_C \frac{R_2}{R_1+R_2} \tag{7.6}$$

and equals -5157, corresponding to an absolute gain of 74.24 dB. The dominant pole is approximately given by

$$p_1 = -\frac{1}{2\pi g_{mB}R_B R_A C_{comp}} \tag{7.7}$$

which corresponds to -11.9 kHz. The second pole is given by the load impedance

$$p_2 = -\frac{1}{2\pi R_L C_L} \tag{7.8}$$

and is located at -11.5 MHz. A third pole is found due to the differential pair current mirror and is located at 54.8 MHz:

$$p_3 = -\frac{g_{m8}}{2\pi C_{gs8}} \tag{7.9}$$

A non-dominant pole at -461 MHz is found due to the feedback network configuration and the input capacitance of the first stage when $R_1 \gg R_L$:

$$p_4 = -\frac{1}{2\pi C_D R_D} \tag{7.10}$$

For this implementation, a non-dominant complex pole pair is found at

$$|p_{5,6}| = \frac{1}{2\pi}\sqrt{\frac{g_{m11}}{R_E C_A C_B}} \tag{7.11}$$

which equals 264 MHz. The damping factor ζ is calculated by

$$\zeta = \frac{R_E C_B + R_A C_A \left(\frac{C_B}{C_{Comp}}+1\right)}{2R_A\sqrt{R_E g_{m11} C_A C_B}} \tag{7.12}$$

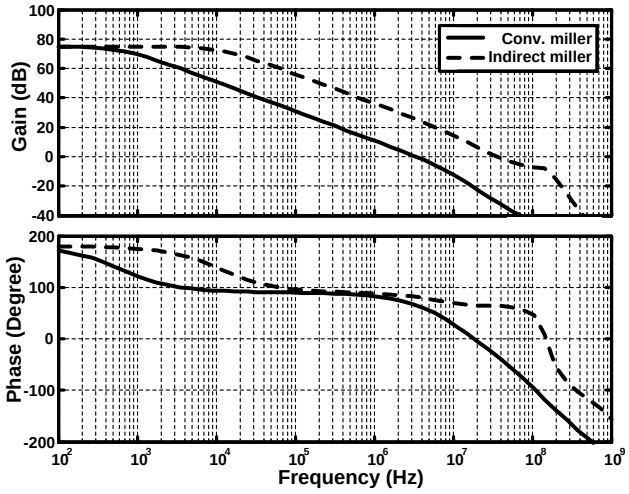


Figure 7.11: Simulated open-loop gain and phase of the voltage regulator with conventional Miller compensation and indirect compensation.

and equals 0.22. These complex poles need to be placed beyond the unity gain frequency to avoid stability issues [134].
A left-half plane (LHP) zero due to C_{comp} is found at

$$z_1 = -\frac{1}{2\pi R_E C_{comp}} \tag{7.13}$$

which corresponds to approximately -22 MHz. A second LHP zero is found due to the differential pair current mirror load and is located at -109 MHz:

$$z_2 = -\frac{2g_{m8}}{2\pi C_{gs8}} \tag{7.14}$$

The simulated open loop characteristics of the voltage regulator are depicted in Fig. 7.11 and compares the conventional Miller compensation (C_{comp} connected between node A and B) with the indirect frequency compensation method used in this work. For the conventional Miller compensation, a 15 pF compensation capacitance is used with a series nulling resistance equal to $1/g_{m11}$ (5 kΩ). Doing so results in a 63 degrees PM and a 3.63 MHz UGBW. For the indirect frequency compensation method, a compensation capacitor of just 1 pF is used to obtain the same 63 degrees PM with a significantly larger UGBW of 40.35 MHz. The voltage regulator with indirect frequency compensation achieves higher loop gain across the entire frequency range and thus offers better PSRR performance.

After adding all parasitic components to the circuit (bondwires, PCB capacitance, test pads), the compensation capacitance C_{comp} is adjusted to 5 pF to obtain a PM of 67 degrees, a gain margin of 10.2 dB and an UGBW of 18.84 MHz. Although this regulator potentially suffers from light load instability, simulations show that the minimum operating current of the WSN is sufficient to ensure stability. The total post-layout current consumption of the voltage regulator equals 53 μA.

7.6 RF Extraction and Frequency Divider

The RF extraction circuit converts the received RF signal into a rail-to-rail square wave signal. The received RF signal is AC-coupled and amplified by the first inverter-based amplifier consisting of M_3 and M_4 shown in Fig. 7.12. Large transistors with high W/L ratios are used to obtain high gain and low noise. A small-scaled inverter replica (M_1 and M_2) is sized to provide a gate bias voltage for the first amplifier while consuming low static current. The input impedance seen from the antenna is made high enough so as not to degrade the RF rectifier performance. The second amplifier (M_5 and M_6) is also AC coupled to avoid duty cycle distortion and provides additional driving capability with fast edge transitions. Self-biasing at the trip point of the inverter is ensured by R_2 and also simultaneously biases the input of the frequency divider. Simulations show that a minimum input voltage swing of about 200 mV is required for RF extraction. When including the passive voltage boosting obtained in the antenna-rectifier interface, this corresponds to approximately -26 dBm.

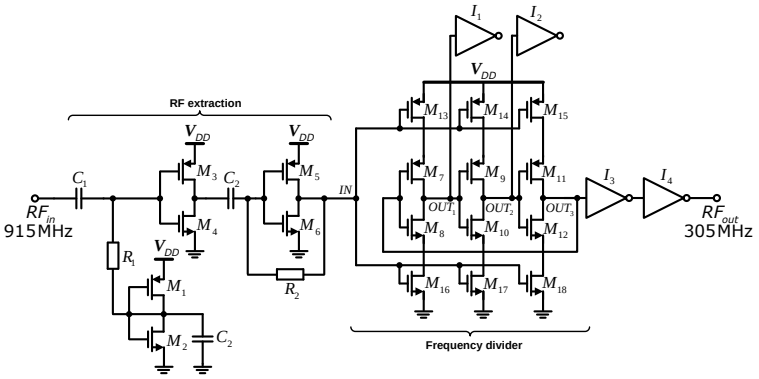


Figure 7.12: RF extraction and frequency divider circuit implementation.

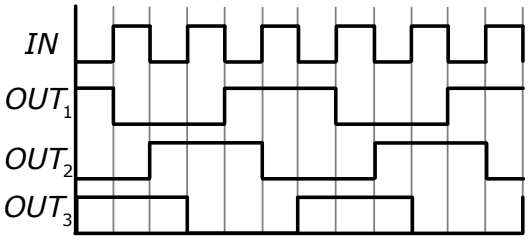


Figure 7.13: Timing diagram of divide-by-three frequency divider.

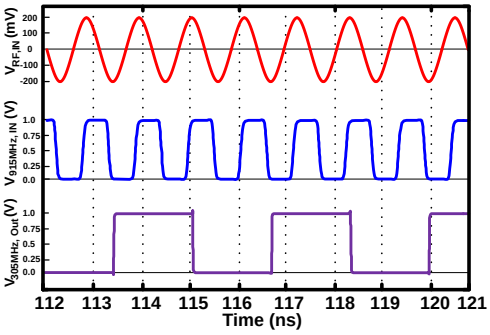


Figure 7.14: Simulated waveforms of RF extraction and divide-by-three frequency divider.

The frequency divide-by-three circuit (also depicted in Fig. 7.12) converts the 915 MHz rail-to-rail signal to a 305 MHz signal and is based on a digital logic divider to obtain a large locking range [135]. The top and bottom transistors are controlled by the input signal and determine when M_7-M_{12} can go to the next transition. Inverter I_1 and I_2 are dummy cells to ensure equal capacitive loading. The timing diagram of the frequency divider is illustrated in Fig. 7.13, where *IN* is the input of the frequency divider and OUT_1, OUT_2 and OUT_3 are the divider output signals of each stage. The simulated waveforms of the complete RF extraction and frequency divider are illustrated in Fig. 7.14 and confirm the functionality. Device mismatch simulations in the TT corner show a mean duty cycle output of 49.9% with a standard deviation of 0.346% and 42.6 μW power consumption. The duty cycle in the SS, FF, FS and SF corner is 49.92, 50.1, 50.4 and 49.9%, respectively.

7.7 Single-Ended-to-Differential Converter

The RF extraction circuit and frequency divider are followed by a single-ended-to-differential converter that provides the pseudo differential reference input to the DLL. The single-ended-to-differential converter depicted in Fig. 7.15 is based on two symmetrical signal paths consisting of inverting and non-inverting buffers with phase interpolation [136]. This structure minimizes the difference of propagation delay between the two output paths. A pseudo differential buffer is adopted to further reduce skew and duty cycle distortion, which is desired to minimize the harmonic contents after frequency multiplication. Transistors M_7 to M_{10} are sized strong enough to overpower the positive feedback of the latch consisting of I_1 and I_2

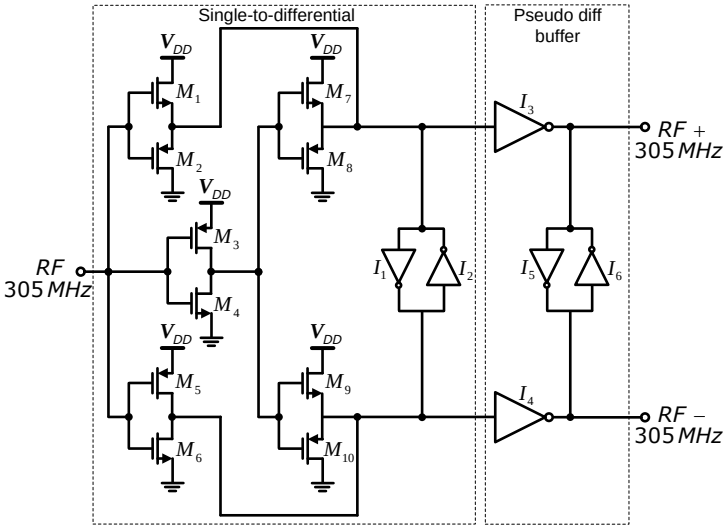


Figure 7.15: Single-ended-to-differential converter circuit implementation.

Post layout simulations of the duty cycle output and power consumption are given in Table 7.3. The duty cycle output is simulated for the entire signal chain, which thus includes the RF extraction, frequency divider and single-ended-to-differential converter.

Table 7.3: Simulated duty cycle output and power consumption over process corners (including RF extraction, frequency divider and single-ended-to-differential converter).

Corner	Duty Cycle RF+	Duty Cycle RF-	Pavg (μW)
TT	49.98	50.02	96
SS	49.74	50.31	90
FF	50.17	49.78	108
FS	50.08	49.72	97
SF	49.85	50.31	96.3

7.8 Delay Locked Loop and Frequency Multiplier

The DLL is configured as shown in Fig. 7.16 and consists of an eight-stage Voltage Controlled Delay Line (VCDL) with dummy delay cells at the input and output for equal loading. A phase detector detects the phase difference between the reference signal φ_{IN} at the input and the signal of the last stage and subsequently drives a charge pump (CP). The CP output is filtered and controls the delay cells with V_{cntrl} such that eight evenly spaced signals are produced.

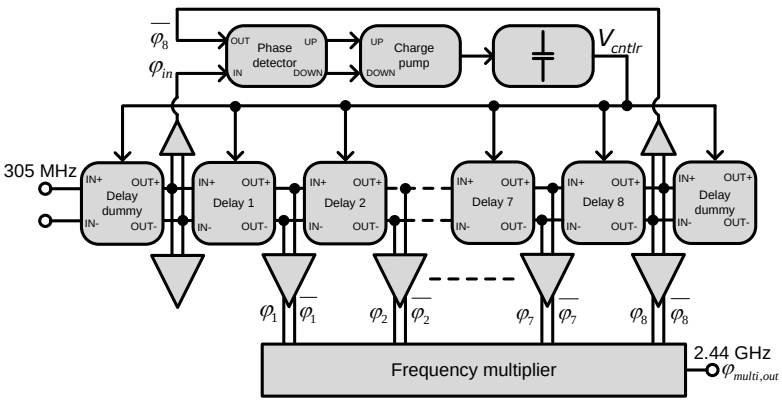


Figure 7.16: Delay locked loop block diagram with frequency multiplier.

Conventional DLLs with an edge combiner only provide an odd numer of frequency multiplication due to the edge alignment of the various phases [137]. An even frequency multiplication can be realized with an edge combiner, but at a two-times lower frequency multiplication factor [138]. This

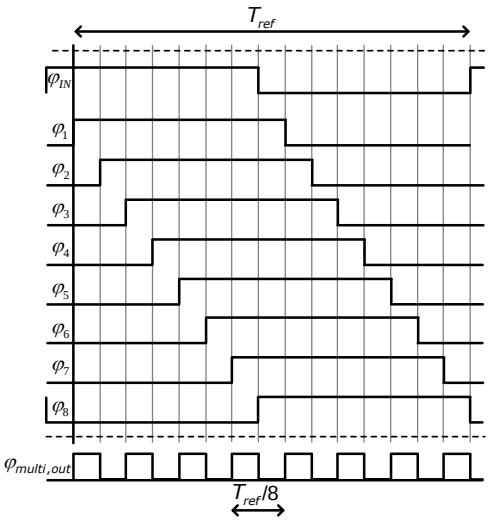


Figure 7.17: Timing diagram of the eight different VCDL phases and the frequency multiplier output.

approach thus requires twice as many delay stages which would considerably increase the power consumption and implementation complexity. To achieve an eight times multiplication factor with eight different phases, the proposed DLL compares φ_{IN} to the inverse of φ_8 as graphically shown in Fig. 7.17 and provides eight evenly spaced signals within half the reference period. This implementation therefore requires a differential delay stage to perform the sign inversion. Frequency multiplication is subsequently achieved by a logic combination of the eight different phases φ_1-φ_8 (the implementation of the frequency multiplier will be discussed in Subsection 7.8.3). The disadvantage of this approach is that the frequency multiplier triggers on both the rising and the falling edge, thereby making the system more sensitive to duty cycle distortion. This can result in a periodic jitter on the output signal $\varphi_{multi,out}$ and thus generates undesirable spurious tones located f_{ref} away from the output center frequency ($f_c \pm f_{ref}$). Symmetry therefore is an important design focus for the implementation of the VCDL.

7.8.1 Voltage Controlled Delay Line

Each delay stage of the VCDL is implemented with a current-starved pseudo differential inverter and an additional buffer as depicted in Fig. 7.18(a). The circuit thus has a rail-to-rail swing with (ideally) zero static current consump-

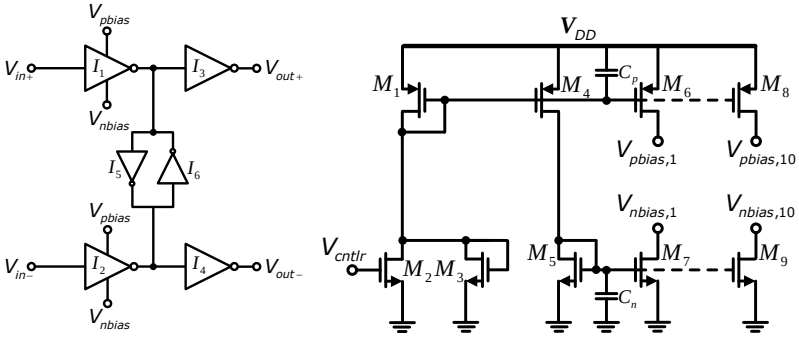


Figure 7.18: Circuit implementation of (a) pseudo-differential current starved delay cell and (b) bias current generation.

tion and low average current consumption. The weak cross-coupled inverters I_5 and I_6 provide good edge alignment between V_{out+} and V_{out-} for minimum duty cycle distortion.

The delay of each stage is controlled by adjusting the maximum current flowing through inverter I_1 and I_2. These bias currents are generated using the circuit shown in Fig. 7.18(b), where transistor M_3 is used to set the minimum delay value and also linearizes the voltage tuning. Capacitors C_p and C_n provide a stable and filtered gate-source voltage of the PMOS and NMOS current sources, respectively. The various bias currents are subsequently distributed to the corresponding delay stages.

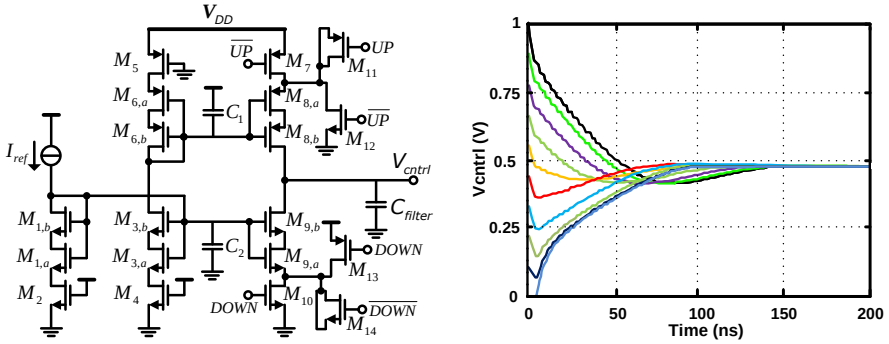
7.8.2 Phase Detector and Charge Pump

The phase detector detects the phase difference between the reference signal φ_{IN} and the last stage φ_8 and outputs two overlapping pulses (UP and DOWN) of equal duration when the input phase error approaches zero. These UP and DOWN signals are subsequently used to control the charge pump current, which is used to charge the tuning capacitor of the VCDL. The implementation of the phase detector in this work (not shown) is adopted from [139], which is based on a precharged dynamic phase detector for low area, low power consumption and high speed operation.

The circuit implementation of the charge pump used in this work is shown in Fig. 7.19(a) and is based on a single ended architecture for low current consumption. Self-cascoded transistors are used to increase the charge pump output resistance and to provide a large output voltage range. The switching

transistors M_7 and M_{10} are placed at the source of M_8 and M_9 to isolate the output V_{cntrl} from the switching action. Dummy transistors M_{14} and M_{11} are utilized to further reduce charge injection. Transistors M_{12} and M_{13} are added to prevent the stored charge on the parasitic capacitance at the drain of M_7 and M_{10} from leaking through the current source to the output node [140, 141]. When the UP or DOWN current source of the CP are turned off (DOWN and/or UP are '0'), M_{12} and/or M_{13} remove the charge from the parasitic capacitance.

Figure 7.19(b) shows the simulated time domain waveforms of V_{cntrl} for various initial voltage conditions for the complete DLL. For all initial conditions the DLL adjusts V_{cntrl} to the same voltage within 150 ns. The small overshoot and undershoot observed in the transient waveform is caused by the charging of decoupling capacitors C_1 and C_2, which also takes time in order to settle to the correct bias voltage during startup.



(a) (b)

Figure 7.19: (a) Charge pump circuit implementation and simulated time domain waveform of V_{cntrl} for various initial voltage conditions.

7.8.3 Frequency Multiplier

The operating principle of the frequency multiplier in this work is based on an XOR logic gate. When two 90 degrees out-of-phase signals are applied to an XOR input as depicted in Fig. 7.20, then a signal at twice the frequency is generated at the output. Since this frequency multiplier triggers at both the rising and the falling edge, it becomes sensitive to duty cycle distortion as was already pointed out earlier. This distortion can be reduced by using duty cycle correction circuits after each frequency multiplication [142, 143]. This however, significantly increases the power consumption and is considered not to

be a feasible solution for the limited power budget in this work. Therefore, the fully symmetric XOR circuit implementation proposed in [144] is adopted to reduce mismatch between the different signal paths. In this XOR implementation (not shown), all signal paths are identical such that they all have equal propagation delay. Simulations of the fully symmetric XOR implementation also show an improved robustness over worst case process corners compared to other conventional XOR circuit implementation.

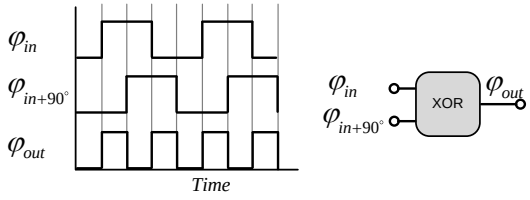


Figure 7.20: Principle of frequency multiplication using an XOR logic gate.

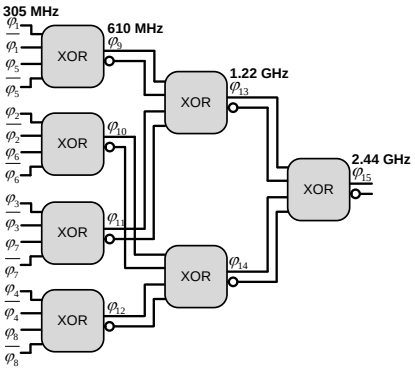


Figure 7.21: Symmetrical XOR-based eight-times frequency multiplier.

By distributing the eight different phases available from the VCDL as shown in Fig. 7.21, an eight-times frequency multiplier is realized using multiple XOR multipliers. The timing diagram of the eight different VCDL phases is again presented in Fig. 7.22, together with the various XOR outputs shown in Fig. 7.21.

Each XOR input has two 90 degrees out-of-phase signals (and the two corresponding inverted signals) that are distributed from the VCDL. After each XOR the frequency is doubled and the signals are distributed further for the next multiplication. Monte Carlo simulations show that duty cycle distortion

doubles with each frequency doubling. The simulated standard deviation in duty cycle is σ=0.061% at 305 MHz input, 0.120% at 610 MHz input and σ=0.239% at 1.22 GHz input. The 2.44 GHz output signal however does not require a 50% duty cycle since the proposed PA uses a duty cycle calibration loop to obtain high drain efficiency, which will be discussed next.

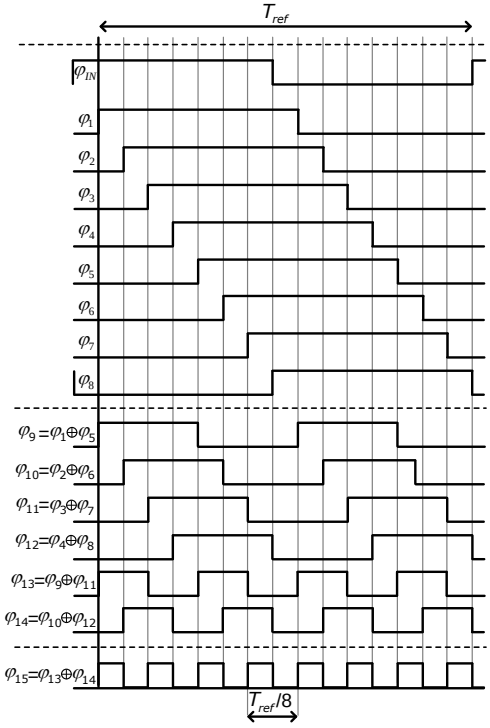
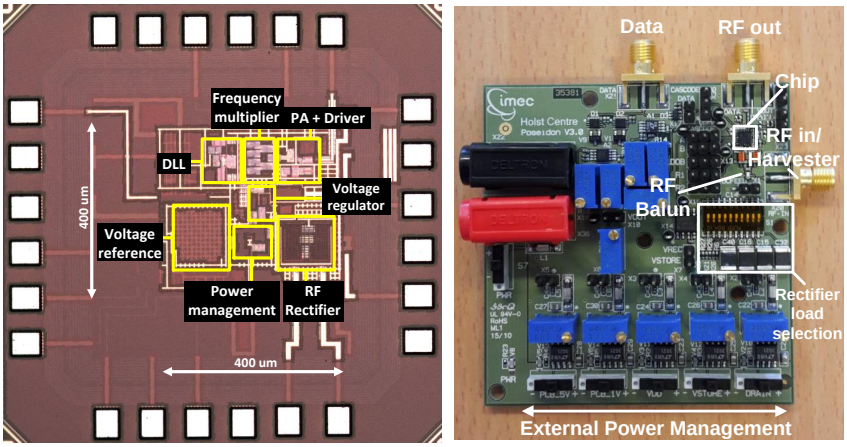


Figure 7.22: Timing diagram of the eight different VCDL phases and the frequency multiplier output.

7.9 Power Amplifier

The tuned switching power amplifier topology with duty cycle calibration loop described in Chapter 6 is again used in the proposed RF-powered transmitter to amplify the 2.44 GHz signal from the frequency synthesizer. In this design, the supply voltages for the PA driver and the PA output stage are equal and provided by the voltage regulator. Similar to the previous prototype, an off-chip matching network transforms the optimum load impedance to the 50 Ω



(a) (b)

Figure 7.23: (a) Chip microphotograph with layout details and (b) photo of the packaged transmitter on a test PCB.

load that represents the antenna impedance during measurements.

7.10 Experimental Results

7.10.1 Measurement Setup

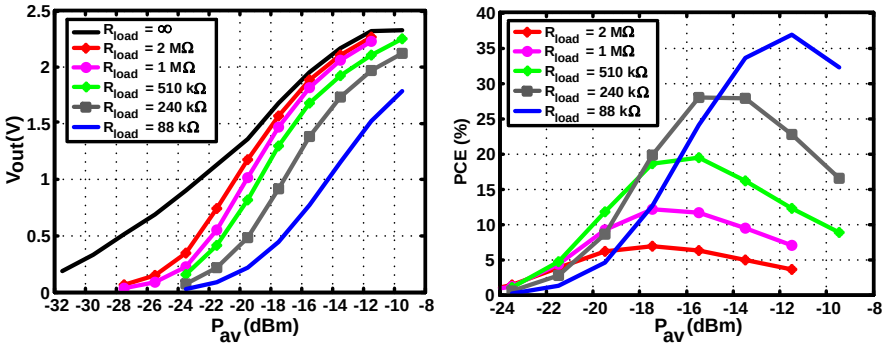
The transmitter has been fabricated in TSMC 40 nm CMOS technology and is bondwired to a 24-lead QFN package that is mounted on a PCB for testing. The complete die size including padring is 0.9 mm^2 while the active area occupies only 0.16 mm^2 as depicted in Fig. 7.23(a). Each sub block is highlighted for clarity. Extensive use has been made of power supply mesh unit cells for good current distribution and on-chip supply decoupling.

The test PCB shown in Fig. 7.23(b) contains external power management to measure the individual current of the various circuit blocks and also provide the opportunity for debugging. The external RF balun with matching network is placed closely between the chip and the RF input SMA to minimize parasitics.

Measurements are done using an Agilent E4438C 6 GHz signal generator, R&S FSW 8 GHz signal & spectrum analyzer, R&S RTO1044 4 GHz oscilloscope and a Keithley 6430 source meter.

7.10.2 RF Rectifier

The RF rectifier performance is evaluated by disconnecting the power management circuits and measuring the steady state DC output voltage for different load conditions and available power. To reduce the loading effect of the measurement equipement for the RF rectifier, a high-impedance commercially available opamp is used as buffer. For the following measurement results, a 50 Ω signal generator is used to supply a 915 MHz RF continuous wave. The losses of the off-chip matching network (Fig. 7.2) are included while the insertion loss of the off-chip balun is excluded since a balun is not required when replacing the 50 Ω source with a differential antenna. The available power therefore is adjusted accordingly during the measurement procedure.



(a) (b)

Figure 7.24: (a) Measured DC output voltage V_{out} and (b) power conversion efficiency for different load conditions and available power P_{av}.

Figure 7.24(a) shows the measured DC output voltage versus P_{av} for different load conditions. For a purely capacitive load ($C_{store} = 1\mu F$), the rectifier requires -22.6 dBm and -18.6 dBm to generate 1V and 1.5V, respectively. The power conversion efficiency (PCE) is determined by measuring the output voltage versus P_{av} for different load resistances and subsequently calculating PCE=$V_{out}^2/(R_{load}P_{av})$. The PCE represented in Figure 7.24(b) peaks around -11.47 dBm with a maximum of 36.83% for a load resistance of R_{load}=88 kΩ. The sensitivity and efficiency performance of this RF energy harvester thus are slightly worse compared to the antenna-rectifier co-design results discussed in Chapter 5. The main reason for this is that the passive voltage boost in the antenna-rectifier interface is lower for the design discussed in this chapter. This is a result of the additional losses of the external matching network since

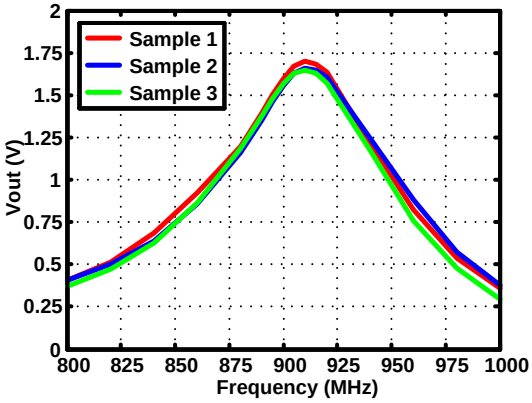


Figure 7.25: Measured rectifier DC output voltage vs. input frequency at P_{av}=-18 dBm and $R_{load} = \infty$ for three different IC samples.

the RF energy harvester reported in Chapter 5 uses the antenna impedance as matching network and thus has no additional matching components. Another explanation is that the second RF energy harvester implementation is designed for a lower Q-factor because this version does not include a control loop to ensure robustness. This also directly lowers the passive voltage boost in the interface and therefore affects the performance.

Figure 7.25 shows the measured output voltage while performing a frequency sweep at the RF rectifier input for P_{av}=-18 dBm and $R_{load} = \infty$. Three different IC samples show very comparable results and all have a -3 dB bandwidth of approximately 60 MHz.

7.10.3 Power Management

Since both the voltage reference and detector limit the overall system sensitivity, the current consumption of these circuits are measured over the complete output voltage range of the rectifier. Figure 7.26 shows the $V_{ref,2}$ versus V_{store} characteristics at room temperature. For $V_{store} \leq 0.3$V, the voltage reference output follows V_{store} since transistor M_6 in Fig. 7.6 connects $V_{ref,2}$ to V_{store} to prevent a false positive 'Enable'. Once $V_{store} \geq 0.4$V, transistor M_6 is switched off and $V_{ref,2}$ settles to approximately 656.5 mV. The voltage reference changes only 0.9 mV when V_{store} changes from 0.9 to 1.5 V, resulting in a line sensitivity $\left(\Delta V_{ref,2}/\Delta V_{store}\right)/V_{ref,2}$ of 0.228 %/V.

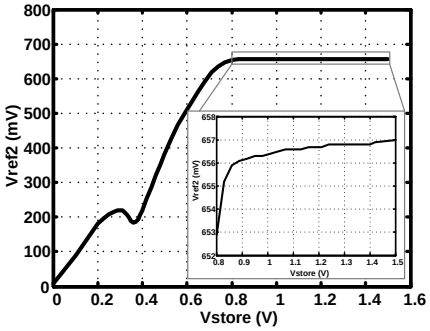
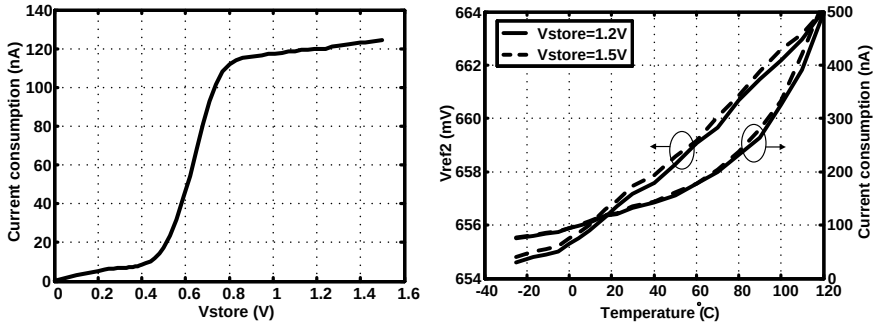


Figure 7.26: Measured reference voltage V_{ref2}.

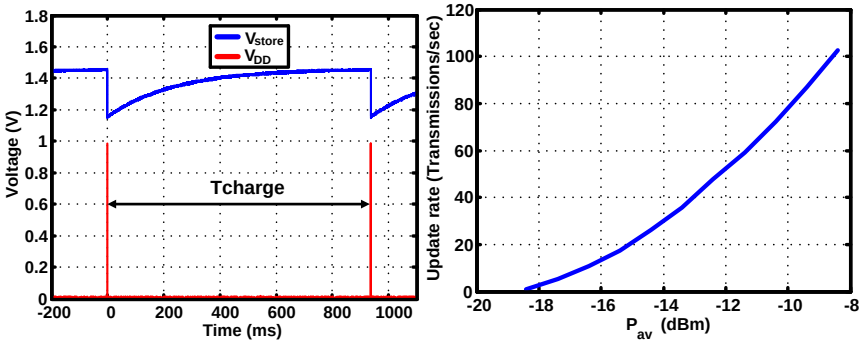


(a) (b)

Figure 7.27: Measured (a) current consumption vs. storage voltage V_{store} at room temperature and (b) voltage reference V_{ref2} and current consumption (voltage reference and detector) vs. temperature.

The measured current consumption depicted in Fig. 7.27(a) includes the current drawn from both the voltage reference and the voltage detector. At V_{store}= 0.8V the total current consumption reaches 112 nA and slowly increases towards 124 nA at V_{store}=1.5 V.

The effect of temperature variations on the voltage reference is illustrated in Fig. 7.27(b). The voltage reference changes 9.6 mV between -20 and 120 °C, resulting in a temperature coefficient of 104.5 ppm/°C. Over the same temperature range, the total current drawn by the voltage reference and detector changes from 80 to 500 nA. Although the current consumption increases at high temperatures, the rectifier output current also increases because the transistor theshold voltage decreases with increasing temperature and thus compensates for this effect. Note that there is very little variation in both the



(a) (b)

Figure 7.28: Measured (a) waveforms of V_{store} and the regulated V_{DD} of the complete transmitter at the minimum startup power $P_{av} = -18.4$ dBm and (b) update rate $\left(1/T_{charge}\right)$ vs. P_{av}.

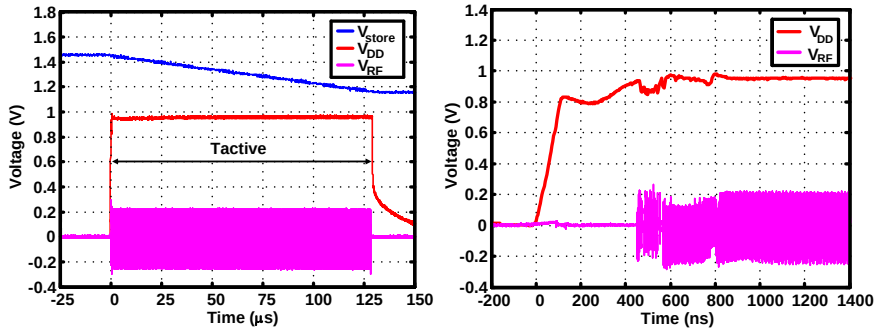
voltage and the current characteristics when V_{store} is changed from 1.2 V to 1.5 V (corresponding approximately to the voltage range from V_L to V_H).

The measured charging waveforms of V_{store} and V_{DD} shown in Fig. 7.28(a) are obtained with a minimum startup power of P_{av}=-18.4 dBm. At this power level, the rectifier (when loaded with the voltage reference and detector) is able to generate V_H=1.44 V and takes approximately 1.4 sec from 0 V. Once V_H has been reached, the voltage detector subsequently enables the voltage regulator and all other circuit blocks. The current drawn by the transmitter discharges the storage capacitor until V_L=1.16 V, after which the detector again disables the circuit blocks. The charging time to reach V_H from V_L for P_{av}= -18.4 dBm and $C_{store} = 1\,\mu F$ equals 936 ms. For higher power levels, T_{charge} decreases such that a higher sensor update rate $(1/T_{charge})$ can be realized as shown in Fig. 7.28(b). As an alternative approach, the V_H level could adaptively be increased with higher power levels such that more energy is available for wireless data transmission instead of a higher sensor update.

7.10.4 Complete Transmitter

Figure 7.29(a) shows a zoomed in image of the active period where the transmitter is enabled at t=0. While the storage capacitor is being discharged from V_H to V_L, the voltage regulator stabilizes V_{DD} and the transmitter outputs a continuous 2.44 GHz RF signal at -2.57 dBm for T_{active}=128 μs. During continuous transmission, the voltage regulator consumes 54 μW and the frequency

synthesizer and PA driver together consume 742 μW. The PA drain current equals 1516 μA, resulting in a drain efficiency of 36.5% from a 1 V regulated supply. The total power consumed by the TX is 2.312 mW, resulting in a global efficiency $P_{out}/P_{DC,total}$ of 23.9%.



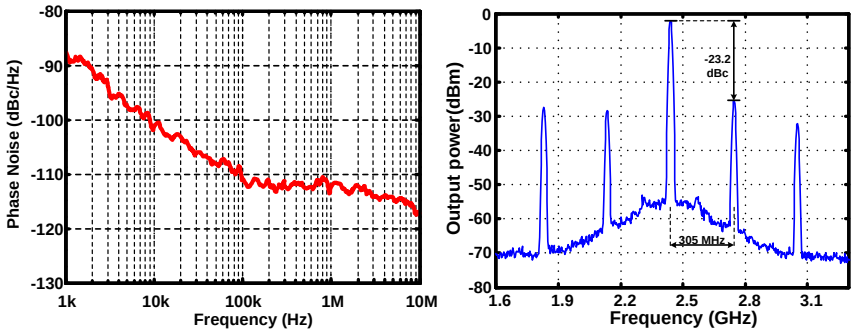
(a) (b)

Figure 7.29: Measured (a) active period and (b) zoomed in cold-start behavior at t=0 of complete transmitter at minimum startup power $P_{av} = -18.4$ dBm.

The startup behavior of the complete transmitter at $P_{av} = -18.4$ dBm input is illustrated in Fig. 7.29(b). Note that this includes all cold-start settling effects like voltage and current biasing and internal and external capacitors charging effects. The DLL is activated after approximately 500 ns and the complete TX is settled after 800 ns with a regulated supply. The minimum power for RF extraction is -25.47 dBm across the entire 902-928 MHz ISM band.

Measurements at $P_{av} = -18.4$ dBm show a residual RMS jitter of 0.9 ps at 2.44 GHz and a phase noise of -112.5 dBc/Hz at 1 MHz offset as illustrated in Fig. 7.30(a). The measured 2^{nd} and 3^{rd} harmonic tones are both 47 dB below the fundamental tone, while the closest spurious tone is -23.2 dBc and is located 305 MHz away from the carrier as depicted in Fig. 7.30(b). These spurs are relatively high compared to for example PLL-based systems, which can achieve a spurious emission of 60 dB below the TX carrier level [65]. Section 15.247 and 15.249 of the FCC regulations dictate a maximum electric field strength of 50 mV/m measured at 3 meter distance from a radiator that is operating in the frequency band of 2.4-2.4835 GHz [56]. This corresponds to an EIRP of –1.23 dBm and is thus higher than the output power in this work. The maximum spurious output is 20 dB below the fundamental RF output power, given that the radiator employs some form of digital modulation tech-

nique to obtain a spread spectrum. Pulse shaping as demonstrated in Section 6.4.3 is another way to reduce the spurious emission. A practical narrowband antenna as a replacement for the 50 Ω analyzer input impedance will also provide some additional suppression of the generated spurs.
It is expected that better results can be obtained when using duty cycle correction circuits. This however is a challenging task given the very stringent power budget. Some authors have used similar DLL-based frequency multipliers with duty cycle correction circuits. In [142] a DLL-based frequency multiplier at 2.64 GHz output consumes 27.79 mW, while the frequency synthesizer in [143] dissipates 38.35 mW at 2.2 GHz output. These power levels are significantly higher compared to the measured 742 μW in this work (excluding PA).



(a) (b)

Figure 7.30: Measured (a) phase noise and (b) output spectrum at 2.44 GHz output with $P_{av} = -18.4$ dBm.

The measured TX output spectrum for a 0.5 Mbps pseudo random OOK modulated signal is shown in Fig. 7.31(a). The power consumption of the complete TX during OOK modulation equals 1.46 mW since only the PA is disabled while the power management and frequency synthesizer are always on to allow for fast startup. Measurement results showed however that the large PA startup current causes a small voltage dip at the output of the voltage regulator. Since all circuit blocks share the same supply voltage, this voltage dip also detunes the DLL and causes a dip in the RF output during transmission of a logic '1' as shown in Fig. 7.31(b). As the duration of this voltage dip is approximately 75 ns, this limits the attainable bitrate. An external LDO was used to test this hypothesis, which indeed eliminated the dip in the RF signal and allowed for higher bitrates.

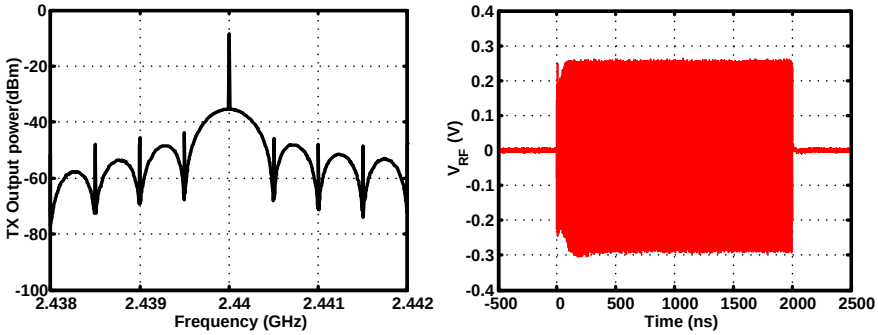


Figure 7.31: Measured (a) TX output spectrum of a 0.5 Mbps pseudo random OOK modulation and (b) time-domain waveform of a logic '1' transmission.

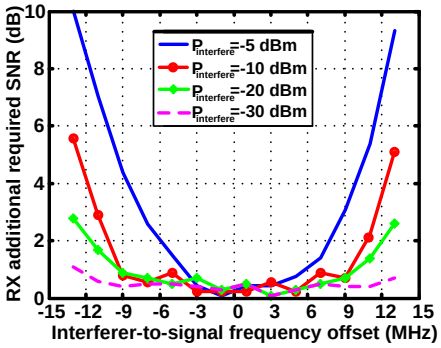


Figure 7.32: Additional required SNR for a 0.1% BER vs. interferer-to-signal frequency offset with desired input signal at -18.4 dBm.

Figure 7.32 gives an indication of the required receiver SNR when an interference signal is present near the desired dedicated RF signal which is utilized for frequency synthesis. The TX output signal is measured while a continuous wave interferer is added at a given frequency offset from the dedicated RF signal. The dedicated RF signal is set to the minimum startup power of -18.4 dBm. Subsequently, the required SNR for a 0.1% bit error rate (BER) at the receiver is determined using an optimum threshold non-coherent demodulator, which is implemented in Matlab. When the interferer power level is below the dedicated RF power level, no significant performance reduction at the receiver is observed. When the interferer power level is increased further, it shows that a higher SNR at the receiver is required to maintain a 0.1% BER. A larger frequency offset results in more frequent edge misalignments

at the DLL and the frequency multiplier which impacts the fundamental signal frequency and amplitude. As an example, in order to demodulate the desired signal with a -10 dBm continuous wave interferer at 13 MHz offset, the receiver requires an increase of 5 dB in SNR, thereby limiting the maximum achievable wireless range.

7.10.5 Comparison with Previous Work

Table 7.4 summarizes the measured experimental results and compares it to prior art. This work shows a very small active area of only 0.16 mm^2 due to the compact DLL and frequency multiplier circuits. Only the work in [60] shows a smaller die area, but is based on backscattering and thus is much more limited in output power and also requires 12.5 dB more (i.e, -5.9 dBm) RF power for startup. The minimum RF startup power of this work is 3.4 dB lower than the design in [65] and 1.6 dB and 1.1 dB higher than the designs of [66] and [145], respectively. A lower RF startup power can be achieved when using a co-designed antena instead of the 50 Ω signal generator with balun and additional matching network. If necessary, the startup RF power can be reduced further by for example employing more rectifying stages. This however also increases the charging time as discussed in Section 5.2.2. So although highly sensitive systems with many rectifying stages can operate wirelessly over longer distances, they may be impractical for some applications if the charging time is too long. The required minimum startup RF power thus is application dependent.
The proposed TX shows a relatively low data rate due to the voltage dip limitation of the voltage regulator. Much higher data rates can be achieved once this is corrected as was demonstrated with the 40 Mbps OOK output in Section 6.4.3. Finally, the proposed TX shows favorable results in terms of output power (-2.57 dBm) and a global efficiency of 23.9%.

Table 7.4: Performance summary and comparison with prior art.

Parameters	This work	Shirane '15 [60]	Papotto '14 [65]	Xia '14 [66]	Ito '14 [145]
Technology	40 nm	65 nm	90 nm	65 nm	65 nm
Active die area$^{(a)}$	0.16 mm^2	0.13 mm^2	0.8 mm^2	1.7 mm^2	0.3 mm^2
Frequency	915 MHz / 2.44 GHz	5.8 GHz (backscattering)	915 MHz / 2.44 GHz	904.5 MHz / 402 MHz	800 MHz / 2.5 GHz UWB
Minimum startup RF power$^{(b)}$	-18.4 dBm	-5.9 dBm	-15 dBm	-20 dBm	-19.5 dBm
Rectifier max PCE	36.83% @ -11.47 dBm	-	16.1% @ -15.83 dBm	-	-
TX output power	-2.57 dBm	-28.6 dBm	-12.5 dBm	-16 dBm	-62.1 dBm
TX global efficiency	23.9% @ 1V supply	1.2% @ 0.6V supply	6.53% @ 1V supply	10.8% @ 0.6-1V supply	0.027% @ 0.6-1V supply
TX Data rate	0.5 Mbps (OOK)	2.5 Mbps (QAM)	5 Mbps (OOK)	0.25 Mbps (OOK)	1 Mbps (OOK)

(a): Extracted or estimated from available data.
(b): Available power P_{av} (including component and mismatch losses).

7.11 Conclusion

A compact RF-powered DLL-based 2.4 GHz CMOS transmitter has been presented. The received dedicated RF signal is used for both RF energy harvesting as well as frequency synthesis by using a nanowatt power management circuit combined with a DLL and XOR-based frequency multiplier. A tuned switching RF power amplifier with 25% duty cycle input is utilized in order to obtain high global efficiency for <0 dBm output power. Experimental results of a 0.16 mm^2 40 nm CMOS prototype show a maximum rectifier efficiency of 36.83% and a power management circuit with 120 nA current consumption during harvesting mode. For a 1 μF storage capacitor and -18.4 dBm minimum available power at 915 MHz RF input, the TX outputs a continuous 2.44 GHz RF signal at -2.57 dBm for 128 μs with 36.5% PA drain efficiency and 23.9% global efficiency. The complete TX consumes 1.46 mW during On-Off Keying (OOK) modulation at 0.5 Mbps.

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS

This dissertation focused on the research, design and implementation of various circuit blocks and system integration of energy scavenged wireless sensor nodes. The main target applications used for this thesis are smart buildings and warehouse inventory management, which require small, low-cost and maintenance-free devices that can transmit their data over several meters. It was found that RF-powered autonomous WSNs have the distinct advantage over other energy harvesting systems that they can operate wirelessly in a large variety of applications, even in thermally constant, dark and static environments. Moreover, additional advantages such as utilizing a dedicated RF source for both energy harvesting as well as a reference frequency greatly reduces the complexity, costs and power consumption of the WSN. For these reasons, this thesis focused on innovative circuit and systems for RF-powered WSNs.

The major contributions that are the result from the research conducted in this thesis are described in Section 8.1. Some recommendations for future research are described in Section 8.2.

8.1 Major Contributions of this Thesis

Co-design principles have been introduced for electrically-short antenna-electronics interfaces for antennas in the receiving mode. It was argued that power transfer is not the only design objective in these interfaces, but that the interface also needs to be optimized for either voltage or current, depending on which is more favorable for the electronics. Furthermore it was

found that when the available power and antenna load are fixed, one cannot increase the load voltage or current to higher levels by means of antenna design only. The first condition to accomplish this is to conjugate match the antenna-electronics interface as this maximizes both the voltage and current at the load. The second condition is to determine at *which* impedance level conjugate matching should occur in order to *further* increase the load voltage or current. In case of voltage sensing, the designer needs to design the electronic circuit for the largest input resistance possible and subsequently co-design the antenna impedance for conjugate matching.

The general consensus of using a 50 Ω antenna-rectifier interface has been challenged and shown to be a suboptimal solution for the design of highly sensitive RF energy harvesters. It was shown that in order to achieve good sensitivity, a sufficiently large voltage swing is required at low input power levels to activate the rectifier as MOS transistors inherently are voltage-controlled devices. This can be achieved by using an antenna with a small radiation resistance and a high inductive reactance. This not only provides significant passive voltage boosting but also simultaneously eliminates external matching components. To demonstrate this, an integrated rectifier in 90 nm CMOS has been co-designed with a compact loop antenna. To ensure the correct interface impedance, a self-calibrating control loop is proposed that compensates variation at the interface while benefiting from the large passive voltage boost. Furthermore, a complementary MOS diode is proposed that significantly reduces the reverse current leakage and extends the harvester's ability to store and hold energy over time by almost a factor 200. Measurements in an anechoic chamber at 868 MHz demonstrate an end-to-end maximum power conversion efficiency of 40% and a sensitivity of -27 dBm to generate 1V across a capacitive load, which is the best sensitivity amongst state-of-the-art published articles found in the literature today.

The theory and design procedure of a high-efficiency 2.4 GHz tuned switching PA for <0 dBm output power has been presented. A simplified theoretical model has been proposed that accurately describes the drain efficiency for a given duty cycle and switch resistance. It was found that a high drain efficiency can be achieved in practice when the input duty cycle is set roughly between $0.2 \leq d \leq 0.3$, depending on the switch and effective load resistance. When the duty cycle decreases below 0.2, the power loss due to the switch resistance becomes relatively large because the fundamental RF output power approaches zero. To set the duty cycle to the optimum value of about 0.25, a novel on-chip duty cycle calibration loop has been proposed that fixes the duty cycle over PVT variations. Furthermore, a method is described to max-

imize the global efficiency by optimizing the capacitive switching losses of the PA driver, the PA switch resistance and the RF input duty cycle. Measurement results of a 40 nm CMOS PA prototype with OOK modulation and pulse shaping capabilities showed a global efficiency of 40% when delivering -5 dBm to a 50 Ω load, which compares favorably to the state-of-the-art.

The accumulated knowledge from the contributions made in this thesis is used to demonstrate the system integration of a complete RF-powered transmitter. The received dedicated RF signal is used for both RF energy harvesting as well as frequency synthesis by using a power management circuit combined with a DLL and XOR-based frequency multiplier. All building blocks (RF energy harvester, power management, RF extraction, DLL, frequency multiplier, PA) have been implemented in 40 nm CMOS technology and occupy only 0.16 mm^2. Experimental results show a maximum rectifier efficiency of 36.83% and a functional power management circuit with 120 nA current consumption during harvesting mode. A minimum startup power of -18.4 dBm at 915 MHz RF input with -2.57 dBm output at 2.44 GHz RF output enables a long wireless operating range. A PA drain efficiency of 36.5% and a global efficiency of 23.9% shows favorable compared to its state-of-the-art competitors. The complete TX consumes 1.46 mW during On-Off Keying (OOK) modulation at 0.5 Mbps. These measurement results confirm the feasibility of an RF-powered transmitter that can be utilized for autonomous wireless sensor node applications.

8.2 Recommendations for Future Research

Although this thesis has identified and addressed the main challenges for RF-powered WSNs, there still is sufficient room for future research. Some suggestions for improved functionality and performance are listed in this section.

- **Implementation of Control Loop:** In this work, the self-calibrating impedance control loop used to optimize the antenna-rectifier interface is implemented off-chip using a micro controller as a proof of principle. For complete system integration, an on-chip loop implementation is needed with a nanowatt power budget. It is advised to put emphasis on a low current leakage design and use duty cycling and a calibrate-and-memorize strategy to reduce the power consumption.

- **Rectifier with Boost Converter:** One of the disadvantages of using multiple rectifying stages is the reduced power conversion efficiency

that can be achieved compared to a single rectifier stage. Another drawback is that when charging a capacitor with a rectifier, maximum power transfer is only achieved at the moment when the capacitor voltage is exactly half of the steady state voltage (see Appendix A).
A combination of a (single) rectifier and a switched-mode boost converter with Maximum Power Point Tracking (MPPT) may be a feasible solution to obtain a more efficient RF energy harvesting system. To activate the boost converter from a cold start, a parallel multi-stage rectifier optimized for high output voltage can be used to provide sufficient supply voltage to active the logic control circuit. Once activated, the boost converter and main rectifier can take over and further optimize the power transfer.

- **Antenna Design:** Both the 915 MHz receiving antenna impedance as well as the 2.44 GHz transmitting antenna impedance are assumed to be 50 Ω in order to simplify the measurement procedure. However, as was strongly emphasized in Chapter 5, this oversimplifies and neglects many aspects that can have a dominant effect on the end-to-end performance. Therefore, an antenna needs to be designed for both the TX and RX. When the co-design procedure as described in Chapter 5 is followed for the RX antenna, it is expected that the RF energy harvesting efficiency and system sensitivity will improve. The TX antenna can also be co-designed with the power amplifier by for example designing for a higher radiation resistance than the conventional 50 Ω. Doing so requires a lower impedance transformation ratio and thus generally results in a more robust interface with larger bandwidth. Using the antenna's reactance as part of the matching network is another possibility to further improve performance.
  Additional design efforts can be made to design for antennas on flexible substrate that can be integrated in clothing and thus allow for wearable WSNs. Integrating both the TX as the RX antenna on a single structure is another interesting topic to improve the system integration. Self-interference in this case is a key design aspect that also needs to be considered during the co-design.

- **Voltage Regulator Redesign:** Measurement results of the voltage regulator in Chapter 7 showed that the large PA startup current caused a small voltage dip at the output of the voltage regulator. Since all circuit blocks share the same supply voltage, this voltage dip also detunes the DLL and causes a dip in the RF output during transmission. This effect

therefore limits the attainable bitrate.
A first solution for this issue is to redesign the voltage regulator such that it can handle the large PA startup current. A second solution is to split the voltage regulator in two parts, one regulator optimized for the PA and one regulator to supply the rest of the chip. The latter has the advantage that the PA drain voltage can be adjusted independently from the rest of the chip and thus allows for the possibility to easily adjust the output power without having to change the output matching network of the PA. The drawback of this output power control is the low voltage regulator efficiency at low output power levels. Alternatively, a high efficient DC-DC converter can be used to adjust the PA drain voltage.

- **Alternative Frequency Synthesis:** Using the received dedicated RF signal as a reference frequency for frequency synthesis is a low cost and low complexity way of realizing an RF carrier for wireless data transmission when no other (stable) reference frequency is available to the WSN. The downside however is that the quality of the RF signal depends on the received signal. Future research is required to investigate ways to realize a clean and robust RF signal with low cost, small size and low power consumption. If such an alternative reference frequency is presented in the future, it is adviced to reconsider the frequency synthesis for improved performance.

- **Power Amplifier:** One of the disadvantages of the tuned switching RF Power Amplifier is the large required impedance transformation ratio at low output powers, which makes the matching network more sensitive to mismatch. Because of the single-ended inductively loaded topology, the drain voltage swings from 0 to $2V_{dd,drain}$. The output voltage swing of a push-pull topology however is two-times smaller and thus requires a four-times lower effective load resistance for the same output power. More research is required to investigate the feasibility of a reduced duty-cycle push-pull PA, where the push and pull path are driven separately with a reduced duty cycle to enhance the efficiency.

- **Additional Measurements:** When both the RX and TX antennas are available, it is advised to obtain more measurement results of the RF-powered transmitter for a full characterization. First, the performance must be evaluated in free-space conditions by using an anechoic chamber. Subsequently, additional measurements (for example a bit error rate test) are needed to evaluate the performance under limiting conditions

such as non-line-of-sight propagation, antenna (polarization) mismatch and interference.

APPENDIX A

COMMENTS ON RF ENERGY HARVESTING DESIGN ISSUES

In this appendix some additional comments are made on RF energy harvesting design issues such as optimum load resistance, loading effects and charging characteristics.

Optimum Load Resistance

Lets us first consider the relationship between the input and output quantities of a lossless N-stage rectifier [1] that is conjugate matched to an inductive antenna as depicted in Figure A.1. Here, $V_A = \sqrt{8R_A P_{av}}$ is the antenna equivalent source voltage, P_{av} is the available power from the source and R_A and X_A are the antenna resistance and reactance, respectively. It is assumed that the rectifier operates in the steady state and is loaded by a resistor and large capacitor. There exists an optimum load resistance R_{opt} for maximum power conversion efficiency because R_{opt} defines the optimum DC voltage to current ratio at the output that corresponds to the available power, voltage and current ratios from input to output. This optimum load resistance can thus be written in terms of the input or output quantities:

$$R_{opt} = \frac{V_{out}^2}{P_{av}} = \frac{V_{rec}^2 N^2}{P_{av}} \tag{A.1}$$

The rectifier input voltage V_{rec} can be described by V_A and the interface impedance. Recalling from Section 4.5.4 on Page 49, this can be written as

[1] As was already pointed out in Section 5.1.1, the rectifier equivalent circuit model depicted in Fig. A.1 is used as a simplified linear approximation to gain an intuitive understanding of the antenna-rectifier interface properties.

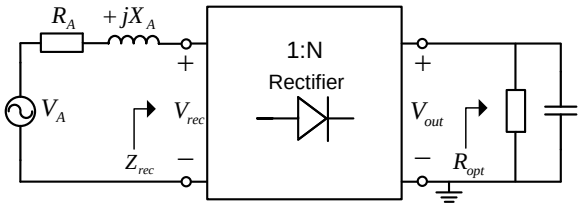


Figure A.1: Circuit model of an N-stage rectifier with resistive load and parallel filter capacitance connected to an inductive antenna.

$$V_{rec} = \sqrt{2P_{av}R_A}\sqrt{1+Q^2} \tag{A.2}$$

where $Q = \frac{X_A}{R_A}$ is the unloaded Q-factor of the interface (or equivalently the Q-factor of the antenna). Substituting (A.2) into (A.1) gives

$$R_{opt} = 2R_A\left(1+Q^2\right)N^2 \tag{A.3}$$

The optimum load resistance thus scales with the square of the total voltage 'gain', which includes the passive voltage gain from the antenna-rectifier interface and the gain obtained from the number of rectifying stages N. It is noteworthy that this simplified model predicts that R_{opt} is independent of P_{av}. In practice however, the rectifier input impedance is dependent on P_{av} as evident from Fig. 5.8 on Page 67. An increase in P_{av} at low power levels typically results in a reduced Q-factor of the rectifier input impedance and hence lowers the required R_{opt}. This phenomena is in accordance with the measured efficiency curves illustrated in Fig. 5.21 on Page 79.

Loading Effects

An RF energy harvester with a high R_{opt} offers a good sensitivity due to the large voltage gain, but can potentially suffer from loading effects. This happens when the output current becomes so low that it becomes comparable to for example the leakage current of the storage capacitor or any circuit connected in parallel to the rectifier load. This is the case when for example connecting a commercially available DC/DC converter to the RF energy harvester designed in this thesis. When the optimum input resistance of the DC/DC converter is for example around 10 kΩ, the designed RF energy harvester cannot deliver enough current since R_{opt} in this work is about 300 kΩ. Hence, in

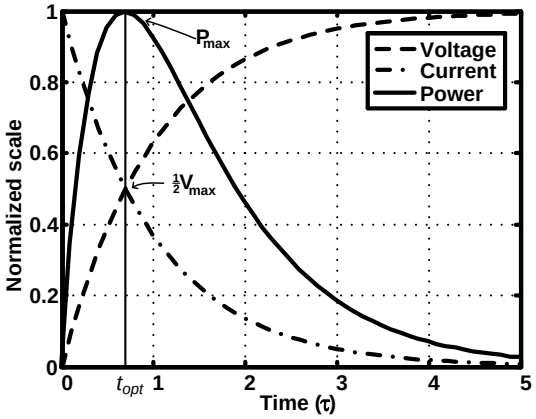


Figure A.2: Typical normalized voltage, current and power characteristics of a capacitor charged by a rectifier.

order to realize a highly sensitive RF energy harvester, the designer needs to know the characteristics of the rectifier load and its limitations.

Capacitive Charging Characteristics

The charging behavior of a rectifier charging a capacitor can be modeled as a typical RC exponential curve. The voltage across the capacitor during charging is thus described by

$$V_{cap}(t) = V_{max}\left(1 - e^{\frac{-t}{RC}}\right) \tag{A.4}$$

while the current through the capacitor is given by

$$I_{cap}(t) = \frac{V_{max}}{R} e^{\frac{-t}{RC}} \tag{A.5}$$

Note that V_{max} corresponds to the maximum output voltage in case of a purely capacitive load. The instantaneous power transferred from the rectifier to the capacitor is given by

$$P_{cap}(t) = \frac{V_{max}^2}{R}\left(e^{\frac{-t}{RC}} - e^{\frac{-2t}{RC}}\right) \tag{A.6}$$

The normalized waveforms of the voltage, current and power over time ($\tau = RC$) are depicted in Figure A.2. Note that maximum power transfer from the source to the capacitor is only achieved at one specific moment in time. This optimum point is found by setting $\frac{dP_{cap}(t)}{dt} = 0$, which results in

$$t_{opt} = \tau \ln(2) \tag{A.7}$$

The corresponding voltage level at this specific point equals

$$V_{cap}(t_{opt}) = \frac{1}{2} V_{max} \tag{A.8}$$

Hence, when the capacitor voltage is either significantly lower or higher than half of the maximum output voltage, only a small fraction of the available source power is transferred to the capacitor and thus the efficiency is reduced.

Ideally, the RF energy harvester should always operate at the optimum point for maximum power transfer, which thus requires a fundamentally different charging characteristic. Such a power management system has been proposed in [146], where two capacitor arrays have been used to dynamically adapt the interface for optimal loading. The charging level of each capacitor is kept within 40-60 % of the maximum output voltage to achieved near-optimum power transfer over a wide range of load resistances.

If the RF energy harvester however can be implemented in such a way that it behaves as a hypothetical constant power source [147], then it would always operate at the maximum power point during charging. The differential equation for a constant power source charging a capacitor is given by

$$P_{av} = i(t)v(t) = C\frac{dV_C(t)}{dt}V_C(t) \tag{A.9}$$

Solving (A.9) for the voltage across the capacitor $V_C(t)$ gives

$$V_C(t) = \sqrt{\frac{2\left(P_{av}t + \frac{1}{2}CV_C^2(0)\right)}{C}} \tag{A.10}$$

where $V_C(0)$ is the initial voltage on the capacitor. This suggests that a steady state voltage will never be reached as long as $P_{av} \neq 0$. A circuit implementation that approaches this theoretical device is a rectifier followed by a switched-mode boost converter with Maximum Power Point Tracking (MPPT).

Rectifier with Boost Converter

A rectifier followed by a switched-mode boost converter has a fundamentally different capacitive charging characteristic than a rectifier which is connected directly to a capacitance. When MPPT is used, the boost converter adapts its effective input resistance such that the rectifier is loaded with its optimum load

resistance and thus always delivers maximum power to the boost converter. If both the rectifier and boost converter are assumed to be 100% efficient, all of the available power is transferred to the capacitor such that the output voltage follows the same charging characteristic as described by (A.10). It therefore is expected that the charging of a capacitor to a desired voltage level can be done much more efficiently with a boost converter than using a multi-stage rectifier.

There are however some practical challenges that can limit the performance of the boost converter. Firstly, the output voltage for example will be limited by internal losses, technology related maximum voltage ratings and stability issues, which causes the capacitor voltage to reach a steady state value. Secondly, the boost converter in practice can only provide a limited range of equivalent input resistances and thus cannot always operate at the maximum power point. Thirdly, it is challenging to achieve a good power conversion efficiency for the low current levels discussed in this thesis. Recently however, Texas Instruments brought the BQ25504 boost converter to the market, which is designed specifically for energy harvesting applications. Efficiencies of nearly 80% are reported for an input current and voltage of just 10 μA and 1V, respectively [148]. This efficiency however rapidly drops for lower input power levels and thus sets a lower limit to the operating range of the boost converter. Nevertheless, a combination of a rectifier and a boost converter with MPPT seems like a feasible solution for high performance energy harvesting applications.

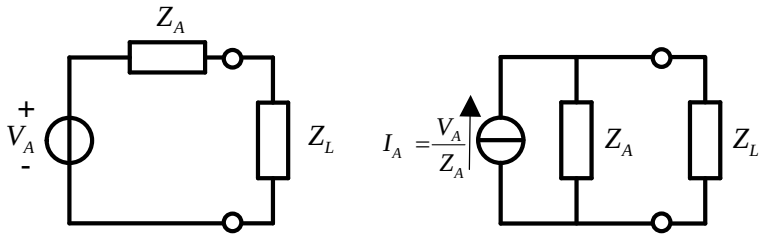
APPENDIX B

ANTENNA EQUIVALENT CIRCUIT MODEL LIMITATIONS

The antenna equivalent circuit described in Section 4.3 is often accurate enough to model the load terminal V-I characteristics of most narrowband antennas. However, it is worth to emphasize the shortcomings of this antenna model. First of all, the dielectric losses cannot be represented by simply adding another series resistance to this model, which is the case for the conduction losses. The dielectric losses have to be simulated with the antenna inside the lossy medium. Also other antenna parameters like radiation pattern, polarization and environment dependence evidently are not included into the antenna equivalent circuit model.
An interesting limitation and misconception of the receiving antenna model arises when the power dissipated in the antenna resistance R_A is referred to the re-radiated power of the antenna, which is very common in most antenna textbooks [54, 83, 84, 149]. But as was already pointed out by Silver in 1949, the power dissipated in R_A has no direct relation to the power re-radiated by the antenna and in general does not have a physical meaning [77]. The limitations of the Norton and Thévenin equivalent antenna circuit models related to re-radiation are discussed in this appendix. In the following analysis, an electrically-short antenna-electronics interface in the receiving mode is assumed.

Norton and Thévenin Circuits for Antennas in the Receiving Mode

From basic circuit theory, it is possible to model the receiving antenna as either a voltage source with series impedance or a current source with parallel



(a) Thévenin equivalent circuit. (b) Norton equivalent circuit.

Figure B.1: Equivalent circuit models for antennas in the receiving mode connected to load Z_L. (a) Thévenin equivalent circuit and (b) Norton equivalent circuit.

impedance as shown in Figure B.1. The power in the load Z_L for both the Norton and Thévenin equivalent circuit is given by

$$P_L = \frac{1}{2}\left|\frac{V_A}{Z_L + Z_A}\right|^2 \mathrm{Re}\,(Z_L) \tag{B.1}$$

It is tempting to calculate the dissipated power inside the antenna impedance Z_A and consider this as re-radiated power as previously described. When following this reasoning, it follows that the dissipated power in the Thévenin equivalent circuit equals

$$P_{A,Th\acute{e}venin} = \frac{1}{2}\left|\frac{V_A}{Z_L + Z_A}\right|^2 \mathrm{Re}(Z_A) \tag{B.2}$$

while the Norton equivalent circuit predicts a dissipated power of

$$P_{A,Norton} = \frac{1}{2}\left|\frac{V_A}{Z_L + Z_A}\right|^2 \left|\frac{Z_L}{Z_A}\right|^2 \mathrm{Re}(Z_A) \tag{B.3}$$

It thus follows that these two models are contradicting *except* for the case that $|Z_L| = |Z_A|$. An interesting paradox arises when looking at the extremes of both models. The Thévenin equivalent circuit model predicts that an antenna with an open circuit termination would not re-radiate at all, while the Norton equivalent circuit model suggests maximum power in Z_A. On the other hand, a short circuit termination causes maximum power in Z_A for the Thévenin model but no power dissipation in Z_A for the Norton model. This antenna model equivalence paradox has been recognized by some antenna engineers and heavily debated between several authors for decades [77, 149–155].

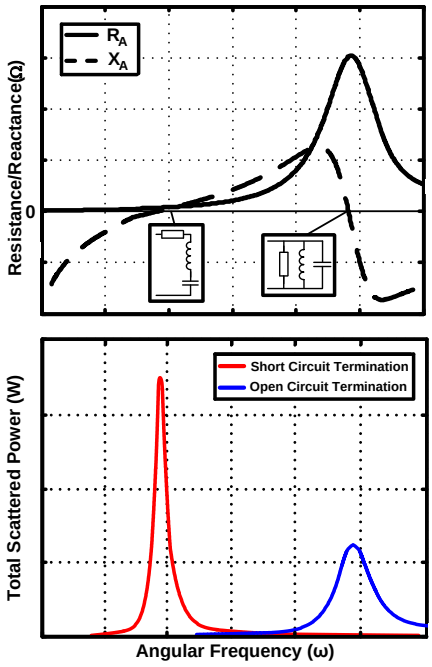


Figure B.2: (Top) Typical impedance-versus-frequency plot for a center fed dipole antenna and (bottom) Total scattered power with open and short circuit termination [82].

Of course, the Norton and Thévenin theorem can only be used to describe the V-I characteristics at the load terminal and cannot be used to compute the internal power dissipation. Still, this apparent contradiction is very noteworthy because the Thévenin model is widely used to calculate the re-radiated power from RFID tags using (B.2), which is verified experimentally and has an excellent theoretical agreement [156, 157]. Therefore, the re-radiated power calculated from the Norton equivalent circuit model seem to be incorrect in this case except for $|Z_L| = |Z_A|$. But the reason why this is so cannot be clearly answered at this point.

A plausible explanation is proposed in [82] and is related to the frequency dependence of the antenna impedance. Figure B.2 shows the impedance versus frequency of a center fed electric dipole antenna with the appropriate impedance circuit models identified near the resonance points. The antenna impedance behaves as a series RLC circuit near its natural resonant frequencies ($X_A(\omega) = 0$ and $\frac{\partial X_A(\omega)}{\partial \omega} > 0$). The antenna impedance behaves as a parallel RLC circuit near its natural anti-resonant frequencies ($X_A(\omega) = 0$ and

$\frac{\partial X_A(\omega)}{\partial \omega} < 0$).

The total simulated scattered power (re-radiated plus residual scattered fields) for the same antenna with open and short circuit termination is extracted from [82] and depicted at the bottom of Fig. B.2. Note that the antenna with a short circuit termination has only scattered power near the region where the antenna impedance behaves as a series RLC circuit. The same antenna with an open circuit termination has only scattered power near the region where the antenna impedance behaves as a parallel RLC circuit. This therefore suggests that the re-radiation model depends on the operation region of the antenna. The Thévenin equivalent circuit model should be limited to antennas that operate near the natural resonant frequency (series RLC circuit) and the Norton equivalent circuit model should be limited to antennas that operate near the natural anti-resonant frequency (parallel RLC circuits). This also explains why the Thévenin equivalent circuit model is used for most RFID backscattering calculations because the operating region of a typical RFID antenna resembles that of a series RLC circuit.

To model the antenna re-radiation characteristics in general, a more complex combination of a Thévenin and Norton equivalent circuit model is required, which recently has been proposed by Niamien [158].

APPENDIX C

SMALL SIGNAL ANALYSIS

Voltage-to-Current Converter

The voltage-to-current converter circuit implementation discussed in Section 7.4 is again depicted in Fig. C.1 without the additional switches used to define the node voltages during standby. Also the feedback capacitance C_{comp} is omitted for the initial analysis.

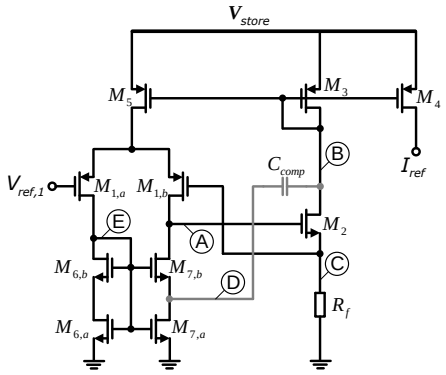


Figure C.1: Voltage-to-current converter circuit implementation.

The poles and zeros are analyzed using the equivalent small signal model in Fig. C.2 (here the self-bias loop is omitted). The differential pair with current mirror load and second stage are modeled as voltage-controlled current sources with transconductances g_{m1} and g_{m2}, respectively. The additional poles and zeros introduced by the differential pair are discussed separately.
Due to the feedback configuration and the relatively high output resistance of

M_2, the load $1/g_{m3}$ can be assumed to be significantly smaller than the amplifier's output resistance and thus has little affect on the loop gain. Therefore, C_{gd2} is connected from node A to ground and r_{o2} is assumed infinite to simplify the analysis. The load capacitance C_B represents the sum of capacitance at node B to AC ground. The DC voltage reference at the input is modeled as a voltage source with a large series resistance (R_s) and a large parallel capacitance (C_s) which is used as filter and buffer. Since $C_s \gg C_{gs1}$, it can be assumed that the positive node of C_{gs1} is grounded for loop gain calculations. The source impedance therefore also does not affect the loop gain.

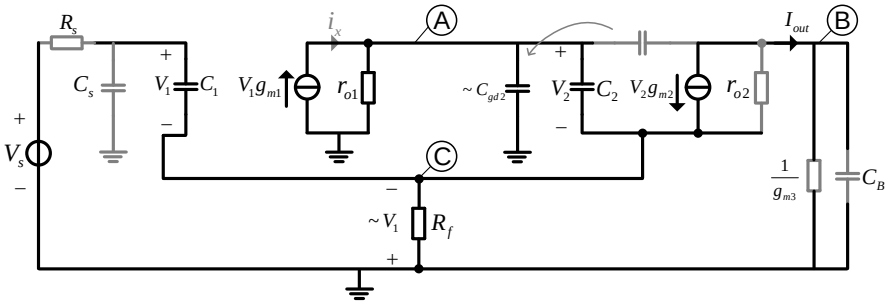


Figure C.2: Voltage-to-current small signal model.

The loop gain L is obtained by first making the voltage-controlled current source at the input uncontrolled and defining its output current as i_x. Subsequently, the transfer function is calculated from i_x to its input V_1 and multiplied with the transfer of the assumed uncontrolled source:

$$L = \frac{V_1}{i_x} g_{m_1} \tag{C.1}$$

To find $\frac{V_1}{i_x}$, the currents at node A are summed using Kirchhoff's Current Law:

$$-i_x + \frac{V_2 - V_1}{r_{o1}} + (V_2 - V_1)\, sC_{gd2} + V_2 sC_{gs2} = 0 \tag{C.2}$$

The currents at node C are summed as

$$V_2 sC_{gs2} + g_{m2} V_2 + \frac{V_1}{R_f} + V_1 sC_{gs1} = 0 \tag{C.3}$$

Rewriting (C.3) for V_2 yields

$$V_2 = -V_1 \frac{sR_f C_{gs1} + 1}{R_f \left(sC_{gs2} + g_{m2}\right)} \tag{C.4}$$

Substituting V_2 in (C.2) and using $L = \frac{V_1}{i_x} g_{m_1}$, the loop gain is found to be

$$L(s) = \frac{-\frac{g_{m1} g_{m2} r_{o1} R_f}{g_{m2} R_f + 1} \left(s \frac{C_{gs2}}{g_{m2}} + 1 \right)}{s^2 \frac{r_{o1} R_f \xi}{g_{m2} R_f + 1} + s \frac{R_f (C_{gs1} + C_{gs2}) + r_{o1} (C_{gs2} + C_{gd2} (R_f g_{m2} + 1))}{g_{m2} R_f + 1} + 1} \tag{C.5}$$

where $\xi = C_{gs1} C_{gs2} + C_{gd2} C_{gs1} + C_{gd2} C_{gs2}$.
The DC loop gain $L(0)$ is thus given by

$$L(0) = -\frac{g_{m1} g_{m2} r_{o1} R_f}{g_{m2} R_f + 1} \tag{C.6}$$

The loop gain contains a zero in the left half plane, which corresponds to the frequency where two currents of opposite polarity combine at node C via C_{gs2} and g_{m2}. The location of this zero (in Hz) is given by

$$z_1 = -\frac{g_{m2}}{2\pi C_{gs2}} \tag{C.7}$$

To estimate the two pole positions, the denominator D of (C.5) can be written in the general form of

$$D = \left(\frac{s}{p_1} - 1 \right) \left(\frac{s}{p_2} - 1 \right) \tag{C.8}$$

$$= s^2 \frac{1}{p_1 p_2} - s \left(\frac{1}{p_1} + \frac{1}{p_2} \right) + 1 \tag{C.9}$$

If it is assumed that $|p_1| \ll |p_2|$, which is common in many amplifier circuits [70], then the coefficient of s in (C.9) is approximately equal to $-\frac{1}{p_1}$. In this case it follows that the dominant pole is located at

$$p_1 \approx -\frac{g_{m2} R_f + 1}{2\pi \left[R_f (C_{gs1} + C_{gs2}) + r_{o1} (C_{gs2} + C_{gd2} (R_f g_{m2} + 1)) \right]} \tag{C.10}$$

If $r_{o1} (C_{gs2} + C_{gd2} (R_f g_{m2} + 1)) \gg R_f (C_{gs1} + C_{gs2})$, then (C.10) simplifies to

$$p_1 \approx -\frac{1}{2\pi r_{o1} (\frac{C_{gs2}}{R_f g_{m2} + 1} + C_{gd2})} \tag{C.11}$$

The second pole is estimated by equating the coefficient of s^2 in (C.9) to the coefficient of s^2 in (C.5):

$$\frac{r_{o1}R_f\left(C_{gs1}C_{gs2}+C_{gd2}C_{gs1}+C_{gd2}C_{gs2}\right)}{g_{m2}R_f+1}=\frac{1}{p_1p_2} \tag{C.12}$$

Again when assuming that $r_{o1}(C_{gs2}+C_{gd2}(R_fg_{m2}+1))\gg R_f(C_{gs1}+C_{gs2})$, the second pole is located at approximately

$$p_2\approx-\frac{C_{gs2}+C_{gd2}(R_fg_{m2}+1)}{2\pi R_f\left(C_{gs1}C_{gs2}+C_{gd2}C_{gs1}+C_{gd2}C_{gs2}\right)} \tag{C.13}$$

Poles and Zeros of a Differential Pair with Current Mirror Load

The current mirror pole associated with node E in Fig. C.1 can readily be found by summing the total capacitance to ground at node E, denoted by C_E, and multiply this with the total resistance seen to ground:

$$p_3\approx-\frac{g_{m6}}{2\pi C_E} \tag{C.14}$$

where g_{m6} denotes the transconductance of the current mirror transistor. To find the locations of the zeros, the equivalent circuit of Fig. C.3 is used, where it is assumed that $M_{1,a}=M_{1,b}$ and $M_6=M_7$. The zeros are found by noting that the differential to single-ended transfer function $\frac{V_A(s)}{V_{in}(s)}$ must drop to zero at the (complex) frequency of the zero. This means that the output (node A) can be shorted to ground while requiring that I_{out}=0 [70].

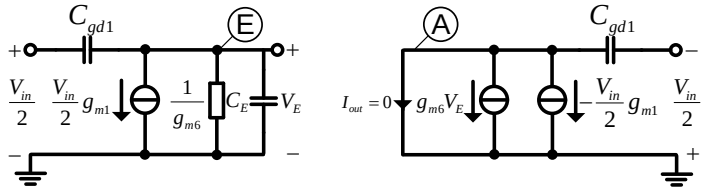


Figure C.3: Small signal model of a differential pair with current mirror load to determine the transfer zeros.

First, the currents at node E are summed to find the voltage V_E:

$$\left(V_E-\frac{V_{in}}{2}\right)sC_{gd1}+g_{m1}\frac{V_{in}}{2}+V_Eg_{m6}+V_EsC_E=0 \tag{C.15}$$

resulting in

$$V_E=\frac{V_{in}}{2}\frac{sC_{gd1}-g_{m1}}{s\left(C_{gd1}+C_E\right)+g_{m6}} \tag{C.16}$$

Then, the currents at node A are summed

$$g_{m6}V_E - g_{m1}\frac{V_{in}}{2} + \frac{V_{in}}{2}sC_{gd1} = 0 \tag{C.17}$$

Substituting (C.16) into (C.17) and rearranging to the general form gives

$$-s^2\frac{C_{gd1}\left(C_{gd1}+C_E\right)}{2g_{m1}g_{m6}} + s\frac{g_{m1}\left(C_{gd1}+C_E\right) - 2C_{gd1}g_{m6}}{2g_{m1}g_{m6}} + 1 \tag{C.18}$$

Assuming that $|z_1| \ll |z_2|$, the dominant zero is found at

$$z_{diff,1} \approx -\frac{2g_{m1}g_{m6}}{g_{m1}\left(C_{gd1}+C_E\right) - 2C_{gd1}g_{m6}} \tag{C.19}$$

The second zero is located at

$$z_{diff,2} \approx \frac{g_{m1}\left(C_{gd1}+C_E\right) - 2C_{gd1}g_{m6}}{C_{gd1}\left(C_{gd1}+C_E\right)} \tag{C.20}$$

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SUMMARY

Emerging applications such as Internet of Things (IoT), smart buildings and warehouse inventory management are important driving forces behind the development of Wireless Sensor Nodes (WSNs). With future advancements made in the semiconductor industry, these WSNs are expected to become smaller, cheaper, more reliable and with improved functionality. The prospect of *energy scavenged* WSNs is to eliminate the burden of battery replacement, thereby significantly saving on maintenance costs in large WSN networks.

This dissertation focuses on the research, design and implementation of various circuit blocks and the system integration of energy scavenged WSNs used in the aforementioned applications. To select a suitable energy harvester, four different energy harvesting approaches are discussed: vibrational, thermal, photovoltaic and RF. Of these harvesters, it shows that RF-powered WSNs have the distinct advantage over WSNs using other forms of energy harvesting that they are low cost and can operate wirelessly in a large variety of applications, even in cold, dark and static environments. Moreover, additional advantages such as utilizing a dedicated RF source for both energy harvesting as well as the generation of a reference frequency greatly reduces the complexity and power consumption of the WSN.

A co-design methodology is presented to optimize the interface between the RF energy harvester and the WSN electronics for maximum sensitivity, efficiency and output power. First, general co-design principles for antenna-electronics interfaces in the receiving mode are introduced, which includes optimum reception of wireless information and wireless power. It is shown that the choice of interface impedance plays a crucial role during the optimization procedure and that, besides maximum power transfer, the interface needs to be optimized for either voltage or current, depending on which is more favorable for the electronics. Design examples are given to, for example, improve noise figure, efficiency and sensitivity without increasing power

consumption.

Based on the presented co-design principles, a CMOS rectifier and a compact loop antenna are presented for a highly sensitive RF energy harvester. A 5-stage cross-connected differential rectifier with a complementary MOS diode in the last rectifying stage is designed that significantly improves the harvester's ability to store and hold energy over a longer period of time than a conventional MOS diode. A low resistive and high-Q interface is utilized to obtain good sensitivity. To compensate variations at the interface, a control loop with a 7-bit binary-weighted capacitor bank is proposed that provides self-calibration. The chip is implemented in TSMC 90 nm CMOS technology, includes ESD protection and is directly mounted on the backside of the custom designed antenna. Measurements in an anechoic chamber at 868 MHz demonstrate an end-to-end maximum PCE of 40% and a sensitivity of -27 dBm to generate 1V across a capacitive load. In an office corridor, 1V could be generated from a 1.78 W RF source at 27 meter distance.

A high efficiency tuned switching Power Amplifier (PA) is proposed for < 0 dBm output power. It is shown theoretically that an optimum duty cycle exists for maximum drain efficiency for a given switch and effective load resistance. To set this duty cycle, an on-chip duty cycle calibration loop is proposed that fixes the duty cycle over PVT variations. A 2.4 GHz PA prototype is implemented in 40nm CMOS technology and supports On-Off Keying (OOK) modulation with pulse shaping capabilities. A global efficiency of 40% is achieved when delivering -5 dBm to a 50 Ω load, which compares favorably to the state-of-the-art. Due to the introduced memory in the duty cycle calibration loop, the rise and fall times are kept below 3.3 ns, making high data rate OOK modulation feasible.

The findings in this thesis have been used for the system integration of a compact RF-powered DLL-based 2.4 GHz CMOS transmitter. The received dedicated RF signal is used for both RF energy harvesting as well as frequency synthesis. An RF energy harvester with a nanowatt power management circuit harvests and subsequently monitors the energy in the storage capacitor to determine when enough energy is accumulated to initiate wireless data transmission. Once the voltage regulator and bias current circuit blocks are enabled, the incoming RF carrier is extracted and used as frequency reference. The frequency synthesizer consits of a frequency divider, Delay Locked Loop (DLL) and XOR-based frequency multiplier and thus allows for a compact integrated solution. All building blocks have been implemented in 40 nm CMOS technology and occupy only 0.16 mm^2. Experimental results show a maximum rectifier efficiency of 36.83% at -11.47 dBm. In harvesting mode,

the complete power management circuit only consumes 120 nA. For a 1 μF storage capacitor and -18.4 dBm minimum available power at 915 MHz RF input, the TX outputs a continuous 2.44 GHz RF signal of -2.57 dBm for 128 μs with 36.5% PA drain efficiency and 23.9% global efficiency. The complete TX consumes 1.46 mW during OOK modulation at 0.5 Mbps.

SAMENVATTING

Opkomende toepassingen zoals Internet of Things (IoT), smart buildings en magazijn voorraadbeheer zijn belangrijke drijvende krachten achter de ontwikkeling van draadloze sensor-knooppunten (Eng: Wireless Sensor Nodes, WSNs). In het licht van de toekomstige vooruitgang in de halfgeleiderindustrie is de verwachting dat deze WSNs kleiner, goedkoper en betrouwbaarder worden met verbeterde functionaliteit. Het vooruitzicht van de energie-oogstende WSNs is om de last van het vervangen van de batterij te elimineren om zo aanzienlijk te besparen op onderhoudskosten in grote WSN-netwerken.

Dit proefschrift richt zich op het onderzoek, ontwerp en de implementatie van verschillende circuit-blokken en de systeem integratie van energie-oogstende WSNs voor de eerder genoemde toepassingen. Om een geschikte energie-oogster te selecteren, worden vier verschillende manieren van energie-oogsting besproken: vibratie, thermisch, fotovoltaïsch en RF. Na beschouwing van deze vier manieren van energie-oogsting, blijkt dat RF-gevoede WSNs duidelijke voordelen hebben ten opzichte van WSNs die gebruik maken van andere energie-oogsters omdat ze goedkoop en draadloos kunnen opereren in een groot aantal toepassingen, zelfs in koude, donkere en statische omgevingen. Bijbehorende voordelen, zoals het gebruik maken van een RF-bron gewijd aan zowel het oogsten van energie als aan het opwekken van een referentie-frequentie vermindert de complexiteit en het vermogensverbruik van de WSN.

Een ontwerp-methodologie is gepresenteerd om de interface tussen de RF energie-oogster en de WSN-elektronica te optimaliseren voor maximale gevoeligheid, efficiëntie en uitgangsvermogen. Eerst zijn de algemene ontwerp-principes voor antenne-elektronica interfaces in de ontvangst-modus geïntroduceerd, welke de optimale ontvangst van draadloze informatie en draadloos vermogen omvatten. Het is aangetoond dat de keuze van de interface-

impedantie een cruciale rol speelt tijdens de optimalisatie-procedure en dat, naast maximale vermogensoverdracht, de interface moet worden geoptimaliseerd voor spanning of stroom, afhankelijk van wat gunstiger is voor de elektronica. Ontwerp-voorbeelden worden gegeven om bijvoorbeeld het ruisgetal (Eng: noise figure), de efficiëntie en gevoeligheid te verbeteren zonder toename van het vermogensverbruik.

Op basis van bovenstaande ontwerp-principes zijn een CMOS gelijkrichter en een compacte lus-antenne gepresenteerd voor een zeer gevoelige RF energie-oogster. Een vijf-traps kruislings-gekoppelde differentiële gelijkrichter met een complementaire MOS-diode in de laatste gelijkrichttrap is ontworpen en maakt het mogelijk voor de energie-oogster om de energie op te slaan en vast te houden over een significant langere tijdsperiode dan een conventionele MOS diode. Een laag-ohmse en hoge-Q interface wordt gebruikt om een goede gevoeligheid te realiseren. Om variaties in de interface te compenseren, wordt een regellus met een 7-bit binair-gewogen capaciteiten-bank voorgesteld die zelf-kalibratie biedt. De chip is geïmplementeerd in TSMC 90 nm CMOS-technologie, bevat beveiliging tegen ESD en is direct gemonteerd op de achterzijde van de speciaal ontworpen antenne. Metingen in een anechoïsche kamer bij 868 MHz tonen een eind-tot-eind maximum PCE van 40% en een gevoeligheid van -27 dBm om 1V te genereren over een capacitieve belasting. In een kantoor gang kon 1V worden gegenereerd uit een 1,78 W RF-bron op 27 meter afstand.

Een hoog-efficiënte afgestemde schakelende vermogensversterker (Eng: Power Amplifier, PA) is voorgesteld voor < 0 dBm uitgangsvermogen. Het is theoretisch aangetoond dat er een optimale duty-cycle bestaat voor maximale drain-efficiëntie voor een gegeven schakelaar en effectieve belastingsweerstand. Om deze duty-cycle in te stellen, is een on-chip duty-cycle kalibratie-lus voorgesteld die de duty-cycle over PVT-variaties vastlegt. Een 2,4 GHz PA-prototype is geïmplementeerd in 40nm CMOS-technologie en ondersteunt On-Off-Keying (OOK) modulatie met mogelijkheden tot pulsvorming. Een globale efficiëntie van 40% is behaald voor -5 dBm uitgangsvermogen in een 50 Ω belasting, wat gunstig vergelijkt ten opzichte van vergelijkbare vermogensversterkers gepubliceerd in de huidige literatuur. Vanwege het geïntroduceerde geheugen in de duty-cycle kalibratie-lus zijn de stijg-en daaltijd onder de 3.3 ns gehouden, wat een hoge OOK-modulatie datasnelheid mogelijk maakt.

De bevindingen in dit proefschrift zijn gebruikt voor de systeemintegratie van een compacte RF-gevoede DLL-gebaseerde 2,4 GHz CMOS zender (Eng:

Transmitter, TX). Het ontvangen signaal van een toegewijde RF-bron wordt gebruikt om zowel RF-energie te oogsten als voor frequentiesynthese. Een RF energie-oogster met een nanowatt vermogensbeheer-circuit oogst en meet vervolgens de energie in de opslagcondensator om te bepalen wanneer voldoende energie verzameld is om draadloze gegevensoverdracht te initiëren. Zodra de spanningsregelaar-en instelstroom circuit-blokken zijn ingeschakeld, wordt de binnenkomende RF-draaggolf onttrokken en gebruikt als frequentie-referentie. De frequentie-synthesizer bestaat uit een frequentiedeler, een Delay Locked Loop (DLL) en een XOR-gebaseerde frequentievermenigvuldiger, wat een compacte geïntegreerde oplossing mogelijk maakt. Alle circuits zijn in 40 nm CMOS-technologie geïmplementeerd en nemen slechts een oppervlakte van 0,16mm^2 in. Experimentele resultaten tonen een maximale gelijkrichter-efficiëntie van 36,83% bij -11.47 dBm. Tijdens het energie-oogsten verbruikt het vermogensbeheer-circuit slechts 120 nA. Voor een 1 μF opslagcondensator en -18,4 dBm minimaal beschikbaar vermogen bij een RF ingangssignaal van 915 MHz, genereert de TX een continu 2,44 GHz RF-signaal van -2,57 dBm voor 128 μs met 36,5% PA drain-efficiëntie en 23,9% globale efficiëntie. De complete TX verbruikt 1,46 mW tijdens 0,5 Mbps OOK modulatie.

List of Publications

Journal Publications

M. Stoopman, K. Philips and W.A. Serdijn, "An RF-Powered DLL-based 2.4 GHz Transmitter for Autonomous Wireless Sensor Nodes", *Transactions on Microwave Theory and Techniques, IEEE*, minor revisions under review, Aug. 2016.

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M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips and W.A. Serdijn, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters", *Journal of Solid-State Circuits, IEEE*, Vol. 49, No: 3, page 622-634, March 2014.

A.T. de Hoop, **M. Stoopman**, W.A. Serdijn and I.E. Lager, "Equivalent Thévenin and Norton Kirchhoff circuits of a receiving antenna", *Antennas and Wireless Propagation Letters, IEEE*, Vol. 12, page 1627-1629, Dec. 2013.

BOOK CHAPTER

W.A. Serdijn, A.L.R. Mansano and **M. Stoopman** "Introduction to RF Energy Harvesting", Wearable Sensors, Elsevier Inc Academic Press, San Diego, page 299 - 322, 2014, ISBN: 978-0-12-418662-0.

CONFERENCE PUBLICATIONS

M. Stoopman, S. Keyrouz, H.J. Visser, K. Philips and W.A. Serdijn,, "*Co-design of a 90 nm CMOS Rectier and Small Loop Antenna for large range RF Energy Harvesters*", Progress In Electromagnetics Research Symposium (PIERS), Stockholm, Sweden, Aug. 12-15, 2013**.**

M. Stoopman, S. Keyrouz, H.J. Visser, K. Philips and W. A. Serdijn, "A Self-Calibrating RF Energy Harvester generating 1V at -26.3 dBm", *IEEE Symposium on VLSI Circuits (VLSIC)*, Kyoto, Japan 2013**.**

M. Stoopman, W.A. Serdijn, K. Philips, "*A Novel Robust and Large Range RF Energy Harvester with Resonance Control Loop*", 2nd International Workshop on Wireless Energy Transport and Harvesting (IWWETH), Leuven, Belgium, May 2012**.**

M. Stoopman, W. A. Serdijn and Kathleen Philips: "A Robust and Large Range Optimally Mismatched RF Energy Harvester with Resonance Control Loop", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, South Korea, May 2012**.**

M. Stoopman and W.A. Serdijn*,* "A sub-GHz UWB Pulse Generator for Wireless Implantable Medical Devices", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, San Diego, USA, Nov. 2011.

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The fact that a bunch of transistors (i.e., sand) tied together in a specific way can be used to wirelessly transmit information is mind-boggling when thinking about it for a brief moment. Connecting the same transistors in a different way may result in a completely different circuit that can be useful in for example a refrigerator or a TV remote. The endless possible circuit configurations and topologies that can be invented or (re)used to solve a specific design problem to me is very exiting and challenging. It therefore has been a privilege to spend the last four and a half years as a PhD researcher at Delft University of Technology and Imec/Holst Centre in Eindhoven.

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Mark Stoopman was born in Rotterdam, the Netherlands, in 1983. He received the M.Sc. degree in Electrical Engineering from Delft University of Technology, the Netherlands in 2010 for his thesis entitled "*A Sub-GHz UWB Pulse Generator for Wireless Biomedical Communication*". In December 2010 he started as a PhD candidate at the same university in close cooperation with Imec/Holst Centre, the Netherlands. His research interests include RF Analog IC Design, wireless power transfer and harvesting, antenna-electronics interface optimization, feedback systems, power management and biomedical electronics. In August 2015 he joined Catena Microelectronics Delft as an Analog/RF design engineer.