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Modeling Soft-Error Reliability Under Variability

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***Abstract*—The Soft-Error (SE) reliability and the effects of Negative Bias Temperature Instability (NBTI) in deep submicron technologies are characterized as the major critical issues of high-performance integrated circuits. The previous scientific research studies provide a comprehensive description that the soft-error vulnerability becomes more severe as the circuit performance degrades with aging. The main reason is the reduction of cell-level critical charge in an aging environment. However, such increased soft-error generation does not necessarily contribute towards circuits' critical functional failures. The proposal of this paper is the experimental investigation of soft error propagation at the aged gate-level by considering the different derating factors like Electrical Derating (EDR), Temporal Derating (TDR), Logical Derating (LDR), and Functional Derating (FDR). As contrary to the previous studies, the results of this work prove that SEU fault propagation probability is reducing in critical paths as time advances while the propagation probability of SET faults is neither reducing nor increasing, but the spot of generation of failure enhancing SETs is shifting within the clock period.**

I. Introduction

System engineering continuously focuses on the aggressive technology scaling which increases the vulnerability of radiation-induced soft-errors [1] [2]. Simultaneously, the time-dependent variabilities like the effects of Bias Temperature Instability (BTI) expedite the reliability assessment of high-performance Cyber-Physical Systems (CPS) into an increasingly challenging job.

Scientific efforts significantly highlighted the relevance of experiments that account for the impact of aging on soft-error reliability. The works [3], [4] and [5] have proposed their methods and chronicled their observations on soft-error susceptibility under circuit aging. A. Gebregiorgis in [6] has presented a cross-layer reliability analysis in the presence of soft-errors, aging, and process variation effects. Similarly, the work [7] provides ramification of aging and temperature on Propagation Induced Pulse Broadening (PIPB) effect of Single Event Transient (SET) pulse for nano-scale CMOS. In [8], F. L. Kastensmidt shows that aging and voltage scaling enhance the Soft Error Rate (SER) susceptibility of SRAM-based FPGAs by two times.

However, the above-cited articles mainly focussing on the increased occurrence of radiation-induced errors on behalf of the declined critical charge Q_{crit} at the technology cells. The SER is not observed in diverse propagational forms of SET and Single Event Upset (SEU) separately. Contrary to previous findings, our results concentrate on the soft-error generation and propagation by considering all the derating factors (EDR, LDR, TDR and FDR) associated with an aged Standard Delay Format (SDF) file. The soft-error reality analysis of aged circuits at higher abstraction (e.g., RTL) is the future vision of this work. The relevant contributions of the paper to the soft-error reliability analysis under aging include the following,

- **Characterization of threshold voltage degradation (ΔV_{th}) for industrial 15 nm technology**
- **Cross-level Modeling of NBTI-induced delay degradation using Artificial Intelligence (AI)**
- **Analysis of derating factors' influence in soft-error propagation and proposing a signal-processing model to locate propagating SETs**

The main motivation of the work is to investigate the soft-error reliability challenges at low-scaled (e.g., 15-nm) technologies with time-dependent voltage variabilities. The downscaled technology results in clock-frequency maximization and provides soft-error propagation a high sensitivity to the path delay variations in the design due to aging. In this work, aging effects are limited to the NBTI. The Positive Bias Temperature Instability (PBTI) remains unconsidered throughout the research based on the facts: the PBTI effect for the NFET transistors at small scale technologies for the High Performance (HP) applications is comparatively low compared to the NBTI effect for PFET transistors [9]. Also, the PBTI effect's dependence on the quality of gate-oxide materials [10] and the complexities in the efficacy to model PBTI's relative voltage degradation, are more than the intended research focus. However, the deduced conclusions for NBTI can extend to the combined effect of NBTI and PBTI.

The paper organized the rest as follows: sections II, III, IV, and V. Section II covers the mathematical formulation of NBTI-induced voltage degradation and cross-level modeling of NBTI-induced delay degradation. The overall experimental setup is briefed in Section III. Section IV explains the results and discussions. Finally, a conclusion to the holistic approaches is provided in section V.

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II. Background

A. Modeling NBTI induced voltage degradation

The primary work of this research activity is to find a mathematical abstraction to estimate the changes in threshold voltage ΔV_{th} due to the NBTI process in the aged circuits, and completely revised from the original papers [11] and [12]. The paper [11] has presented a predictive model for the Negative Bias Temperature Instability (NBTI) of PMOS under both short-term and long-term operations. This model has

TABLE I
Parameters and Units for NBTI Predictive Modeling

Symbol	Quantity	Numerical value in SI unit
K_v	Technology Constant	6.1773e-11
C	Temperature Dependence	2.2987e-12
T_0	Constant	10^{-8} (s/nm^2) $\rightarrow$ 10^{10} (s/m^2)
E_0	Technology-Independent	0.08 V/nm $\rightarrow$ 0.08e9 V/m
E_a	Technology Independent	0.13 eV $\rightarrow$ 2.08260e-20 J
k	Boltzmann Constant	1.38e-23 m^2 kg s^{-2} K^{-1}
$1/n$	H_2 Diffusion Model	1/6
t_{ox}	Oxide Thickness	0.9 * 10e-9 m
ξ_1	Back Diffusion Const.	0.9
ϵ_{ox}	Oxide Permittivity	$3.9 * 8.854 * 10^{-12}$ F/m
K_1	Model Constant	7.5e22.5 $C^{-0.5}$ $m^{-2.5}$
E_{ox}	Electric Field (gate oxide)	27.7e-7 V/m

Unit Abbreviations: K = Kelvin, F = Farad; V = Volt, s = Second, m = Meter, nm = Nano-meter, J = Joule, kg = Kilogram.

comprehensively apprehended NBTI dependence on the key transistor-design parameters, based on the reaction-diffusion (R-D) mechanisms. The work in [11] presented a quality model accuracy verification with 90-nm technology while [12] reassured that with industrial 65-nm technology. A characterization of threshold voltage (ΔV_{th}) degradation due to NBTI for 15-nm technology cells, has been presented through this paper, where the models from [11] and [12] are integrated with 15-nm technology parameters as in Table I. A model for the $\Delta V_{th,t}$ considering the long-term effect of NBTI is provided in [11]. At high frequencies, the threshold voltage degradation of long-term evaluation is independent of the frequency [11] [13]. So the ΔV_{th} at time 't' can be written as [11]:

$$\Delta V_{th,t} \approx \left(\frac{n^2 K_v \alpha C t_1 t}{\xi_1^2 t_{ox}^2 (1-\alpha)} \right)^n \tag{1}$$

The parameter α in (1) is the duty-cycle that defines the signal probability in a clock period. Equation (1) refers to the dynamic NBTI, $\forall\, \alpha \in [0,1]$. As $\alpha \rightarrow 1$, (1) is attributed to the static NBTI that corresponds to the case of PMOS under constant stress. A graph between ΔV_{th} and α, at $t = 1$ year is given in Fig. 1. The upper-limit of the degradation model (1) is estimated by a power law model [14] as privided in (2). The static ΔV_{th} calculation at t = 1 year gives 7mV that fits the trends of static ΔV_{th} of various technology-nodes as given in PTM models [15] [16].

$$|\Delta V_{th,t}| = ({K_v}^2 t)^n \tag{2}$$

The formula in (1) is deduced into a simpler form by substituting the parameters of 15nm technology and follows the form of (3), where relation of technology specific factors is represented as separate form.

$$|\Delta V_{th,t}| \simeq \underbrace{\left(\frac{n^2 K_v C t_1}{\xi_1^2 t_{ox}^2} \right)^n}_{\text{Technology dependent}} t^n \left(\frac{\alpha}{1-\alpha} \right)^n \tag{3}$$

B. An AI revolution for NBTI predictive model

The gate-delay degradations of 15-nm technology library cells are characterized through the SPICE simulation at the transistor level. A neural network called Long Short-Term Memory (LSTM) is a perfect method to predict the future delays from past delay (Δt) samples even without an input like ΔV_{th}. Fig. 2 depicts the complete results of LSTM modeling, where the predicted values from previous samples are shown in blue. However, the LSTM model is not a completely dependable one here for generating a delay Δt for the current input ΔV_{th} in a timely important simulation environment. To simplify the exhaustive fault-injection experiment, a Machine Learning (ML) model called Support Vector Machine (SVM) is used to automate the simulation data. Previous scientific literatures [17] and [18] presented a simple polynomial function for modeling variation between Δt and ΔV_{th}. In this work, SVM can perform as a comprehensive model generator for a triangular relation between α, time 't', and Δt, where ΔV_{th} is hidden in the SVM model. The AI revolution is implicitly referring to such complex and compact modeling of indirectly related multi variables. Fig. 3 delegates a SVM model for an inverter. Once SVM is trained offline, it will become a fast online computing model generator of Δt for the inputs α and time 't'. This compact ML model is very much straightforward in exporting the variability from the transistor level to the gate level. Another important factor to choose SVM over LSTM is the low static ΔV_{th} (7mV at t=1 year) by (3), because a large simulation data needs to train LSTM as provided in Fig. 2, where ΔV_{th} ranges from 0 to 0.4V, while ΔV_{th} in Fig. 3 perfectly follows the ΔV_{th} values as provided in Fig. 1.

III. Methodology

A. Phase I: Fault-Injection Campaign

Single Event Effects (SEEs) are the consequences of interactions between the circuit and the radiation particles. SEUs and SETs are widely used here as the prominent representatives of SEEs. The use-case for SEU fault mainly implies an inversion of the stored value in a flip-flop until the clock period changes. The SET represents a transient pulse of arbitrary width at the gate and having the probability to propagates and latches to the downstream sequential element. Fig. 4 shows a block diagram of the fault-injection campaign that infers the statistical functional failure metrics of SEU/SET events. The mathematical model for Functional Failure Rate ($FFR_{i,seu}$) of an SEU event is described in (4) and the Functional Failure Rate due to SET ($FFR_{i,set}$) is formulated in (5).

$$FFR_{i,seu} = FIT \cdot TDR \cdot LDR \cdot FDR \tag{4}$$

$$FFR_{i,set} = FIT \cdot EDR \cdot TDR \cdot LDR \cdot FDR \tag{5}$$

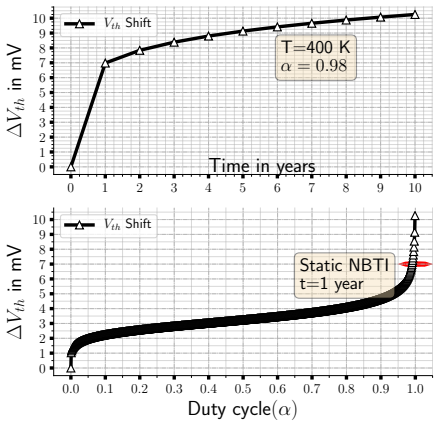

Fig. 1. Mathematical Analysis

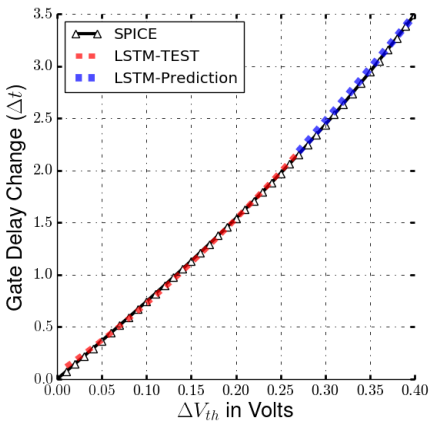

Fig. 2. LSTM Model (Inverter)

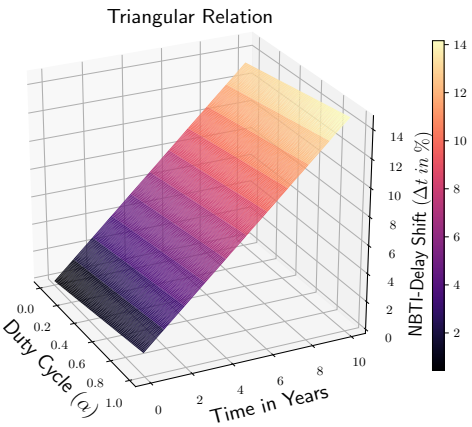

Fig. 3. SVM-Regression Model (Inverter)

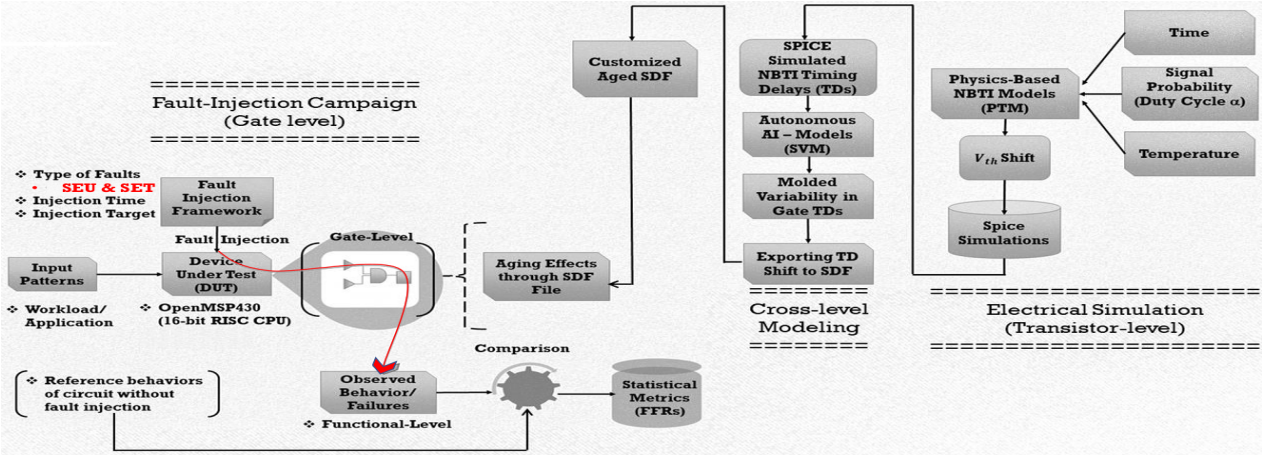

Fig. 4. Delineation of Aging Aware Fault-Injection Framework

where FIT denotes the rate of soft errors at the i^{th} flip-flop/gate in the Failure-In-Time (FIT) unit. Electrical Derating (EDR), Temporal Derating (TDR), Logical Derating (LDR), and Functional Derating (FDR) are more sophistically portrayed in Fig. 5. The classical explanations for each derating factors are available in [1].

B. Phase II: Aging aware gate-level circuit

Fig. 4 represents how an injected fault propagates through the aged circuits. Circuit aging is modeled through degraded propagation delay as the result of the NBTI process at PMOS transistors. Sophisticated cross-layer modeling is also demonstrated in Fig. 4. A way more experimentally proved and scientifically adapted physics-based NBTI models (3) are employed to generate the V_{th} shifts.

Electrical simulations have been carried out using SPICE. Voltage sources have been injected in the gate of PMOS transistors to model the V_{th} shift caused by aging. The voltage introduced by the source was then swept from 0V to 0.4V to represent the effects of different levels of aging. The impact of aging on each logic gate is estimated by measuring the input-to-output time delay, i.e., the time delay from when the input is in $V_{DD}/2$ to when the output rises from '0' to '1' at the $V_{DD}/2$ mark. The spice simulation is conducted for 23 gates from a 15-nm Nangate library which including inverter (NOT), AND, OR, NAND, NOR, XOR, XNOR with input combinations ranging from 2 to 4. The transistor model (SPICE Model Card) for 15-nm Nangate library is customized from HP Predictive Technology Models (PTM) [16].

After the simulation process, the change in propagation delays of combinational cells is submitting to AI models. Fig. 4 depicts the significance of AI models in cross-layer modeling. A versatile model by SVM is used to generate the propagation delay change Δt as a function of duty cycle (α) and time in years. This model is very easy to port to gate-level or even to a higher hierarchical level, and adequately producing Δt values by concurrently changing time and signal probability. Those model-driven values are numerically very close to the original simulation Δt and the test phase of SVM confirms that the Mean Squared Error (MSE) is less than 2% for the given test data.

After testing the compatibility and quality of the model, the model outputs (Δt) are exported to the SDF file. A customized SDF file introduces time-dependent variability at the gate level.

The customization of the SDF file means altering the value under the keyword entry called 'IOPATH' that indicates the gates' Input-Output path delay. Before changing the gates' 'IOPATH' values, corresponding signal probabilities and signal transitions at each terminal are pre-estimated through signal-activity analysis through Verilog Procedural Interface (VPI) functions and Value Change Dump (VCD) files by Modelsim. So that, the changed values should coincide with the real-time input and output transitions between '0' and '1'. To process the above-explained cumbersome work for large IEEE standard SDF files, then a dedicated algorithm is written in python, and the corresponding pseudo-code is presented in Algorithm 1. The algorithm generates an IEEE standard customized aged SDF file that provides an aged behavior while injecting SEUs/SETs in a simulation environment.

Result: **Customized Aged SDF File**
Estimate ΔV_{th} for 10 years $\forall$ used gates $\in$ Tech.lib;
for *Each used Tech.lib gate* **do**
  for *Each 'i'* $\in$ *SVM model Training* **do**
    SVM : input vector [α_i, time$_i$, ΔV_{th_i}] $\mapsto$ Δt_i ;
  end
  Test SVM model and Save in Python script;
end
Read the SDF file in IEEE standard format;
for *Each cell instance in SDF File* **do**
  Identify the Tech. library cell name ;
  Calculate signal probability (α) from VCD file ;
  if *[α_i, time$_i$] given* **then**
    Calculate ΔV_{th_i} by (3) ;
    SVM.gate = Load trained SVM.gate kernel;
    Δt_i = SVM.gate.predict([α_i, time$_i$, ΔV_{th_i}]) ;
    Update the instance's IOPATH in SDF file;
  end
end

Algorithm 1: IEEE Standard Aged SDF File

IV. Results and Discussions

A. Device Under Test

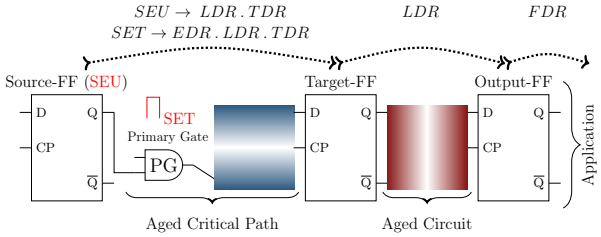

Fig. 5. From SEU/SET Fault to Failure

The case studies are conducted by gate-level circuits of the openMSP430 cores, a 16-bit microcontroller (μC) which is synthesized by the 15-nm NanGate Open Cell Library. As per the static timing analysis of the test case circuit, the critical paths contain a maximum path delay of 250ps. The CPU unit in the MSP430 μC is executing the application 'sandbox' by sourcing a clock period of 2ns. The Fig. 5 demystifies the propagation of SEU/SET faults to the circuit function.

B. Aging impact on SEU fault propagation

The NBTI effect is modeled in terms of propagation delay Δt of logic gates. The setup and hold time constraints of flip-flops dictate the maximum and minimum delays of the logic gates between them. The maximum delay constraint limits the number of consecutive gates on the critical path of a high-speed circuit. In this section, the results are proving that the propagation probabilities of SEU faults are dropping according to the changed delay of the signal path. These results are explaining in Fig. 6 and Fig. 7. In Fig. 6 a term called Polarization Window (PW) is introduced in red color. This is because the time width of the PW completely masks the SEU faults that have been generated inside the window. From 5, it is clear that induced-SEU fault at source flip-flop (Source-FF) reaches the target flip-flop (Target-FF) after a path delay $t_{D_{set}}$ between them. So that, a fault SEU_1 at source-FF between T_0 and T_1 as provided in Fig. 6 not overlaps the latching window (SETUP+HOLD time) when it reaches the target-FF, and masks the SEU_1 fault propagation. But the fault SEU_2 is propagated and latched to the target flip-flop because it is stable during the SETUP and HOLD time of target-FF. After 1 year, the PW is prolonged to $T_0 - T_2$ due to NBTI effect and clearly masks the fault SEU_2 as demonstrated in Fig. 6. Similarly, after 10 years, the faults SEU_1 and SEU_2 are masked and the fault SEU_3 is still propagating to target-FF. These conclusions are statistically derived from the fault-injection campaign of 1582 SEU faults at the path of longest delay as given in Fig. 7, where the upper-row justifies that SEU_1 is masked without aging, and the lower-row justifies that SEU_1 and SEU_2 are masked after 10 years.

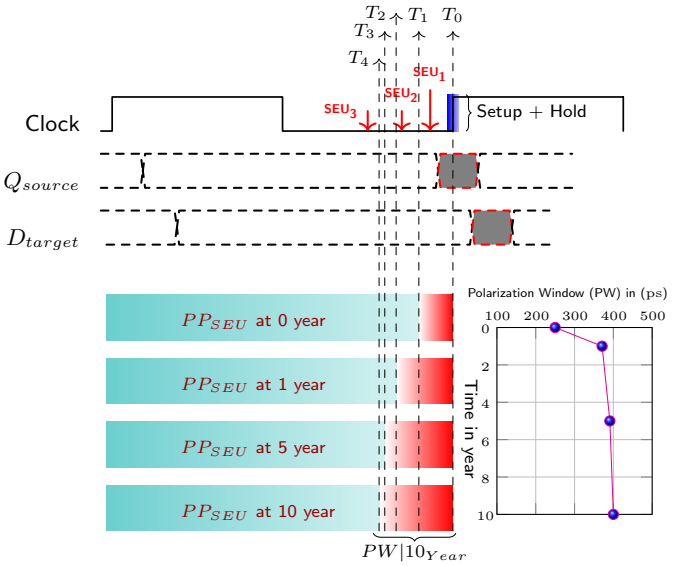

Fig. 6. SEU-Faults' Polarization Window (PW) Elongation

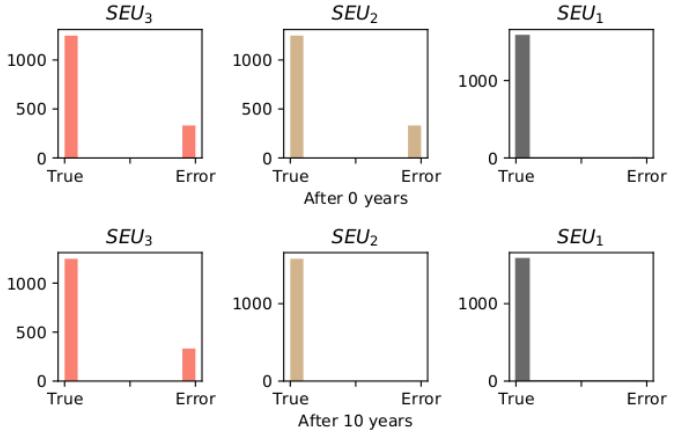

Fig. 7. SEU-Fault Injection Result (After 0-10 years)

C. Impact of aging in SEU caused circuit-functional failures

In Fig. 6, the Propagation Probability (PP_{SEU}) indicates the chances of generated SEUs to propagate through the downstream circuit within an arbitrary clock period T_{clk} and is modeled as an uniform distribution as specified in (6).

$$PP_{SEU} = \begin{cases} \frac{1}{T_{clk}}(T_{clk} - PW|_{\tau_{d_0}}) & \forall \text{ Non-aged } \tau_{d_0} \\ \frac{1}{T_{clk}}(T_{clk} - PW|_{\tau_{d_i}}) & \forall \text{ Aged } \tau_{d_i} \end{cases} \quad (6)$$

The effect of elongated polarization window PW due to aged delays τ_{d_i} in (6) models the increased masking of SEU faults and confirms it through an exhaustive Fault-Injection (FI) campaign as shown in Fig. 8. Color C-2 represents a FI campaign of 74000 injected faults at 188 flip-flops (FFs) of the non-aged circuit, which produce a total of 1181 functional failures as in (4). The 188 FFs are explained as high failure vulnerability FF-instances out of 720 FFs. A 10 year aged model of the same circuit is simulated with an increased FI rate by 50% (color C-1 in Fig. 8). This increment is performed based on the previous studies that the rate of SEU generation increases due to decreased critical charges Q_{crit} while aging.

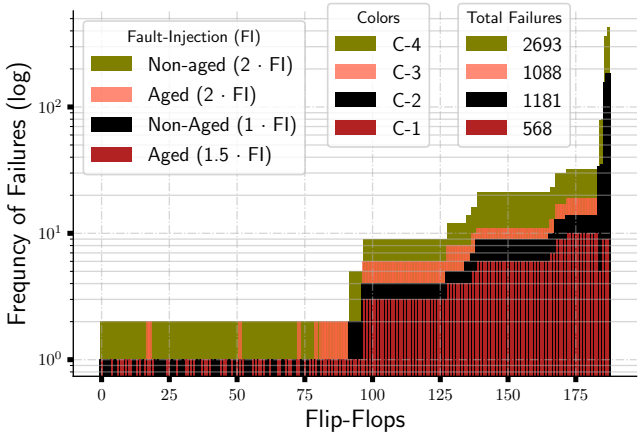

Fig. 8. Functional Failures (4) of SEU-Fault Injection

Even though the FI rate is boosted by 50% for the aged circuit, the number of detected functional failures per flip-flop and the cumulative failures (568), are comparatively less contrary to the case in color C-2 in Fig. 8, which shows high-level masking of SEU faults. As an extension of the analysis, a FI campaign consists of 148000 faults (almost double in number) is performed at the 10-year aged circuit. So that a total of 1088 failures are observed (color C-3 in Fig. 8) and that plot contrasts with a reference bar-graph of FI of 148000 faults at the non-aged circuit (color C-4). FI in C-3 leads to more failures per FF compared to the case in C-2, but still, the overall failures in color C-3 are fewer. This proved that aging causes a masking effect in SEU fault propagation.

D. Aging impact on SET fault propagation

As the circuit ages, considerable propagation-probability deteriorations for SEU faults have been notified. Nevertheless, SETs are not attenuated when traversing the critical paths in response to elongation of the polarization window in Fig. 6. The time-slot at which the generated SETs are latching to target-FF (Fig. 5) is shifting advance in time due to the delay changes in the traversal path of SET. These observations are delineated in Fig. 9, where the propagation delay $t_{D_{set}}$ of SET_1 at gate PG in Fig. 5 varies from 248 ps to 398 ps, which causes a shift in the time slot of propagating SET from T_1 to T_4. The observations are simulated by a SET fault of 20ps in width. Below the timing diagram in Fig. 9, the results of 100 SET fault injections over a second-half cycle of an arbitrary fault-latching clock are provided.

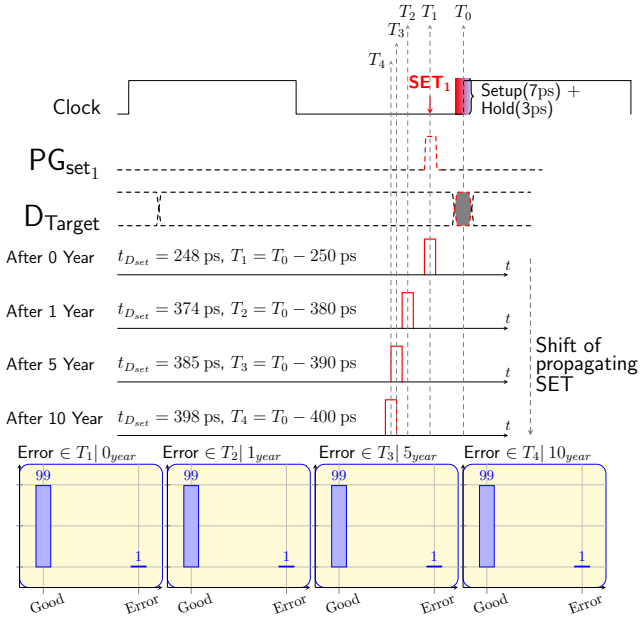

Fig. 9. Shift in Propagating Spot of 20ps-SET

E. Modeling of aging impact on SET fault propagation

The shift in time-spots of propagating SET as provided in Fig. 9, is modeled by the signal processing method. The SET

pulse is assigned by a digital pulse model of width 'w' in gate-level, which possess same electrical boundary properties of a transient pulse at transistor-level. Similarly, the SETUP and HOLD time-periods of a target-FF in Fig. 5, are modeled as a single digital pulse $S_{SH}(t-T_0)$ of width equal to the sum of SETUP and HOLD, and the amplitude is normalized by $1/w$. The delayed impulse function $\delta(t-t_{D_{set}})$ in step-1 of Fig. 10 convolves with induced SETs (G_{set_1} and G_{set_2}), and produces delayed SETs $G_{set_1}(t-(T_1+t_{D_{set}}))andG_{set_2}(t-(T_2+t_{D_{set}}))$ that are analogous to propagated SET pulses through a path delay $t_{D_{set}}$ and reach target-FF as in a real-time scenario of Fig. 5. The convolution and generation of delayed SETs is represented by step-1 and step-2 in Fig. 10. Similarly, step-4 indicates a valid-convolution ($\circledast_v$) [19] between $S_{SH}(t-T_0)$ in step-3 and propagated SETs in step-2, where convolution product is only given for points at which the signals overlap completely. The valid-convolution results in the generation of two impulse functions $\delta(t-(T_2+t_{D_{set}}))$ in blue and $\delta(t-T_0)$in black with amplitudes $A(\delta)$=0 and $A(\delta)$=1 respectively, where $A(\delta)$=1 represents the non-masked fault as given in (7). The case of $A(\delta)<1$ represents the masked fault and various cases of step-4 are presented in Fig. 10.

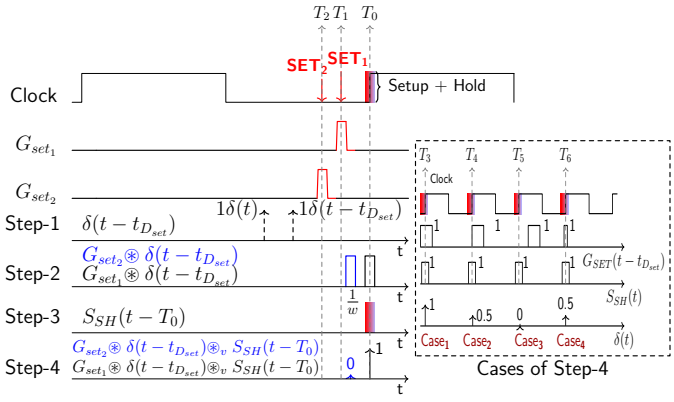

Fig. 10. SET Propagating Model

$$\underbrace{G_{set}(t)\circledast\delta(t-t_{D_{set}})\circledast_v\frac{1}{w}S_{SH}(t)}_{FPP_{i,set}}=\delta(t)*\begin{cases}A(\delta)=1\\0<A(\delta)<1\end{cases}\tag{7}$$

where, $FPP_{i,set}$ is the Fault Propagating Probability of SET pulse at the i^{th} gate. So that, the complex equation (5) can be simplified as:

$$FFR_{i,set}=FIT\cdot FPP_i\cdot LDR_i\cdot FDR_i\tag{8}$$

$FPP_{i,set}$ generate a model which characterize TDR_i and EDR_i in (5). For the case of aging, the path delay $t_{D_{set}}$ in (7) models NBTI caused time-slot shift of propagating SETs and $\frac{1}{w}$ factor in (7) models the width of propagating SETs.

V. Conclusion

Based on the observed results of this research, it has been concluded that voltage variability due to aging shows significant masking property on SEU fault propagation and reduces the effect of increased soft-error susceptibility while aging. Furthermore, this work explicitly reveals that aging shifts the SETs' propagating spots within the clock period. Besides, the latching probability of a SET fault to a downstream flip-flop is successfully modeled by a signal-processing method. The revised AI models and SDF-based aged technology data from this work are considering in the future to emulate aging-aware timing models at the system's RTL abstraction, which enables an early aging analysis in the design process.

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