Delft University of Technology

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Master of Science Thesis

GaN Enabled OLED Driver for Automotive Lighting Application

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February, 2015

To my parents and sister...

Abstract

The impressive features, both in a design and technical aspect, of the Organic LED (OLED) lighting technology have attracted the interest of the research and commercial world and have recently be in the spotlight of the automotive industries, like the Lighting Department of Audi. Some of the most exciting features of these lights are the flexibility, transparency and the very small thickness. It is reasonable, therefore, that in order to take full advantage of this new technology the electronics that drive these lights, that is the dc/dc converter, should also be characterised of low profile, flexibility and small size. A boost towards the direction of the converter minimization and high power density operation could be the recently commercialised power switching technology of Gallium Nitride (GaN) devices. This technology, which exploits the advantages of the wide band gap semiconductors, offers high frequency, high power density, low switching losses operation and low profile design, as well. As every newly commercialised technology, the areas of application that at most exploit the advantages of these switches are still to be found, but it is expected that applications that require high power density or low profile features, like the OLED applications, could benefit the most from the GaN technology.

This area is the exact topic of the current master thesis. At this project a dc/dc converter based on GaN switching devices is designed and built. The converter is purposed for the driving of Organic LED lights that belong to the tail light system of a vehicle. As such, the electrical, mechanical and thermal specifications of the converter are based on the guidelines of the Lighting Department of the Audi automotive industry and the nature of the Organic LED lighting. At this thesis, the required dc/dc converter is designed, built, measured and assessed for its adequacy to the defined requirements. During the design part of this project the necessary simulations are conducted. For the purpose of estimating the losses of the GaN device a detailed analytical model for the switching transients is used. Also, both the possibilities of using a planar and a discrete coil are investigated during the simulations and the two components, which were built in the lab, are compared experimentally. A final prototype of the converter is also built in the lab and the experimental and simulated results are then compared and assessed. The assessment of the results showed that the features of the GaN device can be fully exploited at this application and can offer the low profile and high power density requirements. In order, however, to achieve the minimization of the magnetic component more advanced and wider range of core materials are required, especially if a planar coil is desired. Finally, full exploitation of the detailed analytical GaN loss model requires specialised software tools or accurate analytical models in order to determine the values of the various parasitics and the thermal resistance of the component, both strongly related to the PCB layout. This, also, means that during the design procedure in order to achieve better accuracy -which is required at applications which push the frequency to the limits - the PCB design layout parameters should be included in the iterative process of the parameter specification.

Aknowledgments

First of all, I would very much like to thank Dr. Jelena Popovic for her invaluable help, consistent guidance and thought provoking discussions. Our excellent communication all this time helped me significantly. I would also like to thank Ing. Mark Gerber because his advice, experience and clear way of thinking during my internship proved to be very helpful during this project. A great thanks, also, goes to the Phd students Milos Acanski, Ilija Pecelj and Wenbo Wang whose help during the practical part of my project was extremely important.

Thanks,finally, to my colleagues and fellow master students - Udai, Ralino, Nikolas, Joost, Einar, Andreas, Vasilis, Sotiris, Didier, JK - for the great time that we had all this and the past year.

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Chapter 1

Introduction

1.1 Problem Statement

The Organic LED lighting technology has recently attracted significant attention for its research interest but mainly for its commercial opportunities as it offers thin, flexible, shapeable, transparency features for light applications, allowing for new impressive and futuristic designs for various areas including automotive applications. The Audi automotive industry more specifically has shown special interest in this new technology and it tries to exploit its features for the lighting of its products, a very strong sector for this specific brand. Apart from the various bottlenecks of this still young technology mainly related to temperature and lifetime issues, an aspect that requires special attention is the driver of the OLED components. In order to fully exploit the geometry-related advantages that this technology offers it is very important for the dc/dc converter that drives the lights to be low profile and flexible.

A recently commercialized and innovative power switching technology, the GaN switches, could be a boost towards the direction of the minimization of the converter's size. The new switching components exploit the advantages of the wide band gap semiconductors and they promise high frequency, high power density and high efficiency operation of the switching converters. The utilization of these switches is generally expected to push forward the capabilities of the power electronics applications, especially as regards the reduction of the size, but in order to do so the design and built approaches, used for Si-based converters up till now, need to be carefully reconsidered. Similar to any new commercialized technology, it is a very important aspect to locate the areas of application that this technology could be more useful and the advantages that could be the most exploited. In general, GaN based switches are expected to help significantly at areas where high power density or low profile features are crucial parameters, such as the aerospace industry, the lighting technology and so on.

It seems, therefore, that the requirements of the OLED technology for low profile, small and flexible power converters could be possibly fulfilled to a great extend with the appropriate exploitation of the advantages that the GaN technology offers. Considering the fact that in power supplies the passive components are the main bottlenecks as regards the size minimization of the converter, the possibility of high frequency operation and low losses that GaN switches allow, along with the availability of the appropriate

inductor core materials, could help towards that direction.

This thesis project focuses exactly on this aspect as its purpose is to built an OLED driver for automotive lighting using the advantages of GaN switches.

1.2 Thesis Objectives

As already stated, the main objective of this thesis project is to exploit the advantageous features of the GaN switching devices and build a low-profile OLED driver purposed for automotive applications. The project is carried out in collaboration with the Audi Lighting Department and the basic electrical and mechanical specifications for the driver are imposed by the technical standards of the company and will be presented in detail at Chapter 3, where the design procedure is described.

At Figure 1.1 a general schematic of the desired configuration is presented:

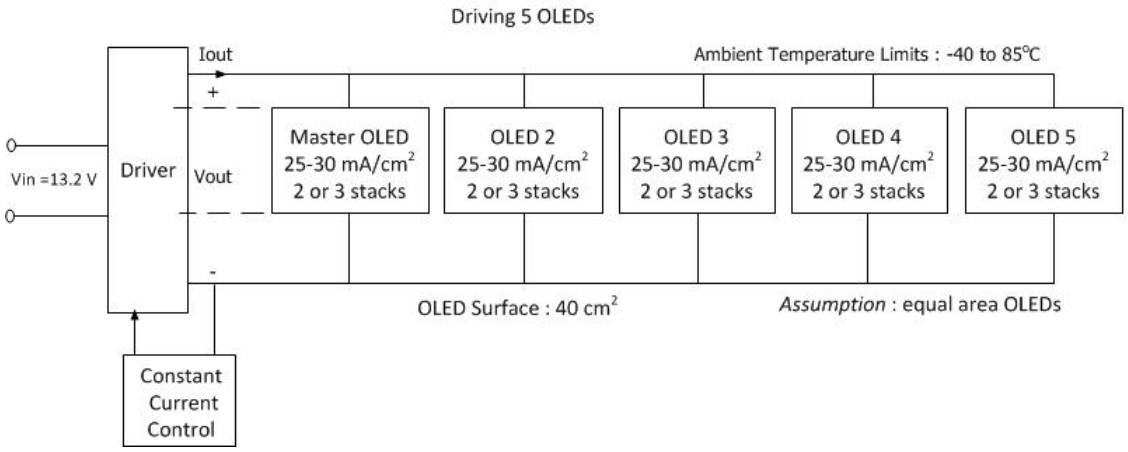


Figure 1.1: General scehmatic of the configuration.

There are two limitations regarding the design: the size, and especially the thickness of the converter (related to frequency) and the maximum component operating temperatures (related to frequency and ambient temperature - the range of which is shown at the previous figure). Due to these limitations the following aspects are also investigated during this project:

- The possibility of using a planar inductor, as compared to a discrete one, for enhancing the low profile feature of the converter.

- The maximum operating frequency that will allow operation into the temperature limits of the converter.

Added to these, an analytical model of the losses of the GaN switch is required to be developed.

1.3 Thesis Layout

The report of this thesis is structured in the same way as the project was conducted during time. Initially, a literature review on the main aspects of the topic took place. Later on, the design process was conducted and, finally, the converter was built and the experimental results were taken and evaluated. Here, a short description of the content of the chapters is presented.

At chapter 2 the appropriate theoretical background regarding the two main aspects of this thesis is developed. At the first part of this chapter the basic concepts of the

organic LED technology are developed along with the electrical and mechanical properties and the advantages and disadvantages of this new technology. At the second part, a thorough review of the GaN technology is presented. Initially, their physical structure and concept is briefly presented and then their basic inherent characteristics are discussed. The influence of parasitics, some thermal issues and a review on their application in the power electronics area follows at the end.

At Chapter 3 the most important parts of the design procedure are presented and discussed. Main axis of this chapter is the construction of an analytical model for simulation purposes. Initially, the reasons for selecting the appropriate topology (buck-boost) are explained and then the boundary conduction operating mode with valley switching is discussed and the corresponding analytical equations are given. Special emphasis is given on the analytical model of the GaN switch losses that is used for the simulation. After that, the design of the magnetic component and the selection of the inductance value is discussed. Note that the value of the inductance defines the operating frequency of the converter and, therefore, is an important parameter. Finally, some other considerations regarding the design procedure are briefly addressed.

Chapter 4 contains the experimental results of the project. Initially, the converter prototype and the experimental setup is presented along with some output waveforms and thermal images. After that, a more accurate calculation of the GaN junction-to-ambient thermal resistance is described. Finally, the experimental results are presented and are compared with simulation results.

Finally, at Chapter 5 an assessment and an evaluation of the final proposed converter is attempted and some conclusions are extracted.

Chapter 2

State of the art

At the previous chapter the problem outline and the project goals and objectives of the current master thesis were presented. It became clear that two recently commercialized components, the organic LED lights and the GaN switches, are the focal points of this project but with the former being treated exclusively from the perspective of an electric load, which means that only the electrical characteristics (and the geometrical which affect the electrical in that case) are of interest, and the latter being, eventually, a very important and fundamental component of the design, as regards its behaviour and contribution.

Because of the importance of these two elements at this project, it is considered necessary to present the theory behind both of them at this chapter. Initially, the OLED technology, physics and some design aspects are presented. Since the OLED device is treated at this project solely as an electric load, similar to a common LED but with its specific electrical properties (and mechanical properties, because they define the electrical ones), the theoretical background for it is not as detailed as the one for the GaN device, which follows and includes thorough descriptions for its physics, electrical characteristics, design aspects and applications.

2.1 The Organic LED Lighting

Electroluminescence in organic materials is known already from the 1950's, however it is mainly the last twenty years that the organic light emitting technology has attracted much of the attention of the lighting research and industry. Because of the various advantages of this technology, which will be presented later at this paragraph, OLED lighting is expected to lead a paradigm shift in the lighting industry. Up to now, OLED technology is mainly used for displays and monitors. Since the early 2000's OLEDs are used in small-screen devices such as cell phones or digital cameras while the last few years large OLED TV screens have been released to the market. However,the spreading of these devices at large area light emitting elements for general application is slower and up to now there is a lack of availability of a broad array of off-the-self products.

At this paragraph, the basics of the organic electroluminescence and the organic devices are initially presented. The main advantages and bottlenecks of this technology follow and, finally, the design aspects of the OLED devices, such as thermal and driving considerations and their electrical characteristics, are demonstrated.

2.1.1 Organic Semiconductors

Organic LEDs are solid state electroluminescence (EL) devices, that is devices which generate light from condensed matter by electrical excitation, based on organic molecular solids. The organic molecules are electrically conductive and are referred to as organic semiconductors, though due to their low electric mobilities (10^{-3} to $10^{-7} cm^2/Vs$ at room temperature), which are highly dependent on temperature and the applied electric field, and their negligible intrinsic concentration of thermally generated free carriers can be considered more as insulators [1], [2], [3]. Although there are differences between the organic semiconductors with the inorganic ones, originating from the different mechanisms that dominate at the various processes, many concepts derived from inorganic semiconductor physics are also used at OLED technology (i.e. voltage drop at p-n junction for inorganic LEDs, built-in voltage for OLEDs).

2.1.2 The Structure of an Organic LED Device

A basic structure of an organic LED device includes an organic material, the emissive layer, at which the recombination of the charge carriers takes place followed by the emission of light. The color of the light depends on the properties of the organic material. Two classes of organic materials are commonly used in organic light devices: polymeric substances and small molecule materials [4]. The charge carriers are injected from the two electrodes, anode for holes and cathode for electrons, that sandwich the emissive layer and at least one of them is transparent. It is quite common for the anode to use Indium Tin Oxide (ITO), a transparent conducting oxide (TCO), and for the cathode aluminum [5]. Between the anode and the emissive layer a hole transport layer (HTL) is usually deposited. Correspondingly, an electron transport layer (ETL) is placed between the cathode and the emissive layer but sometimes the ETL and the emissive layer are the same material (i.e. Alq3). The substrate can be rigid (glass or metal) or flexible using a polymer plastic. Since the color of the emitted light is a material property the total emission and the color temperature can be tuned by stacking different emission layers. For white light red, green and blue emissive layers are used. In figure 2.1 a cross section of an OLED stack is presented [5].

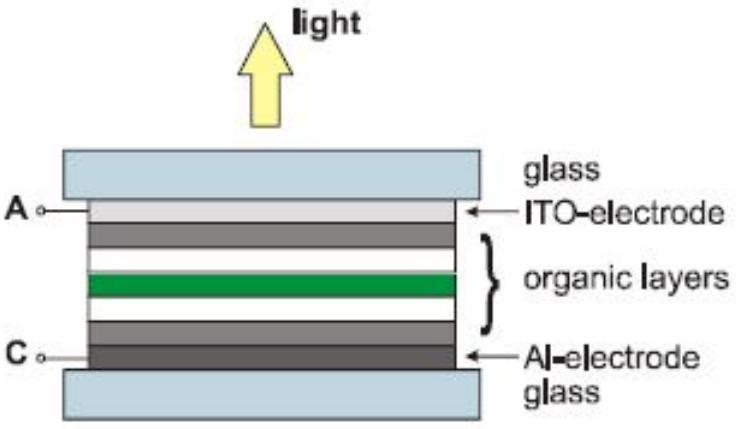


Figure 2.1: Structure of an OLED device [5].

2.1.3 Advantages and Disadvantages of an Organic LED

OLED lighting is a very promising technology with many advantages over the inorganic LEDs, allowing a large area of applications ranging from display monitors (e.g cell phones) and visible light communications (VLC) to automotive and general lighting applications. OLED devices can be made thin, flat and light weighted as well as bendable, flexible and transparent because they can be formed on any substrate such as glass, metal, thin plastic sheets etc. [1]. They also offer significant degree of freedom as regards the color of the light and the shape of the device. At [6] a comparison between LCD, PLASMA and OLED displays showed significant lower power consumption for the latter technology concurrently with wide viewing angle (same for all displays), high brightness and very good contrast. However, the lifetime was by far the smallest (10000 hrs). According to OSRAM [4] large area fabrication of OLEDs can be cost-effective, since there is a possibility of using simple screen printing or wet depositions techniques. The cheap production combined with the high efficiencies that can be achieved [6] make the OLED technology really competitive. The main disadvantage of OLEDs concerns their sensitivity to high temperatures. For an OLED a normal operating temperature is -20^oC to 40^oC (when for LED the junction operating temperature can be larger than 100^oC). For higher temperatures a significant drop of the efficiency and the lifetime is realized. According to OSRAM [7], as a rule of thumb it can be said that for a temperature increase of 20K a 50% reduction of lifetime is possible. This is, actually, the main obstacle for its direct application in the demanding automotive industry, an obstacle that is expected to be surpassed in the near future.

2.1.4 Large Area Organic LEDs

For many applications, like general lighting or visual light communications, the area of the OLED devices needs to be quite large to achieve sufficient luminous flux. Enlarging the area of the OLEDs, though, should be done in great care and consideration should be taken regarding short circuit, non uniform light emission, hot spots, efficiency reduction and heat generation. Extensive study for these aspects has been conducted at [1] and various solutions have been proposed. For example, the uniformity of light emission can be enhanced by enlarging the contact area of the device so that current is injected into the panel from every direction or by changing the material of the electrode or implementing metal grids [8]. The area of the OLED has significant role at the charge and discharge dynamics. The larger the area the slower are these dynamics. This originates most likely from the increase of the significant parasitic capacitance of the OLED devices.

In [2] the dynamic response of large area OLED devices is studied thoroughly. According to this reference, the modulation speed of OLED devices is limited because the organic materials have low carrier mobilities. Another interesting conclusion is that the discharge dynamics of large-area OLEDs are slower compared to the charge dynamics. This is due to the space charges remaining inside the device in the off state. Upon turn off the accumulated charges inside the device are discharged, yet it takes long time since holes at ETL are discharged much dully (due to very low hole mobility inside the ETL).

The electroluminescence (EL) delay time (EL response speed) is the time that is required until the injected holes and electrons meet inside the device, recombine and emit light. This time:

- Decreases when increasing the pulsed bias voltage. That is because higher bias voltage means higher electric field and, thus, higher electron mobility.
- Decreases when decreasing the device length (thickness) despite the fact that the capacitance increases. The effect on reducing the device length on the EL response

speed is higher than that of the increased capacitance. However, it should be noted that a decrease of the length (L) can lead to short circuit problems, luminous inhomogeneity (electrode resistance higher than perpendicular resistance) and short lifetime. In general, device length is a key design parameter for an organic LED device.

2.1.5 Design Aspects of Organic LED devices

Thermal Considerations

It has already been mentioned that OLED devices are sensitive to high temperatures. The dynamic behavior of the OLEDs in response to temperature changes has been meticulously examined at [9]. According to this, when temperature increases the charge carrier mobility increases, due to an increase of the thermally activated hopping speed, which results to a decrease of turn-on voltage, an increase of current density and luminance and an increase of the electroluminescence (EL) response during turn on and turn off (see figure 2.2 [9]). However, the rise of temperature leads to a decrease of the efficiency in both ways. First, the increase of the current density leads to an increase of the Joule losses at the electrodes which are generally significant due to their low conductivity (transparent conducting oxides have generally low conductivity). Second, the current balance, which is the ratio of the recombined current and the device current and approaches unity (depending on the bias voltage) in steady state , is closer to unity at lower temperatures than at higher. This means that less part of the device current contributes to the recombination process resulting to a decrease of the internal quantum efficiency.

Although the OLED devices are sensitive to temperature changes and have a quite restricted temperature range of operation their thermal management can be proved to be quite easy. In many situations heat sinks are not necessary because OLEDs are cooled passively by heat convection and radiation from both surfaces. The heat dissipation is also facilitated by the very small thickness of the devices (short heat transfer pathway). According to OSRAM [7], an OLED device heats between 5K to 15K above ambient temperature at typical operating conditions. Of course, in case the operating temperature exceeds the maximum operating limit of temperature (in case for example of high ambient temperature) then heat sink should be used. Also, because OLEDs are surface light emitting devices a certain luminous flux can be achieved by increasing the emitting area and, this way, operating at lower luminous intensity and, thus, generating less and convecting more heat. However, this is not always the case because by enlarging the area of the OLED device the electrode resistance increases. This leads to a decrease of the efficiency (increase of Joule losses) and also to a non-uniform distribution of current and thus luminance and heat dissipation. So, for small area OLEDs (i.e. $36cm^2$ [1])heat sinks are not needed whereas for general light application (high luminous intensity and flux) heat sink is needed for stable operation and long lifetime.

Electrical Characteristics

The current-voltage characteristic of OLED devices is very similar to the LEDs (and, thus, to that of a diode), as it is obvious from figure 2.2(a), which gives great comfort to handle them since there is already experience from LED technology. At the same figure, the temperature dependency of the characteristic is obvious. At [5] is stated and experimentally proved that the relation between luminance and current is quasi-linear, which is not the case for the voltage. This makes these devices suitable for current control.

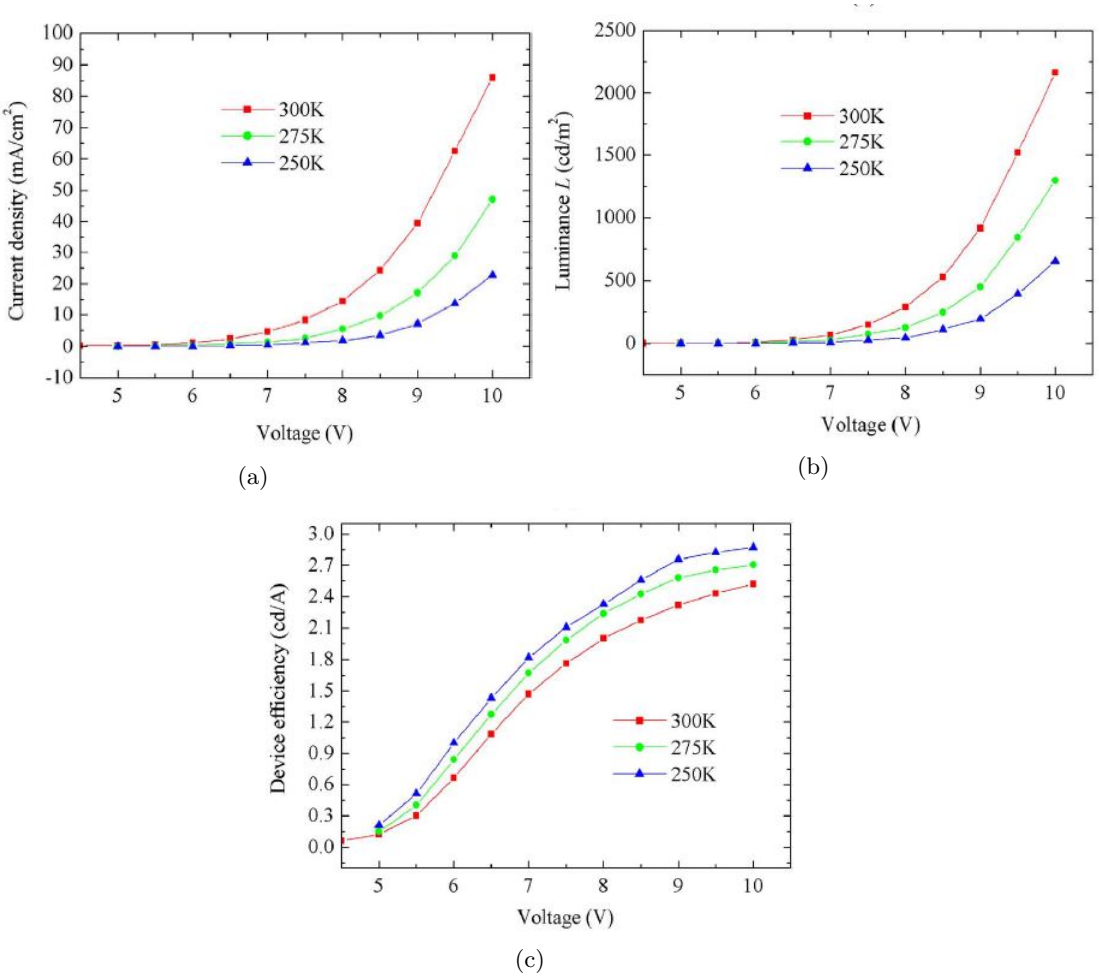


Figure 2.2: Influence of temperature on OLED characteristics [9]

As it is already mentioned, OLEDs exhibit considerable internal parasitic capacitance due to its large surface area and small thickness. At [5] a typical value of 200-400 pF/mm^2 is given. This parasitic capacitance causes a delay at the voltage decay (which can lead to internal flowing current) and can also cause current spike if a step voltage is applied. The internal capacitance is voltage dependent as it is thoroughly explained at [3]. At [10] the relation of the OLED equivalent capacitance and the bias voltage is extracted. The parasitic capacitance, however, can be used as the output filter of the converter or part of it as it is suggested at [5].

Equivalent circuits for OLEDs have been proposed at [5] and [10] and are similar to equivalent circuits of non-ideal diodes. A simple equivalent that stems from the proposed models is shown at figure 2.3.

R_{ITO} is the electrode resistance and R_p the leakage resistance. C is the parasitic capacitance the value of which can be assumed to be constant leading, though, to inaccuracies when simulating the dynamic behaviour of the OLED. V_{th} is the built-in voltage or threshold voltage of the OLED which is temperature dependent. Finally, the diode corresponds to the I-V characteristic after subtracting the linear component $(I \cdot R_{ito} + V_{th})$.

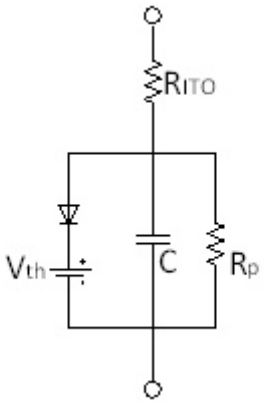


Figure 2.3: Electrical equivalent circuit of an OLED device.

Driving Aspects

The driving of the OLED devices is similar to the driving of the LEDs. For that current control is applied due to the linear relation between current and luminance. Operation above the linear region (Lm-I) results in output power converted to heat which burdens also the driver. When dimming is not necessary Constant Current Mode can be used which usually requires overvoltage protection. Generally, OLEDs exhibit slow dynamic response due to their capacitor-like behaviours. Of course this depends on the panel size. The delay time can be reduced when OLEDs operate under high pulsed voltage which increases the EL response(increase of electron mobility) as it has been already discussed. Finally, it is suggested that parallel connection should be avoided since it may result in different luminance values or even cause damage at the devices. Series connection is preferred when simultaneous light up is needed.

2.2 The Gallium Nitride Power Switches

The past few decades electrical power conversion realized a rapid and wide spread thanks to the development of the semiconductor technology based on Si, a technology which the last decade entered its maturity providing low cost and reliable switching devices to all power electronics applications. In the same time, though, Si has reached its material limits meaning that very few improvements on the existent Si-based technology are to be expected. This slow down of the semiconductor technology development could have a proportional impact at the field of power electronics since semiconductor devices are key-elements at this area of engineering. More specifically, semiconductor switches at power electronic converters are the main source of power losses and their specifications determine the maximum operating frequency and power and as a result the size, the weight and various other aspects of the design, the layout and the thermal management.

A new boost to the semiconductor power switching technology, and thus to electrical power conversion, is expected by the development and commercial application of the wide band-gap semiconductors with the GaN (III-Nitride* compound) switches being a very promising candidate for high-frequency, high power density and high efficiency operation in switching converters. The utilization of these switches is expected to push forward the capabilities of the power electronics topologies, but in order to exploit the full potential of these devices the design and the built approaches, used for Si-based converters, need to be revisited, as it is proposed at [11].

*III-Nitride = compounds of nitride with chemical elements from the boron group (Boron, Aluminum, Gallium, Indium, Thalium, Ununtrium)

2.2.1 Wide Bandgap Semiconductors

A semiconductor is characterized as wide bandgap when the band gap energy (the energy required for an electron to jump from the top of the valence band to the bottom of the conduction band) is significantly larger than 1 eV - typically, larger than Si bandgap (1.1eV) or GaAs (1.4eV). The wide band gap gives the materials the special properties suitable for high-frequency and high-power applications. GaN and SiC are both wide band gap semiconductors.

A comparison between the properties of Si, SiC and GaN are presented at Table 1. The different values at these properties define the differences at the operating capabilities of its compound.

$MaterialProperty$	Si	SiC	GaN
Bandgap (eV)	1.1	3.2	3.4
Critical Field ($10^6 V/cm$)	0.3	3	3.5
Electron Mobility(cm^{-2}/Vs)	1450	900	2000
Electron Saturation Velocity ($10^6 cm/s$)	10	22	25
Thermal Conductivity (W/cm^2K)	1.5	5	1.3

Table 1 :Comparison between material properties of Si, SiC and GaN.

The high critical field of GaN and SiC allows these devices to operate at higher voltages and lower leakage currents compared to Si devices. Electron mobility and electron saturation velocity determine the on resistance and the maximum operating frequency. It is obvious that for GaN both sizes are higher compared to other two allowing high switching frequencies and low conduction losses. High thermal conductivity means that the material is superior in conducting heat efficiently. SiC has higher thermal conductivity than GaN and Si which means that it can operate at higher power densities than the other two.

2.2.2 Structure of the GaN HEMT Devices

Similarly to MOSFET switches, the operation of the GaN switching devices is based on the creation of a channel of electrons which constitutes a conductive path between the drain and the source and can be controlled by the gate to source voltage. However, the mechanism that creates this conductive path in GaN HEMTs (High Electron Mobility transistors) is different to the MOSFET. For the case of GaN devices an electron channel, called 2DEG (= two dimensional electron gas), quantum-mechanically confined in two dimensions, is developed at the heterojunction of two specific semiconducting materials i.e AlGaN/GaN, chosen appropriately so as to create the, necessary for this phenomenon, rectangular quantum well (in which the "sheet" of electrons is trapped. At this heterojunction there is an abundance of electrons, the mobility of which is much higher compared to Si-based Mosfets (see Table 1).

Currently, all the commercialized GaN switches for power applications are heteroepitaxial devices. The reason is that the production process for epi ready GaN substrates of low defect is still at very early stages and, thus, high quality and sufficient size homoepitaxial GaN waffers are not yet available. This is an important disadvantage of GaN HEMTs over SiC Mosfets, for which homoepitaxy is possible (a comparison between Gallium Nitride (GaN) and Silicon Carbide (SiC) devices is found at [3-1-1]),

because at the heteroepitaxial GaN devices the lattice mismatch (17%) and thermal coefficients of expansion mismatch (56%) [12] between the substrate and the GaN layer lead to stress of the materials, especially during power cycling. To deal with the crystallographic differences and to achieve material matching a buffer layer of AlN (Aluminum Nitride) is used. This layer, though, is insulating which means that vertical structure devices are not possible to built with this method but only lateral. Lateral structure, however, is not suitable for high power applications (>50kW) due to the large chip areas that are necessary to achieve high breakdown voltages (bigger distance between the gate and the drain, field plate structures etc.) which are translated to high costs and difficulty of manufacture. The development, performance and status of lateral and vertical GaN devices is discussed at [13].

The most commonly used substrates are Si and SiC. Si substrates are used for their low cost and the large size that can be developed. Actually, thick and crack free GaN film can be successfully grown on large diameter Si substrate leading to a significant reduction of the fabrication cost and thus to the comercialization of the GaN devices.However Si substrates have much lower thermal conductivity than SiC substrates. As a result, the latter have higher power handling capabilities and better thermal management. A state-of-the-art review of GaN-on-SiC HFETs is found at [14].

There are two main categories of lateral structure GaN switches: the depletion mode (d-mode) and the enhancement mode (e-mode). The depletion mode HFETs are normally-on switches which need a negative gate voltage to be applied in order to turn them off. On the contrary e-mode HFETs are normally-off switches and as a result they need a positive voltage to turn them on. Their difference lies on the fact that at the e-mode structure the gate electrode is placed properly on top of the AlGaN layer so that it forms a depletion region (no 2DEG) underneath it. The requirement of negative voltage in order to turn off (the driver needs to provide negative voltage at the initialization of the device in order to avoid a short circuit) is a major disadvantage of the d-mode devices. However, they have a much larger safe operation margin compared to e-mode devices. The e-mode GaN achieves optimum performance for a gate voltage around 5V when the maximum allowable value is 6V, which means that they require a very careful driving and design so as to avoid voltage overshoots at the very sensitive gate. Another type of normally-off GaN devices is the so-called Gate Injection Transistors (GITs) which can succeed increase of the drain current with low on-resistance by injecting holes from the p-type AlGaN gate and using conductivity modulation. This GaN device is presented extensively at [15].

At the following figure (Figure 2.4) [16] the structure of an AlGaN/GaN HEMT on Si substrate is presented. It should be noted that a commonly used dielectric material (cyan) is the SiN.

2.2.3 Inherent Characteristics of GaN Devices

On resistance

GaN devices exhibit much less on-resistance compared to their counterpart Mosfet devices, which is a major advantage for the first since it results to less conduction losses (see Figure 2.5 [17]). However, the Rdson-Vgs curves are similar for the two technologies. It should be noted that the value of the on resistance is not constant but it depends on the applied gate voltage and device temperature.

At high voltage applications, though, GaN switches suffer from current collapse phenomena due to the electron trapping at defects in the AlGaN/GaN interface which leads to a severe increase of the dynamic on resistance of the device (on resistance measured immediately after switching the device from off-state to on-state). According

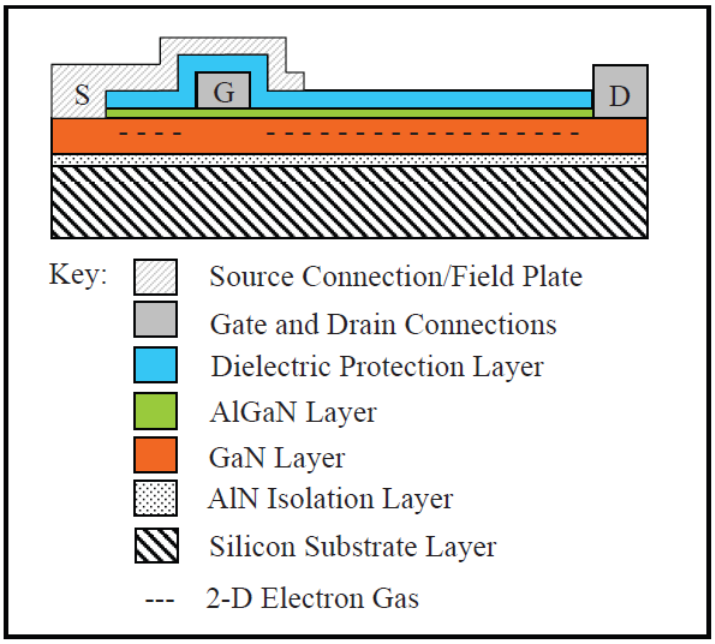


Figure 2.4: Structure of an AlGaN/GaN HEMT on Si substrate [16].

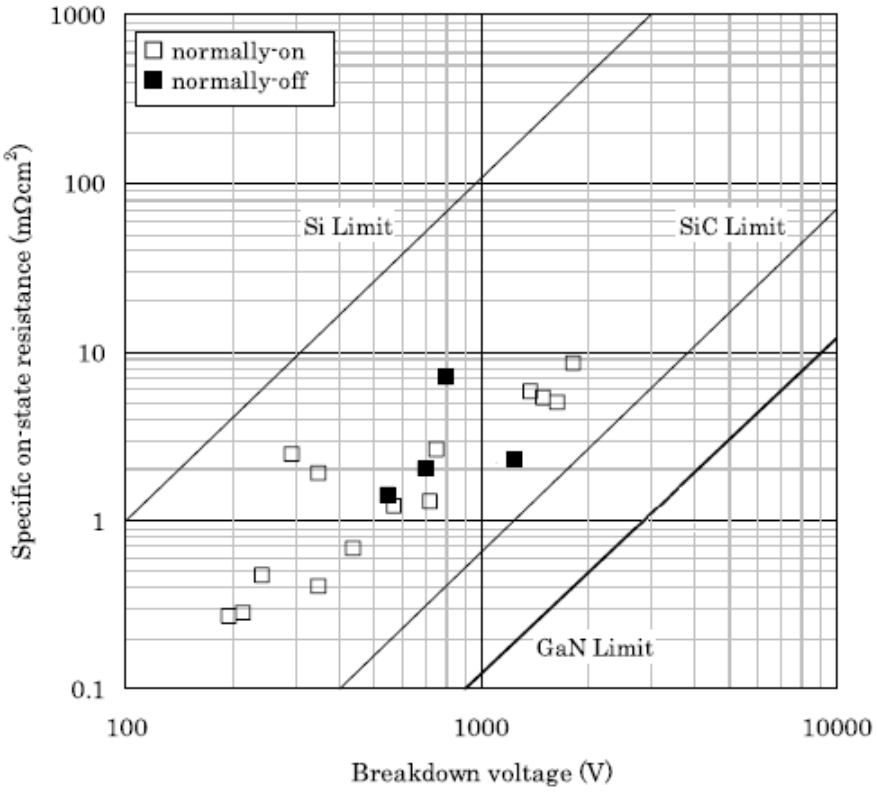


Figure 2.5: On resistance for Si, SiC and GaN devices in relation to breakdown voltage [17].

to [18] the on resistance modulation strongly depends on the electric field distribution and for that reason field plates are implemented on the device structure, either at the source electrode (single FP) or both at source and gate electrodes (dual-FP).This study showed that dual-FP structure is much more effective for suppressing the current collapse than single-FP, as it results to a better electric field distribution. At [19] a 1.2kV GaN-on-Si transistor is fabricated with two field plates at source electrode and one at gate electrode where the dynamic on resistance increase is considerably suppressed up to 600V.

Capacitance

The lateral structure GaN devices come with a very important advantage over their Mosfet counterparts: the values of the parasitic capacitances of the device, which are the gate to drain (C_{gd}), gate to source, C_{gs}, and drain to source, C_{ds}, capacitances are significantly smaller to those of the Mosfet devices. For example, a 40V 42A n-channel Mosfet with Rdson 3.9 mOhm from International Rectifiers exhibits an input capacitance $C_{iss} = 3810$ pF at $V_{ds} = 25$V whereas a 40V 33A GaN switch with $R_{dson} = 4$ mOhm from EPC (EPC2815) exhibits C_{iss}=1100 pF at 20V. The difference is even more obvious when comparing the corresponding charges. For example the Mosfet device has Miller charge (gate to drain) 18nC whereas the GaN device 2.2 nC, both at $V_{ds} = 20$V. The gate to source charge, Q_{gs}, for the first switch is 12 nC whereas for the second 3 nC, also at V_{ds}=20V. It should be mentioned that it is mainly the small value of the gate to drain capacitance,C_{gd}, that allows for high speed operation of the device.

At [20] the BSC027N04 Si Mosfet is compared with an EPC2015 eGaN FET, both at a resonant DC/DC converter. The much smaller gate charge under ZVS at 5V for the GaN device (8.3nC compared to 27.5 nC of the Mosfet) resulted to a significantly faster gate drive speed for this device. What is most important, though, at this application is that the smaller output charge of the GaN device (18.5 nC compared to 40nC of the Mosfet, both at 20V)led to a proportionally shorter period for the ZVS transition, increasing, therefore, the effective duty cycle, reducing conduction losses (lower RMS currents) and improving the converter performance. Another similar study [21] showed that the device losses improved by 42% for a 600V LLC resonant converter implemented with cascode GaN HEMTs compared to the same converter implemented with Si Mosfets, due to the lower output capacitances and charges of the former device. This led to an enhancement of the efficiency by approximately 1% for 20A output current. From the previous examples, it is obvious that the important feature of low parasitic capacitances for the GaN devices can, not only reduce switching losses and increase switching times, but enhance the overall performance of a topology, here for resonant converters.

An unwanted phenomenon that is related to the values of the parasitic capacitances is the so called Miller turn on. This might occur during a high speed turn off where the steep rise of the drain to source voltage (Vds) can induce an unwanted turn on of the device. The possibility of such a behaviour is related to the value of the ratio of the Miller charge (Qgd) and the gate to source charge (Qgs). A device is expected to be immune when the value of this ratio, called Miller ratio, is smaller than 1. 40V devices are inherently immune to unwanted turn on because the Miller ratio is smaller than 1 when Vgs=0. For higher voltages this is not always the case, see for example the Miller ratio for the EPC2010 device of 200V. However, according to Microsemi [16], all future generations of eGaN FETs are expected to have Miller ratios below 1 for Vgs=0.

Body Diode

Mosfet transistors incorporate an anti-parallel parasitic diode which is formed by the p (body) layer and the n+ (drain) layer of the device and is utilized at many power electronics applications, for example as a free-wheeling diode. This, in most cases, results to considerable reverse recovery losses which can seriously deteriorate the overall performance of the set up.

Although at the GaN device structure there is no p-n junction and, thus, no p-n parasitic diode, diode-like operation of the device is possible but is based on a different mechanism. When the gate to source voltage difference is zero at an e-mode device there is no 2DEG layer and the device is off. However, a decrease at the drain voltage leads to a positive bias of the gate relative to the drain which will allow the current to flow through the device at the reverse direction (source to drain) resulting in a voltage drop equal to the threshold voltage in series with the voltage drop across the on resistance. The absence of a bipolar junction, and as a result of stored charge carriers, means literally zero reverse recovery losses, a very important feature of GaN devices as it can lead, with proper use, to efficiency enhancement of an application. On the other hand, though, during the conduction of the GaN diode the forward voltage (source to drain voltage) is significantly higher than silicon transistors (e.g for an EPC 2015 the diode starts to conduct for Vsd>2) which means higher conduction losses.

The poor reverse conduction characteristics is an important disadvantage of GaN devices which is prominent at topologies where free-wheeling is necessary.For this reason, at some applications it is necessary to avoid large diode conduction intervals and a proper dead time management is required. At [22] a loss analysis of an active-clamp flyback converter based on GaN is carried out and after that an optimization of the length of the dead time period in order to minimize the reverse conduction losses is achieved. At [23] a three level driving method is proposed to overcome the high reverse conduction loss issue of GaN devices utilized at a synchronous buck converter. For both cases the proposed techniques proved to be necessary and effective for the enhancement of the GaN-based converters' efficiencies.

Gate Voltage

Special attention should be given from designers when driving GaN switches. The reason is that the operating limits of the gate to source voltage are much smaller (-5V to 6V) compared to Mosfet devices (+-20V). Even worse full enhancement of the GaN devices is achieved for gate voltages of 4V and more. Obviously, the safe operating area of GaN devices is very restricted. It is very important that the maximum and minimum limits of the gate voltage are not exceeded otherwise large current with high steepness will be drawn by the gate,leading to device failure. For this reason an optimized layout which limits the parasitic inductances and thus minimizes ringing and other transients is of the utmost importance. Sometimes, a small gate resistance, in series with the output gate driver, might be necessary to dump the unwanted ringing resulting, though, to higher switching times.

Another aspect is that the threshold voltage of GaN devices is much lower (generally conducts for Vgs over 1.6V) than that of Mosfet devices which means that low driver impedance from gate to source should be ensured to avoid unwanted turn on during high speed switching.

2.2.4 Influence of Parasitics

Because of the small switching times, and, thus, the high di/dt and dv/dt events, as well as the high operating frequencies of the GaN devices the various capacitive and inductive parasitics of the package and the circuit layout have serious impact on the operation and efficiency of the switch. Various resonance phenomena (ringing), which can even cause unwanted turn on of the switch, are due to these parasitics but one equally important aspect is the difficulty in calculating accurately the exact switching losses of the device. Packaging and layout parasitic inductances and capacitances influence decisively the switching times and as a result the standard piecewise linear models for switching calculations used at Mosfets prove to be insufficient because they take into consideration the influence of only the input and output capacitances. At [24] the parasitic inductance of the package is extracted and a simulation model is developed, while its influence on the device operation is clearly presented. At [25] analytical loss models which take into consideration the effect of parasitics are proposed.

Of significant importance is the parasitic inductance that exists at the source electrode of the switch where both the currents of the gate loop and the main circuit flow through. This inductance, called common source inductance, delays the turn on and turn off times because during a di/dt event the voltage that is induced across it opposes the gate drive voltage change and as a result the switching times and, thus, switching losses increase. The value of the inductance depends both on the packaging and layout and optimization of these is desirable. However, it should be noted, that although common source inductance increases switching times it, concurrently, decreases the possibility of a Miller turn on which can be considered a positive effect.

2.2.5 Thermal Management Considerations

Using GaN devices at power electronics applications allows for high switching frequency and high power density operation but with the cost of a very challenging thermal management. Especially in applications where active cooling is not an option, which is a common situation in power electronics, thermal management might even lead to a considerable reduction of the power density because of the significant size of the thermal components. At [11] there is a complete overview of the thermal considerations when using GaN devices, the challenges that occur and the approaches that can be followed.

The physical properties, the packaging and the size of GaN devices are factors that impose various restrictions at the thermal design. The thermal conductivity of GaN material is 1.3 W/cm^2K, that is smaller than Si and much smaller than SiC (Table 1). The substrate on which the GaN material is placed (for lateral structure devices) is also an important factor as, for example, SiC or diamond enhance the thermal conductivity of the device compared to a Si substrate. However, the benefit of SiC over Si diminishes as operating temperature increases [26]. Enhancement can be also achieved by reducing the thickness of the substrate [26] or by integrating more dies into one structure. It should be taken into consideration, though, that optimization techniques on the die are cost effective and challenging while their contribution on the final thermal resistance of the device is not as important as the one of the packaging.

The choice of packaging at GaN devices comes with a significant trade off. From a thermal management perspective, packages like TO-220 are very suitable as they have small thermal resistance. However, their long leads are very undesirable for operation at high frequencies (main advantage of GaN devices) due to their significant parasitic inductance. Significant is also the capacitance that occurs from the capacitive coupling with the heat sink. On the other hand, flip chip packages (like LGA − land grid array− or solder bumps) present very low parasitics but with the drawback of challenging thermal

management and assembly. The latter packaging is generally more suitable for GaN device applications.

The much higher critical electric field of the GaN devices compared to their Si counterparts (Table 1) allows the former to achieve smaller size for similar applications. The small size of the devices, although an attractive feature, imposes difficulties at the thermal management as is, for example, the mounting of the heat sink on the package for top side cooling, especially in situations where flip chip is used. Finally, an important feature of GaN devices that can be proved beneficial for thermal management is their higher operating junction temperature compared to Si based devices. Nitronex has demonstrated an MTTF (= Mean Time To Failure) over 10^7 hours for a junction temperature of 160^oC while an MTTF of 10^6 operating hours can be achieved (reliability requirement) for junction temperature of 180^oC [27]. This feature can be fully exploited when the switching device operates at higher temperature compared to the rest of the components and, thus, allowing simpler thermal management for the GaN device while improving the reliability and efficiency for the rest of the components.

The thermal management approach might differ considerably depending on the application requirements and the package specifications (thermal resistance). Passive or active, bottom side or top side cooling, PCB copper plate thickness, use of heat spreader, plain or 3D PCB, etc are some of the options that need to be carefully considered for the thermal design.

2.2.6 The Figure of Merit

At the previous paragraphs the most important advantages and features of GaN devices were presented, explained and compared to the corresponding Mosfet features. From these some deductions regarding the important assets of the new technology can be extracted. However, for a more straightforward comparison of the new and the old switching technology, on the basis of the power electronics applications, we can use the so-called Figure of Merit (FoM). The FOM diagram is used by MOSFET manufacturers to show generational improvements and to compare competitive devices and it is the product of the gate charge Q_g and the on resistance $R_{DS,on}$. This product is almost constant for a given generation or device technology and it is characteristic of it. Here, the EPC approach and data for the comparison of the two technologies are used. For this, two products are compared, the Q_gd - $R_{DS,on}$, called switching FoM (figure 2.6 [28]), and the Q_g -$R_{DS,on}$ called conduction FoM. (figure 2.7 [28])

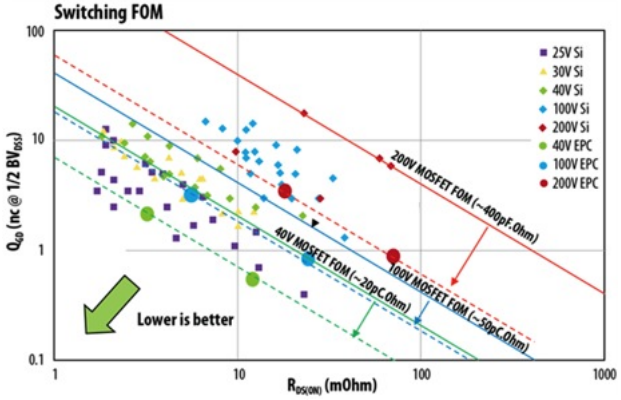


Figure 2.6: Switching FoM [28].

From the previous figure it is clear that for each voltage level the GaN devices outmatch the corresponding Mosfet devices which means that the newer technology can

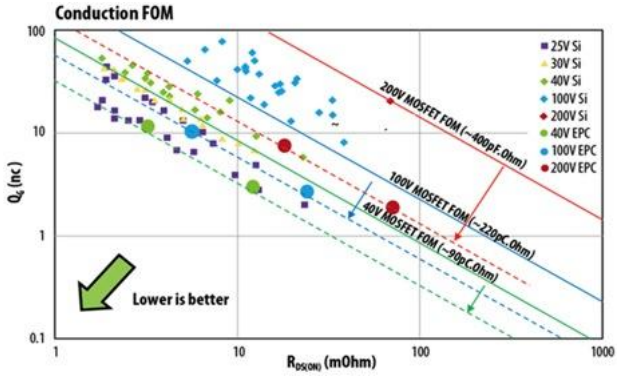


Figure 2.7: Conduction FoM [28].

be proved beneficial for the power electronics field, if its advantageous features are well understood and exploited.

2.2.7 GaN Devices in Power Electronics

Power GaN devices have been commercialized only recently (2010) and up till now there are few companies who are active in this field but their number is steadily increasing as GaN device market is growing. Reports forecast that GaN market is going to grow up to 350$ million in 2015 [29] and over 1$ billion in 2021 [30]. This designates a considerable shift of interest towards this new technology which is justified by the expected contribution of GaN devices at the power electronics field that can be briefly and roughly described as smaller converter size, high switch breakdown voltage and enhanced converter's efficiency.

However, if these new devices are indeed about to replace the silicon based switches their superiority needs to be proved in practice and for that the research interest, from the power electronics point of view, lies on the actual benefits that they can offer as regards the efficiency, the performance and, of course, the cost for existing applications and topologies compared to the older technology as well as the new perspectives and possibilities that they provide. Thus, there has been great effort to exploit the full capabilities, identify the main bottlenecks and deal with the problems of GaN switches on power electronics application.

One of the main research areas regards high voltage applications using high voltage GaN switches. It should be mentioned that up till now there are not commercial GaN devices over 600V, mainly due to the restriction that the lateral structure imposes and the occurrence of the current collapse phenomena. W. Saito et al. have focused the research on the latter problem [18] and they presented back in 2008 a 120W,1MHz boost converter with efficiency 94.2% under a peak voltage of 350V [31] and a 7-10W,13.56MHz resonant inverter with efficiency over 90% under a drain peak of 380V [32]. For both applications double field plate switches were used. At the same time Y. Wu et al. using depletion mode (d-mode) GaN devices constructed a 97.8% efficient 175 to 350V,300W boost converter at 1MHz [33]. More recently, on 2010, Jordi Everts et al., presented a boost converter based on an enhancement mode (e-mode) GaN transistor where they achieved maximum efficiency of 96.1% at 106W,512.5kHz,76 to 142V and maximum efficiency of 93.9% at 97.5W,845.2kHz,76 to 142V [34]. On 2011 Tatsuo Morita et al. presented a 99.3% efficient 900W three phase inverter with DC bus voltage of 200V and carrier frequency 6kHz [35]. For this application the GIT GaN transistor which was used overrun the Si-based IGBT that was used at the same topology. Finally, an LLC resonant converter was used by W.Zhang et al. to compare the performance of

the topology when 600V Cascode GaN HEMT and state of the art Si CoolMos switches are used [21]. The results showed that the total device loss was improved by 42% when GaN devices are used, however, the total efficiency was improved only by 0.5%. The advantages of a 600V GaN cascode structure over silicon Mosfet were also verified at [36] where a 1MHz 300W 400V/12V LLC converter is demonstrated and used to compare the two different devices. Research on this field shows that GaN devices are suitable for high voltage power electronics applications and that they perform better than Si based devices. However their maximum breakdown voltage is still limited.

At the research area of low voltage power electronics significant development has taken place at high power density applications and specifically at the point of load converters. On 2012, D. Reusch et al. demonstrated a 12V, 20A, 2MHz converter with efficiency 83% and power density 750 W/in^3 the highest compared to industry products and research up until then [37]. The following year Shu Ji, D. Reusch and F.C. Lee managed to increase even more the power density of POL converters by demonstrating three 12V to 1.2V POL modules: a single phase 20A, 900 W/in^3, 2MHz using e-mode GaN switches and a single phase 10A, 1100W/in^3, 5Mhz and two-phase 20A, 1100 W/in^3, 5Mhz using d-mode switches [38]. The previous results make clear the significant contribution of GaN devices for low voltage high power density applications. Still at the low voltage area of power electronics, a research made by M.Acanski, J. Popovic-Gerber and J.A. Ferreira clearly showed that e-mode GaN devices used at a 12V to 48V boost converter, aimed for PV applications, achieved better efficiencies compared to their Si counterparts for power values over 60W while operating at double the switching frequency, which also resulted to smaller passive components. The combination of smaller size and better efficiency, thanks to the GaN utilization, is very important for most power electronics applications. The results of the same research, however, showed also that for operation of the converter at lower power values the Si device exhibits better performance (still though at half the frequency) and that is because the GaN device lost its advantage of lower power losses. Finally, the capability that the GaN power devices offer for pushing high the operating frequency was also demonstrated by M. Rodriguez, Y. Zhang and D. Maksimovic at [40] and [41]. At these papers the researchers showed that a 10W buck converter with input voltage up to 40V achieved efficiencies over 95% at 10MHz and over 90% at frequencies up to 40MHz.

Finally, significant research has been also conducted at soft switching topologies like resonant converters where switching losses of the devices can be minimized. For this case, however, the performance of GaN devices compared to Si counterparts cannot be foretold. Weimin Zhang et al. have focused on the performance of all-GaN-based LLC resonant converters and at the papers [21], [34] it is shown that although the switching device losses have been significantly improved when GaN devices were used the enhancement of the efficiencies was only 0.5% and 0.3% respectively.This is because at this kind of topologies by far the greatest contribution of losses come from the transformer component (around 60%). As a result, to fully exploit the GaN capabilities in this occasion the magnetics need to be carefully designed, optimized and new concepts which could exploit the high frequency capabilities of GaN devices should be introduced. Towards this direction D. Reusch and F.C Lee at [43] they study the impact of increased switching frequencies on transformer size and the ability of GaN transistors to increase switching frequency in high frequency resonant topologies. At the same paper they demonstrate a 48V/12V resonant converter which used matrix transformer to improve its performance.Comparing the performance of GaN and Si-based switches it was proved that at loads of 15A the efficiency of GaN devices was 2% higher while operating at double frequency (1.6MHz compared to 800kHz of Si devices). At full load (30A) the efficiencies matched but the GaN based convert had a 100% (900 W/in^3) increase of power density

compared to state of the art Si discrete designs of the date.

GaN switching technology is still at its very early stages and its full capabilities have not yet been fully exploited. However, the definite benefits that can offer are expected to give a significant boost to the area of power electronic and its various applications such as consumer power supplies, LED/OLED driving, automotive industry (HEVs and EVs), PVs and the very demanding aerospace industry. Currently, the commercial devices are GaN-on-Si, mainly due to their low cost, with a breakdown voltage limit at 600V but the extensive research and the increased competition in this field is expected to push the prices down and enhance the capabilities of the devices.

Chapter 3

The Converter Design Procedure

This chapter presents thoroughly the most important steps of the design procedure for the construction of the OLED driver according to the limitation and requirements that are set by the Audi automotive industry. It should be noted that at this chapter the various theoretical aspects that are considered a well established knowledge and can be found in the literature are not presented.

Initially, the driver specifications are clearly stated, the procedure for the selection of the appropriate topology for the converter is presented and the criteria and reasons that support the specific choice are explained. After that follows a short description of the topology and the operating mode as well as the equations that describe the operation of the converter and that will be used at the analytical model. A very thorough description of the Mosfet switching, the influence of the parasitics and the loss model of the GaN switch that will be used at the model follows. Then, the design of the magnetic component is presented and, after that, the process for the selection of the appropriate inductance value is explained. Finally, at the end of this chapter, some design considerations, mainly related to the PCB design, are shortly discussed.

3.1 Driver Specifications

In the chapter of the introduction it was stated that for the project the various electrical and mechanical specifications are in accordance with the requirements of the Audi Lighting Department and the technical standards of the company. These specifications are in detail presented here.

The lighting system of interest is the tail lights of the vehicle, at the lamp housing of which the mechanical and electrical subsystems must be able to function at operating temperatures ranging from -40^oC to 85^oC, using natural cooling and without a direct heat path to the chassis.

The power supply is a 12V system with an actual voltage range from 6V to 19V and a diagnostic range 8.5V to 16.5V. However, for reasons of simplicity the input voltage is considered to be stable at the level of 13.2V assuming to be the output of a

previous level DC/DC converter. Each tail-light segment is housing OLED lights of a total maximum surface area 40 cm^2 and the number of OLED components is chosen to be 5 with parallel connection. There will be one DC/DC converter capable of driving all OLED components of a light segment and placed at the free space of an OLED structure, the master OLED. The required current density for a proper operation of the OLED devices is chosen to be 25-30 mA/cm^2 which means that, in total, the OLED configuration will draw a 1-1.2A current. The typical forward voltage for a single stack OLED ranges from 3.6V to 4.5V. For this application double and triple stack OLEDs are assumed which give a voltage range of $2 \cdot V_f$ and $3 \cdot V_f$ respectively. The forward voltage is strongly dependent on the temperature, and for the boundaries of the current application it gives Vf(-40C)=Vf(22C)+1V and Vf(+85C)=Vf(22C)-1V. As a result the output voltage range is chosen to be 6.5V to 14.5V. This leads to an output power range for the converter of 6.5W (1A, 6.5V) to 17.4W (1.2A, 14.5V). Finally, isolation of the converter from the mains is not necessary. The following table summarizes the driver specifications.

Driver Electrical Specifications	
Input Voltage (V)	13.2
Output Voltage (V)	6.5...14.5
Output Voltage Ripple	10-15%
Output Current(A)	1...1.2
Output Power (W)	6.5...17.4
Operating Temperature (^oC)	-40...85
Isolation	No

Table 3.1: Electrical Specifications for OLED Driver.

3.2 Topology Selection

An important step for this project is the selection of the driver topology. The OLED driver should meet the specific electrical and mechanical requirements imposed by the Audi lighting specifications, as already presented. However, since the main goal of this thesis project is the investigation of the benefits that the GaN switching devices can offer and the possibility of using them at OLED drivers, the final criteria for the topology selection are closely related to these objectives.

At this paragraph, based on these specifications and the objectives of the project the reasoning for selecting the appropriate topology for this application is discussed. The selection process includes two parts. At the first part the candidate topologies are selected out of the whole set of the available DC/DC converters based on their main characteristics and their suitability at this application. At the second part the candidate topologies are compared more thoroughly based on more specific criteria and using the results of the analytical equations, which have been calculated for the candidate topologies. As a result of this process the topology that will be implemented at this project will be determined.

3.2.1 Choosing the Candidate Topologies

There is a considerably wide range of available topologies for DC/DC converters each one offering specific advantages and disadvantages and being suitable for certain types of applications. In order to select the most appropriate of these topologies for this project at first the placed criteria for the topology selection are more general and they are based

on the basic driver specifications. These are:

- Buck-boost conversion capability.
- Mains isolation not necessary. Auxiliary windings not needed.
- Low power operation.
- Smallest number of components possible.

Based on these criteria a first comparison is possible. Here, the reasons for which each topology is or is not suitable for this application are briefly explained.

Buck Converter : Does not offer the appropriate coversion ratio so it is excluded.

Boost Converter : Does not offer the appropriate coversion ratio so it is excluded.

Buck-Boost Converter : Its conversion ratio is suitable, it does not require a transformer, it is suitable for low power applications and has a reasonable number of components (one switch topology). In addition, soft switching methods, like operation in boundary conduction mode or modification to a quasi-resonant topology, can be applied enhancing its efficiency. Thus, it can be a candidate topology.

Cuk family Converters : This family contains the Cuk, Sepic and Zeta converters. All of them provide suitable conversion ratio and do not require a transformer. They are appropriate for low power applications and have a reasonable number of components, however two more passives compared to the buck boost converter (extra inductor and capacitor). Thus, they can be candidate topologies.

Flyback Converter : It is not considered as an option since its non-isolated form, that is the buck-boost converter, matches better the placed criteria.

Forward Converter : It is the isolated form of the buck converter. It requires a coupled coil and in general is outperformed by the flyback converter. Therefore, this topology and its modifications - Two- switch forward, Parallel forward - are excluded.

Full/Half Bridge Converter : This topology is oriented for high power applications and it is excluded.

Push-Pull Converter This converter is useful when multiple outputs are required. However, because of the use of a transformer, which is usually overdesigned, and because there are no special advantages that can offer to that application this topology is excluded.

Full/Half Bridge Load-Resonant Converters : This category of dc/dc converters can utilize soft switching to achieve high efficiencies and relatively small size. For their operation, however, they require either a transformer or a full bridge diode rectifier and generally larger number of components. Although the size of the transformer can be quite small, operation at high frequencies, which is the goal of this project, would result to increased parasitics and losses due to the magnetics (see corresponding literature GaN). In addition, both half bridge and full bridge resonant converters are more suitable for higher power rating applications, according to literature. Therefore they are also excluded.

In conclusion, according to the previous discussion, the topologies that are considered to be suitable for this application are the Buck Boost converter and the Cuk family. Buck

Boost converter can have three modes of operation the continuous, the discontinuous and the boundary (self - oscillating) conduction mode. In addition, on this converter soft switching techniques, in the means of quasi-resonance, can be applied. The Cuk family can operate at continuous and discontinuous conduction mode. At the next part the two converters and their operating modes will be compared.

3.2.2 Selection of the Appropriate Topology

The Candidate Topologies

Here the candidate topologies are discussed briefly and then compared based on the results of the analytical equations and their related characteristics. Two topologies are presented. The first is the buck-boost converter at the three operating modes: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM) and Boundary Conduction Mode(BCM). The second belongs to the Cuk family of converters which includes the Cuk, the Sepic and the Zeta converter. All of these converters have buck-boost conversion ratio and require two magnetic components and one capacitor to transfer the power from the input to the output. The differences between these topologies have to do with the relative position of the magnetic components which results to different ripple of the input and the output current. Other than that their differences are not considerable. Therefore, only one of the three topologies is presented and this is the Sepic converter, at Continuous and Discontinuous conduction modes.

Buck Boost Converter

The buck-boost converter is a simple one-coil topology capable of both bucking and boosting the input voltage but with the expense of an inverted output. It can operate in continuous mode (CCM), where the inductor current is always larger than zero, in discontinuous mode (DCM), where the inductor current is zero for a time period during one cycle, and in an intermediate mode, the boundary conduction mode (BCM), where the switch turns on when the inductor current becomes zero. The schematic of a buck boost converter is shown at figure 3.1 and some characteristic waveforms when operating at CCM at 3.2.

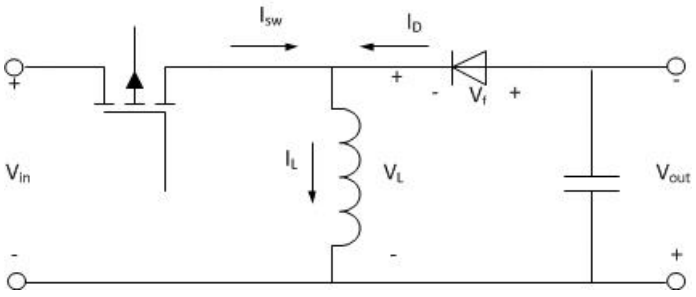


Figure 3.1: Schematic of a buck-boost topology.

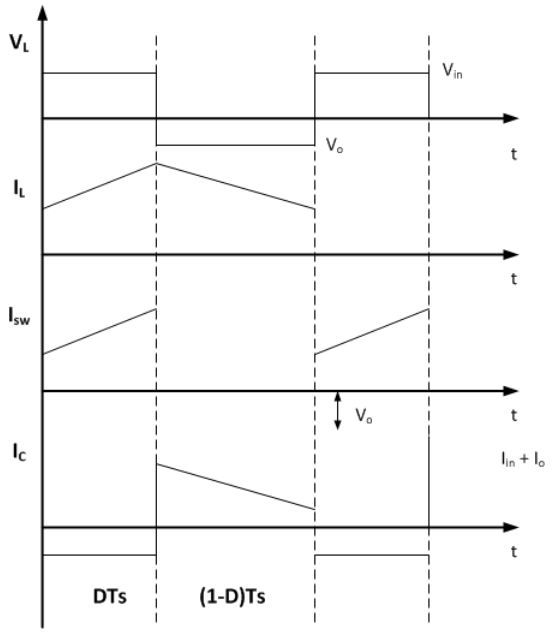


Figure 3.2: Characteristic waveforms of a buck-boost topology at CCM.

Sepic Converter

The Sepic Converter belongs to the family of the Cuk converter. It includes two coils and one capacitor (plus the output capacitor) which are responsible for the energy transfer from the input to the output. It has the possibility of bucking and boosting the input voltage but without inverse output. Its main advantage is the low ripple input current. It can operate in continuous mode, where the currents of both inductors never become zero and in discontinuous mode where the sum of the inductor currents is zero during a time period of a cycle. It should be noted that in the last case one of the two coils has a continuous current whereas the other gets negative values.The schematic of the Sepic converter is shown at figure 3.3 and some characteristic waveforms when operating at CCM at 3.4 .

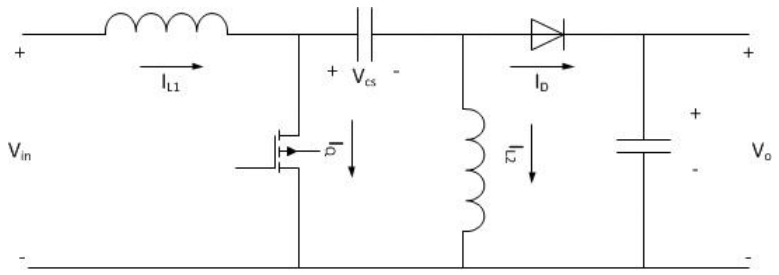


Figure 3.3: Schematic of a sepic topology.

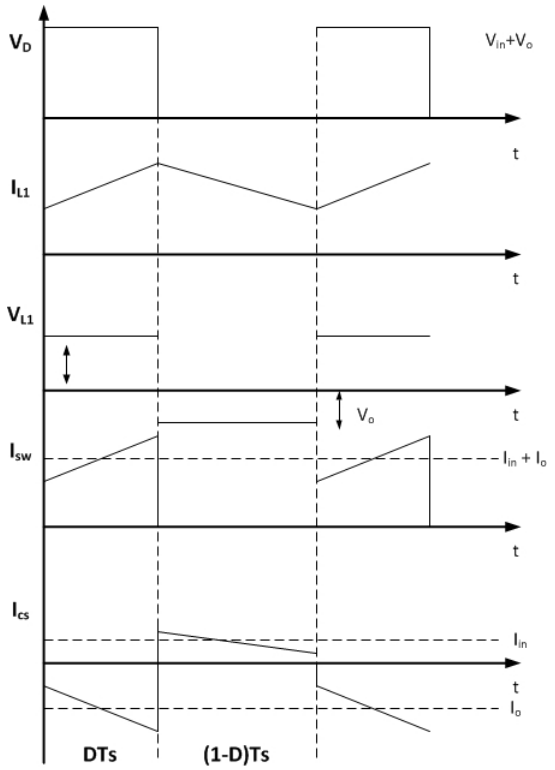


Figure 3.4: Characteristic waveforms of a sepic topology at CCM.

Criteria for Topology Comparison

The application requirements and the thesis objectives specify the criteria of the comparison. These criteria shorted from the most to the least significant are the following:

- Size of the converter.
- Total efficiency.
- Complexity.
- Cost.

Size

Since the converter is designed to be an OLED driver for automotive lighting, where the available area for the placement of the driver is limited by the size of the master OLED segment, as mentioned previously, this design parameter is of the utmost importance. The size of the GaN switches that will be used is negligible, hence the biggest consideration is the volume of the passive components (and more specifically of the magnetics) since heat sink is not used.

In order to estimate and compare the size of the converter, as it would result for each topology and operation mode, the following values were taken into consideration (note that the comparison took place under the same operating frequency):

- The stored energy in the passive components and the losses on the switch and the diode. That is because stored energy is proportional to the size of the passive components. The maximum stored energy for an inductor during a cycle is given by $E_L = 0.5 \cdot L \cdot I_{L,peak}^2$ whereas for a capacitor $E_C = 0.5 \cdot C \cdot V_{C,peak}^2$. When increasing

the operating frequency the size of the passives decrease but the switching losses on the switching device would increase, limiting this way the maximum value of the frequency.

- The power rating of the switching components. The voltage and current rating of a switch determines its size.
- The total number of components. Even if the total size of two discrete components is smaller than one, placing them on a pcb board would most likely occupy some extra space for safety and practical reasons. The number of components is determined by the kind of the topology.

Efficiency

As in all real life applications efficiency is a very important design aspect. Optimum goal for the design of this converter is to achieve sufficient performance for a minimized size. The contribution of the GaN devices towards this direction is going to be investigated at this thesis.

When comparing the different topologies in terms of efficiency the values of the switch, inductor and capacitor currents need to be calculated at a certain operating frequency. Also, as regards the inductor losses the size of the component should be considered (bigger size means harshly higher number of turns, which increase the ohmic losses, and bigger volume of the core, which increases the core losses).

Complexity

Complexity of the topology is unwanted as it can add to the final cost and can make the construction of the driver unattractive. The complexity can be realised by the number and type of components and the complexity of the design and the control of the topology.

Cost

A cost effective OLED driver is a desirable feature since more than one drivers are expected to be used for an ideal automotive lighting. The use of the recently commercialized, and thus still expensive, GaN devices is expected to rise the total cost either way so the cost of the switching and the other components used at a certain topology needs to be considered.

Comparison of the Topologies

Based on the previously presented criteria, and using the results of the first order analysis of the two topologies, a qualitative, and partly quantitative, comparison is possible. The comparison will take place for each criterion individually and in the end a total conclusion will be drawn. It should be noted that a fully quantitative analysis, although possible, is not followed since it would require complete design and analysis of each option which is not the goal of this chapter.

For the construction of the tables used at this paragraph the analytical equations of each topology and conduction mode where used and it was assumed an operating frequency of 1MHz (for BCM a range of frequencies with 1MHz max frequency), voltage ripple 10%, $V_D = 0.7V$ and $P_{o,max} = 17.4W$. Then, the required inductances and capacitances, the peak inductor current and the diode, inductor and switch rms currents were calculated for each case. For the passive components size comparison the equations expressing the stored energy in these components were used. In order to compare the

switching and conduction losses the values of the RMS and peak currents, as well as the voltages across the switching components were used.Note that, since the voltage across the switching components is the same for both topologies then the current values are enough for a qualitative comparison.

Comparing the size

As explained previously the size is roughly a function of four factors: the stored energy in the passive components, the losses on the switch and the diode, the total number of the components and the power rating of them.

Energy in Passive Components

At the following two tables the topologies and modes are presented and ranked according to their performance as regards the size of the passive components and the switching losses of the switch and the diode.

Performance		
	Magnetic Components	Capacitive Components
BB CCM	- -	++
BB DCM	++	- -
BB BCM	+	-
S CCM	- -	+
S DCM	++	- -

Table 3.2: Performance of each case as regards the size of the passive components.

Performance				
	Switching Losses		Conduction Losses	
	Switch	Diode	Switch	Diode
BB CCM	-	-	+	+
BB DCM	-	- -	- -	- -
BB BCM	++	+	-	-
S CCM	-	-	+	+
S DCM	++	+	-	+

Table 3.3: Performance of each case as regards the losses on the switching components.

Power Rating of Switching Components

In both cases the maximum steady state voltage across the switch is $V_{sw} = V_{in} + V_{out}$ which has a maximum value of 27.7V. Also in all operating modes of these topologies, when using a reasonable inductor value (that is for example approx. 2x the value of L_{bcm} at Buck-Boost CCM or $>/2$ the boundary value for DCM) an operation where the maximum currents are well below 10A can be achieved. This way the same GaN component (i.e 40V,10A of EPC which is the minimum in production) can be used and the power rating of the switch does not play any role as regards the size. The same holds for the diode, where the voltage rating is the same for all cases, and the difference of the peak currents is relatively small. This means that there is no significant gain as regards this size between the different modes and topologies.

Total Number of Components

The total number of components refer only to the basic components of the topology neglecting any measurement or control component. At the following two tables the topologies and modes are presented and ranked according to their performance as regards the required number of components.

	Performance
Buck Boost	+
Sepic	-

Table 3.4: Performance of each topology as regards the total number of components.

Conclusion

Based on the previous discussion and the rating at the corresponding tables it might not be totally obvious which case is the best as regards the size, although Buck Boost at BCM and Sepic at DCM seem to achieve better performance. To make this even more clear it is necessary to point out the design aspects that are of special interest at this application and thesis project.

As already explained, it is crucial to achieve a low inductance value and a small magnetic component since, among all, it is planned to design a planar inductor using low profile magnetics. Therefore, small magnetic component is an important design aspect. Equally important are the switching and conduction losses on the switch. The reason for that is that thermal conduction from GaN devices is a challenging process because of the very small size of the component and the high thermal resistance from the device to the PCB. This means that minimization of the losses on the switch are of the utmost importance.Less significant than the previous two are the losses on the diode and the size of the output capacitor. Last is the number of components.

After illustrating the key aspects of the design it is clear, based on the presented rating, that Buck-Boost converter at BCM and Sepic converter at DCM achieve the best performance since they combine low size of the magnetic components and lowest switching losses. The conduction losses of the switch at both cases are slightly higher than the CCM modes. Between these two choices, Buck Boost at BCM requires less components which is a definite advantage.

Comparing the Efficiency

The second design criterion is the efficiency of the converter and it comes, as regards its importance, immediately after the size of the converter. Actually, efficiency and size are strongly connected with each other and during the design this always leads to a trade off among them.

The efficiency depends on the total power losses of the converter during its operation, the sources of which are various. The most important factor on the power losses on a SMPS converter are the switching components with their switching and conduction losses. Significant contribution on the overall efficiency have, also, the magnetic components with the core and ohmic losses which are highly dependent on the frequency, the size and the geometry of the component. The output capacitance and the driver losses are, at a proper design, usually less significant.

Losses on Switch and Diode

The losses on the switching components have been already discussed at the previous

paragraph and their performance was presented at table 3.3.

Losses in Magnetic Components

The losses of a magnetic component come from the ohmic losses at the coil conductors, the resistance of which increase with increased frequency due to the skin and proximity effect, and the core losses which are divided to eddy current losses and hysteresis losses and are highly dependent on frequency while the latter depends also on the volume of the core.

It is quite difficult to predict the contribution of the losses on the magnetic component at a qualitative analysis without the design of the inductor at each case. However some conclusions can be drawn based on the calculated values. As regards the ohmic losses of the component, at first glance, it could be said that the DCM modes with the higher RMS currents would lead to higher ohmic losses. However, this is partly true since at CCM modes the higher inductance value (in buck boost it can be 5 times higher as shown in the results) requires higher number of turns which results to higher resistance. For that, their difference in respect to ohmic losses becomes smaller. At CCM mode the ripple of the inductor current is smaller (but not much smaller at the examined cases where the inductor value is kept small so that it can be comparative to the other cases) compared to the other modes, which would suggest much less core losses but, on the other hand, the volume of the inductor is bigger therefore it deteriorates slightly its performance.

As a conclusion, since the performance of the topologies in respect to the losses of the magnetic component is not easy to be evaluated without a proper design of the component it will be assumed that their contribution on the total losses is more or less equal.

Conclusion

At an SMPS converter the losses on the switching components are the most determinant for its efficiency with the losses on the magnetics following closely, especially at a buck boost topology. Since the determination of the latter requires analytical design it was assumed that regardless the case the influence of the magnetics is the same. The fact that efficiency is not the highest priority factor allows, to a certain extend, such an assumption. As a result, based on the rating at the presented tables and the previous discussion it can be concluded that the BB BCM and S DCM seem to have the best overall performance, at least for this application. Of course, this conclusion is based on the assumptions and the data that are available at this stage of the thesis.

Comparing the Complexity

The complexity of a topology can be evaluated by the number and type of components and the complexity of the design and control.

As it can be realised from the schematics of the two topologies both of them require the same type of components but Sepic converter requires two extra passive components compared to the buck boost converter. This fact adds some complexity both at the operation and at the design of the converter and especially it results to far more complicated analytical equations. This is even more obvious as regards the Sepic converter at DCM operation. Also, the extra magnetic component for the Sepic converter means also requirement for extra designing. Finally, the dynamics of the converter become much more complex as the AC analysis of the converter leads to a transfer function with a forth-order denominator and RHP zeros. It is clear, therefore, that as regards complexity Sepic converter, regardless of the operation, falls back compared to Buck Boost converter.

Between the Buck Boost modes BCM mode is slightly more complicated compared to CCM and DCM because of the requirement of turning on the switch when the inductor current becomes zero. Also, because of the frequency variation with the load, special care needs to be taken so that very low and very high operating frequencies are avoided.

Performance	
BB CCM	++
BB DCM	++
BB BCM	+
S CCM	-
S DCM	-

Table 3.5: Performance of each topology as regards the complexity.

Conclusion

As regards the complexity of the topology, the design and the control it is obvious that Buck Boost at CCM and at DCM are the most suitable options. Buck Boost at BCM is slightly more complicated than the previous two and, finally, Sepic converter comes last, independent of the operating mode.

Comparing the Cost

It is quite clear that despite their differences at size, losses and complexity the cost for all options is similar, or at least their small differences cannot be evaluated at this stage. Even more, since this is a research project the cost of the topology, although a design criterion, is not of high priority as it would be in the case of an industry project. Consequently, there will be no rating of the topologies as regards their cost and it will be assumed that all option are equal in respect to this criterion.

Final Conclusion

Previous paragraphs presented the comparison of the candidate topologies in respect to four basic criteria: size, efficiency, complexity and cost with the assist of the results of the analytical equations. The comparison was mainly qualitative, since a complete quantitative would require detailed analysis and design of each case, and for that in some cases, like when comparing the cost, accurate conclusions were not possible to be drawn. However, in total it was possible to distinguish the most suitable topology for this application.

It has already been mentioned that achieving small size is the most important design aspect for this application and efficiency is following. Complexity and cost come in the end as regards their priority in the design considerations. From the previous discussion it was concluded that as regards size Buck Boost at BCM and Sepic at DCM are the most suitable options. The same topologies also distinguish compared to the other options as regards their performance at the efficiency. It is quite obvious then that the final choice should be made between these two. However, when comparing the two topologies as regards their complexity it is clear that Buck Boost at BCM is preferable to Sepic at DCM. Considering, finally, the fact that as regards the cost the two options do not have significant differences it means that Buck Boost at BCM is the topology of choice.

3.3 Buck-Boost Converter at BCM with Valley Switching

At the previous paragraphs the reasons for choosing the Buck Boost operating at BCM were explained and at figure 3.1 the topology of the converter was presented. Buck-boost is a widely known topology with a simple operating principle which is extensively analysed at the literature and, therefore, it is not presented here. However, the operation of the converter at BCM with Valley switching will be discussed at this paragraph and the corresponding equations will be presented.

3.3.1 The Boundary Conduction Mode

As already explained, at the Boundary Conduction Mode the new switching period starts when the inductor current returns to zero, which means that it is at the boundary between Continuous and Discontinuous Conduction Mode. Since the value of the inductor of the converter is constant, in order to achieve the boundary condition for all the range of the load the frequency needs to vary depending on the operating point. Variable frequency is a fundamental feature of this mode.

Operating the converter at the boundary leads to higher RMS currents compared to CCM for the inductor and the switching devices but it allows for zero current, or depending on the control for zero voltage, switching. This means less losses for the switching devices. This advantage can be proved very beneficial for high frequency operation where the switching losses usually determine the converter's efficiency.

3.3.2 Boundary Conduction Mode with Valley Switching

Valley switching is called the switching method applied at boundary conduction mode (BCM) at which the turn on of the switch does not happen directly when the current goes to zero but instead after half cycle of the oscillation that follows the zero-current instant. This oscillation of the drain current and the voltage of the switch is the result of the resonance between the output capacitance of the switch, C_{oss}, and the inductor L. This way apart from the zero current switching that is achieved, the drain voltage at the turn on switching also reduces and it might even go to zero, depending on the output voltage (the voltage across the switch when the switch turns on is $V_{in} - (Vo + Vf)$). At the following figures the inductor voltage and current during a full circle as well as the voltage across the switch are shown.

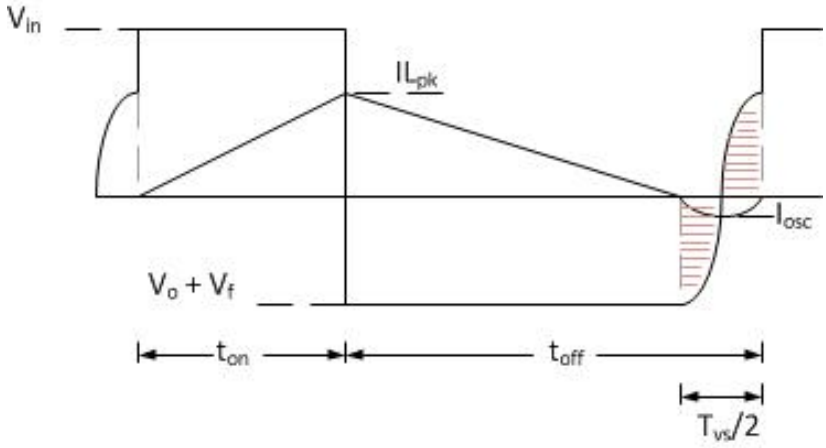


Figure 3.5: Inductor Voltage and Current Including the Oscillation.

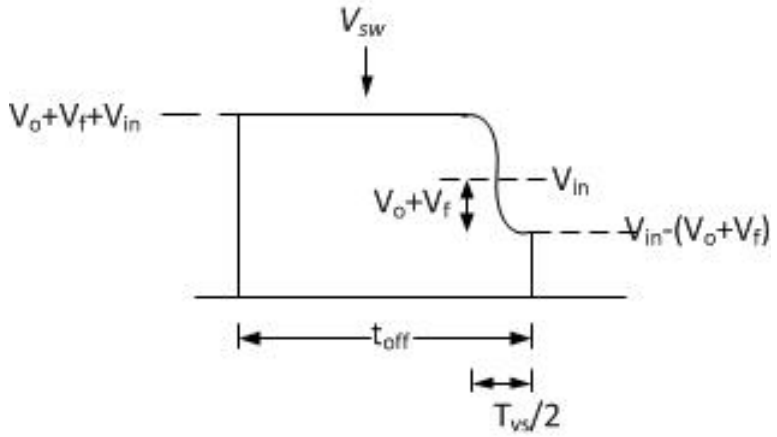


Figure 3.6: Voltage across the switch during the turn off and the valley switching transient.

Because of this oscillating transient the switching frequency is prolonged and the output current and voltage are reduced. In order to compensate for the influence of this transient the oscillation period needs to be considered in the equations that are used to calculate the steady state values of the buck-boost converter at BCM.

Assume that the load of the converter is (V_o,$\bar{I}_o$). Then the steady state equations for the converter, based on figure 3.5, are the following. Note that the two highlighted areas are equal and so they do not influence the Volt·sec balance equation.

$$V_{in} \cdot t_{on} = (V_o + V_f) \cdot (t_{off} - T_{vs}/2) \tag{3.1}$$

$$\frac{V_{in}}{L} \cdot t_{on} = I_{L,pk} \tag{3.2}$$

$$\bar{I}_o = [\frac{1}{2} \cdot I_{L,pk} \cdot (t_{off} - \frac{T_{vs}}{2}) - \frac{2}{w} \cdot I_{osc}] \frac{1}{t_{on} + t_{off}} \tag{3.3}$$

where
V_f is the forward voltage of the diode.
$T_{vs} = 2 \cdot \pi \cdot \sqrt{L \cdot C_{oss}}$ is the period of the oscillation and, thus, $w = \frac{2\pi}{T_{vs}}$
$I_{osc} = \dfrac{V_o + V_f}{\sqrt{L/C_{oss}}}$ is the peak of the oscillating current.
t_{on} and t_{off} are the time periods when the switch is on and off respectively.

The previous equations are solved depending on which values are known and which are unknown. For a known operating point, the unknowns are the $I_{L,pk}, t_{on}$ and t_{off} and solving the system their values can be found.

It should be noted that when operating the converter at valley switching the frequency is different compared to a simple BCM operation. This can be easily realised from figure 3.7, which shows the relation between frequency and output voltage for a certain value of inductor for BCM and BCM-VS operation.

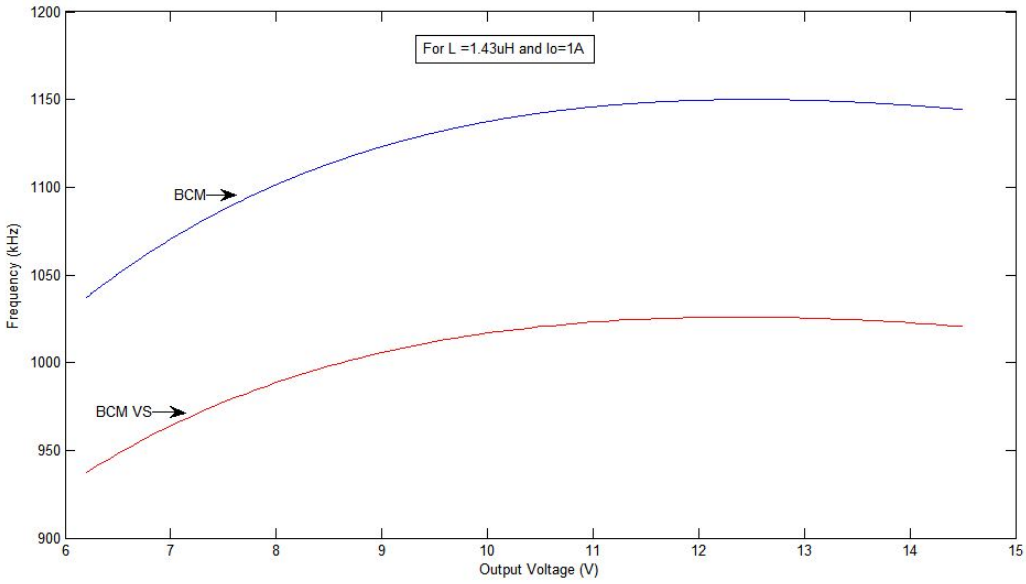


Figure 3.7: Maximum Frequency and Output Voltage for BCM and BCM-VS.

Note : For a certain inductance value the operating frequency depends on the load, that is the output voltage and current. The output voltage influences the operating frequency the way figure 3.7 shows. The output current influences the frequency inversely, which means the smaller it is the higher is the operating frequency.

In the previous equations the ESR of the inductance can also be

Influence of Equivalent Series Resistance of Inductor

The ESR of the inductor component is frequency dependent because of the skin and proximity effects. The effect of this value is not included in the steady state equations of the converter that were previously presented. When the value of ESR is low, which depends on the geometry of the coil and, of course, the operating frequency, its influence is negligible but when its value is high enough then considerable inaccuracies occur at the results of the steady state equations.

Therefore, for more accurate calculation it is necessary to include this influence of ESR in the Buck Boost equations. ESR leads to a voltage drop across it and thus the voltage across the inductor changes. Most of the realistic values of R are small enough so that both voltage and current can be considered linear. The new system of the steady state equations for the buck boost converter when operating at BCM with VS including ESR is:

$$\frac{2 \cdot V_{in} - I_{L,pk} \cdot ESR_L}{2} \cdot t_{on} = \frac{2 \cdot (V_o + V_f) + I_{L,pk} \cdot ESR_L}{2} \cdot (t_{off} - T_{vs}/2) \tag{3.4}$$

$$\frac{2 \cdot V_{in} - I_{L,pk} \cdot ESR_L}{2 \cdot L} \cdot t_{on} = I_{L,pk} \tag{3.5}$$

$$\bar{I}_o = [\frac{1}{2} \cdot I_{L,pk} \cdot (t_{off} - \frac{T_{vs}}{2}) - \frac{2}{w} \cdot I_{osc}] \frac{1}{t_{on} + t_{off}} \tag{3.6}$$

3.4 The GaN Switching Loss Model

As it has already been pointed out at this thesis project it is an objective to use a GaN device operating at high frequencies. High frequency operation, though, is accompanied with higher losses and more intense thermal stress on the switching device which can lead to low efficiencies or even the breakdown of the switch. Therefore, in order to ensure sufficient and effective thermal management for the converter an accurate calculation of the power losses is required. And although the calculation of the losses for most of the converter components and of the conduction losses of the switch is a simple process this is not the case for the calculation of the switching losses. For the latter, the method and the loss model that is used is decisive for the calculation accuracy especially in high frequency operation where a small calculation error, due to an approximation or an assumption for example, can lead to significantly different results.

Generally, various loss models have been proposed for Mosfet switching, each one achieving different accuracies and simulation times. Because, the main factor that limits the accuracy of a model is its complexity and, thus, the time required to simulate the model. Based on these two aspects the loss models can be divided into three main categories [44]: The physical models, the behaviour models and the analytical models. The physical models require the physical parameters of the device and the circuit and using finite element analysis tools can calculate accurately the device losses but with the expense of large computing resources and simulation time. Less accurate but faster are the behaviour models where the device models provided by the vendors can be used at spice simulation tools to calculate the switching losses. Finally, the analytical models, which describe the switching transient with a couple of algebraic equations, provide less accuracy compared to the previous methods but they are much faster, more adjustable and they are suitable for parametric analysis. The classical piecewise-linear model belongs to this last category. From the three categories previously described, the last one i.e the analytical model is usually much preferable when designing a converter because of the simplicity, the suitability for parametric analysis, especially when some design parameters are not predefined, and the small simulation time.

At this paragraph the analytical model that is going to be used for the calculation of the switching losses of the GaN device will be presented and its suitability for this certain application will be justified. Its main advantages and disadvantages will be noted as well as its shortcomings. Before that, however, the influence of the various device and circuit parasitics will be briefly presented because it is considered useful for the model evaluation.

3.4.1 Mosfet Switching and the Influence of Parasitics

The Mosfet principle of operation and the switching process have been extensively and accurately described through the years at the scientific literature and the various power electronics textbooks. For that reason it is not considered necessary to repeat this well established knowledge but instead the reader is referred to corresponding literature (for example [45], [46]). Note that at most of these textbooks, although useful to comprehend and understand the basic principles of the switching operation, the used models are simplified, usually neglecting some of the circuit and switch parasitics, and, thus, they are valid under specific conditions. For that reason, these simplified models can be proved inaccurate at situations where the influence of the neglected parasitics is significant and considerable accuracy is required. In the recent literature various detailed models have been proposed but in order to fully comprehend and realistically compare the various proposed analytical models for switching losses and even more to choose the appropriate model for the design procedure it is necessary to understand the influence

of the various circuit and component parasitics on the switching transients and, thus, to be fully aware of the implications of the assumptions that each model considers.

The influence of the various parasitics on the switching transients of a Mosfet have been thoroughly studied at [47] and [48]. Here, the conclusions of these studies are summarized and briefly explained. The following figure (figure 3.8) presents the circuit and device parasitics of the converter depicted as lumped elements. The components inside the dashed box correspond to the parasitics in the packaging.

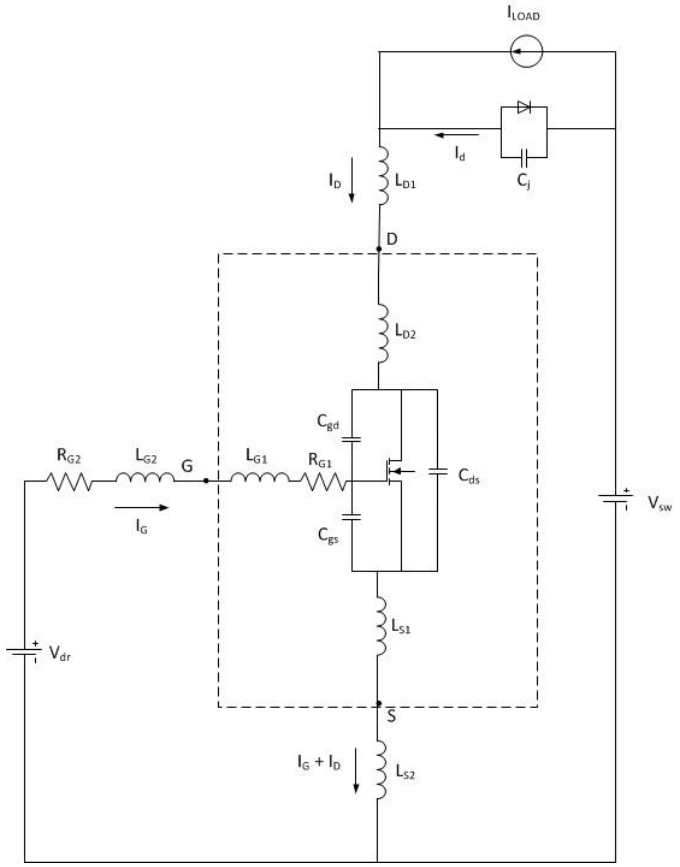


Figure 3.8: Mosfet and circuit parasitics of the converter.

Gate Source Capacitance C_{gs}

The gate-source capacitance, C_{gs}, consists of the junction from the gate to the channel and the capacitance of the dielectric between the gate and the field plate (if it exists) (EPC handbook). C_{gs} is the major part of the so-called input capacitance, C_{iss}, with C_{gd} being the other, usually much smaller, part.

The main influence of C_{gs} is at the on and off delay times because, being the major part of C_{iss}, it determines along with the gate resistance R_g the time constant ($R_g \cdot (C_{gd} + C_{gs}) = R_g \cdot C_{iss}$) of the gate-source voltage rise or fall. The higher the value of the capacitance the bigger the time delay is. This does not have an influence on the switching losses but it certainly affects the driver losses. Equally important is the negative influence on the current slew rate $\frac{di}{dt}$ and, thus, on the corresponding rise and fall times, for the same reason as previously (affects the time constant and thus the rate of change of V_{gs} which, in saturation region, is proportional to the current change). Changing the $\frac{di}{dt}$ has also an impact on the reverse recovery charge, and thus on the current stress, on the V_{ds} drop (turn on) and on the V_{ds} overshoot (turn off).

The input capacitance C_{iss} tends to resonate with the parasitic gate series inductance, L_g, and, as a result, it causes oscillation at the V_{gs} waveform which is not, however, so apparent at the drain current and voltage waveforms. The value of the C_{iss} determines the resonant frequency and amplitude of the resulting oscillation.

Finally, the size relation of the C_{gd} and the C_{gs} parasitic capacitances, or more precisely the ratio of the corresponding charges (Miller ratio $=\frac{Q_{gd}}{Q_{gs}}$), determines the sensitivity of the Mosfet device to $\frac{dv}{dt}$ transients at the drain-source side. The larger is the required gate-source charge compared to the gate-drain charge the more immune is the switch to these transients (i.e the more difficult is for the Mosfet to turn on due to a transient occurring on the drain source side). Therefore, there is an unavoidable trade off between fast switching and transient immunity of the Mosfet related to the size of the C_{gs} parasitic capacitance.

Drain Source Capacitance C_{ds}

The drain source capacitance occurs between the source and the drain parts of the Mosfet, or, in the case of a lateral structure with field place e.g an EPC GaN device, it is formed across the dielectric from the field plate to the drain. C_{ds} is the major part of the output capacitance, C_{oss}, with C_{gd} being the other smaller part and has a non-linear relation with the drain-source voltage.

Since this capacitance is not related with the drive circuit it does not affect the V_{gs} waveform and, therefore, the drain current. On the other hand, since it is the major part of the output capacitance it has a negative but quite small influence on the drain voltage slew rate due to the larger charging and discharging times (for larger capacitance values). The major influence of this capacitance is related to the channel current. Depending on the switching transient C_{oss} either discharges (turn on) or charges (turn off) influencing this way the channel current which is greater or less than the drain current, respectively. This, as it is obvious, has impact on the switching losses since the higher the value of C_{oss} the higher are the turn on and the smaller are the turn off losses.

C_{ds} parasitic capacitance, being the major contributor of C_{oss}, is also strongly related with the parasitic ringing during the turn off transient which occurs because of the resonance of this capacitance with the loop inductance L_d. This ringing could be quite severe for high values of the output capacitance even for moderate switching speeds.

Gate Drain Capacitance C_{gd}

The gate-drain capacitance C_{gd} is also called Miller capacitance because it can be seen as a component placed between the input (gate-source) and output (drain-source) ports of the Mosfet device and, thus, it is related with the Miller effect. The value of this capacitance is strongly dependent on the drain-source voltage and especially at the lower values of it. It is also referred to as C_{rss} and it is part of the input capacitance C_{iss} and output capacitance C_{oss}.

It decisively influences the switching transients of the device and more specifically the V_{ds} slew rate because during the voltage transition the C_{gs} capacitance hardly charges (Miller plateau) and the Miller capacitance is only responsible for the voltage rise or fall. For the same R_g, C_{gs} and operating conditions the higher the value of this capacitance the smaller the slew rate is, i.e the slower the switching transient, and as a result the higher the switching and driver losses. This is because larger C_{gd} capacitances require more charge for the switching. However, a positive consequence of the smaller voltage slew rate is the smaller ringing transient. C_{gd} hardly influences the time constant of V_{gs} (because it is much smaller compared to C_{gs}) and does not affect at all the drain

current but it delays the beginning of its transition either rise or fall (because voltage falls/rises slower). As a result a more expanded Miller plateau is realised.

As already mentioned C_{gd} is also connected with the Miller ratio. Smaller values of this capacitance result to faster switching speed and ensure better immunity to $\frac{dv}{dt}$ transients. Being part of the input and output capacitances it has also a slight influence on the phenomena related to this capacitances which have been described previously.

Gate Drive Loop Inductance L_g

The gate drive loop inductance, $L_g = L_{g1} + L_{g1}$, is formed by the path that the gate current follows. This parasitic component does not have any impact on the switching losses on the Mosfet but it is responsible for the ringing transient at the V_{gs} waveform that occurs due to its resonance with the Mosfet input capacitance, as already stated. This ringing is more severe during turn off. In the case of devices with sensitive gates, like GaN switches where, for example, the maximum driver voltage must be strictly below 6V, the gate loop inductance must be limited in order to eliminate the possibility of voltage overshoots at the gate. For a certain value of gate resistance and C_{gs} capacitance there is an upper limit of this parasitic inductance, or, reversely stated, for a certain value of L_g (defined by the specific design) there will be a minimum source resistance needed to keep V_{gs} in the specific limit. Note that usually (depending on the package) there is some coupling between L_g and L_s parasitics which results to a reduction of the total parasitic inductance.

Power Loop Inductance L_d

Power loop inductance, $L_d = L_{d1} + L_{d2}$, is the parasitic inductance that is formed by the path where the drain current flows. It lumps all the stray inductance along the power loop and the parasitic drain inductance of the Mosfet.

It has a negative influence on the drain current slew rate but its main impact is on the drain-source voltage during the current transition. During the turn on transient the current rise induces a voltage drop across this parasitic inductance and V_{ds} decreases. In low voltage, high speed switching cases this voltage drop might be so significant that the voltage across the switch might be forced to zero, eliminating the turn on losses. On the other hand, during the turn off transient L_d is responsible for the voltage overshoot across the switch, which in cases it might be significant and over-stress the switch while increasing the turn off losses.

Apart from that, L_d is also responsible for the ringing that occurs at the switching waveforms as it resonates with the output capacitance C_{oss} during turn off and with the diode parasitic capacitance, C_j, during turn on. The increase of this value leads to an increase of the amplitude, frequency and settling time of the ringing transient.

Common Source Inductance L_s

Common source inductance, $L_s = L_{s1} + L_{s2}$, is the parasitic inductance that is shared by the gate loop and the power loop inductance which means that both the drain and the gate currents flow though it.

This parasitic works as a negative feedback from the power stage to the gate drive stage. This is because the voltage drop across this element, induced mainly by the change of the drain current, counteracts the change of the gate voltage during the drain current rise or fall (when the Mosfet operates at the saturation region). As a result it influences negatively the drain current slew rate and slows down the switching. The voltage slew rate is not affected and only the transition during the turn on transient is

delayed because of the slower rise of the drain current. It is obvious, therefore, that an increase of this parasitic leads to an increase in the switching losses of the device.

On the other hand, the existence of the CSI tends to suppress the ringing caused by the power loop inductance, since it reduces the $\frac{di}{dt}$ of the drain current. Note, though, that similar to the gate loop inductance, L_s forms with the gate capacitance and the gate resistance an LCR tank (EPC handbook) responsible for a positive voltage ringing across the gate which can turn on the device. Generally, the influence of this parasitic becomes significant at fast switching devices and determines considerably the total losses.

Diode Junction Capacitance C_f

C_f is the parasitic capacitance formed at the junction of the freewheeling diode of the converter.

This parasitic capacitance charges when the diode is turning off (turn on transient of the switch) and discharges when the diode turns on (turn off transient of the switch). Although the stored energy is dissipated all over the circuit, the switching waveforms and, thus the switching losses, are affected by the charging/discharging current of this parasitic. During the turn on of the switch, the charging current of C_f contributes to the current overshoot caused by the reverse recovery current whereas during the turn off the discharging current is opposite to the drain current and therefore a drop at the drain current value occurs. Significant is also the ringing caused by C_f during the turn on transient as it resonates with the power loop inductance, L_d, resulting to oscillation especially at the current waveform. There is no, however, noticeable influence at the ringing during the turn off transient.

3.4.2 Loss Model for the GaN Switching Losses

Every analytical model for the calculation of the Mosfet switching losses that has been developed is dealing with the unavoidable trade offs between accuracy, complexity and speed of calculations. As a result there is neither perfect nor generic model but on the contrary each one has its weaknesses and advantages and certain areas of application. Therefore, in order to use the most appropriate model it is always necessary to consider the specific characteristics of the application and the conditions under which the switching transients occur.

At the previous paragraph it was concluded that the topology that will be used for the implementation of the driver is a buck-boost converter operating at Boundary Conduction Mode (BCM) with Valley Switching (VS). Starting from this at this paragraph the reasons for choosing the specific model are justified and its main advantages and shortcomings are underlined.

Turn on switching transient

Boundary Conduction Mode with Valley Switching means that the turn on of the switch will be realised under zero current conditions (ZCS) and reduced drain voltage, or in specific cases under zero voltage. Zero current switching practically means that during the turn on transient the only losses dissipated on the switch are related to the discharging of the parasitic capacitances. Even more, due to the soft switching of the freewheeling diode there is no reverse recovery current and, hence, no reverse recovery losses. The zero drain current means, also, that there is no influence of the parasitic inductance Ld and the effect of the common source inductance, Ls, is also negligible. Note, however, that although the drain current is zero a small current overshoot will

occur because of the charging current of the parasitic capacitance of the diode. This influence is not taken into consideration here.

Considering the previous and since the influence of the parasitic inductances Ls and Lg is negligible (and Ld does not influence at all) the calculation of the losses during this transient could be likely done by using the simple formula

$$E_{on} = 0.5 \cdot (C_{ds} + C_{gd}) \cdot V_{sw}^2 \tag{3.7}$$

which describes the stored energy in the parasitic capacitances that is dissipated on the switch. The values of the capacitances correspond to their *mean* values across the voltage operating range (from $I_o \cdot R_{ds,on}$ to V_{sw}).

Some inaccuracy is expected when calculating turn on losses using (3.7) for two reasons: The first is that the current overshoot because of the charging current of the diode's capacitance is neglected and the second is the fact that C_{oss} changes while discharging which means that (3.7) is not totally correct since it assumes constant capacitance.

Turn off switching transient

Unlike the turn on, during the turn off transient the switching could be either hard or soft depending on the influence of the Coss on the channel current and the drain-source voltage rise. Therefore, an accurate model should include the effect of two basic parameters : the C_{oss} capacitance and the Ls and Ld parasitic inductances so that both the channel current and the voltage overshoot can be determined. The latter is additionally important because it is required for the calculation of the ringing losses that follow the voltage overshoot. These losses, however, are not dissipated on the switch but on the stray resistance of the circuit.

Various loss models have been proposed in the literature for the switching of Mosfet devices with the classical piecewise linear model being the simplest and most common but also less accurate since it does not incorporate the influence of the parasitic inductances, the channel current and the voltage dependent device parasitic capacitances. A more accurate modification of the classical model was presented by Wang et al. where the influence of the channel current is considered on the switching times and losses. Still, though, it lacks accuracy since it does not incorporate parasitic inductances, which in low voltage and high speed switching can be significant. On 2006 Ren presented a model [44] where the parasitic inductances are incorporated in the current and voltage algebraic equations as well as the voltage dependent capacitances. For the derivation of the algebraic equation, however, the drain current was assumed to be equal with the channel current neglecting this way the influence of the C_{oss} capacitance on the waveforms. On the other hand, the models presented by M.Rodriguez **??** and Jianjing Wang [48] are dealing with this problem as they both handle these two values separately while considering also the influence of the parasitic inductances. Both models, however, neglect the voltage dependency of the parasitic capacitances and use linear approximations.

From the previously presented models, the ones proposed by Rodriguez et al. and Jianjing Wang et al. include the influence of the most important parasitics and combine simplicity and accuracy at a very sufficient level for analytical models. For that reason, the final used model derives from the combination of these two in such a way that their main advantages can be exploited while their weak points can be surpassed. Here, the loss model that is used for the turn off switching of the GaN device is thoroughly discussed. The analytical equations that describe the channel current and drain voltage waveforms, which can be used for the calculation of the turn off switching losses, are

presented along with the main assumptions that were considered. Based on this analysis, the ringing losses and the driver losses related to this transient can also be calculated.

The switching transition can be divided into four discrete stages: the turn-off delay time (stage 1) and the voltage rise time (stage 2) are based on the model presented from Jianjing et al. [48] while the two stages describing the current fall (stage 3 and 4) are based on the approach presented by Rodriguez et al [49]. At the end of the transient, the voltage and current oscillations follow. Note that the ringing transient does not cause power dissipation on the switch but on the stray resistance.

Stage 1 : Turn Off Delay Time

The switch is operating at the ohmic region and the gate driver applies zero voltage across the gate and source electrodes through a gate resistance R_g. Because the rate of change and the value of the gate current compared to the load current is small it is assumed that the influence of L_g and L_s is minor and can be neglected. As a result the equivalent circuit is an RC circuit and the input capacitance discharges with a time constant $\tau_{off} = R_g \cdot C_{iss}$ with $C_{iss} = C_{gs} + C_{gd}$. The gate-source voltage is given by:

$$u_{gs}(t) = V_{dr} \cdot e^{-t/\tau_{off}} \tag{3.8}$$

Since the switch is in the ohmic region the channel current is not influenced by the change of V_{gs}.

This stage ends when $u_{gs}(t) = V_{th} + I_o/gfs$ which is the initial value of the Miller plateau voltage. Normally, the switch does not get into the saturation region until $u_{ds} > u_{gs} - V_{th}$ and the drain-source voltage increases with a slew rate of i_g/C_{gd} until this condition is accomplished. However, because $u_{gs} - V_{th} = Io/gfs$ is very small, especially for this application where Io =1.2A and gfs = 34, this period is neglected and the switch is considered to enter saturation region at the next stage.

Capacitance Values : Because during this stage $V_{ds} = I_{on} \cdot R_{ds,on}$ and it is constant the value of C_{iss} equals the capacitance that corresponds to this voltage (approximately the maximum capacitance value).

Stage 2 : Voltage Rise Time

During this period the output capacitance of the switch, $C_{oss} = C_{gd}+C_{ds}$, is charging up and the drain-source and gate-drain voltages increase. Because of that, the channel current which was initially equal to the load current is now reduced by a portion equal to the charging current of the output parasitic capacitance (C_{oss}) and the discharging current of the parasitic capacitance of the diode (C_f). Because of the $\frac{du_{ds}}{dt}$, the parasitic capacitance of the freewheeling diode C_f, which will turn on when $V_{ds} = V_{sw}$, is discharging and the corresponding current opposes the drain current resulting to a drop of it. Since the switch has entered the saturation region the channel current of the Mosfet is related to V_{gs} by:

$$I_{chan} = gfs \cdot (V_{gs} - V_{th}) \tag{3.9}$$

Because the change of gate-source voltage is small compared to the gate-drain voltage rise, even if the channel current changes considerably, it can be accurately said that $\frac{du_{ds}}{dt} = \frac{du_{gd}}{dt}$.

Both of the output parasitic capacitances influence the slew rate and the channel current of the Mosfet. C_{gd}, as expected by the Miller effect, influences drastically the drain source voltage slew rate and the effect of this is a change on the channel current.

C_{ds}, on the other hand, because of its size has a direct influence on the channel current and the result of this is a different V_{gs} which leads to different charging current of the C_{gd}. Thus, it affects du/dt but less significantly compared to C_{gd}.

This means actually that there is a certain operating point for the Mosfet which can be found by the cross section of the straight lines described from the following equations:

$$\frac{du_{ds}}{dt} = \frac{I_o - I_{chan}}{C_{oss} + C_f} \tag{3.10}$$

$$\frac{du_{ds}}{dt} = \frac{V_{th} + I_{chan}/gfs}{R_g \cdot C_{gd}} \tag{3.11}$$

These equation can be easier realised by the following figure.

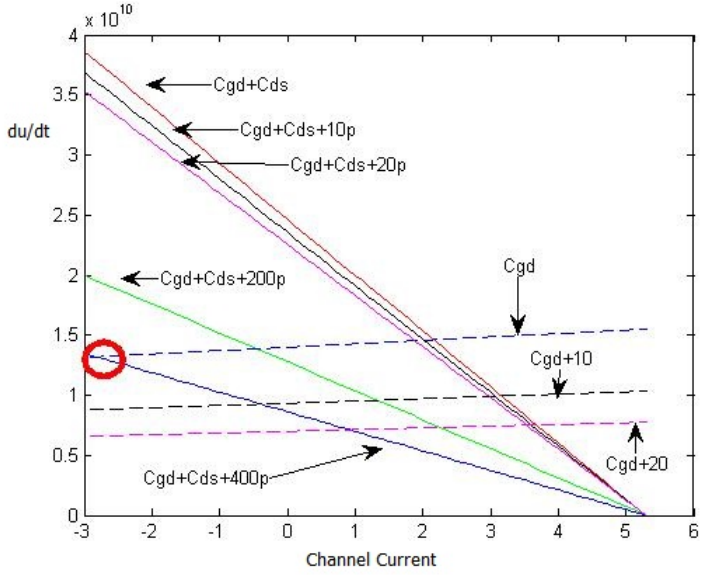


Figure 3.9: The operating point based on the previous equations. Note that $C_{gd} = 20pF$ and $C_{ds} = 200pF$.

From the figure it is clear that the influence of the change of C_{ds} is more intense on the channel current whereas C_{gd} influences mainly the voltage rate of rise.

Also, it is obvious that the previous operating point can be likely at the negative side - see red circle- situation that might occur at fast switching transients or switches with high C_{ds} values. Of course, negative channel current is not realistic. In this case the channel current actually decays to zero and all the load current is charging the capacitances resulting to zero losses on the switch. Because the charges at the inversion layer (the channel current) decrease below the threshold voltage the C_{gs} capacitance also discharges (this capacitance is formed by the charges on the metal electrode of the gate and the charges on the channel current) and V_{gs} keeps falling. During this time the current that discharges the C_{gs}, i_{gs}, is comparable to i_{gd}. However, when V_{gs} approaches its final value, this current can be assumed negligible and the final value of the V_{gs} can be easily found as $V_{gs} = R_g \cdot C_{gd} \cdot I_o / C_{oss}$.

All in all, at this stage from equations (3.10) and (3.11) the operating point $(\frac{du_{ds}}{dt}, I_{chan})$ can be found. The drain and the channel current will be given by:

$$I_{chan} = I_o - \frac{(C_f + C_{oss}) \cdot (I_o + gfs \cdot V_{th})}{gfs \cdot R_g \cdot C_{gd} + (C_f + C_{oss})} \tag{3.12}$$

if $I_{chan} > 0$ then

$$i_{chan}(t) = I_{chan} \tag{3.13}$$

$$u_{gs}(t) = V_{Miller} = \frac{I_{chan}}{gfs} + V_{th} \tag{3.14}$$

$$\frac{du_{ds}}{dt} = \frac{\frac{I_{chan}}{gfs} + V_{th}}{R_g \cdot C_{gd}} \tag{3.15}$$

if $I_{chan} \leq 0$ then

$$i_{chan}(t) = 0 \tag{3.16}$$

$$u_{gs}(t) = R_g \cdot C_{gd} \cdot I_o/(C_{oss} + C_f) \tag{3.17}$$

$$\frac{du_{ds}}{dt} = \frac{I_o}{C_{oss} + C_f} \tag{3.18}$$

For both cases the drain current is constant and equal to :

$$i_d(t) = I_d = I_o - \frac{C_f \cdot (I_o + gfs \cdot V_{th})}{gfs \cdot R_g \cdot C_{gd} + (C_f + C_{oss})} \tag{3.19}$$

This stage ends when the drain-source voltage reaches the operating V_{sw} value and the freewheeling diode becomes forward biased. If the channel current is zero then there are no losses on the switch and this stage is only related with driver losses.

Capacitance Values : Normally the parasitic capacitances during this stage change, because V_{ds} changes, and this affects the rate of the voltage rise and consequently the channel current. In this model, however, capacitances during this stage are considered constant. Because of the nonlinearity of their characteristics their value was decided to be the mean value across the operating voltage range. For that a function that describes the C-V curve would be useful. Based on the datasheets and using interpolation in Matlab software the capacitance curves can be approximated and the mean value can be calculated.

Stage 3 : Current Fall Time I

During this stage the load current commutates from the switch to the diode. The negative current slew rate leads to a voltage overshoot because of the parasitic inductances Ld and Ls. The current that charges the output parasitic capacitances to the overshoot value is the difference $i_d(t) - I_{chan}$. This holds even if the channel current is zero. Of course in this case there are no losses on the switch but this stage is useful for the driver losses (losses on Rg) and the voltage stress on the switch (voltage overshoot).

The analysis of this and the following stage is based on the model proposed by Rodirguez et al. [49] and it assumes that during this stage the gate-source voltage, and hence the channel current, remain constant. Actually, this does not hold totally because the voltage overshoot of the common source inductance, especially at high values of $\frac{di}{dt}$ and L_s, increases the V_{gs} voltage which in return results to a channel current overshoot. Because of that the current fall time increases but also the peak value $V_{ds,pk}$ is smaller since $i_d(t) - I_{chan}$ (charging current) becomes smaller. However, if a reasonably optimized design is assumed, where CSI is minimized, then this effect is not so significant and the assumption can hold.

At this stage the equivalent circuit is shown at figure 3.10 and it is an LC circuit. The initial values of each component are $i_d(0) = I_{ds}$, $i_s(0) = I_{ds}$, $i_{chan}(0) = I_{chan,2}$, $u_{ds}(0) = V_{sw}$ and $u_{dg}(0) = V_{sw} - V_{gs}$.

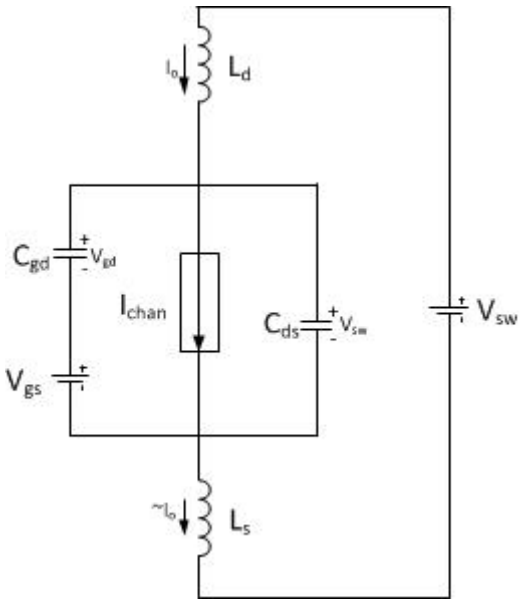


Figure 3.10: Equivalent circuit of the topology at stage 3 when the current commutated from switch to diode.

The solution of this circuit gives the following equations that describe the drain-source voltage and current behaviour.

$$u_{ds}(t) = V_{sw} + (I_d - I_{chan}) \cdot (L_d + L_s) \cdot \omega_0 \cdot sin(\omega_0 \cdot t) \tag{3.20}$$

$$i_d(t) = I_{ds} - (I_d - I_{ch}) \cdot (1 - cos(\omega_0 \cdot t)) \tag{3.21}$$

where

$$\omega_0 = \frac{1}{\sqrt{(L_s + L_d) \cdot (C_{gd} + C_{ds})}}$$

and I_{ch} is the final value of the channel current of the previous stage.

This stage ends when the drain current becomes equal to the channel current. Because now there is no current to charge the capacitances the voltage reaches its maximum value $V_{ds,pk}$.

Capacitance Values : During this stage the values of the parasitic capacitances equal the value that corresponds to maximum operating voltage, which is V_{sw}.

Stage 4 : Current Fall Time II (if $I_{chan} > 0$)

At this stage the drain and the channel current, which are assumed equal, continue to fall. Since there is no current to charge the capacitances the drain voltage does not increase but, on the contrary, it is assumed approximately constant. In this case the channel(or drain) current is decreasing because of the applied voltage difference $V_{sw,pk} - V_{sw}$ across the inductances $L_s + L_d$. Therefore, it is decreasing linearly. The equivalent circuit is similar to fig. 3.10 but with the capacitance voltage constant and the drain/channel current variable. Since the switch is still in the saturation region the gate-source voltage follows the channel current and it decreases until it reaches threshold voltage V_{th}. Exactly because of that (saturation region), however, the channel current cannot fall faster than the C_{gs} capacitance can discharge. Usually the time constant $\tau_g = R_g \cdot C_{gs}$ is very small but when L_s and L_d are also very small (or they are set to

zero if it is required) then this restriction applies. In the case at which the time constant is larger than the time predicted by the linear decrease then the channel current follows the fall of V_{gs} which is exponential (RC circuit).

It makes sense that this stage has a meaning if the channel current is not zero. In case of zero I_{chan}, V_{gs} is falling exponentially to zero and its stored energy is dissipated on the gate resistance R_g (part of the driver losses).

The main assumption of this stage is that $V_{ds,pk}$ is constant during the falling period. In most cases it falls but slightly. This cannot hold accurately especially at higher values of the common source inductance (or faster switching e.g. lower Rg) because at this case the channel current overshoot can be significant and it can surpass considerably the drain current value and at an early stage, discharging this way the capacitances quite fast. This means that using this assumption the model slightly overestimates the losses at this stage but this is not negative since at the previous stage the losses were slightly underestimated since the channel current overshoot was not considered.

As a result of these, the following equations describe the transient at this stage.

Linear Fall Time: $t_{lin} = \frac{I_{chan}}{(V_{ds,pk}-V_{sw})/(L_s+L_d)}$

Gate Time Constant : $\tau_{RC} = R_g \cdot C_{gs}$

Exponential Fall Time: $t_{exp} = R_g \cdot C_{gs} \cdot ln(\frac{V_{th}}{V_{plt}})$

if $t_{lin} < t_{exp}$ (common case)

$$u_{ds}(t) = V_{ds,pk} \tag{3.22}$$

$$i_d(t) = i_{chan}(t) = I_{chan} - \frac{V_{ds,pk} - V_{sw}}{L_s + L_d} \cdot t \tag{3.23}$$

$$u_{gs}(t) = \frac{i_{chan}(t)}{gfs} + V_{th} \tag{3.24}$$

if $t_{lin} < t_{exp}$ or if $L_d = L_s = 0$

$$u_{ds}(t) = V_{ds,pk} \tag{3.25}$$

$$u_{gs}(t) = V_{Miller} \cdot e^{-t/\tau_{RC}} \tag{3.26}$$

$$i_d(t) = i_{chan}(t) = gfs \cdot (u_{gs}(t) - V_{th}) \tag{3.27}$$

$$\tag{3.28}$$

This stage ends when the current becomes equal to zero and therefor V_{gs} equals to the threshold value.

Capacitance Values : During this stage the values of the parasitic capacitances equal the value that corresponds to maximum operating voltage, which is V_{sw}.

Stage 5 : Drain voltage and current oscillations.

When the drain current reaches zero, drain voltage has, according to previous analysis, its maximum value (or in reality a value above its steady stage V_{sw} and below its peak V_{pk} as previously explained). In any case a ringing transient occurs with initial values $u_{ds}(t = 0) = V_{ds,pk}$ and $i_d(t = 0) = I_{ds}$. The turn off ringing occurs because of the resonance of the output capacitance of the switch, Coss, and the power loop (Ld) and common source (Ls) parasitic inductances. The dumping of this oscillation comes from the stray resistance of the circuit. It should be underlined that during the oscillation the power is dissipated on this stray resistance and not on the switch.

The lumped parasitic elements Coss and Ld+Ls) are in series and so they form an RLC series resonant circuit, which in the case of a buck boost converter is as shown at figure 3.11.

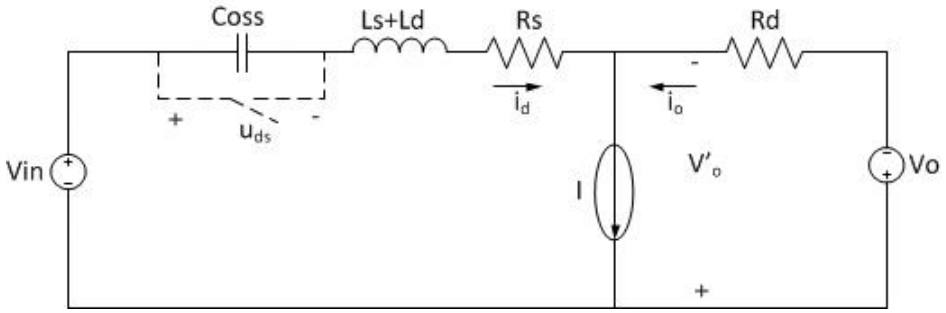


Figure 3.11: Buck-boost converter equivalent circuit during turn off ringing.

When solving the differential equation, the drain and voltage expressions are:

$$u_{ds}(t) = c_1 \cdot e^{at} \cdot cos(\beta t) + c_2 \cdot e^{at} \cdot sin(\beta t) + V_{sw} \tag{3.29}$$

$$i_d(t) = C_{oss} \cdot \frac{du_ds}{dt} = C_{oss} \cdot \gamma \cdot e^{at} \cdot sin(\beta t) \tag{3.30}$$

where

$$c_1 = V_{pk} - V_{sw}$$
$$c_2 = -\frac{\alpha}{\beta} \cdot c_1$$

and

$$\alpha = -\frac{R_s + R_d}{2(L_s + L_d)}$$
$$\beta = \frac{\sqrt{4(L_s + L_d)C_{oss} - ((R_s + R_d)C_{oss})^2}}{2(L_s + L_d)C_{oss}}$$
$$\gamma = c_2 \cdot \alpha - c_1 \cdot \beta = -\frac{\alpha^2 + \beta^2}{\beta} \cdot c_1$$

For the calculation of the total losses that are dissipated on the stray resistance ,R_s of the circuit the energy balance needs to be considered. So:

- Initial Stored Energy at Resonant Tank: $E_{st,init} = 0.5 \cdot C_{oss} \cdot V_{pk}^2$
- Final Stored Energy at Resonant Tank: $E_{st,fin} = 0.5 \cdot C_{oss} \cdot V_{sw}^2$
- Energy from Source: $E_{source} = -V_{in} \cdot C_{oss} \cdot (V_{pk} - V_{sw})$
- Energy to Load: $E_{load} = Vo \cdot C_{oss} \cdot (V_{pk} - V_{sw})$

The total losses on the stray resistance R_s and the diode resistance are :

$$E_{Loss} = (E_{st,init} - E_{st,fin}) + (E_{source} - E_{load}) \Rightarrow$$
$$E_{Loss} = 0.5 \cdot C_{oss} \cdot (V_{pk}^2 - V_{sw}^2) - C_{oss} \cdot V_{sw} \cdot (V_{pk} - V_{sw}) \quad (3.31)$$

Where the term that corresponds to the energy provided to the load from the inductor (which is not related to the oscillation) is, of course, not considered.

Note : In case the channel current is zero, because of the zero losses on the switch, the oscillation could be realised as starting from stage 3 with initial values $u_{ds}(t = 0) = V_{sw}$ and $i_d(t = 0) = I_{ds}$. When the transient ends it is $u_{ds}(t = \infty) = V_{sw}$ and $i_d(t = \infty) = 0$ which means that it is the stored magnetic energy at the parasitics L_s and L_d that is dissipated on the circuit. As a result in this case

$$E_{Loss} = 0.5 \cdot (L_s + L_d) \cdot I_d^2 \quad (3.32)$$

Capacitance Values: For this stage the capacitance values are equal to the values that correspond to the operating voltage V_{sw} (similar to stages 3 and 4).

The following plot (figure 3.12) shows the current and voltage waveforms during the turn off transient based on the presented equations.

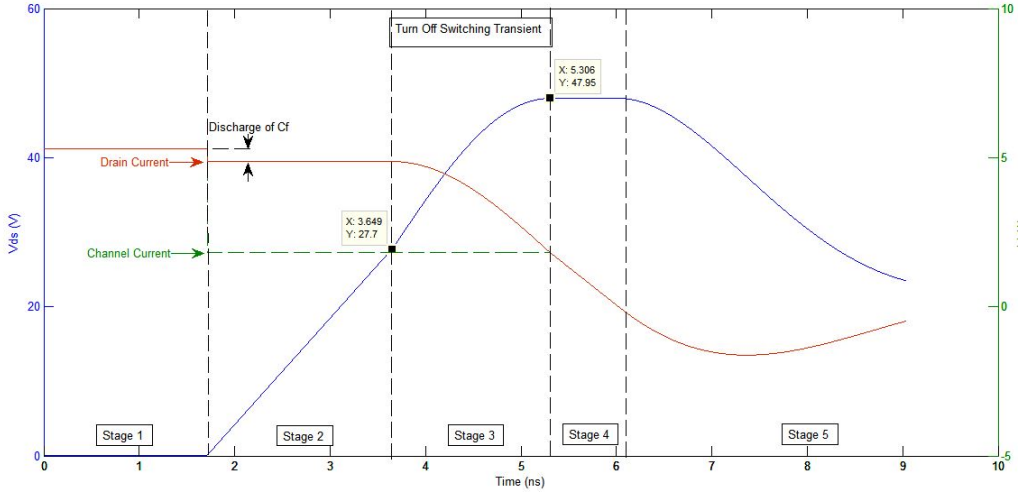


Figure 3.12: Current and voltage waveforms based on the equations of the presented model.

At the following table (table 3.6) the equations related to the turn off transient and used by this model are presented.

Turn Off Transient Loss Model Equations

Stage	*Equations*	*Capacitance Value*
I	$u_{gs}(t) = V_{dr} \cdot e^{-t/(R_g \cdot C_{iss})}$ $i_d(t) = i_{chan}(t) = I_{sw}$ $u_{ds}(t) = V_{sw}$	$C_{iss} = C_{iss}(V_{ds} = I_o R_{ds,on})$
Stage I ends when $u_{gs}(t) = V_{Miller} = \frac{I_{sw}}{gfs} + V_{th}$		
II	$I_{chan} = I_{sw} - \frac{(C_f + C_{oss}) \cdot (I_{sw} + gfs \cdot V_{th})}{gfs \cdot R_g \cdot C_{gd} + (C_f + C_{oss})}$ $I_d = I_{sw} \cdot \frac{C_{oss}}{C_{oss} + C_f}$ Case A : $I_{chan} > 0$ $i_{chan}(t) = I_{chan}$ $u_{gs}(t) = \frac{I_{chan}}{gfs} + V_{th}$ $\frac{du_{ds}}{dt} = \frac{\frac{I_{chan}}{gfs} + V_{th}}{R_g \cdot C_{gd}}$ Case B: $I_{chan} <= 0$ $i_{chan}(t) = 0$ $u_{gs}(t) = \frac{R_g \cdot C_{gd} \cdot I_d}{(C_{oss} + C_f)}$ $\frac{du_{ds}}{dt} = \frac{I_d}{C_{oss} + C_f}$	$C_{oss} = mean(C_{oss})$ for V_{ds} operating range
Stage II ends when $u_{ds}(t) = V_{sw}$		
III	$u_{ds}(t) = V_{sw} + (I_d - I_{chan}) \cdot (L_d + L_s) \cdot \omega_0 \cdot sin(\omega_0 \cdot t)$ $i_d(t) = I_d - (I_d - I_{chan}) \cdot (1 - cos(\omega_0 \cdot t))$ $i_{chan}(t) = I_{chan,II} = const$ $u_{gs}(t) = V_{gs,II} = const$	$C_{oss} = C_{oss}(V_{ds} = V_{sw})$
Stage III ends when $i_d(t) = I_{chan}$		
IV (if $I_{chan} > 0$)	$u_{ds}(t) = V_{ds,pk} = const$ $t_{lin} = \frac{I_{chan}}{(V_{ds,pk} - V_{sw})/(L_s + L_d)}$ $t_{exp} = -R_g \cdot C_{gs} \cdot ln(\frac{V_{th}}{V_{plt}})$ Case A : $t_{lin} > t_{exp}$ $i_{chan}(t) = i_d(t) = I_{chan} - \frac{V_{ds,pk} - V_{sw}}{L_s + L_d} \cdot t$ $u_{gs}(t) = \frac{i_{chan}(t)}{gfs} + V_{th}$ Case B : $t_{lin} < t_{exp}$ or $L_s = L_d = 0$ $i_{chan}(t) = i_d(t) = gfs \cdot (u_{gs}(t) - V_{th})$ $u_{gs}(t) = V_{gs,II} \cdot e^{-t/(R_g \cdot C_{gs})}$	$C_{oss} = C_{oss}(V_{ds} = V_{sw})$
Stage IV ends when $i_d(t) = 0$		

Table 3.6: Equations of the Turn Off Transient of the Used Loss Model.

Using the previous equations the waveforms of the drain and channel current, as well as the gate-source and drain-source voltage, can be represented. More importantly, though, the losses related to the turn off transient can be easily calculated.

Advantages and Limitations of the Used Model

An important advantage of the used model is the simplicity of the equations that describe the transient. Most of the presented equations, with the exception of stage 3, are linear and therefore the calculation of the energy losses is fast and straightforward. Even more, the combination of the two models is expected to give better accuracy than each model separately would give and certainly better accuracy than the classical model.

The considered assumptions of each stage might simplify the results but, in the same time, they constitute the limitations of the model. Especially, the non-linearity of the parasitic capacitances at stage 2 and the channel current overshoot at stage 3 are expected to introduce some inaccuracies at the loss calculations. Another source of inaccuracies is the fact that it is difficult to include and estimate the exact values of the various parasitics that influence the transients (it requires dedicated software for that). Despite these limitations, the calculated losses are expected to give a close approximation of the actual switching losses which is very important for the thermal design.

3.5 Design of the Inductor Component

As it has already been mentioned, the size of the passive components and especially of the inductor is a crucial aspect for this project. For that reason two different coil geometries were used, one planar and one discrete, and their influence on the converter's efficiency and size was investigated. Clearly, a planar inductor is much more preferable when making a low profile flexible converter, however the area that is required is significantly bigger compared to a discrete component, due to the small inductance values that can be achieved, and also the dc and ac resistances are significantly bigger. On the other hand, a discrete inductor, although thicker, can achieve higher inductance values with lower losses. Their influence on the converter will be examined at the next chapter.

At this paragraph, the two different topologies for the inductor component will be presented and discussed.

3.5.1 The Planar Inductor

The geometry of the planar inductor was chosen to be a circle, as it is shown at the following schematic.

The value of the diameter depends on the angle it is defined. As can be seen from fig. 3.13 if the diameter is defined at the x-axis it is larger compared to the one defined at the y-axis. This is because of the spiral geometry of the coil. The shown corresponds to the larger one (x-axis) and it is equal to:

$$d_o = 2 \cdot r_{in} + (2N + 1) \cdot w_c + (2N - 1) \cdot s$$

As it can be realised, each half turn has different radius, and this needs to be considered for the calculation of the length of the conductor. The radius of each half turn for the first two turns is:

1st half : $r_1 = r_{in} + \frac{w}{2}$

2nd half : $r_2 = (r_{in} + \frac{w}{2}) + (\frac{w}{2} + \frac{s}{2})$

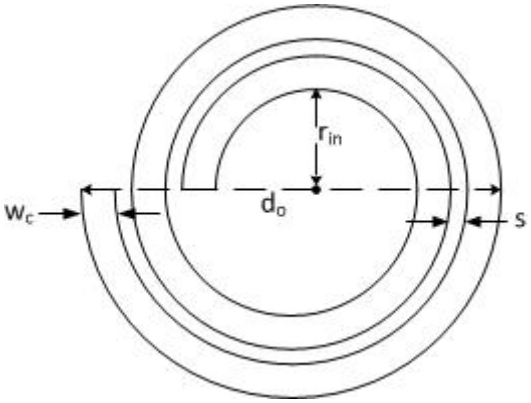


Figure 3.13: Spiral planar inductor.

3rd half : $r_3 = (r_{in} + \frac{w}{2}) + 2 \cdot (\frac{w}{2} + \frac{s}{2})$
4th half : $r_3 = (r_{in} + \frac{w}{2}) + 3 \cdot (\frac{w}{2} + \frac{s}{2})$
It is obvious that each half turn is longer by $\frac{w}{2} + \frac{s}{2}$ to the previous one. The total length for a spiral coil of N turns is then:

$$l_c = \pi \cdot [2N \cdot (r_{in} + \frac{w}{2}) + N(2N-1) \cdot (\frac{w}{2} + \frac{s}{2})]$$

For an air-core planar inductor the inductance value can be easily calculated using the following formula [[50]]:

$$L_{cir} = \frac{\mu_0 N^2 d_{avg}}{2}(log(2.46/r) + 0.2r^2)$$

where $d_{avg} = \frac{do+di}{2}$ and $r = (do - di)/(do + di)$.

The size of the coil, for a certain value of inductance, depends on the inside diameter, the width of the conductors, the width of the spacing and the number of turns. This means that the geometry of the coil can be optimized.

In general, for certain conductor and spacing width, the outer turns have bigger influence on the inductance value compared to the inside turns. However, they result to longer traces and thus higher ohmic resistance.

When decreasing the width of the conductor alone, the inductance value increases and the size of the coil decreases. In the same time, however, both dc and ac resistance increases and the quality factor decreases. This is not the case if the thickness of the conductor increases simultaneously because it leads to constant dc resistance. The ac resistance, however, still increases. In that case the dc quality factor increases but the ac is not influenced.

Although a size optimization of an aircore inductor is easy, when a core is added things become more complicated since there is no more an analytical way to calculate the inductance value. Because a significant amount of flux does not flow through the core the inductance does not improve significantly and also different geometries which might lead to the same inductance with an air core might lead to significantly different value when a core is added. This is obvious at the results that are presented at table 3.9.

For this application it is important that the size of the coil is as small as possible. This is, of course, related to the required inductance value but also to the values of the

aforementioned design parameters. A complete optimization procedure would require a parametric sweep of all the geometric values but for reasons of simplicity, time and computing resources saving and material availability the values of most of them are pre defined and fixed. At table 3.7 the values of the defined sizes are presented:

Fixed Size Coil Values	
Thickness of Conductor, t_c	70 um
Spacing between Conductors, s	0.5 mm
Thickness of Core Material, t_d	0.5 mm

Table 3.7: Fixed coil values used at the Comsol simulation.

Note that the spacing between the conductors was chosen as such quite arbitrarily. It was necessary to be as small as possible and since there was no actual insulation limit because of the low voltage between two adjacent turns the restrictions were imposed mainly by the manufacturing process. It should be mentioned here that the coil was made manually and at the time it was built the process was not very familiar and its limits and possibilities were not quite clear. The fact is that this value could be further decreased at least to 0.2mm resulting to slightly smaller diameter of the coil and, therefore, slightly smaller copper and core losses. However, because of time restrictions a new coil was not made and the project was based on that.

Using the Finite Element Method software Comsol, the inductances for different geometric values and core materials were estimated. At the table 3.8 shows the range of the variable parameters for which the different inductances were calculated.

Variable Coil Values	
Width of Conductor, w_c	4mm and 5mm
Internal Radius, r_{in}	1..15 mm
Number of Turns, N	2..5
Permeability of Material, u_r	40 and 110

Table 3.8: Variable coil values used at the Comsol simulation.

The availability of the flexible core materials in the laboratory determined the range of the magnetic permeability. The two available flexible core materials were the TDK IRJ04, with a permeability of around 40, and the 3M AB7050 EMI Absorber, with a permeability of around 110. As regards the rest of the parameters their maximum values were limited by the maximum size (outer diameter) of the coil. Using the FEM software the AC resistance of the inductor coil for the maximum and minimum frequency (corresponding to minimum and maximum output current respectively) were also calculated and used for the loss estimation of the component.

The inductance values that were simulated in the finite element software range from 0.12uH to 6.95uH and they were in total 242 components. At the following table some of the calculated values are indicatively shown.

Simulated Coil Values

$w_c(mm)$	$r_{in}(mm)$	$Turns$	μ	$L_{air}(uH)$	$L(uH)$	$R_{dc}(mOhm)$	$R_{ac}(mOhm)@f$
5	6	3	40	0.45	0.73	14.1	82@1.91MHz
5	6	3	110	0.45	1.49	14.1	146@833kHz
5	5	5	40	1.68	1.88	30.3	124@785kHz
4	11	3	110	1.03	2.42	21.3	123@621kHz
4	10	5	40	1.67	2.67	42.2	118@563kHz
5	9	4	110	1.03	3.20	25.8	157@473kHz

Table 3.9: Results of the Comsol simulations for some geometries.

At table 3.9 we can see what was previously commented. The core materials do not increase significantly the inductance values of the coils. Specifically the TDK material increases the value not less than 1 time while the 3M material approximately for 3 times. This values are quite small. Even more, we can see from the last two values that although the coils have the same inductance value for as aircores, when using the 3M material they result to different inductance values because of their different geometries. It should be noted here, that the main source of losses of the planar inductor is the dc and ac losses (skin and proximity effect) of the copper. From the simulations this was easily observable when plotting the current distribution in the conductors. The core losses are negligible because, as already mentioned, only a small percent of the magnetic flux passes through the core material.

3.5.2 The Discrete Inductor

The theory regarding the design of a discrete magnetic component is well established and can be found at a wide range of literature. At this project, for the design of the coil the simple method of the equivalent magnetic circuit was used to calculate the air gap and number of turns for the operating range of the application.

For the discrete inductor a 3F4 core at E-shape and I-shape of Ferroxcube was used. 3F4 is a high frequency ferrite used in power and general purpose transformers at frequencies 1-2 MHz. The magnetic permeability of this material is around 900 for room temperature and up to 1MHz operation. The field saturates at the value of 300mT for room temperature but this value falls slightly to 280mT for 100oC.

At figure 3.14 the dimensions and size of the E-shaped core are shown.

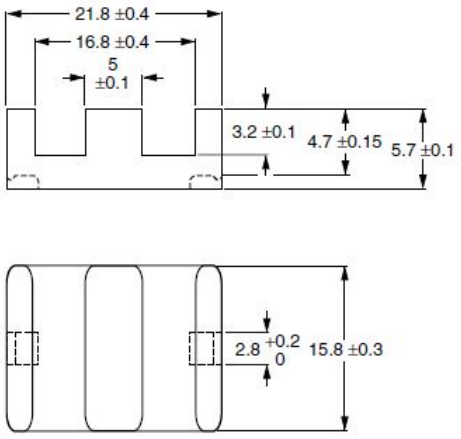


Figure 3.14: Shape & Size (in mm) of the E-shape core (E22/6/16/R).

In order to deal with the skin effect on the copper a Litz wire was used. Because of

the relatively small rms current of the inductor the used Litz wire was thin. In addition to that because of the small number of turns only one layer was used and thus the proximity effect and the parasitic capacitance are also small. Consider that the main source of losses on the discrete inductor is the core losses as opposed to the planar inductor at which it is mainly the copper losses. For the calculation of the core losses of this coil the figures from the datasheet of the core material were used.

3.6 Choosing the Inductance Value

The value of the magnetic component is crucial for this specific topology and operating mode as it is directly related to the operating frequency range. These two values impose an important trade off as regards the design of the converter. The higher is the operating frequency the smaller is the inductance value (which is strongly related to the size of the coil) and vice versa. However, high frequency results to higher switching, core and copper losses which lead also to higher operating temperatures. Since both the inductance value and the frequency are up to this point unspecified, one of them should serve as the independent parameter (the parameter that sweeps at a range of values and for each case will define the value of the other and the analytical equations will be based on that). In this project, this parameter was chosen to be the inductance value clearly for practical (simulation) reasons. For the specification of the inductance value of the planar coil, which was investigated first, a finite element tool is required due to this specific configuration. It was,therefore, considered easier to specify an amount of geometries for the coil, which would result to a wide range of inductance values, and for each case to calculate the frequency and the analytical equations.

3.6.1 Specifying the Component Properties

For the selection of the inductance value the analytical model of the converter will be used. In order to do so, however, the parameters of the components need to be known so that the equations can be solved. The switching components, which are the switch and the diode, were selected according to the basic electrical specifications of the converter and their parameters were taken from the datasheets. The planar coil parameters were specified using the Comsol software and the capacitance values were calculated using the standard equations so that the ripple will be less than 10% . The required data for the components, except for the capacitors, include their electrical and thermal characteristics. The former are important in order to calculate the electrical values of the voltages and currents at the specific operating point and, thus, for the calculation of the losses on the components. The later are required so that the temperature on the components can be calculated. At the following paragraphs firstly the components that were selected are presented, then the analytical model will be discussed and in the end the reasons for selecting the specific inductance value will be explained.

The Coil

The base of the procedure is the initial criterion that the coil that will be used is preferred to be low-profile and flexible so that it can be similar to an OLED as regards its geometry. Towards that direction, as it was presented at the previous paragraph, a bank of various geometries of planar inductors was created using the tool of Finite Elements, Comsol, and sweeping for various variables while keeping some other constant (see tables 3.9, 3.7, 3.8). With this tool the inductance value was estimated as well as the ac resistance of the coil for two frequencies, one corresponding to $I_o = 1A, V_o = 14.5V$ and the other to $I_o = 1.2A, V_o = 14.5V$ which is smaller. For the the rest of the frequencies, close to these

values, the ac resistance is calculated by linear extrapolation. Note that the core losses could not be estimated due to inadequate information for both materials. However, as already explained, they are not expected to be significant, due to the small amount of magnetic flux passing through the core. The bank of the inductor values includes all the necessary information for the coil that can be used at the analytical calculations for the electrical values and losses.

After calculating these values at the specific operating point the resulting voltages and currents are used in combination with the finite element tool and the thermal model of the coil in order to calculate the temperature on the surface of the component. It should be noted here that the maximum operating temperature of the magnetic materials used is 85^oC which means that as regards the thermal aspects they are inappropriate for this application. However, since only these materials were available for this application they had to be used.

The Switching Component

The switching component was chosen based on the electrical requirements of the driver, the results of the first order calculations and between the available GaN options. The selected component is the EPC2014 40V, 10A. From the discussion on the analytical model for the calculation of the switching losses it is clear that there are various parameters that are required for this model. Almost all of them are included in the component datasheet. These are for example, the on resistance, the input and output capacitance, the threshold voltage and so on. However, what is not known but is required for the model are the parasitic inductances of the circuit, which are the loop inductance, the common source inductance and the gate drive loop inductance.

The values of the parasitic inductances are mainly dependent on the circuit layout considering the fact that the packaging of this component, the LGA - Land Grid Array, minimizes the packaging related parasitic inductances. Since the parasitic inductances are layout dependent it is obvious that special care should be given in minimizing these three loops.In order to calculate the values of the parasitic inductances when the circuit layout is known a 3d finite element method can be used but during this project this was not possible. What became obvious, though, during the analytical calculations, where various inductance values were tried, is that these inductances do not affect the losses on the switch in our case because of the zero channel current during the turn off transient. Their influence was, mainly, on the voltage overshoot and the switching time. Therefore these values, during the analytical calculations were arbitrarily chosen using information from corresponding literature.

At [37] on a similar size converter and power loop the inductance value was ranging from 6.3nH down to 1.2nH at a more optimized version. Taking this into consideration in this project the value of the parasitic inductance of the power loop was chosen to be 5nH. The source inductance at the same study was calculated to be less than 1nH. However, in our case it was taken similar to the power loop inductance since the loop of CSI is initially supposed, for simplicity reasons, to have the same influence, and size, as the power loop. Finally, the gate loop inductance is not considered since it is not used in the loss calculation model.

After calculating the power losses on the switch at a specific operating point the results will be used to calculate the operating temperature. For that the data from the datasheet will be used and more specifically the values of the thermal resistance. It is generally more accurate to calculate the losses using the Junction to Board thermal resistance, $R_{th,jb}$ and then to calculate the Board to Ambient value, $R_{th,ba}$, using analytical or simulating tools, but this require knowledge of the PCB board characteristics, therefore it cannot be done during the design procedure. As a result, at this stage of

the thesis the value that was used is the Junction to Ambient, $R_{th,ja}$, which is also commonly used but for more crude calculations. According to the datasheet the value of this resistance is $80^oC/W$ and it is calculated when the device is mounted on one square inch of copper pad, single layer 2oz copper on FR4. The PCB that was initially planned to be used is, indeed, a single layers 2 oz FR4 (actually it is double sided but with no thermal vias - the upper and bottom layer are only electrically connected through the ground) but the copper pad area is not defined either at this stage. In the application notes of the device, however, the thermal resistance is given as a relation to the copper pad area as shown at figure 3.15.

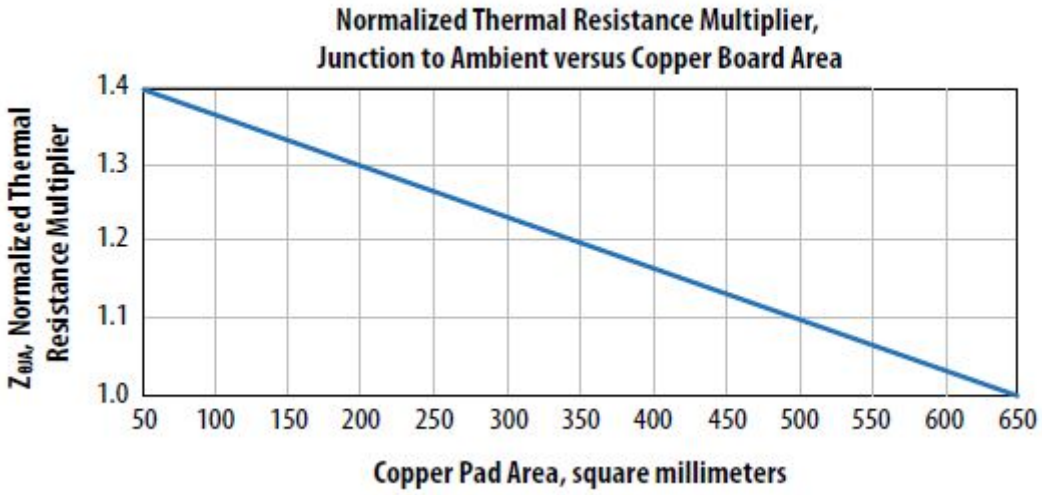


Figure 3.15: Junction to ambient thermal resistance as a function of decreasing copper pad area, normalized to 645.16 mm^2.

Using this plot the value of the thermal resistance was calculated assuming the worst case scenario of an area of 50 mm^2. Therefore the factor 1.4 was used. Note that the maximum junction temperature of this component is 150^oC.

The Diode

The diode that was chosen for the converter, also based on the electrical requirements of the application and the first order calculations, is the SS5P6 high current density surface mount Schottky barrier rectifier with maximum reverse voltage of 60V and average forward current of 5A. From the datasheet all the required electrical characteristics of the component, like the on resistance, the threshold voltage and the parasitic capacitance, can be extracted using the given graphs and making the appropriate assumptions as regards the maximum desired operating temperature. These values are used at the analytical model.

For the thermal calculations of the component, similar to the GaN device, the junction to ambient value is used which equals $65^oC/W$. According to the datasheet, this value corresponds to an FR4 PCB with 1oz. copper layer and a mounting pad layout with given dimensions. Since the used PCB is 2oz. (which means better thermal characteristics) and this specific pad layout is at least planned to be used this value could be relatively accurate for the thermal calculations during the design procedure. The maximum junction temperature of this component is 150^oC.

Input and Output Capacitances.

The values of the input and output parasitic capacitances are calculated assuming maximum voltage ripple of 10% and ESR value of 20mOhm. The value of ESR is taken as such considering the fact that the used capacitors will be ceramic which have low ESR, according to literature not more than 20mOhm in general, especially when compared to the electrolytic ones. Even more, because these capacitors are placed in parallel the ESR value can be significantly low. The temperature on these devices is not taken into consideration.

3.6.2 The Procedure of Selection

Having specified all the necessary electrical and thermal values of the components it is possible now to use the appropriate analytical equations and models that describe the operation of the converter and to calculate the losses and, thus, the corresponding operating temperatures at each operating point. The operating points for which the calculations take place are $V_{in} = 13.2V$, $V_o = 6.5V - 14.5V$ with a step of 1V, and $I_o = 1A$ and $1.2A$. This means that in total there are 18 operating points at which the values are calculated.

So, the procedure of selection has as follows: Each time from the inductor bank one coil geometry is selected. This includes the inductance value, the size of the component, the dc resistance and the ac resistance (for the specific frequencies as explained). Using this inductance value the operating frequency, at a specific operating point, is approximated using the equations 3.1 to 3.3 and then for this frequency the ac resistance of the coil is linearly calculated using the values from the bank. Here, it is assumed that the ac resistance does not change significantly between the two frequencies, which is actually very close to reality. With these new values and the electric values of the rest of the components the equations 3.4 to 3.6 are now solved and the new operating frequency, on and off times and the peak inductor current are found. From these the required input and output capacitances, the average inductor current and the rms values of the rest of the currents can be extracted.

Now, having calculated all the required current and voltage values the losses on each component can be calculated. The losses on the GaN switch are estimated using the equations that are presented at table 3.6. From these equations the driving losses and the losses due to the ringing transient of turn off, which mainly dissipate on the stray resistance of the circuit, can be estimated as well. For the losses on the diode component the common formula is used which is the following:

$$P_{diode} = V_{td} \cdot Io + R_{Don} \cdot I^2_{Drms}$$

where V_{td} is the threshold voltage and R_{Don} the diode on resistance both extracted from the diode's datasheet for a temperature of approximately 100^oC.

Finally, as regards the planar coil only the copper losses are considered, as already explained, and thus the dc and ac resistance values are used for these calculations.

Having calculated the losses on each component it is possible to estimate their operating temperature. For both the diode and the GaN switch the common linear formula $P_{loss} = (T_{junction} - T_{ambient})/R_{th,ja}$ solved for the junction temperature is used. As regards the coil the temperature is estimated with the finite element tool of Comsol using the values of the voltages and currents calculated previously. Note that because of the high values of the ambient temperatures (up to 85^oC) at this application it is important to give special attention on the maximum operating temperature at the component with

the most losses. Both the GaN device and the diode have maximum junction temperature 150^oC, therefore it is clear that in the worst case, where the ambient temperature is 85^oC, the junction temperature should increase less than 65^oC (65^oC is the temperature difference, the increase of the temperature, not the actual junction temperature which is 65^oC+$85^oC = 150^oC$). In practice, however, for safety reasons it is preferred to operate the device 20-25^oC lower than its maximum junction temperature. As a result, the increase of temperature would be better not to exceed the 40^oC.

The whole process is repeated for every geometry of the inductor bank and the results are stored so that they can be compared with each other. The comparison is based on two criteria: the maximum increase of temperature for the components and the size of the planar inductor. This comparison based on the results is presented at the following paragraph. The whole procedure of selection is described with a flowchart at the following figure.

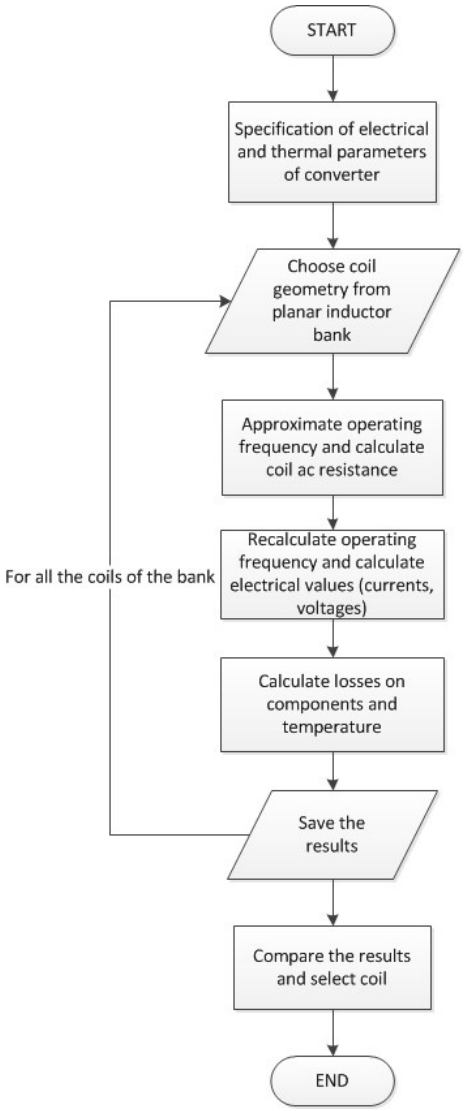


Figure 3.16: Flowchart that shows the procedure for determining the required coil geometry.

3.6.3 Selection of the Inductance Value

Using the Matlab software the previously described procedure was executed. Note that the presented results correspond to the point $V_{in} = 13.2V$, $V_o = 14.5V$ and $I_o = 1.2A$ which is the point at which the maximum losses occur. If the conditions are met at this specific point they will be met as well for the rest of them.

In this application we are mainly interested in two things: the maximum increase of temperature of the components and the size of the planar inductor.

Because of its large area the increase of temperature on the planar coil is relatively small. Also, as already stated the used magnetic materials are thermally not appropriate for this application. For that reason the main focus is on the increase of temperature on the diode and the switch. At figure 3.17 the temperature difference of the diode and the GaN switch are presented.

The presented results show that the diode in this converter is the crucial component as regards its thermal behaviour. This is not an unexpected outcome since in a buck boost converter operating at boundary conduction mode with valley switching the losses on the diode are significantly higher compared to the losses on the switch. This significant difference is expressed on their increase of temperatures quite clearly, despite the fact that the considered junction to ambient thermal resistances differ (for the diode is taken equal to $65^oC/W$ while for the switch is taken equal to $112^oC/W$). It is quite interesting the fact that the temperature increase, after a certain inductor value, hardly falls below 40^oC for this operating point.

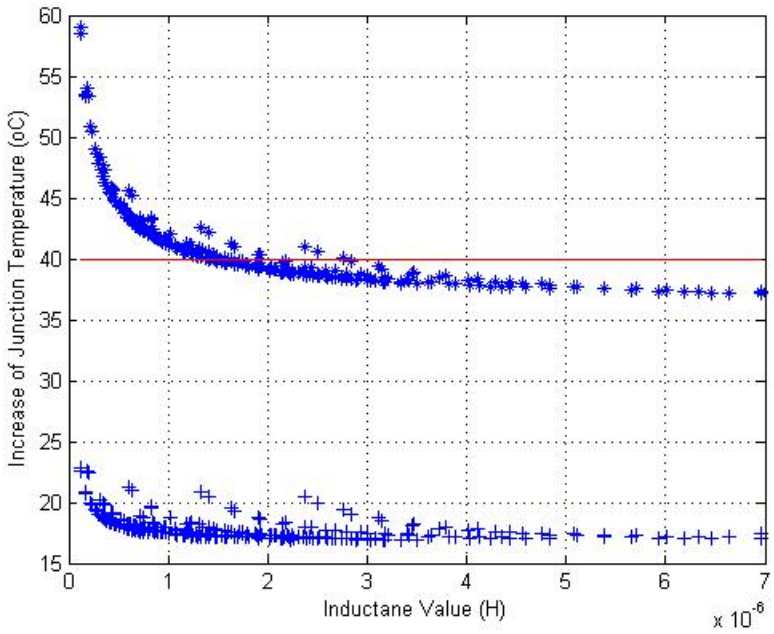


Figure 3.17: Dependence of diode and GaN switch junction temperature with the inductance value.

The second point of interest is the size of the planar coil. At figure 3.18 the diameter of the coil in relation to the inductance value is presented.

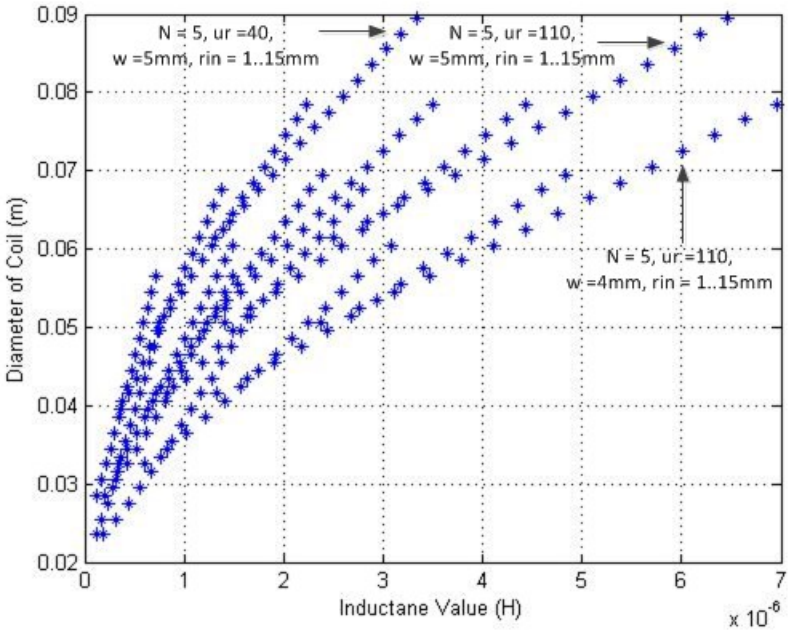


Figure 3.18: Diameter of the coil component in relation to the inductance value.

At this figure it is initially obvious that the increase of the inductance value is directly related with the increase of the coil diameter. Apart from that we can observe different groups of values at this figure. This is related to the step increase of the various values of the geometry which results to the clustering of the data. For example, the last set of points includes all the coil values with $N = 5$,$u_o = 110$,$w = 4mm$ and with the input radius increasing from $r_{in} = 1mm$ to $r_{in} = 15mm$.

Taking into consideration the previous graphs and the results of the simulations it is possible now to choose the inductance value and coil geometry that fits better to this specific applications. At table 3.10 the chosen value with the characteristics of this coil are presented.

Selected Planar Coil Values	
Inductance Value	1.65uH
Diameter	5.15 cm
μ	110
Number of Turns	3
R_{dc}	15 mOhm
R_{ac} @ 761kHz	126 mOhm

Table 3.10: Coil Values for the selected planar inductor geometry.

The results of the simulations for this specific topology are presented at table 3.11

Simulation Results for Selected Planar Coil	
Diode Losses	0.62W
Diode Junction Temperature Increase	39^oC
GaN Losses	0.16W
GaN Junction Temperature Increase	18^oC
Coil Losses	0.73W
Coil Temperature Increase	26^oC
Efficiency	91%
$I_{L,pk}$	5.4A

Table 3.11: Results of the simulations for the selected planar coil geometry.

Comparison with the Discrete Coil.

As it has already been explained, the behaviour and influence of the planar coil is planned to be compared with the behaviour and influence of the discrete coil. In order to do so the discrete inductor needs to have the same inductance value with the planar. Using the properties of the 3f4 ferrite core and the linear magnetic equations the discrete coil was designed and its values are presented at table 3.12

Discrete Coil Values	
Inductance Value	1.7uH
Size	see fig.3.14
μ	950
Number of Turns	2
Airgap	0.116mm
Bmax @ 13.9A	300mT
R_{ac} @ 808kHz	30mOhm

Table 3.12: Coil Values for the discrete inductor.

Note that the ac resistance was not calculated but it was measured after the coil was built.

The values of this coil were used at the analytical model, for the same operating point, giving the results presented at table

Simulation Results for Discrete Coil	
Diode Losses	0.62W
Diode Junction Temperature Increase	40.2^oC
GaN Losses	0.15W
GaN Junction Temperature Increase	17^oC
Coil Losses	0.75W
Efficiency	91.8%
$I_{L,pk}$	5.43A

Table 3.13: Results of the simulations for the discrete coil geometry.

From the results shown on the table it seems that the two coils have more or less the same influence, as regards the losses and efficiency, on the circuit. There are certainly some differences as regards their operation, like the operating frequency or the duty cycle which are due to the different resistance of the coils. The losses, however, are similar because the operating conditions are almost the same. Note that the inductor

losses in the case of the discrete coil include both the copper and the core losses but the copper losses are relatively small compared to the core losses. The latter were calculated in approximation using the information from the datasheet while the former using the measured with the impedance analyser ac resistance. Despite the fact that at the planar coil only the copper losses are calculated whereas at the discrete both the copper and the core, the result is that for both cases the calculated losses are quite close. What will be obvious, however, at the experimental part is that the losses of the planar coil are actually quite higher than the simulated (the built coil has almost double ac resistance from the one simulated at FEM) resulting to significant lower efficiency. This part will be discussed later. Finally, it should be mentioned that the temperature on the discrete coil was not calculated.

3.7 Design Considerations of the Converter

Now that the inductance value and the design of the inductor have been specified everything is in place for the building of the converter. Before that, however, it is considered necessary to mention some side aspects of the converter and the pcb design. This aspects are discussed at this paragraph.

Driving the GaN Switch.

The importance of paying special attention in the driving of the GaN switch has already been discussed at chapter 2. Specific drivers have been developed from Texas Instruments for these components and they have been used for this application as well. The driver that was used is the LM5114 low side gate driver. It should be noted here that in order to use this component the switch should be grounded which means that the topology presented at figure 3.1 is modified as shown in figure 3.19. The benefit of this configuration is that the switch is grounded and thus its driving does not require voltage shifting. On the other hand, however, the output voltage is not grounded but it is floating. In this application this does not consist a problem since the load, that is the OLED lights, does not require to be grounded.

Another important aspect, as regards the driving of the switch, is the selection of the gate resistance. The value of this component should not be too high, as it would slow down the switching speed and, thus, cancel the main benefit of the GaN and increase the driving losses. On the other hand, applications where for the driving of this switch no gate resistance is used can be found this solution was not preferred for reasons which can be seen on chapter 2. As a result, a value of 2 Ohm for the gate resistance was considered reasonable and it was finally used.

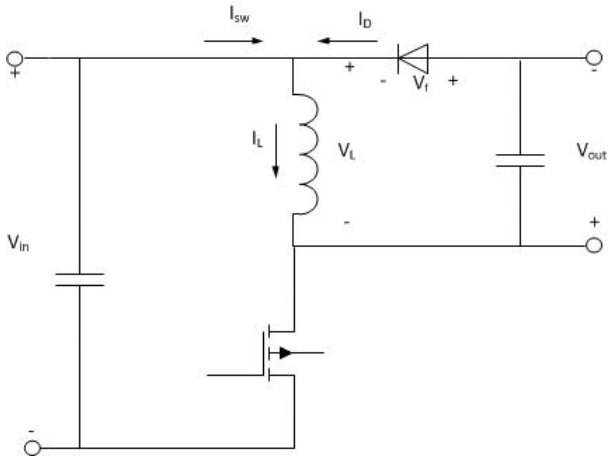


Figure 3.19: Schematic of the Buck-Boost Topology with grounded switch.

Power and driver loop minimization.

It has been already underlined the significance of minimizing these two loops, especially in a high frequency application. Therefore, the design of the PCB layout was, from the beginning, turned towards that direction. This requires careful arrangement of the components so that these two loops are minimized and, in the same time, the electrical and especially the thermal requirements are maintained.

At the following figure these two loops are presented on the PCB layout which was designed at the software Altium Designer. The two yellow rectangles (large dashed lines) correspond to the input and output power loops whereas the third one (small dashed line) corresponds to the driver loop. As it can be seen the three loops are quite small as regards their size.

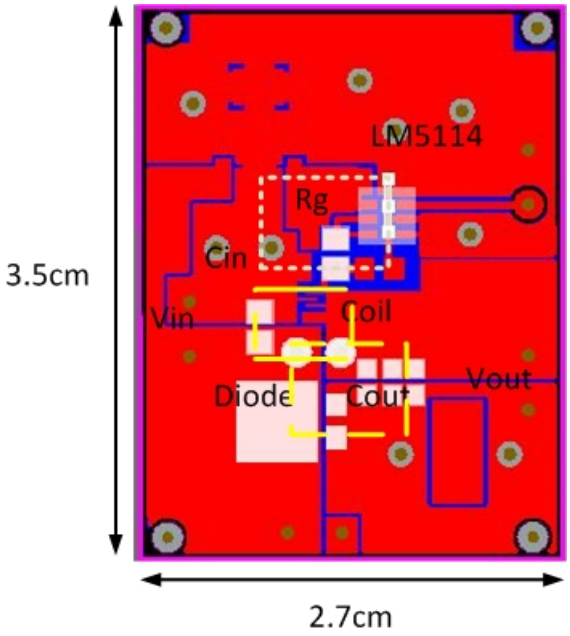


Figure 3.20: The power and driver loops on the PCB layout.

Thermal aspects.

It has already been mentioned that for the analytical models the recommended pads have been assumed so that the given junction to ambient thermal resistance values can be used. During the design of the PCB layout special effort was given so as to increase the area of the copper pads around the diode and the GaN switch and to enhance the thermal dissipation. For the former this was possible as it can be seen at figure 3.20 but this was not the case for the latter where the copper area around the switch is not as large as it would be desired. It is expected, thus, that the temperature increase of the GaN switch will be more than the calculated. Note that the vias that are scattered along the PCB are not thermal vias (they are not copper plated) but they just connect electrically the upper layer and the bottom which is mainly ground.

Chapter 4

Experimental Results

At the previous chapter the most important steps of the design procedure were presented and explained. Based on the results of the design process the PCB of the prototype converter was manually built using the equipment of the laboratory and then tested.

This chapter presents initially the final prototype of the converter and the experimental set up. Some characteristic waveforms of the converter operation and also some pictures presenting the thermal profile are also shown. After that the procedure for a more accurate estimation of the GaN junction-to-ambient thermal resistance is presented. The new approximated value is used to recalculate the temperature of the GaN device using the results of the analytical model and compare it with the experimental results. The experimental results based on the measurements that were conducted on this prototype are presented along with the simulated results and a discussion is made on them.

4.1 The Experimental Setup

4.1.1 The Converter Prototype

At figure 3.19 of chapter 3 a schematic of the buck boost converter with only the fundamental components was presented. Here, at figure 4.1 a complete schematic with all the components used for the converter and the relevant information is shown.

This schematic shows, apart from the basic components which have already been discussed, the driver of the GaN switch, the linear voltage regulator which is used for the power supply of the driver, and two zener diodes. The latter are used in case of an overvoltage so as to protect the switch. If, for example, the load is disconnected while the circuit is operating then the coil, being incapable to discharge, will increase its voltage across it and it will destroy the switch.

Note that both at the output and at the input (although in the schematic is not shown) multiple capacitors are used so that the equivalent series resistance is minimized.

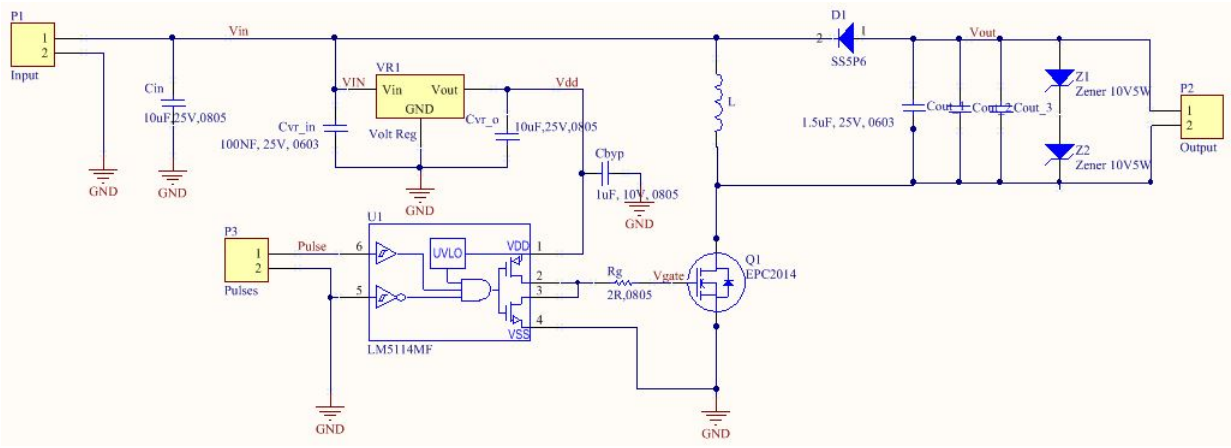


Figure 4.1: Schematic of the converter with all the components.

Using this full schematic the layout of the PCB was made as shown at figure 3.20 (upper layer) of the previous chapter. The Gerber files of the layout were then used in order to build the PCB board. This board was made "manually", which means that the LFPK drilling machine of the laboratory was used. The main advantage of using this machine is that it gives the capability of building several prototype boards without any time delay as it happens with an external manufacturer. On the other hand, it lacks accuracy and it is prone to errors especially for small dimensions where the drills are very thin and fragile. In this case, there was some difficulty in making the GaN pad because of the small dimensions of the clearance between the electrodes (200um). The drill (actually the universal cutter) had to be adjusted properly in order to achieve the correct dimensions.

At figure 4.2 the final prototype converter is shown with the components soldered on it.

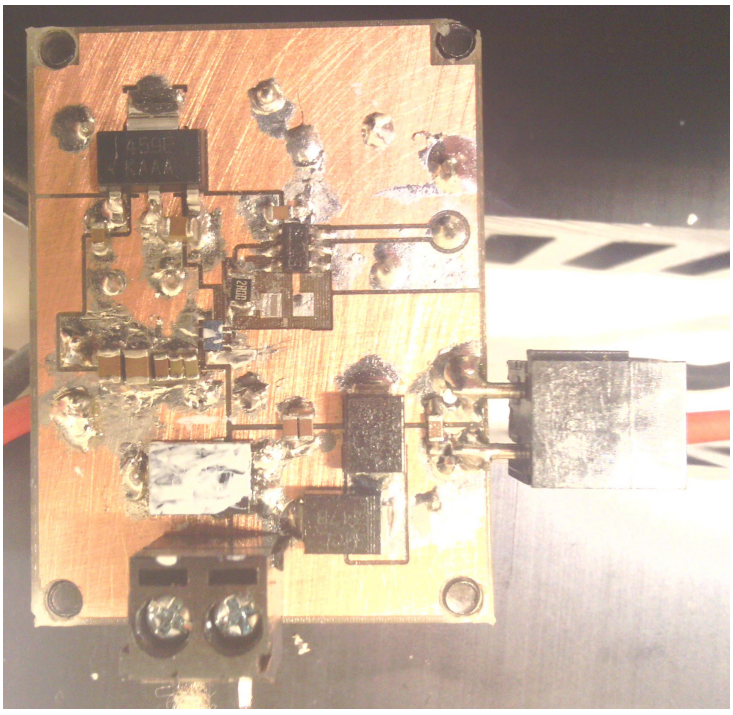


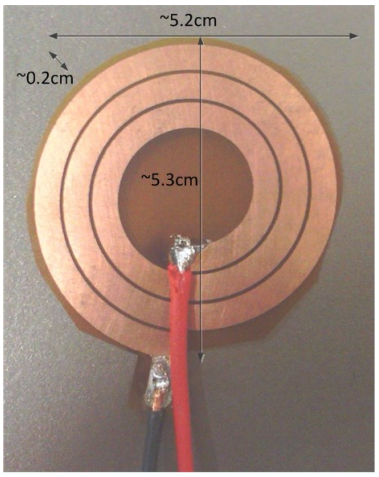
Figure 4.2: The final prototype of the converter with the soldered components.

At the center of the converter with the blue colour the GaN switch can be seen.

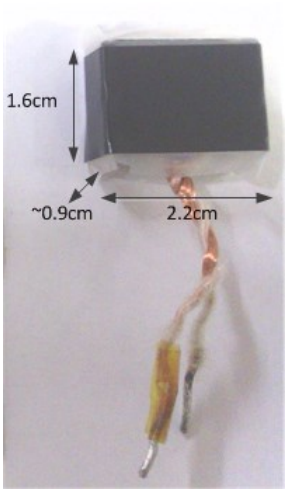
The only component that is not observable is the coil which is connected to the board through a connector. The input is on the left and the output on the right. The pulses come from the microcontroller and they are connected at the bottom side of the board. The measurements are also taken from the bottom side of the board.

4.1.2 The Inductor Components

The two coils that were used, the planar and the discrete, are shown at the following figures. Figure 4.3a shows the planar inductor placed on the bottom leaf of core (grey colour) and figure 4.3b shows the discrete inductor.



(a) The planar inductor.



(b) The discrete inductor.

Figure 4.3: The two inductor components that were used for the experimental set up.

The values of the two coils that were finally built are shown at the following table:

Planar Inductor	
Inductance Value	1.610uH
R_{ac} @ 600kHz	198mOhm
R_{ac} @ 800kHz	227moHm
Discrete Inductor	
Inductance Value	1.606uH
R_{ac} @ 600kHz	23mOhm
R_{ac} @ 800kHz	30moHm

Table 4.1: Final Values for the built inductors.

4.1.3 The Complete Setup

Finally, at figure 4.4 the whole experimental set is presented.

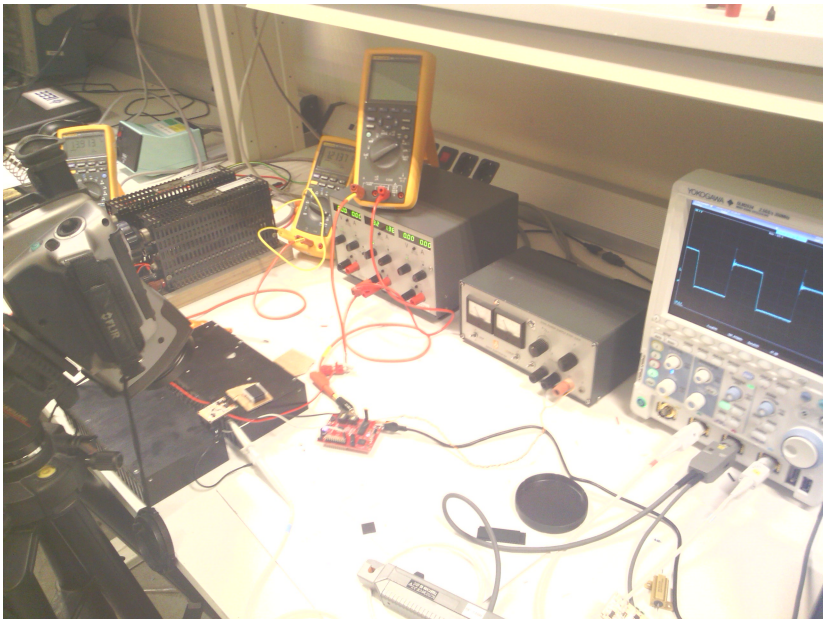


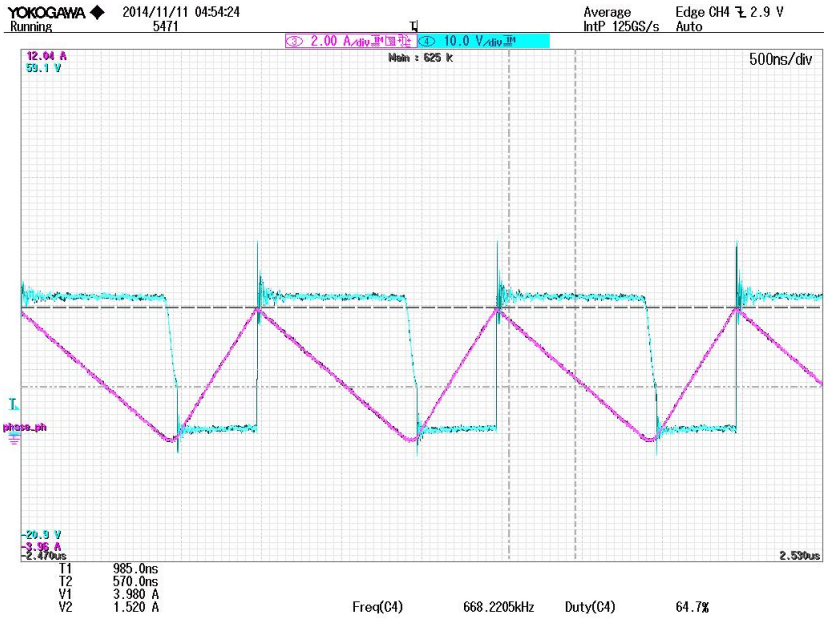
Figure 4.4: The experimental set up with the various instruments.

At this figure the various used instruments are shown including the variable load resistors, the thermal camera with which the thermal measurements were taken, the microprocessor and the measuring instruments. The converter is operating as it can be seen on the screen of the oscilloscope.

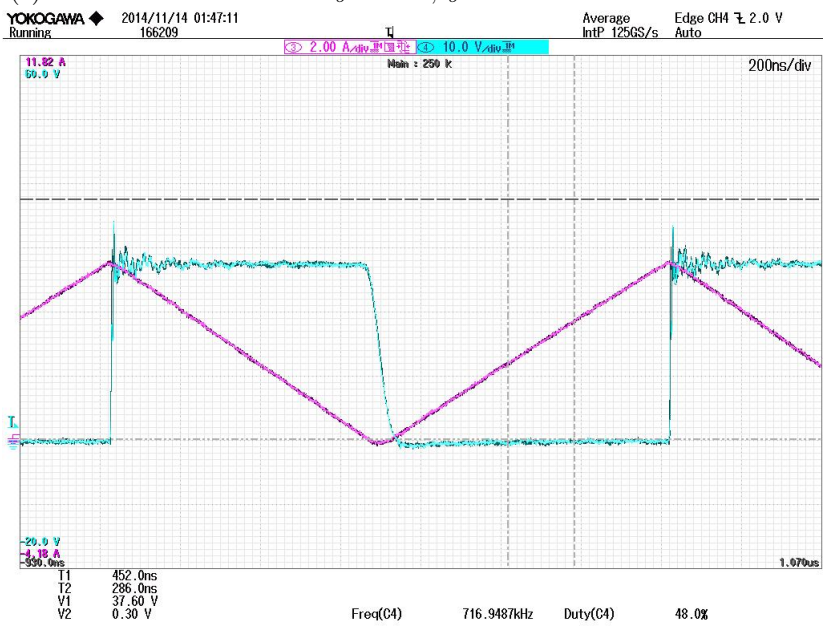
4.1.4 Characteristic Waveforms of the Converter

It is considered necessary to show at this point some of the waveforms of the converter in operation. Figure 4.5 shows the waveforms of the drain to source voltage of the GaN switch (cyan) and the current of the discrete inductor (magenta) when operating at two different points, $V_{in} = 13.2V$, $V_o = 6.5V$,$I_o = 1.2A$ and $V_{in} = 13.2V$, $V_o = 13.5V$,$I_o = 1.2A$.

As it was expected, when the converter is operating at the first operating point the operating frequency is slightly smaller compared to the second one. At both figures we can notice the valley switching, that is the oscillation between the drain-source voltage and coil current, when the switch turns on. At the first one, however, because Vo is smaller than Vin the voltage after the transient does not go to zero as it happens in the second case. Also, because of the fact that the switching (turn on) in the second case happens at almost zero voltage and current no transients occur. At the first case this ringing after the turn on is noticeable. Finally, in both cases the voltage overshoot is acceptable, despite the very fast switching of the switch, which means that the power loop parasitic inductance of the prototype is not significant.



(a) Converter waveforms for $V_o = 6.5V$,$I_o = 1.2A$.



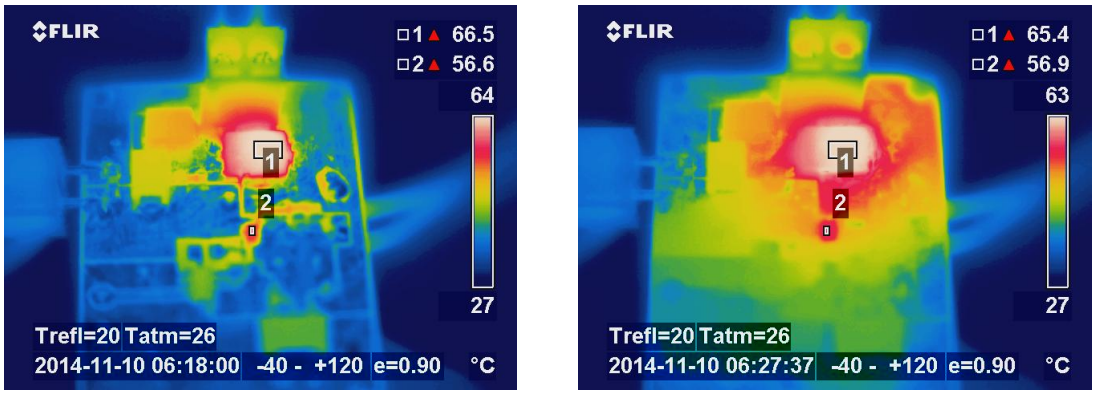
(b) Converter waveforms for $V_o = 13.5V$,$I_o = 1.2A$.

Figure 4.5: The GaN drain-source voltage and coil current waveforms for the two operating points.

4.1.5 Thermal Measurements

For measuring the temperature on the GaN switch and the diode a thermal camera, model of FLIR, was used accompanied with special lens for that size and distance. Even more, a certain kind of spray with known emissivity was used on the surface of the converter for more accuracy and for making possible to observe the heat expansion on the copper area (without which this is not possible because the copper is "seen" in room temperature). In this kind of measurements it is important to keep the room temperature as constant as possible and monitor it but most important is to avoid any kind of air streams because they influence the measurements. At figure a thermal image of the converter is presented with and without the use of the special spray. We can

easily observe the difference as regards the temperature of the copper area.



(a) Thermal image of the operating converter without the use of the spray.

(b) Thermal image of the operating converter at the same point with the use of the spray.

Figure 4.6: Thermal images of the converter operating at the same point without and with the use of the special spray.

The two boxes on the images are used for averaging the temperature values inside them and are placed on the diode and the GaN switch. All the series of thermal measurements were conducted in the same way. Note that the ambient temperature was measured for each different measurement using thermocouples.

4.2 Estimation of the GaN Junction-to-Ambient thermal Resistance

At the design part of this thesis the value that was used for $R_{th,ja}$ was taken from the datasheet and was approximated, using figure 3.15, to the value $112^oC/W$. This value was used for the initial simulations before the built of the prototype and it was useful for this stage of the thesis. Now that the converter prototype has been built and the PCB layout is known the junction-to-ambient thermal resistance can be calculated more accurately. Here, the procedure for calculating the new thermal resistance for the GaN device is presented.

This method is using the resistor model to represent the thermal resistors and their interconnections. For this model it is necessary, initially, to define the area where the thermal energy is flowing laterally. For example, for a generic SMD device we assume that, due to the available copper pad around the device, the lateral flow of energy is symmetrical, at both sides in two arcs that correspond to radius R and angle θ. This is shown at figure 4.7.

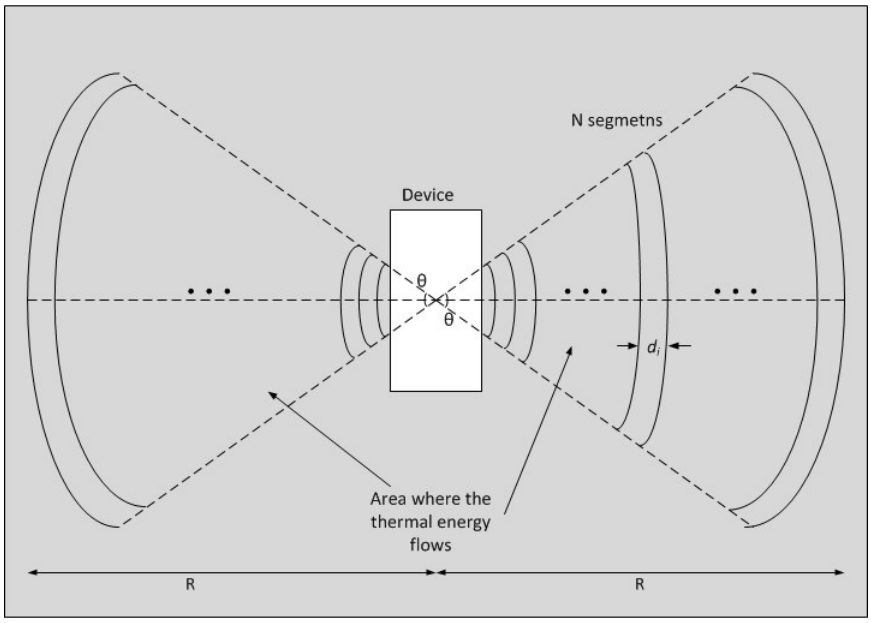


Figure 4.7: Defining the area of the lateral flow of thermal energy.

After defining that, the area in these arcs is divided into N segments of egual size d, as shown at the previous figure.

Based on these, the areas that are defined by the copper pad of the PCB prototype are shown at figure 4.8. For reasons of simplicity of the calculations the areas are defined as two arcs corresponding to an angle of 90^o at each side of the GaN switch, which is a good approximation of the. The radius of each arc is chosen equal to $7.5mm$.

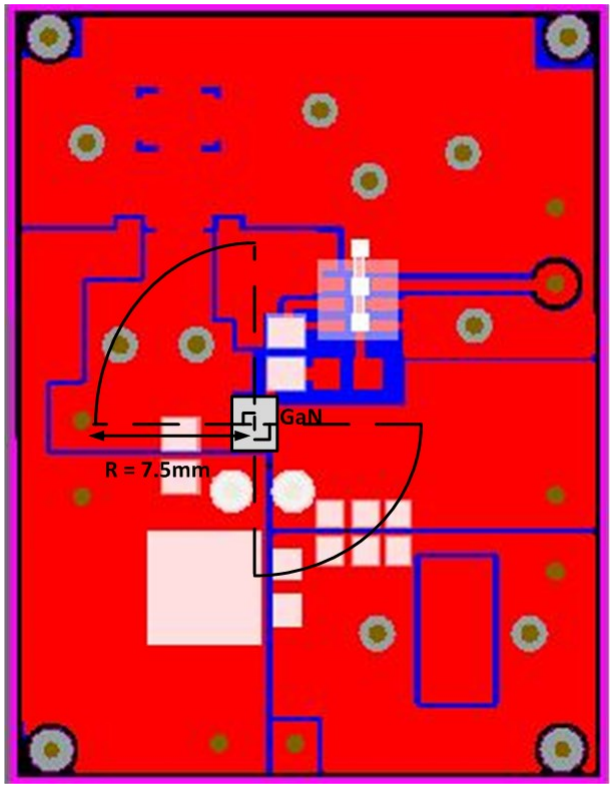


Figure 4.8: Area of the lateral flow of thermal energy for the PCB prototype of the converter.

Of course, thermal energy is flowing both in the lateral and in the vertical direction. For each direction, the flow encounters thermal resistance which is dependent on the material and the dimensions of it and is calculated by the well-known formula:

$$R_{th} = \frac{d}{K_{mat} \cdot A} \tag{4.1}$$

where d is the length of the segment (horizontal to the flow), K_{mat} is the thermal conductivity of the material and A is the area perpendicular to the flow. The thermal conductivities of the copper and FR4 are known and were taken equal to $K_{cu} = 400$ $W/m{\cdot}^oC$ and $K_{FR4} = 0.343$ $W/m{\cdot}^oC$. The following figure shows a segment of a copper or FR4 for which the heat flows either towards the lateral or the vertical direction:

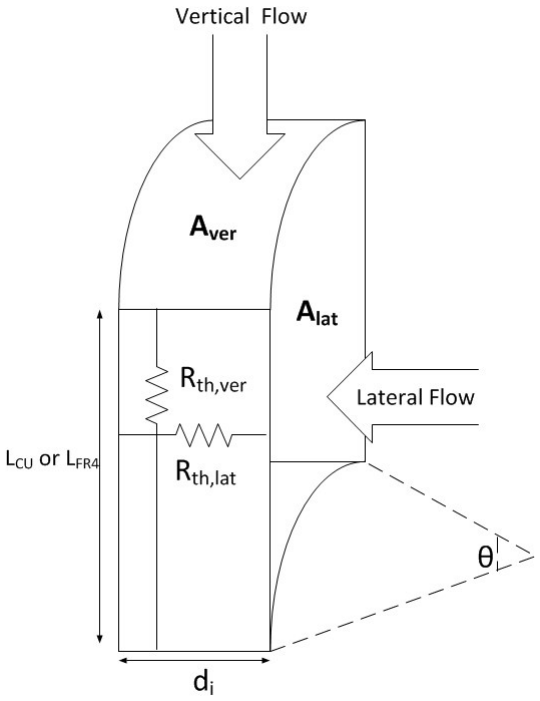


Figure 4.9: Thermal resistance of a segment.

It is clear now that there are both vertical and lateral thermal resistances. In our case, the PCB prototype consists of two copper layers at each side of the board and the FR4 layer. The thickness of each layer is known and the length of it as well(for the lateral flow the length depends on the number of segments that the area is divided).

Another important parameter is the surface-to-ambient thermal resistance which is calculated using the following formula:

$$R_{th,sa} = \frac{1}{h \cdot A} \tag{4.2}$$

where h is the convection coefficient and A is the area of the segment where the thermal convection takes place (in this case from the two copper sides of the PCB). The value of the h coefficient is not easy to accurately calculate but it can be approximated. The calculation of this value is based on the computational fluid dynamics and the corresponding equations are presented at the appendix. Because the value of this parameter is dependent on the size and orientation of the surface this means that for each ring and

for each copper surface (upper and lower) the value of h needs to be recalculated for each ring and, thus, the value of $R_{th,sa}$ differs for each case.

At the following figure, all the thermal resistances corresponding to the thermal flow at the one side of the GaN device are shown.

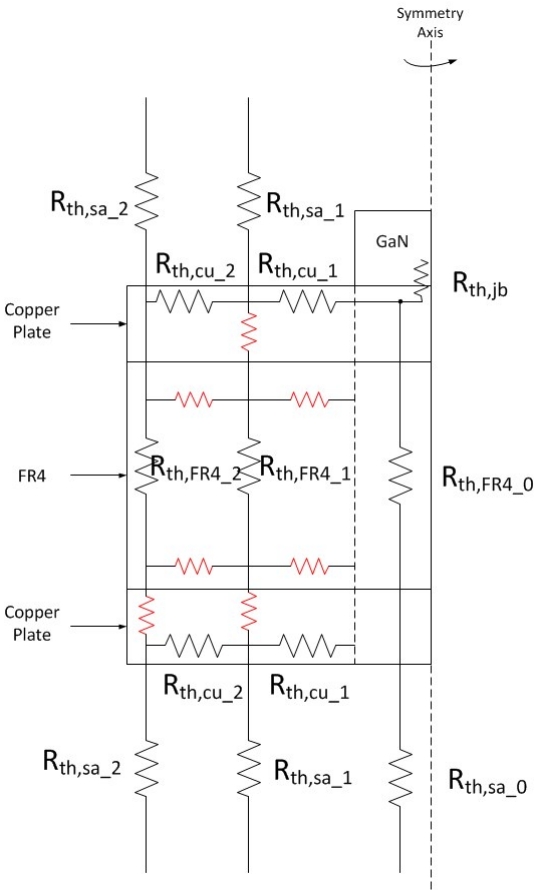


Figure 4.10: Equivalent thermal model of the PCB showing the thermal resistances at the one side of the GaN device.

Note that the resistances that are red and small can be neglected because of their large value compared to the other thermal resistances.

Using this equivalent model it is now possible to calculate the junction-to-ambient thermal resistance. This can be done by calculating all the thermal resistances of the N segments (where N was chosen equal to 10) and using the, known from the datasheet, junction-to-board thermal resistance of GaN device. After that, a current source representing the dissipated power in the switch is placed before the junction-to-board thermal resistance. If the value of this is chosen equal to 1W then the temperature difference (equivalent to voltage difference) between the point before the $R_{th,jb}$ and the point corresponding to the air (equivalent to ground) equals to the junction-to-ambient thermal resistance, $R_{th,ja}$.

Using this method the junction-to-ambient thermal resistance was found equal to $R_{th,ja} = 271^oC/W$. This value is considerably higher compared to the used at the design part which was $R_{th,ja} = 112^oC/W = 1.4 \cdot 80^oC/W$. Using this new value the temperature of the GaN device can be be recalculated and compared to the measured values. This is presented at the next paragraph.

4.3 Experimental Results

4.3.1 Comparison of the Two Coil Topologies

As already explained for the magnetic component of the converter there are two candidate topologies: a planar and a discrete inductor. In order to conclude to the most beneficial it is necessary to compare them as regards the basic requirements of the application which are: size reduction, thermal limits and efficiency. The two components were built as shown at figure 4.3, connected to the converter and tested for the operating range corresponding to Io=1.2A were the losses and therefore the component temperatures are the highest. At this paragraph the experimental comparison of the two components is presented and the results are discussed.

Size Requirements

An important requirement of this application is the small size and low profile character of the converter. The most crucial component here is the magnetic since the rest of them achieve sufficiently this specification.

It is clear that the planar coil ensures low profile for the converter, as well as flexibility, both important characteristics for the OLED technology. At the same time, however, it requires significant area because of the low permeability and the small thickness of the available core. On the other hand the discrete component is thicker but also quite smaller as regards the required area (see figure 4.3). Note, however, that the size of the discrete coil could be further minimized in the case that a smaller core was available. The current core is over-dimensioned for the requirements of this coil (small inductance value, 2 turns). A smaller core would not only reduce the size and the profile of the inductor but it would also reduce the core losses of the component increasing this way the efficiency.

For this application, there are no strictly defined requirements for the thickness or the size of the converter but the minimization of both is an objective. Definitely, the planar coil is more suitable for an application as such but the fact is that the discrete coil is, also, not very far from being a decent choice. The characteristics of both cases would be enhanced if there was more freedom in designing the components (i.e more available core materials).

Temperature Requirements

It is important, now, to examine whether or not the converter is within the thermal limits, as specified from the requirements and discussed at previous chapters, for both cases. At the following figures the temperature rise on the diode, GaN switch and the coil are presented for the case of the discrete and the planar inductor. Note that the temperature rise is given as $T_{component} - T_{ambient}$, where both values are measured for each measurement.

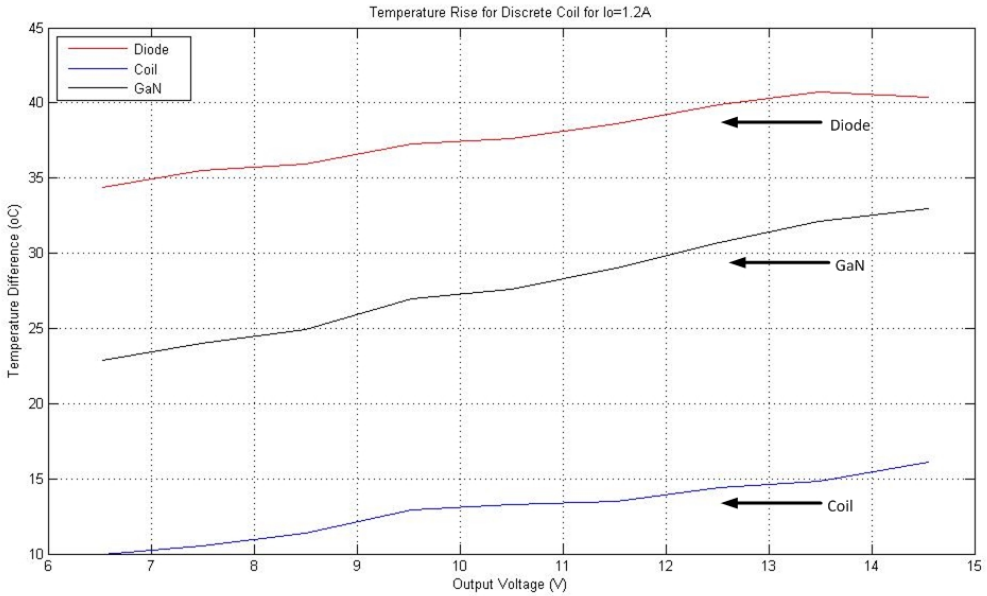


Figure 4.11: The temperature rise of the components when using the discrete coil.

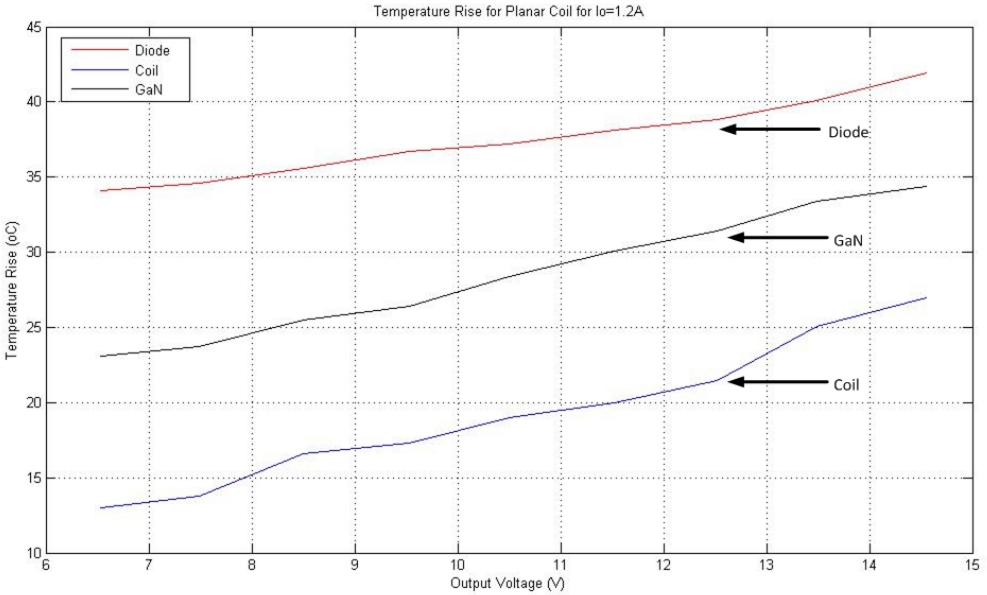


Figure 4.12: The temperature rise of the components when using the planar coil.

It is clear from the results presented at the previous figures that both cases meet the maximum temperature requirements quite well. The maximum temperature rise for both cases happens at the diode component and slightly overpasses the 40^oC. It should be noted here that the measured temperature is the temperature on the case of the component and not the junction temperature. However, the case to junction thermal resistance is very small and especially for the diode which is $R_{th,jl} = 3^oC/W$. This means that the temperature in the junction of the diode is not expected to be much higher than approximately 3^oC, considering the fact that the losses in the diode are not expected to surpass the 1W. The same holds also for the GaN for which the junction to case thermal resistance is $6.9^oC/W$. The low losses expected at this component and the

higher margin (according to the experimental results) from the maximum temperature rise ensure that the junction temperature will not surpass the predefined limit. In conclusion, both components meet the thermal requirements of the application.

Efficiency

Since both coils meet the thermal requirements of the application it is necessary now to compare them as regards the efficiency in order to draw a more robust conclusion. The efficiency of the converter is calculated by measuring the input and output values of the currents and voltages for each case. The efficiencies are compared at the following figure.

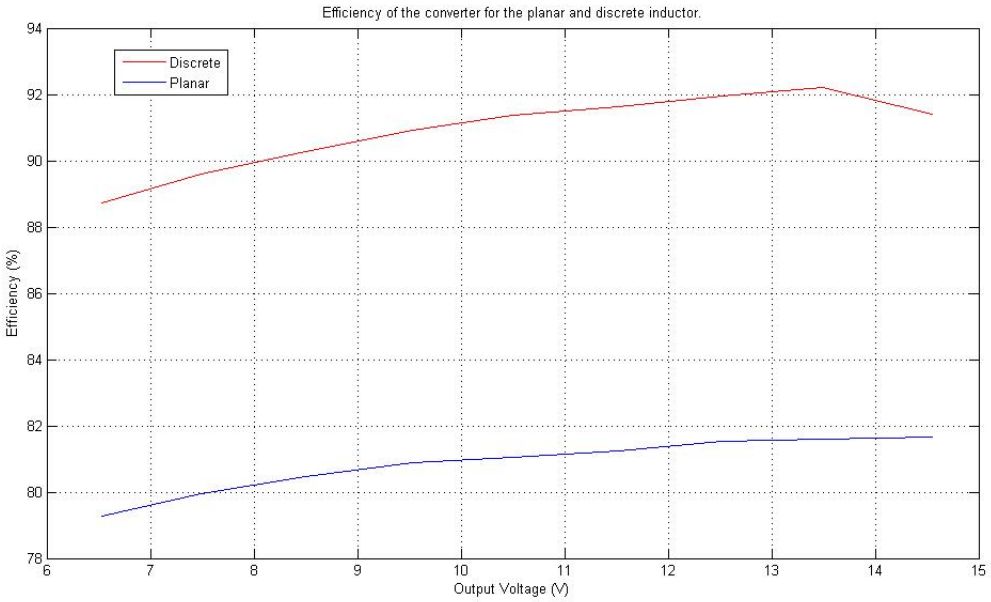


Figure 4.13: The efficiency of the converter for the case of the discrete and the planar inductor.

Figure 4.13 shows clearly that the efficiency of the converter when using the discrete inductor is significantly better compared to the planar one. With the discrete component the maximum achieved efficiency is slightly more than 92% while with the planar coil slightly less than 82%. A 10% difference in converter's efficiency is considerable.

Influence on Frequency and Inductor Current

The influence of the different coil topologies is obvious also at the operating frequency of the converter and the peak inductor values, as shown at table 4.2 . Note that these frequencies are the ones that were given at the microcontroller from the user (since the measurements were taken at open loop).

Operating Frequencies for different Vo and Io=1.2A					
V_o (V)	6.5	8.5	10.5	12.5	14.5
$f_{discrete}$ (kHz)	666.7	697.7	714.3	714.3	705.9
f_{planar} (kHz)	600	638.3	638.3	652.2	645.5

Table 4.2: Various operating frequencies for the built inductors.

Peak Inductor Current for different Vo and Io=1.2A					
V_o (V)	6.5	8.5	10.5	12.5	14.5
$I_{Lpk,discrete}$ (A)	3.9	4.4	4.8	5.2	5.7
$I_{Lpk,planar}$ (A)	4.3	4.7	5.2	5.6	6.1

Table 4.3: Peak inductor currents for the built inductors.

This influence of the ac resistance of the planar coil at both the frequency and the peak inductor current is expected. The reason is that since the inductance value and the desired operating points for the two cases are the same, the required stored energy (that is provided to the load at the turn off time) per cycle at the coil component needs also to be the same. However, part of this energy is dissipated on the coil resistance which, for the case of the planar coil is significantly higher. As a result more energy is required to be provided at the planar magnetic component so that to compensate for the higher losses on the ac resistance. This is expressed with the higher peak inductor value and the lower frequency (longer time to achieve this higher value, and generally to charge and discharge the inductor). Note that the duty cycles do not change significantly.

Conclusion

Using the aforementioned criteria and the experimental results for the selection of the magnetic component of the converter a final conclusion can be drawn. As regards the size the discrete component, although it does not have the low profile and flexible characteristics that the planar coil exhibits, it covers significantly smaller area with the possibility of reducing it even more (including the thickness) if a smaller core (of the same material) was available. Note that the high frequency operation enables this minimization of the core size because it allows a very small inductance value. As regards the temperature limits, they are not exceeded from the operation of any of the two options which means that both components meet this very important criterion. Their main and most significant difference regards the efficiency, where the discrete coil exhibits an efficiency of 10% (percentage points) more than the planar coil. From the figures representing the temperature rise it can be concluded that for both cases the losses on the diode and the switch are more or less the same, since the differences on the temperature are very small. Therefore, the great deviation on the efficiencies is due to the significant higher copper losses on the planar inductor.

As a conclusion, the discrete coil is considered better for this application compared to the planar one despite the fact that it lacks the flexibility and the very low profile character of the latter. It should be underlined again that the comparison refers to the components examined using the available materials, which means that a planar coil is not excluded, in general, as a candidate for such applications. On the contrary, flexible cores with higher permeability would result to planar coils with smaller size and, thus, less ac losses. In that case, the planar coil would be certainly the preferred component as it would fulfil all the size requirements of such an application. Here, however, the discrete coil is chosen as the appropriate magnetic component for the application.

4.3.2 Comparison between Experimental and Simulation Results for the Discrete Coil

In the previous paragraph it was made clear that the discrete coil results in a much better efficiency while maintaining a small size for the magnetic component, a size that could be minimized even more if a smaller core was available, and satisfying the thermal

requirements of the application. As a result this component is chosen to be used for this converter.

At this paragraph the experimental results for the whole operating range of the converter are presented and compared. Also, some other aspects of the converter's operation are examined. Note that the analytical results were obtained by using the analytical model presented at the previous chapter using the actual values of the discrete inductor as the coil parameters and the ambient temperature measured during the experiments.

The following figure presents and compares the measured and simulated efficiencies of the converter for the cases where the output current is Io=1A and 1.2A.

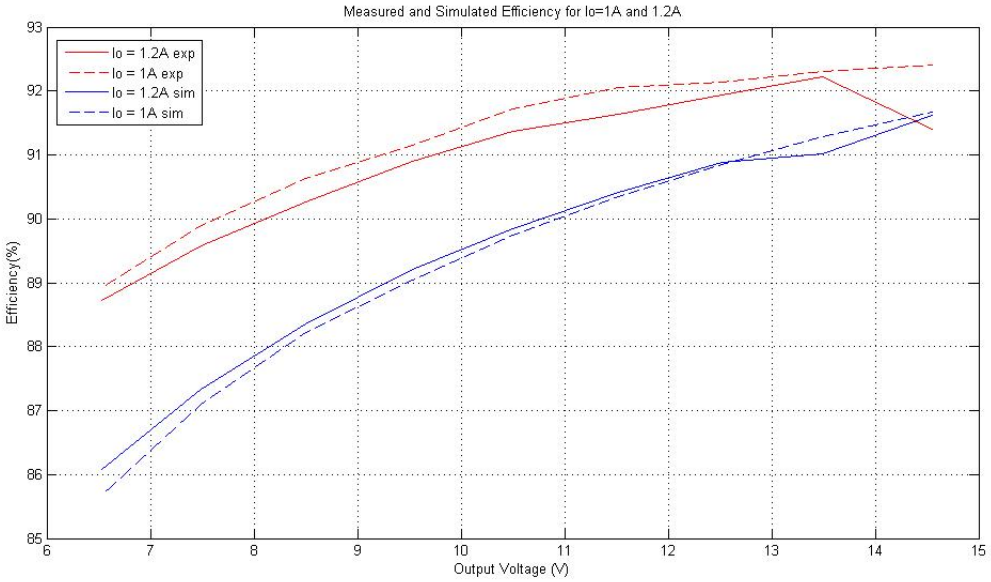


Figure 4.14: The measured and simulated efficiency of the converter for the case of the discrete inductor for Io=1A and 1.2A.

In order to have a more complete overview of the comparison the measured and the simulated temperature rise of the diode and the GaN switch need also to be compared. Note that because at the design procedure the discrete coil was not thermally modelled there is no comparison of the temperatures at the magnetic component. At figures 4.15 and 4.16 the experimental and simulated temperature rise for Io=1A and 1.2A for the case of the discrete coil are presented.

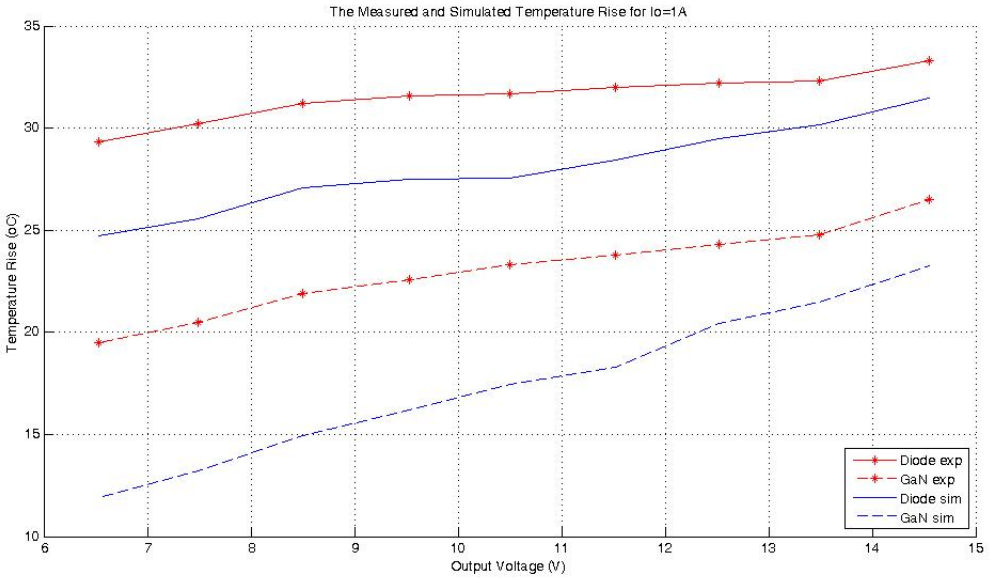


Figure 4.15: The experimental and simulated temperature rise of the components for Io=1A for the new $R_{th,ja}$ of the GaN.

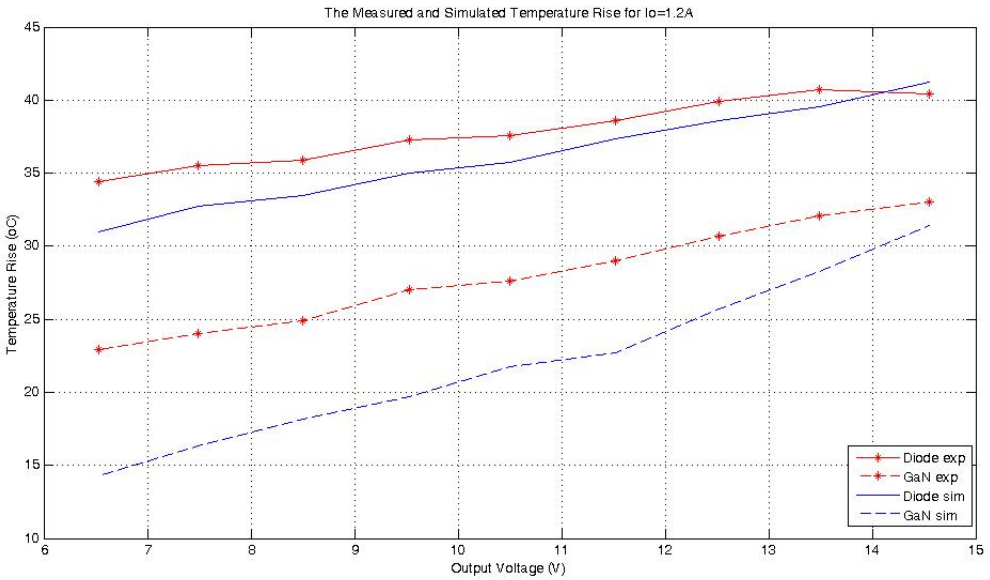


Figure 4.16: The experimental and simulated temperature rise of the components for Io=1.2A for the new $R_{th,ja}$ of the GaN.

At the following figures the experimental and calculated power losses for the three components are presented for both Io=1A and Io=1.2A. Note that in order to estimate the losses from the measured temperatures the thermal resistances that were used for the simulations were also used here. This gives certainly an inaccuracy but it is the only way to compare the measured and the simulated power losses. Also, note that for the case of the coil only the calculated losses are presented since the thermal analysis of the coil was not conducted.

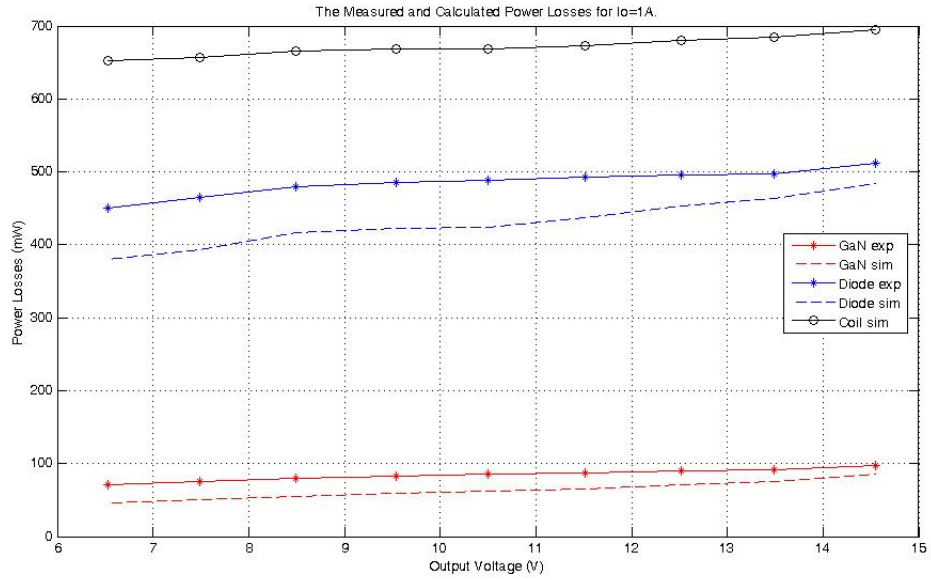


Figure 4.17: The experimental and simulated power losses for the three main components of the converter at Io=1A.

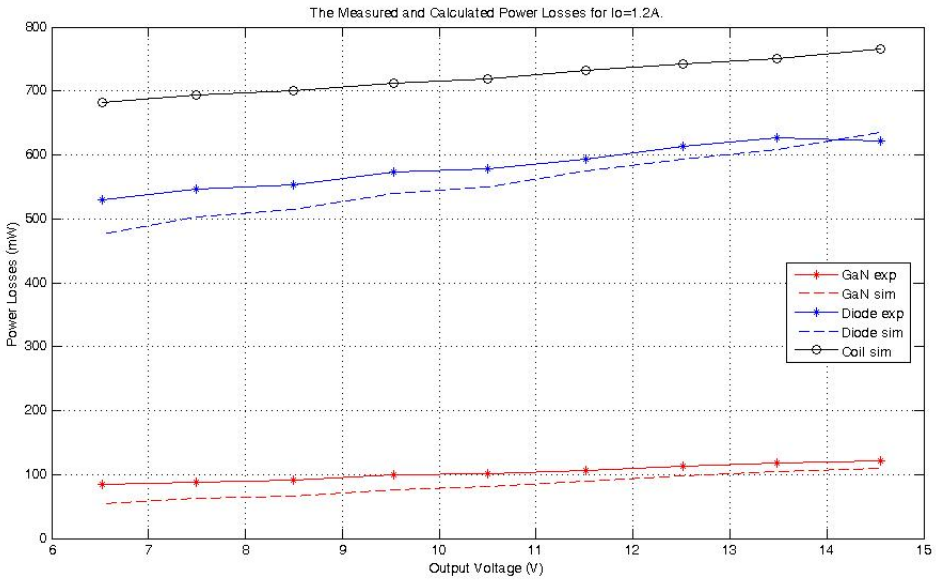


Figure 4.18: The experimental and simulated power losses for the three main components of the converter at Io=1.2A.

Finally, it is considered useful to present here the experimental and simulation results on the values of duty cycle, frequency and peak inductor current for some operating points. Note that the values of the peak currents are rounded at the first decimal digit.

Operating values for different Vo and Io=1.2A					
V_o (V)	6.5	8.5	10.5	12.5	14.5
$f_{experimental}$ (kHz)	666.7	697.7	714.3	714.3	705.9
$f_{simulation}$ (kHz)	702.3	740.3	759.3	758.6	751.4
$D_{experimental}$	33.7	38.8	43.4	48.2	51.2
$D_{simulation}$	32.9	38.4	43.1	47.2	50.8
$I_{Lpk,experimental}$	3.9	4.4	4.8	5.3	5.7
$I_{Lpk,simulation}$	3.8	4.2	4.6	5.1	5.5

Table 4.4: Various operating values from the experimental and simulation results for 1.2A.

Operating values for different Vo and Io=1A					
V_o (V)	6.5	8.5	10.5	12.5	14.5
$f_{experimental}$ (kHz)	759.5	789.5	833.3	833.3	821.9
$f_{simulation}$ (kHz)	802.1	839.6	885.2	887.9	878.4
$D_{experimental}$	33.3	38.7	43.7	47.9	50.5
$D_{simulation}$	32.6	38.3	42.8	46.8	50.2
$I_{Lpk,experimental}$	3.5	3.9	4.1	4.5	4.8
$I_{Lpk,simulation}$	3.3	3.7	3.9	4.3	4.6

Table 4.5: Various operating values from the experimental and simulation results for Io=1A.

Comments on the Experimental and Simulation Results

Using the previous results some conclusions can be drawn as regards the final converter prototype, the analytical model that was used for the simulations and their differences between them. These conclusions are summarized here.

- From the previous figures it is obvious that the efficiency of the converter increases with the output voltage. This result, which is verified both from the experimental and the simulation results, is expected. The reason is that in order to increase the voltage the duty cycle needs to be increased which means that the time that the diode needs to conduct decreases and that the peak current of the inductor increases. Concurrently, the power delivered to the output increases. In total, the increase on the losses on the diode and the inductor (which are the components with the higher losses) is smaller compared to the increase of the output power and this can be seen when comparing the slope of the graph of the efficiency and the temperature. This results to an increasing efficiency with the increase of the voltage. Note that the slope of the efficiency decreases for higher voltages which means that this pattern changes after a certain voltage value (which is out of the operating rage of the converter) and the efficiency decreases with increasing voltage.

  It is interesting to mention that while the operating voltage increases the turn on losses of the GaN switch decrease since the drain voltage approaches zero when the switch turns on. This hardly has any influence on the converter efficiency since the switch losses are very small compared to the diode and the coil losses (see figures 4.17 and 4.18).

- The measured temperature on the diode component is very close to the calculated with the maximum deviation being smaller than 5^oC. It is expected that the

actual junction to ambient thermal resistance is very close to the value used in the design procedure because the specifications given in the datasheet match to a great extend with the prototype specifications (1oz FR4, one layer PCB, with the recommended pad layout as specified in the datasheet). As a result of this, the calculated losses seem to be very close to the actual losses. This can be expected if we consider the small deviation of the experimental and the simulation results on the values of duty cycle, peak inductor current and frequency value presented at tables 4.4 and 4.5 . These small differences contribute to the deviations of the losses on the diode.

- A larger difference between the experimental and the simulation results can be seen at the GaN temperature and losses compared to the diode. Despite that difference the component still operates into the specified thermal limits. It is not very simple to locate the main reason of this deviation since the calculated operating temperature depends on the accuracy of the developed analytical model, the value of the used thermal resistance at the design procedure and the operating points.

  The thermal resistance that was calculated using the equivalent thermal model certainly gives much more accurate results compared to the results when using the value from the datasheet. It can be assumed that this value is a good approximation of the real value of the thermal resistance. Of course, some inaccuracies are also expected at the used analytical model mainly because of the non linearity of the parasitic capacitances. According to the model, the high values of the parasitic capacitances result to a zero channel current during the turn off transient and, thus, to very small turn off losses (compared to the turn on losses). In reality, however, the capacitances depend on the drain voltage which means that the channel current might not be zero for the whole time that is assumed in the model. Also, the non linearity assumption has significant influence on the turn on transient where the losses equal the stored energy in the capacitance which is assumed to be constant, an assumption that does not hold. This is probably one of the reasons that at lower voltages we observe higher deviation between the experimental and simulated GaN losses (the voltage across the switch, during the valley switching, is larger compared to higher voltages). Finally, the differences at the operating values presented at the previous tables are expected to contribute to the losses deviations, but not significantly.

- It is interesting to notice that the efficiency of the prototype converter is 1-3% (percentage units) higher than the results of the simulations. This has an explanation. The major losses of the converter lay on the coil and the diode with the losses on the GaN being the least significant. At the first conclusion it was stated, based on the results, that the diode losses for the experimental and simulated converters are very close, with the former being slightly higher. Because the influence of the losses of the GaN switch are not as significant as the diode's and the inductor's it can be concluded that the major reason for the deviation between the experimental and the simulated efficiency is the calculation of the discrete coil losses, which were overestimated. Since the ac losses were calculated using the measured ac resistances of the component it is clear that the deviation comes from the calculation of the core losses. The fact is that for the calculation of the core losses of the discrete inductor the specific power loss was used and it was extracted from the corresponding figure of the datasheet. This figure, however, presents the results for a temperature of 100^oC and for specific frequencies. The required value, therefore, was crudely approximated resulting to this inaccuracy.

Chapter 5

Conclusions & Suggestions for Future Work

5.1 Conclusions

The main objective of this master thesis project was to build a low profile dc/dc converter capable of driving OLED lights according to the specifications of the Audi Lighting Department using GaN switches to assist towards this direction. The design procedure of the converter, the resulting prototype and the experimental measurements were presented and discussed at chapters 3 and 4. Based on the final prototype and the experimental results and comparing them with the initial requirements and thesis objectives an assessment of the converter can be attempted and some conclusions can be drawn. These are summarised here:

- As regards the electrical and thermal specifications, that were defined at the beginning of this thesis, it could be said that the converter complies quite well to them. Normal operation at all possible operating points within the thermal limits (with natural convection cooling) is ensured, at least as regards the temperature rise of the components, while a decent efficiency for a buck-boost topology at relatively high frequencies (up to 830kHz), ranging from 89% to 92%, is achieved. Of course, in order to verify its capability to operate from -40^oC to 85^oC special thermal measurements at these temperatures should be conducted.

- As regards the size, the specifications of the application required low-profile, minimised and flexible converter. Due to the relatively high operating frequency the passive components were minimised as much as possible, considering the temperature limits which were a break towards this direction and the available magnetic materials, but certainly further miniaturization could be achieved provided that more suitable magnetic materials were available. Even with the discrete component the converter maintains a relatively low profile but flexibility is not achieved, at least for the magnetic component, as it can be with the planar one. The PCB prototype could also be smaller if both sides were exploited - in that case for the ease of measurements only one side was used.

- The contribution of the use of the GaN device at this application also became quite clear. First of all, the use of this switch allowed for an unobstracted high frequency operation which led to a small inductance value resulting to both decently small planar coil and an also small discrete magnetic component. This high frequency operation, which is also possible with some Mosfet devices, was also accompanied with low losses on the switch -attributed to the very low $R_{ds,on}$ and small Miller

capacitance of the GaN device and, of course, the valley switching operation - , low parasitic inductance of the component due to the LGA packaging of the GaN and high maximum junction temperature (150^oC) of the device which allowed for higher margin of the losses (and thus the frequency) at this thermally demanding application. Very important feature of the device, that makes it very suitable for such an application, is the high power density that it achieves. This device is a very low profile component (1.7mm x 1.1mm x 0.82mm) with significant power rating considering its size (max: 40V x 10A) and in combination with the previous characteristics makes it very unique and very promising for this kind of applications. Even its cost, which could be considered a possible drawback, is currently not at all higher than the Mosfets of the same feature. Finally, the GaN-specific drivers that are already commercial resolve the driving issues of this components.

- The analytical model that was used for the calculation of the switching losses of the GaN device gave quite accurate results, as it can be realised at chapter 4. However, for better verification of the accuracy of the switch loss analytical model it is required more accurate calculation of the thermal resistance (junction-to-ambient) of the GaN and better approximation of the parasitic capacitances and inductances that influence the transient, using more specialised software tools. In that case the assessment of the accuracy of the model would be certainly more robust.

- In that application the discrete magnetic component showed better behaviour compared to the planar one. However, in case that flexible cores with somewhat higher permeability, probably around 3-4 times higher, were available it is expected that the planar coil would have had quite smaller size which would certainly result to much better efficiency. In that case the planar coil would certainly be the choice for this application.

5.2 Suggestions for Future Work

At this paragraph some suggestions for future work are taking place.

- As it has already been stated, GaN devices are very good candidates for low profile and high density applications, like the OLED driving which was investigated at this project, because of their very attractive features which have been described. However, for optimal utilization of these switches analytical switch loss models, like the one presented in Chapter 3, need to be used during the design procedure but significant effort should be given in accurately defining (to the extend that is possible, of course) the parasitic values of the component and the thermal resistances. This is important especially in case an optimization method is used during the design procedure. Using specialised tools or developing analytical methods which could give good approximations of these values could help significantly towards this direction. This also means that the iterative loop of the design procedure should "close" not before but after the PCB layout design, otherwise this kind of valuable parameters cannot be calculated.

- In such kind of applications, where the magnetic component needs to be minimized it is important to have an extended view of the available magnetic materials. This means that more investigation on the available magnetic materials is necessary. The fact is that, currently, the variety of the flexible magnetic cores is limited and mainly used for EMI shielding but technology always progresses and new opportunities arise. This could lead to new possibilities for minimizing and achieving flexibility to magnetic components, pushing forward low profile high power density applications.

- Finally, in applications over approximately 200kHz EMI analysis is necessary. In this project this concept was overlooked due to the limited time but it is an essential part , and quite demanding sometimes, in high frequency applications.

Appendix A

Calculation of the convection coefficient h

The topic of the calculation of the convection coefficient approaches the computational fluid dynamics (CFD)and thermal analysis. The equations that are presented here can be found in every related literature or in related websites. For the calculation of the coefficient h it is necessary to find the value of the Rayleigh number which equals:

$$R_a = G_r \cdot P_r \tag{A.1}$$

where G_r is the Grashof number which is equal to:

$$G_r = \frac{L^3 \cdot g \cdot \beta \cdot (T_w - T_{inf}}{v^2} \tag{A.2}$$

where L[m] is the characteristic length, g$[m/s^2]$ is the gravitational acceleration, $\beta[1/K]$ is the thermal expansion, v$[m/s^2]$ is the kinematic viscosity of the fluid. For perfect (ideal) gases it is $\beta = \frac{1}{T_f}$ where $T_f = \frac{T_w + T_{inf}}{2}$ is the film temperature. T_w is the temperature of the wall (temperature on the surface) which in our case was found using the thermal camera and was taken equal to 333K (60^oC for all cases) and $_{inf}$ is the temperature of the free stream of fluid (temperature far from the heated surface).

P_r is the Prandtl number which is equal to :

$$P_r = \frac{c_p \cdot \mu}{k} \tag{A.3}$$

where k$[W/(m \cdot K)]$ is the fluid (air in our case) thermal conductivity, $c_p[J/KgK]$ is the fluid specific heat and $\mu[Kg/ms]$ is the dynamic viscosity of the fluid.

All the previous parameters can be easily found for the air at related tables in the literature.

Finally, the Nusselt number is given by the following equation

$$Nu = \frac{\bar{h} \cdot L}{k} \tag{A.4}$$

For horizontal surfaces, like in our case, the characteristic length equals to $L = \frac{A}{P}$ where A is the area of the surface and P its perimeter.

For the upper surface of the heated plated the relation between the Nusselt and the Rayleigh number is:

if $10^4 \leq Ra \leq 10^7$

$$\bar{Nu} = 0.54 \cdot Ra^{1/4} \tag{A.5}$$

if $10^7 \leq Ra \leq 10^11$

$$\bar{Nu} = 0.15 \cdot Ra^{1/3} \tag{A.6}$$

For the lower surface of the heated plated the relation between the Nusselt and the Rayleigh number is:

if $10^5 \leq Ra \leq 10^10$

$$\bar{Nu} = 0.27 \cdot Ra^{1/4} \tag{A.7}$$

Using the previous equations the h coefficient can be approximated.

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