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***Index Terms*—Buck converter, Silicon Carbide (SiC), MOSFET, Triangular Current Mode, ZVS converters**

***Abstract*—Series-connected MOSFETs with lower voltage ratings can be an alternative for single high-voltage switches. This paper compares two switch configurations for the soft-switched power converter topology targeted for a 1400V DC grid. The first configuration is a single switch rated at 1700V whereas the other is a series connected two MOSFETs rated at 900V. A buck converter with 1400V and 700V as input and output voltages respectively is taken as a case study. Triangular current modulation (TCM) ensures zero voltage switching (ZVS) at turn-on for all the switches. The analysis shows that the series-switch configuration can have much lower overall losses than the single-switch configuration.**

I. Introduction

Climate change is currently one of the main problems facing the human population. Greenhouse gas (GHG) emission is considered one of the main reasons. The electrification of processes and the use of renewable energy resources like solar, wind, and batteries are being considered to reduce greenhouse gas emissions. Furthermore, DC grids will become ubiquitous since most renewable energy resources are DC. This is especially true for rural grids where the penetration of electric grids is still low [1].

The DC grids can be unipolar or bipolar. A unipolar dc (UDC) grid has two conductors. On the other hand, a bipolar dc (BiDC) grid has three conductors. The two grids are illustrated in Fig. 1. The UDC grid has a lower number of conductors. However, the conductor insulation requirements are high because the cable is exposed to the complete pole-to-pole voltage in case of a fault. On the other hand, a BiDC grid has three conductors with the mid conductor usually grounded. Therefore, only half of the pole-to-pole voltage is imparted on the cable in a pole-to-ground fault.

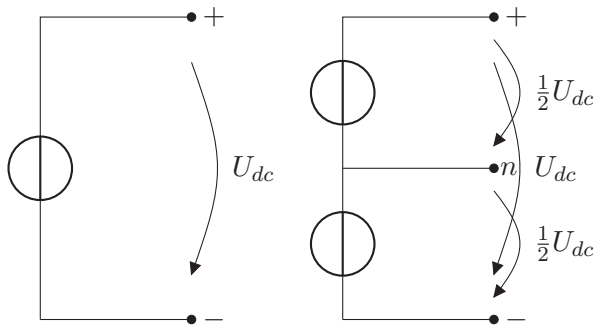

Fig. 1. Left: Unipolar DC grid; Right: Bipolar DC grid.

The Dutch standard on low-voltage DC grids, NEN NPR 9090, proposes the following voltage and corresponding power levels for 16 A of current flow for UDC and BiDC grids [2].

SiC-based switches are being used to create more efficient converters that can switch at a much higher frequency than Si MOSFET and IGBT. Commercially,

TABLE I
VOLTAGE LEVELS PROPOSED BY NEN NPR 9090 STANDARD.

UDC Voltage (VDC)	BiDC Voltage (VDC)	Power (kW)
350	-	5.6
700	± 350	11.2
1400	± 700	22.4

these switches are available at voltage ratings ranging from 650V up to 3.3kV. The switch rating is dependent upon the chosen topology and grid voltage levels. When working with 350V, switches with several voltage ratings can be used. However, for higher voltages, the switch options become limited. In this work, we consider the 1400V level grid. For this voltage level, only 1700V and 3300V switches can be used for the standard half-bridge configuration. Furthermore, due to higher margins 3300V switches will not be a cost-effective solution. Therefore, 1700V is the only possible voltage rating. When higher voltage switches are used, their C_{in} and stored gate charge (Q_g) increases. Hence, the Baliga figure of merit (f_B) value [3] becomes lower thus indicating higher losses. The Baliga figure of merit (FOM) is given by (1).

$$f_B = \frac{1}{R_{ds} C_{in}} \tag{1}$$

This FOM was later revised to include Q_g instead of C_{in} [4]. An alternative to a single 1700V switch is two lower voltage ratings (e.g., 900V) in series. Table II shows the FOM for SiC switches from the same manufacturer with different voltage ratings. The 1700V switches are compared with a series connection of two 900V switches.

TABLE II
COMPARISON OF FOM FOR DIFFERENT SIC SWITCHES.

Switch	Rated voltage (V)	R_{ds} $(m\Omega)$	Q_g (nC)	FOM $(\Omega C)^{-1}$
C3M0030090K	900	30	87	3.83e+08
C2M0045170D	1700	45	200	1.11e+08

It can be seen that the FOM of the 900V switch is much higher than the 1700V switch. Therefore, it indicates that the series-connected low-voltage switches can provide better loss performance than a single high-voltage switch. However, this claim needs to be substantiated with analysis. This comparison is the main contribution of this paper.

The rest of the paper is organized as follows. The topology description is given in section II. This is followed by the loss modeling of a generic half-bridge consisting of two semiconductor switches in section III. Then, a qualitative comparison of the switch configurations is given in section IV. This is followed by a case study of a 1400V to 700V buck converter using the generic half bridge in section V. Finally, the paper is concluded in section VI.

II. TOPOLOGY DESCRIPTION

In this paper, we limit our discussion to a standard half-bridge configuration which is the building block for many converters such as buck, boost, and buck-boost. The half-bridge configuration is shown in Fig. 2.

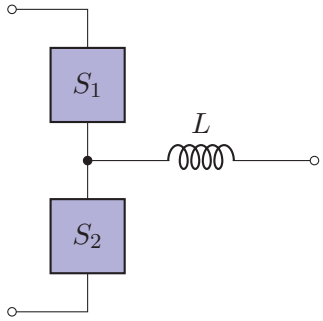

Fig. 2. Standard half-bridge configuration.

S_1 and S_2 represent the top and bottom switch blocks, respectively. L is the inductor connected to the midpoint of the half-bridge leg. The switch blocks can be single high voltage or series-connected switches as shown in Fig. 3.

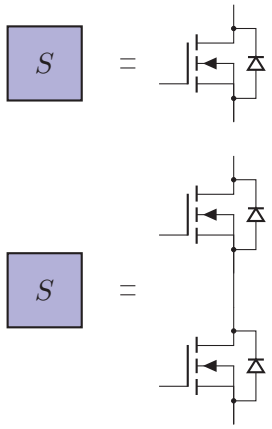

Fig. 3. Up: Single switch; Down: Series connected switch.

The half-bridge topology can exhibit zero voltage switching (ZVS) in the whole operating range

by choosing an appropriate switching frequency [5]. The switching frequency is changed according to the required load current. To achieve ZVS turn-on, a minimum inductor current should discharge the output capacitance (C_{oss}) of the switch during the dead time before it is turned on. This minimum current is given by

$$I_{oss,min} = V_d\sqrt{\frac{8}{3}\frac{C_{oss}}{L}} \tag{2}$$

where V_d is the input voltage of the half-bridge and L is the inductor connected to the mid-point of the half-bridge. If the minimum current condition is met, another condition checks whether the dead time is sufficient to discharge the switch before it is turned on fully. The maximum dead time required to ensure that the switch is fully discharged is given by

$$dt_{max} = \frac{C_{oss}V_d}{I_{oss,min}} \ . \tag{3}$$

By ensuring sufficient inductor current and dead time, the ZVS turn-on of the switches can be guaranteed. Hence, for the rest of the paper, the turn-on switching loss is neglected under all the operating conditions.

III. Loss modeling

The losses in the semiconductor component of the half-bridge can be broadly categorized as conduction loss and switching loss. The conduction loss of MOSFET is defined as the loss that occurs during the steady-state condition of the device. The conduction power loss can be modeled using the MOSFET's equivalent on-resistance as shown in (4) where, $P_{MOS-conduction}$ is the MOSFET Conduction Loss, I_{Drms} is the drain RMS Current, R_{DSon} is the equivalent drain to source resistance and n is the number of MOSFETs connected in series.

$$P_{MOS-conduction} = nI_{Drms}^2 R_{DSon} \tag{4}$$

The expression of the RMS current for a buck-type half-bridge configuration is given by

$$I_{Drms} = \sqrt{D\left({I_{\text{out}}}^2 + \frac{\Delta I_L^2}{12}\right)} \tag{5}$$

where, I_{out} is the average load current and ΔI_L is the inductor ripple current.

The switching losses of the MOSFET are defined as the losses that occur during the dynamic transition from the conduction state to the blocking state and vice versa. The switching power losses of the MOSFET are modeled using (6) where E_{on} and E_{off} are the turn-on and turn-off switching losses of the MOSFET respectively, and f_s is the converter's switching frequency.

$$P_{MOS-switching} = n(E_{on} + E_{off})f_s \tag{6}$$

For the turn-on operation of the MOSFET, the ZVS technique was employed, that is, it is ensured that the voltage across the MOSFETs drops to zero before a gate pulse is provided to turn on the MOSFET. For this, a negative current I_{oss} is set to discharge the C_{oss} and achieve ZVS. Thus, during turn-on, there will be no loss in the MOSFET, so E_{on} is neglected.

IV. Comparison of two methods

A. Cost comparison

The cost of the power stage mainly consists of the semiconductor switches, the gate driver circuitry, and the heatsink necessary for dissipating the losses in the switches. According to the authors' observations, for similar effective $R_{DS,on}$ values of the two switch configurations, the prices of the switches are comparable. For example, on 28 February 2023, the price of a single-piece 900V C3M0030090K switch is approximately 32 euros, and that of the 1700V C2M0045170P switch is approximately 80 euros. Hence, two lower voltage switches would be a cheaper solution. The two switches would also incur additional costs for the double amount of gate driver circuitry. Lastly, the heat sink costs depend on each switch's losses. For the double switch configuration, the losses are spread in multiple switches having a higher case-to-sink area. On the other hand, the single switch would have a lower case-to-sink surface area to dissipate the losses. Depending on the amount of losses from the application, the size of the heat sink required can be different for the different switch configurations.

B. Power density

The area for the double switch configuration will be approximately double that of the single switch configuration. This is due to the replication of the half-bridge configuration. The volumetric power density of the converter depends on the losses because the size of the heatsink greatly changes it.

V. Case study

To evaluate and compare the losses of a series-connected switches half-bridge configuration and a single switch half-bridge configuration, the switching

circuit setup shown in Fig. 4 has been used where, V_d is the input voltage, S1 and S2 are the test switches, L is the inductance, C_{dc} is the capacitance and I_{out} is the average output current.

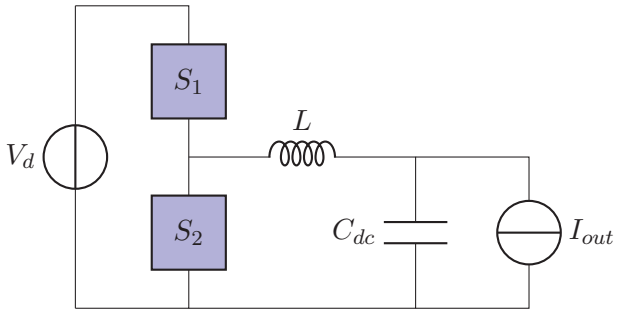

Fig. 4. Test scheme used to compare the two switch configurations.

The buck converter topology operates at 0.5 duty cycle, thus stepping-down the voltage from 1400V to 700V. The inductor chosen has a value of 700 μH. The DC link capacitance has a value of 1 μF. The converter parameters are summarized in table III.

TABLE III
CONVERTER PARAMETERS FOR THE CASE STUDY.

Parameter	Value	Unit
Input voltage	1400	V
Output voltage	700	V
L	700	μH
C_{dc}	1	μF
Power	5.5	kW
Max I_{out}	8	A

MOSFETs C2M0045170P and C3M0030090K were adopted for single and series-connected configurations respectively. The main parameters for the two switches are given in table IV. Using (2), the minimum current required to discharge the switches are also given in the table.

TABLE IV
SWITCH PARAMETERS.

Parameter	C3M0030090K	C2M0045170D	Unit
Rated Voltage	900	1700	V
$R_{DS,on}$	30	45	$m\Omega$
C_{oss}	144	171	pF
Package	TO-247-4	TO-247-4	-
I_{oss}	0.518	1.13	A

As discussed, TCM ensures the ZVS turn-on of the two switches in the half-bridge. An illustration of the modulation scheme and inductor current is provided in Fig. 5. The minimum current required to discharge C_{oss} of the switches is represented by I_{Lmin}. When this current is reached, S_2 is turned off. In this instance, the turn-off losses are incurred in S_2. During the dead time, the current flowing through the inductor (I_{Lmin}) discharges the C_{oss} of S_2 and prepares it for ZVS turn on. Thus, no turn-on losses occur for S_1. The current now increases to I_{Lmax} and at $0.5T_s$, S_1 is turned off. In this instance, turn-off losses occur in S_1. During the dead time, the inductor current discharges the C_{oss} of S_2 and prepares it for ZVS turn on. Hence, no turn-on losses occur in S_1 as well.

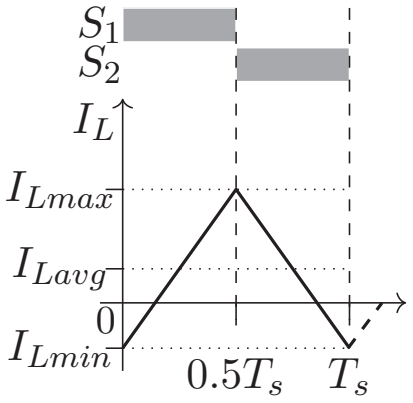

Fig. 5. Triangular current modulation.

The average inductor current (I_{Lavg}) is also the output current of the converter (I_{out}). With the duty cycle fixed at 0.5, the output current of the converter can be varied by changing the converter's switching frequency. For a required I_{out}, the value of I_{Lmax} is given in (7).

$$I_{Lmax} = 2I_{out} - I_{Lmin} \tag{7}$$

The I_{Lmin} value is fixed with changing output current. However, the values of I_{Lmin} are different for the two switch configurations as given in table IV. Using (7) and the volt-second balance rule for the inductor, the switching frequency at equilibrium for different can be found using (8).

$$f_s = \frac{V_d - V_{out}}{4L(I_{out} - I_{Lmin})} \tag{8}$$

The values of the different switching frequencies for the switch C3M0030090K and C2M0045170P are given in tables V and VI, respectively. Using (**??**),

the conduction losses for the two switch configurations can be found. These are shown in Fig. 6. Firstly, the range of switching frequency is different for the two switches. This is because, for the same I_{out}, the different I_{Lmin} values for the two switch configurations will result in different f_s values according to (8). Second, it can be observed that the conduction losses of the series configuration are higher than those of the single switch for all the operating points. This is because the cumulative resistance of the series configuration is higher than that of the single switch.

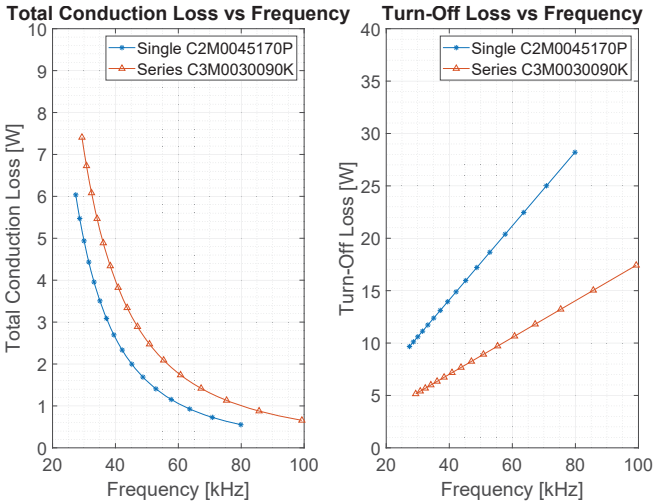

Fig. 6. Conduction and Turn-off loss vs. Frequency for single and series connected MOSFET

To calculate the turn-off losses, finding the energy dissipated in the switches is necessary. The turn-off energy for the two switch configurations was found using double pulse test simulations in LTSpice for different inductor current values. The results of the simulation consisting of energy dissipated for different inductor currents are given in table VII in the appendix. The switch turn-off losses can be calculated using this data and the switching frequency. These are shown in Fig. 6. It can be observed that the turn-off energy losses for the single switch are much higher than those of the series switches combined. This is because of the higher stored energy in the single switch which needs to be dissipated during turn off.

The sum of the conduction and switching losses for the two switch configurations is shown in Fig. 7. The total switch loss (sum of conduction and turnoff loss) for a single MOSFET is much higher than for a series-connected MOSFET. This can lead to a much lower power density of the power stage for the series configuration as the heat sink requirements are considerably reduced. Figure 8 shows the power state of the half-bridge, including the switches and gate drivers, designed in KiCAD. The dimension for the designed area is 47mmx72mm. The area of the series switch configuration would be double this at 47mmx144mm. Hence, the improvement in power density of the converter can be offset by this loss due to the increased area.

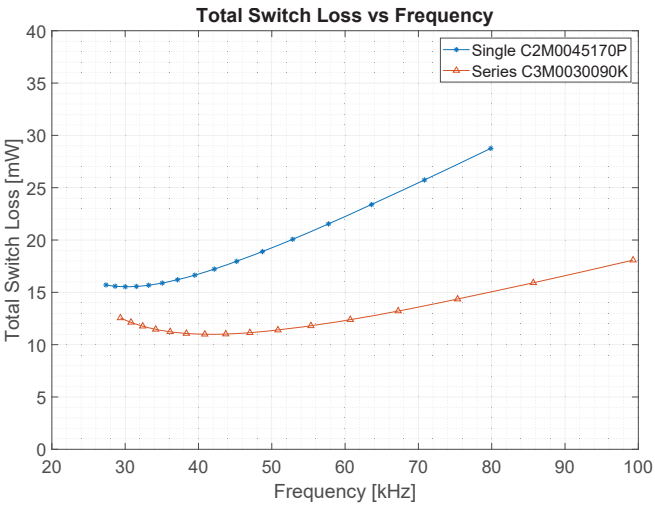

Fig. 7. Total switch loss vs. Frequency for single and series connected MOSFET

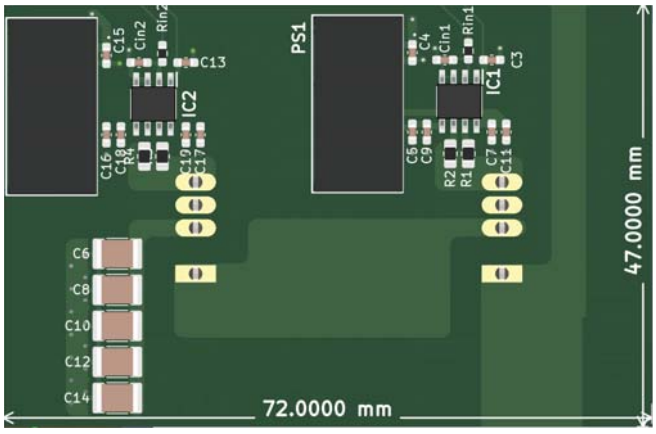

Fig. 8. Area (47mmx72mm) taken by single switch configuration

VI. Conclusion

In this work, we show that for a standard half-bridge configuration, using two series connected low-voltage MOSFET can be beneficial compared to a single switch of high-voltage rating. With TCM, the turn-on losses can be eliminated, and the turn-off losses are lower for a higher operating frequency for the series connected MOSFETs. The benefit is sufficient

to compensate for the increased $R_{DS,on}$ of the series connection of MOSFETs.

However, this increase in performance comes at a price. First, with TCM, the ripple current of the inductor is 100%. Hence, the losses in the inductor can be higher. However, the size of the inductor will be lower to accommodate the ripple current. The high ripple current also leads to high DC link capacitor sizing. Therefore, the overall power density can be quite low. Other challenges with the series connection of MOSFETs are explained in the next subsection.

A. Non-idealities of series connected configuration

In addition to the challenges mentioned above, the other major drawback of using the series connection of MOSFETs is the non-idealities associated with them, resulting in non-uniform behavior. Major non-linearities include a mismatch in gate driver signal due to variation in gate driver device parameters, non-uniformity arising from parasitic capacitance of device and surroundings, and non-uniformity in device parameters such as gate resistance, etc. All these non-linearities adversely affect the voltage sharing across the series-connected MOSFETs thus resulting in unbalanced voltage distribution and, subsequently may lead to device failure.

Multiple control techniques have been proposed in the literature to account for and ensure equal voltage distribution across series-connected MOSFETs. The most prominent methods are divided into three categories: passive snubber circuits [6]–[10], active voltage clamping [11]–[13], and active gate control [14]–[17] techniques. Using RC and RCD snubber circuits for voltage balancing across series-connected MOSFET and providing dynamic voltage sharing between rows of power semiconductors linked in series is a popular choice because of its simplicity, reliability, and low cost.

However, the available literature is scarce and does not account for voltage balancing across series-connected MOSFETs operated with ZVS turn-on. Hence, in future work, it is recommended to design a converter that combines the benefits of using ZVS at turn-on and the snubber circuit to control the distribution of voltages across the switches in series.

B. Future work

The analytical results obtained for this work show promising results in using a series-connected MOSFET half-bridge configuration compared to a single MOSFET configuration and thus need to be experimentally validated as the next step in this direction. Also, modifying the passive snubber circuit voltage control technique would ensure a balanced and equally distributed voltage across the series-connected switches operating with ZVS turn-on.

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APPENDIX

TABLE V
EXPERIMENTAL DATA FOR A SERIES CONNECTED MOSFET (C3M0030090K) HALF-BRIDGE SYNCHRONOUS BUCK CONVERTER

MOSFET: C3M0030090K			
I_{out} **[A]**	**f [kHz]**	I_{Lmax} **[A]**	I_{Lmin} **[A]**
2	99.28515	4.518	0.518
3	71.0631	6.518	
4	55.33422	8.518	
5	45.30627	10.518	
6	38.35532	12.518	
7	33.25352	14.518	
8	29.34961	16.518	

TABLE VI
EXPERIMENTAL DATA FOR A SINGLE MOSFET (C2M0045170P) HALF-BRIDGE SYNCHRONOUS BUCK CONVERTER

MOSFET: C2M0045170P			
I_{out} **[A]**	**f [kHz]**	I_{Lmax} **[A]**	I_{Lmin} **[A]**
2	79.8722	5.13	1.13
3	60.53269	7.13	
4	48.73294	9.13	
5	40.78303	11.13	
6	35.06311	13.13	
7	30.75031	15.13	
8	27.38226	17.13	

TABLE VII
TURN OFF ENERGY LOSSES FOR THE TWO SWITCHES IN μJ. THE ENERGY LOSSES FOR THE SERIES CONFIGURATION ARE THE SUM OF THE ENERGY LOSS IN TWO SWITCHES.

Current (A)	C2M0045170P	C3M0030090K (2 switches)
1	175.68	87.194
2	175.86	87.103
3	176.02	86.04
4	176.28	86.97
5	176.24	86.828
6	176.41	86.95
7	175.92	87.769
8	175.3	88.408
9	175.77	88.409
10	176.67	87.442
11	176.9	88.211
12	177.09	87.818
13	177.65	88.37
14	177.29	88.713
15	178.2	88.83
16	177.78	88.79