Variable-Frequency Soft-Switching Modulation of Non-Isolated DC-DC Converters and Compensation Circuits in WPT Systems

Yu, G.

DOI
10.4233/uuid:589f7376-57ef-4e2b-85f6-c79dc4b98a70

Publication date
2025

Document Version
Final published version

Citation (APA)
Yu, G. (2025). *Variable-Frequency Soft-Switching Modulation of Non-Isolated DC-DC Converters and Compensation Circuits in WPT Systems*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:589f7376-57ef-4e2b-85f6-c79dc4b98a70

Variable-Frequency Soft-Switching Modulation of Non-Isolated DC-DC Converters and Compensation Circuits in WPT Systems

Guangyao YU

Variable-Frequency Soft-Switching Modulation of Non-Isolated DC-DC Converters and Compensation Circuits in WPT Systems

Variable-Frequency Soft-Switching Modulation of Non-Isolated DC-DC Converters and Compensation Circuits in WPT Systems

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
Chair of the Board for Doctorates,
to be defended publicly on
Wednesday 10, September 2025 at 10:00 o'clock

by

Guangyao YU

Master of Science in Electrical Engineering,
Delft University of Technology, The Netherlands,
born in Zhejiang, China.

This dissertation has been approved by the promotors.

Composition of the doctoral committee:

Rector Magnificus,	Chairperson
Prof. dr. ir. P. Bauer,	Delft University of Technology, promotor
Dr. J. Dong,	Delft University of Technology, promotor
Independent members:	
Prof. dr. ir. M. Popov,	Delft University of Technology
Prof. dr. ir. A.H.M. Smets,	Delft University of Technology
Prof. dr. D. Peftitsis,	Norwegian University of Science and Technology
Dr. ir. P. Venugopal,	University of Twente
Dr. ir. B.J.D. Vermulst	Eindhoven University of Technology

ISBN 978-94-6384-809-1

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

To my family

Contents

Summary

Charging electric vehicles (EVs) via wireless power transfer (WPT) has emerged as a novel charging concept in recent years. Although the efficiency of the WPT charging featuring series-series (S-S) compensation has reached a very high level thanks to optimized magnetic coupler design, it is still sensitive to different operating conditions such as coupling coefficient. In order to enable efficient wireless power charging for EVs over a wide operational range, and to meet the charging requirement, additional power conversion control is needed. Meanwhile, the electrical stresses and current distortion in compensation circuits are also critical for the efficient and safe operation.

For a basic wireless power transfer system mentioned in many references, it typically includes at least two power conversion stages, which are dc-ac inversion stage and ac-dc rectification stage. The dc-ac stage converts the dc power source into high-frequency ac source to drive the primary coil while the ac-dc stage converts the ac current received by the secondary coil into dc source. In Chapter 2, a review on state-of-the-art WPT charging system topology has been conducted. Based on this review, it can be concluded that practical WPT charging systems usually have multiple power conversion stages, but it is difficult to conclude which is the best power conversion configuration and topology choice.

In this thesis, a WPT charging system featuring LCC-S compensation and a back-end FSBB converter was chosen as the research object, and this is based on the consideration of the following factors: 1) Compared with front-end power regulation, back-end power regulation avoids communication between primary and secondary sides during charging, which helps improve the system reliability; 2) From a safety perspective, an LCC-S based WPT system allows operation without a secondary coil or with an open circuit on the secondary side, which has a built-in safety advantage over S-S compensated WPT system; 3) Since the WPT coils already provide electrical isolation, a non-isolated dc-dc converter can be simply used to achieve dc voltage conversion. Compared to traditional boost or buck converters, the FSBB converter offers both voltage boost and buck functionality, making it more versatile and better suited for wireless charging systems.

The main research content of this thesis is divided into two parts. The first part delves into the four-switch buck+boost (FSBB) converter, which functions as an additional power conversion stage in the wireless charging system. Comprehensive and detailed analysis on the soft-switching modulation strategy on this converter was investigated and presented. The second part focuses on accurate modeling of electrical stresses and current distortion phenomenon for compensation topologies.

Soft-Switching Modulation of FSBB Converter

This part focuses on the soft-switching modulation of the FSBB converter in order to achieve high-efficiency wide-range operation. At present, although hard-switched dc-dc converter can also reach peak efficiency above 99%, the switching losses cannot be

eliminated, which poses a challenge to the high-frequency or even ultra-high-frequency operation of the converter. With increasing requirement for higher power density and higher operating frequency, soft-switching modulation becomes necessary. Particularly, in this thesis, the soft-switching technique of zero-voltage switching (ZVS) was studied.

In Chapter 3, a three-mode variable-frequency ZVS modulation was proposed for the FSBB converter. The converter operation is subdivided into three operating regions according to the converter static voltage gain, i.e., buck-, buck-boost- and boost-type modes. Triangular current mode (TCM) modulation was adopted for buck-type and boost-type modes while in buck-boost-type mode when the voltage gain is close to unit, three-segment inductor current mode modulation was selected as the optimal modulation technique in terms of inductor rms current reduction and ease of operation. A 300–600 V input, 400 V output, 3 kW laboratory prototype was built to evaluate and validate the proposed concepts. The converter was tested over a wide power range from 10% to full rated load. The measured efficiency was always higher than 99%, i.e., between 99.2% and 99.6%, from 1 to 3 kW for all the considered input voltages.

In Chapter 5, a single mode variable-frequency ZVS modulation was proposed. In this modulation method, the control variables of duty cycle and switching frequency are continuous at the unit voltage gain boundary, which is different from the three-mode variable-frequency ZVS modulation method. Basically, the three-segment inductor current mode modulation was extended to the whole operational range. By fixing the duty cycle for the switch in the buck-type or boost-type half-bridge circuit, and controlling the duty cycle of the switch in the other half-bridge circuit, the FSBB converter can realize a smooth transition at the unit voltage gain boundary without compromising the inductor rms current compared with TCM-ZVS modulation. Based on this, a simple closed-loop control was presented without the need of inductor or switch current detection. In addition, the capacitance selection of input and output capacitors was also analyzed in detail. An FSBB converter was built and tested to validate the proposed concepts with an input voltage of 250–600 V, output voltage of 400 V and output power of 250–2500 W.

In fact, TCM-ZVS modulation can also be applied to the FSBB converter when input and output voltages are close, however, this will result in a large inductor rms current and is therefore not recommended in practice. For TCM-ZVS modulation, the reverse switching current through the inductor, which takes a negative value during the switching interval, is crucial for achieving soft switching for both switches in bidirectional buck, boost, and buck-boost converters. In an ideal situation without considering losses, this reverse switching current can be maintained at a constant value through variable-frequency technique, so the ZVS condition is always satisfied, however, this current value needs to be rethought in non-ideal situations because the decrease of this current (absolute value) could cause possible ZVS loss. Chapter 4 studied the parasitic resistance effects presented in the MOSFET switches and inductor on this reverse switching current for buck, boost and buck-boost converters under voltage-mode variable-frequency TCM-ZVS modulation respectively. Universal closed-form equations of the modified duty cycle and switching current were derived, which can be utilized to calculate the switching current under different operating conditions. The proposed analysis was evaluated and validated through an FSBB converter featuring TCM–ZVS buck, boost, and buck–boost operation capability. The operating voltage and power were from 100 V to 400 V, and 300 W to 1 kW,

respectively.

Compensation Circuits

This part focuses on the study of compensation circuits in terms of providing a more accurate calculation method for the electrical stresses in S-S and LCC-S compensated WPT systems, and a more accurate modeling on the current distortion in the LCC-S based WPT system.

Accurately determining the electrical stresses of the compensation components is an important step in designing a reliable WPT system. However, it was found that the peak voltage calculation is not accurate enough for certain components when applying first harmonic approximation (FHA) method to the equivalent ac circuit. More precisely, the peak voltage calculated for the primary coil and secondary coil in S-S compensation, and the peak voltage calculated for the input resonant inductor and secondary coil in LCC-S compensation contained large errors compared with simulation results. Due to the high accuracy of the rms current calculation, an improved peak voltage calculation method in closed form was proposed in Chapter 6 based on Kirchhoff's voltage law considering the voltage across the related compensation capacitors. The proposed analysis was validated by both simulation and experiments.

Due to the introduction of an additional LC branch in LCC-S compensation compared with S-S compensation, the current through the input resonant inductor has more distortion because of the influence from high-order harmonics. At the same time, the switching current through the input resonant inductor is closely related with the ZVS of the switches in the front-end H-bridge inverter. In order to calculate this switching current accurately, different from previous research, both the high-order harmonics from the primary and secondary sides were considered simultaneously in Chapter 7, and closed-form equations were derived. Unexpectedly, according to the analysis, the first-harmonic current also contributes to the switching current even for a fully compensated LCC-S based WPT system. The new method has shown an improved prediction of the switching current proved by simulation. However, it should be pointed out that the proposed analysis was based on the assumption that the square wave voltages on the primary and secondary sides are in phase, which requires further discussion.

Samenvatting

Het opladen van elektrische voertuigen (EV's) via draadloze stroomoverdracht (WPT) is de afgelopen jaren uitgegroeid tot een nieuw oplaadconcept. Hoewel de efficiëntie van het WPT-oplaadsysteem met serie-serie (S-S) compensatie dankzij geoptimaliseerd magnetisch koppelingontwerp een zeer hoog niveau heeft bereikt, is het nog steeds gevoelig voor verschillende bedrijfsomstandigheden, zoals de koppelfactor. Om efficiënt draadloos opladen van EV's over een breed operationeel bereik mogelijk te maken en aan de oplaadeisen te voldoen, is extra vermogensomzettingscontrole nodig. Tegelijkertijd zijn de elektrische spanningen en de stroomvervorming in de compensatiecircuits ook cruciaal voor de efficiënte en veilige werking.

Voor een basis draadloos energieoverdrachtsysteem, zoals vermeld in veel referenties, omvat het doorgaans ten minste twee vermogensomzettingsstadia: een dc-ac omzettingsstadium en een ac-dc gelijkrichtingsstadium. Het dc-ac stadium zet de dc-voedingsbron om in een hoogfrequente ac-bron om de primaire spoel aan te drijven, terwijl het ac-dc stadium de ac-stroom die door de secundaire spoel wordt ontvangen, omzet in een dc-voedingsbron. In Hoofdstuk 2 is een overzicht gegeven van de meest geavanceerde structuur van WPT-oplaadsystemen. Op basis van dit overzicht kan worden geconcludeerd dat praktische WPT-oplaadsystemen meestal meerdere vermogensomzettingsstadia hebben, maar het is moeilijk te concluderen welke de beste configuratie en topologie voor vermogensomzetting is.

In dit proefschrift is een WPT-oplaadsysteem met LCC-S compensatie en een back-end FSBB-omzetter gekozen als het onderzoeksobject, en dit is gebaseerd op de overweging van de volgende factoren: 1) In vergelijking met front-end vermogensregeling vermijdt back-end vermogensregeling de communicatie tussen de primaire en secundaire zijde tijdens het opladen, wat de betrouwbaarheid van het systeem helpt te verbeteren; 2) Vanuit veiligheidssperspectief stelt een LCC-S-gebaseerd WPT-systeem werking zonder een secundaire spoel of met een open circuit aan de secundaire zijde mogelijk, wat een ingebouwd veiligheidsvoordeel biedt ten opzichte van een S-S gecompenseerd WPT-systeem; 3) Aangezien de WPT-spoelen al elektrische isolatie bieden, kan eenvoudig een niet-geïsoleerde dc-dc-omzetter worden gebruikt om de gelijkspanningsomzetting te realiseren. In vergelijking met traditionele boost- of buck-omzetters biedt de FSBB-omzetter zowel spanningsverhoging als spanningsdaling, waardoor hij veelzijdiger is en beter geschikt voor draadloze oplaadsystemen.

De hoofdinhoud van het onderzoek in deze thesis is verdeeld in twee delen. Het eerste deel verdiept zich in de vier-schakelaar buck+boost (FSBB) converter, die fungeert als een extra vermogensconversiestap in het draadloze oplaadsysteem. Een uitgebreide en gedetailleerde analyse van de soft-switching modulatiestrategie voor deze converter werd onderzocht en gepresenteerd. Het tweede deel richt zich op de nauwkeurige modellering van elektrische spanningen en het fenomeen van stroomvervorming voor compensatietopologieën.

Soft-Switching Modulatie van FSBB Converter

In dit onderdeel ligt de nadruk op de soft-switching modulatie van de FSBB-converter om een hoogrendement en breedbandwerking te bereiken. Tegenwoordig kan een hard-switched dc-dc-omzetter hoewel ook een piekefficiëntie boven de 99% bereiken, de schakelverliezen niet worden geëlimineerd, wat een uitdaging vormt voor de hoge-frequentie of zelfs ultra-hoge-frequentie werking van de omzetter. Door de toenemende vraag naar hogere vermogensdichtheid en hogere bedrijfsfrequenties wordt zachte schakelmodulatie noodzakelijk. In dit proefschrift is met name de soft-switching techniek van nulspanningsschakeling (ZVS) bestudeerd.

In Hoofdstuk 3 werd een drie-modus variabele-frequentie ZVS-modulatie voorgesteld voor de FSBB-converter. De werking van de omzetter wordt onderverdeeld in drie werkingsgebieden op basis van de statische spanningsversterking van de omzetter, namelijk buck-, buck-boost- en boost-type modi. Voor de buck-type en boost-type modi werd TCM-modulatie (Triangular Current Mode) toegepast, terwijl in de buck-boost-type modus, wanneer de spanningsversterking dicht bij de eenheid ligt, drie-segment inductorstroommodusmodulatie werd geselecteerd als de optimale modulatietechniek in termen van reductie van de rms-stroom van de inductor en gebruiksgemak. Een laboratorium prototype van 300–600 V ingang, 400 V uitgang, 3 kW werd gebouwd om de voorgestelde concepten te bewijzen en te verifiëren. De omzetter werd getest over een breed vermogensbereik van 10% tot het volledige nominale vermogen. De gemeten efficiëntie was altijd hoger dan 99%, namelijk tussen 99,2% en 99,6%, van 1 tot 3 kW voor alle beschouwde ingangsspanningen.

Hoofdstuk 5 stelt single-mode ZVS-modulatie met variabele frequentie voor. Met deze modulatiemethode zijn de regelvariabelen van de duty cycle en de schakelingsfrequentie continu op de grens van eenheidsspanningsversterking, wat verschilt van de driemodus variabele-frequentie ZVS-modulatiemethode. In principe werd de drie-segmenten inductor stroommodus modulatie uitgebreid naar het gehele operationele bereik. Door de duty cycle voor de schakelaar in het buck-type of boost-type half-brug circuit vast te leggen en de duty cycle van de schakelaar in het andere half-brug circuit te regelen, de FSBB converter kan een soepele overgang realiseren bij de versterkingsgrens van de eenheidsspanning zonder dat dit ten koste gaat van de rms-stroom van de inductor, vergeleken met TCM-ZVS-modulatie. Een eenvoudige regelkring werd gepresenteerd zonder de noodzaak van detectie van spoel- of schakelaarkringstroom. Daarnaast werd de selectie van de capaciteit van de invoer- en uitvoercondensatoren ook in detail geanalyseerd. Een FSBB-converter werd gebouwd en getest om de voorgestelde concepten te verifiëren, met een invoerspanning van 250–600 V, een uitvoerspanning van 400 V en een uitgangsvermogen van 250–2500 W.

TCM-ZVS-modulatie kan feitelijk ook worden toegepast op de FSBB-converter wanneer de ingangs- en uitgangsspanningen dicht bij elkaar liggen. Dit resulteert echter in een grote inductor-rms-stroom en wordt daarom in de praktijk niet aanbevolen. Voor TCM-ZVS-modulatie is de omgekeerde schakelstroom door de inductor, die tijdens het schakelinterval een negatieve waarde aanneemt, cruciaal om zachte schakeling te bereiken voor beide schakelaars in bidirectionele buck-, boost- en buck-boost-omvormers. In een ideale situatie, zonder rekening te houden met verliezen, kan deze omgekeerde schakelstroom op een constante waarde worden gehouden door middel van een variabele-frequentietechniek, de ZVS-voorwaarde is dus altijd vervuld. In niet-ideale situaties moet deze stroomwaarde

echter opnieuw worden bekeken, omdat de afname van deze stroom (absolute waarde) mogelijk ZVS-verlies kan veroorzaken. Hoofdstuk 4 onderzocht de effecten van parasitaire weerstand in de MOSFET-schakelaars en de spoel op deze omgekeerde schakelstroom voor buck-, boost- en buck-boost-omvormers onder spanningsgestuurde variabele-frequentie TCM-ZVS-modulatie. Universele gesloten vergelijkingen voor de gemodificeerde duty cycle en schakelsstroom werden afgeleid, die kunnen worden gebruikt om de schakelsstroom onder verschillende bedrijfsomstandigheden te berekenen. De voorgestelde analyse werd geverifieerd met behulp van een FSBB-converter met TCM-ZVS buck-, boost- en buck-boost-bedrijfsmogelijkheden. De bedrijfsspanning en het vermogen bedroegen respectievelijk 100 tot 400 V en 300 W tot 1 kW.

Compensatie Circuits

Dit gedeelte richt zich op de studie van compensatiecircuits in termen van het bieden van een nauwkeuriger berekeningsmethode voor de elektrische stress in S-S en LCC-S gecompenseerde WPT-systemen, en een nauwkeuriger modellering van de stroomvervorming in LCC-S gebaseerde WPT-systemen.

Het nauwkeurig bepalen van de elektrische stress van de compensatie componenten is een belangrijke stap bij het ontwerpen van een betrouwbaar WPT-systeem. Het werd echter vastgesteld dat de piekspanningsberekening niet nauwkeurig genoeg is voor bepaalde componenten wanneer de eerste harmonische benadering (FHA) methode wordt toegepast op het equivalente wisselstroomcircuit. Meer precies, de piekspanning berekend voor de primaire spoel en secundaire spoel in S-S compensatie, en de piekspanning berekend voor de invoerresonantie-inductor en secundaire spoel in LCC-S compensatie bevatte grote fouten in vergelijking met de simulatie-resultaten. Vanwege de hoge nauwkeurigheid van de rms-stroomberekening werd in hoofdstuk 6 een verbeterde berekeningsmethode voor de piekspanning in gesloten vorm voorgesteld, gebaseerd op de spanningswet van Kirchhoff, waarbij rekening wordt gehouden met de spanning over de gerelateerde compensatiecondensatoren. De voorgestelde analyse werd gevalideerd door zowel simulatie als experimenten.

Door de introductie van een extra LC-tak in LCC-S compensatie in vergelijking met S-S compensatie, vertoont de stroom door de invoerresonantie-inductor meer vervorming door de invloed van hogere harmonischen. Tegelijkertijd is de schakel stroom door de invoer resonant-inductor hangt nauw samen met de ZVS van de schakelaars in de voorste H-brugomvormer. Om deze schakelsstroom nauwkeurig te berekenen, werden in Hoofdstuk 7, in tegenstelling tot eerder onderzoek, zowel de hogere harmonischen van de primaire als de secundaire kant gelijktijdig in overweging genomen, en werden gesloten vergelijkingen afgeleid. Onverwacht, volgens de analyse, draagt de eerste-harmonische stroom ook bij aan de schakelsstroom, zelfs voor een volledig gecompenseerd LCC-S gebaseerde WPT-systeem. De nieuwe methode heeft een verbeterde voorspelling van de schakelstroom aangetoond, zoals bewezen door simulatie. Het moet echter worden opgemerkt dat de voorgestelde analyse is gebaseerd op de veronderstelling dat de vierkante golfspanningen aan de primaire en secundaire zijde in fase zijn, wat verdere discussie vereist.

Abbreviations

AC	Alternating Current
BESS	Battery Energy Storage System
CC	Constant Current
CCM	Continuous Conduction Mode
CV	Constant Voltage
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
EV	Electric Vehicle
FHA	First Harmonic Approximation
FSBB	Four-Switch Buck+Boost
GA	Ground Assembly
iGSE	Improved Generalized Steinmetz Equation
IPT	Inductive Power Transfer
LCC-S	Inductance and Double Capacitances-Series
ORNL	Oak Ridge National Laboratory
PCB	Printed Circuit board
PI	Proportional-Integral
P-P	Parallel- Parallel
PWM	Pulse Width Modulation
RMS	Root Mean Square
SiC	Silicon Carbide
SMD	Surface-Mounted Device

S-S	Series-Series
SAE	Society of Automotive Engineers
TCM	Triangular Current Mode
VA	Vehicle Assembly
WPT	Wireless Power Transfer
ZCS	Zero Current Switching
ZPA	Zero Phase Angle
ZVS	Zero Voltage Switching

1 Introduction

1.1 Background and Motivation

Road transport electrification has become a sustainable and effective means in climate change and air pollution mitigation. After more than 120 years of development since their introduction in the early 20th century together with internal combustion engine vehicles, electric vehicles (EVs) have finally become a viable solution for an increasing number of private and public transport drivers [1]. Some countries and cities have already announced measures towards the transition to electrified mobility.

The battery is the heart of an EV, providing the energy needed for propulsion and supporting the efficient operation of various systems in the vehicle. Although battery technology is constantly improving, for example, increased energy density and capacity, innovative battery charging solutions are still required to increase the acceptance of EVs and acceleration from traditional to electric mobility [2].

Transmission of power without wires has been envisioned since times of Nikola Tesla. Much achievement has been made in this field since the major success of lighting up a bulb with wireless power from two meters away in 2007 [3], [4]. Compared with traditional wired or plug-in charging systems, wireless power charging offers several benefits. Wireless charging can eliminate the need to plug and unplug cables, making it easier to charge EVs, and this also mitigates the safety concerns such as risk of sparks, short circuits or physical damage to ports caused by poor cable connection and moisture. Since no physical connection is required, wireless charging eliminates wear and tear on charging ports and cables, helping to extend the service life of electrical equipment.

A typical wireless power transfer (WPT) charging system comprises a transmitting unit that transmits the power and a receiving unit that receives this power wirelessly and uses it to charge the battery [5]. According to [5], WPT systems are classified into three categories: inductive, inductive-resonant and capacitive. In this thesis, only inductive-resonant method is discussed and studied, which combines the principles of both inductive and resonant coupling to efficiently transfer energy over a distance without the need for physical connection. In particular, a method of wireless power transfer using magnetic induction is also known as inductive power transfer (IPT). In order to achieve resonance, one can use compensation schemes with series and parallel capacitors and inductors. For

1

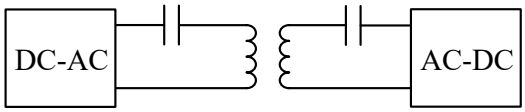


Figure 1.1: Transmitting and receiving coils in an inductive-resonant WPT system [5].

example, Figure 1.1 shows the WPT coils in a resonant WPT system with compensation capacitors on each side. A detailed review on the WPT system topology will be presented in Chapter 2.

At present, optimal designs have already made the efficiency of WPT charging reach a very high level featuring series-series (S-S) compensation [6], [7], [8]. For example, the peak dc-dc efficiency was measured to be 97.2% at 20 kW in [7]. However, the shortcomings of these efficient wireless transmission systems are also obvious, and they are: 1) The peak efficiency was measured at aligned condition, when misalignment occurs, efficiency begins to drop significantly. For example, the dc-dc efficiency drops from 97.2% to 94.1% with 15 cm lateral misalignment [7]; 2) For S-S compensated WPT system, the power transfer efficiency reaches the peak at optimal operating point [9]. When the connected load deviates from this optimal working point, the system efficiency is no longer satisfactory. In summary, although wireless charging can currently achieve efficient power transmission, its working range for efficient power transmission is still narrow. Therefore, how to ensure its efficient operation across a wide range of working conditions to adapt to different scenarios has become an important research topic.

The research focus of this thesis is to study methods for enabling efficient wireless charging over a wide operational range. More precisely, this thesis mainly studies the high-efficiency wide-range operation strategy of non-isolated dc-dc converters and the accurate modeling method of wireless charging compensation network. The detailed study of these two parts provides feasible methods and strategies for the optimal operation of the entire wireless charging system. Briefly, it starts with the overview of state-of-the-art WPT system topology, and this introduces the need to study non-isolated dc-dc converters. Next, modulation strategies to enhance the efficiency performance of the dc-dc converters was researched, more specifically, the focus was on the soft-switching operation of the converter. In the second part, accurate modeling on the compensation topologies in terms of electrical stresses and current distortion phenomenon was given.

1.2 Thesis Objective and Research Questions

As indicated previously, the research objective of this thesis is as follows.

" To research the promising topology of a WPT charging system, and optimization on the operation of its power electronic conversion stages for high efficiency electric vehicle charging over a wide operating range."

More Specifically, the research focus is mainly divided into two parts. The first part

is on the research of high efficiency operation for non-isolated dc-dc converters over a wide operational range taking into account the wireless charging background. The second part is on the modeling of compensation networks for the purpose of achieving more accurate electrical stresses and distorted current calculation. These two parts represent two important subsystems of a whole WPT system. A breakdown of the research objective leads to several research questions as follows.

Question 1: What is the state-of-the-art topology of a WPT charging system ?

In recent years, wireless power transfer has become a very popular research direction as mentioned previously. Numerous research outcomes on this topic are being published every year. Research on WPT topic can be mainly divided into three broad categories: 1) coil/pad designs; 2) compensation topologies; 3) power converters and control. Within each category, the available options are not unique. For example, with regard to compensation topology, one can choose serial or parallel compensation, lower order or high order compensation etc. On the other hand, different compensation methods have different output characteristics, which will affect the selection and operation of the peripheral circuits. Because of these uncertainties, it is necessary to conduct a comprehensive review of the current WPT charging systems with a focus on the corresponding system topology, and this will be addressed in Chapter 2.

Question 2: How to optimize the operation of the FSBB converter such that it can operate efficiently over a wide operational range ?

Since the WPT coil charging pads have already provided electrical isolation between the primary and secondary side, so one only needs to use non-isolated dc-dc converters if a dc-dc conversion stage is needed. Traditional buck and boost converters can only step down or step up the input voltages, which limits their wider applications. Although traditional buck-boost converter can not only step up but also step down the input voltage, it usually has a large inductor rms current, which lowers the converter efficiency. Different from these above mentioned converters, the four-switch buck+boost (FSBB) converter also features both voltage step-up and step-down functions, meanwhile, due to a greater degree of freedom, modulation strategy can be researched for its optimal operation. These characteristics make the FSBB converter a promising topology that can be used in a WPT charging system to help achieve high efficiency power transfer over a wide operational range. Therefore, research on optimal modulation strategy for the FSBB converter is necessary, which will be addressed in Chapter 3.

Question 3: How the parasitic resistances affect the reverse switching current in a dc-dc converter featuring voltage-mode TCM-ZVS modulation ?

Compared with hard-switching modulation such as continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation, traditional dc-dc converters based on a single active switch (this switch is referred to as the original switch in this paragraph) cannot achieve zero-voltage switching. However, one can simply replace the diode with an active switch, and then both switches can be soft-switched through TCM-ZVS modulation. In fact, TCM-ZVS modulation can also be applied to the FSBB converter. In TCM-ZVS

modulation, the reverse switching current through the inductor is the key for the original switch to achieve soft switching. In an ideal case without losses, this switching current can be maintained as a constant value through variable-frequency control. On the other hand, detection of switching current at a high frequency is also a challenge. So variable-frequency voltage-mode TCM-ZVS modulation is preferred. However, in reality, losses is inevitable, so to study the influence on this switching current considering parasitic resistance is meaningful, and this question will be addressed in Chapter 4.

Question 4: How to operate the FSBB converter with a smooth transition between step-up and step-down mode without compromising efficiency ?

As mentioned previously, on one hand, the FSBB converter features both voltage step-up and step-down functions. On the other hand, due to the greater degree of control freedom, the FSBB converter can operate in different modulation modes. The optimal working mode obtained under buck and boost situations does not guarantee that the transition between these two modes will be seamless. Therefore, when the converter changes its operating mode, which usually happens near the unit input-to-output voltage gain, the converter can experience some severe operating oscillations. In order to reduce the negative effects caused by mode switching, an improved modulation strategy should be introduced while maintaining high efficiency operation of the converter. This question will be addressed in Chapter 5.

Question 5: How to accurately determine the electrical stresses of the compensation components in an S-S and LCC-S compensated WPT system ?

As mentioned in the first question, compensation topology is an indispensable part of the WPT system. Among the commonly used compensation topologies, S-S and LCC-S compensations are the two widely adopted topologies. S-S compensated WPT system features constant current output and while LCC-S compensated one features constant voltage output. To accurately determine the electrical stresses of the compensation components is a necessary step to design a reliable WPT system especially for a high-power system, where the resonant peak voltage could easily reach several kilovolts or more, and this presents a greater challenge to the insulation requirements of the components. It is found that the peak voltage calculation is not accurate enough for certain components when applying first harmonic approximation method to the equivalent ac circuit. This question will be addressed in Chapter 6.

Question 6: How to model current distortion of the input resonant inductor in an LCC-S compensated WPT system ?

Compared with S-S compensation, although LCC-S compensation introduces one more LC resonant tank in the primary side, one can use this extra LC circuit to produce a controllable current in the primary coil. This is a beneficial feature because it allows the secondary circuit to be open, but it is fatal to S-S compensation because, in theory, an open circuit from secondary side would induce an infinite current in the primary coil. Furthermore, with the help of serial compensation in the secondary side, constant voltage output can be achieved. On the other hand, the current distortion phenomenon from the

primary side is more obvious in an LCC-S compensated WPT system, and the switching current through the input resonant inductor is closely related with the ZVS realization of the switches in the front-end H-bridge inverter. Therefore, how to accurately and correctly model this current distortion is important. This question will be addressed in Chapter 7.

1.3 Contributions

Targeting to give answers to the aforementioned research questions, the thesis has the contributions as follows.

- A literature review on state-of-the-art WPT charging system topology for electric vehicles was presented (**Chapter 2**).
- A three-mode variable-frequency ZVS modulation was developed for the FSBB converter. Detailed closed-form equations for the operation of the converter were presented. A 3 kW SMD SiC MOSFET-based laboratory prototype with designed input voltage of 300–600 V and output voltage of 400 V was built to evaluate and validate the proposed concepts (**Chapter 3**).
- A universal analytical modeling and calculation method was proposed in closed form to calculate the reverse switching current for buck, boost and buck-boost converters under voltage-mode variable-frequency TCM-ZVS modulation respectively. An FSBB converter with operating voltage of 100–400 V and operating power of 300–1000 W was built to validate the proposed analysis (**Chapter 4**).
- An improved variable-frequency ZVS modulation was developed for the FSBB converter with a smooth transition between step-up and step-down mode. Detailed design procedures were presented. The proposed approach was evaluated and validated by an FSBB converter prototype with an input voltage of 250–600 V, output voltage of 400 V and output power of 250–2500 W (**Chapter 5**).
- An improved peak voltage calculation method was developed for the compensation components in S-S and LCC-S compensated WPT system, which was validated by both simulation and experimentation (**Chapter 6**).
- An improved analytical method was developed for accurate calculation of the switching current in a fully compensated LCC-S based WPT system, which was verified by simulation (**Chapter 7**).

1

1.4 Thesis Outline

The outline of the remainder of this thesis and the interrelations between the chapters are schematically shown in Figure 1.2.

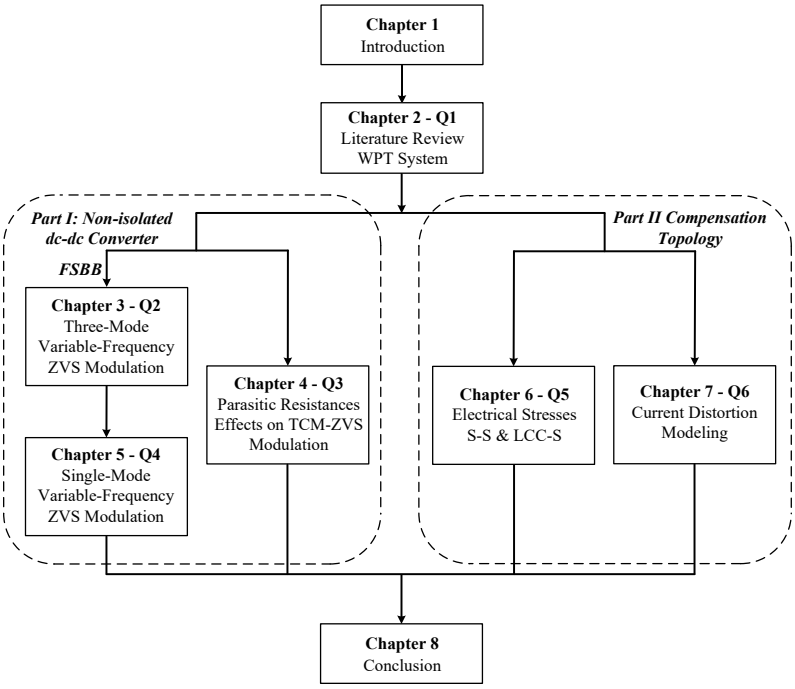


Figure 1.2: Outline of this thesis and the interrelation between the chapters.

2

Brief Overview of WPT System Topology

In this chapter, a brief overview of wireless power transfer system topology will be presented, which explains and illustrates the rationality and feasibility of introducing non-isolated dc-dc converters in wireless charging applications. The WPT research progress introduced in this chapter is divided into three categories by region. Although the literature study provides an overview of development trend and common design choices, it might not be able to cover all studies carried out recently because of the rapid development in this field. [1]

[1] Part of this chapter is based on: G. Yu, T. B. Soeiro, J. Dong and P. Bauer, "Study of Back-end DC/DC Converter for 3.7 kW Wireless Charging System according to SAE J2954," 2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Florence, Italy, 2021, pp. 1-8, doi: 10.1109/CPE-POWERENG50821.2021.9501207.

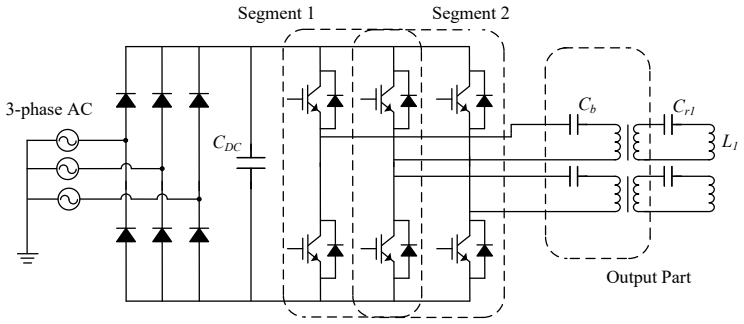


Figure 2.1: Power circuits of the inverter system in [10].

2.1 WPT Research Progress in Asia

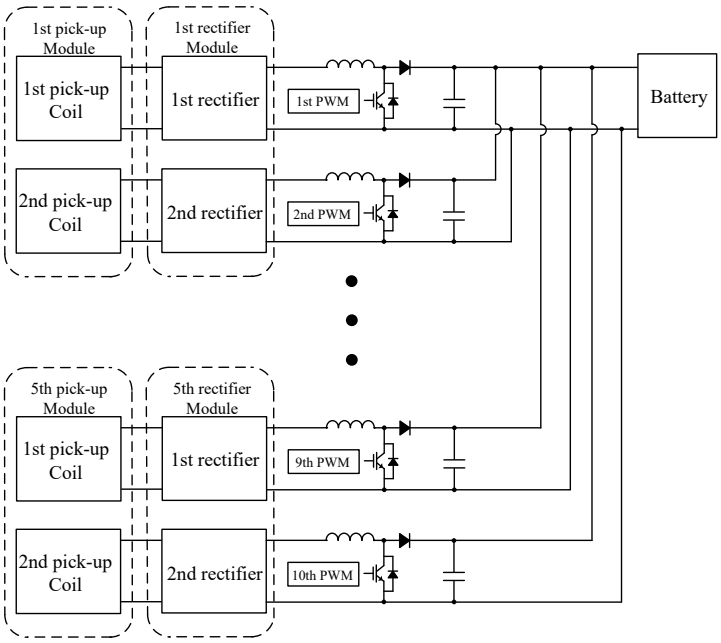
Jaegue Shin et al. from Korea Advanced Institute of Science and Technology (KAIST) built a 100 kW WPT system with 80% efficiency under 26-cm air gap in 2013 [10] . The power supply systems for the proposed system are shown in Figure 2.1. Five 20-kW pickup modules are adopted to obtain 100-kW power capacity, which is shown in Figure 2.2. From Figure 2.2, the inputs of ten boost converters are connected to the outputs of rectifiers while the outputs of ten boost converters are connected to a battery.

Jae Hee Kim et al. from Korea Railroad Research Institute designed and built a 1 MW inductive power transfer system that supplies power to the vehicle in 2015 [11]. The system efficiency was 82.7% at 60 kHz resonant frequency. Figure 2.3(a) shows the configuration of the WPT system for a high-speed train while Figure 2.3(b) shows the electric block diagram. The output voltage of the pick-ups was 2800 V for motor traction, and it was stepped down to 720 V for battery charging through dc-dc converters. The front-end dc voltage was acquired through a thyristor rectifier, and five 200 kW inverters were connected in parallel to convert the dc power to a 60-kHz power source, which is illustrated by Figure 2.4(a). Figure 2.4(b) shows the equivalent circuit with the parameters from the transmitter and pickup. The gap was 5 cm from core to core.

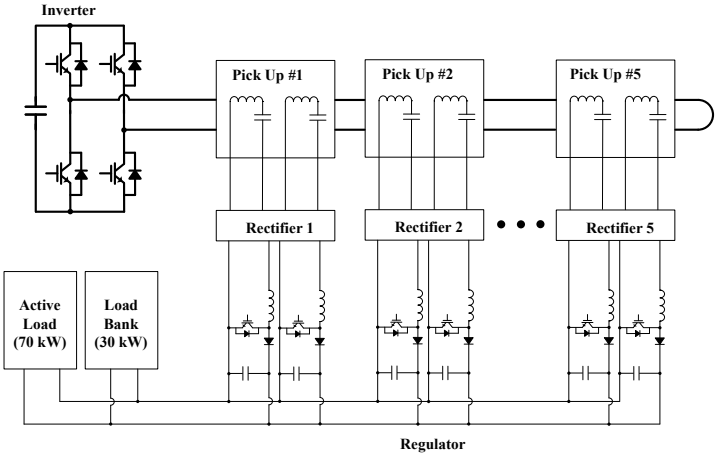
Seung-Hwan Lee et al. from University of Seoul developed a 180 kW inductive power transfer system for a tram in 2016 [12]. The measured efficiency of the system was 85% at 60 kHz and 172 kW output. The equivalent block diagram of the developed system is shown in Figure 2.5. From Figure 2.5, three 60 kW pick-ups and a voltage regulator were installed and delivered power to the battery. The air gap between the transmitter and the pick-up was 7 cm. The output terminals of the pick-ups were connected to diode rectifiers, and a boost regulator was used to supply a constant output voltage [12].

Seung-Hwan Lee et al. from University of Seoul proposed a design methodology for a 300 kW, over 96% coil-to-coil efficiency, online WPT system in 2016 [13]. The overall system block diagram is shown in Figure 2.6. The single 300 kW receiver was separated into two 150 kW receivers in parallel shown in Figure 2.7(a). Figure 2.7(b) shows the measured losses of each component at the rated operation. It can be concluded that the losses of the TX and RX coils dominated the total losses [13].

Tetsu Shijo, Shuichi Obayashi et al. from Toshiba Corporation developed a 44 kW

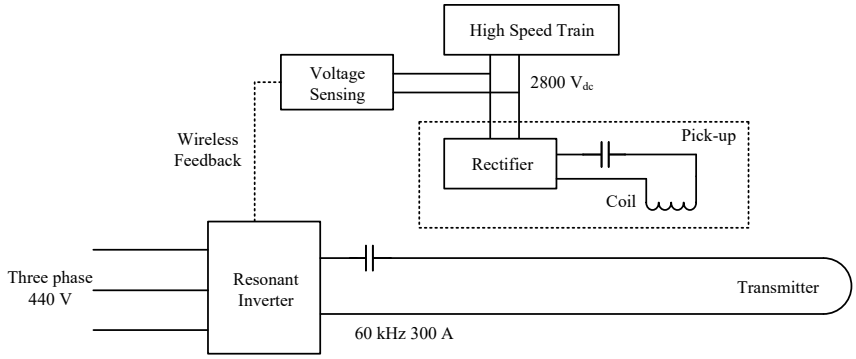


(a)

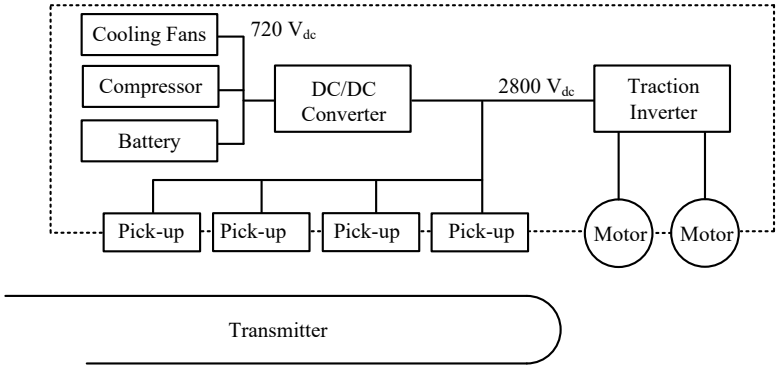


(b)

Figure 2.2: (a) Functional diagram of the online electric vehicle (OLEV) power receiver system [10]. (b) Lab construction of the WPT system [10].



(a)



(b)

Figure 2.3: (a) Configuration of the WPT system for a high-speed train [11]. (b) Electric block diagram of the train using WPT system [11].

WPT system for electric bus charging in the 85 kHz resonant frequency band in 2016 [14], [15], [16]. The transmission distance between the charging pads was 10-13 cm, and the total power transmission efficiency was larger than 85%. A two channel WPT system was adopted with opposite phase current in the transmitting coils to minimize the electromagnetic radiation [14], [15], [16]. Figure 2.8 shows the block diagram of the developed WPT system.

Abubakar Uba Ibrahim et al. from Zhejiang University built a 50 kW three-channel WPT prototype in 2020 with a dc-dc efficiency of 95.2% across 16 cm air gap [17]. The circuit topology is shown in Figure 2.9.

Ganesh R. Nagendra et al. from the University of Auckland developed a 10 kW on-road dynamic inductive power transfer charger with air-gaps ranging from 25-40 cm in 2017 [18]. A secondary power flow controller similar to the one shown in Figure 2.10 was used to regulate the power transfer to the EVs.

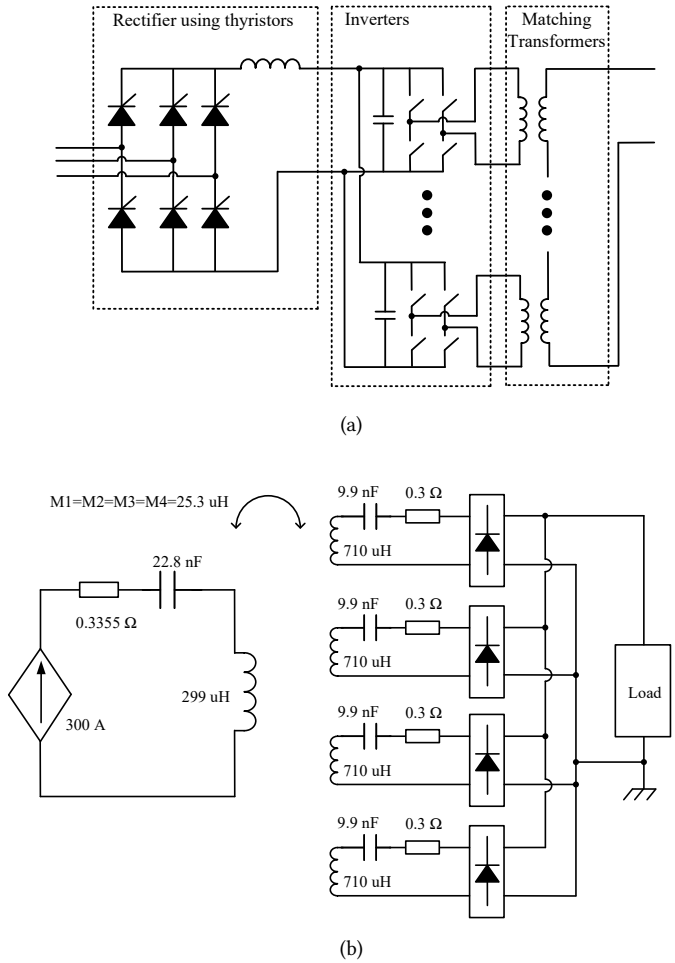


Figure 2.4: (a) Block diagram of the 1-MW resonant inverter for a high-frequency power source [11]. (b) Equivalent circuit of the transmitter and pickups [11].

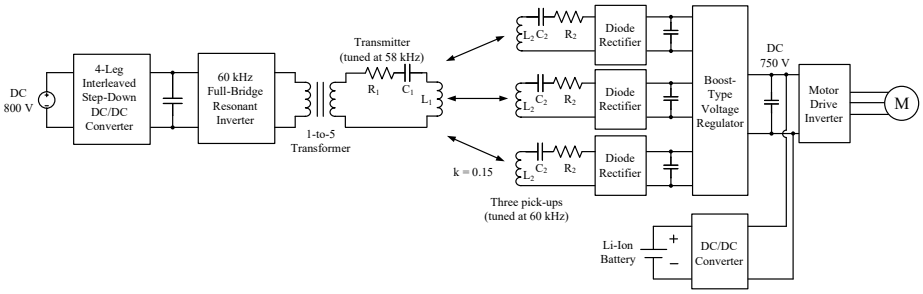


Figure 2.5: Equivalent block diagram of the test-bed [12].

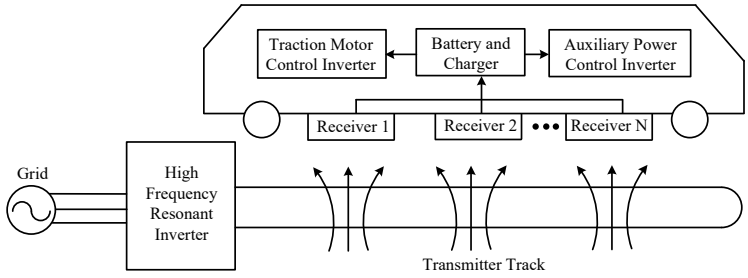
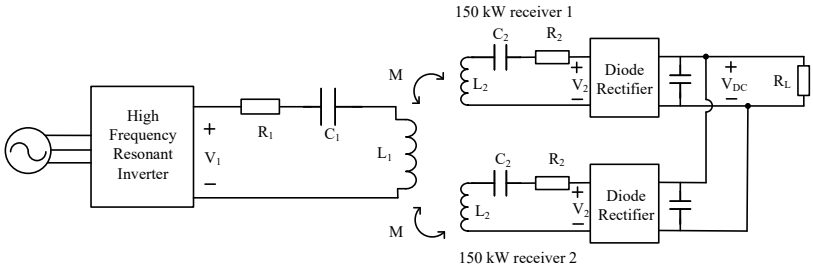
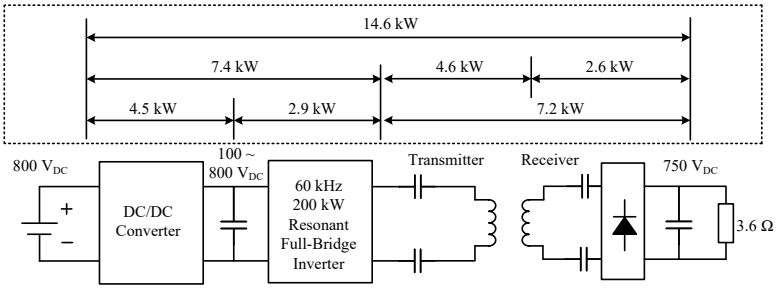


Figure 2.6: Overall system block diagram of a target online WPT system [13].



(a)



(b)

Figure 2.7: (a) Two 150-kW wireless power transfer system [13]. (b) Measured losses of the test-bed [13].

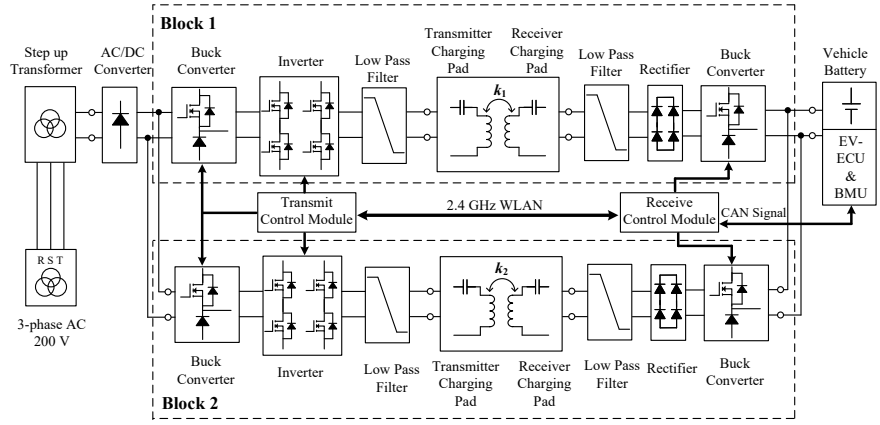


Figure 2.8: Block diagram of dual-block 44 kW wireless rapid charging system [14], [15], [16].

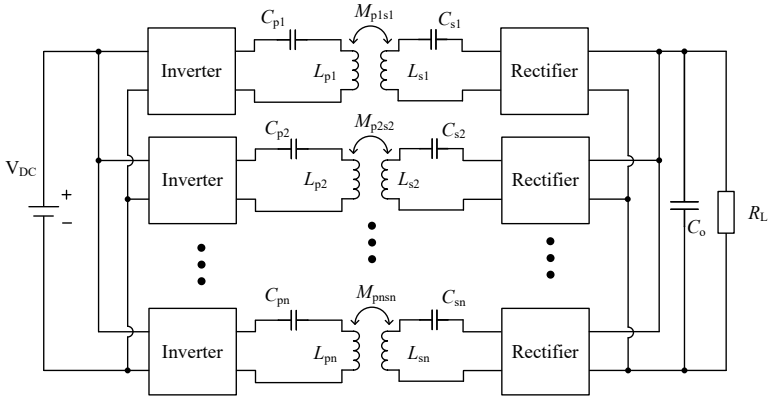


Figure 2.9: Circuit topology of a multichannel system without showing cross mutual inductance [17].

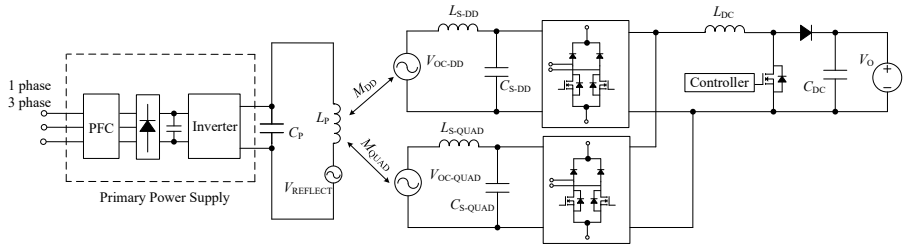


Figure 2.10: Secondary power flow controller [18].

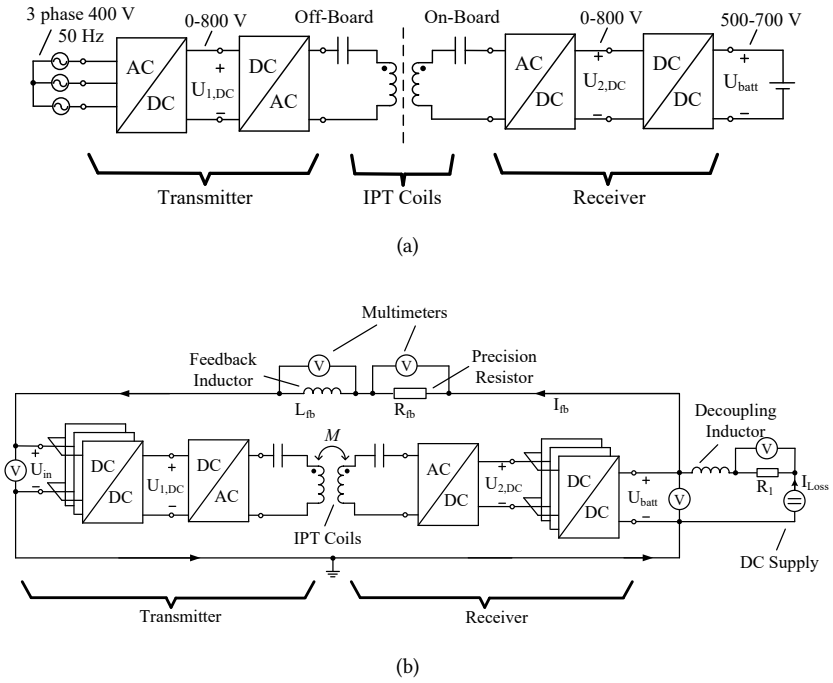


Figure 2.11: (a) WPT system power conversion chain [8]. (b) Experimental setup with energy feedback at the dc link for direct power loss and efficiency measurements [8].

2.2 WPT Research Progress in Europe

Roman Bosshard et al. from ETH Zurich developed a 50 kW WPT system operating at 85 kHz resonant frequency with an air gap of 16 cm in 2016. The dc-dc conversion efficiency (including all the power electronics stages) was 95.8% at 50 kW across 16 cm air gap while the efficiency dropped to 92% with a 15 cm coil misalignment [8], [19]. Figure 2.11 shows the power electronics architecture and the test setup of the WPT system [8]. Three parallel-interleaved buck+boost dc-dc converter modules with coupled magnetic components were adopted, which is shown in Figure 2.12 [19].

B. Goeldi and J. Tritschler et al. from Fraunhofer Institute developed a 22 kW WPT system operating at 100 kHz resonant frequency with over 97% efficiency (dc link to dc link) in 2015, and the nominal coil separation was 13.5 cm [20], [21]. The block diagram of the WPT charging system is shown in Figure 2.13.

Marinus et al. from University of Kiel developed a 6 kW SS-compensated WPT system prototype for low voltage battery charging application in 2015 [22]. The input voltage was 400 V and the output voltage was 24 V. Efficiency between 89% and 94.2% was achieved in any operating conditions between 1 and 6 kW output power. The air gap was between 20 mm and 100 mm while the resonance frequency was 60 kHz. The corresponding power electronic configuration of the system is shown in Figure 2.14.

Jacopo Colussi et al. from Polytechnic University of Turin constructed a 100 kW three-

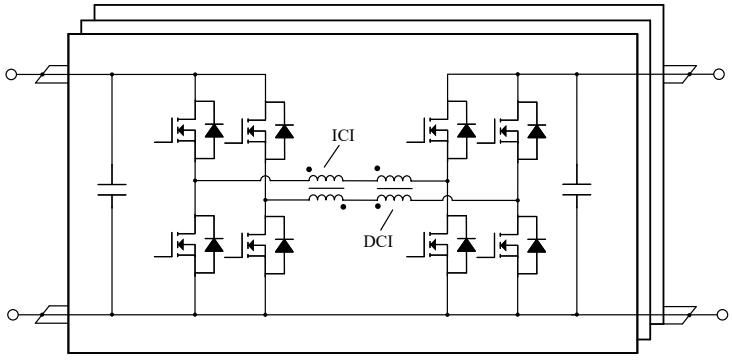


Figure 2.12: Buck+Boost converter with inverse-coupled inductor (ICI) and direct-coupled inductor (DCI) [19].

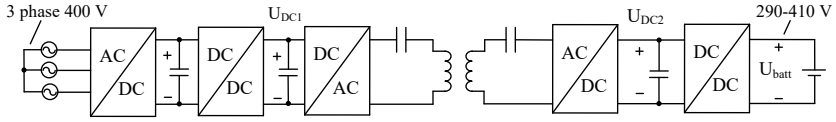


Figure 2.13: Block diagram of the WPT charging system [20].

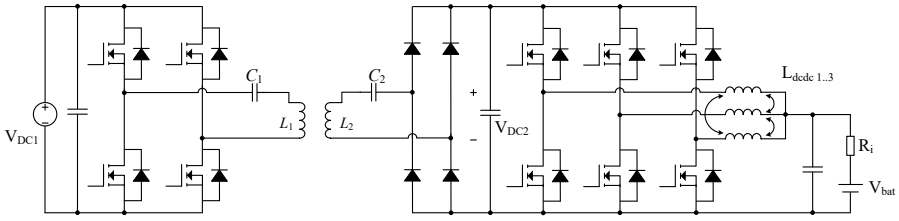


Figure 2.14: Power electronic configuration of the system for high power and low voltage applications [22].

phase WPT prototype operating at 85 kHz with more than 94% dc-dc efficiency over 50 mm air gap distance in 2021 [23]. The dc input voltage was 580 V. The equivalent circuit is shown in Figure 2.15.

Daniel E. Gaona et al. from University of Cambridge built an 11.1 kW WPT system operating at 85 kHz utilizing nanocrystalline ribbon cores in 2021 [24]. The commonly used H-bridge inverter was connected to the transmitter coil while the receiver coil was connected to a passive full-wave diode rectifier.

Recently, Wenli Shi and Francesca Grazian et al. from Delft University of Technology built a 20 kW and 3.7 kW WPT prototypes in 2021 and 2022, respectively [6], [7]. Both prototypes operated at 85 kHz resonance frequency. The peak dc-dc efficiency was 97.2% for the 20 kW prototype while the peak dc-dc efficiency was 96.2% for the 3.7 kW one. The equivalent circuits for the two WPT systems are shown in Figure 2.16.

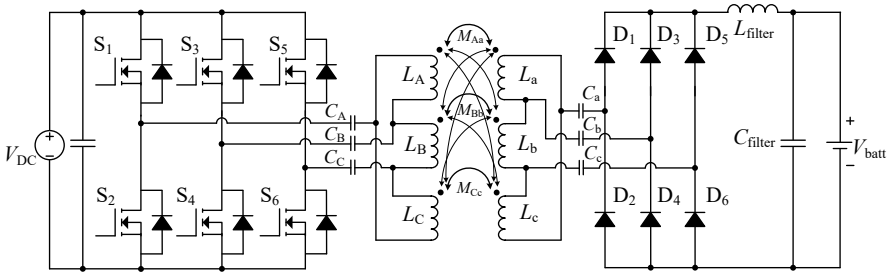


Figure 2.15: Equivalent circuit scheme of the WPT system [23].

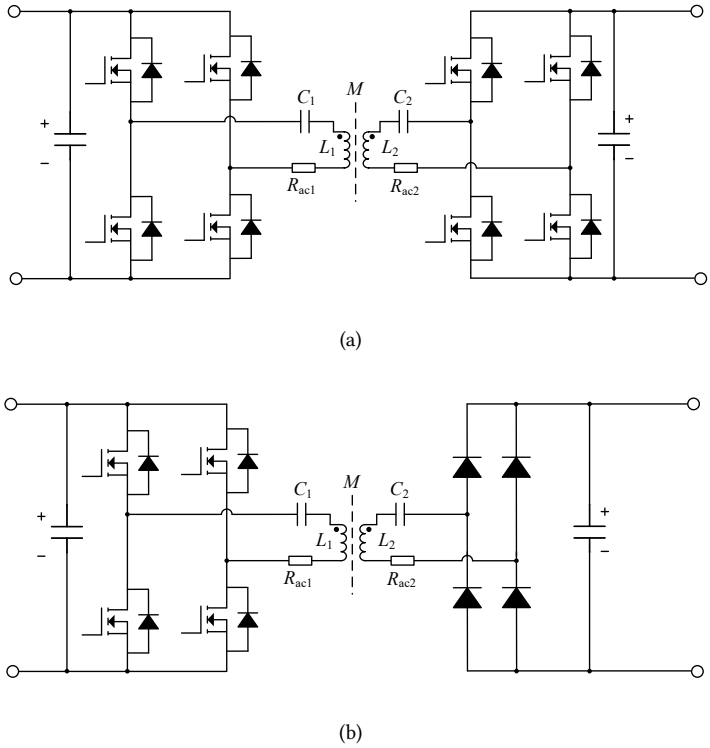


Figure 2.16: Equivalent circuit of the WPT system in (a) [7] and in (b) [6].

2.3 WPT Research Progress in USA

The Oak Ridge National Laboratory (ORNL) has done extensive research work in WPT. Veda P. Galigekere et al. from ORNL built a 10 kW LCC-S compensated WPT system with 94% efficiency in 2017 [25]. The system efficiency of each stage is shown in Figure 2.17. From Figure 2.17, the efficiency of the inversion stage was only 97.74%, however, this

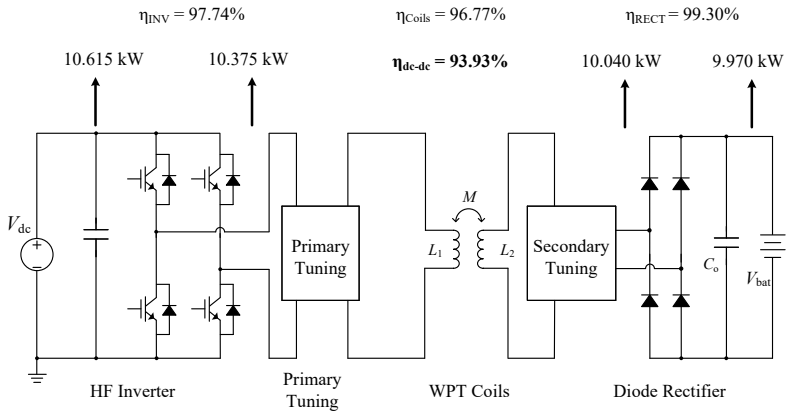


Figure 2.17: System efficiency description of each stage [25].

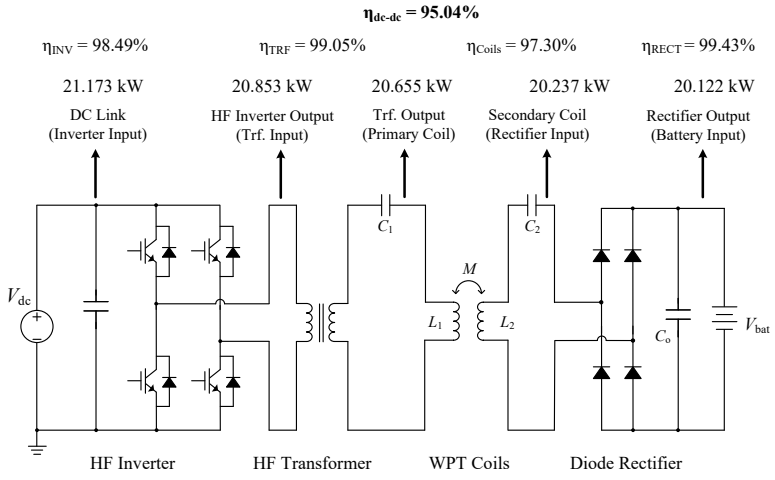


Figure 2.18: Stage-by-stage power flow and efficiencies for 20 kW power transfer [26].

inversion stage typically could reach 99% efficiency with adoption of SiC MOSFETs and soft-switching technique nowadays. So, the dc-dc efficiency can be improved to 95%.

Omer C. Onar et al. from ORNL developed a 20 kW stationary WPT charging system for electric vehicle featuring series-series compensation in 2018 [26]. The dc-dc efficiency (inverter input to the vehicle battery terminals) was over 95%. Figure 2.18 shows the power flow and efficiencies for this WPT system [26].

Jason Pries et al. from ORNL designed and made a novel three-phase 50 kW WPT system using series resonant networks in 2019 [27]. The dc-dc efficiency was 95% with a 15 cm air gap. The system diagram is shown in Figure 2.19.

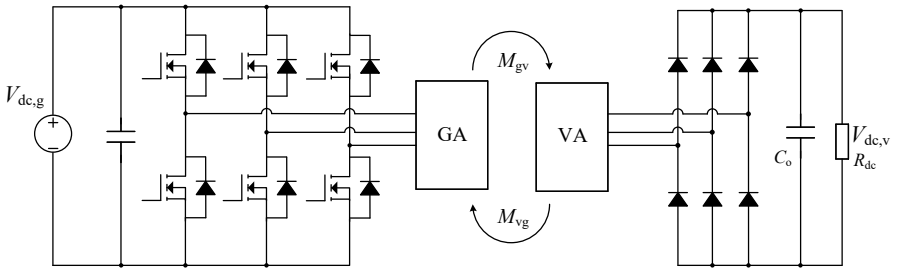


Figure 2.19: WPT system diagram. The GA and VA blocks represent any series resonant circuit [27].

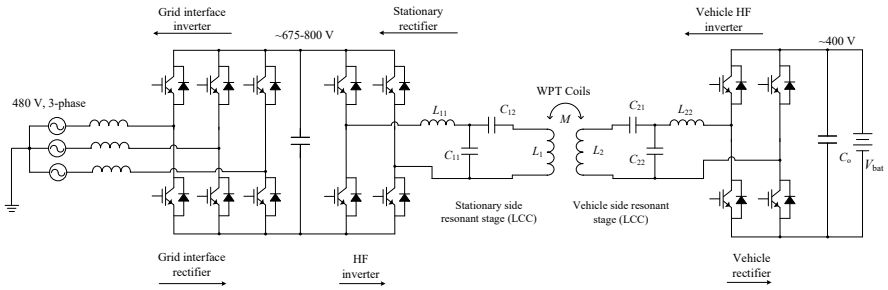


Figure 2.20: System-level schematic of the DLCC WPT charging system [28].

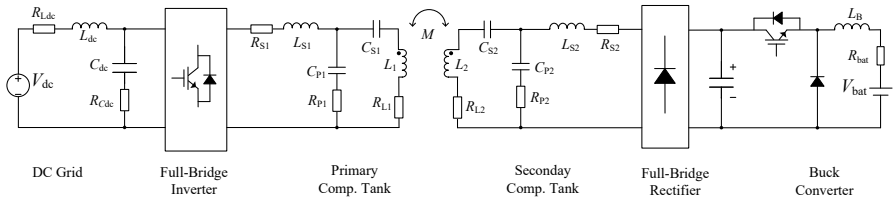


Figure 2.21: Equivalent circuit of the entire WPT system [29].

Mostak Mohammad et al. from ORNL designed and built a bidirectional 20 kW WPT charging system featuring double-sided LCC (DLCC) compensation network in 2020 [28]. The air gap was 28 cm, the input voltage was 800 Vdc and the output voltage was 350 Vdc, and the resonance frequency was 22 kHz. The grid-to-vehicle dc-dc efficiency was 96.1% while the vehicle-to-grid dc-dc efficiency was 96.2%. The system-level schematic of the WPT system is shown in Figure 2.20.

Reza Tavakoli et al. from Utah State University built a 25 kW dynamic WPT charging system for roadway electric vehicles in 2017 [29], [30]. The measured efficiency was 86%, and the equivalent circuit of the WPT system is shown in Figure 2.21.

Table 2.1: Summary of WPT research progress.

References	Year	Power (kW)	Resonance Frequency (kHz)	Power Conversion Stages	Voltage Range	Compensation Type	System Efficiency
Jaegue Shin et al. KAIST [10]	2013	100	20	AC-DC, DC-AC, AC-AC, WPT Coil, AC-DC, DC-DC	500 Vdc (Inverter) -620 Vdc (Output)	S-S	80%
Jae Hee Kim et al. Korea Railroad Research Institute [11]	2015	1000	60	AC-DC, DC-AC, AC-AC, WPT Coil, AC-DC, DC-DC	AC Grid-2800 Vdc (720 Vdc)	S-S	82.7%
Seung-Hwan Lee et al. University of Seoul [12]	2016	180	60	DC-DC, DC-AC, AC-AC, WPT Coil, AC-DC, DC-DC	800 Vdc-750 Vdc	S-S	85%
Seung-Hwan Lee et al. University of Seoul [13]	2016	300	60	DC-DC, DC-AC, WPT Coils, AC-DC	800 Vdc-750 Vdc	S-S	90.4%
Tetsu Shijo et al. Toshiba Corporation [16]	2016	44	85	AC-AC, AC-DC, DC-DC, DC-AC, WPT Coil, AC-DC, DC-DC	AC Grid-300 Vdc	S-S	85%
A. U. Ibrahim et al. Zhejiang University [17]	2020	50	85	DC-AC, WPT Coil, AC-DC	800 Vdc-600 Vdc	S-S	95.2%
G. R. Nagendra et al. University of Auckland [18]	2017	10	40	AC-DC, DC-AC, WPT Coil, AC-DC, DC-DC	AC Grid-325 Vdc	P-P	NA
Roman Bosshard et al. ETH [8]	2015	50	85	DC-DC, DC-AC, WPT Coil, AC-DC, DC-DC	800 Vdc-800 Vdc	S-S	95.8%
B. Goeldi and J. Tritschler et al. Fraunhofer Institute [20]	2015	22	100	AC-DC, DC-DC, DC-AC, WPT Coil, AC-DC, DC-DC	AC Grid-(290–410) Vdc	S-S	90.98%
Marinus et al. University of Kiel [22]	2015	6	60	DC-AC, WPT Coil, AC-DC, DC-DC	400 Vdc-24 Vdc	S-S	94.2%
Jacopo et al. Polytechnic University of Turin [23]	2021	100	85	DC-AC, WPT Coil, AC-DC	580 Vdc-380 Vdc	S-S	94.1%
Daniel et al. University of Cambridge[24]	2021	11.1	85	DC-AC, WPT Coil, AC-DC	~ 600 Vdc-~ 600Vdc	S-S	95.5%
Wenli Shi et al. TU Delft [7]	2021	20	85	DC-AC, WPT Coil, AC-DC	800 Vdc-800 Vdc	S-S	97.2%
Francesca et al. TU Delft [6]	2022	3.7	85	DC-AC, WPT Coil, AC-DC	(360–500) Vdc -(280–400) Vdc	S-S	96.2%
Veda et al. ORNL [25]	2017	10	22	DC-AC, WPT Coil, AC-DC	355 Vdc-380 Vdc	LCC-S	93.9%
Omer et al. ORNL [26]	2018	20	21-24	DC-AC, AC-AC, WPT Coil, AC-DC	(418–439) Vdc -381 Vdc	S-S	95%
Jason Pries et al. ORNL [27]	2019	50	85	DC-AC, WPT Coil, AC-DC	~ 555 Vdc-~ 585 Vdc or ~ 297 Vdc-~ 338 Vdc	3-ph series resonant tank	95%
Mostak et al. ORNL [28]	2020	20	22	AC-DC, DC-AC, WPT Coil, AC-DC	(675–800) Vdc -(320–400) Vdc	LCC-LCC	96.1%
Reza et al. Utah State University [29], [30]	2017	25	20	DC-AC, WPT Coil, AC-DC, DC-DC	600 Vdc-330 Vdc	LCC-LCC	86%

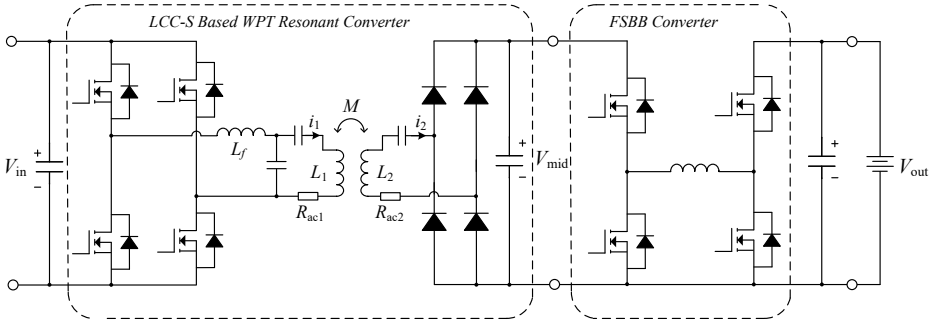


Figure 2.22: Schematic of LCC-S based WPT charging system with a back-end FSBB converter.

2.4 Summary and Discussion

2.4.1 A Brief Summary

Based on the literature review, a table of summary on the design choices of recent remarkable works is given in Table 2.1.

2.4.2 Discussion

From the literature studied previously, it can be found that dc-dc converters have been widely adopted in the wireless power transfer charging systems. These dc-dc converters can be put on the primary side, secondary side or both sides for the purpose of power and voltage regulation. Since the WPT coils have already provided electrical isolation, so, non-isolated dc-dc converters can simply be used. In addition, compared with traditional buck and boost converters, which could only realize voltage step-down or step-up function, the FSBB converter can achieve both voltage step-down and step-up functions. Therefore, it is beneficial to adopt this dc-dc topology. In this thesis, a WPT charging system featuring LCC-S compensation and a back-end FSBB converter was chosen as the research object, and the schematic is shown in Figure 2.22.

There are several advantages with wireless charging solution shown in Figure 2.22, and they are as follows.

- Compared with font-end power regulation, back-end power regulation avoids communication between wireless charging pads during charging, which helps improve the system reliability.

- Different from S-S compensation, LCC-S based WPT system features inherent safety advantage. Because for the S-S compensated WPT system, when the inverter stage is operating, it is not allowed to have no secondary side coil or an open circuit on the secondary side, otherwise, the primary side is equivalent to a short circuit. To prevent such situations from occurring, this indicates that the S-S compensated WPT system needs to have more reliable, stable, and fast detection capabilities in this regard. But for LCC-S compensation, it is allowed to have no secondary coil or an open circuit on the secondary side.

Table 2.2: Summary of the reference parameters from SAE J2954 for WPT1 power level.

	Z1	**Z2**	**Z3**
L_1 min (μH)	185	212	224
L_1 max (μH)	217	223	227
L_2 min (μH)	214	207	198
L_2 max (μH)	232	214	203
k min	0.1	0.085	0.084
k max	0.249	0.221	0.243
M min (μH)	19.89	17.80	17.69
M max (μH)	55.87	48.28	52.16

- The back-end FSBB converter, which can provide both voltage step-up and step-down functions, enables wide-range operation for wireless charging purpose.

Further discussions on the third point are given, which explains why the FSBB converter has advantages in LCC-S based WPT system. The SAE J2954 [31], which is a standard for wireless power transfer for electric vehicles led by SAE International, covers the reference design up to 11.1 kVA input power as of 2020. Therein, three power level classes are defined: WPT1 for 3.7 kVA system, WPT2 for 7.7 kVA, and WPT3 for 11.1 kVA. Three different vertical distance classes (Z-classes) between the ground assembly (GA) and the vehicle assembly (VA) are given: **Z1** = 100–150 mm, **Z2** = 140–170 mm and **Z3** = 170–250 mm. The ground clearance and the offset position of the coils will influence the coil coupling coefficients. The normative design specifications are given for three different Z-classes and are summarized in Table 2.2 [32]. Therein: L_1 and L_2 are the primary and secondary side coil self-inductance respectively; k is the magnetic coupling coefficient and M is the derived mutual inductance. As it can be seen, the mutual inductance can differ by as much as three times, and for a fully compensated LCC-S based WPT system, the output voltage can be expressed by (2.1)

$$V_{\text{mid}} = \frac{M}{L_f} V_{\text{in}}, \tag{2.1}$$

where L_f is the inductance of the input resonant inductor. Therefore, for 400 V class battery, if a buck converter is used considering efficiency performance instead of a boost converter, then the voltage of V_{mid} will vary between approximately 500–1500 V to guarantee that it is always larger than 400 V. Here, 500 V corresponds to the situation with a minimum value of mutual inductance, and it is assumed that L_f and V_{in} remain unchanged. This means only switches with a withstand voltage of 1700 V or higher can be chosen, and currently, the selection of such switches on the market is limited. However, if an FSBB converter is used, the voltage of V_{mid} can be selected, for example, between 200–600 V, and then, there will be more switches on the market that meet the voltage withstand requirements. On top of that, the printed circuit board (PCB) layout design of the power stage will also become easier with a lower bus voltage.

In addition to the above mentioned points, one can also consider the choice of V_{mid} from the perspective of reducing coil losses, namely, to improve the efficiency of the WPT resonant stage. When the H-bridge inverter operates at resonant frequency with a square-wave output voltage, for a fully compensated LCC-S compensation, as will be described

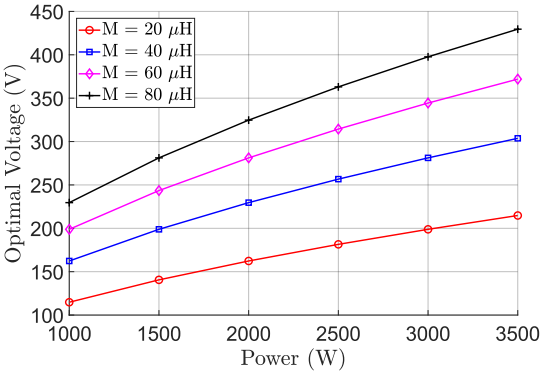


Figure 2.23: Optimal voltage of V_{mid} in terms of different power and mutual inductance values, assuming $R_{\text{ac1}} = R_{\text{ac2}}$.

in Chapter 6, the root mean square (rms) value of the primary coil current based on first harmonic approximation (FHA) method is

$$I_1 = \frac{2\sqrt{2}V_{\text{in}}}{\pi\omega_0 L_f} = \frac{2\sqrt{2}V_{\text{mid}}}{\pi\omega_0 M}, \tag{2.2}$$

where ω_0 is the resonant angular frequency. Assuming the processed power is P_o, then the rms value of the secondary coil current is

$$I_2 = \frac{\pi}{2\sqrt{2}} \cdot \frac{P_o}{V_{\text{mid}}}. \tag{2.3}$$

So, the total conduction losses are

$$P_{\text{cond}} = I_1^2 R_{\text{ac1}} + I_2^2 R_{\text{ac2}} = \frac{8}{\pi^2\omega_0^2 M^2} \cdot V_{\text{mid}}^2 \cdot R_{\text{ac1}} + \frac{\pi^2}{8} \cdot \frac{P_o^2}{V_{\text{mid}}^2} \cdot R_{\text{ac2}}, \tag{2.4}$$

where R_{ac1} and R_{ac2} are the equivalent resistances of the two coils. From (2.4), one can derive the voltage value of V_{mid} that minimizes the conduction losses, which is

$$V_{\text{mid}} = \frac{\pi}{2} \cdot \sqrt{\frac{\omega_0 M P_o}{2} \cdot \sqrt{\frac{R_{\text{ac2}}}{R_{\text{ac1}}}}}. \tag{2.5}$$

It can be seen from (2.5), the optimal voltage does not depend on the input voltage, but it depends on the power value. For example, Figure 2.23 shows this optimal voltage value with different mutual inductance and power as a reference. Although a strict and comprehensive analysis would require considering losses caused by other factors, the above quick and rough analysis still provides a reasonable range for selecting the voltage of V_{mid} based on the coil recommendation from SAE J2954.

In summary, to achieve a safe and reliable WPT charging system that operates efficiently across a wide range of conditions with moderately complex control schemes, this thesis focuses on researching an LCC-S based WPT system combined with a back-end FSBB converter as the preferred topology.

3

Three-Mode Variable-Frequency ZVS Modulation for FSBB Converter

This chapter introduces a three-mode variable-frequency Zero Voltage Switching (ZVS) modulation method for the four-switch buck+boost converter. Herein, the buck+boost converter operation is subdivided into three operating regions according to the converter static voltage gain, i.e., buck-, buck-boost-, and boost-type modes. A ZVS turn-on triangular current mode (TCM) modulation is adopted for buck-type and boost-type modes. In the buck-boost-type mode when the input-to-output voltage gain is close to unit, all the possible modulation cases are studied thoroughly based on the phase shift of the two half bridges in a full switching period. The selection of the most suitable modulation scheme is performed to minimize the rms value of the inductor current while taking into account the simplification of the practical implementation. Closed-form equations are derived, which makes it easy to implement in practice. The proposed strategy is described, analyzed and finally verified through a 3 kW SMD SiC MOSFET-based laboratory prototype with designed input voltage of 300–600 V and the typical output voltage of 400 V class battery. The efficiency from the measured results is remarkably high, i.e., between 99.2% and 99.6% in a power range from 1 kW to 3 kW. Finally, tests for the operating mode transitions demonstrated the feasibility of the proposed modulation method. The power density of this converter is 4.86 kW/L. [1]

[1]This chapter is based on:

G. Yu, J. Dong, T. B. Soeiro, G. Zhu, Y. Yao and P. Bauer, "Three-Mode Variable-Frequency ZVS Modulation for Four-Switch Buck+Boost Converters With Ultra-High Efficiency," in IEEE Transactions on Power Electronics, vol. 38, no. 4, pp. 4805-4819, April 2023, doi: 10.1109/TPEL.2022.3231969.

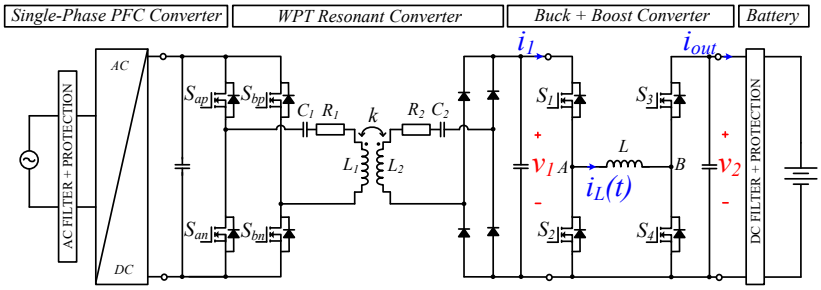


Figure 3.1: S-S compensated WPT system with a four-switch buck+boost converter as a back-end dc-dc converter.

3.1 Introduction

Battery energy storage systems (BESSs) play a vital role in the energy transition market [33], [34]. The advent of more electric transportation is strongly reliant on the BESS technology [35]. The development and performance of a BESS is dependent on the features of the dedicated power electronics-based charger/discharger regulator [36].

Today, an advantageous compound circuit for the BESS charging application is the non-isolated dc-dc converter assembled with the four-switch buck+boost converter. This circuit has both voltage step-up (boost) and voltage step-down (buck) functions. In fact, this converter has found a good fit for the application in the field of wireless power transfer (WPT) electric vehicle (EV) charging as illustrated by Figure 3.1. The reasons behind the adoption of a buck+boost converter in a WPT EV charging system will be briefly discussed in the followings.

The WPT-based EV chargers usually adopt series-series (S-S) compensation in the resonant dc-dc converter stage [7]. In order to achieve the highest efficiency, the equivalent dc load seen by the resonant converter $R_L = \frac{V_1}{I_1}$ (cf., Figure 3.1) should match the so called optimal load R_{opt} [9], [37], which is

$$R_{\text{opt}} = \frac{\pi^2}{8}\sqrt{R_2^2 + \omega_0^2 M^2 \frac{R_2}{R_1}}. \tag{3.1}$$

In (3.1), M is the coil mutual inductance; R_1 and R_2 are the lump equivalent resistances modeling the power losses across the primary and secondary side components; ω_0 is the converter's resonant frequency. In essence, the function of the non-isolated dc-dc converter is to act as a load impedance matching converter [38], [39]. Since the optimal load depends on the mutual inductance, its condition varies with the coils' alignment. Besides, with the change of charging power, it can be imagined that the input voltage of the back-end dc-dc converter V_1 will vary in a wide range. In order to match the EV battery charging profile while allowing the switching frequency of the S-S compensated resonant converter to be narrow according to the specified standards (e.g., the SAE J2954 [31]), a converter with both voltage step-up and step-down functions is therefore advantageous.

The modulation strategies of the four-switch buck+boost converter can be mainly divided into three categories: single mode, two-mode and three-mode operations. Under each category, either hard-switching or soft-switching modulation could be applied. Single

mode operation is the simplest control method when buck-boost-type mode is adopted [40], i.e., switches S_1 and S_4 (cf., Figure 3.1) turn on and off simultaneously, which operates exactly the same as a single-switch buck-boost converter but with a non-inverting output voltage. However, this modulation scheme usually results in poor efficiency due to the high switching and conduction losses. To address this problem, two-mode operation was introduced [41], [42], [43], [44], [45]. In two-mode operation, buck-type or boost-type mode is adopted based on the input and output voltages. There are several advantages of this operation: Firstly, only two switches are active, so the switching losses could be reduced; Secondly, the conduction losses could also be lower; Thirdly, with adoption of zero voltage switching (ZVS) turn-on triangular current mode (TCM) modulation [46], [47], [48], [49], the efficiency of SiC MOSFET-based buck or boost converters can be higher than 99%. However, due to the duty cycle limitation in practice, there will be a voltage transition zone that cannot be covered by the two-mode operation, which is the main drawback of this modulation strategy. Hence, three-mode operation was introduced [50], [51],[52], [53], with an added zone between the buck-type and boost-type modes, the output voltage can be regulated well in this zone. Two-edge modulation was proposed in [52] and [54] to reduce the conduction losses, where switches S_1 and S_4 are trailing-edge and leading-edge modulated resulting in a lower current rms value, however, it is still a hard-switching modulation [52], [53], [54]. With such a concept, the highest power efficiency was 97.8% at rated power of 300 W [52] and 98.5% at 250 W [54].

Although hard-switched SiC MOSFET-based dc-dc converter could also possibly achieve power efficiency higher than 99% [55], [56], the high rate of voltage change (dV/dt) due to the shorter switching transients will cause increased EMI emissions [57]. Furthermore, with the increasing requirements for power density and efficiency, ultra-high frequency converters can only be built through soft-switching techniques to achieve acceptable power efficiency [50], [58]. Considerable efforts have been made to implement the ZVS modulation for the buck+boost converters in recent years. In [50] and [51], the TCM-ZVS modulation was extended to the buck-boost-type mode, however, the operation in this mode was not optimized, and thus, a sudden efficiency drop was observed. The reported conversion efficiency was between 98% and 98.5% for a 2.5 kW prototype by Zhe Yu *et al.* in [51]. In [59] and [60], Zhe Yu *et al.* further optimized this ZVS control. In [59], the assumption of an equal duty cycle was applied to both switches S_1 and S_4, and the highest efficiency was 99.4% for a 3 kW prototype. However, both the detailed mathematical analysis and practical implementation steps are missing in [59] and [60]. In [61], an improved control strategy was proposed for the intermediate mode of variable-frequency modulation, however, the rms value of the inductor current was not studied and an evident efficiency drop was still observed in the intermediate mode with a value around 4%. The reported efficiency was between 93% and 96.9% for a 300 W prototype.

Apart from variable-frequency ZVS modulation, fixed-frequency four-segment inductor current mode ZVS modulation were proposed and studied [57], [62], [63], [64], [65], [66]. In order to make descriptions clearer, the concept is illustrated in Figure 3.2. In [62], the general descriptions of this modulation concept were given, but without detailed mathematical analysis. With the same control concept, Stefan Waffler *et al.*[57] studied the switching times of the switches in a period to maximize the transferred power under ZVS conditions, but the optimization to further minimize inductor current rms value was

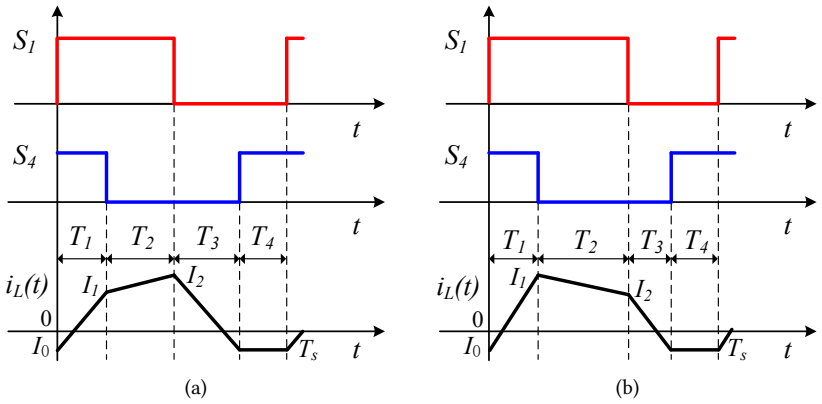


Figure 3.2: Fixed-frequency four-segment inductor current mode ZVS modulation method, I_0 is negative. (a) $V_1 > V_2$. (b) $V_1 < V_2$.

missing, and the peak efficiency was 98.3% for a 12 kW prototype with a power density of 17.4 kW/L. Theoretical analysis for the current rms value minimization was presented in [63], however, due to the complexity of the equations, the optimized switching times can only be calculated offline. Nevertheless, the switching frequency at 800 kHz was impressive and the peak efficiency was 98% for a 300 W prototype. Based on the research work of [63], Lin Tian *et al.* further found a monotonic relationship between the rms and peak value of the inductor current through plotting, however, with the assumption of letting the corner current [I_1 in Figure 3.2(a), I_2 in Figure 3.2(b)] equal to the ZVS turn-on current, the analytical expressions for the switching times can actually be determined, which were not given in [64]. By further checking the proposed method in [64], a combination control of fixed- and variable-frequency modulations is adopted, which increases the control complexity. In [65], it was found that through selecting a certain T_1 (cf., Figure 3.2), the conduction losses and the core losses could be minimized, however, the value of T_1 depends on the working conditions and a look-up table was needed. The peak efficiency was 98.1% for a 280 W prototype operating at 1 MHz frequency [65]. Due to the calculation complexity of the four-segment inductor current mode ZVS modulation, a special case is to set a fixed duty cycle to S_1 or S_4 [66], then the calculations can be simplified considerably. A summary of state-of-the-art four-switch buck+boost converters is shown in Table 3.1.

A thorough study of a three-mode variable-frequency soft-switching modulation strategy for the four-switch buck+boost converter is found to be missing in the literature. The main purpose and contribution of this work is to analyse each possible modulation case in the buck-boost-type mode through the phase shift between S_1 and S_4 in a full switching period with a new set of derived closed-form equations, which can be used to determine parameters such as switching frequency, inductor current rms value, etc. The closed-form equations of the inductor current rms value are usually missing in the literature due to the complicated calculations, thus, the optimization of the peak current [67] was usually adopted instead of the rms value. In this work, it is found that in the buck-boost-type mode, the three-segment inductor current mode ZVS modulation is the most suitable scheme

Table 3.1: Summary of State-of-the-Art Four-Switch Buck+Boost Converters

References	Power	Year	Input (V)	Output (V)	Frequency (kHz)	MOSFET Type	Switching Type	Peak Eff. (%)	Power Density (kW/L)
This Paper	3 kW	2022	300-600	360-400	20-160	SiC	Soft	99.6	4.86
CU-Boulder [43]	500 W	2012	12-38	21-32	100	Si HEXFET	Hard	97.0	N/A
UCF [44]	100 W	2019	11-50	12-36	80-150	Si OptiMOS	Hard	99.31	3.67
DTU[50]	100 W	2017	30-60	30-60	10^4	GaN	Soft	94.4	6.25
NUAA [52]	300 W	2009	36-75	48	200 and 40	Si	Hard	97.8	N/A
Fraunhofer Institute [51]	2.5 kW	2015	400	100-550	N/A	SiC	Soft	>99.0	N/A
Sungkyunkwan University [54]	250 W	2016	15-40	0-43	200	Si OptiMOS	Hard	98.5	N/A
ETH Zurich [57]	12 kW	2009	<450	<450	100	Si HiPerFET	Soft	98.3	17.4
Fraunhofer Institute[59]	3 kW	2016	400	150-500	N/A	SiC	Soft	99.4	N/A
Zhejiang University [63]	300 W	2019	36-72	48	800	Si OptiMOS	Soft	98.0	N/A
Zhejiang University [64]	300 W	2022	36-60	36-60	700-800	Si NexFET	Soft	98.5	N/A
Southeast University [65]	280 W	2021	36-72	48	1000	GaN	Soft	98.1	N/A

because it greatly simplifies the converter operation while maintaining a high-efficiency performance. The proposed modulation strategy combines advantages from different operating modes, thus the converter can always operate efficiently in a wide range. Besides, the mode transition tests were also provided to demonstrate the feasibility of the proposed modulation method.

The rest of this chapter is organized as follows. Section 3.2 presents the working principle of the four-switch buck+boost converter, the proposed modulation strategy featuring ZVS turn-on, and finally the derived formulae. In Section 3.3, design considerations including the selection of the switching ZVS current and inductance are shown. Finally, in Section 3.4, the studied modulation is evaluated through a 3 kW SMD SiC MOSFET-based prototype.

3.2 Working principle of the modulation strategy

3.2.1 Voltage Gain of the Four-Switch Buck+Boost Converter

The four-switch buck+boost converter is composed of two half bridge circuits as shown in Figure 3.1. S_1 and S_2 form the buck-type conversion while S_3 and S_4 form the boost-type conversion. The PWM signals applied to each bridge are complementary.

Some assumptions are made for the following analysis: First, the dead time influence is neglected in this section; Second, the inductor has a constant value; Third, the input and output voltages are taken as constant dc values.

Defining d_1 and d_2 as the duty cycles of S_1 and S_4, respectively. Based on the volt-second balance of the inductor under steady state, the average voltage across points A and B shown in Figure 3.1 should be zero. The average voltages of points A and B with respect to the bottom-side dc-bus rail are

$$\bar{v}_A = d_1 V_1 \tag{3.2}$$

$$\bar{v}_B = (1 - d_2) V_2. \tag{3.3}$$

Therefore, $\bar{v}_A = \bar{v}_B$ leads to the voltage gain equation below

$$G_v = \frac{V_2}{V_1} = \frac{d_1}{1 - d_2}. \tag{3.4}$$

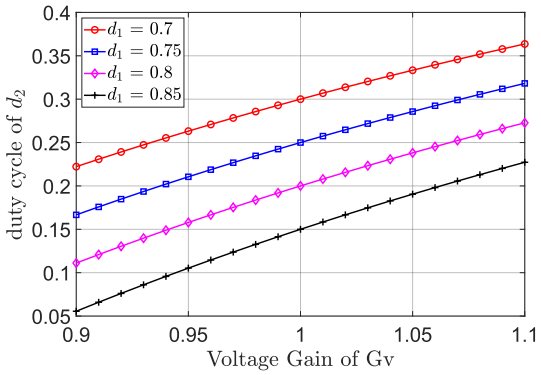


Figure 3.3: Duty cycle of d_2 in terms of different d_1. Herein, d_2 is always smaller than d_1.

Equation (3.4) always holds regardless of the power level. Based on (3.4), infinite control schemes can be found to realize a certain voltage gain since d_1 and d_2 can be controlled independently.

3.2.2 Soft Switching under Buck-Boost-type Mode with Possible Modulations

Depending on the minimum pulse width and switching frequency, the minimum and maximum duty cycle of the PWM signals can be different [53]. In this work, the maximum and minimum duty cycles are set as 0.9 and 0.1, then, the maximum gain under buck mode is 0.9 and the minimum gain under boost mode is 1.11. So, the voltage gain under buck-boost-type mode needs to cover the voltage gain between these two values. Based on (3.4), the difference between d_1 and d_2 is

$$\Delta d = d_1 - d_2 = d_1(1 + \frac{1}{G_v}) - 1. \tag{3.5}$$

If $\Delta d > 0$, as will be seen later, the modulation analysis will be simpler since for each step-down or step-up case, only four modulation types need to be analyzed. When $\Delta d > 0$, (3.6) can be derived as

$$d_1 > \frac{1}{1 + \frac{1}{G_v}}. \tag{3.6}$$

Substitute $G_v = 1.11$ into (3.6), then when $d_1 > 0.526$, d_1 is always larger than d_2. Figure 3.3 shows the duty cycle of d_2 with different values of d_1.

For the rest analysis in this section, $d_1 > d_2$ always holds.

To fully analyse each possible modulation case, the phase shift between the PWM signals of S_1 and S_4 has to be carried out in a full switching period.

Case When $V_1 > V_2$

From (3.4), one has

$$d_1 + d_2 < 1. \tag{3.7}$$

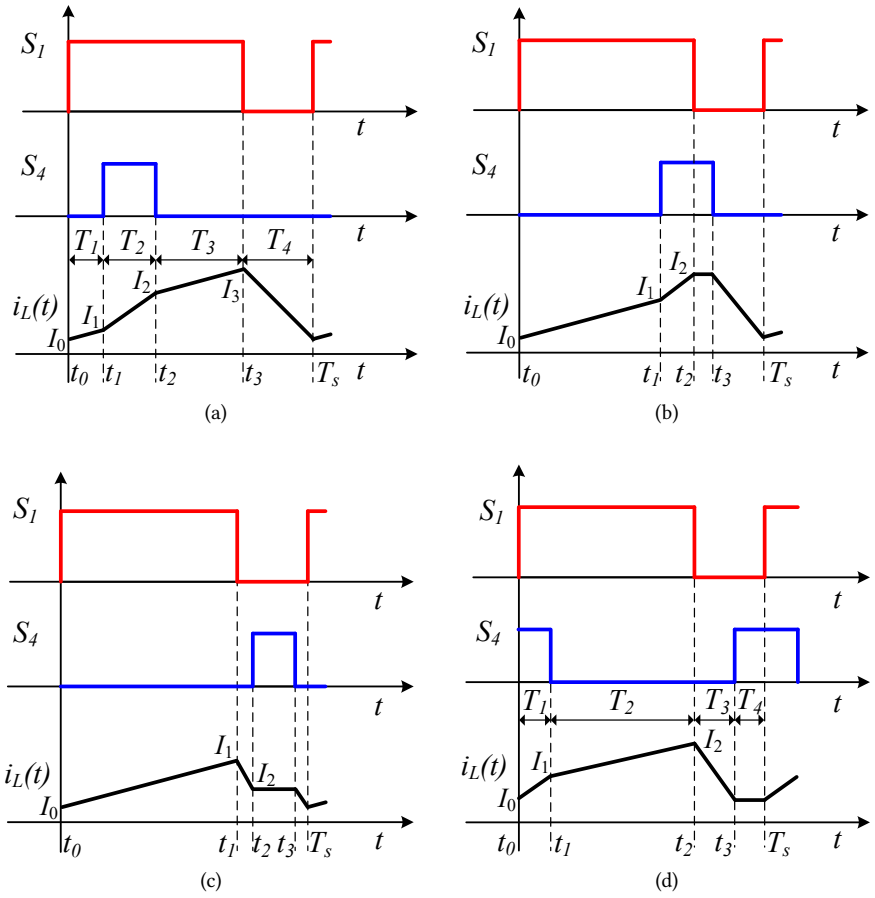


Figure 3.4: All four possible modulation cases when $V_1 > V_2$ under buck-boost-type mode with $d_1 > d_2$.

Figure 3.4 shows all four possible modulation cases when $V_1 > V_2$. It should be noted that the modulations with boundary overlapping are not drawn since they are special cases.

In order to turn on the switches under ZVS condition, the switching current during the dead time needs to first freewheel through the MOSFET body diode, then the MOSFET to be switched can be turned on at zero drain-source voltage due to the low forward voltage drop of the body diode. So, the ZVS turn-on in a four-switch buck+boost converter requires the inductor current to be negative during the switching-on transition for S_1 and S_4, and to be positive while turning on S_2 and S_3.

The requirements for the four switches to realize soft switching with the modulation cases shown in Figure 3.4 are: for Figure 3.4(a), $I_1 < 0$ and $I_2 > 0$; for Figure 3.4(b), $I_1 < 0$; for Figure 3.4(d), $I_0 < 0$ and $I_1 > 0$. However, for Figure 3.4(c), it is impossible to realize ZVS for all the switches since I_2 has to be positive (ZVS turn-on of S_3) and negative (ZVS turn-on of S_4) simultaneously.

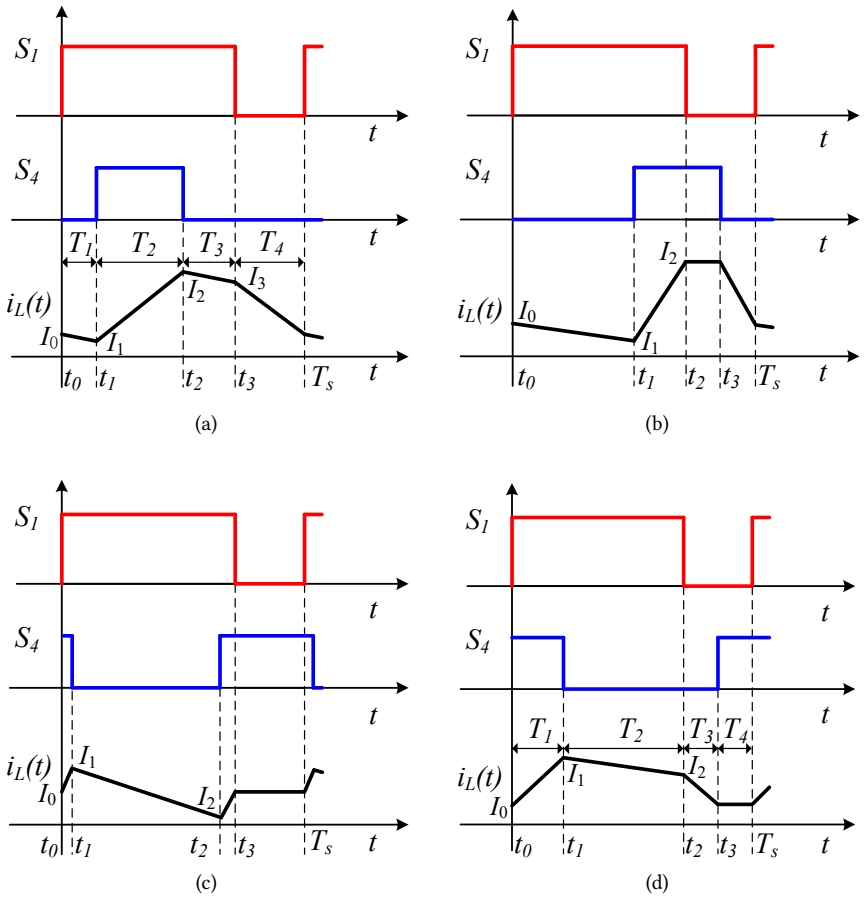


Figure 3.5: All four possible modulation cases when $V_1 < V_2$ under buck-boost-type mode with $d_1 > d_2$.

When considering the modulation case given in Figure 3.4(b), it is not a good choice since both I_0 and I_1 are negative, thus I_2 should be positive to transfer power from the input to output side and the value of I_2 could be considerably large, which could bring high current stresses to other components. Therefore, only the modulation cases in Figure 3.4(a) and Figure 3.4(d) will be considered in this work.

Case When $V_1 < V_2$

From (3.4), one has

$$d_1 + d_2 > 1. \tag{3.8}$$

Figure 3.5 shows all four possible modulation cases when $V_1 < V_2$. Based on the ZVS conditions mentioned earlier, the requirements for the four switches to achieve soft switching in Figure 3.5 are: for Figure 3.5(a), $I_0 < 0$ and $I_3 > 0$; for Figure 3.5(b), $I_0 < 0$; for Figure 3.5(d),

$I_0 < 0$ and $I_2 > 0$. Similar to the case of Figure 3.4(c), for Figure 3.5(c), it is also impossible to realize ZVS for all the switches. The modulation of Figure 3.5(b) also suffers from high peak current of I_2. Therefore, the modulation cases in Figure 3.5(a) and Figure 3.5(d) will be considered.

3.2.3 Rms Value of the Inductor Current with Phase Shift

This section gives the closed-form analytical equations of the inductor current rms value under ZVS conditions. In fact, this value also determines the conduction losses of the MOSFETs, since

$$I_{\text{rms\_}S_1}^2 + I_{\text{rms\_}S_2}^2 = I_{\text{rms\_}S_3}^2 + I_{\text{rms\_}S_4}^2 = I_{\text{rms\_}L}^2. \tag{3.9}$$

$I_{\text{rms\_}S_1}$–$I_{\text{rms\_}S_4}$ are the current rms values through channels of S_1–S_4, and $I_{\text{rms\_}L}$ is the inductor current rms value.

Case When $V_1 > V_2$

Herein, I_1 for the modulation case in Figure 3.4(a) and I_0 in Figure 3.4(d) are selected as a fixed negative value for the variable-frequency ZVS modulation.

In Figure 3.4(a),

$$T_1 + T_2 + T_3 + T_4 = T_s. \tag{3.10}$$

T_1 is defined as $T_1 = \alpha T_s$, α is the phase shift between S_1 and S_4. Therefore, T_2, T_3 and T_4 are

$$T_2 = d_2 T_s, T_3 = (d_1 - d_2 - \alpha)T_s, T_4 = (1 - d_1)T_s. \tag{3.11}$$

The inductor current in a switching period is given below with $t_0 = 0$,

$$i_L(t) = \begin{cases} I_0 + \dfrac{V_1 - V_2}{L} t, & 0 < t \le t_1 \\ i_L(t_1) + \dfrac{V_1}{L}(t - t_1), & t_1 < t \le t_2 \\ i_L(t_2) + \dfrac{V_1 - V_2}{L}(t - t_2), & t_2 < t \le t_3 \\ i_L(t_3) - \dfrac{V_2}{L}(t - t_3), & t_3 < t \le T_s. \end{cases} \tag{3.12}$$

According to (3.12), express I_0, I_2 and I_3 by I_1, one can obtain

$$\begin{cases} I_0 = I_1 - \dfrac{V_1 - V_2}{L} \alpha T_s \\ I_2 = I_1 + \dfrac{V_1}{L} d_2 T_s \\ I_3 = I_1 + \dfrac{V_1 - V_2}{L}(d_1 - \alpha)T_s + \dfrac{V_2}{L} d_2 T_s. \end{cases} \tag{3.13}$$

Since the power is only transferred when S_3 is on, so, the average output current is

$$I_{\text{out}} = \frac{I_0 + I_1}{2}\alpha + \frac{I_2 + I_3}{2}(d_1 - d_2 - \alpha) + \frac{I_3 + I_0}{2}(1 - d_1), \tag{3.14}$$

based on (3.4), (3.13), (3.14), after simplification, (3.15) can be derived as

$$Lf_s = \frac{\frac{V_1}{2}[d_1(1-d_1)+d_2(d_1-d_2)-2\alpha(1-d_1)]}{I_{\text{out}}-I_1(1-d_2)}. \tag{3.15}$$

f_s is the switching frequency. According to (3.45) derived in Appendix showing the rms value calculation of a general polyline function, the rms value of the inductor current is

$$\begin{aligned} &I_{\text{rms\_}L} \\ &= \sqrt{\alpha\frac{I_0^2+I_1^2+I_0I_1}{3}+d_2\frac{I_1^2+I_2^2+I_1I_2}{3}+(d_1-d_2-\alpha)\frac{I_2^2+I_3^2+I_2I_3}{3}+(1-d_1)\frac{I_0^2+I_3^2+I_0I_3}{3}}. \end{aligned} \tag{3.16}$$

According to Figure 3.4(a) and (3.15), α should satisfy

$$0 \le \alpha < \min\{d_1-d_2, \frac{d_1(1-d_1)+d_2(d_1-d_2)}{2(1-d_1)}\}. \tag{3.17}$$

For the case in Figure 3.4(d), the phase shift between S_1 and S_4 is defined by T_4, which is $T_4 = -\beta T_s$ and β is defined as a negative value. So, T_1, T_2 and T_3 are

$$T_1 = (d_2+\beta)T_s, T_2 = (d_1-d_2-\beta)T_s, T_3 = (1-d_1+\beta)T_s. \tag{3.18}$$

The inductor current in a switching period is

$$i_L(t) = \begin{cases} I_0 + \dfrac{V_1}{L}t, & 0 < t \le t_1 \\ i_L(t_1) + \dfrac{V_1-V_2}{L}(t-t_1), & t_1 < t \le t_2 \\ i_L(t_2) - \dfrac{V_2}{L}(t-t_2), & t_2 < t \le t_3 \\ I_0, & t_3 < t \le T_s. \end{cases} \tag{3.19}$$

According to (3.19) and by relating the values of I_1 and I_2 to I_0, one can derive

$$\begin{cases} I_1 = I_0 + \dfrac{V_1}{L}(d_2+\beta)T_s \\ I_2 = I_0 + \dfrac{V_1}{L}d_1T_s - \dfrac{V_2}{L}(d_1-d_2-\beta)T_s. \end{cases} \tag{3.20}$$

The average output current is

$$I_{\text{out}} = \frac{I_1+I_2}{2}(d_1-d_2-\beta) + \frac{I_2+I_0}{2}(1-d_1+\beta). \tag{3.21}$$

After simplification, (3.22) can be derived as

$$Lf_s = \frac{\frac{V_1}{2}[d_1(1-d_1)+d_2(d_1-d_2)+\beta(2d_1-2d_2-\beta)]}{I_{\text{out}}-I_0(1-d_2)}. \tag{3.22}$$

Similar to (3.16), the inductor current rms value can also be derived, which is

$$\begin{aligned} &I_{\text{rms\_}L} = \\ &\sqrt{(d_2+\beta)\frac{I_0^2+I_1^2+I_0I_1}{3}+(d_1-d_2-\beta)\frac{I_1^2+I_2^2+I_1I_2}{3}+(1-d_1+\beta)\frac{I_2^2+I_0^2+I_2I_0}{3}+(-\beta)I_0^2}. \end{aligned} \tag{3.23}$$

According to Figure 3.4(d) and (3.22), the phase shift of β should satisfy: $-d_2 < \beta \le 0$.

Case When $V_1 < V_2$

Herein, both the current values of I_0 in Figure 3.5(a) and (d) are set as a fixed negative value for variable-frequency ZVS modulation.

For the case of Figure 3.5(a), the expression of the inductor current in a switching period is the same as (3.12) and by linking the values of I_1, I_2 and I_3 to I_0, one can obtain

$$\begin{cases} I_1 = I_0 + \dfrac{V_1 - V_2}{L}\alpha T_s \\ I_2 = I_0 + \dfrac{V_1}{L}(\alpha + d_2)T_s - \dfrac{V_2}{L}\alpha T_s \\ I_3 = I_0 + \dfrac{V_2}{L}(1 - d_1)T_s. \end{cases} \tag{3.24}$$

The expression of output current is the same as (3.14), therefore, (3.25) can be obtained as

$$Lf_s = \frac{\frac{V_1}{2}[d_1(1-d_1) + d_2(d_1 - d_2) - 2\alpha d_2]}{I_{\text{out}} - I_0(1-d_2)}. \tag{3.25}$$

According to Figure 3.5(a) and (3.25), α should satisfy

$$0 \le \alpha < \min\{d_1 - d_2, \frac{d_1(1-d_1) + d_2(d_1-d_2)}{2d_2}\}. \tag{3.26}$$

For the modulation case of Figure 3.5(d), the same formula of (3.22) can be obtained with $d_1 - 1 < \beta \le 0$.

The inductor current rms value can then be calculated accordingly for both cases and it is skipped here.

Case When $V_1 = V_2$

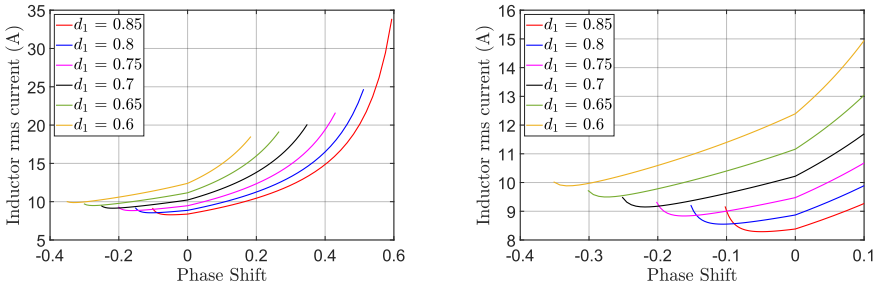
This is the boundary case between $V_1 > V_2$ and $V_1 < V_2$. By comparing (3.15) and (3.25), when $V_1 = V_2$, one has $d_1 + d_2 = 1$ and $I_0 = I_1$, so, the calculated result of Lf_s is the same from these two equations.

Independence between Inductance and Inductor Current rms Value

For variable-frequency ZVS modulation, the rms value of the inductor current is independent of its inductance if the frequency is not limited. To prove this, take the case in Figure 3.4(a) as an example, substitute the switching frequency derived from (3.15) into (3.13), then

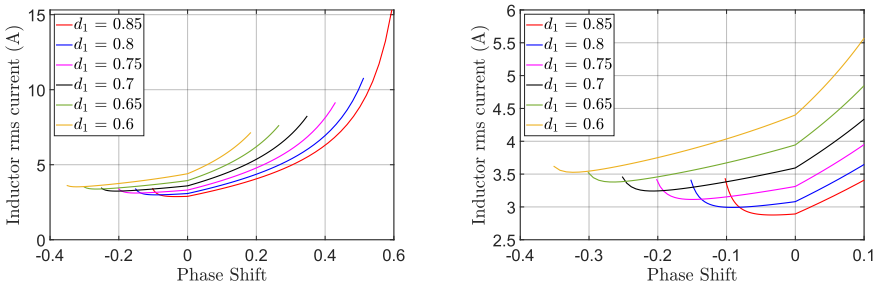
$$\begin{cases} I_0 = I_1 - \dfrac{(V_1 - V_2)\alpha}{k}, \quad I_2 = I_1 + \dfrac{V_1 d_2}{k}, \\ \\ I_3 = I_1 + \dfrac{(V_1 - V_2)(d_1 - \alpha)}{k} + \dfrac{V_2 d_2}{k}. \end{cases} \tag{3.27}$$

In (3.27), $k = \dfrac{\frac{V_1}{2}[d_1(1-d_1) + d_2(d_1-d_2) - 2\alpha(1-d_1)]}{I_{\text{out}} - I_1(1-d_2)}$. By checking these equations, the inductor variable L is eliminated. According to the rms value expression of (3.16), L will not influence the inductor current rms value. Furthermore, the corner value of the inductor current also does not depend on the inductance. The proof is similar for other cases. This property makes the conclusions drawn in this work more general.



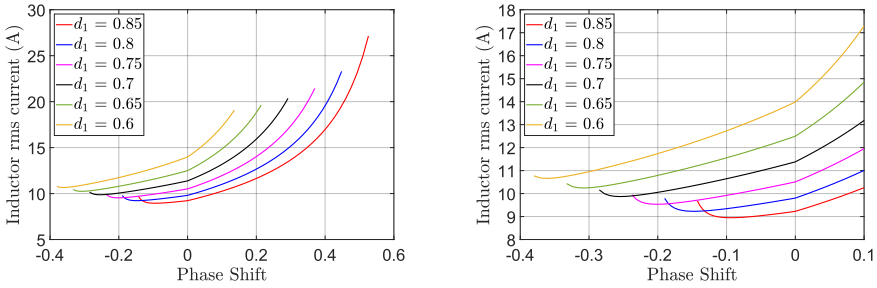
(a) (b)

Figure 3.6: Inductor rms current at different values of d_1, $V_1 = 420$ V, $V_2 = 400$ V, $P_o = 3$ kW, ZVS current is -2 A. Phase shift range is limited by ZVS. (b) is a partial enlargement of (a).



(a) (b)

Figure 3.7: Inductor rms current at different values of d_1, $V_1 = 420$ V, $V_2 = 400$ V, $P_o = 1$ kW, ZVS current is -2 A. Phase shift range is limited by ZVS. (b) is a partial enlargement of (a).



(a) (b)

Figure 3.8: Inductor rms current at different values of d_1, $V_1 = 380$ V, $V_2 = 400$ V, $P_o = 3$ kW, ZVS current is -2 A. Phase shift range is limited by ZVS. (b) is a partial enlargement of (a).

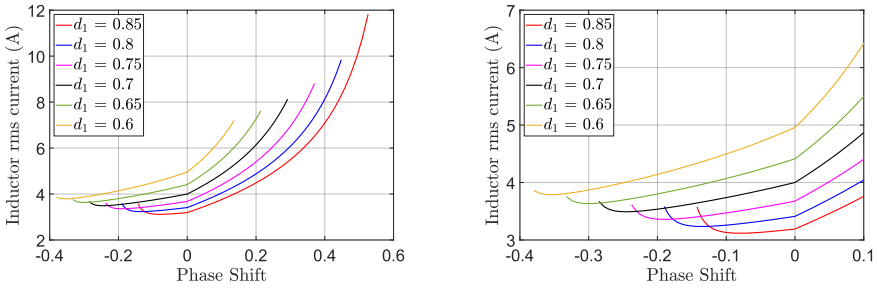


Figure 3.9: Inductor rms current at different values of d_1, $V_1 = 380$ V, $V_2 = 400$ V, $P_o = 1$ kW, ZVS current is -2 A. Phase shift range is limited by ZVS. (b) is a partial enlargement of (a).

Duty Cycle Influence on Inductor rms Current

A specific example with parameters closer to the final design will be given to show the current rms value with phase shift.

The selected parameters are: The power of P_o is selected at two values of 3 kW and 1 kW, V_2 is 400 V, ZVS current is set to -2 A as an example, i.e., $I_1 = -2$ A for Figure 3.4(a), $I_0 = -2$ A for Figure 3.4(d), Figure 3.5(a) and (d), duty cycle of d_1 varies from 0.6 to 0.85.

According to the previous derived equations for inductor rms current calculation, the results of this example are shown in Figure 3.6 to 3.9. The phase shift range is restricted by ZVS.

From Figures 3.6 to 3.9, it can be seen that the inductor current rms value increases as α increases. Generally, a larger value of d_1 is beneficial in terms of conduction loss reduction due to a smaller rms value of the inductor current. With a larger value selection of d_1, the negative phase shift range for ZVS is also smaller. Although the optimum phase shift in terms of minimum current rms value is not zero, the difference between the minimum rms value and the one at zero phase shift is negligible when d_1 is selected to be a larger enough and reasonable value, e.g., 0.8. Therefore, to make the converter operation more convenient and robust in practice, the phase shift is selected at zero in the buck-boost-type mode, i.e., three-segment inductor current mode modulation is adopted.

Once this modulation is adopted, then (3.15), (3.22) and (3.25) can be simplified as

$$Lf_s = \frac{\frac{V_1}{2}[d_1(1-d_1)+d_2(d_1-d_2)]}{I_{\text{out}} - I_0(1-d_2)}. \tag{3.28}$$

I_0 in (3.28) is shown in Figure 3.10.

The current values of I_1 and I_2 can also be simplified as

$$I_1 = I_0 + \frac{V_1}{k}d_2, \quad I_2 = I_0 + \frac{V_2}{k}(1-d_1). \tag{3.29}$$

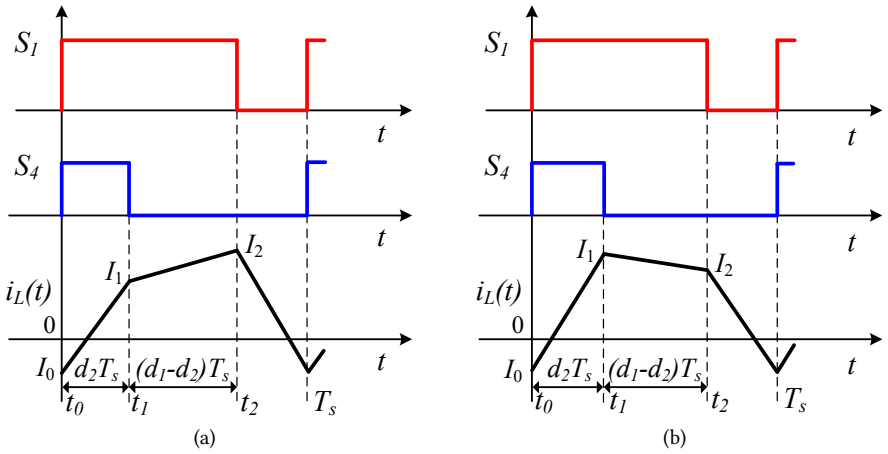


Figure 3.10: Modulation in buck-boost-type mode with zero phase shift. (a) $V_1 > V_2$; (b) $V_1 < V_2$.

In (3.29), $k = \dfrac{\frac{V_1}{2}[d_1(1-d_1)+d_2(d_1-d_2)]}{I_{\text{out}} - I_0(1-d_2)}$. The inductor current rms value is

$$I_{\text{rms\_}L} = \sqrt{d_2\frac{I_0^2+I_1^2+I_0I_1}{3} + (d_1-d_2)\frac{I_1^2+I_2^2+I_1I_2}{3} + (1-d_1)\frac{I_2^2+I_0^2+I_2I_0}{3}}. \tag{3.30}$$

Duty Cycle Influence on ZVS Power Range under Buck-Boost-type Mode
Different from the TCM-ZVS buck or boost-type modulation, which could have full power ZVS range, for the adopted modulation strategy in buck-boost-type mode, the current value of I_1 shown in Figure 3.10(a) or I_2 in Figure 3.10(b) should also satisfy the minimum ZVS current requirement. When the load decreases to a certain extent when I_1 or I_2 reduces to $-I_0$, i.e., the ZVS current, then switch S_3 or S_2 starts to lose ZVS turn-on.

In Figure 3.10(a) during buck-type mode, let $I_1 = -I_0 = I_{\text{zvs}}$, the power level when the switch S_3 starts to lose ZVS turn-on can be expressed as

$$P_{\text{zvs\_min}} = V_2 I_{\text{zvs}} \frac{(d_1-d_2)(1-d_1)}{d_2}. \tag{3.31}$$

In Figure 3.10(b) during boost-type mode, let $I_2 = -I_0 = I_{\text{zvs}}$, the power level when the switch S_2 starts to lose ZVS turn-on is

$$P_{\text{zvs\_min}} = V_2 I_{\text{zvs}} \frac{d_2(1-d_2)(d_1-d_2)}{d_1(1-d_1)}. \tag{3.32}$$

Equations (3.31) and (3.32) lead to the same result when $V_1 = V_2$ since $d_1 + d_2 = 1$.

Figure 3.11 shows the duty cycle influence on the value of $\dfrac{P_{\text{zvs\_min}}}{V_2 I_{\text{zvs}}}$. As it can be seen, with a larger duty cycle of d_1, the converter is more likely to lose ZVS of a certain switch. Due to the possible ZVS loss, the efficiency under buck-boost-type mode will drop more

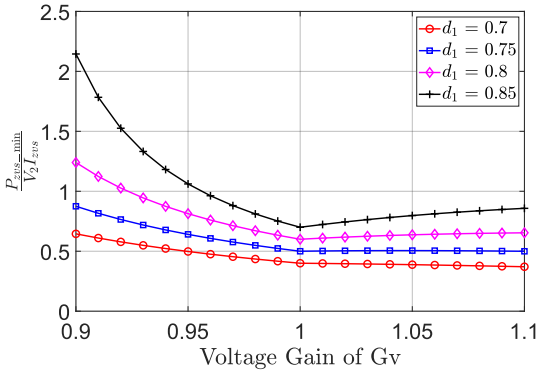


Figure 3.11: Duty cycle influence on $\frac{P_{\text{zvs\_min}}}{V_2 I_{\text{zvs}}}$.

prominently in light load compared with the TCM-ZVS buck or boost-type modulation schemes. This can be seen by the experimental results of the efficiency curves discussed in Section 3.4. However, a larger value of d_1 is beneficial in terms of conduction losses, which has been discussed previously. So, in this work, combined with consideration of d_2 given in Figure 3.3, d_1 will be selected at 0.8 in the transition mode.

3.2.4 TCM-ZVS Buck, Boost Operation

When the converter operates out of the transition zone, simply, only buck or boost mode could be adopted. The TCM-ZVS modulation will be briefly described as follows.

TCM-ZVS Buck Operation

In buck-type mode, the switch S_3 is always on. The switching waveforms is given in Figure 3.12(a). The equations under this mode can be written as

$$I_1 = I_0 + \frac{V_1 - V_2}{L} d_1 T_s, \quad V_2 = d_1 V_1, \quad I_{\text{out}} = \frac{I_0 + I_1}{2}. \tag{3.33}$$

I_0 and I_1 are the minimum and maximum inductor current values. After simplification, the switching frequency is derived as

$$f_s = \frac{V_1 d_1 (1 - d_1)}{2L(I_{\text{out}} - I_0)}. \tag{3.34}$$

TCM-ZVS Boost Operation

In boost-type mode, the switch S_1 is always on. Figure 3.12(b) shows the switching waveforms of the TCM-ZVS boost operation. The equations for this mode are

$$I_1 = I_0 + \frac{V_1}{L} d_2 T_s, \quad V_2 = \frac{V_1}{1 - d_2}, \quad I_{\text{out}} = \frac{I_0 + I_1}{2}(1 - d_2). \tag{3.35}$$

After simplification, the switching frequency is

$$f_s = \frac{V_1 d_2 (1 - d_2)}{2L[I_{\text{out}} - I_0(1 - d_2)]}. \tag{3.36}$$

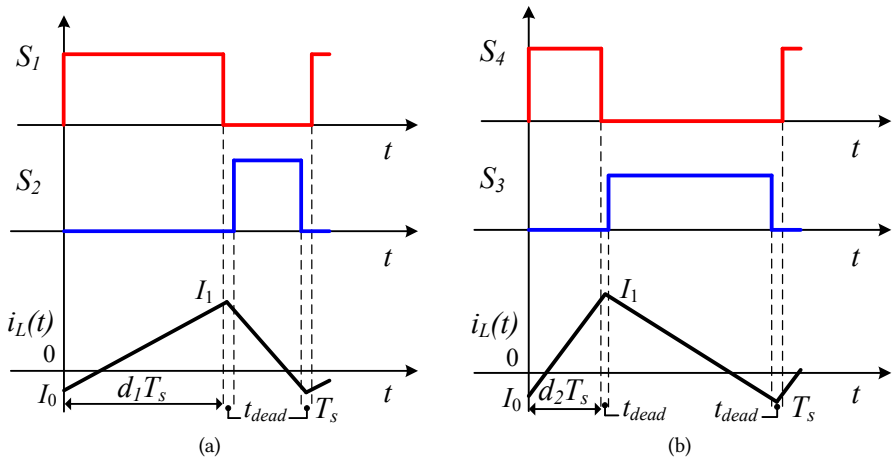


Figure 3.12: TCM-ZVS inductor current waveforms and PWM signals. (a) buck-type mode. (b) boost-type mode.

In fact, the frequency for TCM-ZVS buck or boost-type modulation can also be derived by simply applying the corresponding duty cycle values to (3.28). For example, substitute $d_2 = 0$ into (3.28), then the frequency for TCM-ZVS buck-type modulation is derived, which is the same as (3.34).

3.3 Design Considerations

After determining the modulation scheme described in Section 3.2, some key factors must be considered carefully including the switching current of the inductor for ensuring the ZVS turn-on operation, the inductance value selection based on the switching frequency range, and the inductor design.

3.3.1 Inductance Value Selection

Before the inductor design, the value of the inductance needs to be determined first since this will influence the switching frequency range of the converter. In this work, the switching frequency is chosen between 20 kHz and 160 kHz based on the gate driver capability.

Since the switching frequency depends on the ZVS current, as a first step estimation described in [63] and [64], the inductor current to achieve ZVS should satisfy

$$I_{\text{zvs}} \geq \frac{2C_{\text{oss}} \cdot \max\{V_1, V_2\}}{t_{\text{dead}}}. \tag{3.37}$$

I_{zvs} is the absolute value of the instantaneous inductor current at the switching instant, C_{oss} is the lump equivalent output capacitance of the MOSFET and t_{dead} is the dead time. To build the converter prototype, each MOSFET switch was composed of three hard-paralleled SMD SiC MOSFETs of G3R75MT12J, according to its datasheet, the voltage-related effective output capacitance is 85 pF, therefore, C_{oss} is assumed to be 255 pF. By considering the

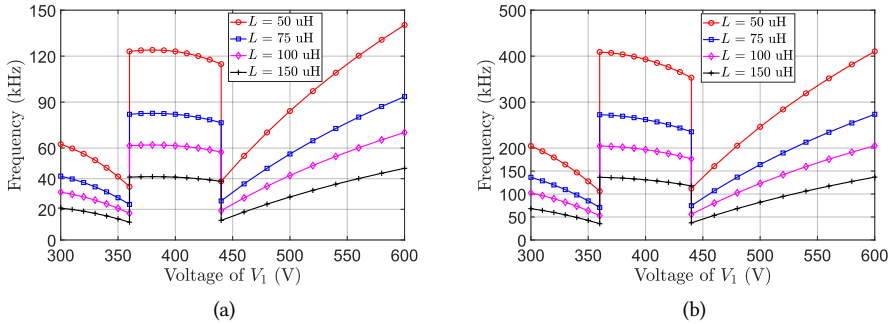


Figure 3.13: Switching frequencies (without frequency restrictions) with different inductance values under three-mode modulations, $I_0 = -2$ A, $d_1 = 0.8$ in buck-boost-type mode, $V_2 = 400$ V. (a) $P_o = 3$ kW. (b) $P_o = 500$ W.

Table 3.2: Inductance and equivalent resistance of the inductor

	20 kHz	60 kHz	100 kHz	160 kHz
L (μH)	102.79	102.84	102.70	102.65
R_s (mΩ)	32.41	68.45	96.69	187.14

dead time value around 100 to 500 ns for SiC MOSFETs [68], the ZVS current is selected as -2 A to determine the switching frequency.

The switching frequencies under different inductance values are given in Figure 3.13 with operating power at 3 kW and 500 W, respectively. As it can be seen, if there is no frequency restrictions, the frequency at light load will become relatively high, therefore, it is necessary to set a switching frequency limit.

By checking the frequency curve, one can find that there are two abrupt frequency changes at the boundary of different modes, i.e., the boundary between boost-type and buck-boost-type modes, and buck-boost-type and buck-type modes. In this work, the inductance of 100 μH will be adopted.

The inductor was built using PM 74/59 core with N87 material. The inductance and the equivalent series resistance measured by Agilent 4294A precision impedance analyzer are given in Table 3.2 at different frequencies.

3.3.2 Resonant Circuit Analysis during Dead Time

A precondition for (3.37) is that the inductor current is assumed to be constant during the dead time, which might not be true in some conditions, such as the cases when a longer dead time or a smaller inductance is adopted [32], [69], which could possibly bring the negative inductor current back to zero and then resonate with the output capacitors causing a loss of the desired ZVS turn-on. Besides, a ZVS current with an unnecessary larger absolute value could also lead to a higher conduction loss due to a higher rms current. Hence, it is important and meaningful to study the resonant behavior during the dead time in a more detailed way [69].

Below, the resonant behavior under buck-type and buck-boost-type modes will be

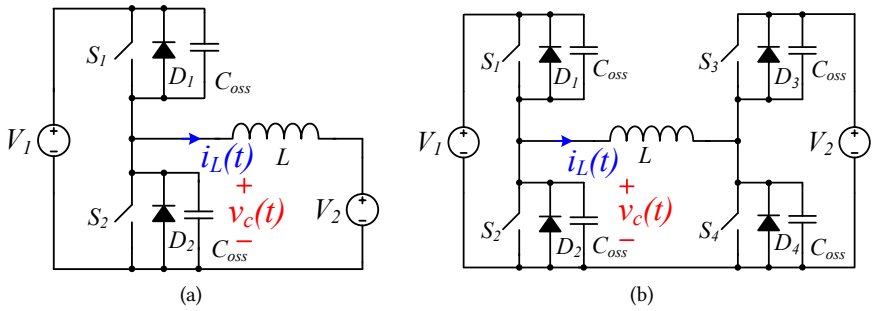


Figure 3.14: Equivalent circuit during resonant interval. (a) buck-type mode. (b) buck-boost-type mode.

studied and compared since in buck-type mode, the input voltage can be as high as 600 V, which proposes a higher requirement to achieve ZVS than in boost-type mode.

Buck-type Mode

The equivalent circuit during resonant interval under buck-type mode is redrawn in Figure 3.14(a).

Suppose the initial inductor current at the beginning of the dead time when S_1 and S_2 are both off is $-I_{zvs}$ (I_{zvs} is a positive value). The drain-source voltage of S_2 [$v_c(t)$] and the inductor current [$i_L(t)$] during the resonant interval before conduction of the upper diode are

$$i_L(t) = -(I_{zvs}\cos\omega_0 t + \frac{V_2}{Z_0}\sin\omega_0 t) \tag{3.38}$$

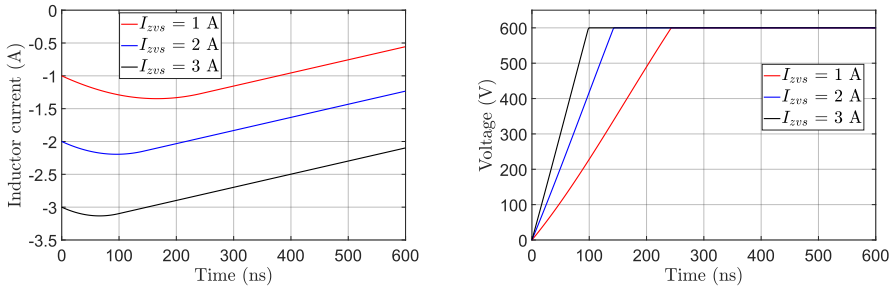
$$v_c(t) = V_2(1-\cos\omega_0 t) + Z_0 I_{zvs}\sin\omega_0 t, \tag{3.39}$$

where $\omega_0 = \frac{1}{\sqrt{2LC_{oss}}}$, $Z_0 = \sqrt{\frac{L}{2C_{oss}}}$. When $v_c(t)$ reaches the value of V_1 at the moment of $t = \frac{1}{\omega_0}[\arcsin(\frac{V_2}{\sqrt{k^2+V_2^2}}) + \arcsin(\frac{V_1-V_2}{\sqrt{k^2+V_2^2}})]$ with $k = I_{zvs}Z_0$, the upper diode will conduct, and then the inductor current will decrease (the absolute value) linearly. Figure 3.15 shows the curves of $v_c(t)$ and $i_L(t)$ with three different initial inductor current values at -1 A, -2 A and -3 A.

Buck-Boost-type Mode

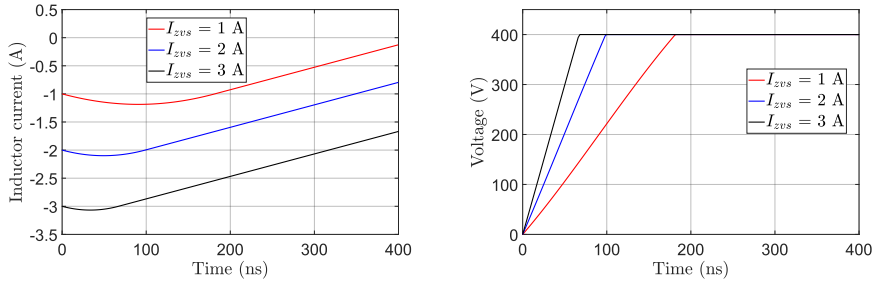
The equivalent circuit during the resonant interval under buck-boost-type mode is redrawn in Figure 3.14(b).

There is a slight difference in time for the drain-source voltages of S_1 and S_4 to reach zero if V_1 is not equal to V_2, however, this time difference is relatively small and to simplify the analysis, one can assume $V_1 = V_2 = V_s$. This assumption makes sense since in buck-boost-type mode, the difference of V_1 and V_2 is relatively small. The equations of $i_L(t)$ and



(a) (b)

Figure 3.15: $i_L(t)$ and $v_c(t)$ when $V_1 = 600$ V and $V_2 = 400$ V, $L = 100$ μH, $C_{\text{oss}} = 255$ pF. (a) inductor current of $i_L(t)$. (b) voltage of $v_c(t)$.



(a) (b)

Figure 3.16: $i_L(t)$ and $v_c(t)$ when $V_1 = V_2 = 400$ V, $L = 100$ μH, $C_{\text{oss}} = 255$ pF. (a) inductor current of $i_L(t)$. (b) voltage of $v_c(t)$.

$v_c(t)$ during the resonant interval before the conduction of diodes are

$$i_L(t) = -(I_{\text{zvs}} \cos \omega_0 t + \frac{V_s}{Z_0} \sin \omega_0 t) \tag{3.40}$$

$$v_c(t) = \frac{1}{2}[V_s(1 - \cos \omega_0 t) + Z_0 I_{\text{zvs}} \sin \omega_0 t], \tag{3.41}$$

where $\omega_0 = \dfrac{1}{\sqrt{LC_{\text{oss}}}}$, $Z_0 = \sqrt{\dfrac{L}{C_{\text{oss}}}}$. When diodes D_1 and D_4 conduct, the current of the inductor decreases (the absolute value) linearly. The curves of $i_L(t)$ and $v_c(t)$ are given in Figure 3.16.

Compared with the estimation equation of (3.37), the equations during the resonant interval show more information, which helps to better determine the needed switching ZVS current and dead time. For example, by solving (3.41) to make v_c equal to V_s, the

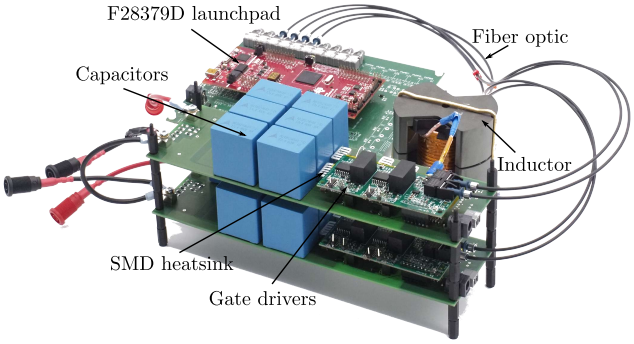


Figure 3.17: Four-switch buck+boost converter prototype.

minimum dead time needed to achieve ZVS turn-on is

$$t_{\min} = \frac{1}{\omega_0} \arcsin\left(\frac{2kV_s}{k^2 + V_s^2}\right), \tag{3.42}$$

where $k = I_{zvs}Z_0$. Substitute (3.42) back into (3.40), then the inductor current value returns back to its initial value of $-I_{zvs}$.

It should be noted that in reality, the value of C_{oss} is nonlinear and voltage-dependent. It is better to find the appropriate current value through some experimental tests. Based on the discussion above, to start the test of the converter for ZVS realization, a switching current of -2 to -3 A and a dead time of 200 to 300 ns is a suitable choice for the designed prototype.

3.4 Experimental Verification

In order to verify the proposed control strategy, a 300–600 V input, 400 V output four-switch buck+boost converter with rated power of 3 kW was designed and constructed. The converter is set to operate with a power from 10% to full rated load and the efficiency will be measured with a Yokogawa WT500 power analyzer.

The converter prototype is shown in Figure 3.17. Three SMD SiC MOSFETs of G3R75MT12J were connected in parallel to form a single switch to increase the current rating capability.

After hardware commissioning, the negative ZVS switching current was selected to be -2.5 A and the dead time was set to 200 ns. The calculated power loss distributions at the worst case when $V_1 = 300$ V, $V_2 = 400$ V and $P_o = 3$ kW are given in Table 3.3.

3.4.1 Steady State Operation

Since there are three operating modes of this buck+boost converter, so, the experimental results at several typical input voltage values of these three modes will be given.

Figure 3.18 shows the experimental results in boost-type mode at 3 kW when V_1 is 300 V and V_2 is 400 V. It can be seen that the MOSFET S_4 turned on at zero voltage. The measured efficiency was 99.30%.

In the buck-boost-type mode, V_1 was tested at three typical voltage values of 380 V, 400 V and 420 V respectively, and d_1 was fixed at 0.8. The measurement results are given in

Table 3.3: Worst case ($V_1 = 300$ V, $V_2 = 400$ V) calculated power losses distribution and converter efficiency

Total losses	15.63 W
Semiconductor	10.13 W
Winding	2.28 W
Core	3.10 W
Input capacitor	0.06 W
Output capacitor	0.06 W
Efficiency ≈ 99.48%	

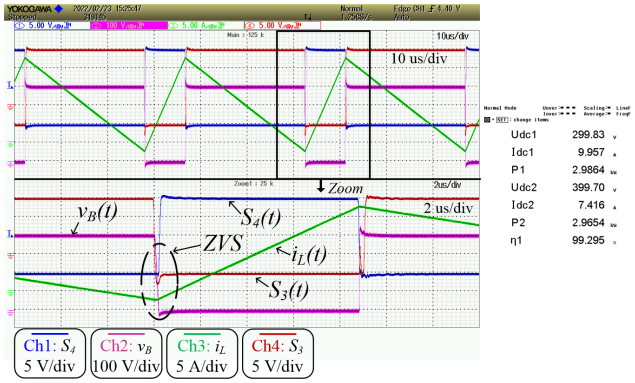


Figure 3.18: Boost-type operating mode: measured waveforms and efficiency at $V_1 = 300$ V and $V_2 = 400$ V, $P_o = 3$ kW. $S_4(t)$ is the gate-source voltage of S_4, $S_3(t)$ is the gate-source voltage of S_3, $i_L(t)$ is the inductor current, $v_B(t)$ is the voltage potential of point B relative to the bottom-side (or lower potential) dc-bus rail shown in Figure 3.1. Efficiency was measured by Yokogawa WT500 power analyzer. Udc1 and Idc1 are the values from input side while Udc2 and Idc2 are the values from the output side.

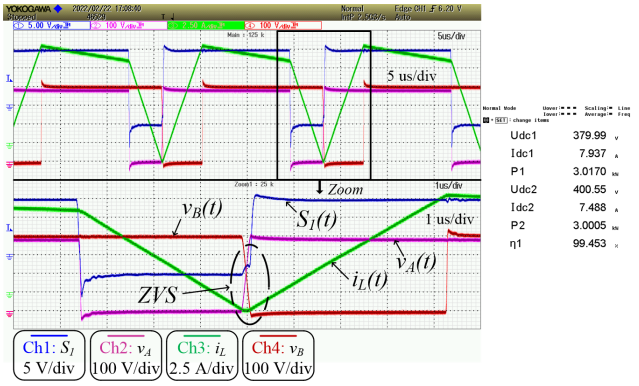
Figure 3.19. As it can be seen from the voltages of v_A and v_B at the switching point when i_L is -2.5 A, v_A reached V_1 while v_B dropped to zero when turning on S_1 and S_4, therefore, the ZVS turn-on of these two switches was achieved. Since the inductor current at the other two switching points were much larger, therefore, the ZVS turn-on of the four MOSFETs were all accomplished.

The measured result of the buck-type operating mode when V_1 is 500 V and 600 V is shown in Figure 3.20. It can be seen that v_A has reached V_1 when S_1 was turned on, so, S_1 has achieved ZVS turn-on and the measured power efficiency was 99.51% when V_1 is 500 V, and 99.39% when V_1 is 600 V.

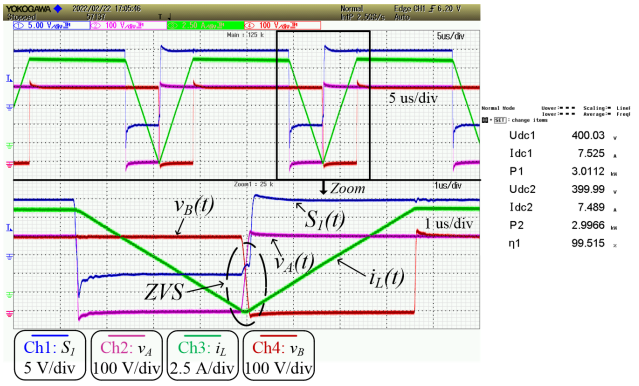
Efficiency curves at different input and output voltages are shown in Figure 3.21. Apart from the performance at 400 V output, the measured efficiency was also given at 360 V output, which covers the battery voltage range of most common commercial EVs.

It can be seen that in the power range from 1 kW to 3 kW, all the measured points show efficiency higher than 99% at 400 V output, i.e., between 99.2% and 99.6%.

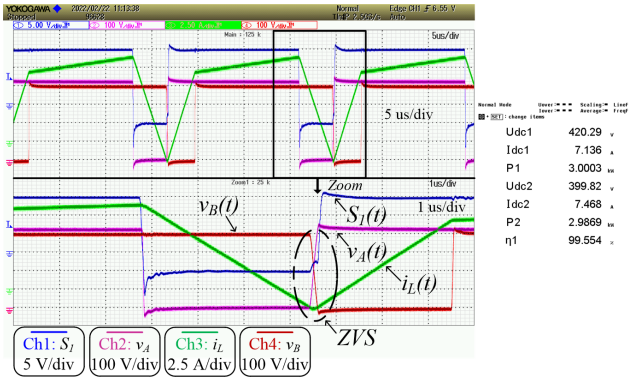
By comparing the efficiency curves at different input voltage values, one can find that the efficiency in the buck-boost-type mode drops more evidently in light load situations



(a)



(b)



(c)

Figure 3.19: Buck-boost-type operating mode: measured waveforms and efficiency at $V_1 = 380$, 400 and 420 V, $P_o = 3$ kW, $d_1 = 0.8$, $V_2 = 400$ V. $S_1(t)$ is the gate-source voltage of S_1, $v_A(t)$ is the voltage potential of point A relative to the bottom-side (or lower potential) dc-bus rail shown in Figure 3.1. (a) $V_1 = 380$ V. (b) $V_1 = 400$ V. (c) $V_1 = 420$ V.

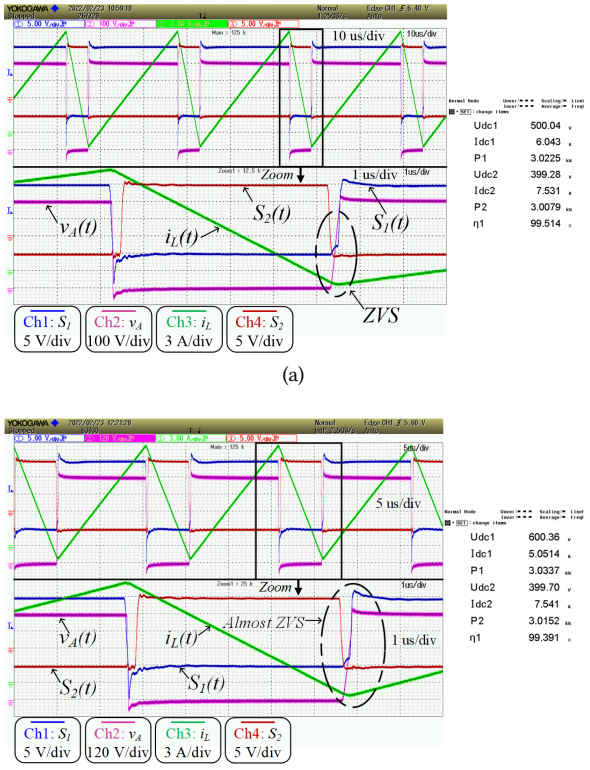


Figure 3.20: Buck-type operating mode: measured waveforms and efficiency at $V_1 = 500$ V and 600 V, $V_2 = 400$ V, $P_o = 3$ kW. $S_2(t)$ is the gate-source voltage of S_2. (a) $V_1 = 500$ V. (b) $V_1 = 600$ V.

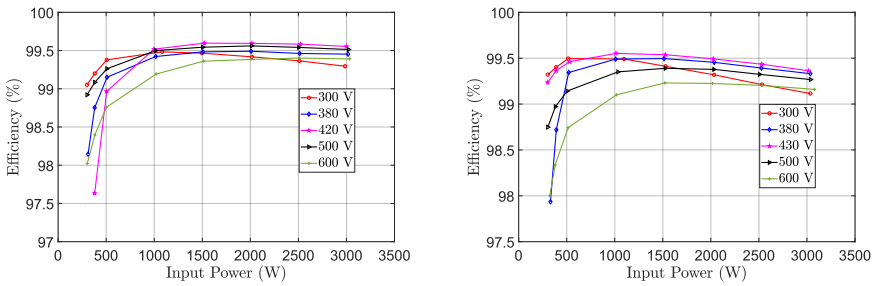


Figure 3.21: Measured power efficiency curves at different input and output voltages. (a) $V_2 = 400$ V. (b) $V_2 = 360$ V.

due to the ZVS turn-on loss of a certain switch. For example, Figure 3.22 shows the ZVS

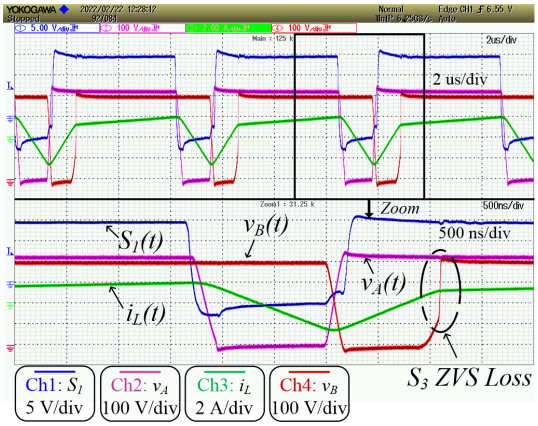


Figure 3.22: ZVS turn-on loss of S_3, $V_1 = 420$ V, $V_2 = 400$ V and $P_o = 380$ W.

turn-on loss of S_3 at 380 W when $V_1 = 420$ V and $V_2 = 400$ V, which can be seen from its sudden drain-source voltage change. As mentioned in Section 3.2, to decrease the duty cycle of S_1 is a possible solution to guarantee ZVS even in the light load condition. However, further optimization through dynamic duty cycle control is out of this work's scope.

Table 3.4: Volume of each part of the converter

	Inductor	Capacitors	Heatsink (With MOSFETs)	Driver
Volume (L)	0.18	0.325	0.027	0.085
Volume Percent (%)	29.2	52.7	4.4	13.8

The power density of this converter is 4.86 kW/L with the volume information of each part shown in Table 3.4.

As for the thermal performance of the converter, an estimation of temperature rise of the MOSFETs can be calculated. Taking the working condition of $V_1 = 300$ V, $V_2 = 400$ V and $P_o = 3$ kW as an example, with ZVS modulation scheme, the conduction losses for each MOSFET are as follows (Since three MOSFETs were in parallel to form a single switch, so, only the losses of one MOSFET is considered. For each MOSFET, one surface mount heatsink 7106DG was used): $P_{S_1\_each} = 1.64$ W, $P_{S_2\_each} = 0$ W, $P_{S_3\_each} = 1.23$ W and $P_{S_4\_each} = 0.51$ W. The 7106DG heatsink has a thermal resistance value around 20°C/W, so, the largest temperature rise would be around 33°C for switch S_1, and this temperature rise is completely acceptable.

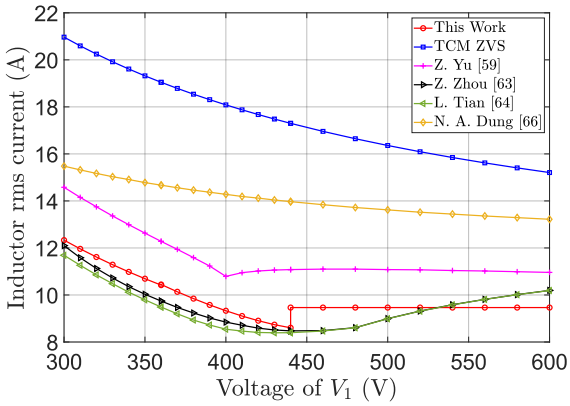
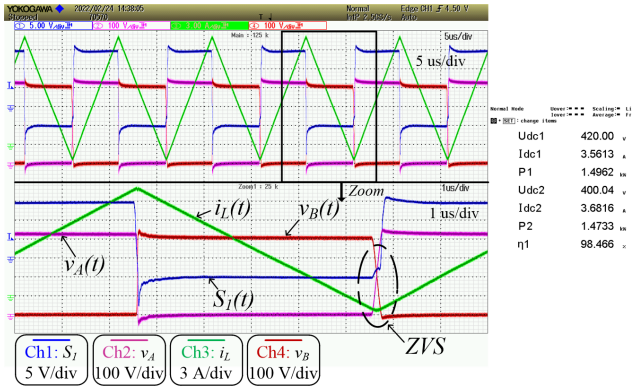


Figure 3.23: Inductor current rms value comparison under different modulation schemes. $V_2 = 400$ V, $P_o = 3$ kW, absolute value of ZVS current is 2.5 A.

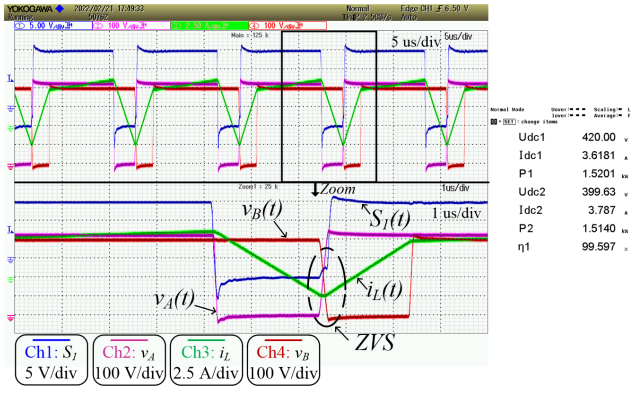
3.4.2 Benchmark with Different ZVS Modulation Schemes

Figure 3.23 compares the obtained inductor current rms value under different modulation schemes at full load. The TCM ZVS modulation is the method that the switches S_1 and S_4 turn on/off simultaneously. For both methods in [63] and [66], the inductor current rms value is calculated with an inductance of 100 μH and frequency of 50 kHz. For the method in [64], the inductance is 100 μH and the frequency varies between 42.5 kHz and 50 kHz. As it can be seen, the inductor current rms value proposed in [63] and [64] shows a smaller value in a wide range, however, [63] adopts a fixed-frequency four-segment inductor current mode modulation while a combination control of fixed- and variable-frequency modulation is adopted in [64], compared with the method in this work, the modulation techniques are different. Besides, the selection of the optimal switching times in [63] and [64] is more complicated.

Apart from the comparison of the current rms value under different modulation schemes, tests were also carried out between the TCM ZVS modulation and the proposed one in the buck-boost-type region. Due to the high peak inductor current in the TCM-ZVS operation, the power efficiency between 1500 W and 300 W was measured and compared. Figure 3.24 shows the measured results at 1500 W. As it can be seen, the power efficiency was improved by 1.13%, and the losses were reduced from 22.9 W to 6.1 W. The measured efficiency curves of these two schemes are presented in Figure 3.25.



(a)



(b)

Figure 3.24: Measured waveforms and efficiency at $V_1 = 420$ V, $V_2 = 400$ V, $P_o = 1500$ W. An efficiency improvement of 1.13% can be seen. (a) TCM-ZVS buck-boost-type operation. (b) ZVS scheme adopted in this work.

3.4.3 Mode Transition Operation

The mode transition is implemented based on the method given in Figure 3.26, $V_{2\text{ref}}$ is the reference value for the output voltage. In order to prevent the switching frequency from swinging frequently at the boundaries between the operational modes (cf., Figure 3.13), a hysteresis of ΔV was applied to avoid this issue.

The mode transition was tested at 1 kW and 400 V output. Figure 3.27 shows the mode transition results when the input voltage increases or decreases to cover all the possible cases in this work's study. For example, in Figure 3.27(a), it shows the transition from boost-type mode to buck-boost-type mode when V_1 increases from 350 V to 380 V. As it can be seen, there is no much visible oscillations of the inductor current during mode transitions.

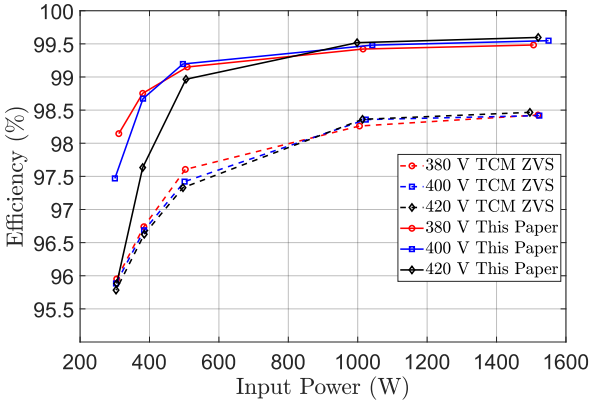


Figure 3.25: Comparison of measured efficiency results. The dotted lines represent the TCM buck-boost-type mode operation while the solid lines represent efficiency measured with the scheme adopted in this work.

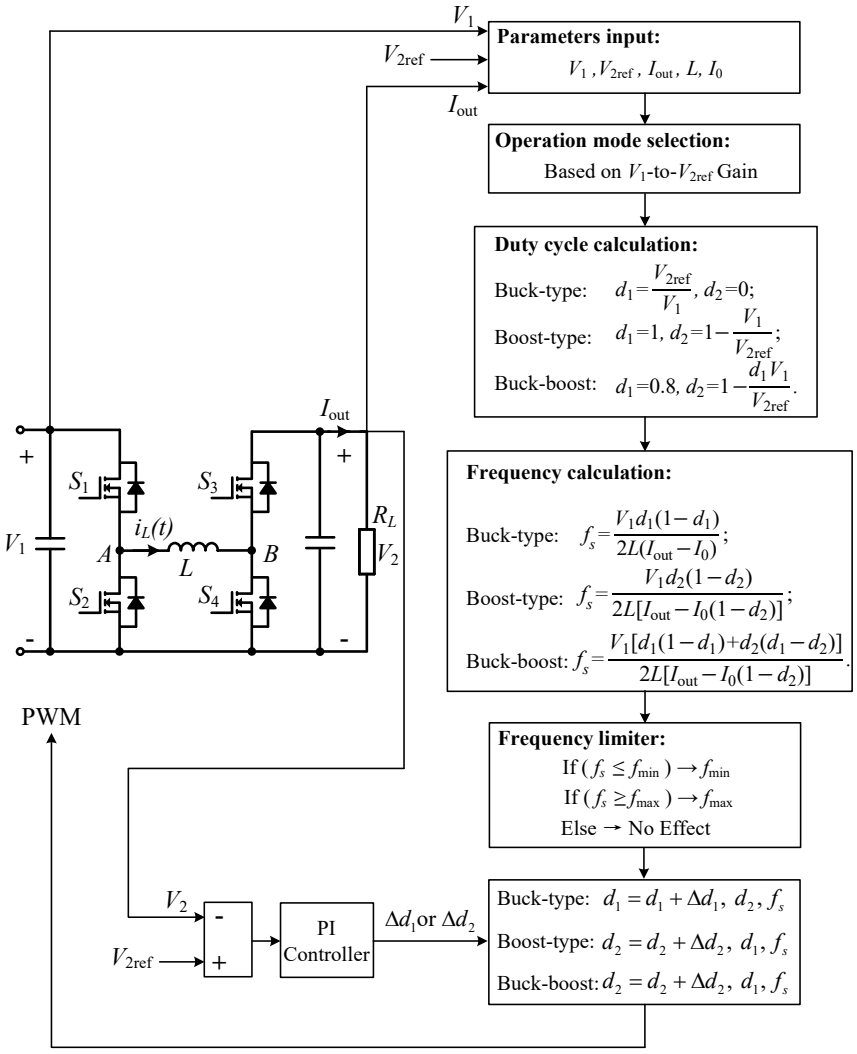


Figure 3.26: Closed-loop control algorithm implemented during mode transition test, I_0 is the switching ZVS current, which is −2.5 A.

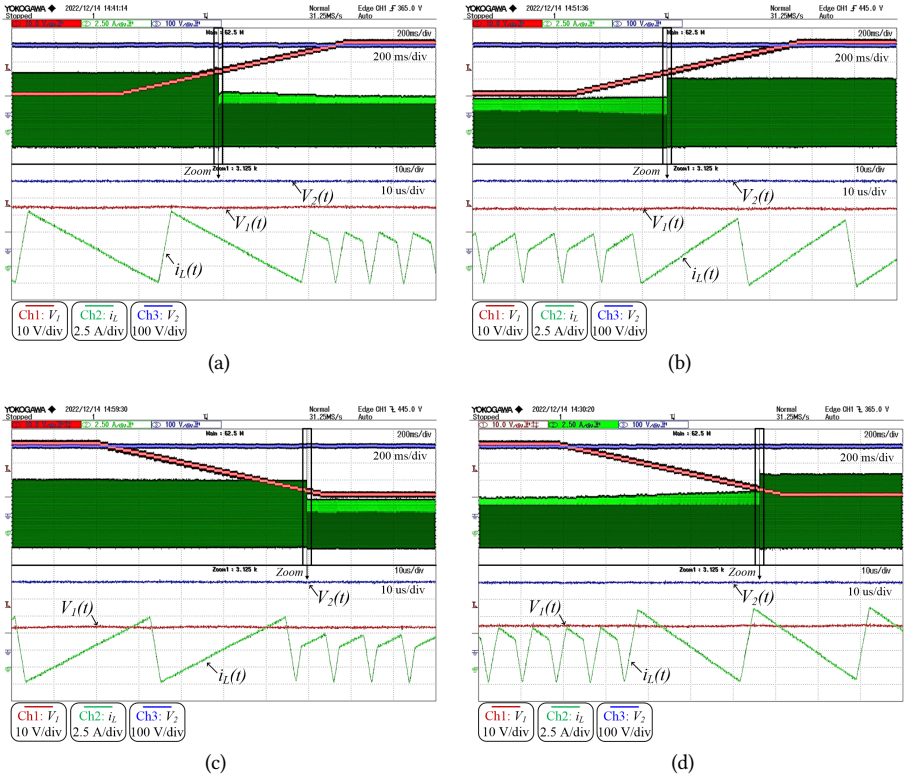


Figure 3.27: Mode transition tested at 1 kW and 400 V output. (a) $V_1 = 350 - 380$ V. (b) $V_1 = 430 - 460$ V. (c) $V_1 = 460 - 430$ V. (d) $V_1 = 380 - 350$ V.

3.5 Conclusion and Future work

In this chapter, the ZVS realization in a four-switch buck+boost converter was analyzed and presented comprehensively in three mode operation by variable frequency technique. TCM-ZVS buck-type or boost-type modulation strategy was adopted when the input voltage is in the higher or lower voltage range. In the buck-boost-type mode when the input-to-output voltage gain is close to unit, three-segment inductor current mode modulation is found to be the most suitable modulation method. A 300–600 V input, 400 V output, 3 kW laboratory prototype was built to prove and verify the proposed concepts. The converter was tested in a wide power range from 10% to full rated load. The measured efficiency was always higher than 99%, i.e., between 99.2% and 99.6%, from 1 kW to 3 kW for all the considered input voltages. Mode transition test was also carried out to show the feasibility of the proposed modulation strategy. The power density of this converter is 4.86 kW/L. The dynamic duty cycle control can be a future study to further improve the efficiency in the transition mode at light load.

3.6 Appendix A

Figure 3.28 shows a general polyline function with values of y_1 at x_1, y_2 at x_2, etc.

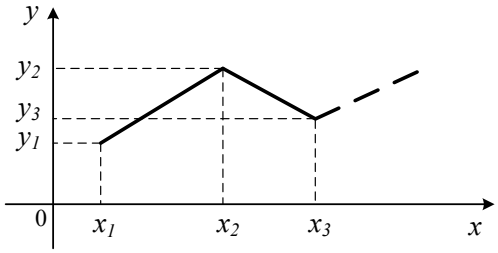


Figure 3.28: A general polyline function.

Based on the definition of rms value of a function, it is

$$F_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T f^2(x)dx} = \sqrt{\frac{1}{T}[\int_{x_1}^{x_2} f^2(x)dx + \int_{x_2}^{x_3} f^2(x)dx + \cdots]}. \tag{3.43}$$

In (3.43), T is the period of the function. The function expression from x_1 to x_2 can be written as $f(x) = kx + b$ with $k = \dfrac{y_2 - y_1}{x_2 - x_1}$ and $b = y_1 - kx_1$. Substitute this equation into (3.43), after simplification, (3.44) is derived as

$$\sqrt{\frac{1}{T}\int_{x_1}^{x_2} f^2(x)dx} = \sqrt{\frac{1}{T}\int_{x_1}^{x_2} (kx+b)^2 dx} = \sqrt{\frac{x_2 - x_1}{T} \cdot \frac{y_1^2 + y_2^2 + y_1 y_2}{3}}. \tag{3.44}$$

Therefore, the rms value of a general polyline function can be expressed as

$$F_{\text{rms}} = \sqrt{\frac{x_2 - x_1}{T} \cdot \frac{y_1^2 + y_2^2 + y_1 y_2}{3} + \frac{x_3 - x_2}{T} \cdot \frac{y_2^2 + y_3^2 + y_2 y_3}{3} + \cdots}. \tag{3.45}$$

3.7 Appendix B

The input and output voltage ripples for the FSBB converter under three-mode variable-frequency modulation is given in this section. The detailed formulas and its derivations for the voltage ripple calculation are shown in Table 4.3 in Chapter 4 for TCM-ZVS modulation, and (5.30) and (5.31) in Chapter 5 for three-segment inductor current mode ZVS modulation.

Figure 3.30 and Figure 3.31 show the input and output side peak-to-peak voltage ripple and its ripple factor with three-mode variable-frequency ZVS modulation when $V_2 = 400$ V, $P_o = 3$ kW, $I_0 = -2.5$ A, $L = 100\ \mu$H. The capacitor values are 40 μF, 70 μF, and 100 μF, respectively.

The ripple factor was defined as $\gamma = \dfrac{\Delta V_{\text{pp}}}{V_{\text{dc}}}$ with V_{dc} being its dc value and ΔV_{pp} being its peak-to-peak ripple, which is illustrated in Figure 3.29. For input side, V_{dc} is the input voltage of V_1, and for output side, V_{dc} is the output voltage of V_2. V_{pp} is the corresponding peak-to-peak voltage ripple of each side. For the built prototype, the input capacitance was 72 μF (12 × 6 μF) and the output capacitance was 84 μF (12 × 7 μF).

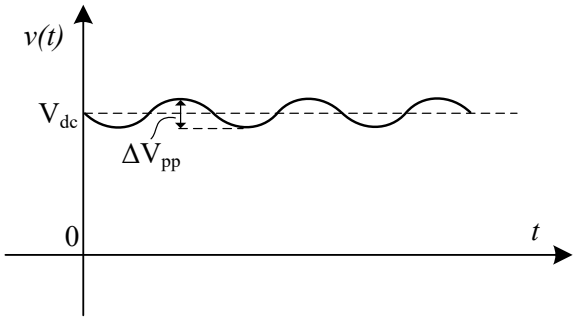
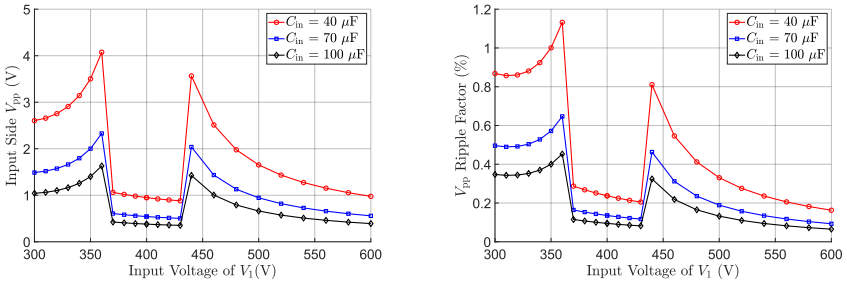
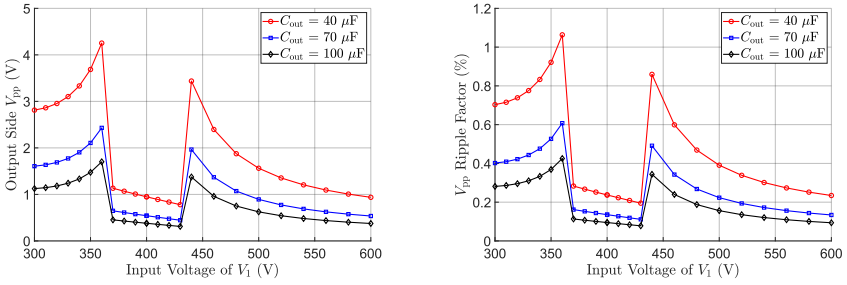


Figure 3.29: Illustration of peak-to-peak voltage ripple (ΔV_{pp}).



(a) (b)

Figure 3.30: Input side peak-to-peak voltage ripple and its ripple factor with three-mode variable-frequency ZVS modulation when $V_2 = 400$ V, $P_o = 3$ kW, $I_0 = -2.5$ A, $L = 100$ μH. In transition mode, $d_1 = 0.8$. (a) V_{pp} of input side. (b) Input side voltage ripple factor.



(a) (b)

Figure 3.31: Output side peak-to-peak voltage ripple and its ripple factor with three-mode variable-frequency ZVS modulation when $V_2 = 400$ V, $P_o = 3$ kW, $I_0 = -2.5$ A, $L = 100$ μH. In transition mode, $d_1 = 0.8$. (a) V_{pp} of output side. (b) Output side voltage ripple factor.

4

Effects of Parasitic Resistance on Reverse Switching Current

Triangular current mode (TCM) zero-voltage switching (ZVS) modulation method is widely adopted in power electronic converters to achieve acceptable efficiency in high switching frequency operations. For bidirectional dc-dc converters, in order to realize ZVS turn-on, a reverse switching current through the inductor, which takes a negative value during the switching interval, can be utilized for this purpose through variable frequency control.

This chapter revisits this reverse switching current considering the parasitic resistances presented in the MOSFET switches and the inductor for three common types of dc-dc converters, i.e., buck, boost and buck-boost converters, which study was normally neglected in the previous research. Universal closed-form equations of the modified duty cycle and switching current are derived, which can be utilized to calculate this switching current under different operating conditions. It is found that the parasitic resistances can have a negative impact on the switching current value, and this may lead to unexpected loss of ZVS turn-on. A laboratory prototype of a four-switch buck+boost converter featuring TCM-ZVS buck, boost and buck-boost operation capability was built to investigate and validate the proposed concepts. The operating voltage and power range are from 100 V to 400 V, and 300 W to 1 kW, respectively. [1]

[1]This chapter is based on:

G. Yu, S. Yadav, J. Dong and P. Bauer, "Revisiting the Reverse Switched Current of Buck, Boost, and Buck–Boost Converters in Voltage-Mode TCM–ZVS Control Considering Parasitic Resistances," in IEEE Transactions on Power Electronics, vol. 39, no. 7, pp. 8254-8268, July 2024, doi: 10.1109/TPEL.2024.3382051.

4.1 Introduction

Non-isolated dc-dc converters can operate as a power buffer interfacing different power stages, which makes it an indispensable role in many applications, including battery energy storage systems, photovoltaic applications, wireless power transfer, etc [38], [69], [70]. With the pursuit of achieving high power density, the switching frequency has been increasing over the last decades due to the continual advancement of power semiconductor device technology [71]. However, a high switching frequency is also accompanied with increased switching losses even with adoption of wide band-gap devices [50]. Therefore, soft switching techniques including zero-voltage switching (ZVS) and zero-current switching (ZCS) are still required in order to guarantee a satisfactory efficiency.

A state-of-the-art review on soft switching technologies for non-isolated dc-dc converters is well presented in [72]. Among the various soft switching implementations, triangular current mode (TCM) modulation is a widely adopted and relatively simpler technique to realize soft switching for conventional power converters without the need to use auxiliary circuits, which also maintains the fundamental characteristics of the conventional topology [46]. In order to realize TCM-ZVS modulation, the diode presented in the unidirectional buck, boost and buck-boost converters for the inductor current freewheeling is required to be replaced by a synchronous MOSFET, thus making it bidirectional. Figure 4.1 shows the circuit topologies of the bidirectional buck, boost and buck-boost converters with parasitic resistances presented in MOSFET and inductor [73]. In TCM-ZVS modulation, the reverse switching current through the inductor, which takes a negative value during the switching interval is the key to realize ZVS turn-on of switch S_1 (cf., Figure 4.1). TCM-ZVS modulation is normally accompanied by variable-frequency control to maintain this current of I_0 (cf., Figure 4.2), and the closed-form equations can be simply solved under ideal cases. However, due to the non-ideal factors including parasitic resistances, this reverse switching current might change. To guarantee the ZVS operation, an inductor current zero crossing detection circuit can be implemented [74], which, however, increases the system complexity and may introduce more losses due to additional sampling circuits. In addition, the detection of switching current operating at high frequencies of hundreds of kHz is also a challenge [75]. Therefore, the realization of TCM-ZVS operation without inductor or switch current detection is preferred. Apart from the current detection method, a conservative and simple solution is to select this switching current value large enough (absolute value) to ensure ZVS margin. However, a larger reverse switching current results in a larger peak inductor current and its root mean square (rms) value, and thus the circuit conduction losses increase [47]. Most of the previous research did not consider the parasitic resistance when evaluating TCM-ZVS modulation. In [41] and [76], the parasitic resistance is considered for the high step-up and non-inverting buck-boost converters operating under continuous conduction mode (CCM). In this mode, the inductor current is assumed to be a dc constant during the analysis, which is not the case for TCM-ZVS modulation since the inductor current has a much larger peak-to-peak ripple.

The main purpose and contribution of this work is to re-evaluate the reverse switching current of the TCM-ZVS modulation for the three most common types of non-isolated dc-dc converters taking into account the parasitic resistances. Detailed and universal closed-form equations are derived for the new modified duty cycle and switching current under variable-frequency voltage-mode TCM-ZVS modulation, which, to the best of authors'

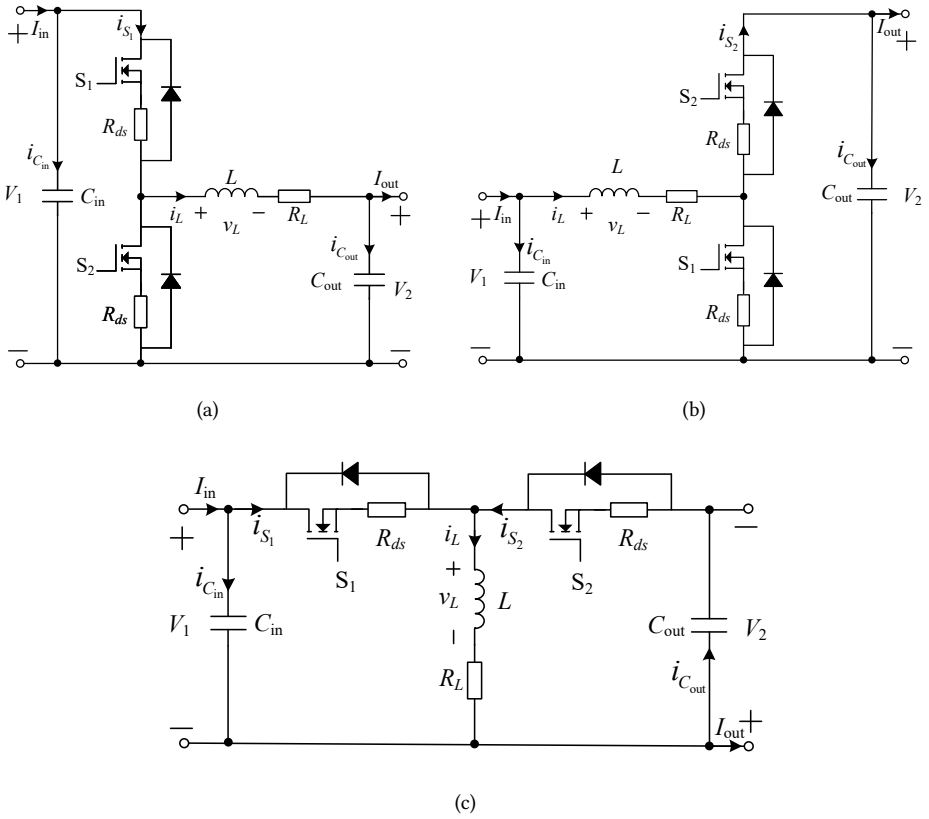


Figure 4.1: Circuit topologies of bidirectional non-isolated dc-dc converters with parasitic resistances. (a) Buck converter. (b) Boost converter. (c) Buck-Boost converter.

knowledge, has not been analyzed elsewhere in the literature. It is found by theoretical calculation, simulation and experimentation that the parasitic resistance has a different impact on the reverse switching current for buck and boost mode operations even with same voltage and power values adopted by this work, and this phenomenon cannot be revealed by the previous formulas derived from ideal cases. Compared to the previous research, the newly derived formulas taking into account the parasitic resistance reveal the reverse switching current change at different operating points, and it can also serve as a better theoretical guidance for this switching current selection.

The rest of this chapter is organized as follows. In Section 4.2, the variable-frequency TCM-ZVS modulation and its universal voltage-mode control method are described. In Section 4.3, newly closed-form equations for modified duty cycle and switching current are derived for three common types of dc-dc converters, i.e., buck, boost and buck-boost converters. In Section 4.4, design considerations including input and output capacitor selection and simulation verification are given. In Section 4.5, the reverse switching current is evaluated through a silicon carbide (SiC) MOSFET-based four-switch buck+boost (FSBB)

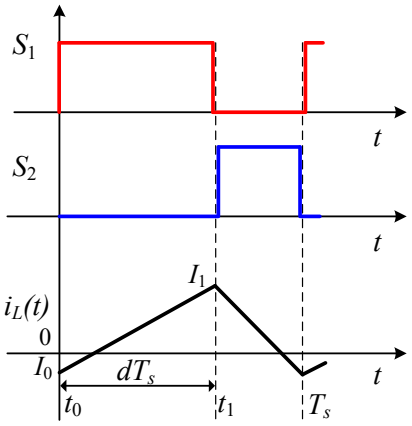


Figure 4.2: Inductor current waveform and gating signals under TCM-ZVS modulation for the three types of dc-dc converters in Figure 4.1.

converter featuring TCM-ZVS buck, boost and buck-boost mode operation capability. Finally, Section 4.6 concludes this chapter.

4.2 Description of Variable-Frequency TCM-ZVS Modulation

In this section, a brief mathematical description of variable-frequency TCM-ZVS modulation for buck, boost and buck-boost converters will be given under ideal circumstances followed by an introduction of its corresponding voltage-mode control method.

4.2.1 Brief Review of Variable-Frequency TCM-ZVS Modulation

The switching waveforms of TCM-ZVS modulation is given in Figure 4.2. Taking buck converter as an example, without considering dead time and parasitic resistances, the inductor current waveform can be expressed as follows with $t_0 = 0$,

$$i_L(t) = \begin{cases} I_0 + \dfrac{V_1 - V_2}{L} t, & 0 < t \le t_1 \\ I_1 - \dfrac{V_2}{L}(t - t_1), & t_1 < t \le T_s, \end{cases} \tag{4.1}$$

where V_1 and V_2 are the input and output voltages, L is the inductance, T_s is the switching period, d is the duty cycle of S_1, namely, $t_1 - t_0 = dT_s$, I_0 and I_1 are the valley and peak current shown in Figure 4.2.

From (4.1), the voltage gain can be derived as

$$G_v = \frac{V_2}{V_1} = d. \tag{4.2}$$

Table 4.1: Summary of duty cycle and frequency in ideal case

Converter Type	Duty Cycle	Frequency
Buck Converter	$d = \frac{V_2}{V_1}$	$f_s = \frac{V_1 d(1-d)}{2L(I_{\text{out}} - I_0)}$
Boost Converter	$d = 1 - \frac{V_1}{V_2}$	$f_s = \frac{V_1 d(1-d)}{2L[I_{\text{out}} - I_0(1-d)]}$
Buck-Boost Converter	$d = \frac{V_2}{V_1 + V_2}$	$f_s = \frac{V_1 d(1-d)}{2L[I_{\text{out}} - I_0(1-d)]}$

Since $I_{\text{out}} = \frac{I_0 + I_1}{2}$, combining (4.1) and (4.2), the switching frequency can be derived as

$$f_s = \frac{V_1 d(1-d)}{2L(I_{\text{out}} - I_0)}. \tag{4.3}$$

The formulas of duty cycle and frequency for boost and buck-boost converters can be derived similarly. Table 4.1 summarizes the results for these three dc-dc converters [77], [78]. In Table 4.1, d is all defined as the duty cycle of S_1. For single-switch buck-boost converter, the output voltage is inverted, so the reference direction of output voltage polarity is reversed compared with buck or boost converters [cf., Figure 4.1(c)].

4.2.2 Brief Introduction of Voltage-Mode TCM-ZVS Control

A universal voltage-mode variable-frequency TCM-ZVS modulation for buck, boost and buck-boost converters without inductor current detection is also proposed herein based on the formulas in Table 4.1. An example of this control method for buck converter is shown in Figure 4.3, which can be easily modified for boost and buck-boost converters as well. Herein, the switching frequency is determined by the formulas in Table 4.1 while the duty cycle of d is regulated to meet the output voltage requirement.

As it can be seen from Figure 4.3, the output voltage of the converter can be regulated well due to the direct feedback control with the reference voltage. However, the inductor current is not controlled directly, and therefore the non-ideal factors including parasitic resistances will affect the switching current value of I_0, which is required to be a negative value in order to discharge the parasitic capacitance of C_{oss} from S_1 (or to charge C_{oss} from S_2) during the dead time to ensure the ZVS turn-on of S_1. Therefore, to study the influence from the non-ideal factors on I_0 under a voltage-mode TCM-ZVS modulation control is meaningful and necessary. In this work, the parasitic resistances presented in MOSFETs and inductor will be considered and studied.

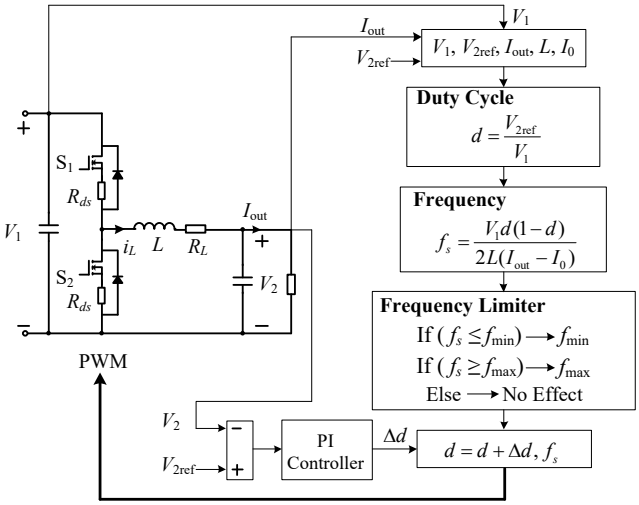


Figure 4.3: Universal voltage-mode variable-frequency TCM-ZVS modulation control diagram, buck converter is taken as an example.

4.3 TCM-ZVS Modulation Considering Parasitic Resistances

In this section, detailed and universal closed-form equations for the modified duty cycle and reverse switching current in voltage-mode TCM-ZVS modulation considering parasitic resistances will be derived.

4.3.1 Derivation Procedures of General Expressions

The parasitic resistances from the MOSFETs and inductor are defined as R_{ds} and R_L respectively as shown in Figure 4.1. Some assumptions are made for the following analysis:

1) the inductance is a constant;

2) the gating signals for S_1 and S_2 are complementary and their dead time is neglected;

3) the inductor current connecting I_0 and I_1 is a straight line;

4) during reverse conduction, the current only passes through the MOSFET channel, not through the body diode.

These assumptions are further discussed in Section 4.4.

During the On Period of S_1

Defining d as the duty cycle of S_1 for all the three converter topologies in Figure 4.1. When S_1 is on, the voltage across the inductor can be expressed as follows, for buck converter, it is

$$v_L(t) = V_1 - V_2 - (R_{ds} + R_L) i_L(t). \tag{4.4}$$

For both boost and buck-boost converters, it is

$$v_L(t) = V_1 - (R_{ds} + R_L) i_L(t). \tag{4.5}$$

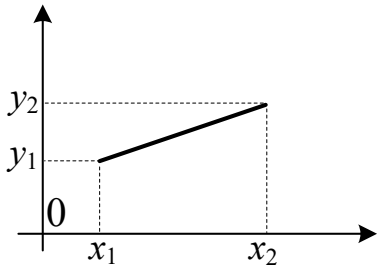


Figure 4.4: A linear function.

In (4.4) and (4.5), $i_L(t)$ is the inductor current, and its reference direction is given in Figure 4.1.

Based on (4.4) and (4.5), the net change of the inductor current during on period of S_1 can be derived. For buck converter, it is

$$I_1 - I_0 = \int_{t_0}^{t_1} \frac{(V_1 - V_2) - (R_{ds} + R_L) i_L(t)}{L} dt. \tag{4.6}$$

Similarly, for both boost and buck-boost converters, it is

$$I_1 - I_0 = \int_{t_0}^{t_1} \frac{V_1 - (R_{ds} + R_L) i_L(t)}{L} dt. \tag{4.7}$$

Since the integral of a linear function (cf., Figure 4.4) can be simply solved by (4.8), so, (4.6) and (4.7) can be simplified to (4.9) and (4.10), respectively.

$$\int_{x_1}^{x_2} f(x)dx = \int_{x_1}^{x_2} [\frac{y_2 - y_1}{x_2 - x_1}(x - x_1) + y_1]dx = \frac{(y_1 + y_2)(x_2 - x_1)}{2}. \tag{4.8}$$

$$I_1[1 + \frac{(R_{ds} + R_L)T_s}{2L} d] = I_0[1 - \frac{(R_{ds} + R_L)T_s}{2L} d] + \frac{(V_1 - V_2)T_s}{L} d. \tag{4.9}$$

$$I_1[1 + \frac{(R_{ds} + R_L)T_s}{2L} d] = I_0[1 - \frac{(R_{ds} + R_L)T_s}{2L} d] + \frac{V_1 T_s}{L} d. \tag{4.10}$$

Equations (4.9) and (4.10) can be re-expressed by the same form as follows:

$$I_1(1 + kd) = I_0(1 - kd) + md, \tag{4.11}$$

where $k = \frac{(R_{ds} + R_L)T_s}{2L}$. In (4.11), for buck converter, $m = \frac{(V_1 - V_2)T_s}{L}$ while for boost and buck-boost converters, $m = \frac{V_1 T_s}{L}$.

During the On Period of S_2

Similar to the previous analysis, during the on period of S_2, the net change of the inductor current can be expressed as follows, for both buck and buck-boost converters, it is

$$I_0 - I_1 = \int_{t_1}^{T_s} -\frac{V_2 + (R_{ds} + R_L) i_L(t)}{L} dt. \tag{4.12}$$

For boost converter, it is

$$I_0 - I_1 = \int_{t_1}^{T_s} -\frac{V_2 - V_1 + (R_{ds} + R_L) i_L(t)}{L} dt. \tag{4.13}$$

Based on (4.8), (4.12) and (4.13) can be simplified to (4.14) and (4.15), respectively.

$$I_1[1 - \frac{(R_{ds} + R_L)T_s}{2L}(1-d)] = I_0[1 + \frac{(R_{ds} + R_L)T_s}{2L}(1-d)] + \frac{V_2 T_s}{L}(1-d). \tag{4.14}$$

$$I_1[1 - \frac{(R_{ds} + R_L)T_s}{2L}(1-d)] = I_0[1 + \frac{(R_{ds} + R_L)T_s}{2L}(1-d)] + \frac{(V_2 - V_1)T_s}{L}(1-d). \tag{4.15}$$

With the same definition of k given in (4.11), (4.14) and (4.15) can be re-expressed with the same form as follows:

$$I_1[1 - k(1-d)] = I_0[1 + k(1-d)] + q(1-d). \tag{4.16}$$

In (4.16), for both buck and buck-boost converters, $q = \frac{V_2 T_s}{L}$ while for boost converter, $q = \frac{(V_2 - V_1)T_s}{L}$.

Analytical Solutions

If k is 0, i.e., $R_{ds} + R_L = 0$, (4.11) and (4.16) degenerate to the formulas in ideal cases, otherwise, combining (4.11) and (4.16) yields

$$\begin{cases} I_0 = \dfrac{md[1 - k(1-d)]}{2k} - \dfrac{q(1+kd)(1-d)}{2k}, \\ I_1 = \dfrac{(1-kd)I_0}{1+kd} + \dfrac{md}{1+kd}. \end{cases} \tag{4.17}$$

Based on (4.17), one can simply get

$$\frac{I_0 + I_1}{2} = \frac{(m+q)d - q}{2k}. \tag{4.18}$$

For buck converter, the output current is

$$I_{\text{out}} = \frac{I_0 + I_1}{2}. \tag{4.19}$$

Table 4.2: Summary of new modified duty cycle expressions

Converter Type	New Modified Duty Cycle	Expression of k	Expression of m	Expression of q
Buck Converter	$d=\frac{q}{m+q}+\frac{2I_{\text{out}}}{m+q}k$	$k=\frac{(R_{ds}+R_L)T_s}{2L}$	$m=\frac{(V_1-V_2)T_s}{L}$	$q=\frac{V_2T_s}{L}$
Boost Converter	$d=\frac{q}{m+q}+\frac{m-\sqrt{m^2-8k(m+q)I_{\text{out}}}}{2(m+q)}$	$k=\frac{(R_{ds}+R_L)T_s}{2L}$	$m=\frac{V_1T_s}{L}$	$q=\frac{(V_2-V_1)T_s}{L}$
Buck-Boost Converter	$d=\frac{q}{m+q}+\frac{m-\sqrt{m^2-8k(m+q)I_{\text{out}}}}{2(m+q)}$	$k=\frac{(R_{ds}+R_L)T_s}{2L}$	$m=\frac{V_1T_s}{L}$	$q=\frac{V_2T_s}{L}$

For both boost and buck-boost converters, the output current is

$$I_{\text{out}}=\frac{I_0+I_1}{2}(1-d). \tag{4.20}$$

As it can be seen from (4.19) and (4.20), in order to transfer power from input side to output side, the sum of I_0 and I_1 should be larger than zero, i.e., $I_0+I_1>0$. If $I_0<0$ and is selected as a value that can guarantee ZVS turn-on of S_1, then the ZVS turn-on of S_2 is also guaranteed automatically since the absolute value of I_1 is always larger than I_0, meanwhile the required net voltage change values across the switches in one arm are the same.

Combining (4.18) and (4.19) yields the modified duty cycle expression for buck converter, which is

$$d_{\text{new}}=\frac{q}{m+q}+\frac{2I_{\text{out}}}{m+q}k. \tag{4.21}$$

Combing (4.18) and (4.20) yields the modified duty cycle expression for both boost and buck-boost converters, which is

$$d_{\text{new}}=\frac{q}{m+q}+\frac{m-\sqrt{m^2-8k(m+q)I_{\text{out}}}}{2(m+q)}. \tag{4.22}$$

With adoption of first-order Taylor expansion, (4.22) can further be simplified to

$$d_{\text{new}}=\frac{q}{m+q}+\frac{2I_{\text{out}}}{m}k. \tag{4.23}$$

When the parasitic resistances reduce to zero in ideal case, (4.21) and (4.22) [or (4.23)] can further be simplified to

$$d_{\text{ideal}}=\frac{q}{m+q}. \tag{4.24}$$

Equation (4.24) can be verified by the definition of m and q given in (4.11) and (4.16).

To summarize, the analytical solutions of the new modified duty cycle for the three dc-dc converters are presented in Table 4.2. Once the duty cycle is known, then the reverse switching current value of I_0 can also be calculated based on (4.17). Figure 4.5 briefly illustrates the calculation procedures of I_0 with the proposed analysis. The estimation of the parasitic resistances will be discussed in detail in Section 4.4.

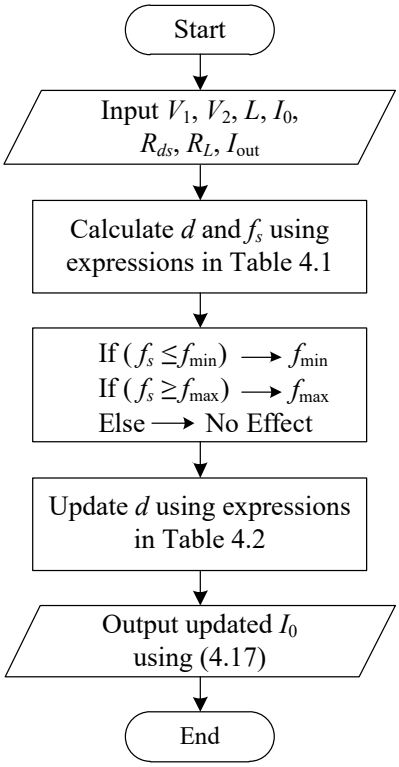


Figure 4.5: Flowchart of I_0 calculation considering parasitic resistances.

4.3.2 Application in an FSBB Converter

TCM-ZVS modulation can also be applied to an FSBB converter featuring multi-mode operation capability [77], [51], [52], and its circuit topology is shown in Figure 4.6.

In order to apply the formulas derived in Table 4.2 to FSBB converter, simply, only the definition of k needs to be replaced by $k = \frac{(2R_{ds} + R_L)T_s}{2L}$. Taking TCM-ZVS buck mode operation as an example, in buck operation mode, S_3 is always on, so, an additional R_{ds} is required to be counted. For boost operation mode, the R_{ds} of S_1 is required. It should be noted that under TCM-ZVS buck-boost mode operation, the output of the FSBB converter is not inverted compared with the single-switch buck-boost converter, but the operating principle is the same.

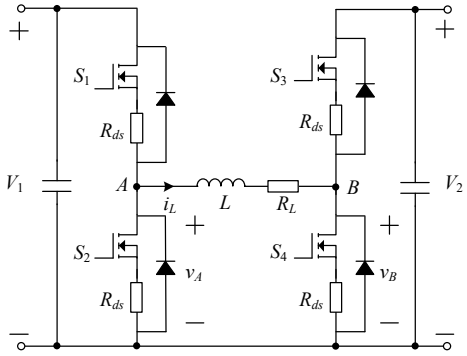


Figure 4.6: Circuit topology of the FSBB converter.

4.4 Design Consideration and Simulation Verification

4.4.1 Switching Frequency and Inductance Parameters Selection

In practice, a frequency limiter is normally adopted to prevent the switching frequency from being too high or too low (cf., Figure 4.3). In this work, the switching frequency is selected between 20 kHz and 150 kHz. The minimum frequency is selected based on the frequency hearing range of human ear (less than 20 kHz) while the maximum frequency is constrained by both the gate driver's driving capability and operating conditions.

For the inductance, a value of 100 μH was chosen to ensure that the switching frequency falls within the desired operational range. The calculated switching frequency is shown in Figure 4.7 with the given operating specifications in this work.

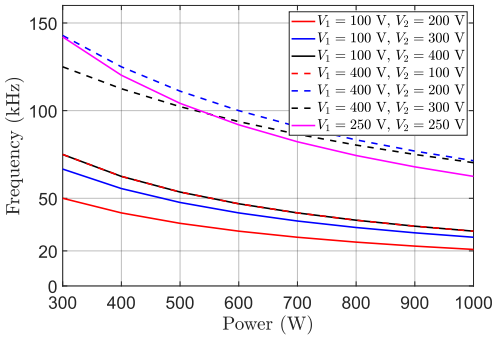


Figure 4.7: Switching frequency under different operating conditions, $L = 100$ μH, $I_0 = -2$ A.

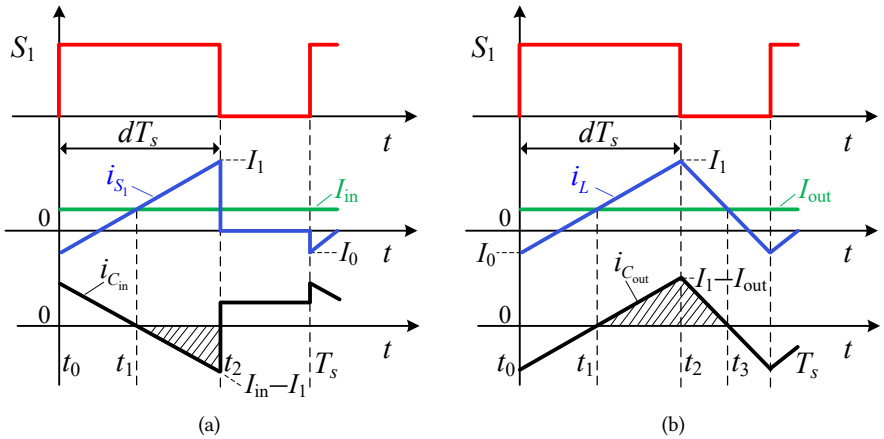


Figure 4.8: Current waveforms of $i_{C_{\text{in}}}$ and $i_{C_{\text{out}}}$ of a buck converter under TCM-ZVS modulation. (a) $i_{C_{\text{in}}}$. (b) $i_{C_{\text{out}}}$.

4.4.2 Selection of Input and Output Capacitors

During the analysis in Section 4.3, the input and output voltages are taken as a dc value. However, voltage ripple is always present and its value depends on the capacitance, so, the capacitance selection is important. In addition, the selection guideline of the input and output capacitors for a dc-dc converter under TCM-ZVS operation is often neglected. Herein, the capacitor voltage ripple is calculated as a selection basis for the capacitors in buck, boost and buck-boost converters, respectively. The reference direction of the current is shown in Figure 4.1. Different from traditional continuous conduction mode (CCM) operation when I_0 is larger than zero, in TCM-ZVS operation, since I_0 is negative while I_{in} and I_{out} (cf., Figure 4.1) are positive, the ripple analysis of capacitor voltage is actually simpler in TCM-ZVS operations.

Case of Buck Converter

The waveforms of current flowing into the input and output capacitors are shown in Figure 4.8.

The peak-to-peak value of the capacitor voltage ripple can be calculated based on the net change of charge in the shaded area. For the case of Figure 4.8(a), the input capacitor peak-to-peak voltage ripple is

$$\Delta V_{\text{pp\_C}_{\text{in}}\text{\_Buck}} = \frac{(I_1 - I_{\text{in}})(t_2 - t_1)}{2C_{\text{in}}}, \tag{4.25}$$

where $t_2 - t_1 = \dfrac{I_1 - I_{\text{in}}}{I_1 - I_0} dT_s$, I_{in} is the average input current.

For the case of Figure 4.8(b), the output capacitor peak-to-peak voltage ripple is

$$\Delta V_{\text{pp\_C}_{\text{out}}\text{\_Buck}} = \frac{(I_1 - I_{\text{out}})(t_3 - t_1)}{2C_{\text{out}}}, \tag{4.26}$$

where $t_3 - t_1 = \dfrac{I_1 - I_{\text{out}}}{I_1 - I_0} T_s$, I_{out} is the average output current.

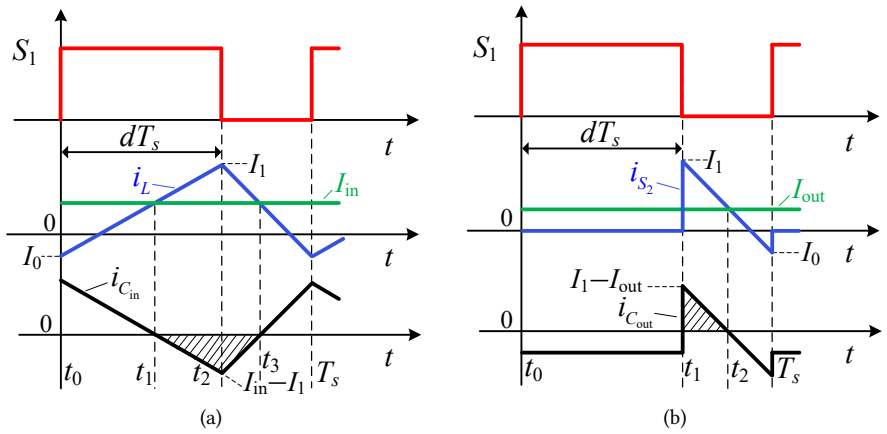


Figure 4.9: Current waveforms of $i_{C_{in}}$ and $i_{C_{out}}$ of a boost converter under TCM-ZVS modulation. (a) $i_{C_{in}}$. (b) $i_{C_{out}}$.

Case of Boost Converter

The waveforms of current flowing into the input and output capacitors are shown in Figure 4.9.

For the case of Figure 4.9(a), the input capacitor peak-to-peak voltage ripple is

$$\Delta V_{pp\_C_{in}\_Boost} = \frac{(I_1 - I_{in})(t_3 - t_1)}{2C_{in}}, \tag{4.27}$$

where $t_3 - t_1 = \dfrac{I_1 - I_{in}}{I_1 - I_0} T_s$.

For the case of Figure 4.9(b), the output capacitor peak-to-peak voltage ripple is

$$\Delta V_{pp\_C_{out}\_Boost} = \frac{(I_1 - I_{out})(t_2 - t_1)}{2C_{out}}, \tag{4.28}$$

where $t_2 - t_1 = \dfrac{I_1 - I_{out}}{I_1 - I_0}(1-d)T_s$.

Case of Buck-Boost Converter

For a buck-boost converter given in Figure 4.1(c), the current waveform flowing into the input capacitor can be illustrated by Figure 4.8(a) while the current waveform flowing into the output capacitor can be illustrated by Figure 4.9(b). Therefore, the peak-to-peak voltage ripple of the input and output capacitors can be expressed by (4.25) and (4.28), respectively.

Equations (4.25) to (4.28) can further be simplified, which are summarized in Table 4.3. It can be concluded from Table 4.3 that for variable-frequency modulation, the input and output side voltage ripple are independent of the frequency if it is not limited.

Figures 4.10 and 4.11 show the peak-to-peak voltage ripple and its ripple factor for both TCM-ZVS buck and boost operations with different capacitances, the inductance is 100 μH. The voltage ripple factor is defined as $\gamma = \dfrac{\Delta_{pp}}{V_{dc}}$ with V_{dc} being its dc value. In this work, both the input and output capacitances were chosen to be 150 μF.

Table 4.3: Summary of peak-to-peak voltage ripple of input and output capacitors

Converter Type	V_{pp} of C_{in}	V_{pp} of C_{out}
Buck Converter	$\frac{L}{2C_{in}} \cdot \frac{(I_1-I_{in})^2}{V_1-V_2}$	$\frac{L}{2C_{out}} \cdot \frac{V_1(I_1-I_{out})^2}{V_2(V_1-V_2)}$
Boost Converter	$\frac{L}{2C_{in}} \cdot \frac{V_2(I_1-I_{in})^2}{V_1(V_2-V_1)}$	$\frac{L}{2C_{out}} \cdot \frac{(I_1-I_{out})^2}{V_2-V_1}$
Buck-Boost Converter	$\frac{L}{2C_{in}} \cdot \frac{(I_1-I_{in})^2}{V_1}$	$\frac{L}{2C_{out}} \cdot \frac{(I_1-I_{out})^2}{V_2}$

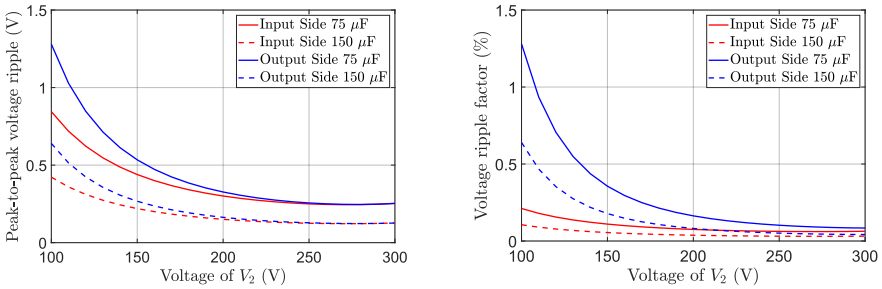


Figure 4.10: Peak-to-peak voltage ripple and its ripple factor under buck operation with 75 μF and 150 μF capacitance, $P_o = 1$ kW, $I_0 = -2$ A, $V_1 = 400$ V. (a) Peak-to-peak voltage ripple. (b) Peak-to-peak voltage ripple factor.

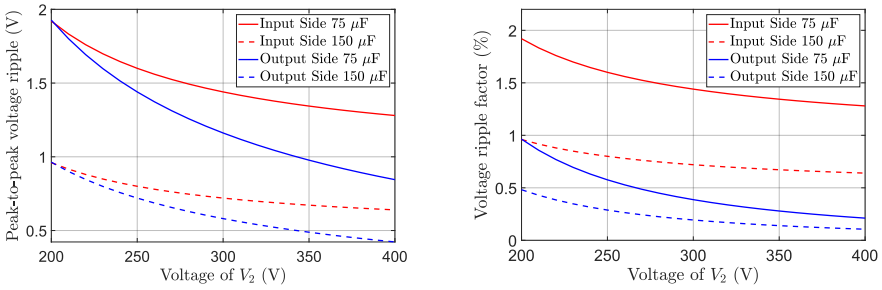


Figure 4.11: Peak-to-peak voltage ripple and its ripple factor under boost operation with 75 μF and 150 μF capacitance, $P_o = 1$ kW, $I_0 = -2$ A, $V_1 = 100$ V. (a) Peak-to-peak voltage ripple. (b) Peak-to-peak voltage ripple factor.

4.4.3 Parasitic Resistances Estimation and Simulation Verification of the Proposed Analysis

With the control logic in Figure 4.3 and the derived formulas in Table 4.2 and (4.17), the reverse switching current value of I_0 can be calculated. In order to verify the correctness of

Table 4.4: Key parameters of the FSBB prototype

MOSFET Switch	C3M0075120J (2 in Parallel)
Input Capacitor C_{in}	Vishay, 25 μF ×6
Output Capacitor C_{out}	Vishay, 25 μF ×6
Inductor	PM 74/59, N87, 100 μH
Switching Frequency	$20-150$ kHz

the formulas, a set of simulation was carried out with the specifications in Table 4.4 based on the laboratory prototype.

Estimation of Parasitic Resistances

Before simulation verification, the parasitic resistance needs to be estimated. The value of R_{ds} can be acquired from its datasheet while for the value of R_L, its equivalent value can be estimated by the energy-conservation approach (4.29) [79], [80], [81]

$$R_L = \frac{P_{\text{Loss\_L}}}{I^2_{\text{rms\_L}}}, \tag{4.29}$$

where $P_{\text{Loss\_L}}$ is the inductor loss, which consists of winding loss and core loss, $I_{\text{rms\_L}}$ is the rms value of the inductor current, which is

$$I_{\text{rms\_L}} = \sqrt{\frac{1}{3}(I_0^2 + I_1^2 + I_0 I_1)}. \tag{4.30}$$

To build the inductor, 600×0.071 mm Litz wire was adopted. The skin depth of $\delta_{C_{\text{u}}}$ at a certain switching frequency can be calculated through $\delta_{C_{\text{u}}} = \sqrt{\frac{2}{\omega \mu_{C_{\text{u}}} \sigma_{C_{\text{u}}}}}$ with $\omega, \mu_{C_{\text{u}}}, \sigma_{C_{\text{u}}}$ being its angular frequency, permeability and electrical conductivity, respectively [82]. Therefore, at 25°C with frequencies of 20 kHz and 150 kHz, the skin depth is calculated as 0.47 mm and 0.17 mm, respectively, which is much larger than the wire diameter. To facilitate the winding loss calculation, its dc resistance is adopted. The number of winding turns is 18, and its measured R_{dc} is 18 mΩ.

As for the core loss, due to the nonsinusoidal inductor current waveform, the improved generalized Steinmetz equation (iGSE) [83] is adopted, which is expressed as

$$P_{\text{core\_iGSE}} = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} V_e \, dt, \tag{4.31}$$

$$k_i = \frac{k}{2^{\beta+1} \pi^{\alpha-1} (0.2761 + \frac{1.7061}{\alpha + 1.354})}, \tag{4.32}$$

where k, α and β are the Steinmetz coefficients, ΔB is the peak-to-peak flux density, V_e is the core volume and k_i can be calculated from (4.32) [83].

With TCM-ZVS modulation, (4.31) can be simplified to the same expression for buck, boost and buck-boost converters, which is

$$P_{\text{core\_iGSE}} = k_i f_s^{\alpha} (\Delta B)^{\beta} [d^{1-\alpha} + (1-d)^{1-\alpha}] V_e. \tag{4.33}$$

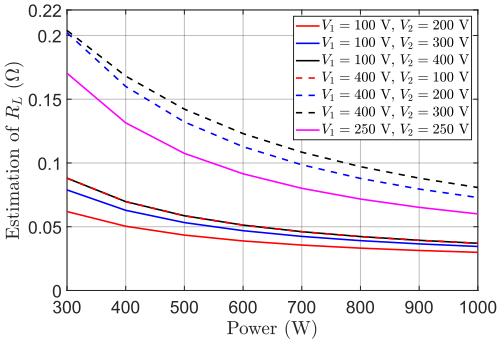


Figure 4.12: Estimation of R_L under different operating points.

4

Therefore, combining (4.29), (4.30) and (4.33) yields the estimation of R_L, which is

$$R_L = R_{\text{dc}} + \frac{k_i f_s^{\alpha} (\Delta B)^{\beta} [d^{1-\alpha} + (1-d)^{1-\alpha}] V_e}{\frac{1}{3}(I_0^2 + I_1^2 + I_0 I_1)}. \tag{4.34}$$

For the inductor design, PM 74/59 core with N87 material was adopted, the Steinmetz parameters are derived by curve fitting as $k = 47.69$, $\alpha = 1.11$, $\beta = 2.07$ at 25°C with SI unit [84]. However, this estimation has a drawback since the core losses of ferrite material depend on dc bias [85] and also cross-sectional area [86], which is not modeled. Nevertheless, this estimation can still be used as a reference.

Figure 4.12 shows the estimation of R_L under different operating conditions. Considering the MOSFETs of C3M0075120J (two in parallel) adopted in this work, a total parasitic resistance around several hundred milliohms could be utilized for simulation verification.

Based on the previous analysis, it can be seen that the estimation of the parasitic resistances could be affected by the operational temperature of the components. For example, the curve fitting coefficients for the inductor core losses, which were derived at a temperature of 25°C. A more accurate and natural solution is to model the losses while taking thermal effects into account, which can be a further research work.

Simulation Verification of Output Voltage

Simulation results from PLECS circuit simulator are provided for buck, boost and buck-boost mode operations respectively. Variable-step non-stiff solver with maximum step size of 1e-8 s or 5e-8 s (i.e., 10 ns or 50 ns) and 1e-6 relative tolerance is used. In order to be consistent with the assumptions of theoretical analysis, the gating signals are fully complementary, which means no dead time is applied.

First, the modified duty cycle expressions were verified based on the output voltage with a total 0.6 Ω parasitic resistance as an example. The output capacitor is selected as 150 μF. An ideal current source is adopted as the load. Figure 4.13 shows the circuit simulation model taking the buck converter as an example. The load current value is set as $I_{\text{Load}} = \dfrac{P_o}{V_2}$.

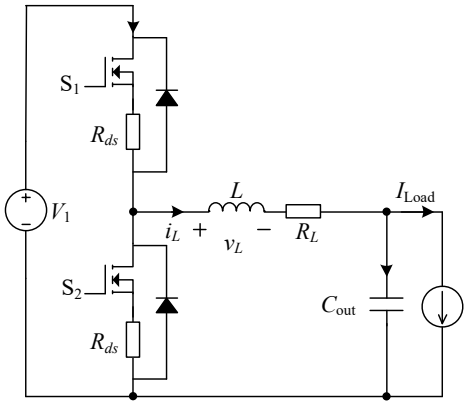


Figure 4.13: Simulation circuit adopted in PLECS circuit simulator, taking buck converter as an example.

Table 4.5: TCM-ZVS buck mode operation, $V_1 = 400$ V, $V_2 = 100$ V, $L = 100$ μH, $I_0 = -2$ A, $d_{\text{ideal}} = 0.25$, $R_{\text{parasitic}} = 0.6$ Ω.

Output Power (W)	300	500	700	1000
Frequency (kHz)	75.00	53.57	41.67	31.25
Output voltage under ideal duty cycle (V)	98.2	97.0	95.8	94.0
Modified duty cycle	0.2545	0.2575	0.2605	0.2650
Output voltage under modified duty cycle (V)	100.0	100.0	100.0	100.0

Table 4.6: TCM-ZVS boost mode operation, $V_1 = 100$ V, $V_2 = 200$ V, $L = 100$ μH, $I_0 = -2$ A, $d_{\text{ideal}} = 0.5$, $R_{\text{parasitic}} = 0.6$ Ω.

Output Power (W)	300	500	700	1000
Frequency (kHz)	50.00	35.71	27.78	20.83
Output voltage under ideal duty cycle (V)	196.3	193.8	191.3	187.5
Modified duty cycle	0.5092	0.5155	0.5220	0.5321
Output voltage under modified duty cycle (V)	199.9	199.8	199.7	199.5

The results are summarized in Tables 4.5 to 4.7, as it can be seen, after applying the modified duty cycle values, the output voltage can reach the expected value, which proves the correctness of the proposed duty cycle formulas.

Simulation Verification of Reverse Switching Current

Second, the simulated and calculated switching current value of I_0 under 0.2 Ω, 0.4 Ω and 0.6 Ω cases are given, which are shown from Figures 4.14 to 4.16. The relative error is

Table 4.7: TCM-ZVS buck-boost mode operation, $V_1 = 250$ V, $V_2 = 250$ V, $L = 100$ μH, $I_0 = -2$ A, $d_{\text{ideal}} = 0.5$, $R_{\text{parasitic}} = 0.6$ Ω.

Output Power (W)	300	500	700	1000
Frequency (kHz)	142.05	104.17	82.24	62.50
Output voltage under ideal duty cycle (V)	247.1	245.2	243.2	240.3
Modified duty cycle	0.5029	0.5049	0.5068	0.5098
Output voltage under modified duty cycle (V)	250.0	250.0	249.9	249.9

defined as $\varepsilon = \frac{\text{Calculated Value}-\text{Simulated Value}}{|\text{Simulated Value}|}$.

It can be seen from Figures 4.14 to 4.16 that under a wide operational power range with different parasitic resistances, the simulated and calculated current values of I_0 could match well for buck and buck-boost mode operations while for boost mode operation, the difference is slightly larger. Both calculated and simulated values follow the same trend as the power changes. The cause of the difference between the calculated and simulated values is discussed in Section 4.4.5.

4.4.4 Estimation of I_0 under Different Operating Cases

It can be concluded that in order to predict the reverse switching current well, accurate determination of the parasitic resistance is required, which is normally difficult in practice. Considering adoption of C3M0075120J MOSFET and external resistor board as a comparison during the experimentation (cf., Figure 4.26), herein, additional 0.1 Ω and 0.2 Ω were added to the value given in Figure 4.12 to represent the total parasitic resistance. Figure 4.17 shows the estimation of I_0 under different operational cases, and its value is supposed to be -2 A in ideal condition.

From the results in Figure 4.17, it can be inferred that the ZVS turn-on is more likely to be lost when the converter is operating in boost mode with the operating specifications adopted in this work, which will be validated by the experimental results.

4.4.5 Discussion on Assumptions

First, during the analysis, the inductance is assumed to be a constant, which can be evidenced by the maximum possible flux density during converter operation. Its value can be calculated by

$$\hat{B} = \frac{L\hat{I}}{NA_e}. \tag{4.35}$$

Substituting corresponding values, i.e., $L = 100$ μH, $N = 18$ and $A_e = 790$ mm^2, the maximum dc bias flux density is calculated to be 70.3 mT, and the maximum flux density is 154.7 mT, and these values are much lower than the N87 material saturation flux density of 490 mT at 25°C or 390 mT at 100°C [84]. Therefore, it is reasonable to assume the inductance to be a constant under dc current bias. As for the influence from variable frequency on the inductance, the inductor was measured within a wide frequency range between 10 kHz

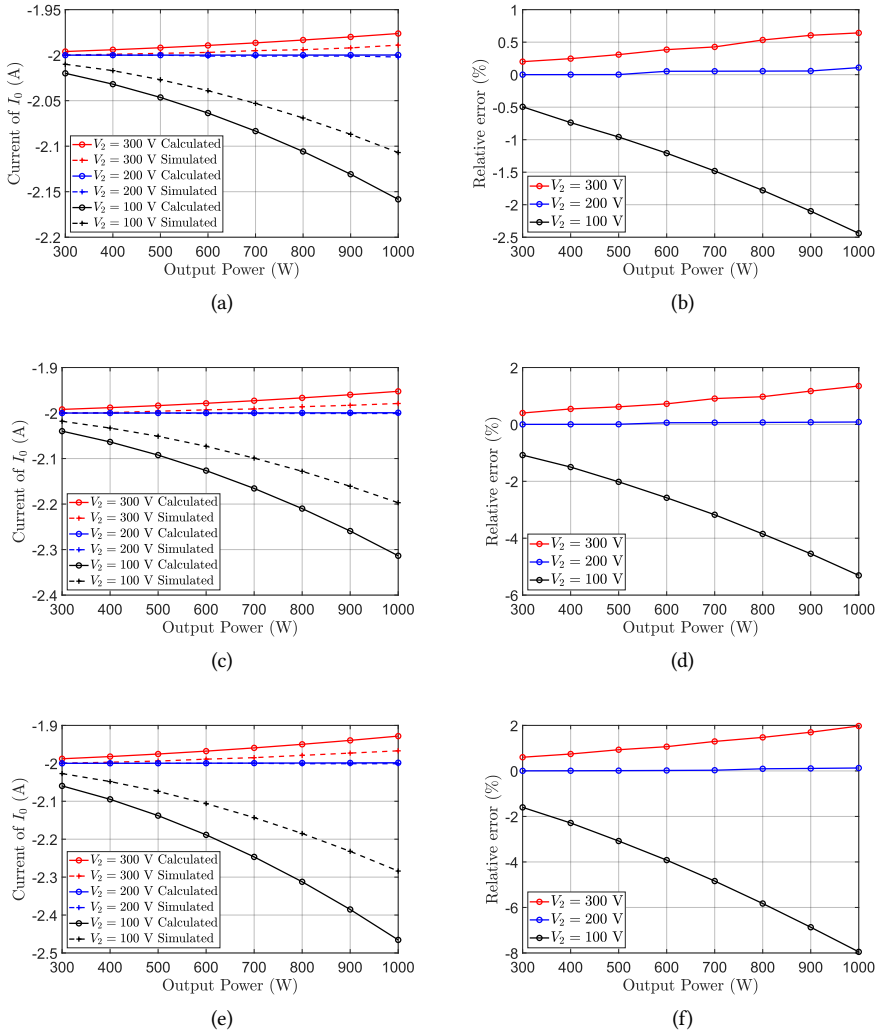


Figure 4.14: Calculated and simulated switching current of I_0 and its relative error when $V_1 = 400$ V with different parasitic resistances of 0.2 Ω, 0.4 Ω and 0.6 Ω, respectively. (a) I_0 at 0.2 Ω. (b) Relative error at 0.2 Ω. (c) I_0 at 0.4 Ω. (d) Relative error at 0.4 Ω. (e) I_0 at 0.6 Ω. (f) Relative error at 0.6 Ω.

and 250 kHz given in Table 4.8 in Section 4.5. As it can be seen, the inductance maintains a constant during a wide frequency range.

Second, it is assumed that the inductor current line is linear, which might not be valid under high power case with large parasitic resistance. For example, Figure 4.18 shows the inductor voltage and current waveforms when the parasitic resistance is intentionally selected at 1 Ω. As it can be seen, the inductor current is not strictly linear, which introduces the difference between the calculated and simulated results. A larger resistance and a larger

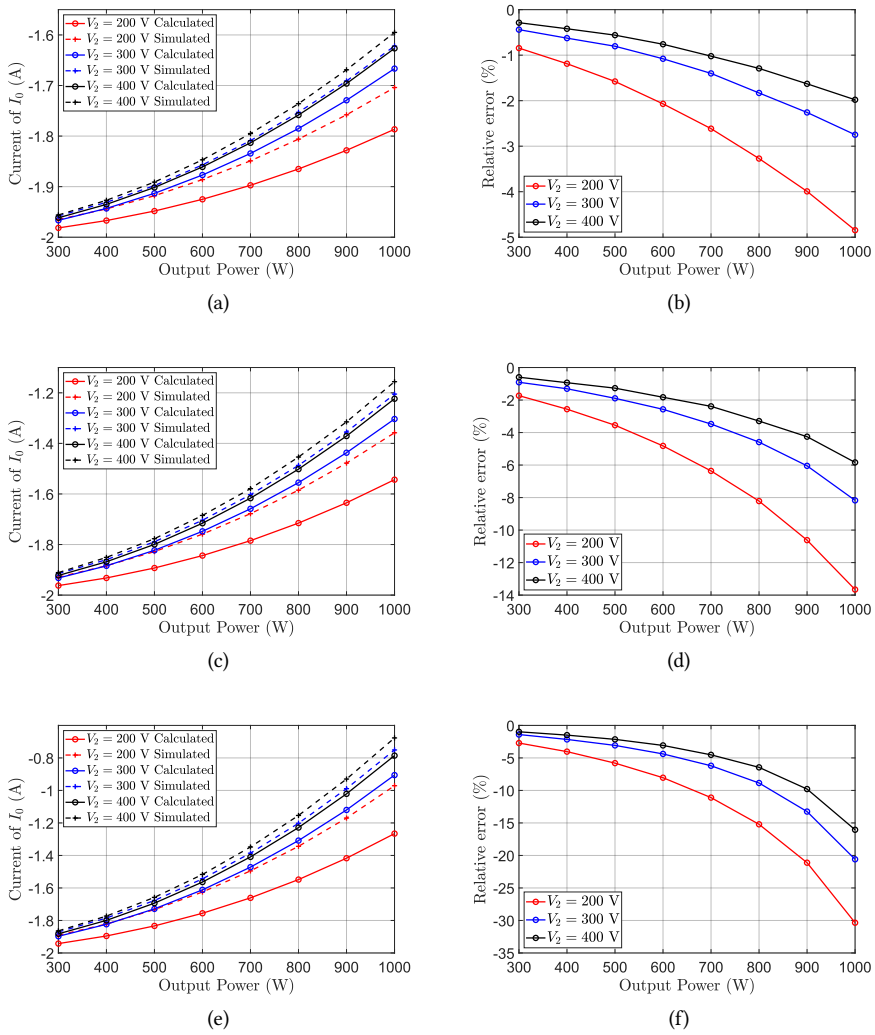
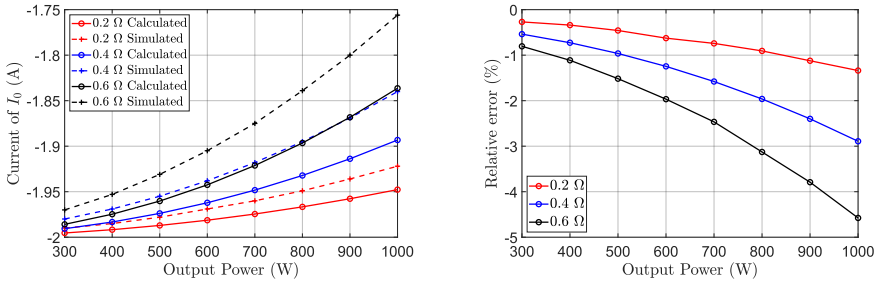


Figure 4.15: Calculated and simulated switching current of I_0 and its relative error when $V_1 = 100$ V with different parasitic resistances of 0.2 Ω, 0.4 Ω and 0.6 Ω, respectively. (a) I_0 at 0.2 Ω. (b) Relative error at 0.2 Ω. (c) I_0 at 0.4 Ω. (d) Relative error at 0.4 Ω. (e) I_0 at 0.6 Ω. (f) Relative error at 0.6 Ω.

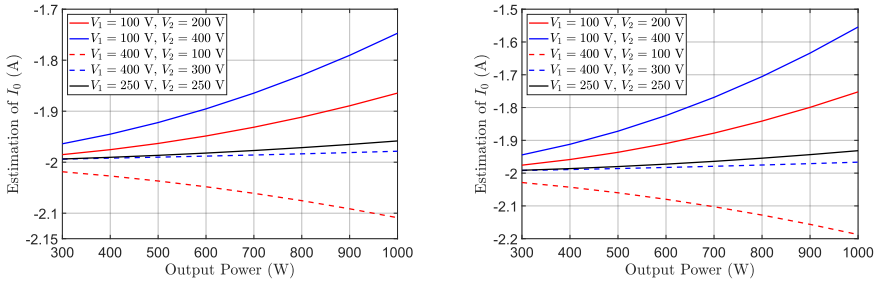
current will lead to a larger difference between these two values, which also explains the results shown in Figures 4.14 to 4.16.

Third, different from the case of reverse parallel current conduction described in [87], it is assumed that during reverse conduction, the current only passes through the MOSFET channel, which is due to the larger forward voltage drop of the SiC MOSFET body diode compared with its Si counterparts. For example, the minimum initial conduction voltage drop of the body diode of C3M0075120J is around 2.2 V, considering its typical 75 mΩ



(a) (b)

Figure 4.16: Calculated and simulated switching current of I_0 and its relative error when $V_1 = V_2 = 250$ V with different parasitic resistances of 0.2 Ω, 0.4 Ω and 0.6 Ω, respectively. (a) Value of I_0. (b) Relative error.



(a) (b)

Figure 4.17: Estimation of I_0 under different operating cases with two parasitic resistances. The total parasitic resistance is the sum of 0.1 Ω or 0.2 Ω and the value in Figure 4.12. I_0 is supposed to be −2 A in ideal condition. (a) I_0 with 0.1 Ω added to Figure 4.12. (b) I_0 with 0.2 Ω added to Figure 4.12.

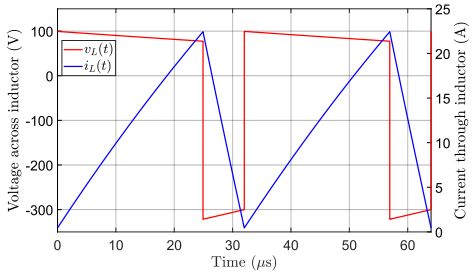


Figure 4.18: A simulation example of inductor current and voltage, $V_1 = 100$ V, $V_2 = 400$ V, $f_s = 31.25$ kHz, $P_o = 1$ kW, $L = 100$ μH, parasitic resistance is 1 Ω.

channel resistance, the current shunting phenomenon of the body diode will only occur when the reverse conduction current is larger than 29.3 A. In this work, two MOSFETs are

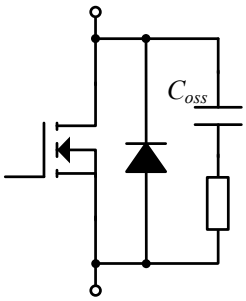


Figure 4.19: MOSFET model including parasitic capacitance of C_{oss}.

in parallel, and the peak current is around 22 A, so, this assumption is valid.

Finally, during the proposed analysis, the dead time and its corresponding circuit resonant behaviour during this period is not considered, which might introduce extra error. Due to complexity of the circuit behavior, simulation was carried out in PLECS circuit simulator to study the influence from the dead time with a more practical modeling of the MOSFET shown in Figure 4.19. It should be noted that a small resistor was connected in series with the parasitic capacitance to avoid simulation errors, and this value is selected to be 1e-4 Ω. The detailed parameters were selected as follows: The parasitic capacitance (C_{oss}) is 200 pF and 500 pF; The dead time (t_{dead}) is 150 ns and 300 ns; The MOSFET channel resistance (R_{ds}) is 50 mΩ while the inductor resistance (R_L) is 350 mΩ. As for the body diode, its forward voltage is 2.2 V and its on resistance is 0.18 Ω. The frequency is calculated through the formulas in Table 4.1 while the duty cycle is fine tuned with a 0.05% duty cycle step to meet the expected output voltage. Variable-step stiff solver is adopted with a maximum step size of 1e-8 s (i.e., 10 ns) and 1e-6 relative tolerance. The simulated results of the valley current (I_0) are shown in Figure 4.20, and the definition of relative error was given in Section 4.4.3. It can be seen that the larger the C_{oss} and dead time, the larger the error between the calculated and simulated results. The maximum error can reach 15% in the given example. Therefore, the circuit resonant behavior during the dead time could be considered to improve the proposed analysis as future work.

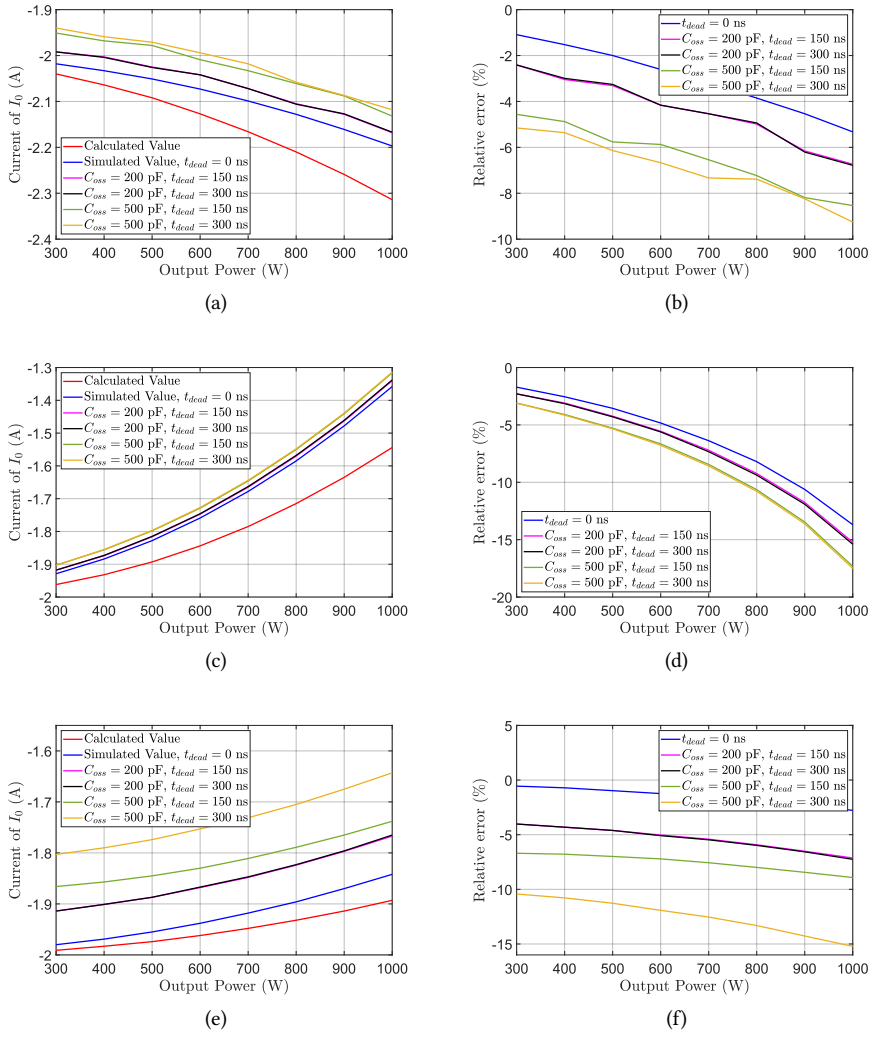
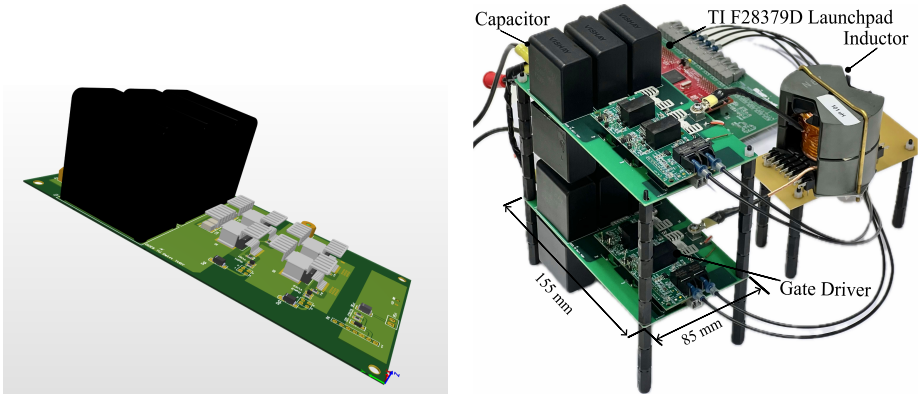


Figure 4.20: Calculated and simulated values of I_0 and its relative error with different parasitic capacitance and dead time values using a more practical MOSFET model. (a) Buck operation case, $V_1 = 400$ V and $V_2 = 100$ V. (b) Relative error under Buck operation. (c) Boost operation case, $V_1 = 100$ V and $V_2 = 200$ V. (d) Relative error under Boost operation. (e) Buck-Boost operation case, $V_1 = V_2 = 250$ V. (f) Relative error under Buck-Boost operation.

4.5 Experimental Verification

A laboratory prototype of FSBB converter was built for the experiment, which can be operated in TCM-ZVS buck, boost and buck-boost modes. The converter prototype is shown in Figure 4.21.

The experiment was carried out in three cases, i.e., buck, boost and buck-boost operating modes. For buck operation case, the input voltage is 400 V while for boost operation case,



(a) (b)

Figure 4.21: (a) 3D layout of the designed half-bridge board from Altium Designer. (b) Laboratory prototype of the FSBB converter featuring TCM-ZVS buck, boost and buck-boost operating modes.

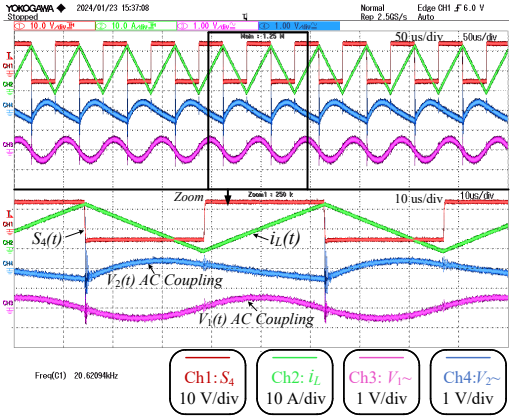


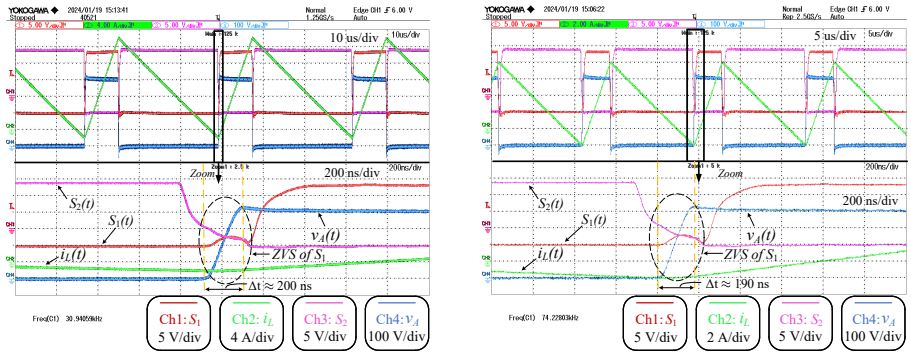
Figure 4.22: Voltage ripple under boost operation, $V_1 = 100$ V, $V_2 = 200$ V and $P_o = 1$ kW. $S_4(t)$ is the gate-to-source voltage of S_4.

the input voltage is 100 V. For buck-boost operation case, both the input and output voltages are 250 V. The output power varies between 300 W and 1 kW. The reverse switching current value of I_0 is selected as -2 A for the experiment. The dead time defined by the two gate-to-source voltage signals crossing zero volt was around 230 ns. The measured inductance value is given in Table 4.8, which is around 101 μH by Keysight E4990A impedance analyzer. The SiC MOSFET channel resistance (two in parallel) was also measured, and its values are given in Appendix in this chapter.

Keysight current probe N2782B featuring 50 MHz bandwidth, ±10 mA amplitude accuracy and maximum 30 Arms current rating was adopted to measure the inductor current. Before each set of measurements, the current probe is demagnetized to guarantee

Table 4.8: Measured inductance

f_s (kHz)	10	20	60	100	150	200	250
L (μH)	101.1	101.0	101.0	101.1	101.1	101.1	101.2



(a) (b)

Figure 4.23: TCM-ZVS buck operation, $V_1 = 400$ V, $V_2 = 100$ V. $S_1(t)$ is the gate-to-source voltage of S_1, $S_2(t)$ is the gate-to-source voltage of S_2, $v_A(t)$ is the voltage across switch S_2 shown in Figure 4.6. (a) $P_o = 1$ kW. (b) $P_o = 300$ W.

its measurement accuracy. Keysight N2791A differential voltage probe with 25 MHz bandwidth was adopted to measure the voltage signals.

4.5.1 Voltage Ripple Verification

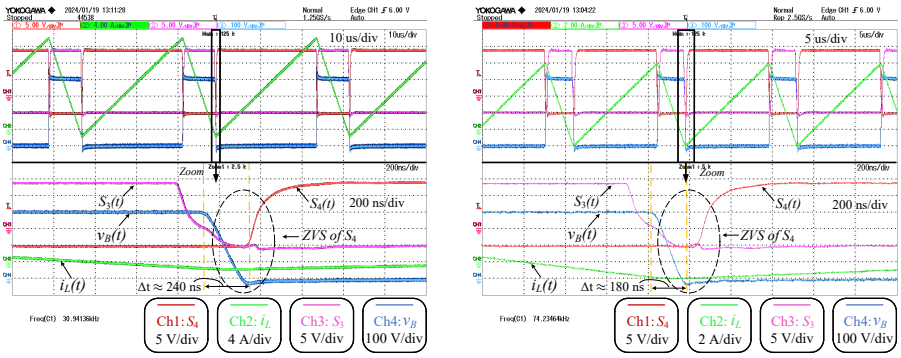
Figure 4.22 shows the voltage ripple of the converter under boost mode operation when $V_1 = 100$ V, $V_2 = 200$ V and $P_o = 1$ kW. As it can be seen, the peak-to-peak voltage ripples of the input and output sides match the derived formulas in Table 4.3 and the result shown in Figure 4.11(a).

4.5.2 TCM-ZVS Operating Waveforms

In order to show the parasitic resistance influence on the value of I_0, two sets of experiments were carried out with or without external 84 mΩ resistor.

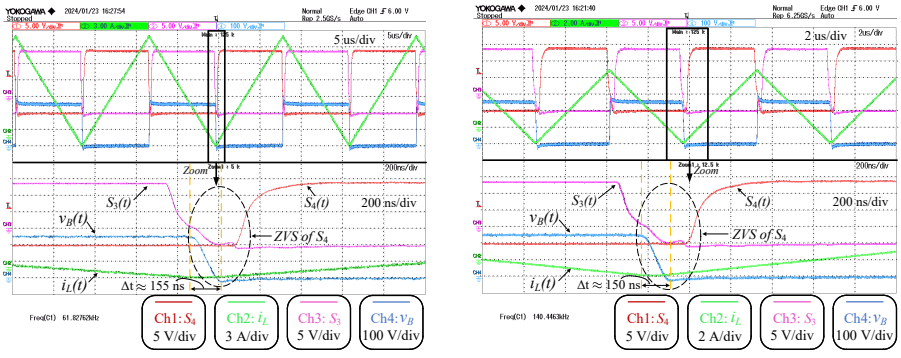
Figures 4.23 to 4.25 show the typical experimental results in buck, boost and buck-boost mode operation cases under 300 W and 1 kW without external resistor, respectively.

By comparing the gate-to-source voltage of S_4 at the moment when v_B drops to zero (marked by the orange dashed line) or the time it takes for v_B to drop to zero (the time between the two orange dashed lines) in Figure 4.24, it can be inferred that the absolute value of I_0 from 1 kW operation is smaller than the one in 300 W condition. However, this phenomenon is not obvious in Figures 4.23 and 4.25 when the converter operates in buck and buck-boost modes, which is as expected from the description in Section 4.4.3.



(a) (b)

Figure 4.24: TCM-ZVS boost operation, $V_1 = 100$ V, $V_2 = 400$ V. $S_3(t)$ is the gate-to-source voltage of S_3, $v_B(t)$ is the voltage across switch S_4 shown in Figure 4.6. (a) $P_o = 1$ kW. (b) $P_o = 300$ W.



(a) (b)

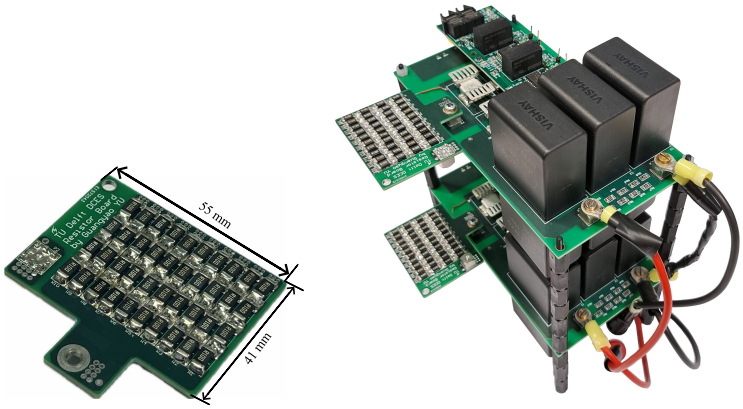
Figure 4.25: TCM-ZVS buck-boost operation, $V_1 = 250$ V, $V_2 = 250$ V. (a) $P_o = 1$ kW. (b) $P_o = 300$ W.

4.5.3 Measured Values of Reverse Switching Current

The external 84 mΩ resistor consists of two 42 mΩ resistor boards, which is inserted into the inductor path illustrated in Figure 4.26.

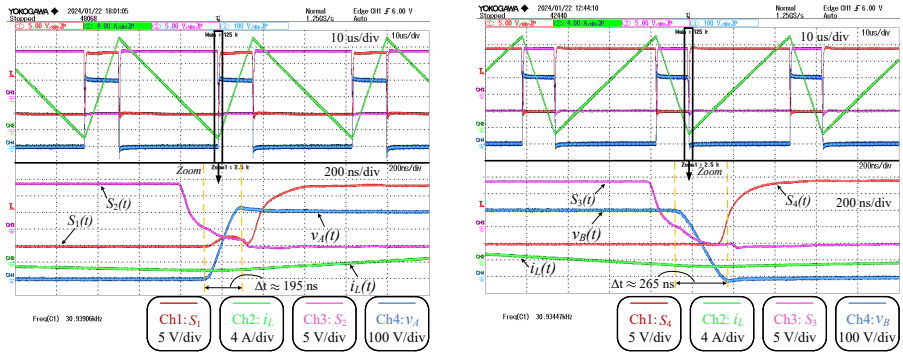
Since the reverse switching current is more likely to deviate from the ideal value under high power condition, and therefore the measured waveforms at 1 kW output power are given in Figure 4.27 as a comparison. By comparing the time between the two dashed orange lines, the absolute value of I_0 in Figure 4.27(b) is much less than the one in Figure 4.27(a).

In order to show the measured results of I_0, each operating point was measured twice. The averaged value of I_0 are given in Figure 4.28, and the length of the error bar represents the standard deviation σ of the measurement at that point, which is $\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \bar{x})^2}$,



(a) (b)

Figure 4.26: Resistor board and its insertion into the inductor path. (a) 42 mΩ external resistor board. Resistor type is CRA2512-FZ-R100ELF. (b) FSBB converter with external resistor.



(a) (b)

Figure 4.27: Measured waveforms with an external 84 mΩ resistor, P_o = 1 kW. (a) Buck operation, V_1 = 400 V, V_2 = 100 V. (b) Boost operation, V_1 = 100 V, V_2 = 400 V.

where x_i is the measured I_0 for each test, $\bar{x}$ is the averaged value, and N is the number of measurements. In particular, when $N = 2$, the standard deviation is $\sigma = \frac{1}{2}|x_1 - x_2|$. The deviation of I_0 from ideal value is also given, which is defined as $deviation = \dfrac{I_{0\_measured} - I_{0\_ideal}}{|I_{0\_ideal}|}$.

From the measured results, it can be seen that under TCM-ZVS boost mode operation, I_0 increases obviously when power increases, besides, when the parasitic resistance increases by adding an external resistor, this phenomenon is more obvious, which is as expected according to the analysis in Section 4.4. For TCM-ZVS buck operation, I_0 basically maintains at a constant value close to −2.0 A indicating that it is less susceptible to the parasitic

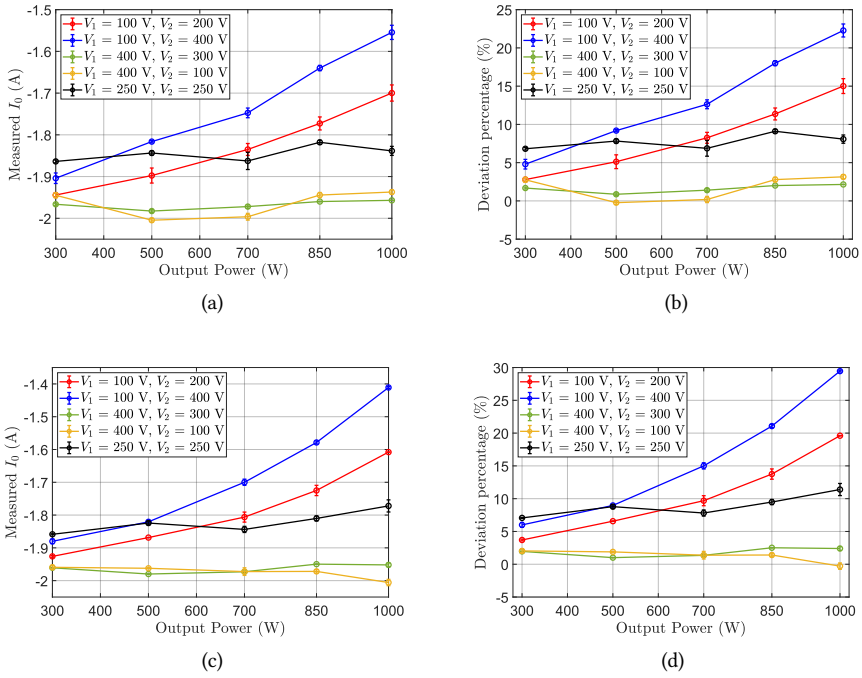


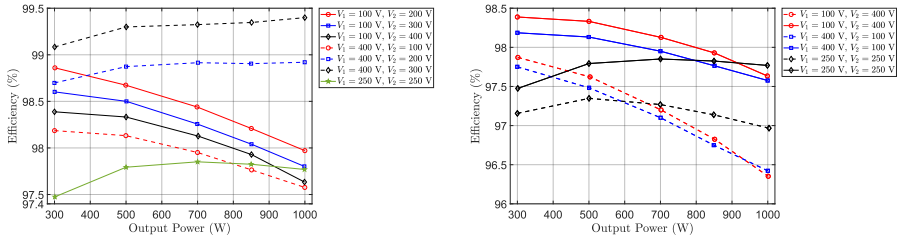
Figure 4.28: Measured value of I_0 and its deviation from the ideal value at different operating points with and without external 84 mΩ resistor. (a) Measured I_0 without external resistor. (b) Deviation percentage of I_0 without external resistor. (c) Measured I_0 with external resistor. (d) Deviation percentage of I_0 with external resistor.

resistance.

4.5.4 Efficiency and Thermal Performance

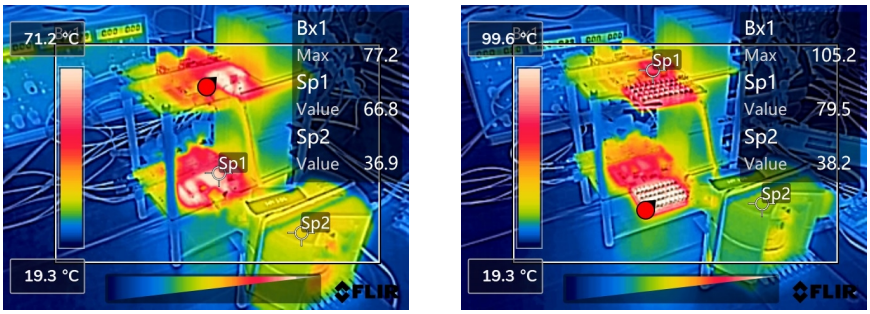
The efficiency performance of the FSBB converter is shown in Figure 4.29 as a reference. It should be noted that the power losses from the auxiliary power supply for the gate drivers are not included. The efficiency was measured by Yokogawa WT500. The measured efficiency values in Figure 4.29(a) is comparable to the mainstream efficiency of similar converters today [69],[74], [77], [51], [55]. Therefore, the measured results of the reverse switching current in Figure 4.28 also provide valuable information for the TCM-ZVS modulation design based on current commercial SiC MOSFET.

Figure 4.30 shows the steady-state thermal image of the prototype converter operating at $V_1 = 100$ V, $V_2 = 200$ V, $f_s = 20.63$ kHz and $P_o = 1$ kW condition continuously after 40 minutes with an ambient temperature around 21°C by Teledyne FLIR C5. Due to the possible reflection from the adopted 7106DG heatsink, black electrical tape was used to increase its emissivity according to [88]. The converter is natural cooled and the hottest spot from Figure 4.30(a) is around 77.2°C. In this case of boost operation, S_1 is always on and has the highest thermal stress among the four switches. The rms current through each (two in parallel) MOSFET is around 6.1 A, and the calculated conduction loss would be



(a) (b)

Figure 4.29: Measured efficiency of FSBB converter at different operating points. (a) Measured efficiency without external resistor. (b) Efficiency comparison, dashed lines represent the values with an external 84 mΩ resistor while solid lines represent the values without external resistor.



(a) (b)

Figure 4.30: Steady-state thermal image of the converter operating continuously at $V_1 = 100$ V, $V_2 = 200$ V, $f_s = 20.63$ kHz and $P_o = 1$ kW after 40 minutes with an ambient temperature around 21°C. (a) Thermal image without adding external resistor board, and measured efficiency is 97.9%. (b) Thermal image with external resistor board, and measured efficiency is 96.6%.

around 2.7 W. By further checking the thermal resistance (40°C at 2 W) of the 7106DG heatsink, this temperature rise is reasonable.

4.6 Conclusion

In this chapter, the reverse switching current required for TCM-ZVS modulation is revisited for buck, boost and buck-boost converters considering the influence from the parasitic resistances with variable-frequency voltage-mode control. Universal and detailed closed-form equations of the new modified duty cycle and switching current are derived. The models show that the parasitic resistance could have a negative impact on the reverse switching current, which may lead to unexpected loss of ZVS turn-on. For the operating specifications adopted in this work, this phenomenon is more obvious in boost mode. A four-switch buck+boost converter featuring multi-mode operation capability was built to verify the proposed analysis. The influence from the dead time combined with the parasitic resistance can be a future study to further improve the accuracy of the analytical model.

4.7 Appendix

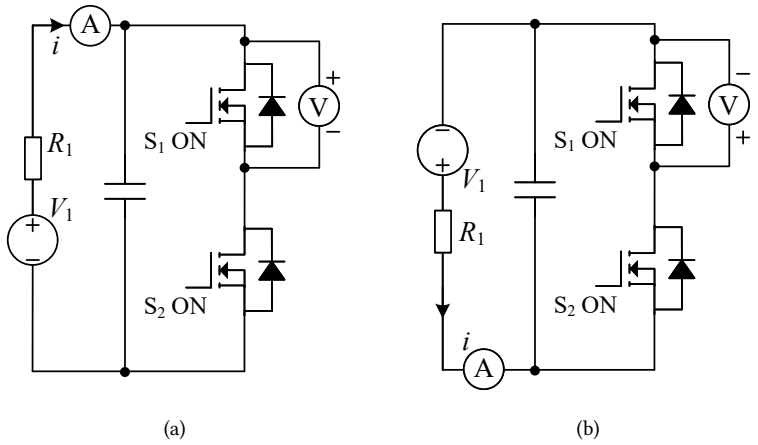


Figure 4.31: Static MOSFET R_{ds} measurement circuit, taking S_1 as an example. (a) Forward conduction R_{ds} measurement. (b) Reverse conduction R_{ds} measurement.

Figure 4.31 shows the static MOSFET channel resistance measurement circuit. In Figure 4.31, R_1 functions as a current limiting resistor. Due to the extremely large insulation resistance of the dc link capacitor, the leakage current through this branch is negligible. The measured results are given in Table 4.9 at a room temperature of 20°C. S_1-S_4 correspond to the switches shown in Figure 4.6.

Table 4.9: Measured results of forward and reverse conduction channel voltages and currents

Current (A)	1	3	5	7	9
V_{ds} of S_1 (mV)	35.47	107.04	180.20	256.99	335.62
V_{ds} of S_2 (mV)	38.28	115.33	194.69	279.90	361.63
V_{ds} of S_3 (mV)	36.62	110.74	186.32	265.36	346.60
V_{ds} of S_4 (mV)	34.37	103.77	174.93	248.80	324.00
V_{sd} of S_1 (mV)	35.44	106.11	176.89	248.92	327.89
V_{sd} of S_2 (mV)	37.49	112.35	187.75	265.67	345.90
V_{sd} of S_3 (mV)	36.49	109.20	182.09	256.14	333.00
V_{sd} of S_4 (mV)	34.30	102.76	171.65	242.30	314.90

5

Single Mode Variable-Frequency ZVS Modulation For FSBB Converter

This chapter studies the detailed design and implementation of an improved variable-frequency zero voltage switching (ZVS) modulation method where the inductor current has three segments during the whole operational range. By fixing the duty cycle for the switch in the buck-type or boost-type half-bridge circuit, and controlling the duty cycle of the switch in the other half-bridge circuit, the FSBB converter could realize a smooth transition at the boundary of unit voltage gain. Combined with variable-frequency control, zero voltage switching for the four switches can be achieved within a wide operational range without compromising the inductor rms current compared with triangular current mode (TCM) ZVS modulation. Based on this, a simple closed-loop control was proposed without the need of inductor or switch current detection. In addition, the capacitance selection of input and output capacitors is analyzed and derived in detail in this chapter, which was missing in the previous research. Finally, a laboratory prototype of an FSBB converter was built and tested to verify the proposed concepts with an input voltage of 250−600 V, output voltage of 400 V and output power value of 250−2500 W. [1]

[1]This chapter is based on:

G. Yu, J. Dong, T. B. Soeiro and P. Bauer, "A Variable-Frequency ZVS Modulation for Four-Switch Buck+Boost Converters with Seamless Step-up/down Mode Transition," 2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia), Jeju Island, Korea, Republic of, 2023, pp. 2808-2813, doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213482.

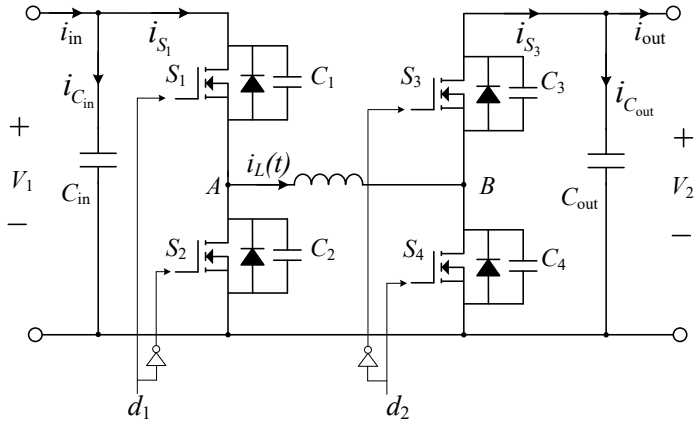


Figure 5.1: Circuit topology of the four-switch buck+boost (FSBB) converter.

5

5.1 Introduction

Recently, more attention has been paid to the nonisolated four-switch buck+boost (FSBB) converter with the circuit topology shown in Figure 5.1. This is due to its bidirectional power flow capability. Another reason is that it has both voltage step-up and step-down capabilities. For example, this converter has found a good application in the field of electric vehicles (EVs) charging due to its excellent performance for the wide operating range of input and output voltage values.

There are two main different classification methods on the modulation schemes for the FSBB converter: The first one is based on the modulation methods of soft switching and hard switching while the second one is based on single-mode and multi-mode modulation methods, which is well summarized in [77]. With the pursuit of higher power density, the switching frequency of the power electronic converters has been increasing over the last decades due to the continual advancement in power semiconductor device technology [71]. In order to reduce the switching losses accompanied by the high switching frequency operation even with adoption of wide band-gap devices [50], [58], soft-switching techniques including zero-voltage switching (ZVS) and zero-current switching (ZCS) are still required. Therefore, only soft switching modulation is considered in this chapter.

According to [72], ZVS turn-on and ZCS turn-off can almost completely eliminate the switching losses. Meanwhile, due to the existence of output parasitic capacitance C_{oss}, the turn-on losses of MOSFET switches are typically larger than its turn-off losses [57], and therefore, to eliminate the switching losses through ZVS turn-on is preferred. Depending on whether the switching frequency changes, the soft-switching modulation strategies for the FSBB converter can further be divided into fixed-frequency and variable-frequency ZVS modulations. For these two ZVS modulations, the basic principle is to utilize the inductor current during the dead time to charge and discharge the parasitic output capacitance C_{oss} of the MOSFET such that when the drain-source voltage damped to zero through the body diode conduction, the MOSFET can be turned on at zero voltage

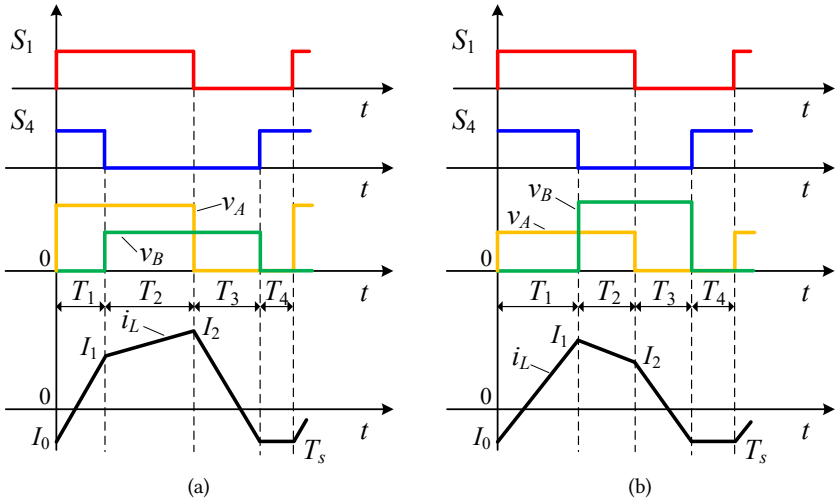


Figure 5.2: Fixed-frequency four-segment inductor current mode ZVS modulation method, I_0 is negative. (a) $V_1 > V_2$. (b) $V_1 < V_2$.

to reduce the switching losses. The quadrilateral or four-segment inductor current control scheme has received a lot of attention and research since it was proposed in [62], and its modulation scheme is shown in Figure 5.2. In [57], the switching times of the switches were studied to maximize the power transfer under ZVS condition with a constant frequency, but the optimization on inductor root-mean-square (rms) current reduction was missing. Zhou et al. [63] revisited the same modulation concept and proposed a control strategy to minimize the inductor rms current, which control scheme was implemented in a 300 W prototype operating at a frequency of 800 kHz. However, the optimized switching times need to be calculated offline due to the complexity of the equations. In [89] and [90], a constant frequency pulse width modulation (PWM) plus phase-shift control was proposed to achieve ZVS in full input voltage and load range while minimize the inductor rms current, which consists of two operating modes under different load conditions, i.e., pseudocritical continuous current mode (PCRM) and pseudocritical discontinuous current mode (PDCM). This proposed concept was verified through an analog circuit due to the need of high-frequency inductor current detection. However, this modulation scheme poses challenges in parameter selection of inductance and frequency in order to achieve a wide range of heavy load operation. In fact, if the optimal solution in [63] happens when T_4 equals zero (cf., Figure 5.2), which is usually the case, then the analytical solution is given in [89], and thus, the derived inductor rms current will be the same based on [63] and [89]. This will be further discussed in Section 5.3.

Apart from fixed-frequency modulation strategy, variable-frequency modulation is also a popular control scheme adopted in power electronic converters, e.g., triangular current mode (TCM) ZVS modulation [46], [69], [91]. In [50] and [51], TCM-ZVS modulation was extended to the transition mode, however, with this modulation, the rms value of the inductor current is not optimized, and therefore, a sudden efficiency drop was observed,

besides, an abrupt frequency and duty cycle change during the transition between different operating modes can also be found. In [77], all the possible variable-frequency ZVS modulation cases were studied in the buck-boost-type (transition) mode with duty cycle of d_1 for switch S_1 being larger than d_2 for switch S_4 (cf., Figure 5.1), it is found that the three-segment inductor current mode modulation is the most suitable solution in terms of inductor rms current reduction and convenient operation. Zhe Yu et al. proposed a novel variable-frequency ZVS modulation method in [60], however, the analytical solutions were missing. In [92], an improved single mode control strategy was proposed with a fixed duty cycle applied to switch S_1 , which, however, is a fixed-frequency hard-switching modulation. As a further extension of the work in [63], Tian et al. proposed a combination control of fixed- and variable-frequency modulation scheme, and a monotonic relationship between the inductor rms current and peak current was found through figure plotting, which, however, increases the control complexity [64]. In [93], a closed-loop operation based on feed-forward control of a variable-frequency multi-mode quasi-resonant boundary-conduction mode was introduced for the FSBB converter, however, it can still be obviously seen from the experiments that the valley current changes significantly during mode transitions.

Based on the aforementioned research progress, this chapter studies the detailed design and implementation of a variable-frequency zero voltage switching modulation suitable for an FSBB converter, which has the advantage of seamless transition between step-up and step-down operating modes. Based on this, a simple and convenient closed-loop control method was proposed without the need of inductor or switch current detection. The capacitance selection of input and output capacitors was found to be missing in the previous research, which will also be analyzed and solved in this chapter.

The rest of the work is organized as follows. Section 5.2 introduces the working principle of a variable-frequency ZVS modulation with seamless step-up/down mode transition for FSBB converters and its closed-loop control method. In Section 5.3, design considerations including the effect of duty cycle selection on the ZVS operating range, capacitance selection, benchmark of different modulation schemes on inductor rms current are shown. Section 5.4 presents the losses breakdown and estimated efficiency of the FSBB converter. Experimental results are given in Section 5.5. Finally, Section 5.6 concludes this chapter.

5.2 Converter Operation Principle

5.2.1 Basics of Converter Operation

Figure 5.1 shows the circuit topology of the FSBB converter. The basic operating principle is already described in Chapter 3. For ease of reading, the operating principle will be repeated here. Semiconductor switches of S_1 and S_2 form the buck-type half-bridge while switches of S_3 and S_4 form the boost-type half-bridge. Some assumptions are made for the analysis [78], [77], [94]:

1) The PWM signals to each half bridge are complementary, and the dead time is neglected.

2) The inductance is a constant during operation.

3) The nonideal factors such as power losses and any possible parasitic parameters are

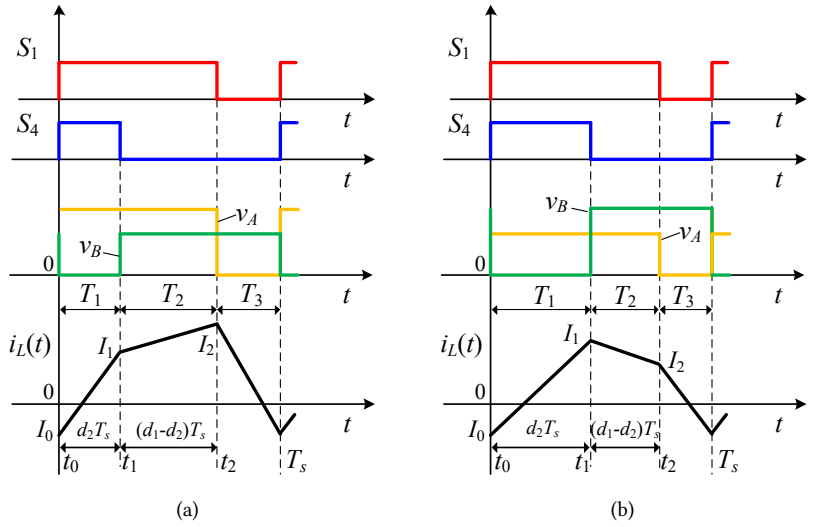


Figure 5.3: Gating signals and its corresponding inductor waveforms. (a) $V_1 > V_2$. (b) $V_1 < V_2$.

neglected.

Defining d_1 and d_2 as the duty cycles applied to S_1 and S_4, the average voltage values of points A and B with regard to the bottom-side dc-bus rail are

$$\bar{v}_A = d_1 V_1, \quad \bar{v}_B = (1 - d_2) V_2, \tag{5.1}$$

where V_1 and V_2 are the input and output voltages. According to the inductor volt-second balance law under quasi-steady-state operation, the average voltage across the inductor should be zero, by relating $\bar{v}_A = \bar{v}_B$, the voltage gain can be simply derived as

$$G_v = \frac{V_2}{V_1} = \frac{d_1}{1 - d_2}. \tag{5.2}$$

Equation (5.2) always holds in an ideal case regardless of the load conditions.

5.2.2 Simple ZVS Modulation Scheme with Seamless Mode Transition

In order to achieve ZVS turn-on, the inductor current is required to be negative during the turn-on transition of S_1 and S_4, and to be positive during the turn-on transition of S_2 and S_3 [77]. In [77], all the variable-frequency modulation cases were studied through phase-shift technique with duty cycle d_1 being larger than d_2, it is found that the three-segment inductor current mode modulation could reduce the inductor rms current with a relatively larger d_1 in the transition mode. In this work, this three-segment inductor current mode modulation will be extended to cover the whole converter operating range. The gating signals and its corresponding inductor current waveforms are illustrated in Figure 5.3.

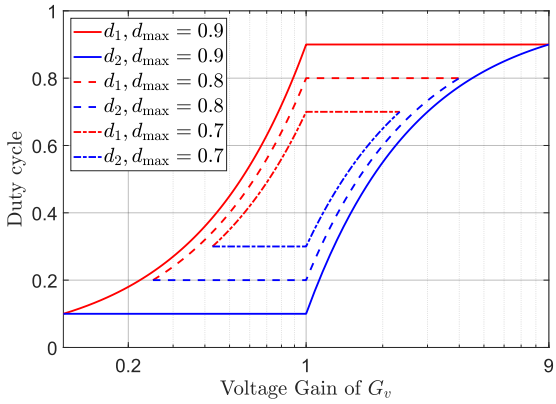


Figure 5.4: Possible voltage gain under different values of $d_{\max}$ with $d_1 > d_2$.

5

It can be found that this modulation method has three independent variables, i.e., d_1, d_2 and f_s. The switching frequency f_s is utilized to maintain I_0 at a fixed negative value. In order to realize a seamless transition, the control variables are suggested to be continuous when the converter crosses the unit voltage gain boundary when V_1 equals V_2 [64]. At the unit voltage gain boundary, based on (5.2), the duty cycles of d_1 and d_2 should satisfy the following expression

$$d_1 + d_2 = 1. \tag{5.3}$$

Naturally, based on the aforementioned discussion, a modulation strategy featuring a seamless step-up/down mode transition can be proposed as follows

$$d_1 = \begin{cases} G_v(1-d_{\min}), G_v < 1 \\ d_{\max}, G_v \geq 1. \end{cases}, d_2 = \begin{cases} d_{\min}, G_v < 1 \\ 1 - \frac{d_{\max}}{G_v}, G_v \geq 1. \end{cases} \tag{5.4}$$

In (5.4), $d_{\max}$ and $d_{\min}$ are the maximum and minimum duty cycles, respectively, and $d_{\min} + d_{\max} = 1$. As an illustration example, Figure 5.4 shows the range of voltage gain under different selections of $d_{\max}$ with $d_1 > d_2$.

For the modulation shown in Figure 5.3, in both step-up and step-down cases, the inductor current waveform can be expressed as follows with $t_0 = 0$,

$$i_L(t) = \begin{cases} I_0 + \dfrac{V_1}{L}t, & 0 < t \leq t_1 \\ i_L(t_1) + \dfrac{V_1 - V_2}{L}(t - t_1), & t_1 < t \leq t_2 \\ i_L(t_2) - \dfrac{V_2}{L}(t - t_2), & t_2 < t \leq T_s. \end{cases} \tag{5.5}$$

In (5.5), I_0 is the reverse switching current featuring a negative value, $T_1 = t_1 - t_0 = d_2 T_s$, $T_2 = t_2 - t_1 = (d_1 - d_2)T_s$, T_s is the switching period, L is the inductance.

For the FSBB converter, the inductor current is only transferred to the output side when S_3 is on, so, the average output current is

$$I_{\text{out}} = \frac{I_1 + I_2}{2}(d_1 - d_2) + \frac{I_2 + I_0}{2}(1 - d_1), \tag{5.6}$$

where I_1 and I_2 are the corner current values. According to (5.2), (5.5) and (5.6), the switching frequency can be derived as (5.7) for both step-up and step-down cases:

$$f_s = \frac{V_1[d_1(1-d_1) + d_2(d_1 - d_2)]}{2L[I_{\text{out}} - I_0(1-d_2)]}. \tag{5.7}$$

It can be seen from (5.7) that the switching frequency and power are inversely proportional. When the converter operates at a low power condition, the frequency could be high and vice versa. In practical application, a frequency limiter will be adopted to prevent the switching frequency from being too high or too low. Therefore, the switching point current values of I_0, I_1 and I_2 have to be discussed under two cases depending on the switching frequency when it is inside the defined range or when it is clamped to the maximum or minimum value.

Switching Point Current Values With Frequency Inside the Defined Range

For a well-designed converter, its operating frequency will be within the defined range under most operating conditions. In this case, I_0 is selected as a fixed negative value for variable-frequency modulation, so, I_1 and I_2 can be simply derived by substituting (5.7) into (5.5), which yields

$$I_1 = I_0 + \frac{d_2}{q}, \quad I_2 = I_0 + \frac{d_1(1-d_1)}{q(1-d_2)}, \tag{5.8}$$

where $q = \dfrac{d_1(1-d_1) + d_2(d_1 - d_2)}{2[I_{\text{out}} - I_0(1-d_2)]}$. It can be seen from (5.8) that I_1 and I_2 are independent of inductance if the switching frequency is not clamped.

Switching Point Current Values with Clamped Frequency

In this case, the switching frequency is clamped to the pre-defined minimum or maximum value, and I_0 cannot be maintained as the predefined value. Based on (5.7), I_0 can be derived as

$$I_0 = \frac{I_{\text{out}}}{1-d_2} - \frac{V_1[d_1(1-d_1) + d_2(d_1 - d_2)]}{2Lf_s(1-d_2)}. \tag{5.9}$$

After determining I_0, the values of I_1 and I_2 can be derived accordingly as

$$I_1 = I_0 + \frac{V_1 d_2}{Lf_s}, \quad I_2 = I_0 + \frac{V_2(1-d_1)}{Lf_s}. \tag{5.10}$$

Substituting f_s with $f_{\max}$ or $f_{\min}$, then, the corresponding current values of I_0, I_1 and I_2 can be calculated respectively.

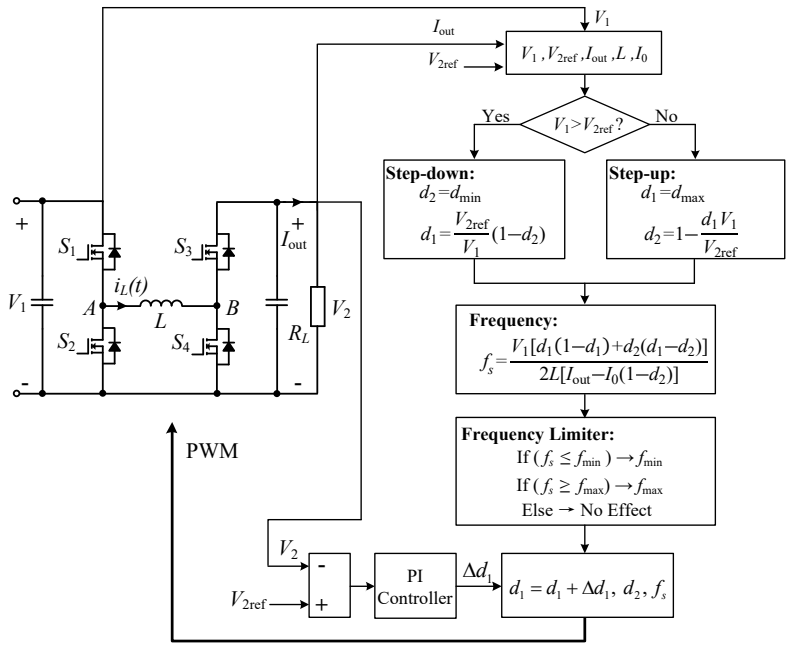


Figure 5.5: Voltage-Mode closed-loop control diagram based on derived equations.

Inductor RMS Current

The rms value of the inductor current shown in Figure 5.3 can be expressed as

$$I_{\text{rms\_}L} = \sqrt{I_{\text{rms1}}^2 + I_{\text{rms2}}^2 + I_{\text{rms3}}^2}. \tag{5.11}$$

In (5.11), I_{rms1}, I_{rms2} and I_{rms3} are the rms values of each segment of the inductor current, and they are

$$\begin{aligned} I_{\text{rms1}} &= \sqrt{d_2 \tfrac{I_0^2+I_1^2+I_0 I_1}{3}}, \quad I_{\text{rms2}} = \sqrt{(d_1-d_2)\tfrac{I_1^2+I_2^2+I_1 I_2}{3}}, \\ I_{\text{rms3}} &= \sqrt{(1-d_1)\tfrac{I_2^2+I_0^2+I_2 I_0}{3}}. \end{aligned} \tag{5.12}$$

From the discussions above, when the frequency is inside the range, both I_1 and I_2 are independent of inductance, combined with (5.11) and (5.12), it can be concluded that the rms value of the inductor current is also independent of inductance if the switching frequency is inside the defined range. It should be noted that this conclusion does not hold when the frequency is clamped to the minimum or maximum value.

5.2.3 Closed-loop Control Scheme

Based on the discussion above, a voltage-mode feedback control with a frequency limiter is proposed in Figure 5.5. Herein, control variable of Δd_1 for S_1 is preferred due to the possible existence of right-half plane zero in the transfer function caused by controlling Δd_2 for S_4 [78], which would make it harder to design the compensation loop compared with controlling Δd_1.

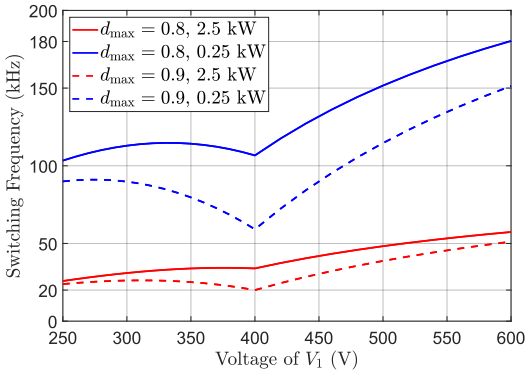


Figure 5.6: Switching frequency in terms of different values of input voltage, d_{max} and power, $I_0 = -2.5$ A, $L = 200$ μH.

5.3 Design Consideration

5

Before converter commissioning, some key parameters should be considered including selection of inductance, maximum duty cycle of d_{max}, input and output capacitors.

5.3.1 Selection of Inductance

In this work, the switching frequency is chosen between 20 kHz and 160 kHz according to the gate driver capability, i.e., $f_{min} = 20$ kHz and $f_{max} = 160$ kHz.

Due to the nonideal factors such as the rise and fall time of the gating signal, minimum pulse width and dead time, there is a limit to the maximum and minimum duty cycles [53], [95]. Herein, the maximum and minimum duty cycles are set as 0.9 and 0.1.

The inductance is selected as 200 μH, and the switching frequency is shown in Figure 5.6 under different power values. As it can be seen, the switching frequency is continuous at the unit voltage gain boundary as expected, which is an improvement compared with multi-mode variable-frequency modulation. The selection of I_0 will be discussed in detail later.

5.3.2 ZVS Requirement on Switching Current Value

The absolute values of the switching current shown in Figure 5.3 need to be larger enough to charge or discharge the MOSFET parasitic capacitance C_{oss} during the dead time so that the ZVS turn-on of the corresponding switch can be achieved.

The ZVS conditions have been described in detail in [51], [59], [60], [63], [64], [77], [96] with the assumption of the inductor current being a constant due to the small variation during the dead time, and the requirement for the corner current values is expressed as follows

$$I_0 t_{dead} \leq -2C_{oss} \cdot \max(V_1, V_2), \tag{5.13}$$

$$I_1 t_{dead} \geq 2C_{oss} V_2, \quad I_2 t_{dead} \geq 2C_{oss} V_1, \tag{5.14}$$

where t_{dead} is the dead time, C_{oss} is the equivalent output capacitance of a single switch.

For an FSBB converter, since the four switches will usually adopt the same type of MOSFETs, so it is assumed that C_{oss} of each switch is equal, i.e., $C_1 = C_2 = C_3 = C_4 = C_{\text{oss}}$ (cf., Figure 5.1). $\max(V_1, V_2)$ is the larger value between V_1 and V_2. It must be pointed out here that the output capacitance of a MOSFET exhibits a nonlinear dependence on the applied drain-source voltage of V_{ds}, thus, a linear charge-equivalent capacitance should be used, which is defined as $C_{Q,eq(V_{DS})} = \dfrac{1}{V_{DS}} \displaystyle\int_0^{V_{DS}} C_{\text{oss}}(v)dv$ [97], [98]. For the ease of analysis, a rough assumption is made for the C_{oss}, which is assumed to be a constant during the operations under varied voltages.

In this work, the dead time is selected as a fixed value. Define $I_{\text{zvs}} = \dfrac{2C_{\text{oss}}V_{\max}}{t_{\text{dead}}}$ with $V_{\max}$ being the maximum voltage value that the input or output voltage may encounter, herein, the value of $V_{\max}$ is 600 V, and therefore, I_0 can be chosen as follows

$$I_0 = -kI_{\text{zvs}}, \quad k \geq 1, \tag{5.15}$$

where k is a conservative coefficient. It should be pointed out that $V_{\max}$ is not equal to $\max(V_1, V_2)$, e.g., if $V_1 = 300$ V and $V_2 = 400$ V, then $\max(V_1, V_2) = 400$.

Based on (5.14) and (5.15), in order to realize ZVS turn-on of S_3 and S_2 with a specific input and output voltage value, I_1 and I_2 should satisfy the following expressions

$$I_1 \geq \frac{V_2}{V_{\max}} I_{\text{zvs}}, \quad I_2 \geq \frac{V_1}{V_{\max}} I_{\text{zvs}}. \tag{5.16}$$

Compared with previous research [63], [64] , [77], [89], [90], where I_{zvs} is selected as the minimum required ZVS current value for I_1 and I_2, (5.16) could provide a more accurate ZVS range prediction.

5.3.3 Minimum ZVS Load

For a well-designed FSBB converter, the inductance can be selected at a desired value so that when the converter is operated at rated load, the calculated switching frequency from (5.7) is near or slightly larger than the minimum value $f_{\min}$, which is also the inductance selection strategy in this chapter. Therefore, when the converter is operated under partial load, the switching frequency will increase and fall into the desired range. However, when the load keeps decreasing, the switching frequency will keep rising until the maximum value $f_{\max}$ at a certain point, and therefore, the ZVS boundary at light load should be calculated under the consideration of possible frequency clamping.

Minimum ZVS Load With Switching Frequency Inside the Designed Range

Combining (5.8), (5.15) and (5.16) yields the requirement to ensure a ZVS turn-on of S_3, which is

$$I_1 = I_0 + \frac{d_2}{q} = -kI_{\text{zvs}} + \frac{2d_2[I_{\text{out}} - I_0(1-d_2)]}{d_1(1-d_1) + d_2(d_1-d_2)} \geq \frac{V_2}{V_{\max}} I_{\text{zvs}} \tag{5.17}$$

After simplification, one can get

$$I_{\text{out}} \geq \frac{V_2}{V_{\max}} \cdot \frac{[d_1(1-d_1) + d_2(d_1-d_2)]}{2d_2} I_{\text{zvs}} + \frac{d_1(1-d_1) + d_2(d_1+d_2-2)}{2d_2} kI_{\text{zvs}}. \tag{5.18}$$

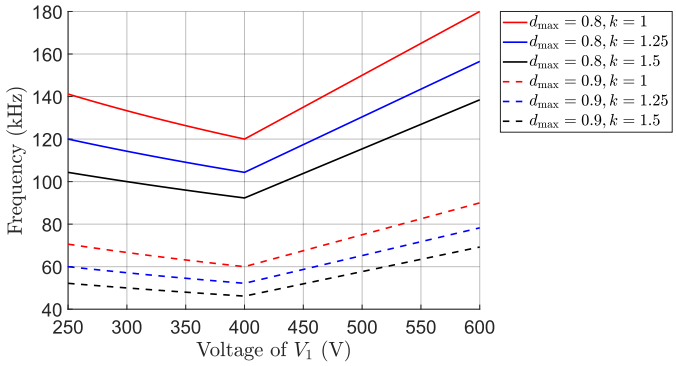


Figure 5.7: Switching frequency calculated from (5.7) according to the minimum ZVS load requirement of (5.18) and (5.19) in terms of different d_{max} and k values. $I_{zvs} = 2$ A, $L = 200$ μH.

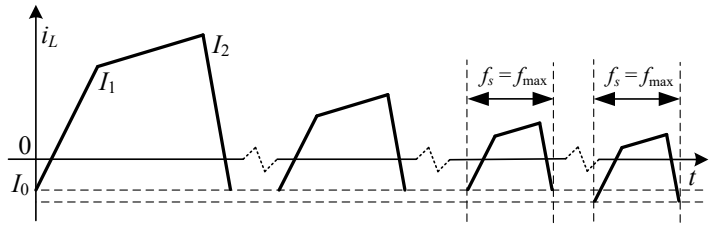


Figure 5.8: Illustration of the change trend of the inductor current when the load decreases, depicted with $V_1 > V_2$. With reduction of the load, the switching frequency will increase until its maximum value f_{max}, and the minimum inductor current can be maintained at a fixed negative value. However, if the load further decreases, the frequency will not change, and the minimum current starts to decrease.

Similarly, the requirement for the output current to ensure a ZVS turn-on of S_2 is

$$I_{out} \geq \frac{V_1}{V_{max}} \cdot \frac{(1-d_2)[d_1(1-d_1)+d_2(d_1-d_2)]}{2d_1(1-d_1)} I_{zvs} + \frac{(1-d_2)[d_2(d_1-d_2)-d_1(1-d_1)]}{2d_1(1-d_1)} kI_{zvs}. \tag{5.19}$$

Therefore, the required output current needs to satisfy: $I_{out} \geq \max\{(5.18),(5.19)\}$. Equations (5.18) and (5.19) lead to the same minimum I_{out} when $V_1 = V_2$ since $d_1 + d_2 = 1$, which is as expected since $I_1 = I_2$.

As mentioned in Section 5.2, the current values of I_1 and I_2 are independent of inductance if the frequency is not limited, so the minimum ZVS load derived from (5.18) and (5.19) is also independent of inductance.

Minimum ZVS Load with Frequency Clamped to f_{max}

In light load condition, the calculated frequency from (5.7) based on the results from (5.18) and (5.19) could be larger than the allowed maximum frequency f_{max}, for example, Figure 5.7 shows the frequency based on (5.18) and (5.19). In this case, the frequency will be clamped to f_{max}, I_0 starts to become less than $-kI_{zvs}$ explained by (5.9), i.e., $|I_0| \geq kI_{zvs}$, so, the ZVS turn-on of S_1 and S_4 is guaranteed (cf., Figure 5.8). Therefore, the current values of

I_1 and I_2 need to satisfy the ZVS turn-on requirement by (5.16). Combining (5.9), (5.10) and (5.16) yields the requirement for the output current to ensure a ZVS turn-on of S_3, which is

$$I_1 = \frac{I_{\text{out}}}{1-d_2} - \frac{V_1[d_1(1-d_1)+d_2(d_1-d_2)]}{2Lf_s(1-d_2)} + \frac{V_1 d_2}{Lf_s} \geq \frac{V_2}{V_{\max}} I_{\text{zvs}}. \tag{5.20}$$

After simplification and replacing f_s with $f_{\max}$, one can get

$$I_{\text{out}} \geq \frac{V_1[(d_1-d_2)(1-d_1-d_2)+(d_1-1)d_2]}{2Lf_{\max}} + \frac{d_1 V_1}{V_{\max}} I_{\text{zvs}}. \tag{5.21}$$

Similarly, the requirement for the minimum output current to ensure ZVS turn-on of S_2 is

$$I_{\text{out}} \geq \frac{V_1[d_1(d_1-1)+d_2(d_1-d_2)]}{2Lf_{\max}} + \frac{(1-d_2)V_1}{V_{\max}} I_{\text{zvs}}. \tag{5.22}$$

Therefore, the required output current needs to satisfy: $I_{\text{out}} \geq \max\{(5.21),(5.22)\}$. Equations (5.21) and (5.22) lead to the same minimum I_{out} when $V_1 = V_2$ since $d_1 + d_2 = 1$, which is as expected since $I_1 = I_2$.

5

Algorithm to Determine ZVS Range

As a summary of the previous description, an algorithm is shown in Figure 5.9 to determine the minimum ZVS load for a given input and output voltage.

5.3.4 $d_{\max}$ Influence on Minimum ZVS Load and Inductor RMS Current

As it will be seen later, there is a trade-off between the selection of $d_{\max}$ in terms of achieving a wider ZVS range and lower inductor rms current. Figure 5.10 shows the minimum ZVS load at 400 V output under different $d_{\max}$ and k based on the algorithm given in Figure 5.9. It can be seen from Figure 5.10 that a larger $d_{\max}$ results in a narrower ZVS range, in order to achieve a wider ZVS range, a smaller $d_{\max}$ is preferred, however, it can result in a larger inductor rms current, which corresponds to a higher conduction loss. Figure 5.11(a) shows the inductor rms current at different values of $d_{\max}$ with $P_o = 2.5$ kW and $V_2 = 400$ V. Figure 5.11(b) shows the normalized value taking the inductor rms current at $d_{\max} = 0.9$ as a reference.

According to the previous discussion, in can be found that there is a trade-off between achieving a wider ZVS range and a smaller inductor rms current. For the design of the FSBB converter in this chapter, $d_{\max}$ is selected as 0.8 and inductance as 200 μH.

5.3.5 Selection of Input and Output Capacitors

In this section, the selection of the input and output capacitors will be discussed based on the voltage ripple, which is rarely discussed for FSBB converter under ZVS modulation schemes. In order to facilitate the analysis, the voltage ripple is considered without frequency restriction, which is a reasonable assumption since the larger voltage ripple occurs at rated power condition when the switching frequency is typically within the predefined range.

For both input and output capacitors, there are four different cases to be analyzed, which are given in detail as follows.

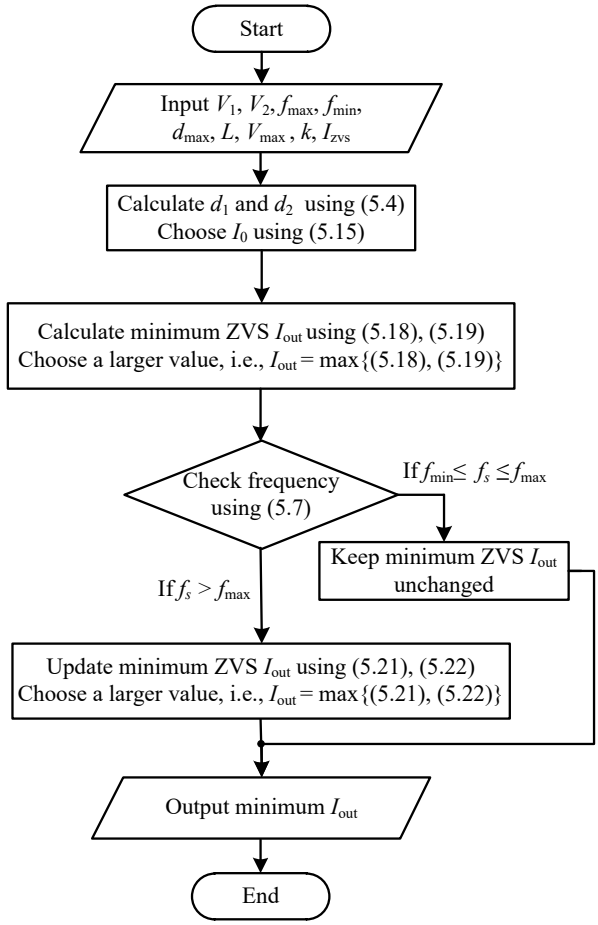


Figure 5.9: Algorithm to determine minimum ZVS load.

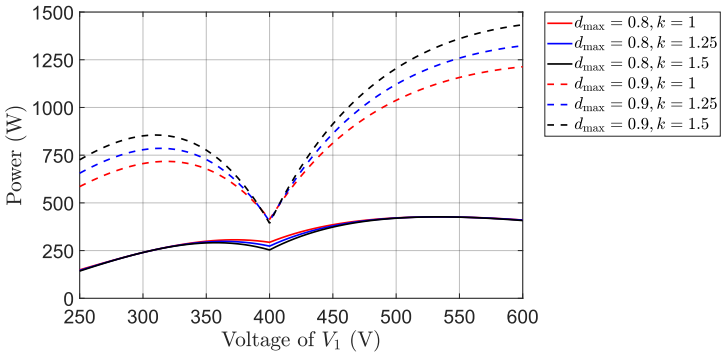
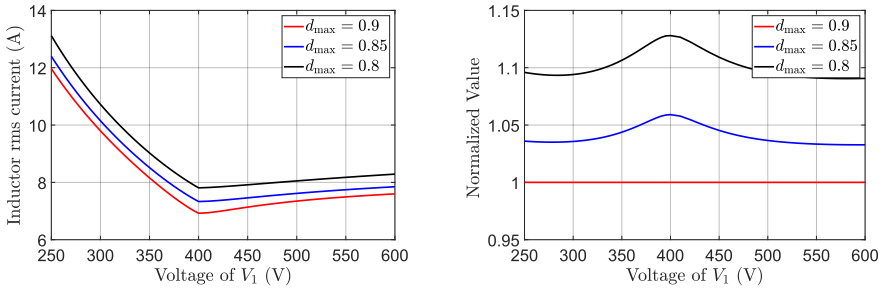


Figure 5.10: Minimum ZVS power in terms of different d_{max} and k, $I_{zvs} = 2$ A, $f_{max} = 160$ kHz, $V_2 = 400$ V, $L = 200$ μH.



(a) (b)

Figure 5.11: Inductor rms current in terms of different d_{max} (without frequency restriction) values, $P_o = 2.5$ kW, $V_2 = 400$ V, $I_0 = -2.5$ A. (a) Rms current value. (b) Normalized value with reference to the rms current at $d_{max} = 0.9$.

Peak-to-Peak Voltage Ripple on Input Capacitor

In step-down mode when $V_1 \geq V_2$, the current waveforms of i_{S_1} and $i_{C_{in}}$ (cf., Figure 5.1 and Figure 5.3) can be divided into two cases depending on the numerical relationship between I_{in} and I_1, where I_{in} is the average input current. Figure 5.12 shows the corresponding waveforms with $I_{in} \leq I_1$ and $I_{in} \geq I_1$.

The peak-to-peak value of the capacitor voltage ripple can be calculated from the charge accumulated in the shaded area. For the case of Figure 5.12(a), the voltage ripple is

$$\Delta V_{pp\_C_{in}\_buck1} = \frac{1}{C_{in}}\left[\frac{(I_{in} - I_0)(t_1 - t_0)}{2} + I_{in}(1 - d_1)T_s\right], \tag{5.23}$$

where $t_1 - t_0 = \dfrac{I_{in} - I_0}{I_1 - I_0} d_2 T_s$, $I_{in} = \dfrac{P_o}{V_1}$ with P_o being the power processed by the converter. The values of the variables can be calculated from (5.7) and (5.8).

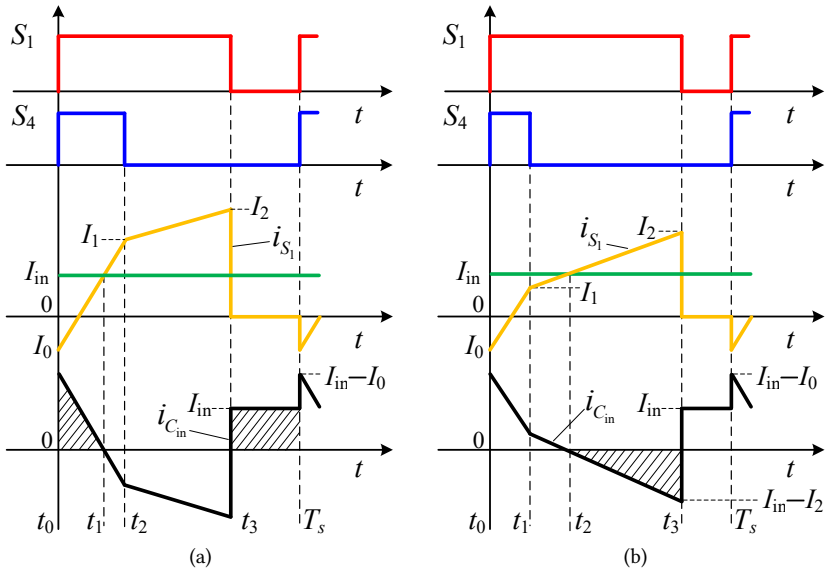


Figure 5.12: Current waveforms of i_{S_1} and $i_{C_{in}}$ in step-down mode when $V_1 \geq V_2$. (a) $I_{in} \leq I_1$. (b) $I_{in} \geq I_1$.

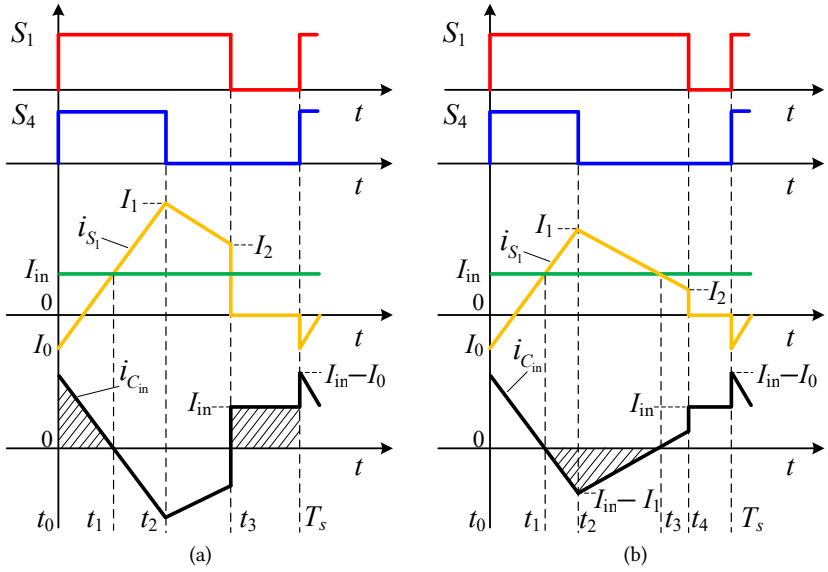


Figure 5.13: Current waveforms of i_{S_1} and $i_{C_{in}}$ in step-up mode when $V_1 \leq V_2$. (a) $I_{in} \leq I_2$. (b) $I_{in} \geq I_2$.

For the case of Figure 5.12(b), the peak-to-peak voltage ripple is

$$\Delta V_{pp\_C_{in}\_buck2} = \frac{(I_2 - I_{in})(t_3 - t_2)}{2C_{in}}, \tag{5.24}$$

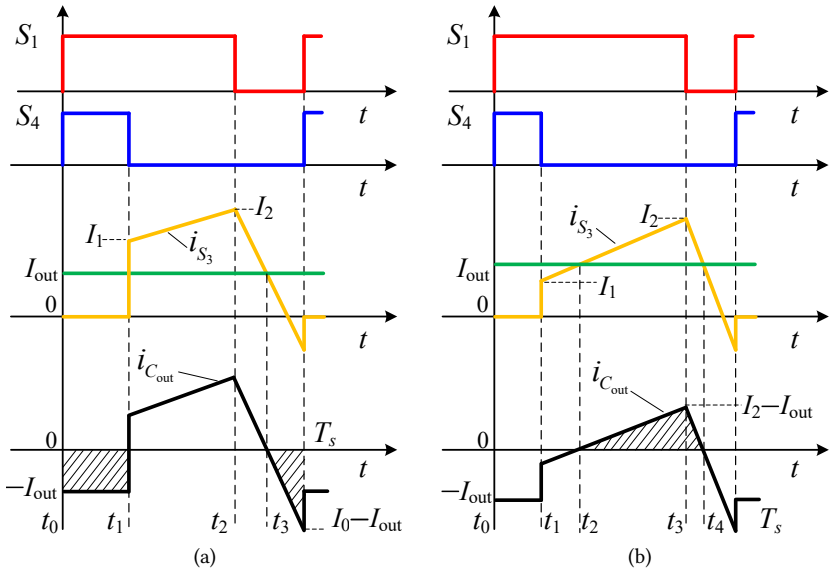


Figure 5.14: Current waveforms of i_{S_3} and $i_{C_{out}}$ in step-down mode when $V_1 \geq V_2$. (a) $I_{out} \leq I_1$. (b) $I_{out} \geq I_1$.

where $t_3 - t_2 = \dfrac{I_2 - I_{in}}{I_2 - I_1}(d_1 - d_2)T_s$. It should be noted that (5.24) also holds when $I_1 \leq 0$.

In step-up mode when $V_1 \leq V_2$, the current waveforms of i_{S_1} and $i_{C_{in}}$ can also be divided into two cases depending on the numerical relationship between I_{in} and I_2. Figure 5.13 shows the corresponding waveforms with $I_{in} \leq I_2$ and $I_{in} \geq I_2$.

For the case of Figure 5.13(a), the peak-to-peak voltage ripple expression is the same as (5.23).

For the case of Figure 5.13(b), the peak-to-peak voltage ripple is

$$\Delta V_{pp\_C_{in}\_boost} = \frac{(I_1 - I_{in})(t_3 - t_1)}{2C_{in}}, \tag{5.25}$$

where $t_3 - t_1 = \dfrac{I_1 - I_{in}}{I_1 - I_0} d_2 T_s + \dfrac{I_1 - I_{in}}{I_1 - I_2}(d_1 - d_2)T_s$. It should be noted that (5.25) also holds when $I_2 \leq 0$.

Peak-to-Peak Voltage Ripple On Output Capacitor

The analysis of peak-to-peak voltage ripple on the output capacitor will be similar to that on the input capacitor, following the same analytical steps.

In step-down mode when $V_1 \geq V_2$, the current waveforms of i_{S_3} and $i_{C_{out}}$ (cf., Figure 5.1 and Figure 5.3) can be divided into two cases depending on the numerical relationship between I_{out} and I_1. Figure 5.14 shows the corresponding waveforms with $I_{out} \leq I_1$ and $I_{out} \geq I_1$.

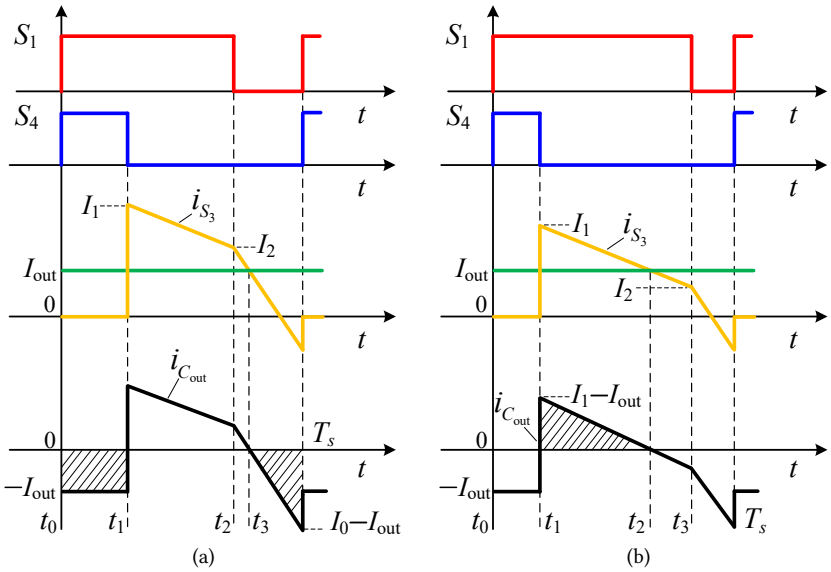


Figure 5.15: Current waveforms of i_{S_3} and $i_{C_{\text{out}}}$ in step-up mode when $V_1 \le V_2$. (a) $I_{\text{out}} \le I_2$. (b) $I_{\text{out}} \ge I_2$.

For the case of Figure 5.14(a), the peak-to-peak voltage ripple is

$$\Delta V_{\text{pp\_}C_{\text{out}}\text{\_buck1}} = \frac{1}{C_{\text{out}}}\left[I_{\text{out}} d_2 T_s + \frac{(I_{\text{out}} - I_0)(T_s - t_3)}{2}\right], \tag{5.26}$$

where $T_s - t_3 = \dfrac{I_{\text{out}} - I_0}{I_2 - I_0}(1 - d_1)T_s$.

For the case of Figure 5.14(b), the peak-to-peak voltage ripple is

$$\Delta V_{\text{pp\_}C_{\text{out}}\text{\_buck2}} = \frac{(I_2 - I_{\text{out}})(t_4 - t_2)}{2C_{\text{out}}}, \tag{5.27}$$

where $t_4 - t_2 = \dfrac{I_2 - I_{\text{out}}}{I_2 - I_1}(d_1 - d_2)T_s + \dfrac{I_2 - I_{\text{out}}}{I_2 - I_0}(1 - d_1)T_s$. It should be noted that (5.27) also holds when $I_1 \le 0$.

In step-up mode when $V_1 \le V_2$, the current waveforms of i_{S_3} and $i_{C_{\text{out}}}$ can also be divided into two cases depending on the numerical relationship between I_{out} and I_2. Figure 5.15 shows the corresponding waveforms with $I_{\text{out}} \ge I_2$ and $I_{\text{out}} \le I_2$.

For the case of Figure 5.15(a), the peak-to-peak voltage ripple expression is the same as (5.26).

For the case of Figure 5.15(b), the peak-to-peak voltage ripple expression is

$$\Delta V_{\text{pp\_}C_{\text{out}}\text{\_boost}} = \frac{(I_1 - I_{\text{out}})(t_2 - t_1)}{2C_{\text{out}}}, \tag{5.28}$$

where $t_2 - t_1 = \dfrac{I_1 - I_{\text{out}}}{I_1 - I_2}(d_1 - d_2)T_s$. It should be noted that (5.28) also holds when $I_2 \le 0$.

Finally, by simplifying (5.23) to (5.28) according to (5.29) derived from (5.5), a more compact form of the peak-to-peak voltage ripple of the input and output capacitor can be obtained, which is expressed as follows

$$\begin{cases} \dfrac{d_2 T_s}{I_1 - I_0} = \dfrac{L}{V_1} \\ \dfrac{(d_1 - d_2) T_s}{I_2 - I_1} = \dfrac{L}{V_1 - V_2} \\ \dfrac{(1 - d_1) T_s}{I_2 - I_0} = \dfrac{L}{V_2}. \end{cases} \tag{5.29}$$

$$\Delta V_{\text{pp\_C}_{\text{in}}} = \begin{cases} \dfrac{L}{C_{\text{in}}}\left[\dfrac{(I_{\text{in}} - I_0)^2}{2V_1} + \dfrac{I_{\text{in}}(I_2 - I_0)}{V_2}\right], \text{ [Fig. 5.12(a)}, V_1 \geq V_2,\ I_{\text{in}} \leq I_1] \\ \dfrac{L}{2C_{\text{in}}} \cdot \dfrac{(I_2 - I_{\text{in}})^2}{V_1 - V_2}, \text{ [Fig. 5.12(b)}, V_1 \geq V_2,\ I_{\text{in}} \geq I_1] \\ \dfrac{L}{C_{\text{in}}}\left[\dfrac{(I_{\text{in}} - I_0)^2}{2V_1} + \dfrac{I_{\text{in}}(I_2 - I_0)}{V_2}\right], \text{ [Fig. 5.13(a)}, V_1 \leq V_2,\ I_{\text{in}} \leq I_2] \\ \dfrac{L}{2C_{\text{in}}} \cdot \dfrac{(I_1 - I_{\text{in}})^2 V_2}{V_1(V_2 - V_1)}, \text{ [Fig. 5.13(b)}, V_1 \leq V_2,\ I_{\text{in}} \geq I_2] \end{cases}. \tag{5.30}$$

$$\Delta V_{\text{pp\_C}_{\text{out}}} = \begin{cases} \dfrac{L}{C_{\text{out}}}\left[\dfrac{(I_{\text{out}} - I_0)^2}{2V_2} + \dfrac{I_{\text{out}}(I_1 - I_0)}{V_1}\right], \text{ [Fig. 5.14(a)}, V_1 \geq V_2,\ I_{\text{out}} \leq I_1] \\ \dfrac{L}{2C_{\text{out}}} \cdot \dfrac{(I_2 - I_{\text{out}})^2 V_1}{V_2(V_1 - V_2)}, \text{ [Fig. 5.14(b)}, V_1 \geq V_2,\ I_{\text{out}} \geq I_1] \\ \dfrac{L}{C_{\text{out}}}\left[\dfrac{(I_{\text{out}} - I_0)^2}{2V_2} + \dfrac{I_{\text{out}}(I_1 - I_0)}{V_1}\right], \text{ [Fig. 5.15(a)}, V_1 \leq V_2,\ I_{\text{out}} \leq I_2] \\ \dfrac{L}{2C_{\text{out}}} \cdot \dfrac{(I_1 - I_{\text{out}})^2}{V_2 - V_1}, \text{ [Fig. 5.15(b)}, V_1 \leq V_2,\ I_{\text{out}} \geq I_2] \end{cases}. \tag{5.31}$$

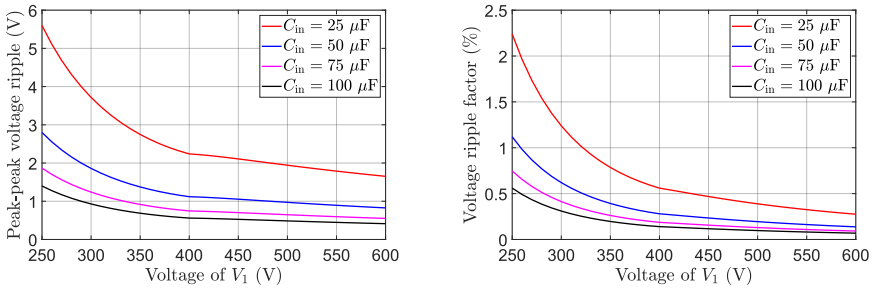
Numerical Example of Capacitor Voltage Ripple

Based on the derived formulas on the voltage ripple calculation, Figure 5.16 and 5.17 show the peak-to-peak voltage ripple and its ripple factor of the input and output capacitor voltages with different capacitance values when $P_o = 2.5$ kW, respectively.

Based on the results from Figures 5.16 and 5.17, the input and output capacitor values can be selected accordingly based on the voltage ripple requirement. In this chapter, both the input and output capacitor values are selected as 75 μF such that the peak-to-peak voltage ripple factor is less than 1%.

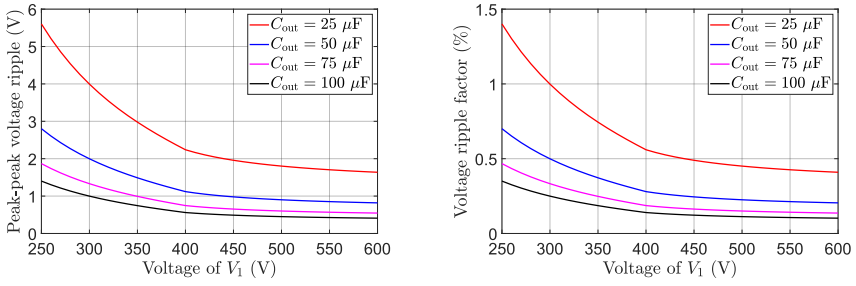
5.3.6 Benchmark with Different ZVS Modulation Schemes on Inductor RMS Current

Different advanced ZVS modulation schemes are compared in terms of inductor rms current as shown in Figure 5.18 at full load of 2.5 kW. For the methods in [63], [89] and [64], the



(a) (b)

Figure 5.16: Peak-to-peak input capacitor voltage ripple and its ripple factor, $P_o = 2.5$ kW, $L = 200\ \mu$H, $V_2 = 400$ V, $d_{max} = 0.8$, and $I_0 = -2.5$ A. (a) Input capacitor peak-to-peak voltage ripple. (b) Voltage ripple factor, defined as $\frac{\Delta V_{pp\_C_{in}}}{V_1}$.

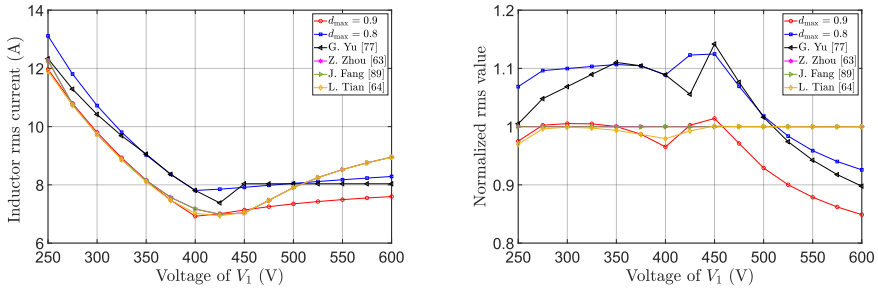


(a) (b)

Figure 5.17: Peak-to-peak output capacitor voltage ripple and its ripple factor, $P_o = 2.5$ kW, $L = 200\ \mu$H, $V_2 = 400$ V, $d_{max} = 0.8$, and $I_0 = -2.5$ A. (a) Output capacitor peak-to-peak voltage ripple. (b) Voltage ripple factor, defined as $\frac{\Delta V_{pp\_C_{out}}}{V_2}$.

rms value of the inductor current is calculated with an inductance of 200 μH. The switching frequency is selected at 25 kHz for [63] and [89] since it is a constant frequency modulation. For the method in [64], a combination of fixed- and variable-frequency control is adopted, so, the frequency is between 22.1 kHz and 25 kHz. For the method in [77], since variable-frequency modulation is adopted, so the inductor rms current is independent of inductance. It should be noted that for the method proposed in [89], in order to have a full input voltage range rated load ZVS operation based on selected parameters, both the PCRM and PDCM have to be adopted, which is a bit different from the description in [89], where PDCM is adopted for low power conditions. Herein, the specific switching timing calculation for PDCM is based on [64], that is, let the corner current values of I_1 or I_2 (cf., Figure 5.2) equal to the minimum required ZVS current.

According to the description in Section 5.3, the inductor rms current of the proposed



(a) (b)

Figure 5.18: Rms value of inductor current with different ZVS modulation methods. $P_o = 2.5$ kW, $V_2 = 400$ V, absolute value of switching ZVS current is 2.5 A. (a) Inductor rms current. (b) Normalized value with reference to the rms current from [63].

5

method depends on the value of $d_{\max}$, as it can be seen from Figure 5.18(b), when $d_{\max} = 0.9$, the inductor rms current is overall smaller than the values from other state-of-the-art methods, which is preferred if the converter is always operated near or slightly lower than the rated load. However, in order to achieve a wider operational ZVS range even at light load, in this chapter, $d_{\max}$ is selected as 0.8 where the inductor current rms value is slightly larger.

5.4 Converter Losses Estimation

In this section, the losses breakdown of each component will be analyzed in detail, i.e., the losses from SiC MOSFETs, inductor, input and output capacitors.

5.4.1 MOSFET Losses Estimation

As for switching losses, since the turn-off losses of MOSFETs are typically low due to the voltage rise delay effect from the parasitic output capacitance C_{oss} [57], in addition, ZVS turn-on is also achieved, therefore, the switching loss is ignored.

As for the conduction losses, the rms values of the current through each MOSFET are required, which can be expressed as follows

$$I_{\text{rms\_}S_1} = \sqrt{I_{\text{rms1}}^2 + I_{\text{rms2}}^2},\ I_{\text{rms\_}S_2} = I_{\text{rms3}}, \tag{5.32}$$

$$I_{\text{rms\_}S_3} = \sqrt{I_{\text{rms2}}^2 + I_{\text{rms3}}^2},\ I_{\text{rms\_}S_4} = I_{\text{rms1}}, \tag{5.33}$$

where I_{rms1} to I_{rms3} are given by (5.12). In fact, based on (5.11), (5.32) and (5.33), (5.34) could also be derived

$$I_{\text{rms\_}L}^2 = I_{\text{rms\_}S_1}^2 + I_{\text{rms\_}S_2}^2 = I_{\text{rms\_}S_3}^2 + I_{\text{rms\_}S_4}^2. \tag{5.34}$$

The conduction losses of the MOSFETs can then be calculated as

$$P_{MOS} = (I_{\text{rms\_}S_1}^2 + I_{\text{rms\_}S_2}^2 + I_{\text{rms\_}S_3}^2 + I_{\text{rms\_}S_4}^2)R_{\text{ds(on)}}, \tag{5.35}$$

where $R_{\text{ds(on)}}$ is the equivalent channel resistance of a single switch.

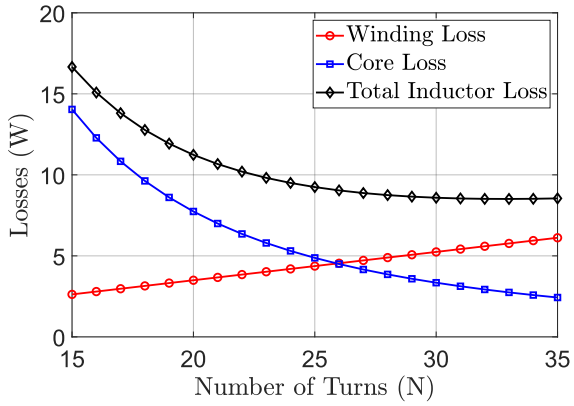


Figure 5.19: Estimated inductor core and winding losses, $V_1 = 250$ V, $V_2 = 400$ V, $P_o = 2.5$ kW, $d_{\max} = 0.8$, $L = 200$ μH, $I_0 = -2.5$ A.

5.4.2 Inductor Losses Estimation

The inductor losses consist of winding loss and core loss. For the convenience of calculation, only the dc resistance is considered due to the adoption of 600×0.071 mm Litz wire. The winding loss can be expressed as

$$P_{\text{winding}} = I_{\text{rms\_}L}^2 R_L, \tag{5.36}$$

where R_L is the winding resistance.

As for the core loss, due to the nonsinusoidal inductor current waveform, the improved generalized Steinmetz equation (iGSE) is adopted to achieve a more accurate core loss estimation mainly for MnZn ferrite materials [83]. The iGSE is expressed as

$$P_{\text{core\_iGSE}} = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} V_e dt, \tag{5.37}$$

$$k_i = \frac{k}{2^{\beta+1} \pi^{\alpha-1} (0.2761 + \frac{1.7061}{\alpha+1.354})}, \tag{5.38}$$

where k, α and β are the Steinmetz coefficients, ΔB is the peak-to-peak flux density, V_e is the core volume and k_i can be calculated from (5.38) when α is from 0.5 to 3 [83].

Based on (5.37), the equations to calculate the core loss can be expressed by (5.44) and (5.45) derived in Appendix A. For the inductor design, PM 74/59 core with N87 material is adopted, the Steinmetz parameters are given by $k = 47.69$, $\alpha = 1.11$, $\beta = 2.07$ at 25°C with SI unit [84]. For the adopted 600×0.071 mm Litz wire, the calculated dc resistance is 1.01 mΩ per turn at 25°C.

In order to optimize the inductor design, inductor losses can be estimated with different number of winding turns (or air gap equivalently) [99], [32]. Figure 5.19 shows the inductor losses with different number of turns when $V_1 = 250$ V, $V_2 = 400$ V and $P_o = 2.5$ kW. It can be seen from Figure 5.19 that as the number of turns increases, the rate of decrease in

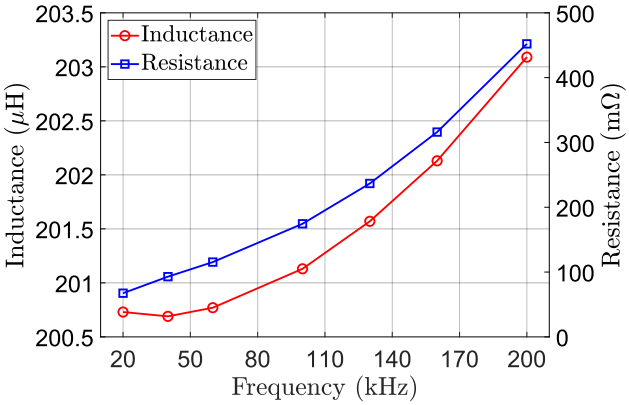


Figure 5.20: Measured inductance and series resistance in terms of frequency by E4990A impedance analyzer.

inductor total losses decreases. Considering winding convenience, the number of turns is selected as 26, and its measured dc resistance is 23.6 mΩ.

The inductance and the equivalent series resistance of the built inductor measured by Keysight E4990A impedance analyzer is shown in Figure 5.20.

5.4.3 Capacitor Losses Estimation

To determine the capacitor losses, the rms values of the current through the capacitors are required.

For the input capacitor, the rms current can be expressed as

$$I_{\text{rms\_}C_{\text{in}}} = \sqrt{I^2_{\text{rms\_}S_1} - I^2_{\text{in}}}, \tag{5.39}$$

where $I_{\text{rms\_}S_1}$ can be calculated by (5.32).

For the output capacitor, the rms current can be expressed as

$$I_{\text{rms\_}C_{\text{out}}} = \sqrt{I^2_{\text{rms\_}S_3} - I^2_{\text{out}}}, \tag{5.40}$$

where $I_{\text{rms\_}S_3}$ can be calculated by (5.33). The derivation of (5.39) and (5.40) is given in Appendix B. So, the capacitor losses are

$$P_{C_{\text{in}}} = I^2_{\text{rms\_}C_{\text{in}}} R_{ESR\_C_{\text{in}}}, \quad P_{C_{\text{out}}} = I^2_{\text{rms\_}C_{\text{out}}} R_{ESR\_C_{\text{out}}}, \tag{5.41}$$

where $R_{ESR\_C_{\text{in}}}$ and $R_{ESR\_C_{\text{out}}}$ are the equivalent series resistances of the input and output capacitors.

5.4.4 Estimated Losses and Efficiency

The key parameters of the prototype are listed in Table 5.1. Figure 5.21 shows the estimated losses and efficiency of the prototype operating at different input voltages under rated power of 2.5 kW.

Table 5.1: Key parameters of the prototype

Input Voltage	250 – 600 V
Output Voltage	400 V
Power	250 – 2500 W
Switch S_1 to S_4	C3M0075120J (2 in Parallel)
Input Capacitor	MKP1848C, 800 VDC, 25 μF ×3
Output Capacitor	MKP1848C, 800 VDC, 25 μF ×3
Inductor	PM 74/59, 200 μH
Switching Frequency	20 – 160 kHz

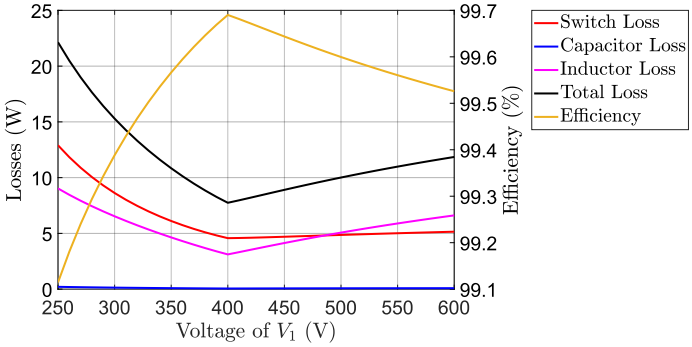


Figure 5.21: Estimated losses and efficiency with different input voltages, $V_2 = 400$ V, $P_o = 2.5$ kW, $d_{\max} = 0.8$, $L = 200$ μH, $I_0 = -2.5$ A. The losses from gate drivers are not included.

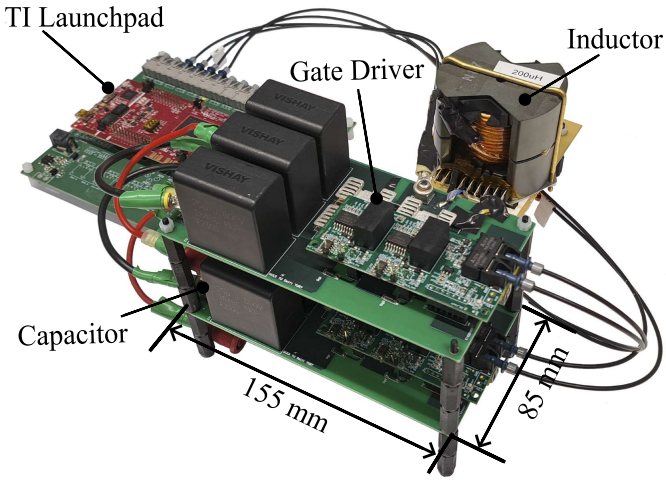


Figure 5.22: Four-switch buck+boost converter prototype.

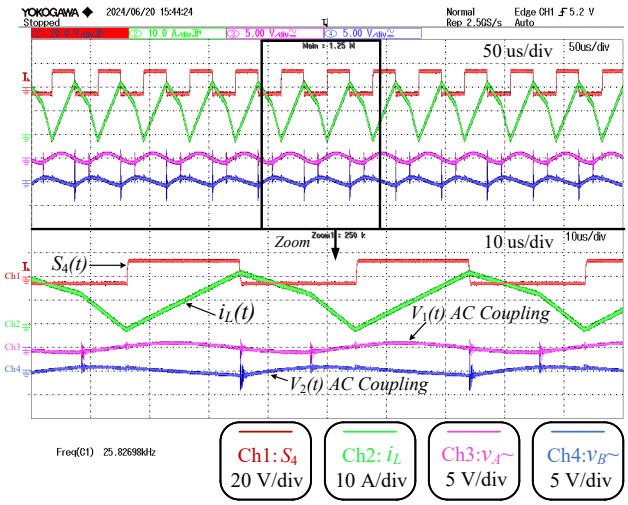


Figure 5.23: Voltage ripple under step-up operation, $V_1 = 250$ V, $V_2 = 400$ V and $P_o = 2.5$ kW. $S_4(t)$ is the gate-to-source voltage of S_4.

5.5 Experimental Verification

The experimentation was carried out through two FSBB prototypes. One set of the experimental results was done by the author based on the prototype shown in Figure 3.17, and these results can be found in [78] and also in the Appendix D of this chapter, where the operating input voltage was 300–600 V, output voltage was 400 V, operating power was 350–3300 W.

Another setup was shown in Figure 5.22 with key parameters given in Table 5.1. After commissioning of the hardware, the negative ZVS switching current was chosen as −2.5 A and the dead time defined by the two gate-to-source voltage signals crossing zero volt was around 250 ns. The efficiency was measured by Yokogawa WT500 power analyzer, the voltage was measured by Keysight N2791A differential probe, and the inductor current was measured by Keysight N2782B current probe.

5.5.1 Steady State Operation

Figure 5.23 shows the voltage ripple of the converter under step-up operation case when V_1 = 250 V, V_2 = 400 V, and P_o = 2.5 kW. As it can be seen, the measured peak-to-peak voltage ripples of the input and output sides are close to the calculated values derived in Section 5.3.5 .

Since there are step-up, step-down and unit voltage gain operations, therefore, the experimental results showing ZVS realization under several typical input voltages are given in Figure 5.24. It should be noted that the gating signal of S_4 was measured for step-up operating case since V_2 is larger than V_1 while the gating signal of S_1 was measured for step-down operating case since V_1 is larger than V_2. Taking Figure 5.24(d) as an example when the maximum input voltage of 600 V was adopted, during the circled transient, v_B

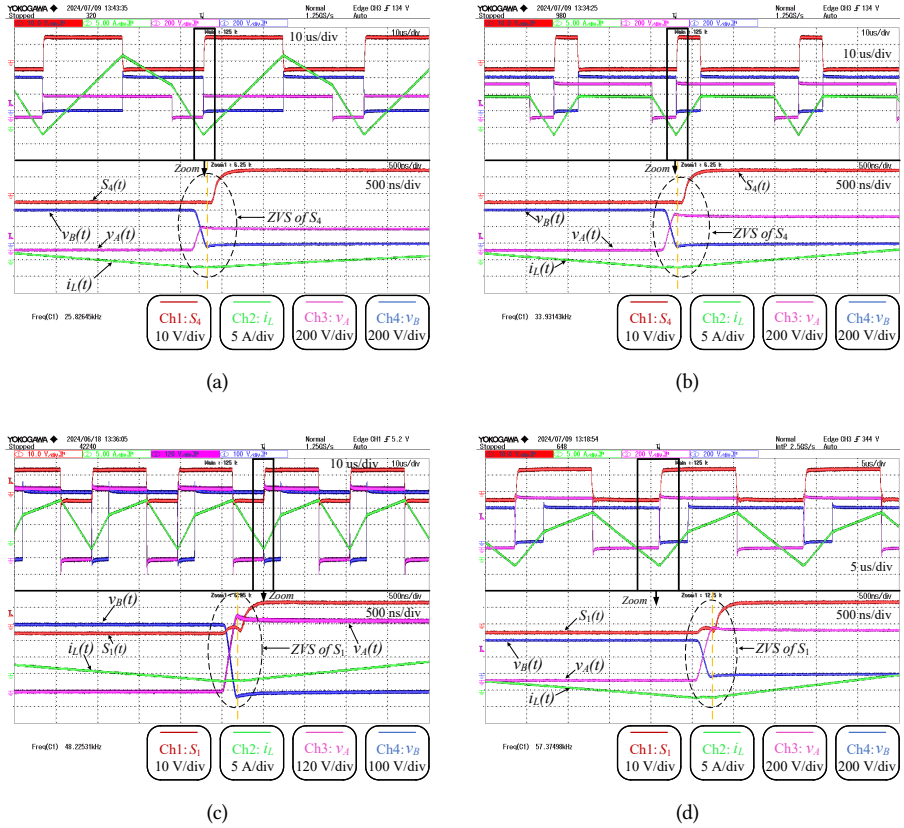


Figure 5.24: Steady-state operation waveforms when V_1= 250, 400, 500 and 600 V respectively, $V_2 = 400$ V, P_o = 2.5 kW, $d_{\max} = 0.8$, $I_0 = -2.5$ A. $S_1(t)$ and $S_4(t)$ are the gate-to-source voltages of S_1 and S_4. $v_A(t)$ and $v_B(t)$ are the voltages of points A and B relative to the dc-bus rail shown in Figure 5.1. (a) $V_1 = 250$ V. (b) $V_1 = 400$ V. (c) $V_1 = 500$ V. (d) $V_1 = 600$ V.

decreased to zero while v_A reached to the input voltage before turning on S_4 and S_1, so, it can be concluded that the ZVS turn-on of S_1 and S_4 was achieved, meanwhile, since the corner current values of I_1 and I_2 are much larger than $|I_0|$, so, it can be inferred that the ZVS turn-on for all the four switches was achieved simultaneously.

On the other hand, it is mentioned in Section 5.3.3 when the load decreases to a certain value, due to the corresponding decrease of the corner current of I_1 or I_2, ZVS turn-on could be lost. Figure 5.25 clearly shows the process of switch S_3 gradually losing full ZVS turn-on due to the gradual decrease of output power, i.e., decrease of I_1 when $V_1 = 500$ V. Besides, it also verifies the fact that the V_{ds} (V_B) voltage transition time gets smaller if I_1 becomes larger.

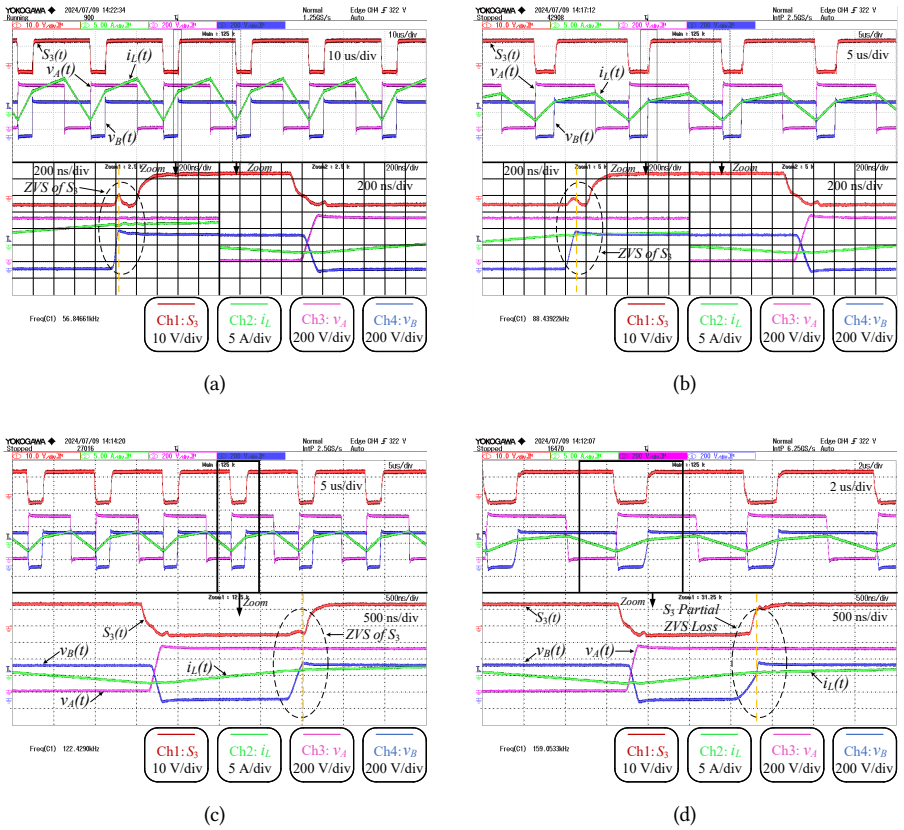


Figure 5.25: Steady-state operation waveforms showing the process of S_3 gradually losing ZVS with $V_1 = 500$ V, $V_2 = 400$ V. The output power decreases. (a) $P_o = 2$ kW. (b) $P_o = 1$ kW. (c) $P_o = 500$ W. (d) $P_o = 200$ W.

5.5.2 Efficiency and Thermal Performance

The measured efficiency performance of the FSBB converter is shown in Figure 5.26 covering a power range between 250 and 2500 W. It should be noted that the auxiliary power consumption from gate drivers is not included. As it can be seen, the efficiency maintains at a relatively high value within a wide operational range.

Figure 5.27 shows the thermal image of the converter after operating at $V_1 = 250$ V, $V_2 = 400$ V and $P_o = 2$ kW continuously for one hour measured by FLIR C5. Black electrical tape was attached to cover the 7106DG heatsink to increase its emissivity according to [88]. The converter is natural cooled and the hottest spot was around 74.2°C under this operating case.

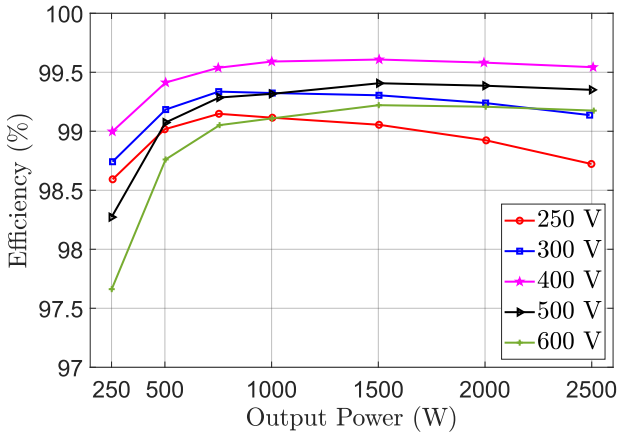


Figure 5.26: Measured efficiency at different operating input voltage and power values with V_2 = 400 V, I_0 = −2.5 A, and $d_{\max}$ = 0.8.

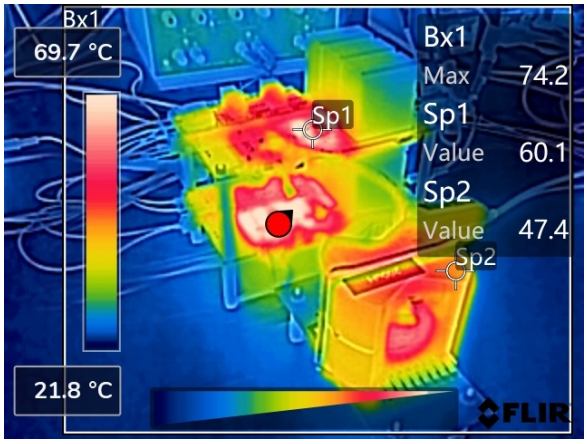


Figure 5.27: Thermal image of the converter operating continuously at V_1 = 250 V, V_2 = 400 V, f_s = 31.0 kHz and P_o = 2 kW after 60 minutes. The ambient temperature was around 22°C. The measured efficiency was 98.9%.

5.5.3 Dynamic Operation Across Unit-Voltage Gain

A simulation result implemented in PLECS circuit simulator for the transition between voltage step-up and step-down is shown in Figure 5.28 based on the control scheme from Figure 5.5. As for the experimental tests on the mode transition, the result was shown in Figure 5.36 based on the prototype shown in Figure 3.17. The detailed information is given in Appendix D.

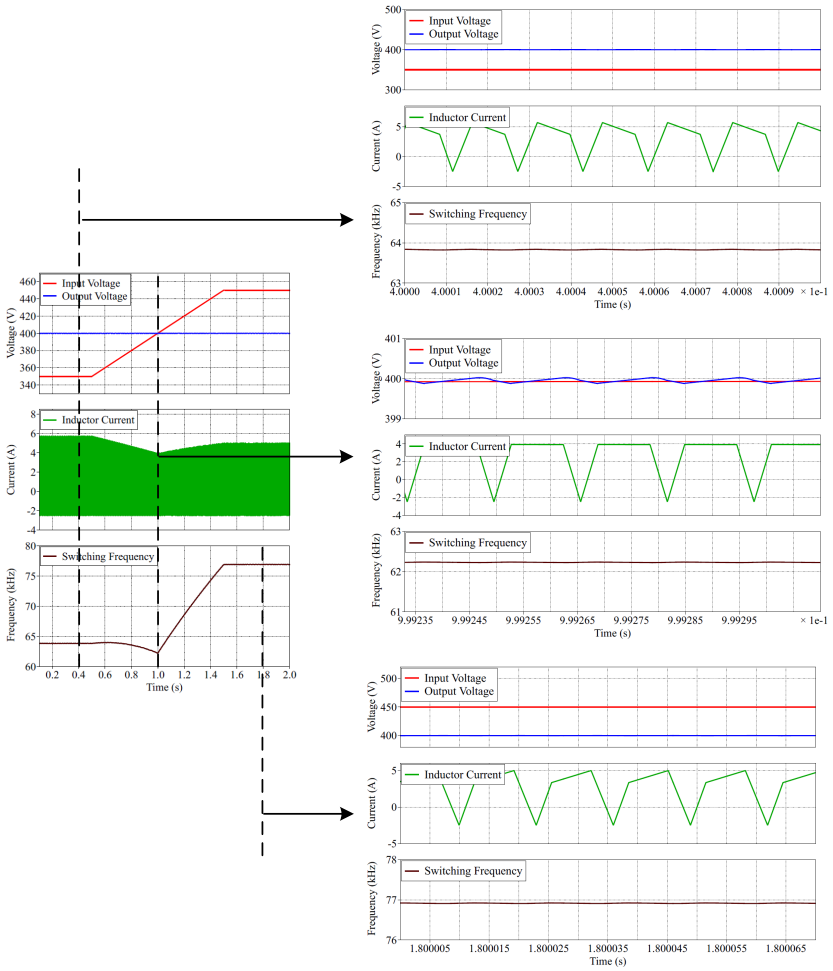


Figure 5.28: Simulation results of transition operation from PLECS. $V_1 = 350 - 450$ V, $V_2 = 400$ V, $d_{\max} = 0.8$, $P_o = 1$ kW, $I_0 = -2.5$ A, $L = 200$ μH.

5.6 Conclusion

In this chapter, the detailed design procedures, analysis and implementation of a variable-frequency ZVS modulation was presented for the four-switch buck+boost converter with three-segment inductor current mode modulation covering the whole operational range. By fixing the duty cycle of the switch in the buck-type or boost-type half-bridge during step-up or step-down cases, and adjusting the duty cycle of the switch in the other half-bridge circuit, the FSBB converter could realize a smooth transition across the unit voltage gain boundary. A simple closed-loop control method without current detection was proposed accordingly. Different from previous research focusing on modulation techniques, this chapter also provides the selection guidelines for the input and output capacitors based on a comprehensive study of the capacitor voltage ripples. Experimental testing results on a 250–600 V input, 400 V output, 2.5 kW FSBB prototype proves the correctness and effectiveness of the analysis in this chapter. The results derived in this work can be easily applied to the converter parameter design under other working conditions.

5.7 Appendix A

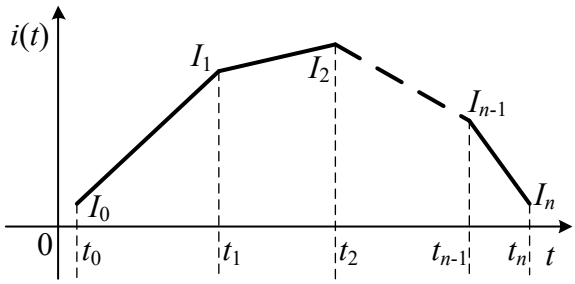


Figure 5.29: Illustration of general multi-segment inductor current waveform.

The general multi-segment inductor current iGSE core loss formula will be derived first, then, the core loss expression with three-segment inductor current will be a special case. Figure 5.29 shows a general n-segment inductor current with current values of I_0 at time t_0, I_1 at t_1, etc.

Defining $\Delta I_1 = I_1 - I_0$, $\Delta I_2 = I_2 - I_1 ... \Delta I_n = I_n - I_{n-1}$, and $t_1 - t_0 = \delta_1 T_s$, $t_2 - t_1 = \delta_2 T_s ... t_n - t_{n-1} = \delta_n T_s$ with $\sum_{j=1}^{n} \delta_j = 1$. The core loss based on iGSE can be expressed as follows

$$P_{\text{core}} = \frac{k_i V_e (\Delta B)^{\beta-\alpha}}{T_s} \times \sum_{j=1}^{n} \int_{t_{j-1}}^{t_j} |\frac{dB}{dt}|^{\alpha} dt = \frac{k_i V_e (\Delta B)^{\beta-\alpha}}{T_s} \times \sum_{j=1}^{n} [\frac{|\Delta I_j|}{\Delta I_{\text{pp}}} (\Delta B)]^{\alpha} (\delta_j T_s)^{1-\alpha}$$
$$= k_i (\Delta B)^{\beta} f_s^{\alpha} V_e \times \sum_{j=1}^{n} (\delta_j^{1-\alpha} |\frac{\Delta I_j}{\Delta I_{\text{pp}}}|^{\alpha}). \tag{5.42}$$

In (5.42), ΔI_{pp} is the peak-to-peak current value.

Based on (5.42), the specific core loss expression with three-segment inductor current mode modulation can be considered under two cases, i.e., step-down and step-up cases. In step-down case [cf., Figure 5.3(a)], since $I_2 - I_0 = \frac{V_2}{L}(1-d_1)T_s$, $I_1 - I_0 = \frac{V_1}{L} d_2 T_s$ and $I_2 - I_1 = \frac{V_1 - V_2}{L}(d_1 - d_2)T_s$, combined with (5.2), one can get

$$\frac{I_1 - I_0}{I_2 - I_0} = \frac{d_2(1-d_2)}{d_1(1-d_1)}, \quad \frac{I_2 - I_1}{I_2 - I_0} = \frac{(d_1 - d_2)(1-d_1-d_2)}{d_1(1-d_1)}. \tag{5.43}$$

Substituting (5.43) into (5.42) yields

$$P_{\text{core}} = k_i (\Delta B)^{\beta} f_s^{\alpha} [\frac{d_2(1-d_2)^{\alpha}}{d_1^{\alpha}(1-d_1)^{\alpha}} + \frac{(d_1-d_2)(1-d_1-d_2)^{\alpha}}{d_1^{\alpha}(1-d_1)^{\alpha}} + (1-d_1)^{1-\alpha}] V_e. \tag{5.44}$$

In step-up case, the core loss can also be derived similarly, which is

$$P_{\text{core}} = k_i (\Delta B)^{\beta} f_s^{\alpha} [d_2^{1-\alpha} + \frac{(d_1-d_2)(d_1+d_2-1)^{\alpha}}{d_2^{\alpha}(1-d_2)^{\alpha}} + \frac{d_1^{\alpha}(1-d_1)}{d_2^{\alpha}(1-d_2)^{\alpha}}] V_e. \tag{5.45}$$

Equations (5.44) and (5.45) lead to the same core loss expression when $V_1 = V_2$ since $d_1 + d_2 = 1$, which is as expected. Besides, when d_2 is set to 0 or d_1 is set to 1, (5.44) and (5.45) would degenerate to the core loss formulas in triangular current mode, which has the same form as in [91].

5.8 Appendix B

Herein, the capacitor rms current will be derived. According to the definition of rms value, the input capacitor rms current can be expressed as follows (cf., Figure 5.1)

$$\begin{aligned} I_{\text{rms\_}C_{\text{in}}} &= \sqrt{\frac{1}{T_s}\int_0^{T_s}[I_{\text{in}} - i_{S_1}(t)]^2 dt} = \sqrt{\frac{1}{T_s}\int_0^{T_s}[I_{\text{in}}^2 - 2I_{\text{in}} i_{S_1}(t) + i_{S_1}^2(t)]dt} \\ &= \sqrt{I_{\text{in}}^2 - \frac{1}{T_s}[2I_{\text{in}}\int_0^{T_s} i_{S_1}(t)dt - \int_0^{T_s} i_{S_1}^2(t)dt]}. \end{aligned} \tag{5.46}$$

Since $\frac{1}{T_s}\int_0^{T_s} i_{S_1}(t)dt = I_{\text{in}}$ and $\frac{1}{T_s}\int_0^{T_s} i_{S_1}^2(t)dt = I_{\text{rms\_}S_1}^2$, therefore, (5.46) can be simplified to

$$I_{\text{rms\_}C_{\text{in}}} = \sqrt{I_{\text{rms\_}S_1}^2 - I_{\text{in}}^2}. \tag{5.47}$$

For the output capacitor rms current, its derivation is similar, therefore, it is omitted here.

5.9 Appendix C

Compared with the ZVS power range determination described in Section 5.3, calculating the ZVS range based on enumeration is more intuitive, but the trade-off is that the closed-form expressions are not given. The corresponding enumeration algorithm is briefly shown in Figure 5.30. Based on the algorithm in Figure 5.30, Figure 5.31 and 5.32 show the ZVS and non-ZVS range at 400 V output under different $d_{\max}$ and k. In Figure 5.30, equation (5.48) is expressed as follows:

$$I_0 < 0 \text{ and } |I_0| \geq \frac{\max(V_1, V_2)}{V_{\max}} \cdot I_{\text{zvs}}. \tag{5.48}$$

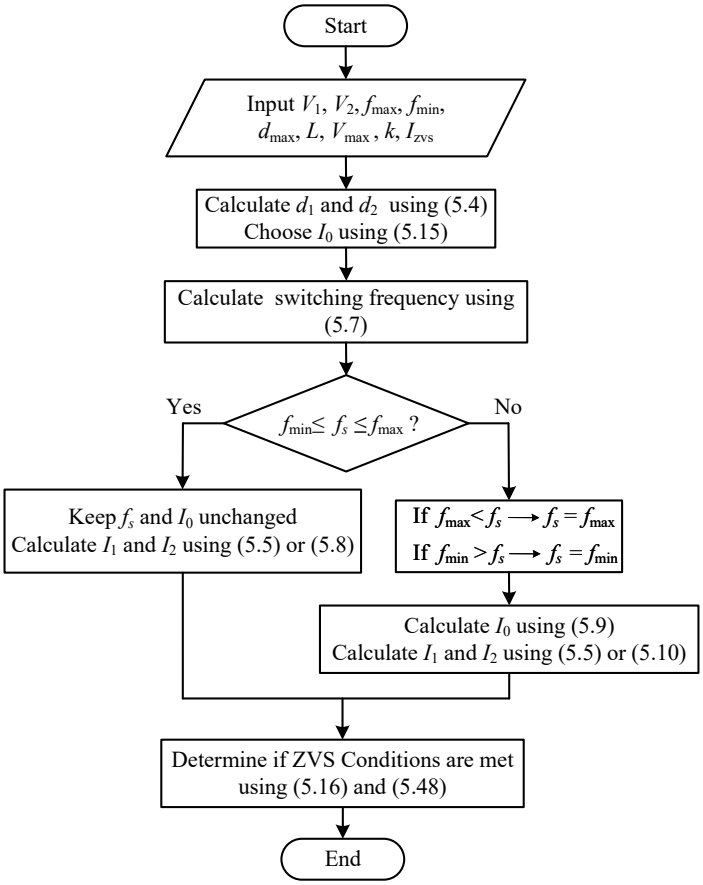


Figure 5.30: ZVS range determination using brute force.

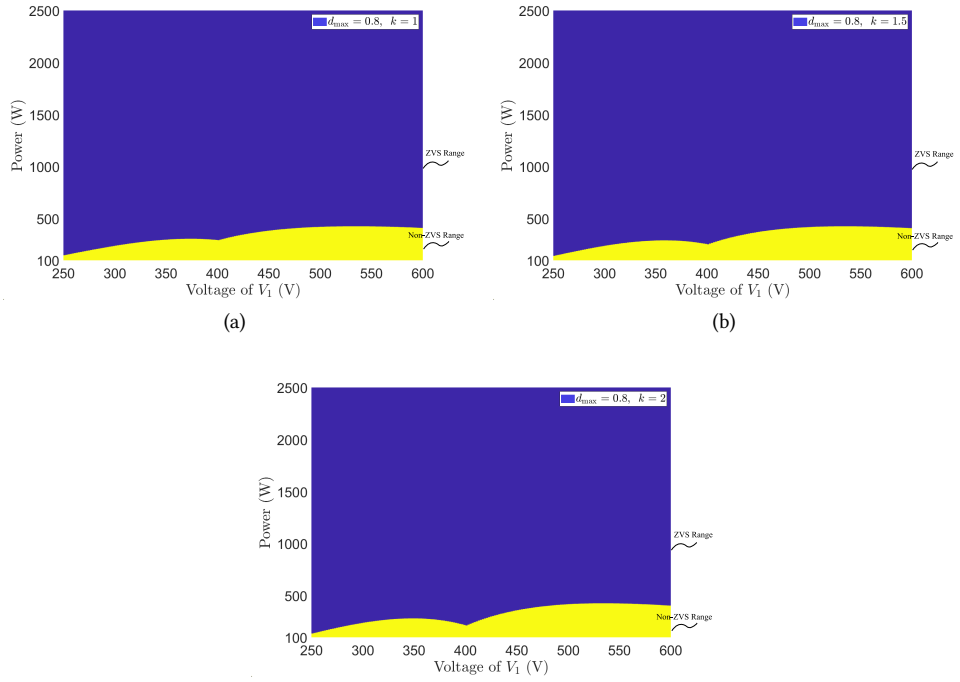


Figure 5.31: ZVS range in terms of different k, $d_{max} = 0.8$, $I_{zvs} = 2$ A, $f_{max} = 160$ kHz, $f_{min} = 20$ kHz, $V_2 = 400$ V, $L = 200$ μH. (a) $k = 1$. (b) $k = 1.5$. (c) $k = 2$.

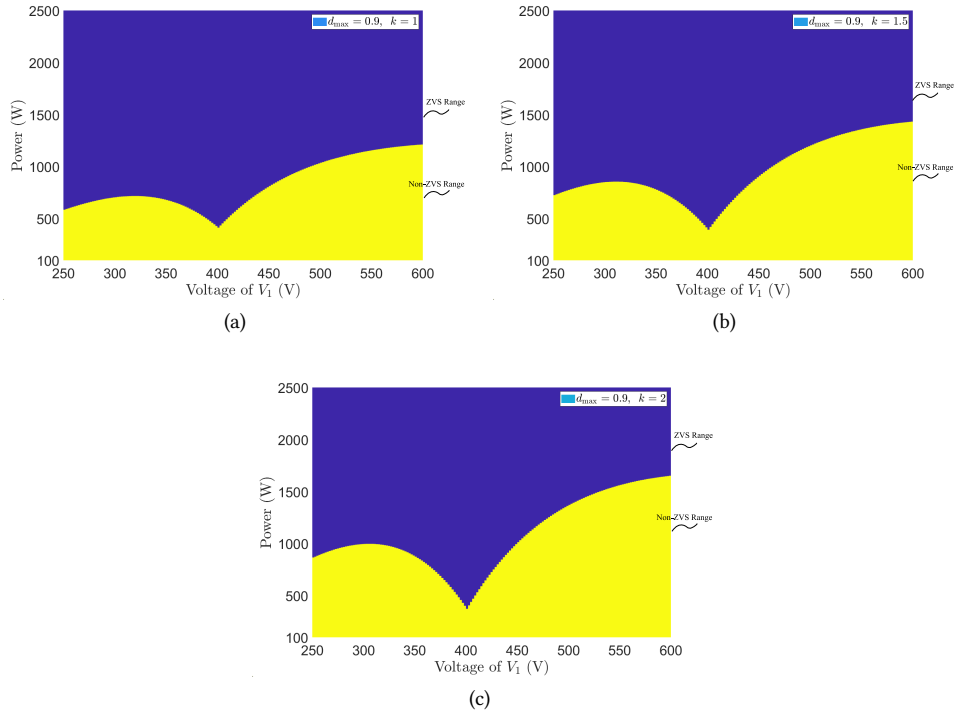


Figure 5.32: ZVS range in terms of different k, $d_{\max} = 0.9$, $I_{zvs} = 2$ A, $f_{\max} = 160$ kHz, $f_{\min} = 20$ kHz, $V_2 = 400$ V, $L = 200$ μH. (a) $k = 1$. (b) $k = 1.5$. (c) $k = 2$.

Table 5.2: Inductance and equivalent resistance of the inductor

Frequency (kHz)	20	60	100	140	160
L (μH)	155.51	155.53	155.48	155.53	155.70
R_s (mΩ)	49.5	99.5	144.7	205.9	283.0

5.10 Appendix D

In this section, some measurement results will be given based on the prototype shown in Figure 3.17 from Chapter 3, and the schematic is shown in Figure 5.1. Each single switch was composed of three parallel-connected silicon carbide (SiC) MOSFETs of G3R75MT12J from GeneSiC semiconductor. The inductor was made with N87 material on PM 74/59 core. The inductance and equivalent resistance is given in Table 5.2, which was measured by Agilent 4294A precision impedance analyzer. During experiments, the inductance was selected as 155.5 μH. Herein, I_0 is chosen as -2 A and the dead time is 300 ns.

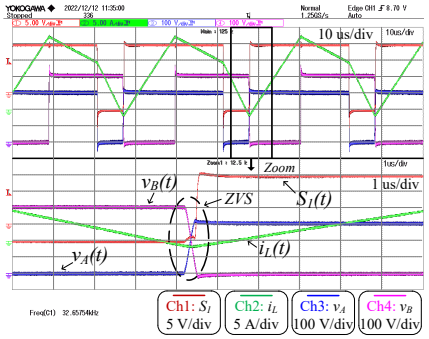
5.10.1 Steady State Operation

The experimental oscilloscope waveforms are given in Figure 5.33 when the input voltage is 300 V, 400 V and 600 V respectively at 3.3 kW power level. The value of $d_{\max}$ is chosen as 0.8.

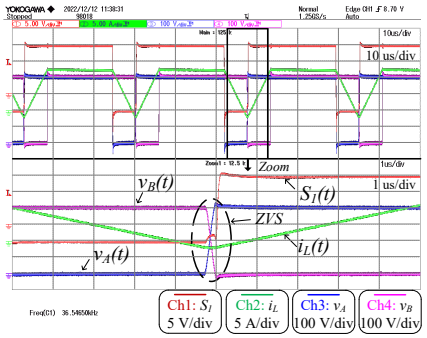
Figure 5.34 shows the efficiency measured by Yokogawa WT500 power analyzer at 3.3 kW when input voltage is 400 V and 600 V respectively. Efficiency measured at different operating points is shown in Figure 5.35, which, covers a power range between 350 and 3300 W, as it can be seen, the efficiency remains at a relatively high value over a wide operational range.

5.10.2 Transition Operation under Constant Power

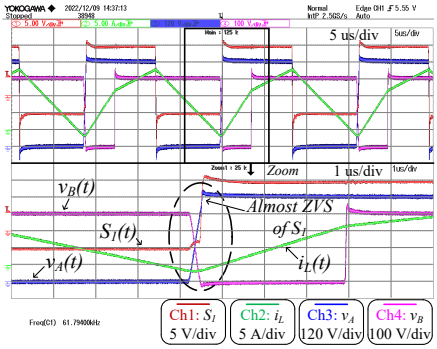
The transient experiment was carried out under a constant power of 2 kW, the input voltage first decreased from 425 V to 375 V, after another period of 1 s, it rose from 375 V to 425 V to cover both transition cases from voltage step-down to step-up and voltage step-up to step-down. The result is given in Figure 5.36.



(a)



(b)



(c)

Figure 5.33: Measured waveforms at $V_1 = 300$, 400 and 600 V, $P_o = 3.3$ kW, $d_{\max} = 0.8$, $V_2 = 400$ V. The switching frequency is calculated based on (5.7). $S_1(t)$ is the gate-source voltage of S_1, $i_L(t)$ is the inductor current, $v_A(t)$ and $v_B(t)$ are the voltage potentials of terminals A and B relative to the bottom-side dc-bus rail illustrated in Figure 5.1. (a) $V_1 = 300$ V. (b) $V_1 = 400$ V. (c) $V_1 = 600$ V.

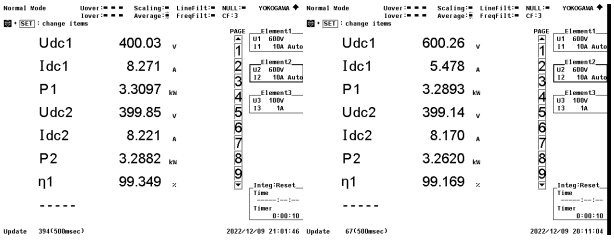


Figure 5.34: Measured efficiency from Yokogawa WT500 power analyzer. Udc1, Idc1 and P1 are the DC bus voltage, current and delivered active power values respectively from input side while Udc2, Idc2 and P2 are the DC bus voltage, current and delivered active power values respectively from the output side. The prototype efficiency is defined as $\eta 1 = \frac{\text{P2}}{\text{P1}}$.

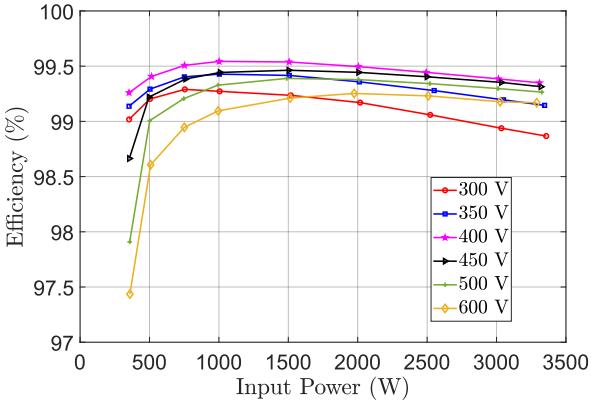


Figure 5.35: Measured efficiency at different operating input voltage and power values with $V_2 = 400$ V and $d_{\max} = 0.8$.

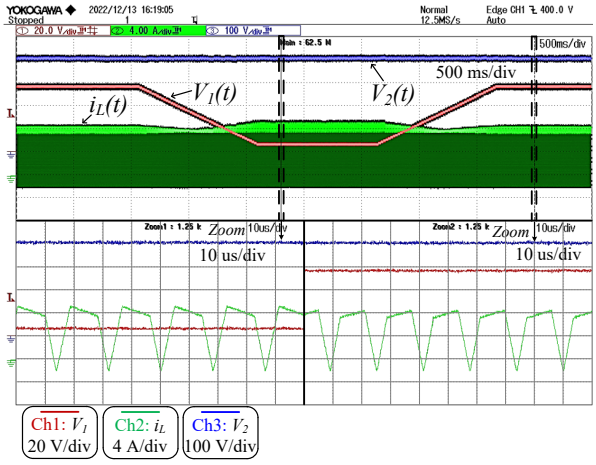


Figure 5.36: Experiments of transition operation. V_1=425−375−425 V, $V_2 = 400$ V, $d_{\max} = 0.8$, $P_o = 2$ kW, $I_0 = -2$ A.

6

Improved Peak Voltage Calculation Method for Compensation Components in S-S and LCC-S WPT Systems

This chapter studies the compensation component (including coils) stresses in two commonly adopted compensation topologies, namely S-S and LCC-S compensations. Accurately calculating electrical stress is a key step in ensuring the safe and reliable operation of electrical equipment, especially for resonant circuits in wireless charging under high-power conditions. Due to the peak voltage calculation inaccuracy for certain components based on conventional first harmonic approximation analysis, an improved peak voltage calculation method is introduced in closed form, which is proved to be more accurate by both simulation and experimental results. [1]

[1]This chapter is based on:

G. Yu, P. Ye, F. Grazian, J. Dong, T. B. Soeiro and P. Bauer, "An Improved Peak Voltage Calculation Method for Compensation Components in S-S and LCC-S Compensated Wireless Power Transfer Systems," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-9, doi: 10.23919/EPE23ECCEEurope58414.2023.10264576.

6.1 Introduction

Compensation network plays an indispensable role in wireless power transfer (WPT) systems, which is used to improve power transfer efficiency. Due to the resonance characteristics, the compensation components may be subject to high voltage and current stresses, which needs to be considered throughout the system design. Series-series (S-S) and LCC-S compensation topologies featuring constant current (CC) and constant voltage (CV) output at resonant operating frequency are two widely used compensations since the component values are independent of the coupling and load conditions [9], [100].

In [7] and [101] , the compensation component stresses were studied between S-S and LCC-LCC compensations at 7.7 kW and 20 kW, respectively. A comprehensive comparison of four resonant topologies, i.e., S-S, S-LCC, LCC-S and LCC-LCC, was studied in terms of efficiency and component stresses in [102]. A comparative study focusing on efficiency and circuit parameter sensitivity between S-S and LCC-S compensations was given in [100]. However, few literature has been found to provide accurate peak voltage calculation methods for the compensation components. Peak voltage directly affects the insulation reliability of the circuit system, which could be even worse in a higher frequency operating condition [103], [104], and therefore, to determine it accurately is the first step to design a system with reliable electrical insulation.

In this chapter, the voltage and current stresses of the compensation components (including coils) of S-S and LCC-S topologies will be studied at 3 kW power level, which is the WPT1 power level suggested by SAE J2954 for wireless power charging of light-duty electric vehicles [31]. The study of current stress is meaningful and necessary since its value under fundamental frequency analysis directly affects the accuracy of peak voltage calculation, which will be seen in Section 6.2. The rest of this chapter is arranged as follows: First, voltage and current stresses of compensation components will be given based on fundamental frequency analysis, which is also referred to as first harmonic approximation (FHA) method. Second, the inaccuracy of certain components' peak voltage calculation will be pointed out through a specific example. The improved formulas will be derived afterwards, which is then verified through simulation. Finally, experiments were carried out to validate the improved method through a laboratory WPT setup.

6.2 S-S and LCC-S Compensations

Figure 6.1 shows a typical schematic of the WPT system. The H-bridge inverter composed of switches S_1-S_4 operates close to the resonant frequency to produce a high-frequency AC voltage to excite the primary side coil while the passive full-wave diode rectifier is used for the secondary side rectification. R_L is the equivalent load resistance modeling the power of subsequent stage, which is defined as $R_L = \frac{V_{out}}{I_{out}}$.

The compensation networks of S-S and LCC-S topologies are illustrated in Figure 6.2 with defined current and voltage reference direction. The loosely coupled transformer is modeled through a mutual inductance model [105]. To facilitate the analysis, the lump resistance modeling the losses of the WPT system is not included.

In Figure 6.2, $\dot{V}_s$, $\dot{I}_1$, $\dot{I}_2$, $\dot{I}_{L_f}$, $\dot{V}_{Tx}$ and $\dot{V}_{Rx}$ are corresponding phasors. R_{ac} is the equivalent resistance seen before the rectification stage (cf., Figure 6.1) with a value of $R_{ac} = \frac{8}{\pi^2} R_L$

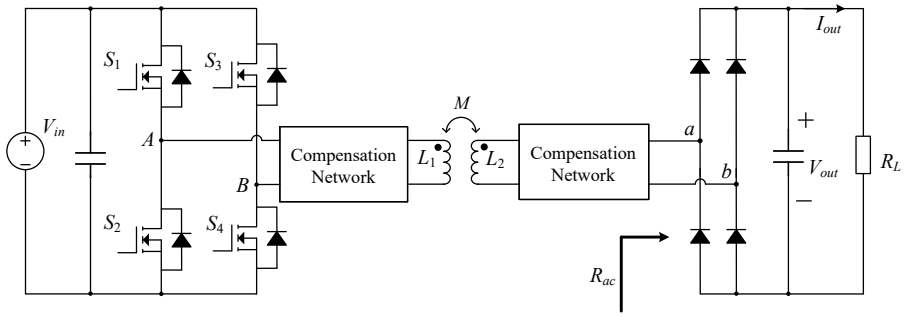


Figure 6.1: Schematic of a typical WPT system.

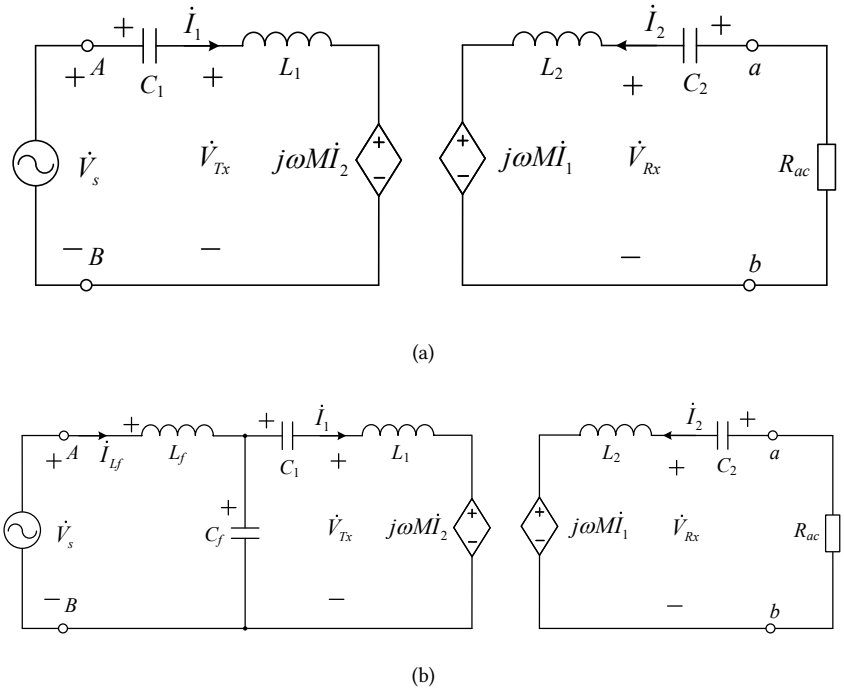


Figure 6.2: Equivalent circuits of S-S and LCC-S compensations based on the transformer's mutual inductance model. (a) S-S compensation. (b) LCC-S compensation.

[106]. Herein, the amplitude of $\dot{V}_s$ is assumed as the root-mean-square (rms) value of the fundamental frequency component of the inverter output voltage. So, when the inverter operates at natural resonant frequency with a square wave output voltage, the amplitude of $\dot{V}_s$ is: $V_s = |\dot{V}_s| = \frac{2\sqrt{2}}{\pi} V_{in}$.

Table 6.1: General expressions of compensation component stress in S-S topology.

	C_1	C_2	Primary Coil	Secondary Coil
RMS Current	$\lvert\dot{I}_1\rvert$	$\lvert\dot{I}_2\rvert$	$\lvert\dot{I}_1\rvert$	$\lvert\dot{I}_2\rvert$
Peak Voltage	$\sqrt{2}\lvert\frac{\dot{I}_1}{j\omega_0 C_1}\rvert$	$\sqrt{2}\lvert\frac{\dot{I}_2}{j\omega_0 C_2}\rvert$	$\sqrt{2}\lvert j\omega_0 L_1\dot{I}_1 + j\omega_0 M\dot{I}_2\rvert$	$\sqrt{2}\lvert j\omega_0 M\dot{I}_1 + j\omega_0 L_2\dot{I}_2\rvert$

Table 6.2: Simplified expressions of compensation component stress in S-S topology with $R_{ac} = P_o\frac{\omega_0^2 M^2}{V_s^2}$.

	C_1	C_2	Primary Coil	Secondary Coil
RMS Current	$\frac{P_o}{V_s}$	$\frac{V_s}{\omega_0 M}$	$\frac{P_o}{V_s}$	$\frac{V_s}{\omega_0 M}$
Peak Voltage	$\frac{\sqrt{2}\omega_0 L_1 P_o}{V_s}$	$\frac{\sqrt{2}L_2 V_s}{M}$	$\sqrt{2}V_s\sqrt{1+(\frac{L_1 R_{ac}}{\omega_0 M^2})^2}$	$\sqrt{2}V_s\sqrt{(\frac{L_2}{M})^2+(\frac{R_{ac}}{\omega_0 M})^2}$

6.2.1 Component Stress based on First Harmonic Approximation Method (FHA)

S-S Compensation

Based on Kirchhoff's voltage law, the equations for Figure 6.2(a) can be written as

$$\begin{cases} \dot{V}_s = (j\omega L_1 + \frac{1}{j\omega C_1})\dot{I}_1 + j\omega M\dot{I}_2, \\ j\omega M\dot{I}_1 + (j\omega L_2 + \frac{1}{j\omega C_2} + R_{ac})\dot{I}_2 = 0. \end{cases} \tag{6.1}$$

In (6.1), ω is the angular frequency, M is the mutual inductance. At resonant frequency of ω_0, the capacitor values of C_1 and C_2 are selected as

$$C_1 = \frac{1}{\omega_0^2 L_1}, \quad C_2 = \frac{1}{\omega_0^2 L_2}. \tag{6.2}$$

Based on (6.1) and (6.2), the voltage and current stresses of each component can be derived. The general and simplified expressions of peak voltage and current rms values are given in Table 6.1 and 6.2, respectively. In Table 6.2, R_{ac} can also be expressed as $R_{ac} = P_o\frac{\omega_0^2 M^2}{V_s^2}$ with P_o being the processed power.

LCC-S Compensation

Based on Kirchhoff's voltage law, the equations for Figure 6.2(b) can be written as

$$\begin{cases} \dot{V}_s = j\omega L_f\dot{I}_{L_f} + \frac{1}{j\omega C_f}(\dot{I}_{L_f} - \dot{I}_1), \\ \dot{V}_s = j\omega L_f\dot{I}_{L_f} + (j\omega L_1 + \frac{1}{j\omega C_1})\dot{I}_1 + j\omega M\dot{I}_2, \\ j\omega M\dot{I}_1 + (j\omega L_2 + \frac{1}{j\omega C_2} + R_{ac})\dot{I}_2 = 0. \end{cases} \tag{6.3}$$

Table 6.3: General expressions of compensation component stress in the LCC-S topology.

	C_1	C_2	C_f	Primary Coil	Secondary Coil	L_f
RMS Current	$\lvert\dot{I}_1\rvert$	$\lvert\dot{I}_2\rvert$	$\lvert\dot{I}_{L_f}-\dot{I}_1\rvert$	$\lvert\dot{I}_1\rvert$	$\lvert\dot{I}_2\rvert$	$\lvert\dot{I}_{L_f}\rvert$
Peak Voltage	$\sqrt{2}\lvert\frac{\dot{I}_1}{j\omega_0 C_1}\rvert$	$\sqrt{2}\lvert\frac{\dot{I}_2}{j\omega_0 C_2}\rvert$	$\sqrt{2}\lvert\frac{1}{j\omega_0 C_f}(\dot{I}_{L_f}-\dot{I}_1)\rvert$	$\sqrt{2}\lvert j\omega_0 L_1\dot{I}_1+j\omega_0 M\dot{I}_2\rvert$	$\sqrt{2}\lvert j\omega_0 L_2\dot{I}_2+j\omega_0 M\dot{I}_1\rvert$	$\sqrt{2}\lvert j\omega_0 L_f\dot{I}_{L_f}\rvert$

Table 6.4: Simplified expressions of compensation component stress in the LCC-S topology with $R_{ac}=\frac{1}{P_o}(\frac{M}{L_f}V_s)^2$.

	C_1	C_2	C_f	Primary Coil	Secondary Coil	L_f
RMS Current	$\frac{V_s}{\omega_0 L_f}$	$\frac{MV_s}{L_f R_{ac}}$	$\sqrt{(\frac{P_o}{V_s})^2+(\frac{V_s}{\omega_0 L_f})^2}$	$\frac{V_s}{\omega_0 L_f}$	$\frac{MV_s}{L_f R_{ac}}$	$\frac{P_o}{V_s}$
Peak Voltage	$\sqrt{2}(\frac{L_1}{L_f}-1)V_s$	$\sqrt{2}\omega_0 L_2\frac{MV_s}{L_f R_{ac}}$	$\sqrt{2}\omega_0 L_f\sqrt{(\frac{P_o}{V_s})^2+(\frac{V_s}{\omega_0 L_f})^2}$	$\sqrt{2}V_s\sqrt{(\frac{L_1}{L_f})^2+(\frac{\omega_0 M^2}{L_f R_{ac}})^2}$	$\sqrt{2}V_s\sqrt{(\frac{M}{L_f})^2+(\frac{\omega_0 L_2 M}{L_f R_{ac}})^2}$	$\sqrt{2}\frac{\omega_0 L_f P_o}{V_s}$

At resonant frequency of ω_0, the capacitor values of C_f, C_1 and C_2 are selected as

$$C_f=\frac{1}{\omega_0^2 L_f},\quad C_1=\frac{1}{\omega_0^2(L_1-L_f)},\quad C_2=\frac{1}{\omega_0^2 L_2}. \tag{6.4}$$

Based on (6.3) and (6.4), the current of $\dot{I}_1$ and $\dot{I}_2$ can be derived as

$$\dot{I}_1=\frac{\dot{V}_s}{j\omega_0 L_f},\quad \dot{I}_2=-\frac{1}{R_{ac}}\cdot\frac{M}{L_f}\dot{V}_s. \tag{6.5}$$

So, according to (6.3), (6.4) and (6.5), the voltage and current stresses of each component can be derived. The general and simplified expressions are given in Table 6.3 and 6.4. In Table 6.4, R_{ac} can also be expressed as $R_{ac}=\frac{1}{P_o}(\frac{M}{L_f}V_s)^2$.

6.3 Inaccuracy of Derived Formulas

Simulation results from circuit simulator PLECS based on a specific example are adopted to verify the calculations. Voltage and current sources are applied as the load for S-S and LCC-S compensations, respectively.

The coil parameters are taken from the laboratory prototype designed at 3 kW power rating with $L_1=338$ μH and $L_2=226$ μH. The operating frequency f_0 is 85 kHz recommended by SAE J2954 standard [31]. V_{in} (see Figure 6.1) is selected as 400 V.

6.3.1 S-S Compensation

The simulated and calculated results for each component are summarized in Table 6.5 with $M=90$ μH and $P_o=3$ kW. The relative error is defined by $\varepsilon=\frac{\text{Calculated Value}-\text{Simulated Value}}{\text{Simulated Value}}$. For PLECS solver, the max step size is 1e-7 s and the relative tolerance is 1e-6.

As it can be seen from Table 6.5, the calculated peak voltage for both primary and secondary coils is not as accurate as other values. Besides, both of the calculated values are smaller than the simulated ones. However, the current calculation based on FHA method has high accuracy.

Table 6.5: Compensation component stress in S-S topology with $M = 90\ \mu$H, $P_o = 3$ kW.

	C_1	C_2	Primary Coil	Secondary Coil
Cal.[1] RMS Current (A)	8.33	7.49	8.33	7.49
Sim.[2] RMS Current (A)	8.34	7.51	8.34	7.51
Error of ε (%)	-0.12	-0.27	-0.12	-0.27
Cal. Peak Voltage (V)	2126.7	1278.9	2186.8	1398.7
Sim. Peak Voltage (V)	2125.1	1275.4	2520.8	1720.1
Error of ε (%)	0.08	0.27	-13.25	-18.68

[1,2] Cal. and Sim. are short for Calculated and Simulated in this chapter.

Table 6.6: Compensation component stress in LCC-S topology with $M = 90\ \mu$H, $P_o = 3$ kW, $L_f = 100\ \mu$H.

	C_1	C_2	C_f	Primary Coil	Secondary Coil	L_f
Cal. RMS Current (A)	6.74	9.26	10.72	6.74	9.26	8.33
Sim. RMS Current (A)	6.74	9.30	10.35	6.74	9.30	8.41
Error of ε (%)	0	-0.43	3.57	0	-0.43	-0.95
Cal. Peak Voltage (V)	1212.1	1580.0	809.5	1832.8	1645.1	629.2
Sim. Peak Voltage (V)	1220.2	1580.0	756.0	1800.8	1940.0	1029.2
Error of ε (%)	-0.66	0	7.08	1.78	-15.2	-38.9

6.3.2 LCC-S Compensation

The simulated and calculated results for each component are summarized in Table 6.6 with $M = 90\ \mu$H, $P_o = 3$ kW, $L_f = 100\ \mu$H.

As it can be seen from Table 6.6, the calculated peak voltage for the secondary coil and L_f is not accurate, similar to S-S compensation, both of the calculated values are smaller than the simulated ones.

6.3.3 Improved Method

Due to the high accuracy of the current calculation based on FHA method, the more accurate component peak voltage can then simply be calculated based on Kirchhoff's voltage law considering the voltage across the related compensation capacitors.

S-S Compensation

Figure 6.3 shows the simulated waveforms at 3 kW, which is used to help explain the following calculation.

Refer to Figure 6.1 and 6.2, the voltage across the primary side coil can be expressed as: $v_{Tx} = v_{AB} - v_{C_1}$. Since $\dot{I}_1$ and $\dot{V}_s$ are in phase, so, the voltage of $-v_{C_1}$ is 90° (or $\frac{\pi}{2}$ radian) ahead of v_{AB} [cf., Figure 6.3(a)]. Therefore, the peak voltage is

$$\hat{V}_{Tx\_improved} = V_{in} + \hat{V}_{C_1} = V_{in} + \frac{\pi\omega_0 L_1 P_o}{2V_{in}}. \tag{6.6}$$

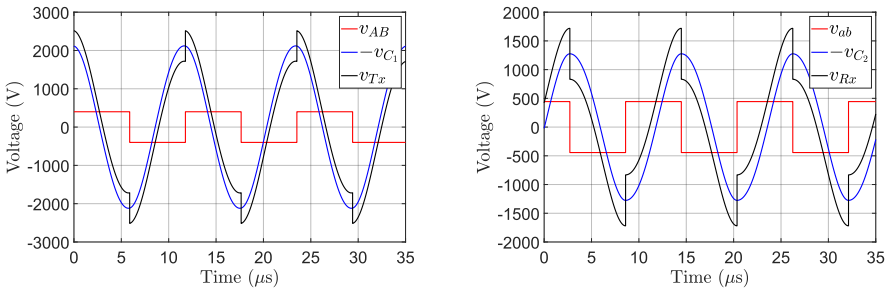


Figure 6.3: Simulated waveforms of the S-S compensation, defined reference direction is shown in Figure 6.2. (a) Primary side. (b) Secondary side.

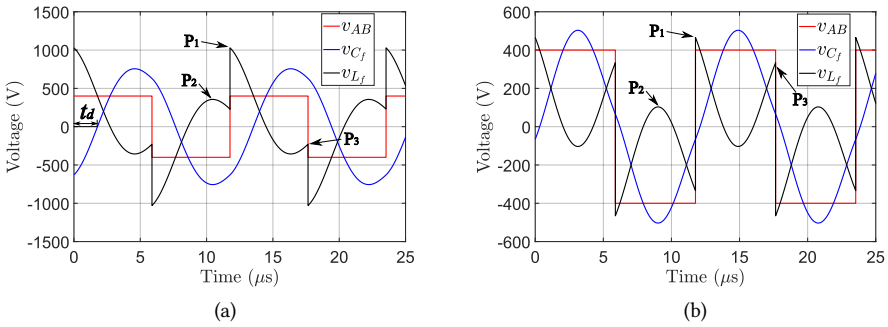


Figure 6.4: Simulated waveforms of the LCC-S compensation, defined reference direction is shown in Figure 6.2. (a) $P_o = 3$ kW. (b) $P_o = 300$ W.

Similarly, the peak voltage across the secondary coil is

$$\hat{V}_{Rx\_improved} = V_{out} + \hat{V}_{C_2} = \frac{\pi^2 \omega_0 M P_o}{8 V_{in}} + \frac{4 L_2 V_{in}}{\pi M}. \tag{6.7}$$

LCC-S Compensation

Figure 6.4 shows the simulated waveforms at 3 kW and 300 W, which is used to help explain the following calculation. The voltage across L_f can be expressed as

$$v_{L_f} = v_{AB} - v_{C_f}. \tag{6.8}$$

The phasor representation of v_{C_f} is

$$\dot{V}_{C_f} = (\frac{1}{j\omega_0 C_1} + j\omega_0 L_1)\dot{I}_1 + j\omega_0 M \dot{I}_2 = (j\omega_0 L_f + Z_r)\dot{I}_1. \tag{6.9}$$

Table 6.7: Improved formulas for peak voltage calculation.

S-S	$\hat{V}_{Tx} = V_{in} + \frac{\pi\omega_0 L_1 P_o}{2V_{in}}$	$\hat{V}_{Rx} = \frac{\pi^2\omega_0 M P_o}{8V_{in}} + \frac{4L_2 V_{in}}{\pi M}$
LCC-S	$\hat{V}_{L_f} = V_{in} + \frac{\pi\omega_0 L_f P_o}{2V_{in}}$	$\hat{V}_{Rx} = \frac{MV_{in}}{L_f} + \frac{\pi\omega_0 L_2 L_f P_o}{2MV_{in}}$

In (6.9), $Z_r = \dfrac{\omega_0^2 M^2}{R_{ac}}$. Substitute $\dot{I}_1$ from (6.5) into (6.9), then

$$\dot{V}_{C_f} = (j\omega_0 L_f + Z_r)\dot{I}_1 = \dot{V}_s - jZ_r \frac{\dot{V}_s}{\omega_0 L_f}. \tag{6.10}$$

Assuming $\dot{V}_s = V_s\angle 0^\circ$, at the instant when v_{AB} changes from $-V_{in}$ to V_{in}, the instantaneous value of v_{C_f} is the imaginary part of (6.10) multiplied by $\sqrt{2}$, i.e., $-\sqrt{2}\dfrac{\omega_0 M^2 V_s}{L_f R_{ac}}$. Therefore, the voltage across L_f at point P_1 is

$$\hat{V}_{L_f\_improved} = V_{in} + \sqrt{2}\frac{\omega_0 M^2 V_s}{L_f R_{ac}} = V_{in} + \frac{\pi\omega_0 L_f P_o}{2V_{in}}. \tag{6.11}$$

However, by further checking Figure 6.4, there are another two local peaks of P_2 and P_3. The proof that the voltage at P_1 is the global peak is given in Appendix in this chapter.

For the peak voltage across the secondary coil, it is similar to S-S compensation, which is

$$\hat{V}_{Rx\_improved} = V_{out} + \hat{V}_{C_2} = \frac{M}{L_f} V_{in} + \frac{\pi}{2}\frac{\omega_0 L_2 L_f P_o}{M V_{in}}. \tag{6.12}$$

The improved formulas are summarized in Table 6.7.

6.3.4 Discussion on Improved Formulas

For both methods based on FHA and improved formulas, a minimum peak voltage for primary and secondary coils in S-S compensation, and for L_f and secondary coil in LCC-S compensation can be derived. Since $a + b \geq 2\sqrt{ab}$ when $a \geq 0$ and $b \geq 0$, and therefore, the minimum peak voltage values for the components derived from Table 6.2, Table 6.4 and Table 6.7 are given as follows.

S-S Compensation

According to the FHA method given in Table 6.2:

$$\hat{V}_{Tx} \geq 2\sqrt{\omega_0 L_1 P_o},\ \hat{V}_{Rx} \geq 2\sqrt{\omega_0 L_2 P_o}. \tag{6.13}$$

According to the improved method:

$$\hat{V}_{Tx} \geq \sqrt{2\pi\omega_0 L_1 P_o},\ \hat{V}_{Rx} \geq \sqrt{2\pi\omega_0 L_2 P_o}. \tag{6.14}$$

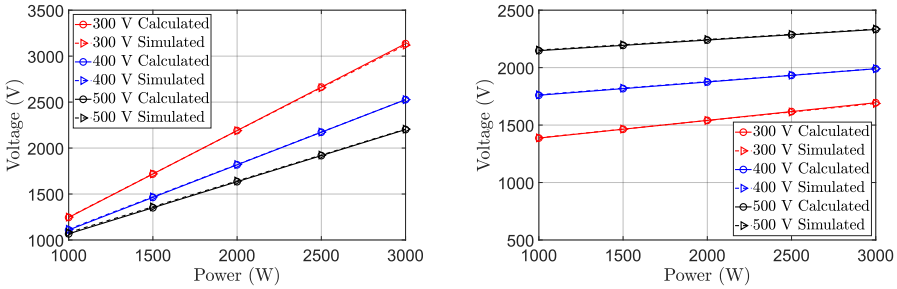


Figure 6.5: Peak voltage with S-S compensation at different input voltages, $M = 70$ μH. (a) Peak voltage of primary coil. (b) Peak voltage of secondary coil.

LCC-S Compensation

According to the FHA method given in Table 6.4:
For L_f, a similar formula of the minimum peak voltage cannot be derived. For L_2, it is:

$$\hat{V}_{Rx} \geq 2\sqrt{\omega_0 L_2 P_o}. \tag{6.15}$$

According to the improved method:

$$\hat{V}_{L_f} \geq \sqrt{2\pi\omega_0 L_f P_o},\ \hat{V}_{Rx} \geq \sqrt{2\pi\omega_0 L_2 P_o}. \tag{6.16}$$

From (6.14) and (6.16), it can be found that the minimum peak voltage expressions have the same form.

6.4 Simulation Verification

The newly derived formulas will be verified by simulation with different mutual inductance, power and input voltage values, which are shown from Figure 6.5 to Figure 6.8. The power changes from 1 kW to 3 kW, and the coil parameters are the measured values, i.e., $L_1 = 338$ μH and $L_2 = 226$ μH. The mutual inductance is selected between 70 μH and 105 μH, which corresponds to a coupling coefficient between 0.25 and 0.38. For LCC-S compensation, $L_f = 100$ μH.

6.4.1 S-S Compensation

Figure 6.5 and Figure 6.6 show the simulated and calculated peak voltage across the primary and secondary coils when M is 70 μH and 105 μH, respectively.

6.4.2 LCC-S Compensation

Figure 6.7 and Figure 6.8 show the simulated and calculated peak voltage across L_f and secondary coil when M is 70 μH and 105 μH, respectively.

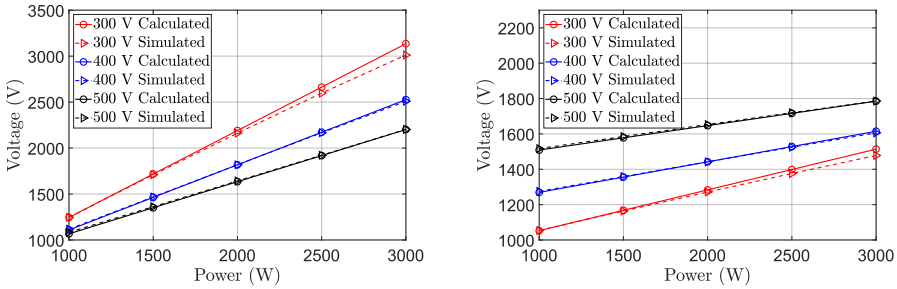


Figure 6.6: Peak voltage with S-S compensation at different input voltages, $M = 105\ \mu$H. (a) Peak voltage of primary coil. (b) Peak voltage of secondary coil.

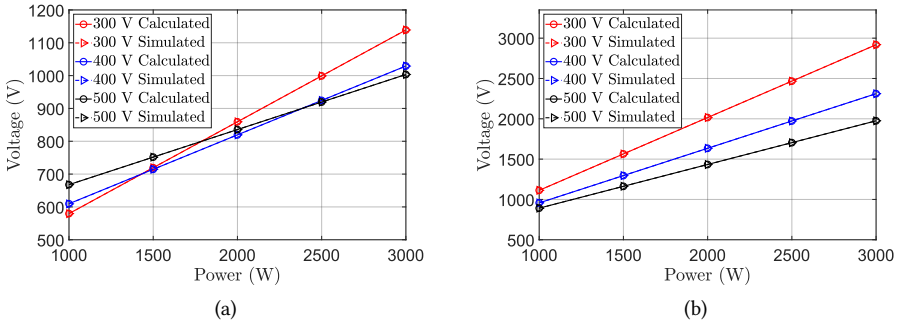


Figure 6.7: Peak voltage with LCC-S compensation at different input voltages, $M = 70\ \mu$H. (a) Peak voltage of L_f. (b) Peak voltage of secondary coil.

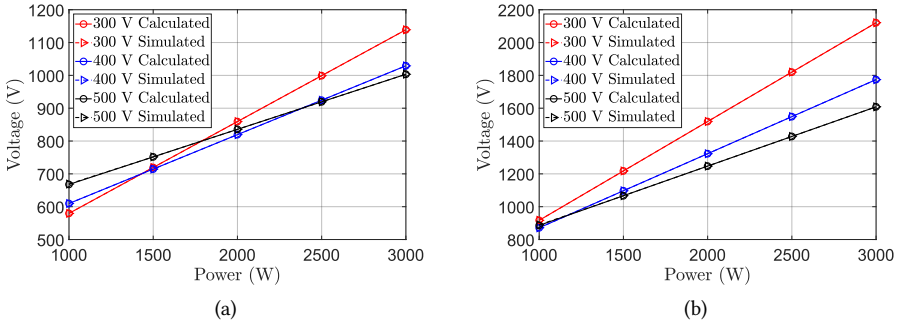
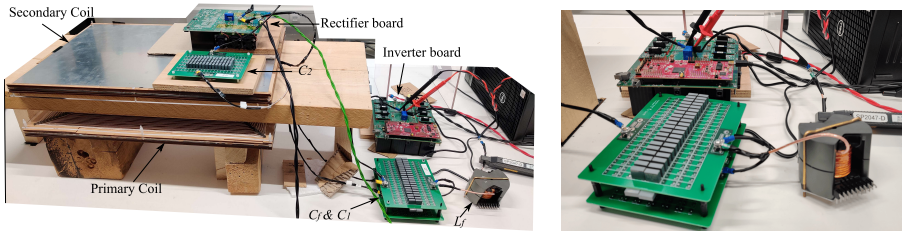
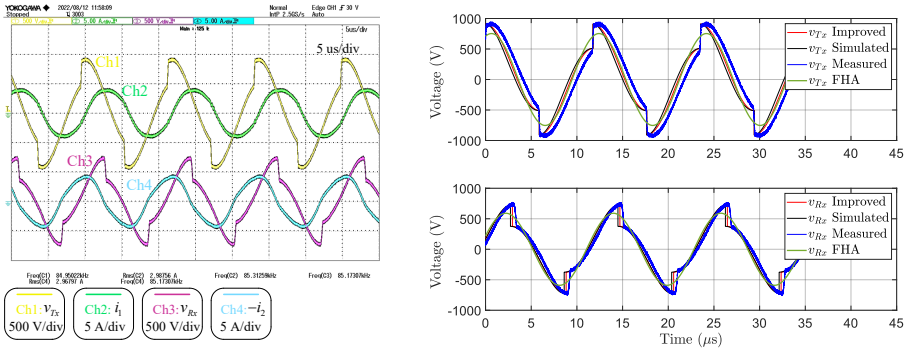


Figure 6.8: Peak voltage with LCC-S compensation at different input voltages, $M = 105\ \mu$H. (a) Peak voltage of L_f. (b) Peak voltage of secondary coil.



(a) (b)

Figure 6.9: (a) Experimental setup with LCC-S compensation. (b) Zoom-in of primary side circuit.



(a) (b)

Figure 6.10: Experimental results of S-S compensation operating at $V_{in} = 200$ V and $P_o = 500$ W, defined reference direction is shown in Figure 6.2. (a) Measured waveforms. (b) Voltage waveforms of v_{Tx} and v_{Rx} based on improved method, simulation, measurement and FHA method.

It can be seen that the calculated peak voltage values match the simulation results well for both compensations. For LCC-S compensation, the two values are almost the same, so, the two lines coincide. For S-S compensation, due to the small power mismatch between simulation and calculation in some cases, the two peak voltage values could have a small difference.

6.5 Experimental Validation

The experimental setup with LCC-S compensation is shown in Figure 6.9. For the experiment, the mutual inductance M was measured to be 105 μH at a vertical distance around 10 cm. The inductance value of L_f is 100.5 μH. Based on the voltage rating of the available differential probes of Keysight N2791A and Yokogawa 700924, the WPT prototype was tested at a lower voltage and power value.

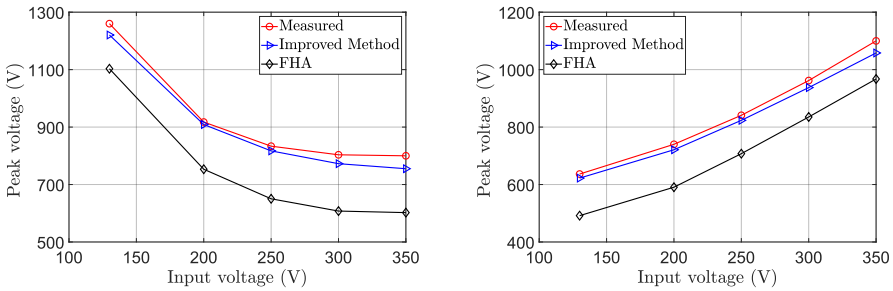


Figure 6.11: S-S compensation, peak voltage across coils at 500 W from measurement, improved and FHA method. (a) Peak voltage of primary coil. (b) Peak voltage of secondary coil.

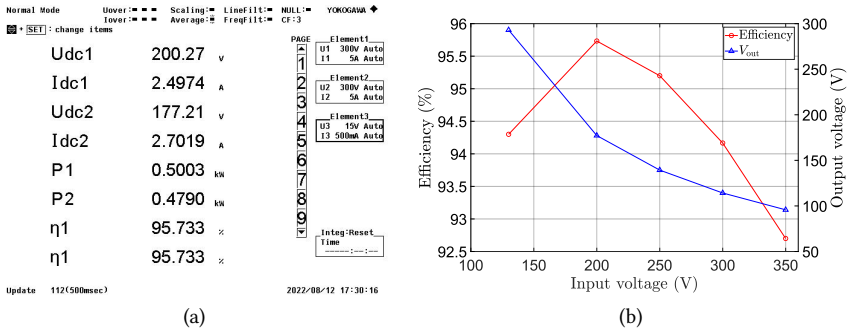


Figure 6.12: DC-DC efficiency of the S-S compensated WPT system. (a) Screenshot of the WT500 power analyzer. Udc1 and Idc1 are dc voltage and current values from input side, and Udc2 and Idc2 are the voltage and current values from output side. The efficiency is $\eta = \frac{P2}{P1}$. (b) Curve of the system efficiency at 500 W power level, and the corresponding output voltage.

6.5.1 S-S Compensation

Figure 6.10 shows the measurement results with $V_{in} = 200$ V and $P_o = 500$ W. Figure 6.11 shows the peak voltage of the coils under different input voltage values when $P_o = 500$ W.

As an additional reference, Figure 6.12 shows the measured dc-dc efficiency of the S-S compensated WPT system at 500 W power level.

6.5.2 LCC-S Compensation

Figure 6.13 shows the measurement results with $V_{in} = 300$ V and $P_o = 500$ W. Figure 6.14 shows the peak voltage of L_f and secondary coil under different input voltage values when $P_o = 500$ W.

As an additional reference, Figure 6.15 shows the measured dc-dc efficiency of the LCC-S compensated WPT system at 500 W power level.

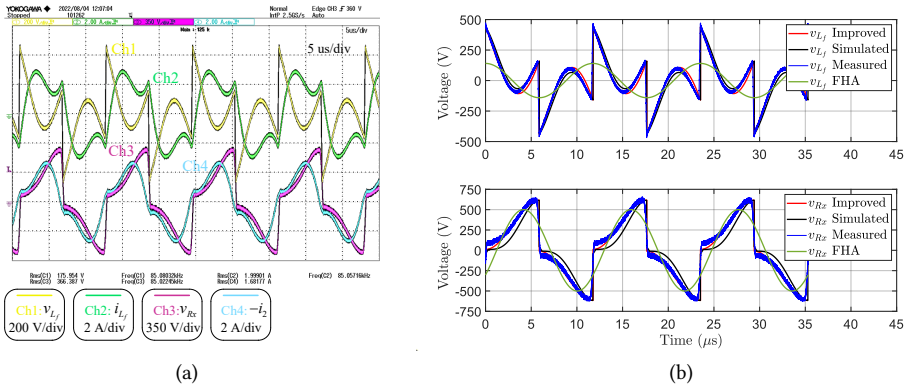


Figure 6.13: Experimental results of LCC-S compensation operating at $V_{in} = 300$ V and $P_o = 500$ W, defined reference direction is shown in Figure 6.2. (a) Measured waveforms. (b) Voltage waveforms of v_{L_f} and v_{Rx} based on improved method, simulation, measurement and FHA method.

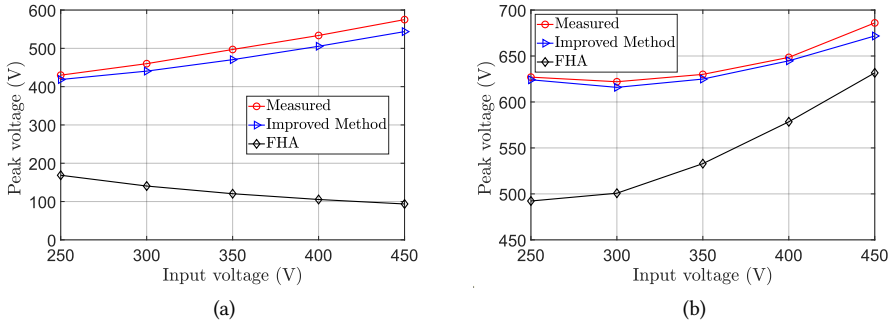
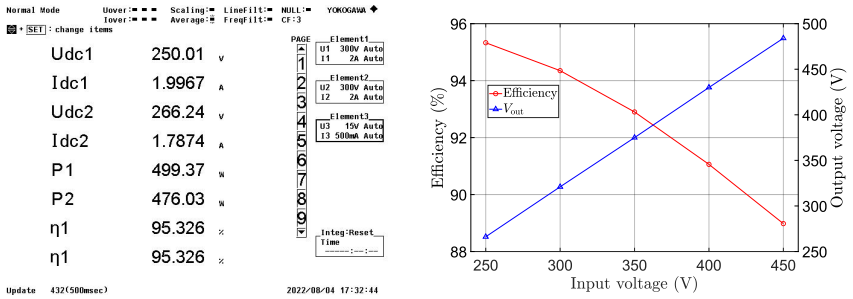


Figure 6.14: LCC-S compensation, peak voltage across L_f and secondary coil at 500 W from measurement, improved and FHA method. (a) Peak voltage of L_f. (b) Peak voltage of secondary coil.

6.5.3 Discussion

As it can be seen from the experiments, the improved formulas can provide accurate peak voltage results for both S-S and LCC-S compensations. The improved piecewise voltage analytic function is given in Appendix in this chapter.

It should be noted that in practical application, the resonant compensation circuit will usually be tuned to be a bit inductive for zero voltage switching (ZVS) turn-on of the front-end full-bridge inverter, which could introduce some calculation error, however, this error can be neglected at designed rated condition when the components bear the maximum stress.



(a) (b)

Figure 6.15: DC-DC efficiency of the LCC-S compensated WPT system. (a) Screenshot of the WT500 power analyzer. (b) Curve of the system efficiency at 500 W power level, and the corresponding output voltage.

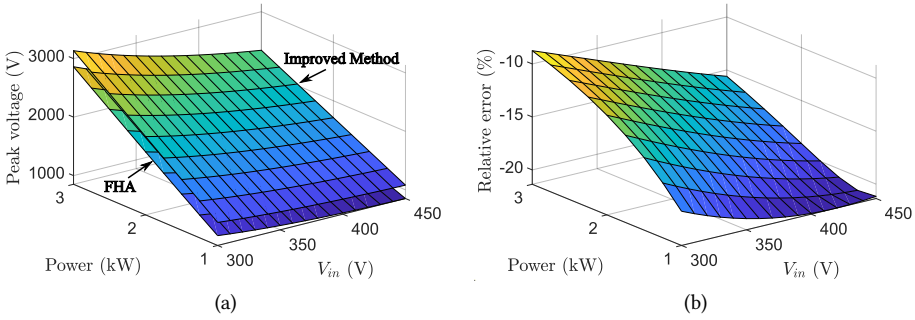
6.5.4 Voltage Stress over a Wider Operational Range

Herein, the voltage stresses will be calculated and compared over a wider operational range based on the FHA and improved methods. The relative error between these two methods will be given with the expression of $\varepsilon = \frac{\text{Value of FHA}-\text{Value of Improved Method}}{\text{Value of Improved Method}}$. Below, $L_1 = 338\ \mu$H, $L_2 = 226\ \mu$H, $M = 105\ \mu$H, $L_f = 100\ \mu$H.

From these results, it can be seen that the newly introduced method can improve the accuracy of the peak voltage estimation over a wide operating range, which is especially true for the peak voltage calculation on the input resonant inductor in the LCC-S compensated WPT system.

S-S Compensation

The results are given in Figure 6.16 and Figure 6.17.



(a) (b)

Figure 6.16: S-S compensation. (a) Peak voltage of primary coil. (b) Relative error.

LCC-S Compensation

The results are given in Figure 6.18 and Figure 6.19.

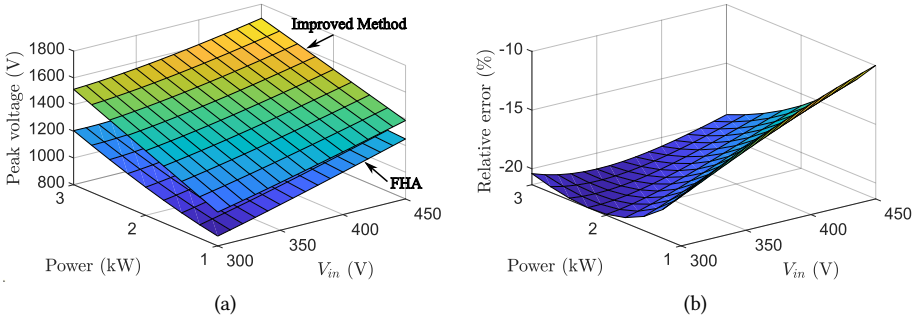


Figure 6.17: S-S compensation. (a) Peak voltage of secondary coil. (b) Relative error.

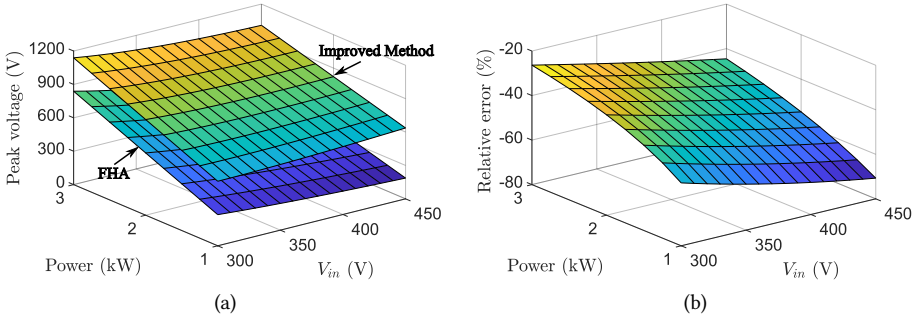


Figure 6.18: LCC-S compensation. (a) Peak voltage of L_f. (b) Relative error.

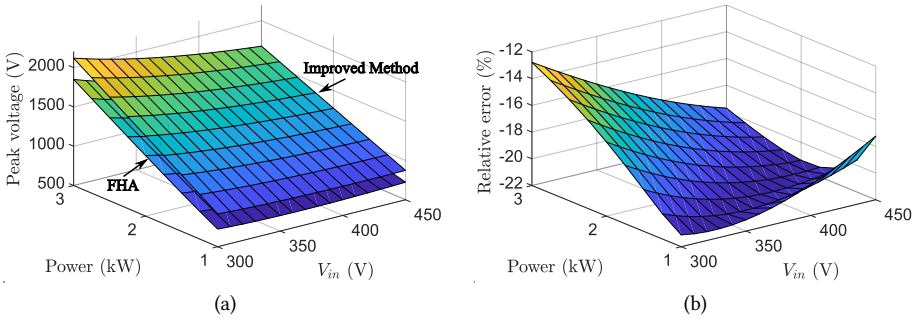


Figure 6.19: LCC-S compensation. (a) Peak voltage of secondary coil. (b) Relative error.

6.6 Conclusion

An improved peak voltage calculation method for compensation components is introduced in wireless power transfer systems employing S-S and LCC-S compensation topologies, which is often ignored in current literature. This method is verified by both simulation and experimental results, which provides practical guidance for the design of WPT systems, especially for electrical insulation design. The introduced method can also be applied to other compensation networks such as LCC-LCC compensation topology in a similar way. In essence, the accuracy of the introduced method depends on the related compensation capacitor voltage calculation under FHA method, and this condition is often satisfied for a well-designed WPT system.

6.7 Appendix A

For reading convenience, the equation is re-given as follows.

$$v_{L_f} = v_{AB} - v_{C_f}, \quad \dot{V}_{C_f} = \dot{V}_s - jZ_r \frac{\dot{V}_s}{\omega_0 L_f}, \quad Z_r = \frac{\omega_0^2 M^2}{R_{ac}}. \tag{6.17}$$

As it can be seen from (6.17), the phase delay of v_{C_f} relative to the fundamental frequency component of v_{AB} is less than $\frac{\pi}{2}$ radian and larger than zero [cf., Figure 6.4(a), i.e., $0 < \frac{t_d}{T_0} < \frac{1}{4}$ with T_0 being the switching period], and therefore, the voltage of v_{L_f} has and only has three local peaks.

The voltage across L_f at P_1, P_2 and P_3 can be calculated as

$$\begin{cases} v_{L_f\_P_1} = V_{in} + \sqrt{2}\frac{\omega_0 M^2}{L_f R_{ac}} V_s, \\ v_{L_f\_P_2} = [\sqrt{2} \times \sqrt{1 + (\frac{\omega_0 M^2}{L_f R_{ac}})^2} - \frac{\pi}{2\sqrt{2}}] V_s, \\ v_{L_f\_P_3} = V_{in} - \sqrt{2}\frac{\omega_0 M^2}{L_f R_{ac}} V_s. \end{cases} \tag{6.18}$$

From (6.18), it is clear that $v_{L_f\_P_1}$ is larger than $v_{L_f\_P_3}$. The voltage difference between P_1 and P_2 is

$$\Delta v_{L_f\_P_1P_2} = v_{L_f\_P_1} - v_{L_f\_P_2} = \sqrt{2} V_s [\frac{\pi}{2} + \frac{\omega_0 M^2}{L_f R_{ac}} - \sqrt{1 + (\frac{\omega_0 M^2}{L_f R_{ac}})^2}]. \tag{6.19}$$

Since (6.19) is always larger than 0, so, $v_{L_f\_P_1}$ is larger than $v_{L_f\_P_2}$. Summarizing, the voltage across L_f at P_1 instant is the maximum voltage in one period.

6.8 Appendix B

Without loss of generality, assuming the time instant when v_{AB} passes zero from $-V_{in}$ to V_{in} is 0 s, and T_0 is the switching period, then the time domain expressions are as follows:

6.8.1 S-S Compensation

$$v_{Tx}(t) = \begin{cases} V_{in} + \hat{V}_{C_1} \sin(\omega_0 t + \frac{\pi}{2}), t \in [0, \frac{T_0}{2}), \\ -V_{in} + \hat{V}_{C_1} \sin(\omega_0 t + \frac{\pi}{2}), t \in [\frac{T_0}{2}, T_0). \end{cases} \tag{6.20}$$

$$v_{Rx}(t) = \begin{cases} V_{out} + \hat{V}_{C_2} \sin(\omega_0 t), t \in [0, \frac{T_0}{4}), \\ -V_{out} + \hat{V}_{C_2} \sin(\omega_0 t), t \in [\frac{T_0}{4}, \frac{3T_0}{4}), \\ V_{out} + \hat{V}_{C_2} \sin(\omega_0 t), t \in [\frac{3T_0}{4}, T_0). \end{cases} \tag{6.21}$$

In (6.20) and (6.21), $\hat{V}_{C_1} = \dfrac{\pi\omega_0 L_1 P_o}{2V_{in}}$, $\hat{V}_{C_2} = \dfrac{4L_2 V_{in}}{\pi M}$.

6.8.2 LCC-S Compensation

$$v_{L_f}(t) = \begin{cases} V_{in} - \hat{V}_{C_f}\sin(\omega_0 t + \varphi), t \in [0, \dfrac{T_0}{2}), \\ -V_{in} - \hat{V}_{C_f}\sin(\omega_0 t + \varphi), t \in [\dfrac{T_0}{2}, T_0). \end{cases} \tag{6.22}$$

$$v_{Rx}(t) = \begin{cases} V_{out} + \hat{V}_{C_2}\sin(\omega_0 t - \dfrac{\pi}{2}), t \in [0, \dfrac{T_0}{2}), \\ -V_{out} + \hat{V}_{C_2}\sin(\omega_0 t - \dfrac{\pi}{2}), t \in [\dfrac{T_0}{2}, T_0). \end{cases} \tag{6.23}$$

In (6.22) and (6.23), $\varphi = -\arctan\dfrac{\omega_0 L_f P_o}{V_s^2}$, $\hat{V}_{C_f} = \sqrt{2}\omega_0 L_f \sqrt{(\frac{P_o}{V_s})^2 + (\frac{V_s}{\omega_0 L_f})^2}$, and $\hat{V}_{C_2} = \dfrac{\pi\omega_0 L_2 L_f P_o}{2MV_{in}}$.

7

Current Distortion Modeling of a fully Compensated LCC-S based WPT System

This chapter studies the current distortion phenomenon in an LCC-S compensated wireless power transfer (WPT) system. Due to the constant voltage output property of WPT system featuring LCC-S compensation, a traditional back-end dc-dc converter can be easily and relatively safely connected to its system, which improves the voltage regulation ability of the WPT system. However, for the LCC-S compensated WPT system, the current through the input resonant inductor is highly distorted, and therefore, the parameter tuning of compensation components to achieve zero voltage switching (ZVS) based on first harmonic approximation (FHA) method is limited. This chapter will introduce a more accurate calculation model for the switching current, and this analytical model will be verified through circuit simulation results. [1]

[1]This chapter is a summary of part of the master thesis "Benchmark of Different Compensations for Wireless Power Transfer with DC/DC Converter Included" by Pengcheng Ye, who was at that time daily supervised by Guangyao Yu for his master thesis work.

7.1 Introduction

As mentioned in Chapter 6, compensation network plays an important role in a wireless power transfer (WPT) system. Different compensation networks have their own characteristics. For example, S-S compensated WPT system has a constant current (CC) output, which finds a suitable application in battery charging while LCC-S compensated WPT system has a constant voltage (CV) output, where a traditional back-end dc-dc converter can be easily and relatively safely connected to its output.

To achieve a high efficiency performance for the WPT system, zero voltage switching (ZVS) turn-on is recommended for the switches, so, correct tuning of the compensation component is necessary. For the ZVS implementation, the inverter frequency can be adjusted [107], however, the adjustable frequency range is limited according to SAE J2954 [31] for electric vehicles charging, and its natural resonant frequency is recommended at 85 kHz. Therefore, another feasible method is tuning of the compensation components [108], [109]. The principle of both methods is to make the input impedance seen by the front-end H-bridge inverter slightly inductive, thus, the switching current can be utilized to charge or discharge the parasitic output capacitance C_{oss}. However, this switching current in a high-order compensation network is difficult to be modeled and calculated. In [108], a calculation method for the switching current (or MOSFET turn-off current) is described and introduced for a double sided LCC compensated WPT system, however, under some cases, the error between the calculated and simulated values is huge.

In this chapter, the switching current in an LCC-S compensated WPT system is modeled considering the harmonics from both the input and output side, and this method shows an improved prediction of the switching current. The rest of this chapter is arranged as follows: Section 7.2 introduces the parameter tuning for LCC-S compensation and the switching current calculation under FHA analysis. Section 7.3 presents the enhanced modeling for switching current considering high-order harmonics from both input and output sides. Section 7.4 shows the simulation results, and Finally, Section 7.5 concludes this chapter.

7.2 Analysis Based on First Harmonic Approximation (FHA) Method

The typical LCC-S compensated WPT system is shown in Figure 7.1. Herein, V_{in} is the input voltage source, switches of S_1-S_4 form the primary side H-bridge inverter, L_f, C_f and C_1 form the primary side LCC compensation network while C_2 is the secondary side serial capacitance. L_1 and L_2 are the self inductances of the loosely coupled transformer, which has a mutual inductance of M. The loosely coupled transformer can be modeled through a mutual inductance model [105]. Under FHA method when only the fundamental-frequency component is considered, the circuit is redrawn in Figure 7.2. The reflected impedance of Z_{eq} in Figure 7.2(b) can be easily calculated as $Z_{\text{eq}} = \dfrac{-j\omega M\dot{I}_2}{\dot{I}_1} = \dfrac{\omega^2 M^2}{Z_{\text{sec}}}$, where $Z_{\text{sec}} = j\omega L_2 + \dfrac{1}{j\omega C_2} + Z_{\text{ab}}$. In particular, under FHA analysis, Z_{ab} can be represented by an equivalent resistance R_{ac} [106], which is calculated by (7.1).

$$R_{\text{ac}} = \frac{8}{\pi^2} R_L. \tag{7.1}$$

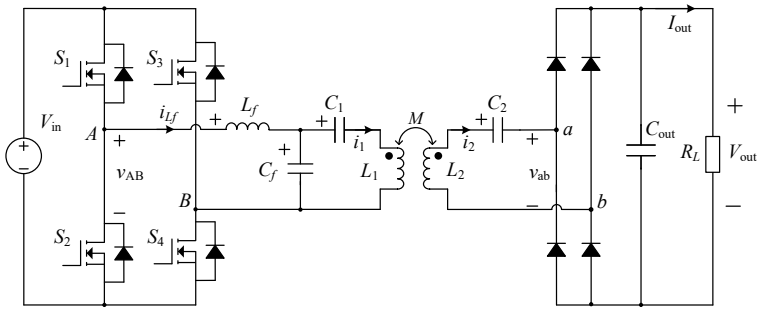


Figure 7.1: Schematic of a typical LCC-S compensated WPT system.

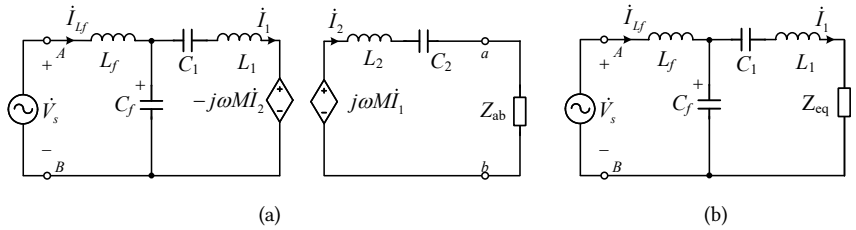


Figure 7.2: Equivalent circuit of LCC-S compensation based on the transformer's mutual inductance model. (a) Circuit with mutual inductance model. (b) Circuit with reflected impedance.

7

The amplitude of $\dot{V}_s$ is assumed as the root-mean-square (rms) value of the fundamental frequency component of the inverter output voltage. So, when the inverter operates with a square wave output voltage, the amplitude of $\dot{V}_s$ is: $V_s = |\dot{V}_s| = \frac{2\sqrt{2}}{\pi} V_{\text{in}}$.

In Chapter 6, the selections of the compensation parameters are given by (6.4), which are regiven in (7.2)

$$C_f = \frac{1}{\omega_0^2 L_f}, \quad C_1 = \frac{1}{\omega_0^2 (L_1 - L_f)}, \quad C_2 = \frac{1}{\omega_0^2 L_2}. \tag{7.2}$$

In (6.4), ω_0 is the resonant angular frequency.

To better understand and remember the selection of compensation parameters, one can analyze a more general circuit shown in Figure 7.3, which is redrawn from Figure 7.2(b). In Figure 7.3, the equivalent input impedance is

$$Z_{\text{in}} = Z_1 + \frac{Z_2 Z_3}{Z_2 + Z_3}. \tag{7.3}$$

Therefore, the current through primary coil is

$$\dot{I}_1 = \frac{\dot{V}_s}{Z_{\text{in}}} \cdot \frac{Z_2}{Z_2 + Z_3} = \frac{\dot{V}_s}{Z_1 + \frac{Z_1 + Z_2}{Z_2} \cdot Z_3}. \tag{7.4}$$

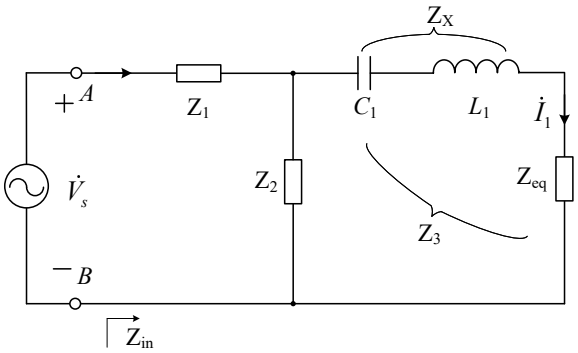


Figure 7.3: General circuit analysis for LCC-S compensation redrawn from Figure 7.2(b).

Since the impedance Z_3 is affected by the load, in order to ensure that the coil current is not influenced by Z_3, one can simply let $Z_1 + Z_2 = 0$. Therefore, if Z_1 is an inductor with an inductance value of L_f, then Z_2 can be a capacitor, and its value is given in (7.2).

If $Z_1 + Z_2 = 0$, which is achieved by adding an additional LC resonant branch circuit, then the primary coil current becomes

$$\dot{I}_1 = \frac{\dot{V}_s}{Z_1}. \tag{7.5}$$

For the selection of C_2, it is similar to the one in S-S compensation, which is selected to cancel the self inductance of L_2, and its value is given in (7.2).

The selection of C_1 is to achieve zero phase angle (ZPA) seen from the input side to minimize the reactive power. When $Z_1 + Z_2 = 0$, the input impedance is $Z_{\text{in}} = \dfrac{Z_1 Z_2}{Z_2 + Z_3} = \dfrac{Z_1 Z_2}{Z_3 - Z_1}$. Since $Z_1 = j\omega_0 L_f$, $Z_2 = \frac{1}{j\omega_0 C_f}$, $Z_3 = Z_X + Z_{\text{eq}}$, where $Z_{\text{eq}} = \dfrac{\omega_0^2 M^2}{R_{\text{ac}}}$, to let the input impedance be pure resistance, Z_X should be equal to Z_1, and therefore, (7.6) should be satisfied.

$$j(\omega_0 L_1 - \frac{1}{\omega_0 C_1}) = j\omega_0 L_f. \tag{7.6}$$

To solve C_1 in (7.6) leads to the result given in (7.2).

Based on the discussions above, one can easily get expressions for the primary coil current $\dot{I}_1$, induced voltage across the secondary coil, which equals to $\dot{V}_{\text{ab}}$ due to the impedance cancellation of L_2 and C_2, and the output dc voltage V_{out} as follows.

$$\dot{I}_1 = \frac{\dot{V}_s}{j\omega_0 L_f}, \quad \dot{V}_{\text{ab}} = j\omega_0 M \dot{I}_1 = \frac{M}{L_f}\dot{V}_s, \quad V_{\text{out}} = \frac{M}{L_f} V_{\text{in}}. \tag{7.7}$$

The voltage gain is $G_v = \dfrac{V_{\text{out}}}{V_{\text{in}}} = \dfrac{M}{L_f}$.

For example, Figure 7.4 shows one simulation result with LCC-S compensation. Suppose

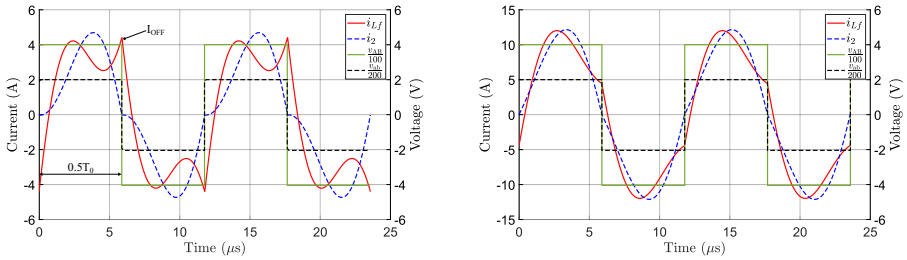


Figure 7.4: Simulation results of v_{AB}, v_{ab}, i_{Lf} and i_2 with $L_1 = 300$ μH, $L_2 = 200$ μH, $M = 80$ μH, $L_f = 80$ μH, $V_{in} = 400$ V. (a) P_o= 1 kW. (b) P_o = 3 kW.

the phase of $\dot{V}_s$ is zero, namely, $\dot{V}_s = V_s\angle 0^\circ$, and the imaginary part is used for time domain calculation, then,

$$\begin{cases} i_1(t) = \dfrac{\sqrt{2}V_s}{\omega_0 L_f}\sin(\omega_0 t - \dfrac{\pi}{2}) \\ i_2(t) = \dfrac{\sqrt{2}MV_s}{L_f R_{ac}}\sin(\omega_0 t) \\ v_{C1}(t) = \dfrac{\sqrt{2}V_s}{\omega_0^2 L_f C_1}\sin(\omega_0 t - \pi). \end{cases} \tag{7.8}$$

From Figure 7.1, one can know

$$L_f\frac{di_{Lf}}{dt} + v_{C1} + L_1\frac{di_1}{dt} - M\frac{di_2}{dt} = v_{AB}. \tag{7.9}$$

Integrating both sides of equation (7.9) from 0 to $\dfrac{T_0}{2}$ with T_0 being the switching period, (7.10) can be derived. Here, $2I_{OFF} = i_{Lf}(t = \frac{T_0}{2}) - i_{Lf}(t = 0)$, and I_{OFF} is the value of the switching current.

$$2I_{OFF}L_f + \int_0^{\frac{T_0}{2}} v_{C1}(t)dt + L_1[i_1(t = \frac{T_0}{2}) - i_1(t = 0)] - M[i_2(t = \frac{T_0}{2}) - i_2(t = 0)] = \frac{T_0}{2}V_{in}. \tag{7.10}$$

Substitute (7.8) and $C_1 = \dfrac{1}{\omega_0^2(L_1 - L_f)}$, $\dfrac{\omega_0 T_0}{2} = \pi$ into (7.10), one can get

$$I_{OFF} = \frac{(\pi - \frac{8}{\pi})V_{in}}{2\omega_0 L_f} = (\frac{\pi}{2} - \frac{4}{\pi})\cdot\frac{V_{out}}{\omega_0 M}. \tag{7.11}$$

Interestingly, from (7.11), the switching current I_{OFF} will not change when the load varies.

7.2.1 A specific simulation and calculation example

The result of (7.11) is verified through two simulation circuits, one is shown in Figure 7.1 and the other is shown in Figure 7.5 with an equivalent resistance of R_{ac}.

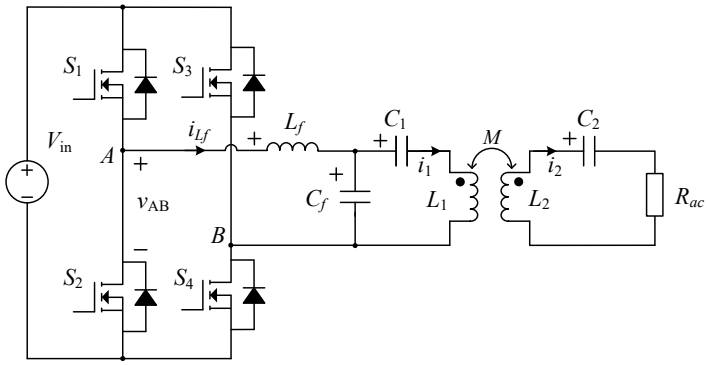


Figure 7.5: LCC-S compensated WPT system without secondary side diode rectifier .

Table 7.1: Summary of results from a specific LCC-S compensated WPT example.

Presumed Power (W)	1000	1500	2000	2500	3000
I_{OFF} from (7.11)	2.79	2.79	2.79	2.79	2.79
Sim. Power from Fig. 7.5 (W)	1000.0	1500.0	2000.0	2500.0	3000.0
Sim. I_{OFF} from Fig. 7.5 (A)	2.99	2.99	2.99	2.99	2.99
Sim. Power from Fig. 7.1 (W)	1000.1	1500.0	2000.0	2500.0	3000.0
Sim. I_{OFF} from Fig. 7.1 (A)	4.40	4.41	4.41	4.41	4.41
I_{OFF} Relative Error with Fig. 7.5 (%)	−6.69	−6.69	−6.69	−6.69	−6.69
I_{OFF} Relative Error with Fig. 7.1 (%)	−36.59	−36.73	−36.73	−36.73	−36.73

The parameters for the circuit simulation are: $L_1 = 300\ \mu$H, $L_2 = 200\ \mu$H, $M = 80\ \mu$H, $L_f = 80\ \mu$H, $C_{\text{out}} = 100\ \mu$F, $V_{\text{in}} = 400$ V, $f_0 = 85$ kHz, all other components are ideal. The load resistance of R_L is selected based on (7.12):

$$R_L = \frac{M^2 V_{\text{in}}^2}{L_f^2 P_o}, \tag{7.12}$$

where P_o is the presumed power.

PLECS circuit simulator is used for simulation with maximum step size of 2e-8 s (or 5e-8 s) and 1e-6 relative tolerance. The results are summarized in Table 7.1.

From the simulation results in Table 7.1, the simulated I_{OFF} is also a constant within the power range selected in this example. It is obvious that the calculated switching current I_{OFF} is closer to the simulated results based on Figure 7.5. For example, Figure 7.6 shows the current through L_f under 2 kW condition. Therefore, a more accurate model needs to be introduced where both the primary side and secondary side harmonics are considered.

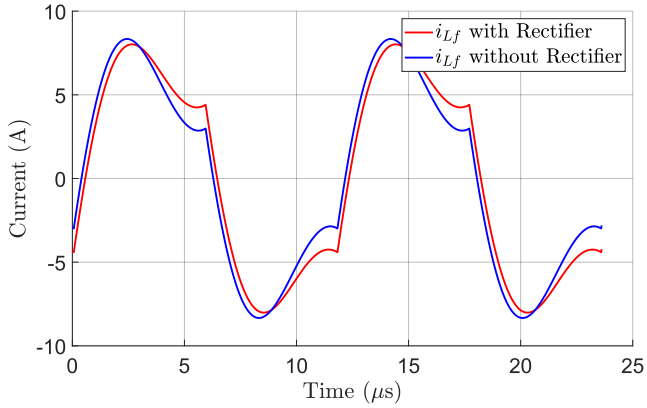


Figure 7.6: Current through L_f with and without diode rectifier, both are under 2 kW condition.

7.3 Enhanced modeling Considering Harmonics from Both Sides

Some assumptions have to be made for the rest of the analysis, and they are: 1) The secondary side voltage of v_{ab} is a square wave; 2) v_{AB} and v_{ab} are in phase. For the first assumption, in light load condition, it might be invalid because i_2 is zero for some time periods.

7.3.1 Derivation of High-order Harmonic Currents

Applying Kirchhoff's voltage law to the two circuits of the primary side and one of the secondary side shown in Figure 7.1, (7.13) can be obtained considering a specific high-order harmonic.

$$\begin{cases} jk\omega_0 L_f \dot{I}_{Lf\_kh} + \dfrac{1}{jk\omega_0 C_f}(\dot{I}_{Lf\_kh} - \dot{I}_{1\_kh}) = \dfrac{2\sqrt{2}}{k\pi} V_{\text{in}} e^{j0} = \dfrac{2\sqrt{2}}{k\pi} V_{\text{in}} \\ \dot{I}_{1\_kh}\left(\dfrac{1}{jk\omega_0 C_1} + jk\omega_0 L_1 + \dfrac{1}{jk\omega_0 C_f}\right) - jk\omega_0 M \dot{I}_{2\_kh} - \dfrac{1}{jk\omega_0 C_f}\dot{I}_{Lf\_kh} = 0 \\ jk\omega_0 M \dot{I}_{1\_kh} - \left(jk\omega_0 L_2 + \dfrac{1}{jk\omega_0 C_2}\right)\dot{I}_{2\_kh} = \dfrac{2\sqrt{2}}{k\pi} V_{\text{out}} e^{j0} = \dfrac{2\sqrt{2}}{k\pi} V_{\text{out}} \end{cases} \tag{7.13}$$

In (7.13), $\dot{I}_{Lf\_kh}$, $\dot{I}_{1\_kh}$ and $\dot{I}_{2\_kh}$ are the phasors of the corresponding high-order harmonics, and $k = 2n+1$ (n = 1, 2, 3..., namely, k = 3, 5, 7...).

Based on (7.2), (7.13) can also be re-written as follows for ease of analysis.

$$\begin{cases} j\omega_0 L_f\left(k - \dfrac{1}{k}\right)\dot{I}_{Lf\_kh} + j\dfrac{1}{k}\omega_0 L_f \dot{I}_{1\_kh} = \dfrac{2\sqrt{2}}{k\pi} V_{\text{in}} \\ j\omega_0 L_1\left(k - \dfrac{1}{k}\right)\dot{I}_{1\_kh} - jk\omega_0 M \dot{I}_{2\_kh} + j\dfrac{1}{k}\omega_0 L_f \dot{I}_{Lf\_kh} = 0 \\ jk\omega_0 M \dot{I}_{1\_kh} - j\omega_0 L_2\left(k - \dfrac{1}{k}\right)\dot{I}_{2\_kh} = \dfrac{2\sqrt{2}}{k\pi} V_{\text{out}} \end{cases} \tag{7.14}$$

By solving the first equation of (7.13) and based on $\omega_0^2 L_f C_f = 1$, one can get the expression for $\dot{I}_{Lf\_kh}$

$$\dot{I}_{Lf\_kh} = \frac{1}{1-k^2}(\dot{I}_{1\_kh} + j\frac{2\sqrt{2}V_{\text{in}}}{\pi\omega_0 L_f}). \tag{7.15}$$

Substituting (7.15) into the second equation of (7.13) and based on $\omega_0^2(L_1 - L_f)C_1 = 1$, (7.16) can be derived as follows.

$$\dot{I}_{2\_kh} = j\frac{2\sqrt{2}V_{\text{in}}}{k^2(1-k^2)\omega_0 M\pi} + [\frac{(k^2-1)}{k}L_1 + \frac{1}{k(1-k^2)}L_f]\cdot\frac{\dot{I}_{1\_kh}}{kM}. \tag{7.16}$$

In (7.16), since the ratio between $\frac{(k^2-1)}{k}L_1$ and $\frac{1}{k(1-k^2)}L_f$ is

$$\text{ratio} = -\frac{L_1}{L_f}(k^2-1)^2 = -\frac{G_v L_1(k^2-1)^2}{M} = -\frac{G_v}{k_{\text{cp}}}\cdot\sqrt{\frac{L_1}{L_2}}\cdot(k^2-1)^2, \tag{7.17}$$

where k_{cp} is the coupling coefficient, which is defined as $k_{\text{cp}} = \frac{M}{\sqrt{L_1 L_2}}$. This ratio in a practical LCC-S compensated WPT system is usually much larger than 1. For example, suppose $0.5 \le G_v \le 2$, $0.1 \le k_{\text{cp}} \le 0.5$, and the coil self inductances are close to each other [31], [32], then this ratio's absolute value is larger than 64. Therefore, the item of $\frac{1}{k(1-k^2)}L_f$ is neglected, (7.16) can be approximated by (7.18)

$$\dot{I}_{2\_kh} \approx j\frac{2\sqrt{2}V_{\text{in}}}{k^2(1-k^2)\omega_0 M\pi} + \frac{(k^2-1)L_1}{k^2 M}\dot{I}_{1\_kh}. \tag{7.18}$$

Substituting (7.18) into the third equation of (7.13), the expression for $\dot{I}_{1\_kh}$ can be derived as

$$\dot{I}_{1\_kh} = -j\frac{2\sqrt{2}}{\pi}\cdot\frac{L_2 V_{\text{in}} + k^2 M V_{\text{out}}}{k^4\omega_0 M^2 - \omega_0 L_1 L_2(k^2-1)^2}. \tag{7.19}$$

Since $k^2 - 1 \approx k^2$, and therefore, (7.19) can be approximated by (7.20) as follows:

$$\dot{I}_{1\_kh} \approx j\frac{2\sqrt{2}}{\pi}\cdot\frac{L_2 V_{\text{in}} + k^2 M V_{\text{out}}}{k^4\omega_0(L_1 L_2 - M^2)}. \tag{7.20}$$

Substituting (7.20) to (7.15), $\dot{I}_{Lf\_kh}$ can be expressed as follows

$$\dot{I}_{Lf\_kh} = -j\frac{2\sqrt{2}}{\pi}\cdot\frac{1}{k^2}[\frac{L_2 V_{\text{in}} + k^2 M V_{\text{out}}}{k^4\omega_0(L_1 L_2 - M^2)} + \frac{V_{\text{in}}}{\omega_0 L_f}]. \tag{7.21}$$

By further checking the expression for (7.21), since $\frac{1}{\omega_0 L_f} \gg \frac{L_2}{k^4\omega_0(L_1 L_2 - M^2)}$, which can be explained as follows. The ratio between these two coefficients is

$$\text{ratio} = \frac{k^4(L_1 L_2 - M^2)}{L_2 L_f} = \frac{k^4 G_v(1-k_{\text{cp}}^2)}{k_{\text{cp}}}\cdot\sqrt{\frac{L_1}{L_2}}. \tag{7.22}$$

Suppose $0.5 \le G_v \le 2$, $0.1 \le k_{cp} \le 0.5$, and the coil self inductances are close to each other [31], [32], this ratio will be larger than 60. So, compared with $\frac{1}{\omega_0 L_f}$, $\frac{L_2}{k^4\omega_0(L_1L_2-M^2)}$ can be neglected. Therefore, $\dot{I}_{Lf\_kh}$ is approximated by (7.23)

$$\dot{I}_{Lf\_kh} \approx -j\frac{2\sqrt{2}}{\pi}\cdot\left[\frac{V_{in}}{k^2\omega_0 L_f}+\frac{MV_{out}}{k^4\omega_0(L_1L_2-M^2)}\right]. \tag{7.23}$$

Substituting (7.20) to (7.18), $\dot{I}_{2\_kh}$ can be expressed as follows

$$\dot{I}_{2\_kh} = j\frac{2\sqrt{2}}{\pi}\cdot\frac{MV_{in}+k^2L_1V_{out}}{k^4\omega_0(L_1L_2-M^2)}. \tag{7.24}$$

As a summary, the high-order harmonic currents of $\dot{I}_{1\_kh}$, $\dot{I}_{2\_kh}$ and $\dot{I}_{Lf\_kh}$ are re-written as follows:

$$\begin{cases} \dot{I}_{1\_kh} = j\frac{2\sqrt{2}}{\pi}\cdot\frac{L_2V_{in}+k^2MV_{out}}{k^4\omega_0(L_1L_2-M^2)}, \\ \dot{I}_{2\_kh} = j\frac{2\sqrt{2}}{\pi}\cdot\frac{MV_{in}+k^2L_1V_{out}}{k^4\omega_0(L_1L_2-M^2)}, \\ \dot{I}_{Lf\_kh} = -j\frac{2\sqrt{2}}{\pi}\cdot\left[\frac{V_{in}}{k^2\omega_0 L_f}+\frac{MV_{out}}{k^4\omega_0(L_1L_2-M^2)}\right]. \end{cases} \tag{7.25}$$

According to (7.25), the corresponding time domain equations for the harmonic currents can be expressed as follows:

$$\begin{cases} i_{1\_kh}(t) = \sqrt{2}|\dot{I}_{1\_kh}|\sin(k\omega_0 t+\frac{\pi}{2}) = \frac{4}{\pi}\cdot\frac{L_2V_{in}+k^2MV_{out}}{k^4\omega_0(L_1L_2-M^2)}\sin(k\omega_0 t+\frac{\pi}{2}), \\ i_{2\_kh}(t) = \sqrt{2}|\dot{I}_{2\_kh}|\sin(k\omega_0 t+\frac{\pi}{2}) = \frac{4}{\pi}\cdot\frac{MV_{in}+k^2L_1V_{out}}{k^4\omega_0(L_1L_2-M^2)}\sin(k\omega_0 t+\frac{\pi}{2}), \\ i_{Lf\_kh}(t) = \sqrt{2}|\dot{I}_{Lf\_kh}|\sin(k\omega_0 t-\frac{\pi}{2}) = \frac{4}{\pi}\cdot\left[\frac{V_{in}}{k^2\omega_0 L_f}+\frac{MV_{out}}{k^4\omega_0(L_1L_2-M^2)}\right]\sin(k\omega_0 t-\frac{\pi}{2}). \end{cases} \tag{7.26}$$

Based on (7.26), the switching current caused by the high-order harmonics can be calculated with $t=\frac{T_0}{2}$. Substituting $t=\frac{T_0}{2}$ to (7.26), and add up all the harmonics with the equations in (7.27), one can get (7.28)

$$\begin{cases} \sin(\frac{k\omega_0 T_0}{2}+\frac{\pi}{2}) = \sin[(2n+1)\pi+\frac{\pi}{2}] = -1 \\ \sin(\frac{k\omega_0 T_0}{2}-\frac{\pi}{2}) = \sin[(2n+1)\pi-\frac{\pi}{2}] = 1 \\ \sum\frac{1}{k^2} = \sum_{n=1}^{\infty}\frac{1}{(2n+1)^2} = \frac{\pi^2}{8}-1 \\ \sum\frac{1}{k^4} = \sum_{n=1}^{\infty}\frac{1}{(2n+1)^4} = \frac{\pi^4}{96}-1. \end{cases} \tag{7.27}$$

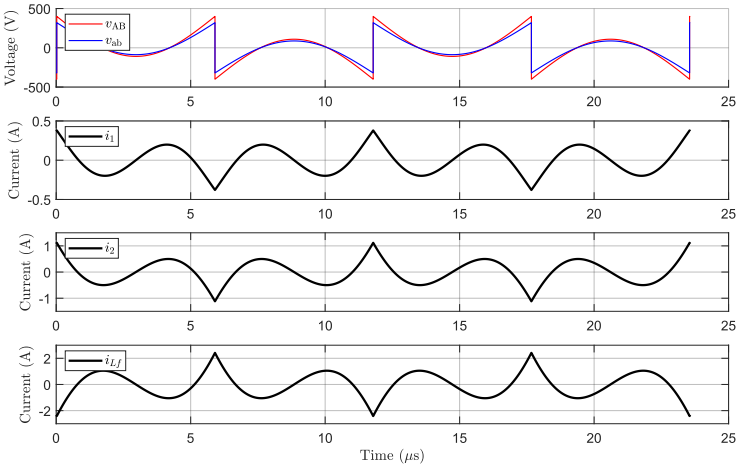


Figure 7.7: A simulation example showing the currents due to high-order harmonics, $L_1 = 300$ μH, $L_2 = 200$ μH, $M = 80$ μH, $L_f = 100$ μH, $f_0 = 85$ kHz, $V_{\text{in}} = 400$ V.

$$
\begin{cases}
\sum i_{1\_kh}(t=\dfrac{T_0}{2}) = -\dfrac{4}{\pi}\cdot(\xi_1+\xi_2) \\
\sum i_{2\_kh}(t=\dfrac{T_0}{2}) = -\dfrac{4}{\pi}\cdot(\xi_3+\xi_4) \\
\sum i_{Lf\_kh}(t=\dfrac{T_0}{2}) = \dfrac{4}{\pi}\cdot(\xi_5+\xi_6) \\
\xi_1 = (\dfrac{\pi^2}{8}-1)\cdot\dfrac{MV_{\text{out}}}{\omega_0(L_1L_2-M^2)}, \quad \xi_2 = (\dfrac{\pi^4}{96}-1)\cdot\dfrac{L_2V_{\text{in}}}{\omega_0(L_1L_2-M^2)} \\
\xi_3 = (\dfrac{\pi^2}{8}-1)\cdot\dfrac{L_1V_{\text{out}}}{\omega_0(L_1L_2-M^2)}, \quad \xi_4 = (\dfrac{\pi^4}{96}-1)\cdot\dfrac{MV_{\text{in}}}{\omega_0(L_1L_2-M^2)} \\
\xi_5 = (\dfrac{\pi^2}{8}-1)\cdot\dfrac{V_{\text{in}}}{\omega_0L_f}, \quad \xi_6 = (\dfrac{\pi^4}{96}-1)\cdot\dfrac{MV_{\text{out}}}{\omega_0(L_1L_2-M^2)}
\end{cases}
\tag{7.28}
$$

As it can be seen from (7.28), the sum of the high-order harmonics for i_{Lf} and i_2 will not change when the load varies. In fact, this is because during the derivation, the assumptions made are independent of the load. Figure 7.7 shows a simulation example of the currents due to the harmonics.

7.3.2 Simulation Verification of Derived High-order Harmonic Currents

First, the rms values of the harmonic current are verified. The parameters of the simulation example are: $L_1 = 300$ μH, $L_2 = 200$ μH, $M = 80$ μH, $L_f = 100$ μH, $V_{\text{in}} = 400$ V, $f_0 = 85$ kHz. The capacitor values of C_1, C_2 and C_f are selected based on (7.2). So, the output voltage V_{out} is 320 V. The circuit for simulation is shown in Figure 7.8. Two 10mΩ damping resistors are used to eliminate the influence due to initial conditions. The time domain equations

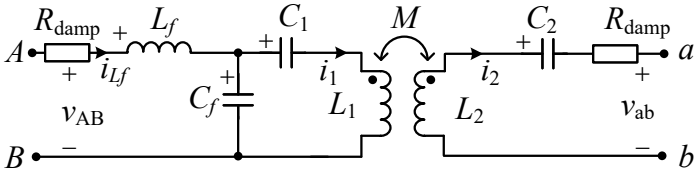


Figure 7.8: Circuit for simulation with two damping resistors.

Table 7.2: Summary of harmonic current simulation and calculation results based on Figure 7.8.

k-th harmonic	3	5	7	9
Calculated I_{1_kh} (A)	0.121	0.036	0.017	0.010
Calculated I_{2_kh} (A)	0.348	0.122	0.062	0.037
Calculated I_{Lf_kh} (A)	0.759	0.271	0.138	0.083
Simulated I_{1_kh} (A)	0.158	0.040	0.018	0.011
Simulated I_{2_kh} (A)	0.408	0.129	0.064	0.038
Simulated I_{Lf_kh} (A)	0.862	0.283	0.141	0.084

Table 7.3: Summary of calculated and simulated harmonic peak current at switching moment.

	$M = 40\ \mu$H $L_f = 80\ \mu$H	$M = 40\ \mu$H $L_f = 40\ \mu$H	$M = 40\ \mu$H $L_f = 32\ \mu$H	$M = 80\ \mu$H $L_f = 160\ \mu$H	$M = 80\ \mu$H $L_f = 80\ \mu$H	$M = 80\ \mu$H $L_f = 64\ \mu$H
Cal. $\sum i_{1\_kh}$ (A)	−0.124	−0.201	−0.239	−0.219	−0.385	−0.468
Cal. $\sum i_{2\_kh}$ (A)	−0.582	−1.154	−1.441	−0.645	−1.268	−1.580
Cal. $\sum i_{Lf\_kh}$ (A)	2.791	5.581	6.976	1.403	2.807	3.508
Sim. $\sum i_{1\_kh}$ (A)	−0.148	−0.236	−0.280	−0.263	−0.457	−0.554
Sim. $\sum i_{2\_kh}$ (A)	−0.628	−1.243	−1.551	−0.710	−1.390	−1.729
Sim. $\sum i_{Lf\_kh}$ (A)	2.993	5.980	7.473	1.512	3.017	3.770

for v_{AB} and v_{ab} are:

$$\begin{cases} v_{\text{AB}} = \dfrac{4V_{\text{in}}}{k\pi}\sin(k\omega_0 t) \\ v_{\text{ab}} = \dfrac{4V_{\text{out}}}{k\pi}\sin(k\omega_0 t). \end{cases} \tag{7.29}$$

For simulation setting, the maximum time step size is $t_{\text{maxstep}} = \dfrac{1}{kf_0 N_{\text{step}}}$ (N_{step} is the minimum simulated points in a switching period), and the relative tolerance is 1e-6. Herein, $N_{\text{step}} = 100$. As it can be seen from Table 7.2, the simulated results could match the calculated results well especially when k becomes larger.

Second, the sum of the harmonic current given in (7.28) is also simulated and compared with different values of L_f and M. The other parameters for simulation are: $L_1 = 300\ \mu$H, $L_2 = 200\ \mu$H, $V_{\text{in}} = 400$ V, $f_0 = 85$ kHz. The maximum time step is 2e-8 s (or 5e-8 s) and the relative tolerance is 1e-6. The results are summarized in Table 7.3. As it can be seen, the calculated results can also match the simulated ones well.

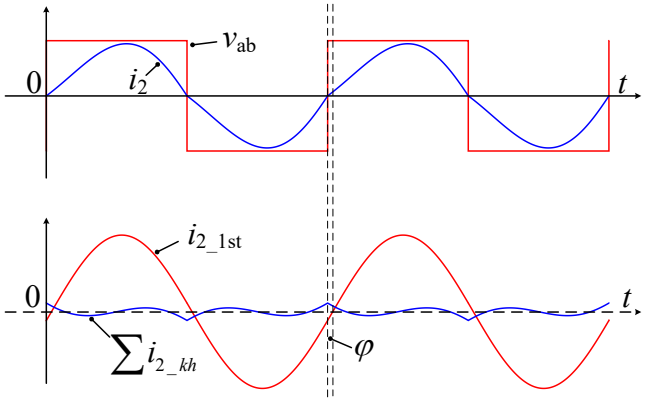


Figure 7.9: Effects from high-order harmonics on the secondary side, $i_2 = i_{2\_1st} + \sum i_{2\_kh}$.

7.3.3 Contribution to Switching Current Due to First Harmonic Current

Since the sign of v_{ab} is determined by i_2, and it consists of both first- and high-order harmonics, which is similar to double-sided LCC compensation network [108]. This phenomenon is illustrated in Figure 7.9. As it can be seen from Figure 7.9, there exists a phase shift of φ, by which i_{2_1st} lags behind v_{ab}. This value can be easily calculated by (7.30):

$$\varphi \approx \sin\varphi = -\frac{\sum i_{2\_kh}(t = \frac{T_0}{2})}{\sqrt{2}\cdot|\dot{I}_{2\_1st}|}. \tag{7.30}$$

In fact, this φ is also the reason for the phase shift between i_{Lf_1st} and v_{AB}. Based on this phase shift, an equivalent impedance of $Z_{ab} = |Z|e^{j\varphi}$ from secondary side is used for the FHA analysis. Figure 7.2(b) is re-drawn in Figure 7.10 for a fully compensated condition. Therefore, the input impedance of the circuit can be simply solved as $Z_{in} = \frac{X^2}{Z_{eq}} = \frac{X^2}{\omega_0^2 M^2} Z_{ab}$, which means the first-harmonic current i_{Lf_1st} also lags behind v_{AB} by a phase shift φ illustrated in Figure 7.11. So, the additional contribution of i_{Lf_1st} to the switching current is

$$I_{OFF\_Lf1st} = \sqrt{2}\cdot|\dot{I}_{Lf\_1st}|\sin\varphi \approx -\frac{M}{L_f}\cdot\sum i_{2\_kh}(t = \frac{T_0}{2}) \tag{7.31}$$

So, the switching current I_{OFF} is

$$I_{OFF} = I_{OFF\_Lf1st} + \sum i_{Lf\_kh}(t = \frac{T_0}{2}) = \frac{4}{\pi}\cdot\frac{M}{L_f}\cdot(\xi_3 + \xi_4) + \frac{4}{\pi}\cdot(\xi_5 + \xi_6), \tag{7.32}$$

where ξ_3, ξ_4, ξ_5 and ξ_6 are given in (7.28).

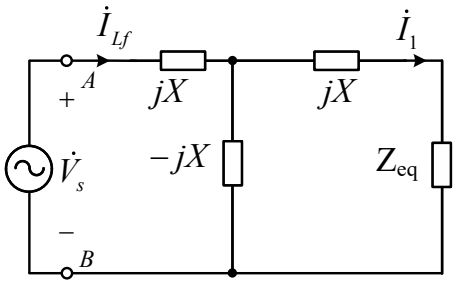


Figure 7.10: Equivalent circuit for calculating input impedance with $Z_{eq} = \frac{\omega_0^2 M^2}{Z_{ab}}$.

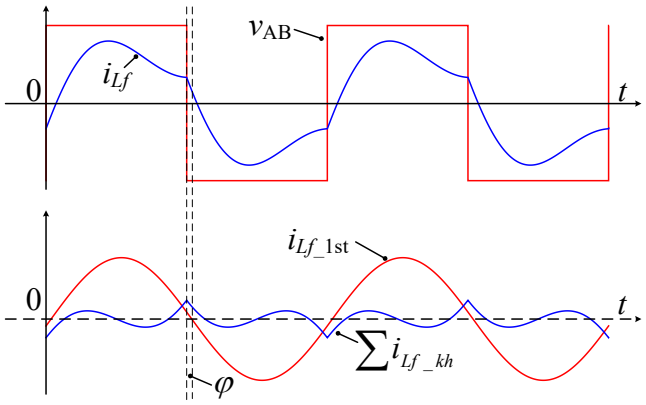


Figure 7.11: Effects from high-order harmonics on the primary side, $i_{Lf} = i_{Lf\_1st} + \sum i_{Lf\_kh}$.

Discussion on Equation (7.32)

Equation (7.32) can be further simplified. The ratio between ξ_3 and ξ_4 is

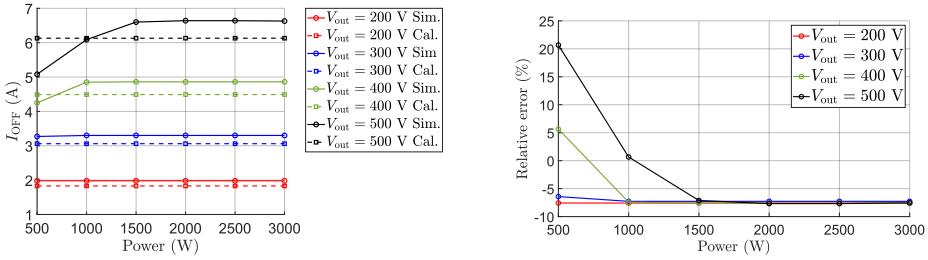
$$\text{ratio} = \frac{\xi_3}{\xi_4} = \frac{(\frac{\pi^2}{8} - 1)}{(\frac{\pi^4}{96} - 1)} \cdot \frac{L_1}{L_f} \approx 15.92 \frac{L_1}{L_f}. \tag{7.33}$$

In (7.33), L_1 is always larger than L_f for the LCC-S compensation with CV output. Therefore, ξ_4 can be neglected compared with ξ_3.

The ratio between ξ_5 and ξ_6 is

$$\text{ratio} = \frac{\xi_5}{\xi_6} = \frac{(\frac{\pi^2}{8} - 1)}{(\frac{\pi^4}{96} - 1)} \cdot \frac{(L_1 L_2 - M^2)}{M^2} \approx 15.92 \cdot (\frac{1}{k_{cp}^2} - 1). \tag{7.34}$$

And this value is also much larger than 1, so, ξ_6 can also be neglected compared with ξ_5.



(a) (b)

Figure 7.12: Simulated and calculated results of I_{OFF}, V_{in} = 300 V, M = 80 μH. (a) I_{OFF} value. (b) Relative error of I_{OFF}.

After simplification, (7.32) is simplified as follows

$$I_{OFF} \approx \frac{4}{\pi}\cdot(\frac{M}{L_f}\cdot\xi_3+\xi_5)=\frac{4}{\pi}\cdot(\frac{\pi^2}{8}-1)\cdot[\frac{1}{\omega_0 M}\cdot V_{out}+\frac{L_1}{\omega_0(L_1L_2-M^2)}\cdot\frac{V_{out}^2}{V_{in}}]. \tag{7.35}$$

From (7.35), it can be concluded that the switching current I_{OFF} will increase monotonically with the increasing of the output voltage, which phenomenon will be verified in the simulation section in this chapter. Comparing (7.35) and (7.11), it can be found that an extra item, namely, the right part of (7.35) is included to approach a more accurate value.

7

7.4 Simulation Verification

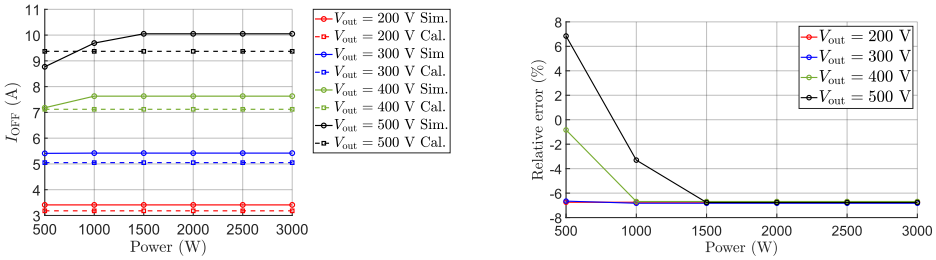
7.4.1 Simulation Verification of Switching Current

The figures below show the simulated results of switching current I_{OFF} under different values of M and L_f. The other parameters are: L_1 = 300 μH, L_2 = 200 μH, V_{in} = 400 V, f_0 = 85 kHz. The capacitor values of C_1, C_2 and C_f are selected based on (7.2). The output voltage will be simulated at 200 V, 300 V, 400 V and 500 V respectively based on the ratio of M and L_f. The power will vary between 500 W and 3000 W. The simulated circuit is based on Figure 7.1. The load resistance is calculated and selected as $R_L=\frac{V_{out}^2}{P_o}$. As for the selection of C_{out}, herein, it is selected as 200 μF. Since the voltage ripple is given by (7.36) in Appendix A of this chapter, the maximum voltage ripple will be around 93 mV at 200 V and 3 kW output, which value is negligible.

Figures 7.12 and 7.13 show the simulated and calculated I_{OFF} when V_{in} = 300 V, M = 80 μH and 40 μH, respectively. The relative error is defined as: $\varepsilon=\frac{I_{Cal.}-I_{sim.}}{I_{sim.}}\times 100\%$.

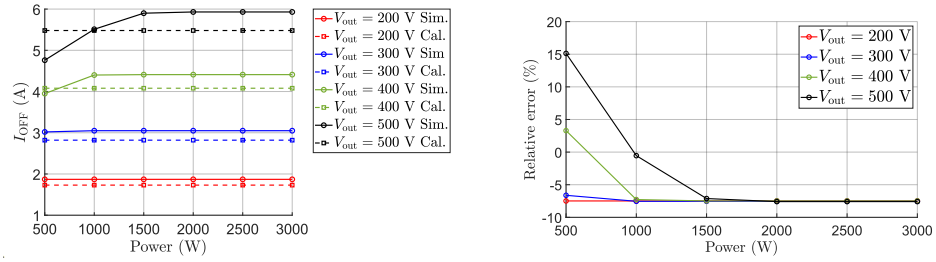
Figures 7.14 and 7.15 show the simulated and calculated I_{OFF} when V_{in} = 400 V, M = 80 μH and 40 μH, respectively.

Table 7.4 shows the two current components for I_{OFF} based on the previous analysis, namely, I_{OFF_Lf1st} and $\sum i_{Lf\_kh}$.



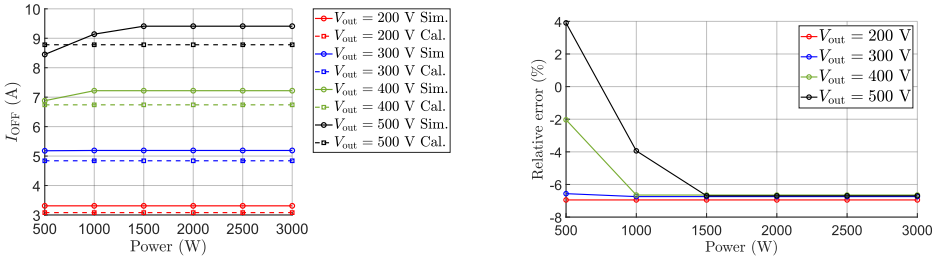
(a) (b)

Figure 7.13: Simulated and calculated results of I_{OFF}, $V_{in} = 300$ V, $M = 40$ μH. (a) I_{OFF} value. (b) Relative error of I_{OFF}.



(a) (b)

Figure 7.14: Simulated and calculated results of I_{OFF}, $V_{in} = 400$ V, $M = 80$ μH. (a) I_{OFF} value. (b) Relative error of I_{OFF}.



(a) (b)

Figure 7.15: Simulated and calculated results of I_{OFF}, $V_{in} = 400$ V, $M = 40$ μH. (a) I_{OFF} value. (b) Relative error of I_{OFF}.

7.4.2 Result Discussion

As it can be seen from the results in the Figures 7.12-7.15 and table 7.4, the calculated result of I_{OFF} in this chapter could match the simulated result well, which has a better prediction accuracy than the one mentioned in [110]. It is found from table 7.4 that under some cases

Table 7.4: Summary of two current components of I_{OFF_Lf1st} and $\sum i_{Lf\_kh}$, and the calculated I_{OFF} from [110].

V_{out} (V)		200	300	400	500
$V_{in} = 300$ V, $M = 80$ μH	I_{OFF_Lf1st} (A)	0.43	0.95	1.68	2.63
	$\sum i_{Lf\_kh}$ (A)	1.40	2.11	2.81	3.51
	I_{OFF} (A)	1.83	3.06	4.49	6.13
	I_{OFF} from [110] (A)	1.49	2.24	2.98	3.73
$V_{in} = 300$ V, $M = 40$ μH	I_{OFF_Lf1st} (A)	0.39	0.87	1.54	2.40
	$\sum i_{Lf\_kh}$ (A)	2.79	4.19	5.58	6.98
	I_{OFF} (A)	3.18	5.05	7.12	9.37
	I_{OFF} from [110] (A)	2.98	4.47	5.96	7.45
$V_{in} = 400$ V, $M = 80$ μH	I_{OFF_Lf1st} (A)	0.32	0.72	1.27	1.98
	$\sum i_{Lf\_kh}$ (A)	1.40	2.10	2.81	3.51
	I_{OFF} (A)	1.73	2.82	4.07	5.48
	I_{OFF} from [110] (A)	1.49	2.24	2.98	3.73
$V_{in} = 400$ V, $M = 40$ μH	I_{OFF_Lf1st} (A)	0.29	0.65	1.15	1.80
	$\sum i_{Lf\_kh}$ (A)	2.79	4.19	5.58	6.98
	I_{OFF} (A)	3.08	4.84	6.74	8.78
	I_{OFF} from [110] (A)	2.98	4.47	5.96	7.45

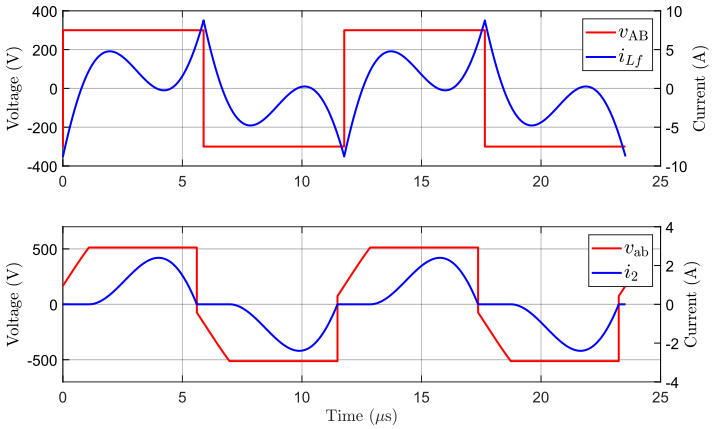


Figure 7.16: Corresponding waveforms when the secondary side current i_2 becomes discontinuous.

the contribution from first-harmonic of i_{Lf} on I_{OFF} is considerable, which is not mentioned and neglected in [110]. In [110], it is believed that for a fully compensated LCC-S based WPT system, the switching current only consists of high-order harmonics.

With a further check on Figures 7.12-7.15, the relative error is more obvious in light load condition, that is because the secondary side current becomes discontinuous when the load decreases, and therefore, the assumptions made in Section 7.3 are not valid. For example, Figure 7.16 shows the simulated result when the secondary side current is discontinuous. As it can be seen from Figure 7.16, the voltage of v_{ab} is not square wave output.

7.5 Conclusion and Future Work

In this chapter, the switching current in a fully compensated LCC-S based WPT system is investigated and modeled considering harmonics from both primary and secondary side under ideal conditions. Newly derived closed form equations provide accurate predictions of the switching current under various working conditions, which could bring new inspirations to future readers.

However, it has to be pointed out that the analysis in this chapter is based on the assumption that the primary side voltage v_{AB} and secondary side voltage v_{ab} are in phase. Although this claim is correct with FHA analysis and obvious from simulation, but it seems rather complicated to be proved when secondary side diode rectifier is included, which could be further investigated.

7.6 Appendix A

Figure 7.17 shows the voltage ripple calculation method on output capacitor C_{out} according to Figure 7.1. Considering the charge accumulated in the shaded area, the peak-to-peak

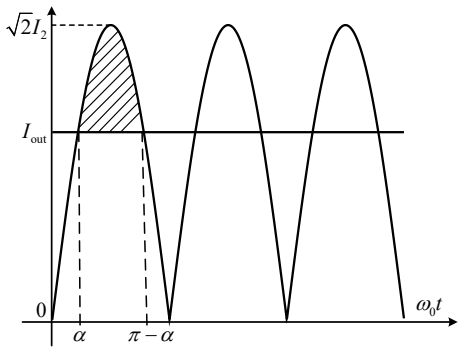


Figure 7.17: Output voltage ripple calculation on C_{out}.

voltage ripple can be expressed by (7.36), where $\alpha = \arcsin\frac{I_{out}}{\sqrt{2}I_2}$, $I_{out} = \frac{2\sqrt{2}I_2}{\pi}$.

$$\begin{aligned}\Delta V_{pp} &= \frac{1}{\omega_0 C_{out}}\int_{\alpha}^{\pi-\alpha}(\sqrt{2}I_2\sin\beta - I_{out})d\beta \\ &= \frac{2\sqrt{2I_2^2 - I_{out}^2}}{\omega_0 C_{out}} - \frac{I_{out}}{\omega_0 C_{out}}(\pi - 2\arcsin\frac{I_{out}}{\sqrt{2}I_2}) \\ &= [\sqrt{\pi^2-4} - \pi + 2\arcsin(\frac{2}{\pi})]\cdot\frac{I_{out}}{\omega_0 C_{out}} \approx 0.6613\frac{I_{out}}{\omega_0 C_{out}}.\end{aligned} \tag{7.36}$$

7.7 Appendix B

Equation (7.11) is derived based on the integration method under FHA analysis, which can be derived based on superposition theorem. The analysis is based on Figure 7.5. For the first-harmonic component in a fully compensated WPT system, switching current is zero.

In [108], it is claimed that the interaction of high-order harmonics between the primary and secondary sides for double-sided LCC network can be neglected without explanation, and this will be addressed herein for an LCC-S network.

For a k-th harmonic, the reflected impedance to the primary side is

$$Z_{\text{eq}} = \frac{k^2\omega_0^2M^2}{jk\omega_0L_2 + \frac{1}{jk\omega_0C_2} + R_{\text{ac}}} = \frac{k^2\omega_0^2M^2}{j\omega_0L_2(k-\frac{1}{k}) + R_{\text{ac}}}. \tag{7.37}$$

According to Figure 7.2(b), the impedance through C_f branch is

$$Z_{Cf} = \frac{1}{jk\omega_0C_f} = \frac{\omega_0L_f}{jk}. \tag{7.38}$$

The impedance through L_1 (also C_1) branch is

$$Z_{L1C1} = jk\omega_0L_1 + \frac{1}{jk\omega_0C_1} + Z_{eq} = jk\omega_0L_1 - j\frac{\omega_0(L_1-L_f)}{k} + \frac{k^2\omega_0^2M^2}{j\omega_0L_2(k-\frac{1}{k}) + R_{\text{ac}}}. \tag{7.39}$$

It will be shown that the magnitude of Z_{Cf} is much smaller than Z_{L1C1}, and therefore, the L_1C_1 branch can be neglected for simplified analysis. Herein, only considering the imaginary part of Z_{L1C1} since the real part will only increase the total magnitude, and then, one can get

$$\begin{aligned}\text{Im}(Z_{L1C1}) &= k\omega_0L_1 - \frac{\omega_0(L_1-L_f)}{k} - \frac{\omega_0^3k^2M^2L_2(k-\frac{1}{k})}{\omega_0^2L_2^2(k-\frac{1}{k})^2 + R_{\text{ac}}^2} \\ &> k\omega_0L_1 - \frac{\omega_0(L_1-L_f)}{k} - \frac{\omega_0k^2M^2}{L_2(k-\frac{1}{k})} > \omega_0L_1(k - \frac{1}{k} - \frac{k^2k_{\text{cp}}^2}{k-\frac{1}{k}}).\end{aligned} \tag{7.40}$$

Herein, $k_{\text{cp}} = \frac{M}{\sqrt{L_1L_2}}$. It is easy to prove that $\text{Im}(Z_{L1C1})$ is larger than zero, which simply is

$$\text{Im}(Z_{L1C1}) > \omega_0L_1(k - \frac{1}{k} - \frac{k^2k_{\text{cp}}^2}{k-\frac{1}{k}}) = \omega_0L_1 \cdot \frac{[(1-k_{\text{cp}}^2)k^2 - 2]\cdot k^2 + 1}{k(k^2-1)}. \tag{7.41}$$

Since the coupling coefficient k_{cp} is typically less than 0.5, so, (7.41) is obviously larger than 0. The ratio between $\text{Im}(Z_{L1C1})$ and $|Z_{Cf}|$ is

$$\begin{aligned}\text{ratio} = \frac{\text{Im}(Z_{L1C1})}{|Z_{Cf}|} > \frac{L_1}{L_f}\cdot k\cdot(k - \frac{1}{k} - \frac{k_{\text{cp}}^2k^2}{k-\frac{1}{k}}) &= \frac{G_v}{k_{\text{cp}}}\cdot\sqrt{\frac{L_1}{L_2}}\cdot k(k - \frac{1}{k} - \frac{k_{\text{cp}}^2k^2}{k-\frac{1}{k}}) \\ &\approx \frac{G_v}{k_{\text{cp}}}\cdot\sqrt{\frac{L_1}{L_2}}\cdot(1-k_{\text{cp}}^2)k^2.\end{aligned} \tag{7.42}$$

For high-order harmonics, the value of the ratio is much larger than 1, so, the impedance of the L_1C_1 branch is much larger than the C_f branch. For example, suppose $0.5 \le G_v \le 2$, $0.1 \le k_{\text{cp}} \le 0.5$, and the coil self inductances are close to each other, and then, the minimum

value of the ratio is 6.75. So, for simplified analysis, this branch is neglected. Therefore, the high-order harmonics of i_{Lf} is

$$\dot{I}_{Lf\_kh} \approx \frac{\frac{2\sqrt{2}}{k\pi} V_{\text{in}}}{jk\omega_0 L_f + \frac{1}{jk\omega_0 C_f}} \approx -j\frac{2\sqrt{2}V_{\text{in}}}{\pi} \cdot \frac{1}{k^2\omega_0 L_f}. \tag{7.43}$$

Its time domain equation is

$$i_{Lf\_kh} = \frac{4V_{\text{in}}}{\pi} \cdot \frac{1}{k^2\omega_0 L_f} \sin(k\omega_0 t - \frac{\pi}{2}). \tag{7.44}$$

At the instant of $\frac{T_0}{2}$, $i_{Lf\_kh}(t = \frac{T_0}{2}) = \frac{4V_{\text{in}}}{\pi} \cdot \frac{1}{k^2\omega_0 L_f}$. The summation of all the high-order harmonics is

$$\sum i_{Lf\_kh}(t = \frac{T_0}{2}) = (\frac{\pi^2}{8} - 1) \cdot \frac{4}{\pi} \cdot \frac{V_{\text{in}}}{\omega_0 L_f}. \tag{7.45}$$

Interestingly, (7.45) is the same as (7.11).

8

Conclusion

The objective of this thesis was to study and research the promising topology of a WPT charging system, and optimization on the operation of its power electronic conversion stages for high efficiency electric vehicle charging over a wide operating range. The selection on the WPT system and power converter topology was answered through a literature review on state-of-the-art WPT charging system presented in Chapter 2. It has been found that non-isolated dc-dc converters have been widely adopted in a WPT system, and it can be placed on the primary side, the secondary side, or both sides. In this thesis, a WPT charging system featuring LCC-S compensation and a back-end FSBB converter was chosen as the research object. Compared with S-S compensation featuring constant current output, LCC-S compensated WPT system features inherent built-in safety advantage in terms of connecting a back-end dc-dc converter because of its constant voltage output.

In the following Chapters 3 and 5, the soft-switching, more precisely, zero-voltage switching modulation technique was researched through variable-frequency strategy for the FSBB converter. In Chapter 3, the operation of the FSBB converter was divided into three operating modes according to the voltage gain, i.e., buck-, boost- and buck-boost-type mode. TCM-ZVS modulation was adopted for buck- and boost-type mode while three-segment inductor current mode modulation was adopted for the buck-boost-type mode. Due to the sudden change of the switching frequency during mode transition, which may cause excessive oscillation of the inductor current in the converter, in Chapter 5, the three-segment inductor current mode modulation was extended to the whole operating range for the purpose of achieving a smooth transition at the unit voltage gain boundary. Since the reverse switching current through the inductor is the key to realize ZVS for some certain switches with TCM-ZVS modulation, so the influence from the parasitic resistance on this switching current value was studied in a voltage-mode control for buck, boost and buck-boost converters respectively in Chapter 4.

On top of that, Chapters 6 and 7 studied the compensation networks in a WPT system. More precisely, Chapter 6 studied electrical stresses on components in two commonly adopted S-S and LCC-S compensation networks. An improved peak voltage calculation method was introduced when the front-end H-bridge inverter operates at a natural resonant frequency with a square wave output voltage. Compared with S-S compensation, the current

distortion phenomenon is more obvious in LCC-S compensated WPT system, which is closely related to the ZVS of the switches in the front-end H-bridge inverter, so Chapter 7 investigated the switching current in a fully compensated LCC-S based WPT system by considering harmonics from both the primary and secondary sides under ideal conditions.

The research objective has been partitioned into six research questions, and the main conclusions of each question, and finally, future recommendations are given.

8.1 Research Questions

Question 1: What is the state-of-the-art topology of a WPT charging system ?

In Chapter 2, a comprehensive literature review on the WPT charging system was presented. According to this review, it can be found that the overall WPT system typically has several power conversion stages, which, however, has no fixed conclusion on the optimal power conversion configuration and topology selection except the dc-ac-dc conversion stage involved in the coil. However, the common point that is easy to see is the wide adoption of non-isolated dc-dc converters in wireless charging system, and this is because of the following reasons: 1) The WPT coils already provide electrical isolation between primary and secondary sides, so only non-isolated dc-dc converters are required; 2) To enable wireless power transfer efficiently over a wide operating range, the bus voltage of the primary side, the secondary side, or both sides need to be adjusted. So, a dc-dc converter is a suitable candidate to achieve this purpose.

In this thesis, the FSBB converter has been selected as the most promising topology for dc-dc conversion since it has both voltage step-up and step-down functions. As for the promising compensation network, LCC-S compensation featuring CV output was preferred compared with S-S compensation network because of its safety advantage. Since a back-end power regulation can avoid the communication between charging pads, so, LCC-S based WPT charging system with a back-end FSBB converter is the preferred system topology to be researched in this thesis.

Question 2: How to optimize the operation of the FSBB converter such that it can operate efficiently over a wide operational range ?

Although hard-switched SiC MOSFET-based dc-dc converter could also possibly achieve power efficiency larger than 99%, the switching losses cannot be eliminated. With increasing requirements for power density and efficiency, ultra-high-frequency converters can only be built through soft-switching techniques to achieve acceptable efficiency.

In Chapter 3, the soft-switching modulation technique of the FSBB converter was researched. More precisely, variable-frequency ZVS modulation was studied. When the input and output voltages differ greatly, simply, TCM-ZVS modulation can be used. Although TCM-ZVS modulation can also be used when the voltage gain is close to unit, however, it results in large inductor rms current causing large conduction losses. In order to find the most suitable modulation strategy in this mode, all the possible modulation cases were studied through phase shift between the two half bridges in a full switching period with a new set of derived closed-form equations, which can be used to calculate circuit parameters, such as frequency and inductor rms current etc. Three-segment inductor current mode modulation was selected as the optimal modulation technique in this mode in terms of

inductor rms current reduction and ease of operation. A 300–600 V input, 400 V output, 3 kW laboratory prototype was built to prove and verify the proposed concepts. The converter was tested over a wide power range from 10% to full rated load. The measured efficiency was always higher than 99%, i.e., between 99.2% and 99.6%, from 1 to 3 kW for all the considered input voltages.

Question 3: How the parasitic resistances affect the reverse switching current in a dc-dc converter featuring voltage-mode TCM-ZVS modulation ?

TCM-ZVS modulation is a widely adopted method in power electronic converters to achieve soft switching. The key to achieve ZVS for both switches in a bidirectional buck, boost and buck-boost converters is to have a reverse switching current through the inductor during the switching interval before turning on the desired switch. Due to the detection challenge of switching current operating at a high frequency, voltage-mode TCM-ZVS modulation can be used, where closed-form equations for the switching frequency can be easily derived. In an ideal case without considering losses and dead time, this switching current maintains a constant value, so the ZVS condition is always satisfied, however, this reverse switching current value needs to be rethought in non-ideal situations because the decrease of this current (absolute value) could cause possible ZVS loss.

In Chapter 4, this switching current was rethought considering parasitic resistances presented in the MOSFETs and inductor. Universal closed-form equations of the modified duty cycle and switching current were derived to predict this switching current under different operating conditions for buck, boost and buck-boost converters, respectively. It is found by theoretical calculation, simulation and experimentation that the parasitic resistance could have a different impact on this switching current under buck and boost mode operations even with the same voltage and power adopted by this thesis. More specifically, the phenomenon of unexpected ZVS loss is more obvious in boost mode as power increases. The operating voltage and power range of the built prototype for testing were from 100 V to 400 V, and 300 W to 1 kW, respectively.

Question 4: How to operate the FSBB converter with a smooth transition between step-up and step-down mode without compromising efficiency ?

Following the second research question, where a three-mode variable-frequency ZVS modulation was utilized to operate the FSBB converter, during mode transitions, the switching frequency will have an abrupt change with this method, which may cause large fluctuations in inductor current, and this oscillation could potentially affect the stable operation of the converter.

In Chapter 5, an improved single mode variable-frequency ZVS modulation was developed. In this modulation method, the control variables of duty cycle and switching frequency are continuous at the unit voltage gain boundary. Basically, the three-segment inductor current mode modulation method was extended to the whole operational range. By fixing the duty cycle for the switch in the buck-type or boost-type half-bridge circuit, and controlling the duty cycle of the switch in the other half-bridge circuit, the FSBB converter can realize a smooth transition at the unit voltage gain boundary. Compared with TCM-ZVS modulation, the rms value of the inductor current is slightly larger. Since ZVS was also achieved over a wide operational range, so the efficiency performance of

this modulation strategy was also high. A simple closed-loop control method without current detection was proposed accordingly. Different from previous research focusing on modulation techniques, Chapter 5 also provided the selection guidelines for the input and output capacitors based on a comprehensive and detailed study on the capacitor voltage ripples. A laboratory prototype of an FSBB converter was built and tested to verify the proposed concepts with an input voltage of 250−600 V, output voltage of 400 V and output power of 250−2500 W.

Question 5: How to accurately determine the electrical stresses of the compensation components in an S-S and LCC-S compensated WPT system ?

For a WPT system, S-S and LCC-S compensations are the two most widely used compensation networks due to their simplicity and high efficiency performance. S-S compensation features CC output while LCC-S compensation features CV output. To accurately determine the electrical stresses of the compensation components is the first step to design a reliable WPT system. It is found that the peak voltage calculation is not accurate enough for certain components when applying FHA method to the equivalent ac circuit.

In Chapter 6, the voltage and current stresses of the compensation components were studied at 3 kW power level with the front-end H-bridge inverter operating at natural resonant frequency featuring a square wave output voltage. The power of 3 kW is the WPT1 power level suggested by SAE J2954. Compared with simulation based on mutual inductance model, the calculation of the current rms value was quite accurate based on FHA method. However, the calculated peak voltage of the primary coil and secondary coil in S-S compensation, and the calculated peak voltage of the input resonant inductor and secondary coil in LCC-S compensation contained large error compared with simulated results. Due to the high accuracy of the rms current calculation, a more accurate peak voltage calculation method was proposed based on Kirchhoff's voltage law considering the voltage across the related compensation capacitors. The newly derived closed-form equations for peak voltage calculation were proved to be more accurate by both simulation and experiments.

Question 6: How to model current distortion of the input resonant inductor in an LCC-S compensated WPT system ?

Because of the constant voltage output property of LCC-S compensated WPT system, it has inherent built-in safety advantages in terms of connecting a back-end dc-dc converter compared with S-S compensated WPT system. However, the current distortion phenomenon is also more obvious in an LCC-S compensated WPT system due to the introduction of an extra LC resonant tank, and the current through the input resonant inductor at switching moment is closely related to the ZVS of the switches in the front-end H-bridge inverter.

In Chapter 7, by considering the secondary side diode-bridge rectifier as an equivalent resistance or by disconnecting the primary coil branch when considering high-order harmonics for a fully compensated LCC-S based WPT system, both of these two methods would lead to the same switching current value, which still contained a large error compared with simulated results. In order to improve the accuracy of the calculated results, the high-

order harmonics from the secondary side were also considered. Unexpectedly, according to the analysis, the first-harmonic current through the input resonant inductor also contributes to the switching current even in a fully compensated WPT system. The new modeling method has shown an improved prediction of the switching current proved by simulation.

However, it has to be pointed out that the analysis in Chapter 7 was based on the assumption that the primary and secondary side square wave voltages are in phase. Although this claim is in line with FHA analysis and is obvious from simulation, it seems rather complicated to be proved, which requires further discussion.

8.2 Future Work

Several recommendations are presented here for the future work following the research results in this thesis, and they are as follows:

- In this thesis, variable-frequency ZVS modulation strategies were researched for the FSBB converter, which has achieved the goal of high efficiency operation of this converter over a wide operating range. However, the frequency selection was still quite conservative, which fell into the range of 20−160 kHz. However, a 6.6 kW 550 kHz full-bridge LLC dc-dc converter with SiC MOSFETs was already developed by Wolfspeed in 2019. The input voltage of the converter was 380–420 V, output voltage was 400 V and peak efficiency was 98% [111]. Therefore, how to operate FSBB converter with a high or even very high frequency efficiently over a wide operating range can be a promising research topic.
- In Chapter 7, it is mentioned that the current distortion modeling for a fully compensated LCC-S based WPT system was based on the assumption that the square wave voltages on the primary and secondary sides are in phase. This assumption seems quite intuitive, however, it lacks strict proof, which can be future studied.
- Finally, although comprehensive and detailed research on the FSBB converter and LCC-S compensation network has been conducted in this thesis, the system-level optimization and operation of the WPT system based on these two subsystems can be considered as a future integrated work.

Acknowledgments

Finally, it has come to the acknowledgement part. I thought I would be excited about this moment, but in fact, at this moment, my heart is as peaceful as a calm lake.

Firstly, I would like to thank Prof. Pavol Bauer and Dr. Jianning Dong for giving me the opportunity to join DCE&S group as a PhD candidate. I feel lucky that I can become a member of this group and can get access to the DCE&S Lab equipped with a lot of advanced equipment, which makes practical work happen. I am also grateful for the financial support to me for buying prototype components and attending conferences. In addition, I would also like to show many thanks to both of you for your continuous support, guidance and encouragement, patient discussion and feedback throughout my PhD journey. Meanwhile, I would also like to thank Dr. Thiago Batista Soeiro for the guidance in the early stage of my PhD, which ensures that my research is on the right track and not going astray. I also deeply appreciate your careful and timely feedback on my papers and your selfless sharing on the knowledge of power electronics.

For a PhD to successfully graduate, their colleagues play a vital role. Sachin Yadav, we started our PhD contract on the same date, and more coincidently, we both share the same passion towards hardware. You are a real pioneer in our group in terms of making PCBs among our generation. We cannot guarantee that the board can work when we have built it, since failure is the norm, so we cherish the difficulty of success even more. I also want to thank your purchase of the FLIR thermal camera, which makes the thermal measurement more professional. Lu Wang, I appreciate your patience and empathy, which you have shown not only in front of the senior but also in front of the junior, meanwhile, I am also inspired by our discussions from time to time, especially your thoughts on the meaning of life. I believe both of us have experienced struggling during this journey. Thanks also to Tianming Luo and Yang Wu for booking the basketball court, where we used to play a lot of basketball and have fun together. To Junjie Xiao, I appreciate your kindness, frankness, and also approachability to me. Dhanashree, Djurre and Adnan Ahmad, you guys made our office a perfect place to work in, thank you for that. Thanks also to Fan Yang and Jundong Wang, who later joined the office, and brought different types of tea and professional tea-making equipment to our office. I would also like to thank the technicians in our group especially Mladen Gagic for your patient and selfless help when I just started my experimental work in the lab. Your help helped me get started with the experimental work faster. I still remember those, thanks. I also want to thank all the technicians including Bart Roodenburg, Joris Koeners, Harrie Olsthoorn, Mladen, Hitesh Dialani for helping me order components efficiently. Discussions during lab coffee breaks with Miad Ahmadi, Siddhesh Shinde, Sachin, Mladen, Hitesh etc. is always fun. I also want to thank Sharmila for providing administrative support to all PhD candidates.

I also want to thank the people related with WPT group, including Calvin Riekerk, Francesca Grazian, Wenli Shi, Gangwei Zhu, Zichen Deng, Shibo Zhang etc, and also Kun-Che Ho, who was an exchange PhD student in the early time. I am also grateful for the

patient WPT experimental demonstration by Francesca, and the trust you let Pengcheng Ye and I use your setup. Zian Huang and Pengcheng Ye, thanks for the trust on me and choosing to work with me on your master thesis. To Haoyuan Yu, thank you for the sincere suggestions and discussions we had on career choices. I also want to thank Zhihong Zhang for the discussions we had from time to time, which reminded me that it was actually not easy to study step by step from our hometown to where I am now.

DCE&S is a group of outstanding talents who strive to contribute to research academia with their own efforts and wisdom. Thanks to the rest of the colleagues including Xuliang, Yunhe, Yun Chen, Yongpeng, Heshi, Yawen, Zhengzhao, Ruijun, Reza, Faezeh, Robin, Mischa, Farshid, Marco, Ibrahim, Koen, Alvaro, Sohrab, Mohamad, Zian, Gautham, Aditya, Laura, Sebastian, Hani, Joel, Rohan, Bagas, Gautam, Manfredo, Leila, Dario, Istvan, Felipe, Nikos, Carina, Margo, Julian, Sourabh, Abdourahim and others in this group for creating a friendly working atmosphere.

When I look back, I have been studying and working at TU Delft for more than six years, including two years of my master's program. Being able to study and work in such a beautiful and modern campus, it should be realized that this kind of opportunity is rare. To the country of China where I come from, I appreciate the education that I received back there, as it helped me laid solid foundation for my further research and study. I also want to show my special and sincere thanks to my family including my parents, my sister and my wife for the unconditional support, care and love, who makes me realize that I am not alone in this world.

Last but not least, I would also like to take a moment to thank myself for the courage, patience, dedication, and persistence that have been integral in completing this thesis. There were many moments when I was afraid of uncertainties, but the dedication to pushing through challenges, learning from failures, and continuing despite setbacks has brought me to the completion of this thesis.

All in all, the end of every journey is the beginning of the next one, which is also true to this PhD journey. Cheers !

Guangyao YU
Delft, July 2025

Bibliography

References

[1] Paulo G Pereirinha, Manuela González, Isabel Carrilero, David Anseán, Jorge Alonso, and Juan C Viera. Main trends and challenges in road transportation electrification. *Transportation research procedia*, 33:235–242, 2018.

[2] Roman Bosshard and Johann W Kolar. Inductive power transfer for electric vehicle charging: Technical challenges and tradeoffs. *IEEE Power Electronics Magazine*, 3(3):22–30, 2016.

[3] Andre Kurs, Aristeidis Karalis, Robert Moffatt, John D Joannopoulos, Peter Fisher, and Marin Soljacic. Wireless power transfer via strongly coupled magnetic resonances. *science*, 317(5834):83–86, 2007.

[4] Muhammad Amjad, Muhammad Farooq-i Azam, Qiang Ni, Mianxiong Dong, and Ejaz Ahmad Ansari. Wireless charging systems for electric vehicles. *Renewable and Sustainable Energy Reviews*, 167:112730, 2022.

[5] Chris Clearman et al. Exploring the evolution and optimization of wireless power transfer. Texas Instruments, 2018.

[6] Francesca Grazian, Thiago Batista Soeiro, and Pavol Bauer. Design trade-offs between the coupled coils' inductance and the series-series compensation capacitance for ev wireless charging systems. In *2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, pages 270–276, 2022.

[7] Wenli Shi, Jianning Dong, Thiago Batista Soeiro, Calvin Riekerk, Francesca Grazian, Guangyao Yu, and Pavol Bauer. Design of a highly efficient 20-kw inductive power transfer system with improved misalignment performance. *IEEE Transactions on Transportation Electrification*, 8(2):2384–2399, 2022.

[8] Roman Bosshard and Johann W. Kolar. Multi-objective optimization of 50 kw/85 khz ipt system for public transport. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(4):1370–1382, 2016.

[9] Jaime Garnica, Raul A Chinga, and Jenshan Lin. Wireless power transmission: From far field to near field. *Proceedings of the IEEE*, 101(6):1321–1331, 2013.

[10] Jaegue Shin, Seungyong Shin, Yangsu Kim, Seungyoung Ahn, Seokhwan Lee, Guho Jung, Seong-Jeub Jeon, and Dong-Ho Cho. Design and implementation of shaped magnetic-resonance-based wireless power transfer system for roadway-powered moving electric vehicles. *IEEE Transactions on Industrial Electronics*, 61(3):1179–1192, 2014.

[11] Jae Hee Kim, Byung-Song Lee, Jun-Ho Lee, Seung-Hwan Lee, Chan-Bae Park, Shin-Myung Jung, Soo-Gil Lee, Kyung-Pyo Yi, and Jeihoon Baek. Development of 1-mw inductive power transfer system for a high-speed train. *IEEE Transactions on Industrial Electronics*, 62(10):6242–6250, 2015.

[12] Seung-Hwan Lee, Jae-Hee Kim, and Jun-Ho Lee. Development of a 60 khz, 180 kw, over 85% efficiency inductive power transfer system for a tram. *Energies*, 9(12):1075, 2016.

[13] Seung-Hwan Lee, Byung-Song Lee, and Jun-Ho Lee. A new design methodology for a 300-kw, low flux density, large air gap, online wireless power transfer system. *IEEE Transactions on Industry Applications*, 52(5):4234–4242, 2016.

[14] Tetsu Shijo, Kenichirou Ogawa, Masatoshi Suzuki, Yasuhiro Kanekiyo, Masaaki Ishida, and Shuichi Obayashi. Emi reduction technology in 85 khz band 44 kw wireless power transfer system for rapid contactless charging of electric bus. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–6, 2016.

[15] Akihisa Matsushita, Fumiaki Takeuchi, Shuichi Obayashi, Masaaki Ishida, and Tatsuro Abe. 85 khz band wireless charging system for ev or electric bus. In *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–7, 2018.

[16] Shuichi Obayashi, Tetsu Shijo, Masatoshi Suzuki, Fumi Moritsuka, Kenichirou Ogawa, Koji Ogura, Yasuhiro Kanekiyo, Masaaki Ishida, Toru Takanaka, Nobumitsu Tada, et al. 85 khz band 44 kw wireless rapid charging system for field test and public road operation of electric bus. *World Electric Vehicle Journal*, 10(2):26, 2019.

[17] Abubakar Uba Ibrahim, Wenxing Zhong, and Mark Dehong Xu. A 50-kw three-channel wireless power transfer system with low stray magnetic field. *IEEE Transactions on Power Electronics*, 36(9):9941–9954, 2021.

[18] Ganesh R. Nagendra, Grant A. Covic, and John T. Boys. Sizing of inductive power pads for dynamic charging of evs on ipt highways. *IEEE Transactions on Transportation Electrification*, 3(2):405–417, 2017.

[19] Roman Bosshard and Johann W. Kolar. All-sic 9.5 kw/dm3 on-board power electronics for 50 kw/85 khz automotive ipt system. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(1):419–431, 2017.

[20] Benriah Goeldi, Johannes Tritschler, and Stefan Reichert. Measurement results of a 22 kw bidirectional inductive charger. In *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, 2015.

[21] J. Tritschler, S. Reichert, and B. Goeldi. A practical investigation of a high power, bidirectional charging system for electric vehicles. In *2014 16th European Conference on Power Electronics and Applications*, pages 1–7, 2014.

[22] Marinus Petersen and Friedrich W. Fuchs. Design of a highly efficient inductive power transfer (ipt) system for low voltage applications. In *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, 2015.

[23] Jacopo Colussi, Alessandro La Ganga, Roberto Re, Paolo Guglielmi, and Eric Armando. 100 kw three-phase wireless charger for ev: Experimental validation adopting opposition method. *Energies*, 14(8):2113, 2021.

[24] Daniel E. Gaona, Chaoqiang Jiang, and Teng Long. Highly efficient 11.1-kw wireless power transfer utilizing nanocrystalline ribbon cores. *IEEE Transactions on Power Electronics*, 36(9):9955–9969, 2021.

[25] Veda P. Galigekere, Omer Onar, Jason Pries, Shenli Zou, Zhiqiang Wang, and Madhu Chinthavali. Sensitivity analysis of primary-side lcc and secondary-side series compensated wireless charging system. In *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 885–891, 2018.

[26] Omer C. Onar, Madhu Chinthavali, Steven L. Campbell, Larry E. Seiber, Cliff P. White, and Veda P. Galigekere. Modeling, simulation, and experimental verification of a 20-kw series-series wireless power transfer system for a toyota rav4 electric vehicle. In *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 874–880, 2018.

[27] Jason Pries, Veda Prakash Nagabhushana Galigekere, Omer C. Onar, and Gui-Jia Su. A 50-kw three-phase wireless power transfer system using bipolar windings and series resonant networks for rotating magnetic fields. *IEEE Transactions on Power Electronics*, 35(5):4500–4517, 2020.

[28] Mostak Mohammad, Omer C. Onar, Gui-Jia Su, Jason Pries, Veda Prakash Galigekere, Saeed Anwar, Erdem Asa, Jonathan Wilkins, Randy Wiles, Cliff P. White, and Larry E. Seiber. Bidirectional lcc–lcc-compensated 20-kw wireless power transfer system for medium-duty vehicle charging. *IEEE Transactions on Transportation Electrification*, 7(3):1205–1218, 2021.

[29] Reza Tavakoli and Zeljko Pantic. Analysis, design, and demonstration of a 25-kw dynamic wireless charging system for roadway electric vehicles. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 6(3):1378–1393, 2018.

[30] Reza Tavakoli and Zeljko Pantic. Dc modeling of an lcc resonant compensation network in wireless power transfer systems. In *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 6187–6193, 2018.

[31] SAE International. *Wireless Power Transfer for Light-Duty Plug-in/Electric Vehicles and Alignment Methodology*, October 2020. Revised.

[32] Guangyao Yu, Thiago Batista Soeiro, Jianning Dong, and Pavol Bauer. Study of back-end dc/dc converter for 3.7 kw wireless charging system according to sae j2954. In *2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, pages 1–8. IEEE, 2021.

[33] Murat Yilmaz and Philip T. Krein. Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. *IEEE Transactions on Power Electronics*, 28(5):2151–2169, 2013.

[34] Marco Stecca, Laura Ramirez Elizondo, Thiago Batista Soeiro, Pavol Bauer, and Peter Palensky. A comprehensive review of the integration of battery energy storage systems into distribution networks. *IEEE Open Journal of the Industrial Electronics Society*, 1:46–65, 2020.

[35] Srdjan M. Lukic, Jian Cao, Ramesh C. Bansal, Fernando Rodriguez, and Ali Emadi. Energy storage systems for automotive applications. *IEEE Transactions on Industrial Electronics*, 55(6):2258–2267, 2008.

[36] Hua Kevin Bai, Daniel Costinett, Leon M. Tolbert, Ruiyang Qin, Liyan Zhu, Ziwei Liang, and Yang Huang. Charging electric vehicle batteries: Wired and wireless power transfer: Exploring ev charging technologies. *IEEE Power Electronics Magazine*, 9(2):14–29, 2022.

[37] Francesca Grazian, Wenli Shi, Thiago Batista Soeiro, Jianning Dong, and Pavol Bauer. Electric vehicle charging based on inductive power transfer employing variable compensation capacitance for optimum load matching. In *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, pages 5262–5267, 2020.

[38] Minfan Fu, Chengbin Ma, and Xinen Zhu. A cascaded boost–buck converter for high-efficiency wireless power transfer systems. *IEEE Transactions on Industrial Informatics*, 10(3):1972–1980, 2014.

[39] Yong Huang, Naoki Shinohara, and Tomohiko Mitani. Impedance matching in wireless power transfer. *IEEE Transactions on Microwave Theory and Techniques*, 65(2):582–590, 2017.

[40] Liuchen Tai, Mingyao Lin, Jianhua Wang, and Chongsheng Hou. Synchronous control strategy with input voltage feedforward for a four-switch buck-boost converter used in a variable-speed pmsg energy storage system. *Electronics*, 10(19):2375, 2021.

[41] Erik Schaltz, Peter Omand Rasmussen, and Alireza Khaligh. Non-inverting buck-boost converter for fuel cell applications. In *2008 34th Annual Conference of IEEE Industrial Electronics*, pages 855–860, 2008.

[42] F. Caricchi, F. Crescimbini, and A. Di Napoli. 20 kw water-cooled prototype of a buck-boost bidirectional dc-dc converter topology for electrical vehicle motor drives. In *Proceedings of 1995 IEEE Applied Power Electronics Conference and Exposition - APEC'95*, volume 2, pages 887–892 vol.2, 1995.

[43] Greg Stahl, Miguel Rodriguez, and Dragan Maksimovic. A high-efficiency bidirectional buck-boost dc-dc converter. In *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1362–1367, 2012.

[44] Xi Chen, Anirudh Ashok Pise, John Elmes, and Issa Batarseh. Ultra-highly efficient low-power bidirectional cascaded buck-boost converter for portable pv-battery-devices applications. *IEEE Transactions on Industry Applications*, 55(4):3989–4000, 2019.

[45] F. Caricchi, F. Crescimbini, F.G. Capponi, and L. Solero. Study of bi-directional buck-boost converter topologies for application in electrical vehicle motor drives. In *APEC '98 Thirteenth Annual Applied Power Electronics Conference and Exposition*, volume 1, pages 287–293 vol.1, 1998.

[46] C.P. Henze, H.C. Martin, and D.W. Parsley. Zero-voltage switching in high frequency power converters using pulse width modulation. In *APEC '88 Third Annual IEEE Applied Power Electronics Conference and Exposition*, pages 33–40, 1988.

[47] Junhong Zhang, Jih-Sheng Lai, Rae-Young Kim, and Wensong Yu. High-power density design of a soft-switching high-power bidirectional dc–dc converter. *IEEE Transactions on Power Electronics*, 22(4):1145–1153, 2007.

[48] O. Knecht, D. Bortis, and J. W. Kolar. Comparative evaluation of a triangular current mode (tcm) and clamp-switch tcm dc-dc boost converter. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–8, 2016.

[49] Junzhong Xu, Thiago Batista Soeiro, Yong Wang, Fei Gao, Houjun Tang, and Pavol Bauer. A hybrid modulation featuring two-phase clamped discontinuous pwm and zero voltage switching for 99 *IEEE Transactions on Vehicular Technology*, 71(2):1454–1465, 2022.

[50] Kristian Kruse, Mads Elbo, and Zhe Zhang. Gan-based high efficiency bidirectional dc-dc converter with 10 mhz switching frequency. In *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 273–278. IEEE, 2017.

[51] Zhe Yu, Holger Kapels, and Klaus F. Hoffmann. High efficiency bidirectional dc-dc converter with wide input and output voltage ranges for battery systems. In *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, 2015.

[52] Xiaoyong Ren, Xinbo Ruan, Hai Qian, Mingqiu Li, and Qianhong Chen. Three-mode dual-frequency two-edge modulation scheme for four-switch buck–boost converter. *IEEE Transactions on Power Electronics*, 24(2):499–509, 2009.

[53] Hidenori Kobayashi. Circuit of high efficient buck-boost switching regulator and control method thereof, June 14 2012. US Patent App. 12/928,876.

[54] Dong-Hee Kim and Byoung-Kuk Lee. An enhanced control algorithm for improving the light-load efficiency of noninverting synchronous buck–boost converters. *IEEE Transactions on Power Electronics*, 31(5):3395–3399, 2016.

[55] Jimmy Liu, Kin Lap Wong, Scott Allen, and John Mookken. Performance evaluations of hard-switching interleaved dc/dc boost converter with new generation silicon carbide mosfets. *Cree Inc*, pages 1–6, 2013.

[56] Zheyu Zhang, Hao Tu, Xu She, Tomas Sadilek, Ramanujam Ramabhadran, Huan Hu, and William Earls. High-efficiency silicon carbide-based buck-boost converter in an energy storage system: Minimizing complexity and maximizing efficiency. *IEEE Industry Applications Magazine*, 27(3):51–62, 2021.

[57] Stefan Waffler and Johann W. Kolar. A novel low-loss modulation strategy for high-power bidirectional buck+boost converters. *IEEE Transactions on Power Electronics*, 24(6):1589–1599, 2009.

[58] Alex J. Hanson, Rachel S. Yang, Seungbum Lim, and David J. Perreault. A soft-switched high frequency converter for wide voltage and power ranges. In *2016 IEEE International Telecommunications Energy Conference (INTELEC)*, pages 1–8, 2016.

[59] Zhe Yu, Holger Kapels, and Klaus F. Hoffmann. Extreme high efficiency non-inverting buck-boost converter for energy storage systems. In *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, 2016.

[60] Zhe Yu, Holger Kapels, and Klaus F. Hoffmann. A novel control concept for high-efficiency power conversion with the bidirectional non-inverting buck-boost converter. In *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, pages 1–10, 2016.

[61] Tianzhi Fang, Yuan Wang, Huili Zhang, Yu Zhang, Shuheng Sheng, and Jianyu. Lan. An improved three-mode variable frequency control strategy based on four-switch buck-boost converter. *Transactions of China Electrotechnical Society*, 36(21):4544–4557, 2021.

[62] Patrizio Vinciarelli. Buck-boost dc-dc switching power conversion, September 7 2004. US Patent 6,788,033.

[63] Zongjie Zhou, Haiyan Li, and Xinke Wu. A constant frequency zvs control system for the four-switch buck–boost dc–dc converter with reduced inductor current. *IEEE Transactions on Power Electronics*, 34(7):5996–6003, 2019.

[64] Lin Tian, Xinke Wu, Congrang Jiang, and Jinxu Yang. A simplified real-time digital control scheme for zvs four-switch buck–boost with low inductor current. *IEEE Transactions on Industrial Electronics*, 69(8):7920–7929, 2022.

[65] Qi Liu, Qinsong Qian, Min Zheng, Shengyou Xu, Weifeng Sun, and Tingying Wang. An improved quadrangle control method for four-switch buck-boost converter with reduced loss and decoupling strategy. *IEEE Transactions on Power Electronics*, 36(9):10827–10841, 2021.

[66] Nguyen Anh Dung, Pham Phu Hieu, Huang-Jen Chiu, Yao-Ching Hsieh, and Jing-Yuan Lin. A dsp based digital control strategy for zvs bidirectional buck+boost converter. In *2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG)*, pages 1–4, 2018.

[67] Kun Xia, Zheng Li, Yujian Qin, Yin Yuan, and Qingqing Yuan. Minimising peak current in boundary conduction mode for the four-switch buck–boost dc/dc converter with soft switching. *IET Power Electronics*, 12(4):944–954, 2019.

[68] Zheyu Zhang, Fred Wang, Daniel J. Costinett, Leon M. Tolbert, Benjamin J. Blalock, and Haifeng Lu. Dead-time optimization of sic devices for voltage source converter. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1145–1152, 2015.

[69] Maria R. Rogina, Alberto Rodriguez, Aitor Vazquez, and Diego G. Lamar. Improving the efficiency of sic-based synchronous boost converter under variable switching frequency tcm and different input/output voltage ratios. *IEEE Transactions on Industry Applications*, 55(6):7757–7764, 2019.

[70] Hao Tu, Hao Feng, Srdjan Srdic, and Srdjan Lukic. Extreme fast charging of electric vehicles: A technology overview. *IEEE Transactions on Transportation Electrification*, 5(4):861–878, 2019.

[71] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round. Pwm converter power density barriers. In *2007 Power Conversion Conference - Nagoya*, pages P–9–P–29, 2007.

[72] Xu-Feng Cheng, Chenyang Liu, Dianlong Wang, and Yong Zhang. State-of-the-art review on soft-switching technologies for non-isolated dc-dc converters. *IEEE Access*, 9:119235–119249, 2021.

[73] Alejandro Pozo Arribas, Fei Shang, Mahesh Krishnamurthy, and Krishna Shenai. Simple and accurate circuit simulation model for sic power mosfets. *IEEE Transactions on Electron Devices*, 62(2):449–457, 2015.

[74] Oliver Knecht, Dominik Bortis, and Johann W. Kolar. Zvs modulation scheme for reduced complexity clamp-switch tcm dc–dc boost converter. *IEEE Transactions on Power Electronics*, 33(5):4204–4214, 2018.

[75] Bart F. J. Bokmans, Bas J. D. Vermulst, and Jan M. Schellekens. High-frequency inductor current estimator for power converters. In *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, pages 1–8, 2021.

[76] Wilmar Martinez, Camilo Cortes, Masayoshi Yamamoto, and Jun Imaoka. Effect of inductor parasitic resistances on the voltage gain of high step-up dc–dc converters for electric vehicle applications. *IET Power Electronics*, 11(10):1628–1639, 2018.

[77] Guangyao Yu, Jianning Dong, Thiago Batista Soeiro, Gangwei Zhu, Yu Yao, and Pavol Bauer. Three-mode variable-frequency zvs modulation for four-switch

buck+boost converters with ultra-high efficiency. *IEEE Transactions on Power Electronics*, 38(4):4805–4819, 2023.

[78] Guangyao Yu, Jianning Dong, Thiago Batista Soeiro, and Pavol Bauer. A variable-frequency zvs modulation for four-switch buck+boost converters with seamless step-up/down mode transition. In *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, pages 2808–2813, 2023.

[79] R. A. Salas and J. Pleite. Equivalent electrical model of a ferrite core inductor excited by a square waveform including saturation and power losses for circuit simulation. *IEEE Transactions on Magnetics*, 49(7):4257–4260, 2013.

[80] D. Czarkowski and M.K. Kazimierczuk. Energy-conservation approach to modeling pwm dc-dc converters. *IEEE Transactions on Aerospace and Electronic Systems*, 29(3):1059–1063, 1993.

[81] M. Bartoli, A. Reatti, and M.K. Kazimierczuk. High-frequency models of ferrite core inductors. In *Proceedings of IECON'94 - 20th Annual Conference of IEEE Industrial Electronics*, volume 3, pages 1670–1675 vol.3, 1994.

[82] John G Kassakian, David J Perreault, George C Verghese, and Martin F Schlecht. *Principles of power electronics*. Cambridge University Press, 2023.

[83] K. Venkatachalam, C.R. Sullivan, T. Abdallah, and H. Tacca. Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters. In *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.*, pages 36–41, 2002.

[84] TDK Electronics. Ferrites and accessories-siferrit material n87. *Data Sheet, February*, 2023.

[85] Jonas Muhlethaler, Jürgen Biela, Johann Walter Kolar, and Andreas Ecklebe. Core losses under the dc bias condition based on steinmetz parameters. *IEEE Transactions on Power Electronics*, 27(2):953–963, 2012.

[86] Michael Baumann, Christoph Drexler, Jonas Pfeiffer, Jens Schueltzke, Erwin Lorenz, and Michael Schmidhuber. Investigation of core-loss mechanisms in large-scale ferrite cores for high-frequency applications. In *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, pages 1–10, 2022.

[87] Guangyao Yu, Thiago Batista Soeiro, Jianning Dong, and Pavol Bauer. Comparison of two and three-level ac-dc rectifier semiconductor losses with sic mosfets considering reverse conduction. In *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, pages 01–09, 2022.

[88] FLIR Teledyne. Use low-cost materials to increase target emissivity. *Teledyne FLIR LLC*, 2015.

[89] Jie Fang, Xinbo Ruan, Xinze Huang, Renxi Dong, Xiaojian Wu, and Jianyu Lan. A pwm plus phase-shift control for four-switch buck-boost converter to achieve zvs in full input voltage and load range. *IEEE Transactions on Industrial Electronics*, 69(12):12698–12709, 2022.

[90] Renxi Dong, Xinbo Ruan, and Lingxuan Xiao. A simplified implementation with improved dynamic performance of pwm plus phase-shift control for four-switch buck–boost converter. *IEEE Transactions on Power Electronics*, 39(3):3014–3023, 2024.

[91] Guangyao Yu, Sachin Yadav, Jianning Dong, and Pavol Bauer. Revisiting the reverse switched current of buck, boost, and buck–boost converters in voltage-mode tcm–zvs control considering parasitic resistances. *IEEE Transactions on Power Electronics*, 39(7):8254–8268, 2024.

[92] Yuan Wang, Jianyu Lan, Xin Huang, Tianzhi Fang, Xinbo Ruan, and Mengxue Dong. An improved single-mode control strategy based on four-switch buck-boost converter. In *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 320–325. IEEE, 2020.

[93] Wiljan Vermeer, Marck Wolleswinkel, Jos Schijffelen, Gautham Ram Chandra Mouli, and Pavol Bauer. Three-mode variable-frequency modulation for the four-switch buck-boost converter: A qr-bcm versus tcm case study and implementation. *IEEE Transactions on Industrial Electronics*, 72(2):1512–1523, 2025.

[94] Xiao Li, Yushan Liu, and Yaosuo Xue. Four-switch buck–boost converter based on model predictive control with smooth mode transition capability. *IEEE Transactions on Industrial Electronics*, 68(10):9058–9069, 2021.

[95] Yuning Bai, Sideng Hu, Zhi Yang, Mustafa Tahir, and Yongjian Zhi. A selective common mode noise mitigation method using phase-shifted modulation for four-switch buck–boost dc/dc converter. *IEEE Transactions on Power Electronics*, 38(6):7183–7196, 2023.

[96] Ned Mohan, Tore M Undeland, and William P Robbins. *Power electronics: converters, applications, and design*. John wiley & sons, 2003.

[97] Matthias Kasper, Ralph M. Burkart, Gerald Deboy, and Johann W. Kolar. Zvs of power mosfets revisited. *IEEE Transactions on Power Electronics*, 31(12):8063–8067, 2016.

[98] Toshiba. *Power MOSFET Electrical Characteristics*, January 2023.

[99] Gautham Ram Chandra Mouli, Jos H. Schijffelen, Pavol Bauer, and Miroslav Zeman. Design and comparison of a 10-kw interleaved boost converter for pv application using si and sic devices. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(2):610–623, 2017.

[100] Yafei Chen, Hailong Zhang, Chang-Soo Shin, Kyung-Ho Seo, Sung-Jun Park, and Dong-Hee Kim. A comparative study of s-s and lcc-s compensation topology of

inductive power transfer systems for ev chargers. In *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 99–104, 2019.

[101] Francesca Grazian, Wenli Shi, Thiago B. Soeiro, Jianning Dong, Peter van Duijsen, and Pavol Bauer. Compensation network for a 7.7 kw wireless charging system that uses standardized coils. In *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, 2020.

[102] F. Corti, L. Paolucci, A. Reatti, F. Grasso, L. Pugi, N. Tesi, E. Grasso, and M. Nienhaus. A comprehensive comparison of resonant topologies for magnetic wireless power transfer. In *2020 IEEE 20th Mediterranean Electrotechnical Conference (MELECON)*, pages 582–587, 2020.

[103] Andrea Cavallini, Davide Fabiani, and Gian Carlo Montanari. Power electronics and electrical insulation systems - part 1: Phenomenology overview. *IEEE Electrical Insulation Magazine*, 26(3):7–15, 2010.

[104] Andrea Cavallini, Davide Fabiani, and Gian Carlo Montanari. Power electronics and electrical insulation systems - part 2: life modeling for insulation design. *IEEE Electrical Insulation Magazine*, 26(4):33–39, 2010.

[105] Zhen Zhang, Hongliang Pang, Apostolos Georgiadis, and Carlo Cecati. Wireless power transfer—an overview. *IEEE Transactions on Industrial Electronics*, 66(2):1044–1058, 2019.

[106] R.L. Steigerwald. A comparison of half-bridge resonant converter topologies. *IEEE Transactions on Power Electronics*, 3(2):174–182, 1988.

[107] Jongeun Byeon, Minhyuck Kang, Minkook Kim, Dong-Myoung Joo, and Byung Kuk Lee. Hybrid control of inductive power transfer charger for electric vehicles using lccl-s resonant network in limited operating frequency range. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–6. IEEE, 2016.

[108] Siqi Li, Weihan Li, Junjun Deng, Trong Duy Nguyen, and Chunting Chris Mi. A double-sided lcc compensation network and its tuning method for wireless power transfer. *IEEE Transactions on Vehicular Technology*, 64(6):2261–2273, 2015.

[109] Xiaohui Qu, Yanyan Jing, Hongdou Han, Siu-Chung Wong, and Chi K. Tse. Higher order compensation for inductive-power-transfer converters with constant-voltage or constant-current output combating transformer parameter constraints. *IEEE Transactions on Power Electronics*, 32(1):394–405, 2017.

[110] Wenbo Wang, Junjun Deng, Deliang Chen, Zhenpo Wang, and Shuo Wang. A novel design method of lcc-s compensated inductive power transfer system combining constant current and constant voltage mode via frequency switching. *IEEE Access*, 9:117244–117256, 2021.

[111] Yuequan Hu, Jianwen Shao, and Teik Siang Ong. 6.6 kw high-frequency full-bridge llc dc/dc converter with sic mosfets. In *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 6848–6853, 2019.

List of Publications

As A First Author

1. **G. Yu**, S. Yadav, J. Dong and P. Bauer, "Revisiting the Reverse Switched Current of Buck, Boost, and Buck–Boost Converters in Voltage-Mode TCM–ZVS Control Considering Parasitic Resistances," in IEEE Transactions on Power Electronics, vol. 39, no. 7, pp. 8254-8268, July 2024, doi: 10.1109/TPEL.2024.3382051.

2. **G. Yu**, J. Dong, T. B. Soeiro, G. Zhu, Y. Yao and P. Bauer, "Three-Mode Variable-Frequency ZVS Modulation for Four-Switch Buck+Boost Converters With Ultra-High Efficiency," in IEEE Transactions on Power Electronics, vol. 38, no. 4, pp. 4805-4819, April 2023, doi: 10.1109/TPEL.2022.3231969.

3. **G. Yu**, P. Ye, F. Grazian, J. Dong, T. B. Soeiro and P. Bauer, "An Improved Peak Voltage Calculation Method for Compensation Components in S-S and LCC-S Compensated Wireless Power Transfer Systems,"
2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-9, doi: 10.23919/EPE23ECCEEurope58414.2023.10264576.

4. **G. Yu**, J. Dong, T. B. Soeiro and P. Bauer, "A Variable-Frequency ZVS Modulation for Four-Switch Buck+Boost Converters with Seamless Step-up/down Mode Transition," 2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia), Jeju Island, Korea, Republic of, 2023, pp. 2808-2813, doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213482.

5. **G. Yu**, T. B. Soeiro, J. Dong and P. Bauer, "Comparison of Two and Three-Level AC-DC Rectifier Semiconductor Losses with SiC MOSFETs Considering Reverse Conduction," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 01-09.

6. **G. Yu**, T. B. Soeiro, J. Dong and P. Bauer, "Study of Back-end DC/DC Converter for 3.7 kW Wireless Charging System according to SAE J2954," 2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Florence, Italy, 2021, pp. 1-8, doi: 10.1109/CPE-POWERENG50821.2021.9501207.

7. **G. Yu**, M. G. Niasar, D. Ganeshpure, T. B. Soeiro and P. Bauer, "A Transformer Isolated Driving Method for SiC MOSFETs with a Constant Negative Off Voltage," 2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC), Gliwice, Poland, 2021, pp. 39-45, doi: 10.1109/PEMC48073.2021.9432530.POWERENG50821.2021.9501207.

As A Co-author

1. F. Grazian, **G. Yu**, C. Riekerk, W. Shi, J. Dong, G. Zhu, T. B. Soeiro and P. Bauer, "Modeling of the Inverter Current Distortion in the Double-sided LCC Compensation for Inductive Power Transfer Systems," (Accepted by IECON 2025)

2. S. Yadav, **G. Yu**, Z. Qin and P. Bauer, "A Balancing Converter with Series Connected MOSFETs for ±700V Bipolar DC Grids," PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2024, pp. 2578-2585, doi: 10.30420/566262361.

3. G. Zhu, J. Dong, **G. Yu**, W. Shi, C. Riekerk and P. Bauer, "Optimal Multivariable Control for Wide Output Regulation and Full-Range Efficiency Optimization in LCC–LCC Compensated Wireless Power Transfer Systems," in IEEE Transactions on Power Electronics, vol. 39, no. 9, pp. 11834-11848, Sept. 2024, doi: 10.1109/TPEL.2024.3414157.

4. W. Shi, J. Dong, **G. Yu**, G. Zhu and P. Bauer. "Low Output Power Ripple Dynamic Wireless Power Transfer based on Dual-Phase Non-Overlapped Transmitters." Authorea Preprints (2023).

5. W. Shi, J. Dong, T. B. Soeiro, C. Riekerk, F. Grazian, **G. Yu** and P. Bauer, "Design of a Highly Efficient 20-kW Inductive Power Transfer System With Improved Misalignment Performance," in IEEE Transactions on Transportation Electrification, vol. 8, no. 2, pp. 2384-2399, June 2022, doi: 10.1109/TTE.2021.3133759.

Author Profile

Guangyao Yu was born in Haiyan, Zhejiang, China, in 1992. He received the bachelor's degree in electrical engineering and automation in 2015 from Zhejiang University, Hangzhou, China, and the master's degree (with cum laude) in electrical engineering in 2020 from the Delft University of Technology (TU Delft), Delft, The Netherlands. From 2020 to 2025, he has been working toward the Ph.D. degree in electrical engineering with DCE&S Group (dc systems, energy conversion, and storage). From 2016 to 2018, he was with Solax Power Company, Ltd., Hangzhou, China, where he was an Electrical Engineer.