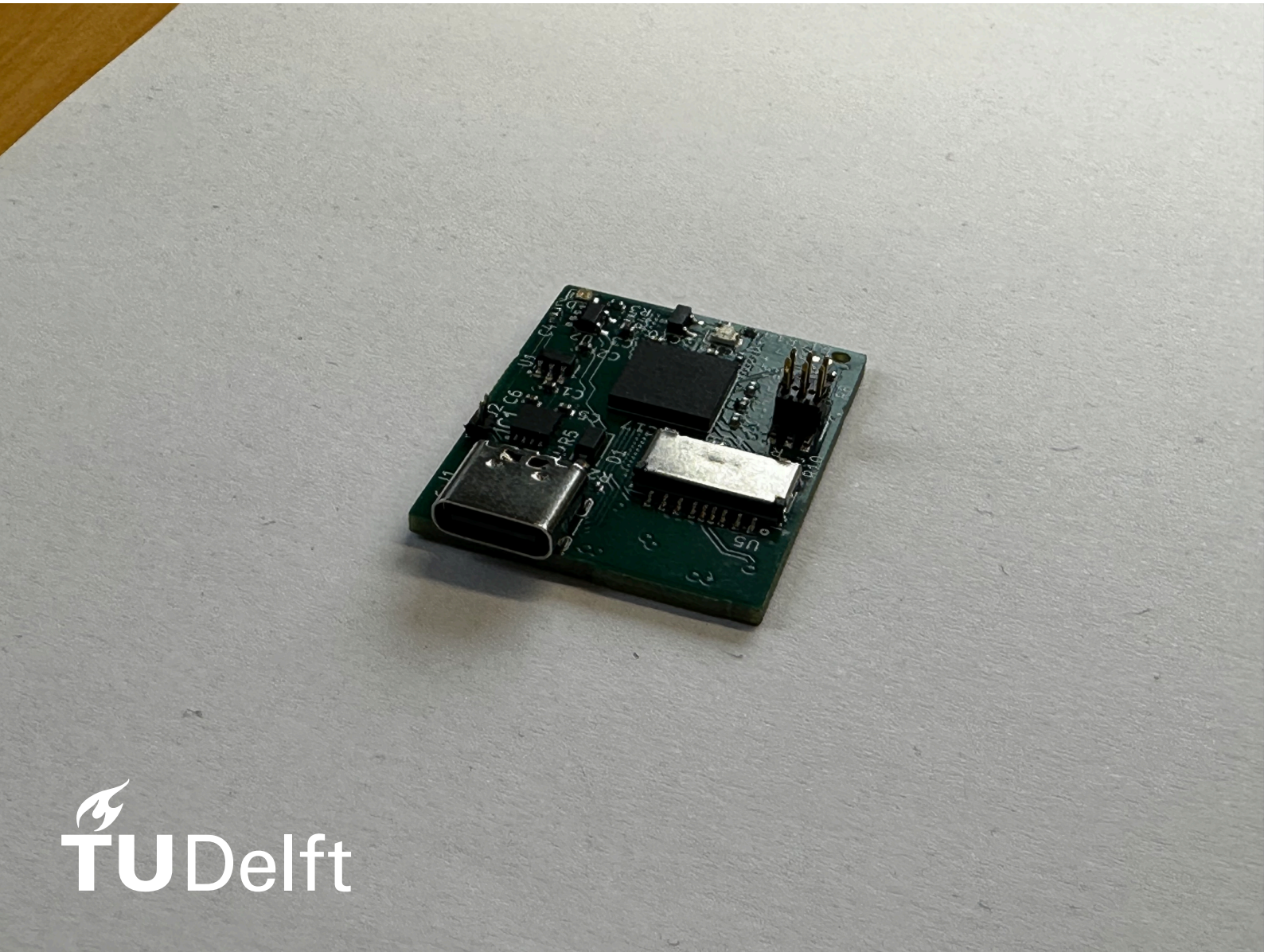
Neurologger: Ultra Light Neural Activity Recorder

Hardware Design and Implementation

EE3L11: BSc Electrical Engineering BAP Q1/Q2

Francesco Foglia and Rik de Moor



TU Delft

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Hardware Design and Implementation

by

Francesco Foglia and Rik de Moor

Supervisor:	Dr. ir. C. Strydis
Daily Supervisors:	A. Movahedin & L. Landsmeer
Project Duration:	October, 2025 - December, 2025
Faculty:	Faculty of Electrical Engineering, Mathematics and Computer Science, Delft

TU Delft

Preface

We would like to thank our supervisor Christos Strydis for the opportunity to work on this project. He was closely involved and motivated us to work diligently. We would also like to thank our daily supervisors Amirreza Movahedin and Lennart Landsmeer for their constant support and quick reactions on the Mattermost communication channel.

We would also like to thank Brian Nanhekhan for his help with checking the PCB design.

Furthermore we would like to thank the Software group consisting of Anass al Mahdoui, Daniel Abed and Foivos Sourlas for the effective cooperation in this project.

We would also like to extend our gratitude to James Hutton and Victor Scholten for the educational workshops which put our research into perspective.

Lastly we would like to thank our family and friends for the constant support.

Francesco Foglia and Rik de Moor
Delft, December 2025

Summary

As technologies in embedded systems are rapidly advancing, possibilities are opening up in many research fields. Neuroscience is one of those fields. Research on the brain is crucial for medial applications such as seizure prevention, understanding neurological disorders like Parkinson's disease and developing Brain Machine Interfaces for prosthetics. In order to make accurate neural recordings, invasive techniques like Intracortical electrophysiology (IC-Ephys) are often required. Using tiny probes, neural signals are measured directly from the brain tissue. These experiments are almost always performed on animals because of the health risks that they pose.

The Neuroscience department at the Erasmus Medical Center (EMC) has been conducting these sorts of experiments on mice using either wired or battery-based neural recording devices (Neurologgers). These devices simply make neural recordings without processing the data in any other way. To get the most realistic neural response in the brain, the mouse should be free to move and not be limited by the recording device. Ideally, signal processing and spike detection is done immediately on the device, so that it outputs useful data instead of raw data.

For these reasons our group was given the task by the Neuroscience department to make a battery-based neural-logging device containing an FPGA for real-time signal processing and spike detection. In this thesis, the design process, implementation and validation of the hardware of this so called Neurologger is discussed.

We were able to make a compact design that weighs 4.139 g without battery. It has an FPGA which performs real-time signal processing and spike detection. Two neural probes can be attached to perform neural recordings in multiple parts of the brain. Finally, 64 channels can be recorded simultaneously at a sampling rate of 20 kHz.

This thesis also contains a proposal for an even smaller Neurologger design. Making specific design choices, more channels can be recorded with a device that has a significantly smaller surface area than the current design.

Contents

1

Introduction

The brain is one of the most complex organs of the human body. Understanding it is crucial for medical applications, such as preventing seizures and aiding people with handicaps. In order to understand the brain it is important to know the purpose that the different parts serve and when certain parts activate. Using Intracortical electrophysiology (IC-ephys), brain activity can be measured directly from inside the brain tissue. This is an invasive technique where the test subject has to be surgically operated so that the electrodes can be implanted correctly. For this reason and because of similarities in brain anatomy [1], IC-ephys measurements are often performed on animals such as mice. Research involving IC-ephys is being conducted for applications like BCI [2] and seizure prevention [3]. Neural probes are used to make measurements of multiple locations in the selected part of the brain tissue. The measured signal amplitudes are higher for IC-ephys than for less invasive techniques like electroencephalography (EEG), where the electrodes are simply placed on the scalp [4]. A higher signal amplitude in this case means more localized information with higher resolution.

1.1. Motivation

The Neuroscience department of the Erasmus Medical Center (EMC) is conducting research in the fields of sensorimotor control [5] and real-time neuronal spike classification [6]. In this research field brain activity is measured using methods like IC-ephys on live mice. These recordings show spikes with specific timestamps on which spike classification and spike-based analyses are performed. The mice are either head-fixed or attached via a wire and thus not able to move freely. Following up on this and similar research, the Neuroscience department at EMC expressed the need for an implantable, battery-based recording device, which could enable the mouse to move freely while neural recordings like IC-ephys measurements are done.

Such a device is called a Neurologger: A logging device which stores neural activity on ultra-compact memory media [7]. There are a lot of different types of Neurologgers with different applications. The department of Neuroscience at EMC has developed tethered recording systems which have made successful measurements [6]. However, these systems so far were wired or only logged raw data without immediately processing it. The task was given to us to develop a battery-based Neurologger that performed real time data processing and spike detection on neural recordings using a Field Programmable Gate Array (FPGA).

1.2. Thesis Goals and Contributions

Based on the task that was given to us by the Neuroscience department at EMC the following thesis goal can be formulated:

The thesis goal is to develop a Neurologger that weighs less than 5 grams, uses an FPGA for signal processing, has a power autonomy of at least 30 minutes, while supporting 64 channels from 2 neural probes at a sampling rate of 20 kHz.

The contributions that this thesis will make are:

- Conduct a state-of-the-art survey regarding Neurologgers and using it to make design specifications that sets our design apart from the rest.
- Develop a Neurologger with an FPGA that can perform real time signal processing and spike detection.
- Test the Neurologger with the required tools such that it can eventually be tested on live mice.
- Design an improved iteration of the device for future development.

1.3. Thesis Methodology

An extensive state of the art analysis was done (chapter 2) that led to the conclusion that our device would have a unique set of abilities when compared to the current technology. In cooperation with the Software Group (Anass al Mahdoui, Danial Abed and Foivos Sourlas) this device was realized. Our group is responsible for the hardware and therefore this thesis will focus on the PCB (Printed Circuit Board) design of the Neurologger.

It is important to note that, when the project started, we immediately got access to a set of schematics, which form the basis of the design we have now. These files contained all the necessary major components for the device. These were mainly derived from 2 earlier Neurologger designs by the Neuroscience department of EMC. That is also the reason that our design is called the Neurologger V3. The two earlier designs can be seen next to our Neurologger in figure 1.1.

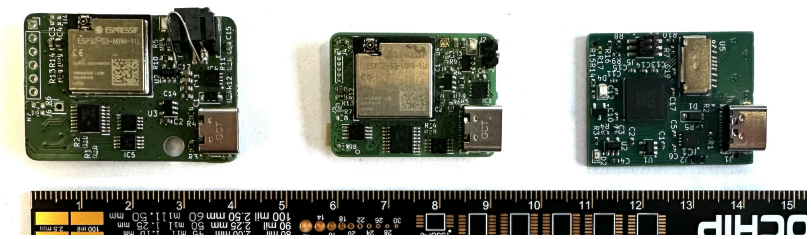


Figure 1.1: From left to right: Neurologger V1, V2 and V3

In the obtained schematics, a lot of signals were not yet connected and resistor and capacitor values often needed correction. This is important to keep in mind, as this means that our design process was a continuation of an initial design. This was done because our priority was having a working device before the end of the project. Taking into account manufacturing and shipping delays, the decision was made to take this initial design as a foundation to build on, while still taking a critical look at the component choices.

The first step of making the design was finishing the component selection and checking and correcting the schematics that were provided. After this, the placement of components and routing of the PCB could begin. Ordering the PCB and making plans for a second iteration were the next steps. The last step was combining our hardware with the software made by the Software Group and testing the device. The results are then visualized and finally the PCB and the design process are evaluated in the final report. A timeline of the design process can be seen in figure 1.2. The FPGA software group design process can be found in figure 1.3.

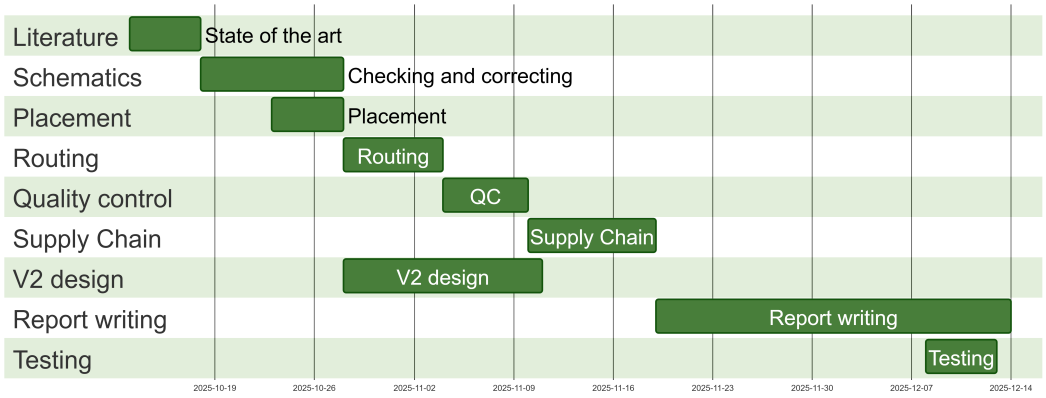


Figure 1.2: Neurologger PCB design process

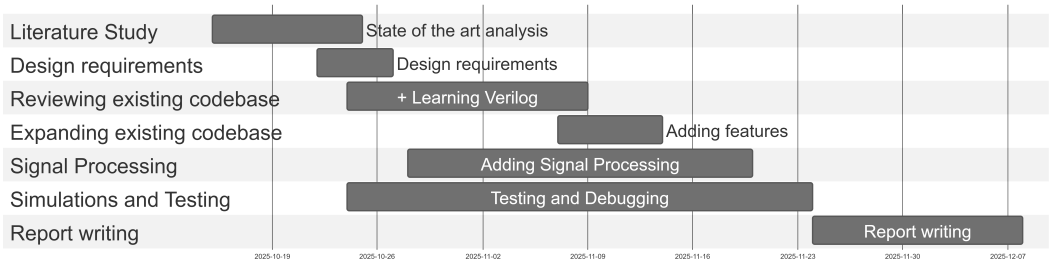


Figure 1.3: FPGA software group design process

1.4. Thesis organization

As mentioned before, in chapter 2 we will take a look at comparable devices that already exist. In chapter 3, we will discuss the design specifications of our device. The implementation of the Neurologger will be discussed in chapter 4 and in chapter 5, we will dive into the implementation of the schematics and the routing of this complex PCB. In chapter 6, the testing of the PCB will be discussed. A proposal for a new iteration will be discussed in chapter 7. Finally, chapter 8 draws conclusions from the testing.

2

Related Work

Previously, some use cases of electrophysiology and more specifically IC-ephys were established. The device which is used to record these brain signals is called a Neurologger. In this chapter a number of concepts related to the Neurologger will be explained and analyzed.

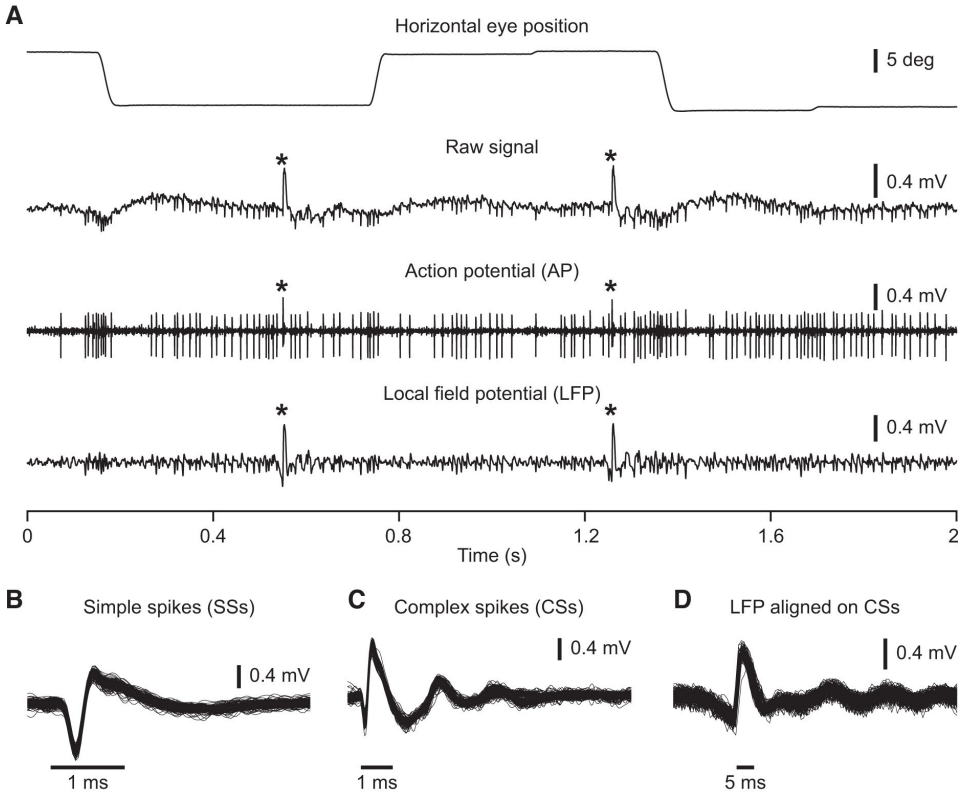


Figure 2.1: Characteristics of an exemplary Purkinje cell. **A**; raw signal (wide-band, 2nd row), action potential (AP; high band-passed, 300 Hz to 3 KHz, 3rd row), and local field potential (LFP; low passed, 30–400 Hz, 4th row) activity in relation to horizontal eye movements (1st row). *Complex spikes (CSs). **B**: a subset of isolated simple spike (SS) waveforms aligned on SS start. **C**: a subset of isolated CS waveforms aligned on CS start.**D**: a subset of LFP responses aligned to CS start. [8](with modifications)

2.1. Electrophysiological signals

Before a Neurologger can be designed, it first has to be established what it's trying to measure. The goal of a Neurologger is to record signals from the brain. Communication in the brain is achieved through spikes, which are also known as action potentials. These action potentials are created by ion-flux accross the neural membrane, which lead to a current into or out of the the resistive extracellular medium. This causes an electrical field outside the cell, making it possible to measure the action-potential in the extracellular environment. These resulting electrical field potentials are measurable as a voltage between -500 to 500 µV. An example of such an electrical field potential in Purkinje cells can be found in figure 2.1[8], where it is referred to as the raw signal. The action potential (AP) in this figure is the high-passed waveform of this electrical field potential, and is directly related to the action potential inside the cell. The local field potential (LFP) is the low-pass version of the electrical field potential (or it can be recorded using a dedicated LFP probe). This high-passed AP has a peak-to-peak amplitude ranging from 50 to 500µV and a spectrum between 300Hz and 5kHz [9]. The spectrum of the LFP lies below 300Hz. There are different kinds of spikes and in order to be able to differentiate between these different spikes at least 40 samples are needed, taking into account a spike duration of about 2ms, this gives us a minimum sampling frequency of about 20kHz [10].

2.2. Neurologger

Now that some important parameters of the electrophysiological signals have been established, a closer look can be taken at a Neurologger as a whole. A Neurologger can be split up into 2 main parts: the probe(s) and the headstage. An illustration of a tethered Neurologger can be found in figure 2.2

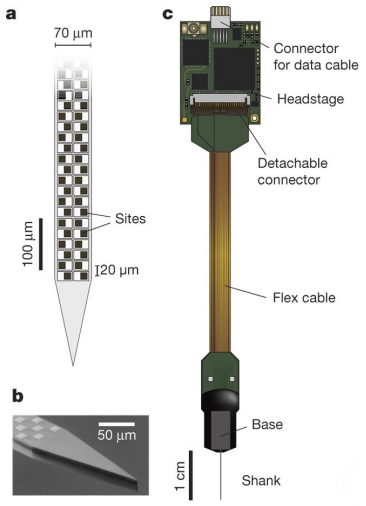


Figure 2.2: **a**, Illustration of probe tip. **b**, Scanning electron microscope image of probe tip. **c**, Neurologger packiging, including probe with flex cable and headstage. [11] (with modifications)

The probe(s) contains a needle, commonly referred to as a shank, which contains an array of electrodes at which measurements can be performed. An illustration of both the probe, probe tip and the mentioned measurement sites can be found in figure 2.2. The earliest probes circa 1950s consisted of an insulated metal microelectrode which only had a single measurement point [12]. Due to advancement in production techniques it has become possible to manufacture neural probes with an increasing number of measurement sites, while keeping the physical dimensions to a minimum. Three mayor types of neural probes are widely used: microwire based, silicon based and flexible neural probes [13]. These are available from numerous manufacturers and are highly customizable. To give an idea, probes are often characterized by the following main parameters:

- Number of shanks
- Number of electrodes/channels

- Location of electrodes
- Shank dimensions
- Tip shape
- Connector type

These probe(s) are surgically inserted into the relevant areas of the brain by cutting open a part of the head of the animal and drilling a hole in the skull above the target area. Afterwards the opening is closed and the probe is kept in place using medical cement [14].

The headstage consists of 1 or multiple Printed Circuit Boards (PCBs), which as the name implies are worn on the head by the animal. The headstage is connected to the probe using a connector. There are numerous headstages available with various different features which could aid or enable certain experiments. The core function of the headstage, however, is to digitize the raw analog electrophysiology signals. These signals can then be stored, transmitted, analyzed, etc. depending on the headstage and the needs of the user.

2.3. Commercially available solutions

Numerous commercial solutions for headstages and neural recording systems are available. Compared to custom solutions they have the advantage of offering great support and being generally well tested and validated, reducing the time spent debugging the system. This does, however, come at the cost of having an increased price and limited flexibility compared to custom designs. An analysis of these solutions has been conducted and the results of this can be seen in table 2.1. In order to both limit the scope and keep the solution space relevant to the problem statement the following (soft) criteria were set in order for a headstage to qualify.

- The headstage must be battery-powered
- The total weight of the headstage must be below 5g in order to permit use on mice

As can be seen from the table 2, exceptions to these criteria can be seen. The Plexon Neural recording system has been included since it is specified to be designed for experiments on freely moving mice [15]. Furthermore, a tethered digital headstage from Blackrock Neurotech was added in order to give the reader a better idea of how these battery-powered systems compare to the available tethered solutions. The information in this table was compiled using publicly available product pages, datasheets and manuals.

Some problems that were encountered during the making of this table are that specifications and information regarding these headstages are often hard to find, key specifications are sometimes missing entirely (given specifications even differ with different loggers from the same manufacturer) and conditions under which battery life are determined are often vague. An important note to make is that this table does not contain all information regarding these headstages. Some of these systems are available with a different number of channels, have multiple different battery size options or have restrictions regarding the operation of multiple loggers simultaneously. For a complete picture it is recommended to contact the manufacturer directly.

Table 2.1: Neurologger comparison

Product name	Bit depth	Channels	Weight (g)	Size (mm)	Comm. Interface	Power consumption	Sampling rate	BW	Features	Note
Multichannel systems W2100-HS32 [16]	16	32	3.6g W/O	12.5x12.5x6.5	Wireless (5m)	100mAh: 1h12min (3.9g)	20kHz	1Hz–5kHz	A,G,L	Various versions available
TainiTec Taini [17]	12	16	2.2g	19x14.5x15.5	Wireless (2.5m)	2mA draw: 120h	19.5kHz	0.35Hz–9.7kHz	–	Weight incl battery; various battery sizes
SpikeGadgets Sprite32 [18]	16	32	3.8g	21x18x10	SD card	25mAh: 1h15min	20kHz	–	A,G	Wireless status monitoring
Evolocus Neurologger 3 [19]	16	32[1]	1.96g W/O	24x15x8	SD card	25mA: 15min–2h15min (0.63–1.58g)	20.8kHz[2]	–	M,A,G,Mag	Bluetooth configuration + data access
Deuteron Technologies MouseLog16C [20]	–	16	2.88g	18x13	SD card	60mAh: 1h40min (1.3g)	31.25kHz	–	M,A,G,Mag	Optional wired operation
Deuteron Technologies SpikeLog-32 [20]	16	32	2.3g W/O	23x16x3	SD card	45mAh: 1h (1g)	32kHz	0.2Hz–500Hz or 200Hz–10kHz	M,A,G,Mag	Limited wireless data transfer
Blackrock Neurotech CerePlex µ [21]	16	32	1.2g W/O	13.2x18.2x3	Tethered	Tethered	30kHz	0.3Hz–7.5kHz	A,G,L	–
Plexon Datalogger Neural recording system [15]	16	32	8g	31x23x15.5	Wireless (1.5m)	45min	40Khz	–	L	Infrared link control
Spike Neuro Headstage [22]	–	4	3.3g	12.7x12.7	Wireless Bluetooth	40mAh: 6h	30kHz	–	–	Still in development
Doric FiWi [23]	–	4	2.8g	9.6x14.9x18.6	Wireless (3m)	40maAh: 1h30min (1.2g)	14.3kHz	–	–	Currently not available
White Matter Wireless Headstage [24]	–	64[3]	4.2g	12x10.4	Wireless	3h (2.04g)	20kHz	–	M,A,G,Mag[4]	Highly customizable

W/O: without battery M: microphone A: accelerometer G: gyroscope Mag: magnetic compass

[1] Number of channels can be increased by daisy-chaining ADC boards
[2] Sampling rate scales with number of channels
[3] Available with 64, 128, 192, 256 and 320 channels
[4] Optional modules, will increase weight by 1.42g (including bigger battery)

A number of things stand out from this table:

- The maximum number of channels with the exception of Evolocus and White Matter is 32. The Evolocus logger, however, scales its sampling rate with the number of channels. For example, if 64 channels are desired the maximum sampling frequency is reduced to 9.75kHz. This means that if a sampling frequency of 20KHz is desired the maximum number of channels is again 32. The White Matter Logger has versions that feature up to 320 channels, albeit with diminished battery life.
- The weight of the loggers vary quite a bit, the lightest logger is the TainiTec Taini which comes in at a total of 2.2g including battery.
- Regarding size, it is difficult to draw any real conclusions due to some loggers not having their height defined. Furthermore, for loggers of which the weight is specified without battery, it is not mentioned whether the dimension of the logger include the battery or not. A possible reason for this could be the multiple battery options for these loggers.
- In terms of power consumption most loggers hover around the 1 hour mark with some loggers approaching the 2 hour mark with either a reduced number of channels or a larger battery. Two notable outliers are the TainiTec Taini and the White Matter Wireless Headstage. The Taini has an impressive battery life of 120h (5 days), making this headstage highly suitable for long term monitoring. The White Matter Headstage has a relatively high battery life with a high channel count.
- For the sampling rate and bandwidth some differences again become visible. The sampling frequency of all loggers lie between 14.3kHz and 40kHz with most loggers having a sampling frequency higher than 20kHz. A larger difference can be spotted, at least when it is given, in the supported bandwidth of the loggers. Except for TainiTec, the relation between the bandwidth and sampling frequency does not follow nyquist sampling theorem and instead the incoming signal is oversampled up to a factor of 2.

2.4. Related work

Numerous battery-based headstages for mice have been proposed [25, 26, 27, 28, 29] each having their own focus points and downsides. As previously mentioned, these custom designs often offer functionality not available in off-the-shelf solutions, but come at the cost of requiring significant time in order to build, test, and debug. Following is a small description of these designs:

- [25] Presents a low-cost tethered headstage and electrode array solution with 16 channels. It utilizes a custom 3d-printed connector in order to remove the dependence on expensive of the shelf connectors. This does come with the downside of only using 16 out of the 32 available Intan ADC channels due to size constraints of this connector.
- [26] This research presents a battery-based headstage allowing recording and electrical stimulation of up to 32 channels. In order to achieve this it makes use of a custom 32-channel ”neuromodulator” ASIC. Data is streamed back to a computer using Bluetooth Low Energy (BLE), which is also the bottleneck of the system, as at the maximum sampling frequency of 20kHz only 3 channels can be used. It has a long battery life of 283 minutes.
- [27] Provides a design for a very low energy 32 channels headstage with a limited sampling frequency of up to 1kHz. In order to achieve this is makes uses of an Intan RHD2132 ADC and a Nordic Semiconductors integrated receiver-transmitter and microcontroller. For data transfer it makes use of Bluetooth Low Energy (BLE). This results in a total battery life of more than 35 hours. Furthermore, it utilizes a custom 12-channel micro-electrode. It is important to note that the current design does not fully support all 32 channels due to making use of a probe connector with limited pin count.
- [28] Presents a design using off the shelf components for a headstage with 32 channels (Intan RHD2132), a maximum sampling frequency of 4kHz with data transmission using a 2.4GHz radio transceiver from Nordic Semiconductors. With this, it achieves a battery life of about 77 minutes with the selected battery. Furthermore, it supports optogenetic stimulation.

- [29] has similar specification to the previous designs. It has 32 channels (Intan RHD2132), 32 channels of optical stimulation and features data transmission using a 2.4GHz radio transceiver. There are ,however, a few key differences. Firstly, it supports a sampling frequency of 20kHz and secondly, it utilizes an FPGA for real time spike detection and data compression. This all resulting in a maximum (no stimulation) battery life of 105 minutes.

In conclusion, there are numerous existing solutions available on the market. These solutions, however, have various (differing) shortcomings: too little channels, too low sampling rate, undesirable bandwidth, limited battery life or high weight. Furthermore, most loggers do not have the ability to connect multiple probes with separate references. In specifications, the headstage discussed in [29] is similar in the goals of this thesis (which will be discussed in more depth in the next section), however, a different approach will be taken in the sense of increased channel count, 2 separate probe references and possible spike sorting, albeit with the downside of possible reduced battery life and no optical stimulation.

3

Design Specifications

The first step of the design process is setting the design requirements. This is important for component selection and routing strategies. The requirements are summarized in table 3.1 and are explained in more detail below.

Weight with battery	lower than 5g
Battery Life	30 minutes
Channel count	64
Sampling rate	20 kHz
Features	
Implemented FPGA to manage high-speed data handling and real time signal processing	
Sufficient on-board storage	
Capable of performing neural recordings with 2 neural probes	
Compatible with external 64 channel ADC boards	
Wired and battery power mode	
Integrated LED	

Table 3.1: Requirements Neurologger

1. **The Neurologger, including its integrated battery, must have a total weight below 5 grams and a form factor suitable for attachment to a mouse without restricting its natural movement.**

   In similar applications, a weight limit of about 10% of the weight of the mouse is imposed to prevent the mouse from being hindered too much by the device [6, 30, 31]. This would be about 2-4 g depending on the mouse. A target of 5 grams including the battery is chosen to set a realistic goal.

2. **The Neurologger must be able to operate on battery for at least 30 minutes, with a target of 1 hour.**

   The Neuroscience department at EMC expressed that the battery life should be as long as possible. Using rough estimates of the devices' power consumption, 30 minutes was set as a minimum with a target battery life of 1 hour.

3. **An FPGA must be integrated to manage high-speed data handling and real-time signal processing of the acquired data.**

The Neuroscience department at EMC gave us the task to make a Neurologger device that has an implemented FPGA for high-speed data handling and real time signal processing.

4. **The Neurologger must be capable of monitoring 64 channels simultaneously.**

   The Neuroscience department at EMC expressed the device should be able to record 64 channels simultaneously.

5. **The channels that are logged by the Neurologger must each be sampled at a rate of at least 20 kHz.**

   The channels should be sampled at a sampling rate of at least 20 kHz to sample fast-spiking action potentials [10].

6. **The Neurologger must be capable of connecting to 2 neural probes for neural recordings.**

   The Neuroscience department at EMC expressed that the device should be able to connect to 2 neural probes so measurements in multiple regions can be done simultaneously.

7. **The Neurologger must include onboard storage capable of recording data from all channels at the full sampling rate for the intended duration of use.**

   To ensure battery-based capabilities, the device needs on-board storage with enough storage to record at full capacity for the entire duration of the battery life.

8. **The Neurologger must be compatible with the Cambridge Neurotech Mini-Amp-64 headstage.**

   The Neuroscience department at EMC expressed that the logger should have backwards capability with a Cambridge Neurotech Mini-Amp-64 headstage [32]. Since the department already had this device it could easily be used for testing.

9. **The Neurologger must support operation in both battery and wired modes.**

   In order to increase the versatility of the device, it was decided that it should be able to operate with both battery and wired power.

10. **The Neurologger must feature an integrated Light Emitting Diode (LED) to facilitate synchronization and provide visual indication of system status during operation.**

    The LED can be used to synchronize the logged data with a video recording of the experiment. It can also be used for system status indication. These features are important because they increase the ease of use for the researchers.

In the next two chapters the implementation of these design choices will be discussed.

4

Neurologger Headstage Implementation

In this chapter, we detail the design of the Neurologger PCB. The goal of this project is to build a device (in this case a PCB) that achieves the function defined in the introduction while fulfilling the requirements set in chapter 3. This PCB can be further divided in a number of subsystems which each have their own function and are directly related to meeting a part of the requirements. This chapter discusses the top-level design, the subsystems and the interaction between these subsystems.

4.1. Top-level Design Neurologger

In figure 4.1, an overview can be seen of the top-level design of the PCB. The PCB can be divided into 4 subsystems:

1. The FPGA subsystem: This is the brain of the design, implementing reprogrammable logic to let all the other components function correctly. It is also the component that will run the spike detection algorithm and handle real-time data processing.
2. The power system: Supplies all other subsystems with the required power.
3. The memory: The memory is used to store the measured and/or processed data.
4. The Analog Front-End (AFE) subsystem: The analog front-end consists of amplifiers, the analog-to-digital converter(s), the possible needed input filtering and the connectors used to connect the probes to the PCB.

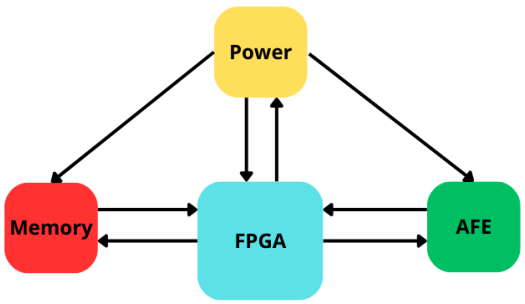


Figure 4.1: Toplevel design Neurologger

4.2. Field Programmable Gate Array

The FPGA is one of the most important components of the design. An FPGA performs digital logic just like a microcontroller. The main difference is that the FPGA can be reprogrammed and reconfigured at the hardware level after manufacturing, as opposed to a microcontroller that can only be reprogrammed on the software level. An FPGA is ideal for systems which require a lot of parallel processing capacity and flexible prototyping capabilities [33].

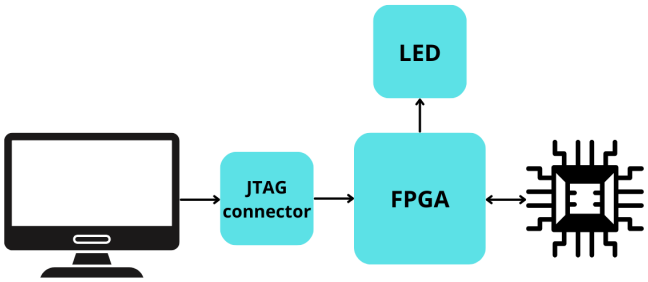


Figure 4.2: FPGA system schematic

An overview of the FPGA subsystem can be seen in figure 4.2, it consists of an FPGA, a JTAG connector and a Light Emitting Diode (LED).

JTAG is an industry standard for verifying designs and testing of PCBs. Since the used FPGA supports JTAG, this standard can be used to programm the FPGA, and for testing and debugging purposes. A Samtec FTSH series connector was selected as the JTAG connector. This connector is often used for these purposes and is a surface mount component (SMD), thus simplifying the routing process.

The LED is a component that emits light when current flows through it. It is connected to the FPGA and turns on when the FPGA tells it to. This can be used in a number of situations. Examples would be to signal the start of a neural recording such that it can be synchronized with a video recording or having it blink whenever a spike is detected.

The FPGA for this design has to meet the following requirements:

- Low power
- Small form factor
- Enough I/O (Input/Output) pins
- At least 2000 LUTs (Look Up Tables)
- SPI (Serial Peripheral Interface) controller
- LVDS (Low Voltage Differential Signaling) support

The FPGA should be as small as possible and consume as little power as possible in order to meet our requirements as explained in chapter 3. Another rather obvious requirement is that the FPGA should have enough pins to be connected to all components on the PCB. A rough estimate by the Software Group led to the requirement of at least 2000 LUTs to run the desired software. Lastly, the external Mini-Amp-64 boards described in requirement 8 make use of SPI communication with LVDS signalling [32]. Therefore the FPGA needs a SPI controller and it should support LVDS. The functioning of LVDS will be explained in more detail in section 4.5.2.

These requirements led to the decision of using the MachX02-4000HC-6MG132C by Lattice Semiconductors. This FPGA belongs to the MachX02 FPGA family. This is a family of low power, instant-on, non-voltatile programmable logic devices (PLDs) [34]. This FPGA family has 6 devices ranging from 256 to 6848 Look-Up Tables (LUTs). This family of FPGAs supports LVDS (certain models) and has

an SPI controller. The model that was chosen for this design has 4320 LUTs. This was based on the requirement of at least 2000 LUTs estimate by the Software Group.

A choice had to be made between the HC, HE and ZE model:

- HC: This version of the device is powered using either a 2.5V or 3.3V power supply. It supports LVDS and has an internal voltage regulator that drops the supply voltage to 1.2V [34, 35]. It is specified as a high performance variant.
- HE: This version of the device is powered using a 1.2V power supply. It is also a high performance variant but is slightly more efficient than the HC model, because it does not have an internal voltage regulator [34]. It does not support LVDS [35].
- ZE: This version of the device is also powered using a 1.2V power supply. This version is optimized for low power and is slower than the other versions [34]. It does not support LVDS [35].

The decision was made to integrate the HC version. Firstly because our device uses LVDS for communication with the external Mini-Amp-64 headstage [32]. Secondly because, our device will perform real time data processing which will require a fast FPGA. Lastly, the components on our device run on a supply voltage of 3.3V. Choosing one of the other models would mean having to use 2 voltage regulators instead of 1. This would take up more space on the PCB and possibly consume more power due to decreased efficiency.

The HC version is offered in 3 speed grades. -4, -5 and -6, where -6 is the fastest option. These speed grades mainly affect the timing characteristics of the device, such as the setup and hold times of the FPGA. Shorter setup and hold times allow for a higher maximum clock frequency of the FPGA, which results in higher performance. The fastest version was chosen because:

1. Choosing a faster option only changes the maximum clock frequency and does not immediately affect the power consumption. It allows for more freedom to meet timing.
2. Design freedom for the Software Group was a priority in this design. By choosing the fastest model, it is less likely that the hardware will be a limiting factor for timing or performance requirements.

Finally the package that was chosen was the 132csBGA because this was the smallest available for this version of the FPGA.

4.3. Power Distribution

The power subsystem is responsible for the distribution of power to all the components in the PCB. The system consists of the following components:

1. USB-C connector
2. Battery
3. Battery Charger
4. Power Mux
5. Low Dropout Voltage Regulator

These components will be discussed in more detail below. A schematic overview of the system can be found in figure 4.3.

As mentioned before, the Neuroscience department at EMC has already developed working Neurologgers. These devices do not have all of the same features, but they do have a working power distribution system. As stated previously, our design is the continuation of an initial design. This was done because having a working device that could be tested was our priority. Therefore, the choice was made to re-use the power distribution system of the previous Neurologger design as this would be almost guaranteed to work. Research was done into even smaller and efficient components for the power system which is discussed in chapter 7.

4.3.1. USB-C connector

Requirement 9 specifies that the device should be able to operate with either wired power or battery power. When opting for wired power it will be possible to do recordings until the storage capacity runs out. However, this option has the drawback of limiting the movement of the test subject as in this mode the PCB is constantly connected to an external power source. In this mode the power comes in via the USB-C port and is sent to the power mux. In order to draw power from the USB-C connector, the system has to adhere to the USB-C specifications. This is rather straightforward if the standard 5V is requested and no USB PD (Power Distribution) is required. As specified in the USB Type-C specification, a 5.1kΩ resistor should be connected between the CC pins of the USB-C connector and Ground (1 resistor per pin) [36]. This lets the connected system know that the device is a power sink and that standard 5V is requested.

In figure 4.3 a bidirectional connection can be spotted between the USB-C connector and the FPGA. These arrows represent the RX and TX lines of the UART communication interface that are connected to the Sideband Use (SBU) pins of the USB-C connector. These pins can be used, in combination with a external USB to UART converter or another UART device, to establish a UART connection with the Neurologger. This connection can then be used to, for example, change recording settings of the logger.

4.3.2. Battery and Battery Charger

When the battery-based capabilities are preferred, the battery can be used. Before use this battery has to be charged. In order to do this the PCB is temporarily connected to an external power source. The power comes in via the USB-C port and goes to the Lithium-Ion battery charger. After charging, the PCB can be disconnected from the external power source. The battery power is the other input to the power mux.

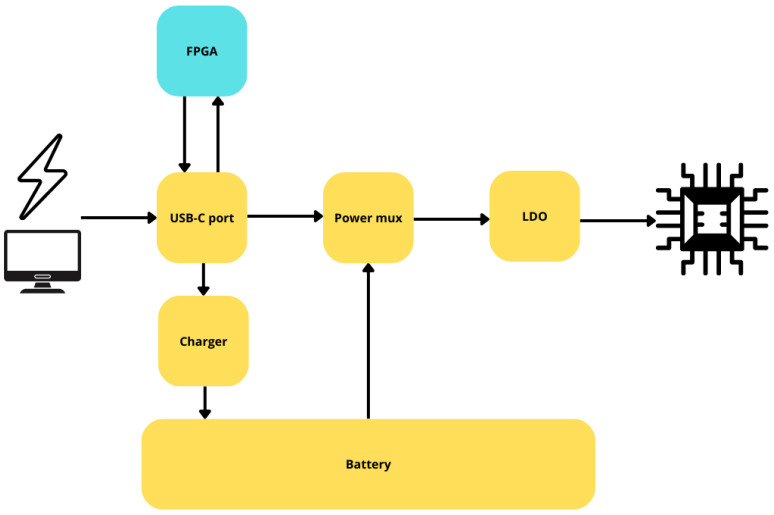


Figure 4.3: Power distribution schematic

4.3.3. Power Mux

Some way is needed to select which power source to use, this is done using a power mux. A power mux is a device that connects its output to 1 of the 2 inputs depending on a control signal [37]. This control signal can be either external or, as in our case, internally generated. The device is configured in such a way that it will automatically select the power source with the highest voltage. Since a Lithium-ion battery typically has a maximum voltage of around 4.2V and the USB standard is 5V, the external USB-C power source will be selected when connected. This is of course logical because the external

power source is only connected when it is intended to be used.

4.3.4. Low Dropout Voltage Regulator

After the power mux has made a decision on which power source to use, the power is diverted to the Low Dropout (LDO) voltage regulator. This component steps down the voltage from the external power source or the battery to the desired operating voltage of the PCB: 3.3 V. From here power is supplied to all the other subsystems.

4.4. Memory

The memory subsystem consists of a microSD card holder with a microSD card in it. It is powered by the power subsystem and takes data from the FPGA. After recording, the microSD card can be taken out an plugged into a computer to retrieve the data. A schematic of this system can be seen in figure 4.4. The power system is connected to all components but is left out here for clarity

The main reasons for using microSD storage are:

- Easily implementable
- Easily upgradeable
- Small form factor
- Sufficient data throughput
- High storage capacity
- Successfully implemented in neurologging devices [18, 19, 20, 21, 38]

Other options for storage are discussed in chapter 7.

The microSD that is chosen for our design has to satisfy the following requirements:

- **Minimum 32 GB of storage:** Following requirements 4 and 5, the system should be able to record 64 channels, at sampling speeds of 20 kHz with 16 bits per sample. This equals a minimum writing speed of around 2.6 MB/s, which would be for purely logged data without spike detection data. Recording for 1 hour would mean having to write about 9.2 GB/hour. Since the goal is to record for several hours, a microSD of at least 32 GB of storage should be used.
- **Minimum sequential writing speed of 4 MB/s:** As mentioned above, a rough estimate of the writing speed of the microSD should be at least 2.6 MB/s. Seeing as it is difficult to predict the actual sequential writing speed, the minimum sequential writing speed is taken a bit higher at 4 MB/s.

The Neuroscience department at the EMC already has a microSD from Sandisk with part number SDSQXCG-032G-GN6MA. It has a capacity of 32 GB and has speed class V30 classifications, this should give it a minimum sequential write speed of 30 MB/s [39]. This card matches our requirements and is therefore used in our design.

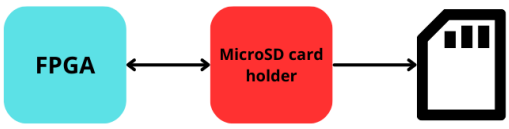


Figure 4.4: Memory system schematic

4.5. Analog Front-End

The final subsystem is responsible for processing the signals received by the neural probe and sending them to the FPGA. The schematic of this subsystem can be seen in figure 4.5. The power system is connected to all on-board components, but is left out here for clarity.

The analog front-end (AFE) is responsible for preparing the raw signals from the neural probes and sending them to the FPGA. How this is done varies in designs as certain priorities shift. In general, there are 3 main solutions.

First, there are multiple examples of designs in which the AFE is built from the ground up as an ASIC [26, 17, 24]. This generally leads to very small and efficient designs because every component of the design is optimized and chosen for a specific purpose. The drawback is that designing the AFE yourself takes a lot of time and resources, making it unsuitable for our design.

A second option would be the use of off-the-shelf components in order to build an AFE, this includes components for input filtering and the use of precision analog-to-digital (ADC) converters and amplifiers for digitization. A major downside of this solution is that it requires a large quantity of relatively big components which increase the required area, especially at higher channel counts. Therefore, this solution is more often used for EEG loggers which in general require less channels and have the added benefit of having readily available AFEs from manufacturers such as Texas Instruments (TI) [40].

The third and last option is presented by Intan Technologies, which makes AFE chips specifically for use in Electrophysiology recording devices. Their chips are widely used on existing devices [32] and are already in use in research by the EMC Neuroscience department [6]. Tests on the performance of this chip can be found, which led to the conclusion that while the chip can produce minimal ADC artifacts, no compelling alternatives to the Intan chips have been found [41]. These chips offer very high channel count in a small package without the need for large external components. Some highlights of the Intan RHD2000 family include:

- Available in 16 (differential),32 (unipolar) and 64 (unipolar) channels
- 16 bit quantization
- SPI interface with possibility for LVDS signaling
- Up to 30kHz sampling per channel
- Configurable upper and lower cutoff frequency
- Electrode impedance measuring capabilities
- Auxiliary ADC inputs for additional sensors

In the end, the choice was made to go with the Intan chips as AFE mainly due to their very compact size, but other factors include their good performance, low effort of implementation, and widespread use in existing systems. Furthermore, this choice was reinforced by requirement 8, which requires the integration of the Intan RHD2164 on the Mini-Amp, meaning that integration of on-board Intan-chips would be simplified. The final system will consist of 2 RHD2132 Intan chips [42]. This leads to having 64 on-board channels which makes our design meet requirement 4. The choice (and requirement) for 2 32-channel chips instead of 1 64-channel chip stems from the fact that each chip only has a single reference. Having 2 separate chips and thus 2 separate references gives more flexibility in possible research as it makes it possible to get more accurate measurements when, for example, measurements are made in 2 separate brain regions (which might have a different base/reference potential).

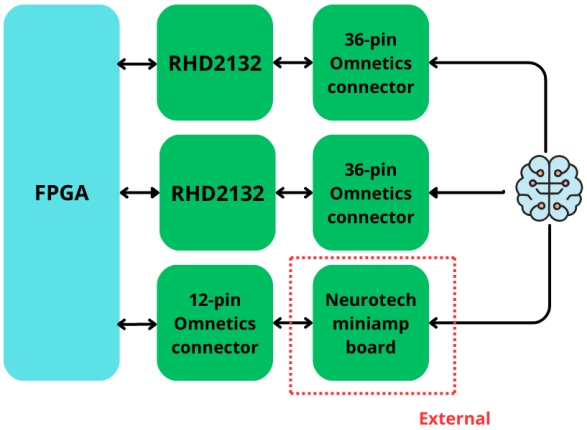


Figure 4.5: analog front-end subsystem schematic

4.5.1. Probe connectors

The on-board Intans are connected to 2 different neural probes via 2 36-pin Omnetics connectors. These connectors were chosen for compatibility with the desired cambridge Neurotech probes. Furthermore, this connector is relatively easy to route compared to other industry standard connectors.

Another part of the subsystem is the 12-pin Omnetics connector. This connector is used to connect the PCB to an external Cambrdige Neurotech Mini-Amp-64 headstage [32]. This headstage has an RHD2164 Intan chip which is a 64-channel version of the RHD2000 family. The reason for the addition of this connector is because the Neuroscience department of EMC already uses these mini-amp modules, thus making our headstage compatible with the existing used hardware.

4.5.2. LVDS

The Intan chips use four-wire SPI with either CMOS or LVDS signaling to the FPGA for digital data transfer. LVDS stand for Low-Voltage Differential Signaling and is, as the name implies, a differential signaling standard. LVDS is often used when a low cost, high speed and and low power communication is needed.

LVDS has a center voltage of 1.25V with a 350mV swing as can be seen in the driver output in figure 4.7. This swing is generated by the driver by injecting a constant current of 3.5mA into the wires with the direction determining the voltage level. This current passes through a 100Ω termination resistance at the receiver end causing a voltage drop or rise over the resistor. The voltage polarity is then sensed by the receiver in order to determine the logic level. This process is illustrated in figure4.6. The value of the termination resistor is matched to the characteristic impedance of the cable to reduce reflections.

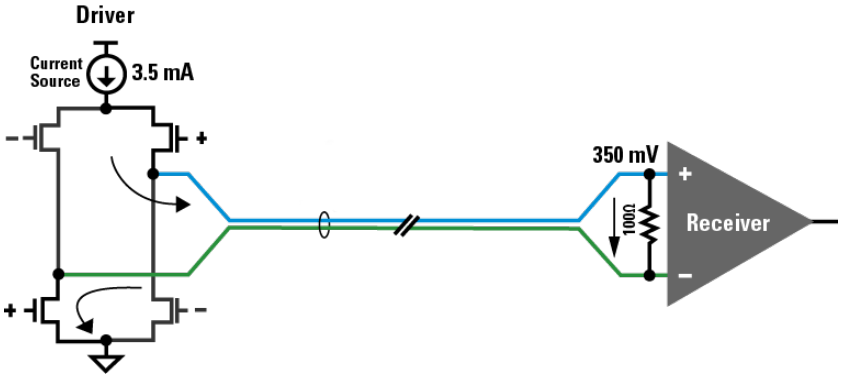


Figure 4.6: Basic LVDS circuit operation [43] (with modifications)

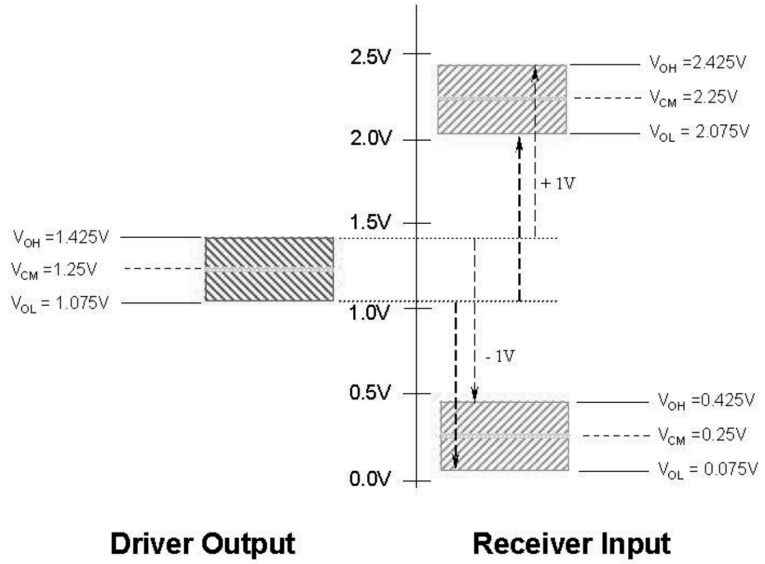


Figure 4.7: LVDS Common Mode Noise Range [44]

LVDS (and differential signaling) has a number of advantages over single ended technologies:

- The low center voltage and low swing make for a low power consumption.
- Differential signaling offers great common mode rejection, as much as a ±1V ground shift between the driver and receiver is tolerated [44].
- The lower voltage swing reduces reflections [44].
- The use of LVDS on the Intan does not introduce noise to the on-chip power supply [42].
  - Amplifier noise will be increased by 10% when the ADC is operated at 350KS/s with standard CMOS signaling. When operating the ADC at 1.05MS/s, amplifier noise increases by at least 30%. [42]
  - If low noise operations is required, standard CMOS signaling is recommend only up for ADC sampling rates up to 175KS/s. Using 32 channels, this gives a 5KS/s/channel sampling rate. [42]

For these reasons, the decision was made to use LVDS for the on-board Intans as well. Another consideration for this decision is the fact that the mini-amp boards use LVDS and the same signaling for both could give greater flexibility for both the routing and the software implementation.

5

PCB Implementation

In this chapter, the implementation of the PCB design is detailed and encountered challenges and decisions are discussed. The printed circuit board (PCB) design was created using the open-source software KiCad version 9.0.
This section will go over the main points and considerations that were made during the PCB design aspect of the project.

5.1. Schematics

As mentioned in chapter 1, at the beginning of the project a set of almost finished schematics were provided. They are fairly straightforward due to a low component count, and their contents can be summarized as the interconnection of all components according to their datasheets. There are, however, 2 key points that require a bit more attention as they impact the functionality and the routing of the PCB.

5.1.1. FPGA pin map

The pin map of the FPGA was configured in deliberation with the FPGA (software) team using the Lattice Diamond Software in order to ensure the chosen pins can be configured with the needed functionality.
Several different functionalities are needed to implement the logger. For debugging and flashing purposes, the dedicated JTAG pins are needed. General Purpose Inputs and Outputs (GPIO) are needed for the communication with the SD card, the UART implementation on the USB and for driving the LED. Finally, LVDS input and output signal pairs are needed for communication with both the internal and external Intan ADCs. These functionalities are distributed on I/O banks on the FPGA.
In total, there are 6 different I/O banks on the MachXO2-4000[34] which can be seen in figure 5.1.

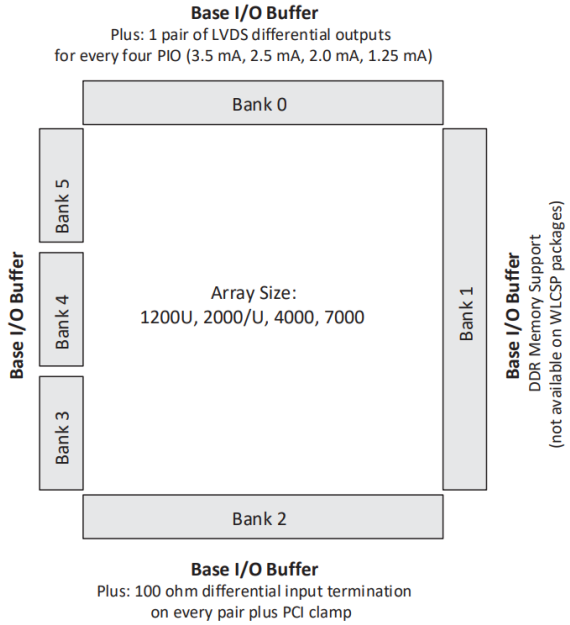


Figure 5.1: MachX02-4000 I/O banks [35]

These I/O banks are not identical in capabilities and thus one has to pay attention when selecting pins. All banks have pins capable of generic single-ended I/O and thus the most convenient pins for routing can be selected. This is not the case for the JTAG and LVDS pins, where the following restrictions apply:

- The JTAG pins (TDO, TDI, TMS, TCK) have a fixed pin on bank 0 and cannot be changed.
- 5 True LVDS outputs are present on bank 0, other banks only support LVDS emulation.
- Differential inputs with termination are only present on the bottom side (bank 2) of the FPGA, other sides/banks support differential input without termination.

This gives a set of restrictions which must be taken into account during routing.

An important note to make here is that the last condition regarding terminated input for differential pairs was unfortunately overlooked during design and only found during the writing of this section (and after the ordering of the PCB), in the next subsection it will be explained why this might be an issue.

5.1.2. Intan termination

In section 4.5.2 the use of LVDS for both the internal and external Intan ADC's was explained. As explained, LVDS is a differential signaling scheme that requires a 100Ω termination resistor placed close to the receiver (in the case of a single point-to-point configuration). There are, however, a number of different situations that must be taken into account when designing the termination, which stem from requirement 8 and the fact that the Cambridge Neurotech Mini-Amp 64 boards have on-board termination for the receiving signal pairs. This results in the following scenarios:

- Internal Intans are used without external Intan connected.
- External Intan is used with internal Intans present. Note that this scenario is undesirable due to the extra power consumption of the on-board and unused Intans and is therefore less likely to occur.
- External Intan is used without internal Intans present.

There are 3 logical solutions which can be used in case true LVDS is desired.

1. A single set of signals for both the internal and external Intans.
   This will most likely result in a center driven multi-drop configuration [44] (see figure 5.2) in case the exernal intan is connected. In this case 2 termination resistors are needed in order to prevent reflections from either end of the line, the driver will see these 2 resistors as parallel and therefore must provide twice the current to drive the bus, doubling the power consumption on that LVDS pair. When the external intan is not present the stub/branch length needs to be highly minimized in order to prevent reflections. This also applies to the branches on the on-board intans.
   Furthermore, this will increase the complexity of the software since all three of the previously described scenarios have to be taken into account for the configuration of the Intans.
2. Using a physical switch or a multiplexer to switch the LVDS lines over from internal to external (or vice versa).
   In this solution, multiplexers or switches are placed close to the FPGA which will allow either the user or the FPGA to switch over the LVDS pairs from internal to external. This requires the use of rather large components and will significantly affect the routing of the signal pairs.
3. Using completely separate dedicated LVDS lines for the internal and external Intans.
   In this case 6 LVDS outputs and 4 LVDS inputs would be needed. As mentioned in the previous subsection, the FPGA only has 5 LVDS outputs, which means 1 of the output signal pairs will need to be shared. This is possible since it is an output pair and the not-connected Intan has no way to send any signal back to the FPGA or cause interference on other signal lines since they are completely separated. This will however, increase the power consumption on this signal pair due to the double termination (see figure 5.2) A disadvantage of this solution is that it heavily increases the number of signals on bank 0 of the FPGA which increases routing complexity.

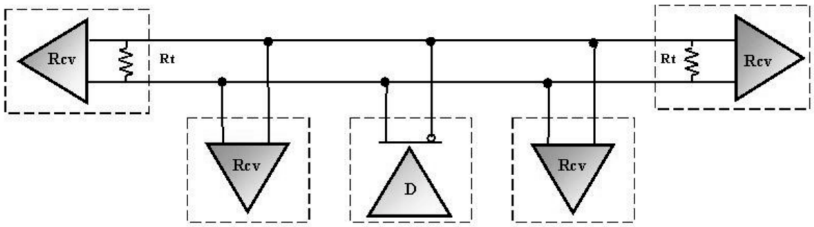


Figure 5.2: Center driven multi-drop LVDS configuration [44]

Solution 3 was chosen because it has the least impact on power consumption and required board space while having only a slightly higher routing complexity as the other 2 solutions.
The Chip-select (CS) signal was chosen as the differential pair that would go to both the internal and external Intan's as it has the lowest frequency (in terms of how often it changes).

5.2. Routing

This subsection will go over the main consideration for the PCB routing and explains how the design came to be.

5.2.1. Component placement

Before the PCB can be routed, it is generally recommended to first start with placement of large components and components that have restrictions, as these have the biggest effect on the design. For the headstage, there are a number of restrictions that must be taken into account which stem from requirement 1. Working out this requirement, we end up at the following set of restrictions for the placement of components. A visualization of the (final) layout can be found in figure 5.3.

1. The USB-C connector must be on the edge of the board
2. The SD-card holder must be on the same edge of the board as the USB.
3. The 12-pin Omnetics connector for the Mini-Amp board must be on the opposite edge and opposite side (think: top and bottom) as the USB and SD-card holder

4. The 2 36-pin Omnetics connectors for the probes must be on the same side and same half as the 12 pin Omnetics. However, they can be at a 90 degree angle to the 12-pin connector. They must be on the edge of the board.

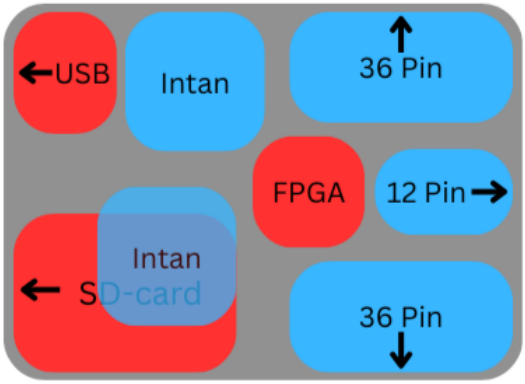


Figure 5.3: PCB Layout and component restrictions (Red: top layer, Blue: bottom layer)

Furthermore, a number of restrictions can be set due to the selected components.

1. No large components can be placed on the opposite side as the USB due to it's through-hole pins.
2. No components except for decoupling capacitors can be placed on the opposite side of the FPGA due to use of via-in pad.

The use of via-in pad for the FPGA is required due to the small pitch of the FPGA's Ball Grid Array (BGA) package in combination with the production capabilities of the used manufacturer. These two conditions together make it impossible to route a (minimum width) trace between two pads of the FPGA and still meet the required spacing requirements set by the manufacturer.

The placement seen in figure 5.3 is the final layout and has been optimized for minimal surface area while not increasing the routing complexity too much.

5.2.2. PCB stackup

The PCB uses a 6-layer stackup which is characterized in table 5.1. A 6 layer board was selected in order to accommodate the high density of traces between the Intan chip and the 36 pin Omnectics connector while still having a dedicated power- and ground-plane. The inner signal layers are used to route the analog input signals and some LVDS signal pairs as will be seen in the next subsection. The colours in this figure have been matched to their respective layer's colour in KiCad.

Layer	Type
1	Top signal layer
2	Power plane
3	Inner Signal Layer 1
4	Inner Signal Layer 2
5	Ground Plane
6	Bottom Signal Layer

Table 5.1: PCB Stackup

There is extensive literature giving recommendations when determining the layer stackup of a PCB to

reduce the effect of Electromagnetic Interference (EMI)[45]. In the end, the choice was made to put the Ground-plane closest to the bottom signal layer since signal integrity is of most importance for the analog signals on the bottom layer and the 2 Inner signal layers.

5.2.3. General routing considerations

The final routing can be seen in figure 5.4, the colours are matching the colours in table 5.1.

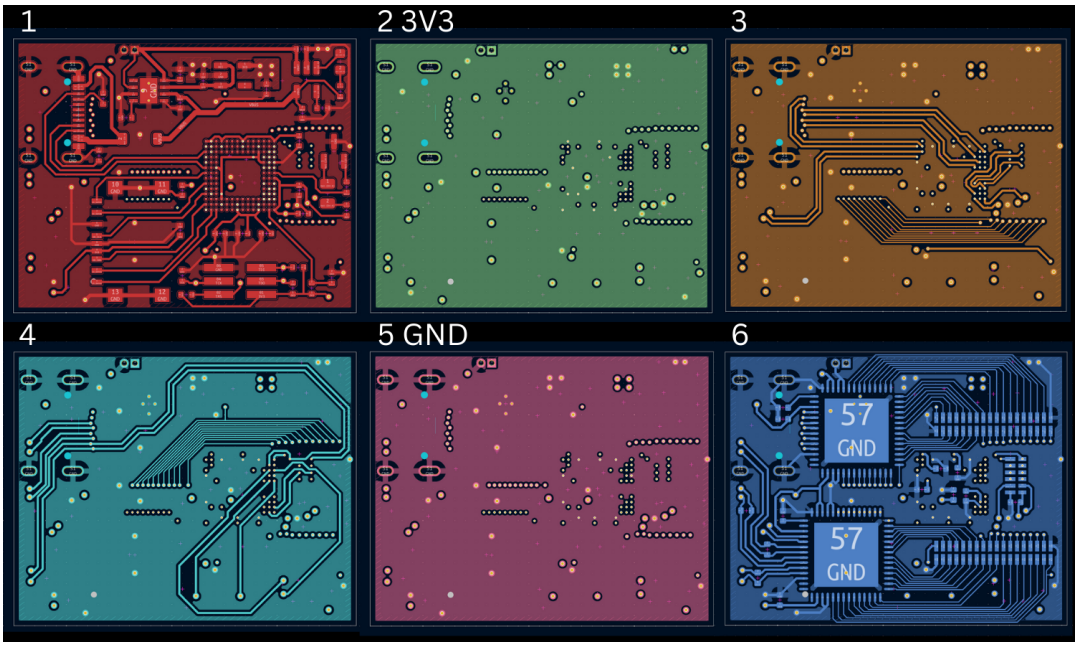


Figure 5.4: PCB Layers and Routing

Some key considerations that were taken into account during routing can be found in this figure:

- The intact 3.3V power-plane and the ground-plane can be seen in layers 2 and 5, respectively.
- The placement and orientation of the Intans were determined so that the trace length of the measurement signals can be kept to a minimum and the number of signals on the bottom layer can be maximized.
- A small trace width (0.1mm) is used for the measurement signals in order to increase the density of these signals, thus minimizing the needed area. The trace width has very little effect on the measurement value due to the very high input impedance of the Intan (MΩ range [42]) combined with the very low amplitude of the measured signals. The trace resistance is in the range of (0.15 to 0.3Ω, resulting in an error (voltage drop in the trace) in the zepto-volt (10^{-21}) range)
- Care was taken to minimize overlap between the LVDS pairs on layers 3 and 4 and the analog measurement signals on layer 6.
- The orientation of the FPGA was chosen so that the traces are as straightforward as possible, avoiding the need to cross signals by the use of vias and the use of other layers.
- The 12 pin Omnetics connector is offset to 1 side in order to be able to accommodate the mini-amp board with the 36 pin Omnetics connectors soldered on. This offset on the mini-amp board can be seen in figure 5.5.

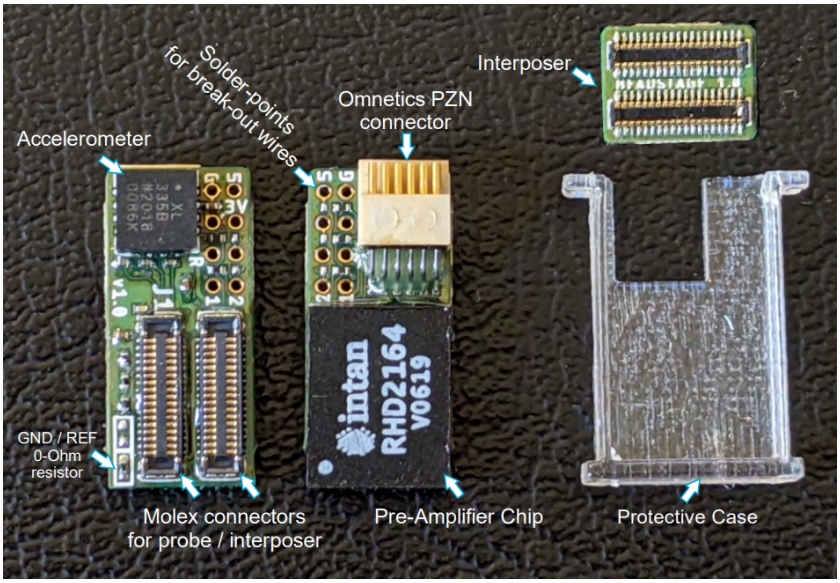


Figure 5.5: Cambridge NeuroTech mini-amp-64 [46]

6

Evaluation

Only limited results could be obtained due a lack of testing time which was partially the result of incurred delays due to the unavailability of both the FPGA and SD card holder at the supplier. Nonetheless, some testing was done, the results of which will be presented in this chapter. Furthermore, this chapter will describe a testing procedure that can be used to verify the functionality of the neurologger.

6.1. Testing procedure

The following procedure will be followed to test the functionalities of the logger. It assumes all required components have been soldered on. Some components can be left unsoldered if their functionality is not required (for example the internal Intans). The procedure can be split up into 2 main parts, a part that requires FPGA software and a part that requires no FPGA software. The second part covers the testing of the power distribution system and goes as follows:

1. Solder on the required components
2. Ensure that no shorts are present on the PCB
3. Power on the system using the USB-C connector
4. Power on the system using a battery
5. Test the battery charger by plugging in the USB-C with a battery connected
6. Test the mux by powering up the PCB using either power source, connecting the second source and then disconnecting the first source. The Neurologger should remain powered.

The second part of the testing procedure looks as follows:

1. Power up the system
2. Confirm JTAG communication with the FPGA using the programming tool
3. Program the FPGA with the desired software
4. Subsystem testing
    a) Confirm the led can be turned on and off
    b) Confirm SD card writing code
    c) Confirm functionality of the Intans (all configurations), run the validation commands, check response to the initialization commands
    d) Confirm UART communication with the FPGA is possible (if implemented)
5. Confirm channel data can be received from the Intan and written into the SD card
6. Connect with a wire to a external Intan on a mouse and check if data can be recorded
7. Mount the Neurlogger onto a mouse and use the internal Intans to record data

Furthermore, a number of tests can be run to further extract specifications and parameters from the Neurologger

- Power measurements: measure the power consumption of the device while enabling/disabling different subsystems. This gives a rough idea of the power consumption per susbystem.
- Weigh the Neurologger
- Battery test: connect a battery and continuously log data to the SD card from a full charge, check how long the battery lasts.

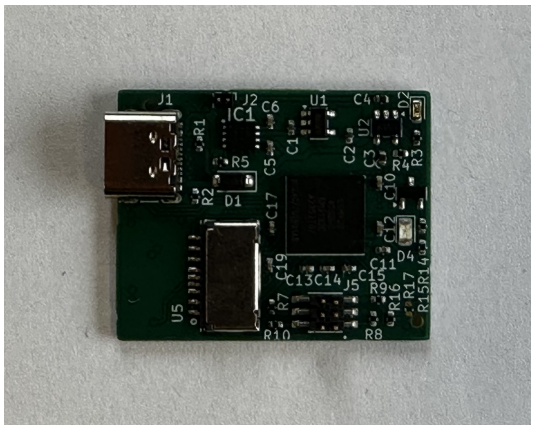
PCBA (PCB assembly by the PCB manufacturer) was used for the assembly of the PCBs, but as can be seen from figure 6.1b the bottom side of the logger was not assembled. The bottom side of the Neurologger contains the Intan chips, Omnetics probe connectors, Omnetics mini-amp connector, termination resistors and decoupling capacitors for the FPGA. There are a number of reasons for this:

1. Significantly higher price of the Omnetics connectors at PCB manufacturer.
2. Omnetics connector are not in stock or not known in inventory system at the PCB manufacturer.
3. Intan chips are not in the system at the PCB manufacturer due to being very application specific and not widely used. It is possible to sent in customer components, however, this would cause significant delays in the production process.
4. High price of Intan chips compared to the rest of the logger.

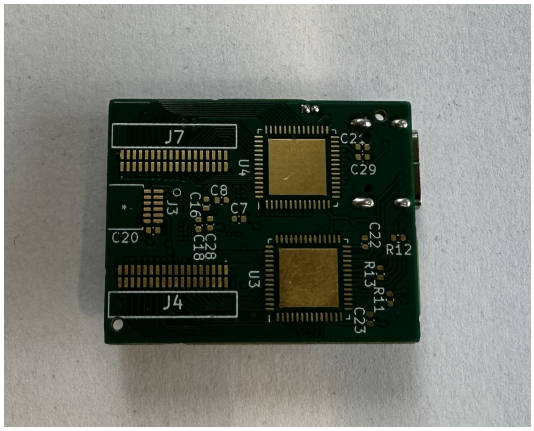
Overall, the high price of the Omnetics connectors and Intan chips is one of the main considerations to not solder these components on immediately. The decision was taken to only solder on the components once all other functionalities of the Neurologger have been tested to reduce the chance of destroying an Intan chip and to reduce the chance of needing to desolder these components in case of the PCB not functioning correctly.

6.2. Results

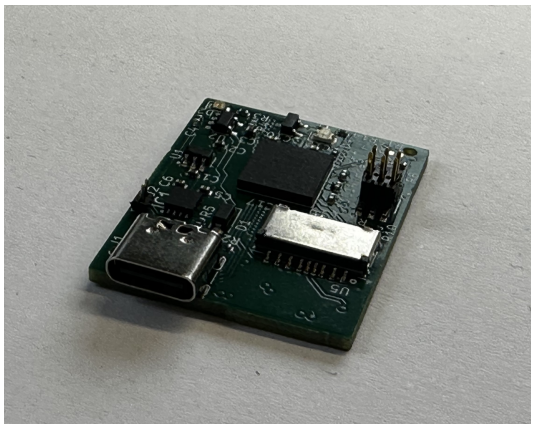
Pictures of the Neurologger can be found in figure 6.1, the final specifications are presented in table 6.1 along with the specification of the previous loggers developed by the Neuroscience department at the EMC. A comparison picture between the three versions can be found in figure 6.2.



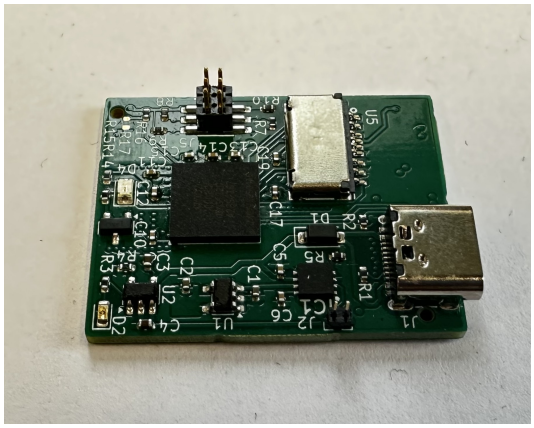
(a) Top



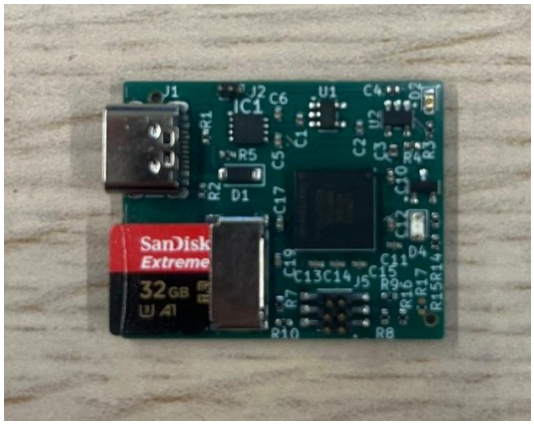
(b) Bottom



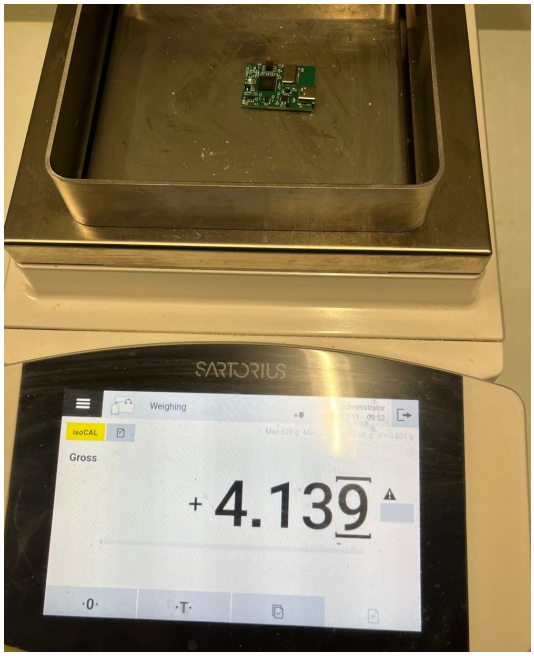
(c) Side



(d) Side



(e) Neurologger with MicroSD



(f) Neurologger weight

Figure 6.1: Neurologger

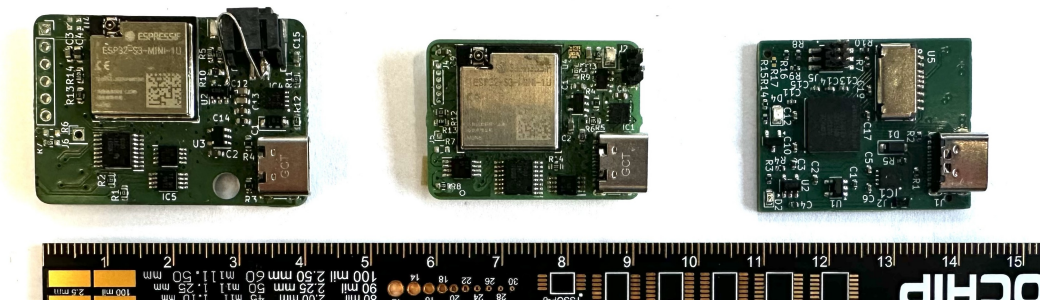


Figure 6.2: Neurologger comparison (V1: left, V2: middle, V3: right)

Neurologger specifications			
	Version 3	Version 2	Version 1
Bit depth	16	16	16
Channel count	2x32	1x64	1x64
Sampling frequency	30kHz	30kHz	20kHz
Bandwith	0.02-20000Hz (tunable)	0.02-20000Hz (tunable)	0.02-20000Hz (tunable)
Weight	4.139g w/o	∼4g w/o	∼7g w/o
Size	34.2x26mm	33.5x23.5	39x27
Communication interface	SD card storage + UART	SD card storage + USB	SD card storage + USB
Power consumption	TBD	215mA	–
Features	LED	–	–

Version 1 and 2 do not have any onboard AFE/Intan, specifications are using Cambridge Neurotech mini-amp-64

Table 6.1: Neurologger specifications

From this table we can see that version 3 has roughly the same dimensions and weight as the previous version. However, this version includes 2 onboard 32 channel Intans allowing the connection of 2 separate probes with 2 different references. Furthermore, this removes the necessity for external mini-amp boards of which dimension and weight are not taken into account in this comparison. While this verion does lack the native USB support, this can be easily resolved using a USB to UART converter as described in chapter 4.

6.2.1. Weight

One thing that stands out from this table is the relatively high weight (see also figure 6.1f), especially taking into account that not all components are soldered on. The exact cause of this is hard to pinpoint as individual component weights are not given by the manufacturer and the density of the PCB stackup itself is also unknown to the manufacturer. When compared to version 2 that has similar dimensions, it can be seen that a similar weight was achieved.

6.2.2. Power consumption

Although no testing of the power consumption of the system could be done, an estimate can be made using datasheets of the main components and power consumption data of the previous loggers. The power consumption of the subsystems have been calculated with a supply voltage of 3.3V. A summary of this analysis can be found in table 6.2 and is explained in more detail below:

- **FPGA subsystem:** Using estimates provided by the FPGA software group (which were obtained using the Lattice Diamond software), we arrive at an estimated current draw for the FPGA of 40.4

mA. This estimation is for logging of all the channels and single channel spike detection. We estimate the LED to have a effective current draw of 1 mA assuming it blinks every 0.1 s. This leads to a total current draw of 41.4 mA for this subsystem.

- **Memory subsystem:** The memory subsystem in the Neurologger V2 had a current draw of about 40 mA. The estimate for our current draw is 35 mA seeing as we anticipate the system to be slightly more efficient using an FPGA instead of a microcontroller.
- **AFE subsystem:** Using the datasheet of the RHD2132 Intan chips [42] at a sampling rate of 20 kHz we arrive at a current draw of 20.80 mA for 2 Intan chips.

	Current draw (mA)
FPGA subsystem	41.4
Memory subsytem	35
AFE subsystem	20.80
Total	97.2

Table 6.2: Current draw Neurologger V3

Even though our Power subsystems does have some idle current draw, the main losses come from the LDO voltage regulator. In section 7.1.2 it is explained that the LDO with our battery has an efficiency of about 89.1%. This means that with a battery of 195 mAh (3.7V nominal voltage), the total effective available energy is 643.5 mWh. Assuming a current draw of 97.2 mA, we arrive at an estimated battery life of approximately 2 h.

6.2.3. Testing progress

The Neurologger has been successfully powered up using a USB cable. JTAG communication has been confirmed and the FPGA is successfully identified in the Lattice programming software. Furthermore, the FPGA can be successfully programmed with the desired software. While this leaves a lot of subsystems to be tested, the apparent functioning of the FPGA is already a major success. The used test setup can be seen in figure 6.3.

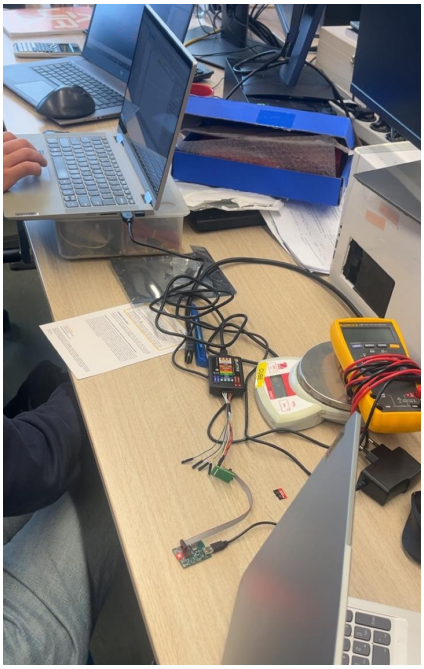


Figure 6.3: FPGA flashing setup

7

Future work

In this chapter, we go over various improvements on our Neurologger V3 design in order to propose an improved version. As previously mentioned, the design of the PCB was built on an initial design. The priority was having a tested, working device by the end of the project. Choosing and implementing a whole set of new components did not fit in our design process as we had to account for manufacturing and delivery time of the PCB. This part of the design is however very important and was done during the design process of the current iteration. Using the research we did and the knowledge we gained designing the Neurologger V3, we were able to make a proposal for an improved version of the Neurologger. After deliberation with our daily supervisor, the priorities for this fourth iteration became:

- **Smaller form factor**
- **Higher number of channels**
- **Improved battery life**
- **Maintaining user-friendliness**

Table 7.1 summarizes the changes made for the fourth iteration.

7.1. Changes per subsystem

7.1.1. FPGA

Research was done into options for a smaller and more efficient FPGA. It is important that this FPGA is able to meet our requirements as described in chapter 4.2. Lattice Semiconductors makes even smaller FPGAs, like the FPGAs in the iCE40 LP/HX family [47] that come in packages that are at least half the size of our MachX02 device. At first inspection these FPGAs seem compatible with our system as they support LVDS, have enough I/O pins, an SPI controller and enough LUTs. However, a full evaluation would require an analysis of timing, hardware blocks and compatibility with existing code. Given the limited scope of this project, we decided to stick with the current FPGA for the proposal for the fourth iteration. Nevertheless, we encourage research into a different model for the FPGA, as this could provide improvements in battery life and form factor of the Neurologger.

7.1.2. Power

The power distribution system is very important for the overall efficiency of the design. Below all the components are discussed separately:

- **Battery Charger**: When operating the battery charger consumes little to no power as its only purpose is to charge the battery. Therefore choosing a different charger would not increase recording time. It does however take up space (3.1 mm x 1.8 mm) on the PCB. For the next design this component will be removed and the battery will be charged externally. This will save space.

- **USB-C port:** The measurements of the USB-C port are 9.00 mm x 10.7 mm. Firstly the option was explored to remove this component as it would not be used to charge the battery any more. The choice was however made to keep it for multiple reasons:

  1. Keeping the option for UART communication.
  2. Keeping the option for tethered power.

  Different connector options were also explored. Seeing as user friendliness remained a priority, we opted for USB-C connection as this can be directly connected to the computer or laptop of a lab researcher without needing a special adapter.

- **Power Mux:** Seeing as we wanted to have the option for tethered power in our fourth iteration, the power mux is a crucial component. The Power Mux that is used right now is the TPS2115ADRBT [48]. It has very low standby current and comes in a 3 x 3 mm package with an area of 9 mm^2. A convenient feature is that it automatically switches to the power source which has the highest voltage. We were able to find a smaller power mux that meets all our requirements: The TPS2117 by Texas Instruments [49] which comes in a 2.10 x 1.60 mm package. It has similar power consumption characteristics and is about one third of the size of the previous mux. It can be implemented to prioritize one of the 2 power inputs. For these reasons our current mux would be replaced with this new component.

- **Battery**: The battery that was used for the previous designs is the HPL402323-2C Lithium-ion (Li-ion) battery with a capacity of 190 mAh at a weight of 4.5g. A rough estimate of our current draw during recording is 100 mA. Li-ion batteries are known for having high power densities, making them suitable for our design as we need to match our needs for current delivery [50].

  Another option that is used in successful Neurologger designs [17] are Zinc-air batteries. These are light-weight, high energy density, single use batteries, meaning a lot of energy is stored in a small volume. Take the Renata ZA312 maratone+ [51]. This Zinc-air battery has a capacity of 180 mAh at 0,6g. This is a lot lighter at a similar capacity to our Li-ion battery and could therefore be a great improvement. The problem is however that Zinc-air batteries are known for their low power output capabilities [52]. This specific Renata battery has an output current of 2 mA in high drain mode. This is not nearly enough to power our PCB.

  For this reason the decision was made to stick with a Lithium-ion battery. The battery that is used now is too heavy, namely 4.5 g, which is almost as heavy as our maximum design specification in requirement 1. Therefore we chose to switch to a lighter Lithium-ion battery with lower capacity: The ICP641414PE by Renata batteries [53]. It has a capacity of 95 mAh, a weight of 2.7g and a maximum discharge current of 190 mA. Even though this design choice lowers the battery life of the device, the reduced weight of the Neurologger will produce more realistic measurements as the mouse will not be hindered by the device as much.

- **Voltage regulator:** Right now an LDO voltage regulator is used to lower the power supply voltage to the operating voltage of the PCB. Advantages of using an LDO are that it produces very little noise and has a stable output voltage. The efficiency of an LDO can roughly be estimated by using the following formula:

$$\eta = \frac{V_{out}}{V_{in}} \cdot 100\% \tag{7.1}$$

  The Lithium-ion battery that was used for the previous design is a Lithium-ion battery which supplies a nominal voltage of 3.7 V [54]. Using formula 7.1 and that the output of the voltage regulator should be 3.3 V, using an LDO with this battery gives an efficiency of roughly 89.1%

  An alternative that was explored was replacing it with a buck converter. Buck converters are known for their high efficiency. An example is the LTC3536 [55] which can reach efficiencies between 90-95 %. The drawback of these converters is that the voltage switching can create noise in other parts of the circuit. Seeing as we measure very small neural signals, this could pose problems.

  Since measurement quality is very important in our design, the decision was made to stick with an LDO voltage regulator. The small increase in efficiency is not worth the possible noise in our

measurements.

After research, an LDO voltage regulator was chosen that comes in a package of 2 x 2 mm [56]. This is less than half the area of the LDO that is used right now which comes in a package of 3 x 3.10 mm [57].

7.1.3. Memory

Our system should be able to record 64 channels, at a sampling speeds of 20 kHz with 16 bits per sample. This equals a minimum writing speed of around 2.6 MB/s. Recording for 1 hour would mean needing to write 9.2 GB/hour. Since the goal is to record for several hours, at least 64 GB of storage are necessary.

In the current design microSD storage is used for multiple reasons:

- Easily implementable
- Easily upgradeable
- Small form factor
- Sufficient data throughput
- High storage capacity
- Succesfully implemented in neural devices [18, 19, 20, 21, 38]

An alternative to microSD is eMMC storage. It combines NAND flash technology with a built in controller to create a robust storage system that is soldered onto the PCB. Its main advantages with respect to microSD are:

- **Slightly smaller form factor:** It takes up slightly less space on the PCB for our specifications of with typical measurements are 11.5 x 13 mm. MicroSD combined with the footprint of the connector has measurements of 11.25 x 15.15 mm.
- **Soldered onto the PCB:** It is therefore more robust, which can be useful for long recordings on the head of a live animal.

Some research is done on implementing eMMC storage on an FPGA [58], but not enough for a seamless transition in our design. The software would have to be rewritten and routing would become more complex due to the BGA (Ball Grid Array) package that it comes in [59].

We believe the mentioned minimal improvements do not weigh up against the increased complexity of the design. We know microSD works and is used in other designs. Switching to eMMC would unnecessarily complicate matters in our opinion. MicroSD meets our specification requirements and therefore the decision is made to stick with this storage type.

7.1.4. AFE

The AFE subsystem takes up the largest area on the PCB of all the subsystems. One of the priorities for the fourth iteration was achieving a higher number of channels. This becomes very hard when achieving a smaller form factor is also very important. Multiple options were explored:

- **Designing a custom AFE:** This option was also discussed in section 4.5. This would be a great option for optimizing the size and power consumption of the AFE. The drawback is that it takes a lot of time and resources.
- **Using 2 RHD2164 chips:** Intan has also made 64-channel versions of the RHD2132 chips that are used in the current design [42]. They are about the same size of the 32-channel version. Implementing these would double the amount of channels that can be recorded with on-board Intan chips. The drawback is however that the routing of the PCB will become a lot more complex as the amount of signal paths required for the AFE will double. This could potentially lead to a larger form factor.
- **Cambridge Neurotech 128-Intan probe [46]:** This probe by Cambrdige Neurotech (figure 7.1) has a built-in 128-channel Intan chip. It can connect to our Neurologger via the 12-pin Omnetics

connector that is implemented in the current design. The consequences of implementing this would be:

- **Drastically reducing the PCB area**: Seeing as the AFE subsystem on our Neurologger would simply exist out of a 12-pin Omnetics connector, the PCB could become a lot smaller. This can easily be seen in figure 5.3, where the 2 Intan chips and the 2 36-pin connectors would be removed. This would also mean that the PCB would require fewer signal layers, as there would not nearly be as many signal paths running through te PCB.
- **Doubling the channel count:** Using this probe would result in being able to record 128 channels instead of 64.
- **Not meeting requirement 6**: The drawback of implementing this design choice is that requirement 6 will not be met because only 1 probe can be attached to this device. This requirement can be met by simply adding another 12-pin Omnetics connector for a second 128-channel probe. This would however further decrease battery life and increase PCB area. On top of this, a re-evaluation of the FPGA would have to be done in order to ensure that these 256 channels can be logged without problems.

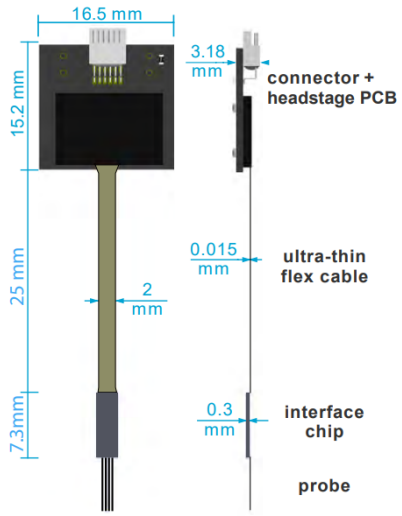


Figure 7.1: Cambridge Neurotech 128-Intan probe [46]

Because of the major improvements that using the Cambridge Neurotech 128-Intan probe would bring to the design, the choice is made to implement it in the proposal for a fourth iteration.

7.1.5. USB integration

A further possible improvement would be a more extensive integration of the USB port by supporting the USB2.0 standard. This interface could then be used to change settings of the logger or get data out of the logger. There are 2 main ways to achieve this:

- **Integrating the USB2.0 standard on the FPGA:** This would mean connecting the USB data lines to the FPGA directly and having it support the USB2.0 standard. This is generally not recommended due to the high complexity of implementing the USB2.0 standard, furthermore, this comes with a number of hardware requirements for the FPGA. Due to it's high complexity and the fact that the selected FPGA does not have native USB support, this option will not be further explored.
- **Integration of a USB to UART converter on the PCB:** In this solution a USB to UART converter is used in order to support the USB protocol and having UART communication between the FPGA and the converter.

The second option is a widely used solution for integrating USB on a PCB. These converter are more generally referred to as a USB PHY chip. These chips take digital input data and translate it to the

physical USB layer. The digital input can be in a number of formats (e.g. FIFO, I2C and UART) and are available from numerous manufacturers. A example of such a chip is the FT232RN[60] from FTDI chip. This is a USB2.0 to UART converters with a physical size of 5 by 5 mm, that requires minimal external components and supports UART at voltage levels from 1.8 to 5V. An import feature that many of these chips have is that they can be configured to be USB bus powered, meaning that they take their power from the external USB power source. The integration of such a converter thus does not affect the battery life of the logger. Therefore this component will be added in the proposed fourth iteration.

7.2. Neurologger V4 Design Summary

	Change?	What changed?	Impact on Neurologger
FPGA system			
FPGA	No	-	-
JTAG connector	No	-	-
Power system			
Charger	Yes	Removed	Area reduction of 5.58 mm^2
USB-C port	No	-	-
Battery	Yes	Replaced	Weight reduction of 1.8 g
Power Mux	Yes	Replaced	Area reduction of 5.64 mm^2
LDO regulator	Yes	Replaced	Area reduction of 5.3 mm^2
Memory system			
MicroSD card socket	No	-	-
Micro SD card	No	-	-
AFE system			
2 36-pin connectors	Yes	Removed	Area reduction of 194.93 mm^2
2 RHD2132 chips	Yes	Removed	Area reduction of 128 mm^2
12-pin connector	No	-	-
USB to UART converter FT232RN	Yes	Placed	Area increase of 25 mm^2

Table 7.1: Summary design changes V4

In table 7.1 a summary of the changes for V4 can be seen. The impact on the design as a result of these changes is discussed below:

- **PCB area reduction of at least 18.6%**: The changes resulted in a total area reduction of at least 314,45 mm^2. This will probably be more as the PCB will need less capacitors and resistors because of the removal of some components. Routing will also become easier due to a significant decrease in signal paths. This could possibly result in an even smaller form factor and will definitely reduce the weight of the PCB due to less signal layers being required.

  The PCB has 2 sides, both with a surface area of 32.5 mm x 26 mm = 845 mm^2. Its total surface area is therefore 2 x 845 mm^2 = 1690 mm^2. The proposed removal or replacement of several components would consequently lead to a surface area reduction of at least 18.6%.
- **128 channels:** The device will be able to record 128 channels due to the advanced neural probe by Cambridge Neurotech [46].
- **Battery Life of 54 minutes:** The removal and replacement of some components will reduce the idle currents drawn by the PCB. However, as a result of recording twice as many channels, the overall power consumption of the device will increase. Using 1 RHD2132 chip at full capacity consumes about 37.3 mW [42]. 1 RHD2164 chip at full capacity consumes about 53.1 mW [61]. We assume that this probe will contain 2 RHD2164 chips, seeing as Intan has released no information about the production of a 128 channel chip.

The power consumption ratio of the 64-channel chip with respect to the 32-channel chip is $\frac{53.1}{37.3} = 1.42$. This means that a doubling of the amount of channels will result in a power consumption increase of the AFE of about 42%. Seeing as the other changes to the device have minimal effect on the total power consumption, it can be concluded that the battery life will decrease. We believe this to be a justifiable trade-off, seeing as the logger will be able to record a lot more information and the device will become significantly smaller.

The use of a smaller battery reduces the battery life even further. Assuming a 42% increase in power consumption by the AFE subsystem, we arrive at a current draw estimate of 105.94 mA. With our new battery that has a capacity of 95 mAh, we arrive at an estimated battery life of 0.90 h or approximately 54 minutes. This still lets us meet requirement 2 with a significant decrease in weight.

- **Maintained user friendliness:** By keeping the USB-C port, the plug and play capability of the device is maintained as it can still easily be hooked up directly to the computer of a lab researcher. Furthermore by adding the USB to UART converter, communication with the device remains straightforward.
- **Weight reduction of at least 1.8g:** By choosing a battery that weighs 2.7g instead of 4.5g, the weight of the Neurologger decreases significantly. This will enable the mouse to behave in a more natural way as it is hindered less by the device. This will give more realistic measurement results.
- **Not meeting requirement 6:** Unfortunately, by choosing to implement the 128-channel probe by Cambridge Neurotech, only 1 probe can be attached to this Neurologger. Despite this limitation, the advantages of this design choice are considered to outweigh this disadvantage.

8

Conclusions

In this work, we presented the design for a compact battery-based Neurologger, that performs real time signal processing and neural spike detection using an FPGA.

In chapter 2 we provided an extensive analysis of the state of the art which shows comparable designs and their limitations. Multiple existing solutions are available on the market, however these suffer from the following limitations: a low number of channels, a sampling rate that is not high enough, an undesirable bandwidth, a limited battery life, a design that is too heavy or only capable of connecting to 1 neural probe. There is a design [29] that is very similar to our design specification wise. This headstage can perform optical stimulation while our design cannot do this. It however does not have our channel count, it does not have the option for spike sorting and does not have the option for connecting to 2 neural probes.

In chapter 3 the design specifications are determined and discussed. These set the foundations for the rest of the design process.

In chapter 4 the implementation is first discussed from a toplevel view and then divided in subsystems which are discussed separately. Implementation choices are justified using the earlier determined design specifications.

In chapter 5 the PCB implementation is discussed, which focuses mainly on the implementation of schematics and routing of the PCB.

In Chapter 6 we evaluate the results of the design. Limited testing was done due to time constraints, basic tests were however done to determine functionality. The device weighs 4.139 g without battery and MicroSD card and has measurements of 34.2 x 26 mm. It powered up using a USB cable and the FPGA was successfully programmed with the desired software. We see this as a great success, given the time frame of this project.

8.1. Thesis Contributions

Our achievements with respect to our design specifications and thesis goal are discussed below:

1. **The Neurologger, including its integrated battery, must have a total weight below 5 grams and a form factor suitable for attachment to a mouse without restricting its natural movement.**

   The Neurologger has a weight of 4.139 g without MicroSD card and battery. Including the battery and microSD card the device has a total weight of 8.89 g. Therefore we did not meet this requirement.

   Using the battery that was proposed for the Neurologger V4, a total weight of 7.19 g would be achieved. This would still not meet our requirement but be a nice improvement.

2. **The neurologger must be able to operate on battery for at least 30 minutes, with a target of 1 hour.**

   Our power consumption estimates with the current battery lead to a battery life of 2 hours. Therefore, this requirement is met.

   Using the battery that was proposed for the V4, a battery life of approximately 1 hour is estimated. Using this battery, we would also meet this requirement with a reduction in weight of 1.8g.

3. **An FPGA should be integrated to manage high-speed data handling and real-time signal processing of the acquired data.**

   An FPGA was implemented and flashed successfully. Therefore, this requirement was met.

4. **The Neurologger must be capable of monitoring 64 channels simultaneously.**

   The device is designed to record 64 channels simultaneously. Therefore this requirement was met.

5. **The channels that are logged by the Neurologger should each be sampled at a rate of at least 20 kHz.**

   2 RHD2132 Intan chips are implemented with a maximum sampling rate of 30 kHz. Therefore, this requirement was met.

6. **The Neurologger must be capable of connecting to 2 neural probes for neural recordings.**

   The Neurologger has 2 36-pin Omnetics connectors that are designed to connect to neural probes. These connectors are both connected to their own Intan RHD2132 chip. Therefore, this requirement was met.

7. **The Neurologger must include onboard storage capable of recording data from all channels at the full sampling rate for the intended duration of use.**

   The device has onboard storage in the form of MicroSD with enough storage to record for multiple hours at full capacity. Therefore this requirement was met.

8. **The Neurologger must be compatible with the Cambridge Neurotech Mini-Amp-64 headstage.**

   The Neurologger has a 12-pin Omnetics connector which enables it to connect with the Mini-Amp-64 headstage. Therefore this requirement was met.

9. **The Neurologger must support operation in both battery and wired modes.**

   The Neurologger uses a validated power distribution system that was designed to support operation in both battery and wired modes. Therefore this requirement was met.

10. **The Neurologger must feature an integrated Light Emitting Diode (LED) to facilitate synchronization and provide visual indication of system status during operation.**

    The Neurologger has an integrated LED. Therefore, this requirement was met.

Our thesis contributions are:

1. We performed an extensive research of the state of the art technology in this field. This was used to make design specifications for a unique neural logging device.
2. We developed a battery-based Neurologger that uses an FPGA that can perform real time signal processing and spike detection.
3. Initial testing of the Neurologger was done and a test-plan was presented in order to further validate the Neurologger.
4. An improved iteration of the device was designed for future development.

8.2. Future Work

In chapter 7, a design for a fourth iteration of the Neurologger was proposed. The most critical changes with respect to the current design are:

1. **PCB area reduction of at least 18.6%:** By removal and replacement of components.
2. **128 Channels:** Doubling the amount of channels in the current design.
3. **Battery life of 54 minutes:** Due to the increased number of channels and therefore power consumption of the AFE and the smaller battery, the device has a lower battery life than the V3. Requirement 2 is however still met with an estimated battery life of 54 minutes.
4. **Maintained user friendliness:** User friendliness is maintained by keeping the USB-C port and adding a USB to UART converter for straightforward communication with the device.
5. **Weight reduction of at least 1.8g:** By choosing a smaller battery the weight will be reduced by 1.8g. The removal and replacement of other components will probably also lead to a small decrease in weight.
6. **Not meeting requirement 6:** By implementing the 128-channel probe by Cambridge Neurotech, this device will only be able to log with 1 neural probe and will therefore not meet requirement 6. We however believe that the advantages of this design choice outweigh this disadvantage.

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