Ultrasound power RX ASIC design for wireless powering of brain implants

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by

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Acknowledgment

I would like to begin by expressing my heartfelt gratitude to my daily supervisor at IMEC-NL, Marios Gourdouparis, for his patient guidance and inspiring discussions. I learned so much from him, and every conversation with him brought me valuable insights that greatly enriched my research experience.

I am also deeply grateful to my supervisor, Professor Wouter Serdijn, for his constant encouragement and for sharing with me precious new ideas and perspectives. His support has been an important source of motivation throughout this journey.

My sincere thanks also go to Stefano Stanzione and Jesse Pasterkamp at IMEC-NL, who have always been friendly and willing to answer my questions. Their thoughtful responses often opened up new directions for me to explore.

I owe special thanks to my parents, whose continuous care and unwavering support gave me the strength to keep going during challenging times.

Finally, I would like to thank all the students at the IMEC-NL student corner, who made my days at IMEC-NL so joyful, colorful, and full of laughter.

The two years I spent in the Netherlands passed by in the blink of an eye. Along the way, I experienced moments of confusion and frustration, but also of joy and excitement. Above all, this journey has been one of the most meaningful and unforgettable periods of my life.

Mingyang Zhang
Eindhoven, August 2025

Abstract

Implantable medical devices, especially brain implants, show great promise for applications such as epilepsy detection, Parkinson's disease regulation, and brain–computer interfaces. However, battery-based power supplies suffer from degradation, surgical replacement risks, and limited compatibility with miniaturization, motivating wireless power transfer (WPT) as a promising alternative. Among various approaches, ultrasonic WPT is particularly attractive due to its strong penetration capability, no electromagnetic interference, and favorable safety profile. This thesis presents the design and implementation of a high-efficiency receiver (RX) circuit for ultrasonic WPT applications, with a focus on biomedical implants. Several rectifier topologies are investigated. Although the current-mode rectifier (CMR) demonstrates promising characteristics, its performance is significantly limited in ultrasonic WPT due to the low quality factor of the transducer. Consequently, the cross-coupled rectifier is ultimately selected for its simplicity and superior conversion efficiency. A boost converter is integrated to further increase the rectified voltage, with its duty cycle serving as the sole tunable parameter for impedance matching. Based on the maximum power transfer theorem, an adapted perturb and observe (P&O) maximum power point tracking (MPPT) algorithm is developed to dynamically adjust the duty cycle, thereby achieving automatic impedance matching and maximizing the power delivered to the load. The start-up issue is resolved through the implementation of a maximum-voltage selector, ensuring stable operation from system initialization. Simulation results demonstrate a peak overall system efficiency of 83.55%, with the cross-coupled rectifier and boost converter achieving efficiencies of 91.55% and 91.26%, respectively. The proposed system maintains high efficiency under varying load and input conditions, validating its feasibility for reliable and efficient power delivery in ultrasonic WPT systems for brain implants.

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Chapter 1

Introduction

1.1 Background

With the rapid development of medical diagnostic and monitoring technologies, the focus of research in the field of medical engineering is gradually shifting toward intelligent, integrated healthcare systems [1, 2]. In this trend, implantable medical sensors and devices have become a hot topic of research due to their unique advantages: they can enable long-term dynamic monitoring of conditions such as chronic diseases and neurodegenerative diseases while optimizing treatment plans through precise data feedback, significantly reducing the costs of repetitive examinations and hospitalizations. Especially in the field of brain implants, such devices demonstrate revolutionary potential in applications such as epilepsy warning, Parkinson's disease regulation, and brain-computer interfaces.

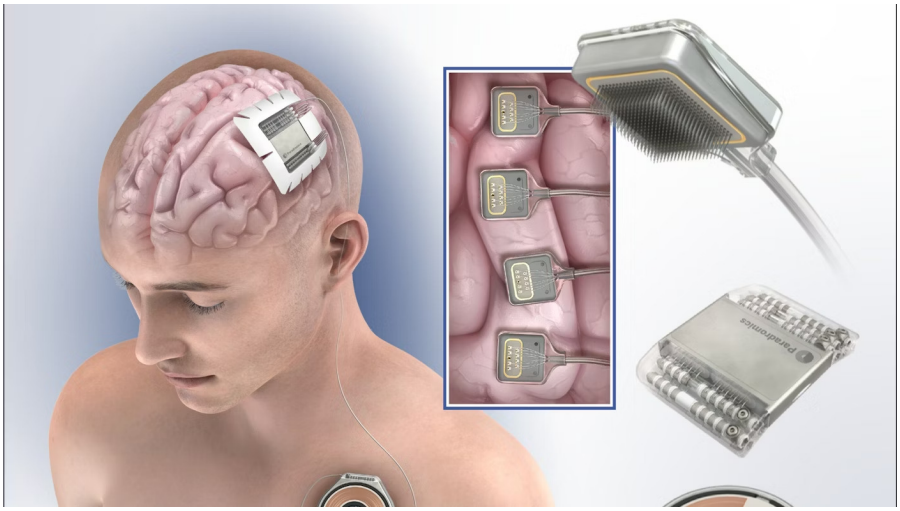
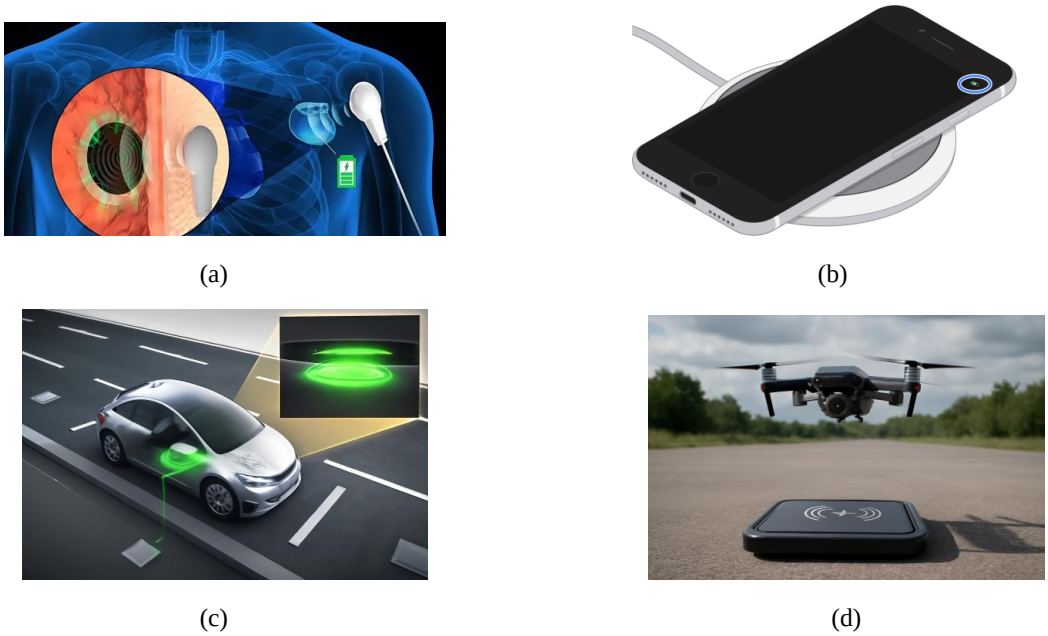


Figure 1.1: Brain implants [3]

However, the widespread adoption of implantable devices still faces core challenges, particularly the limitations of power supply systems. Traditional battery-powered systems have two major bottlenecks. On one hand, the unpredictable state of the battery after implantation, caused by nonlinear degradation, the influence of the in vivo environment, and the difficulty of accurately monitoring residual capacity, may lead to sudden voltage drops or unexpected failures, posing a critical risk to device reliability and patient safety. On the other hand, regular surgical battery replacements increase cumulative health risks such as infection, tissue damage, and procedural complications. In addition, the contradiction between the demand for miniaturization of future brain implants and the volume of high-capacity batteries has become increasingly evident. Device miniaturization is key to improving biocompatibility and reducing rejection reactions, but it also forces researchers to abandon high-power energy storage solutions.



(a) (b)

(c) (d)

Figure 1.2: Applications of WPT: (a) Implantable Medical Devices(IMDs)[4]. (b) Smartphone wireless charging. (c) electric vehicle wireless charging[5] (d)Drones wireless charging

To overcome this challenge, wireless power transfer (WPT) technology has emerged as a focal point of interdisciplinary research in recent years. This technology enables charging of implanted devices via an external energy transmission device, thereby completely eliminating the constraints of battery life. Patients no longer need to endure the risks associated with repeated surgeries. Current research is delving into areas such as energy transmission efficiency, safety of deep tissue penetration, and adaptive charging regulation. It is foreseeable that the maturation of WPT technology will drive implantable medical devices from ”passive

treatment" toward "smart health management," ultimately becoming a core pillar of future personalized healthcare systems. In addition to the medical field, WPT is also widely used in wireless charging for electric vehicles, mobile phones, and drones.

1.2 WPT System

The basic block of a WPT system is shown in Figure 1.3, which consists of two parts: the transmitter (TX) and the receiver (RX), while the former is placed outside and the latter is located inside the human body. At the transmitter, the power supply provides input power, and the power converter converts the power into a form suitable for wireless transmission. The receiver receives the wireless power through an appropriate receiving device (such as a coil or piezoelectric transducer) and converts it into usable power through a power converter for use by the load.

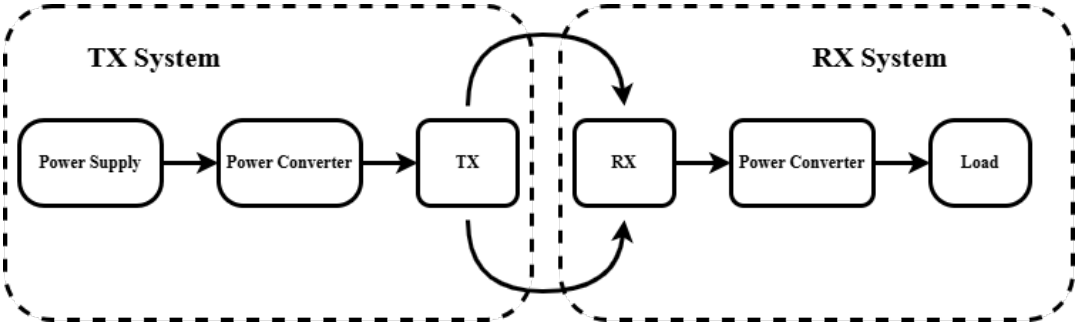


Figure 1.3: Block of WPT system

Based on its operating principle and application requirements, WPT technology can be categorized into five types: inductive-based, capacitive-based, radio frequency(RF), and ultrasonic-based WPT.

1. **Inductive-based WPT**: Inductive-based WPT is one of the most commonly used WPT technologies, relying on the principle of electromagnetic induction. In this system, an alternating current in the transmitter coil generates a time-varying magnetic field, which induces a voltage in the nearby receiver coil—thus enabling wireless energy transfer. This method also has some limitations. The power transfer distance is very short, and the efficiency drops significantly if the transmitter and receiver coils are not properly aligned. Nevertheless, due to its reliable operation, ease of implementation, and safety, inductive WPT remains widely used [6, 7].

2. **Capacitive-based WPT**: Capacitive-based WPT utilizes high-frequency electric field coupling between metal plates to achieve wireless power transmission. Its core principle

involves creating a displacement current path between the transmitter and receiver plates through an alternating electric field. Compared to inductive-based systems, capacitive-based WPT offers advantages such as simple structure, insensitivity to metallic environments, and cheaper cost. However, it has a significant limitation: the distance between TX and RX must be short enough [8, 9].

3. **Radio Frequency WPT**: RF WPT utilizes electromagnetic waves, particularly those in the radio frequency band (several hundred MHz to several GHz), to transmit electrical energy through the air or other media. The primary advantage of this technology is its ability to efficiently transmit energy over long distances, making it suitable for applications requiring long-range wireless power supply. However, the efficiency of RF WPT is generally lower than that of inductive coupling, and there is significant energy attenuation in human tissue. Therefore, biological safety must be considered, particularly the potential risks associated with prolonged exposure to high-intensity microwave radiation. To ensure human safety, RF WPT systems typically incorporate appropriate frequency, power, and safety limits in their design and comply with relevant electromagnetic radiation standards.

4. **Optical WPT**: Optical WPT utilizes electromagnetic waves in the optical spectrum (typically in the near-infrared band, such as 780-870 nm) to transmit electrical energy through air or transparent media in the form of highly directional light beams. Its core advantage lies in enabling highly efficient wireless power supply over long distances (ranging from tens of meters to kilometers), making it particularly suitable for specific scenarios such as space and underwater environments; however, the end-to-end energy conversion efficiency of this technology (typically 10-20%) remains significantly lower than that of short-range magnetic coupling technologies. Additionally, it poses risks of severe energy attenuation and thermal effects when penetrating biological tissues, necessitating strict control of eye safety risks. System design must strictly adhere to international safety standards such as the maximum permissible exposure (MPE) and ensure biological safety through mechanisms such as active beam interruption, dynamic power regulation, and reflection avoidance strategies.

5. **Ultrasonic-based WPT**: Ultrasonic WPT technology is a relatively novel method of wireless power supply that utilizes the propagation of ultrasonic waves through human tissue to achieve power transmission. This technology employs an ultrasonic transmitter to convert electrical energy into ultrasonic signals, which then pass through biological tissue. At the receiving end, an ultrasonic receiver converts these signals back into electrical energy. Compared to traditional electromagnetic wave wireless transmission methods, ultrasonic WPT offers several advantages. First, ultrasonic waves have short wave-

lengths and deep penetration capabilities, enabling them to penetrate conductive materials that are opaque to electromagnetic waves, making them suitable for more complex biological environments. Additionally, this technology does not produce electromagnetic radiation, thus posing no harm to the human body and causing no electromagnetic interference (EMI), ensuring high biological safety.

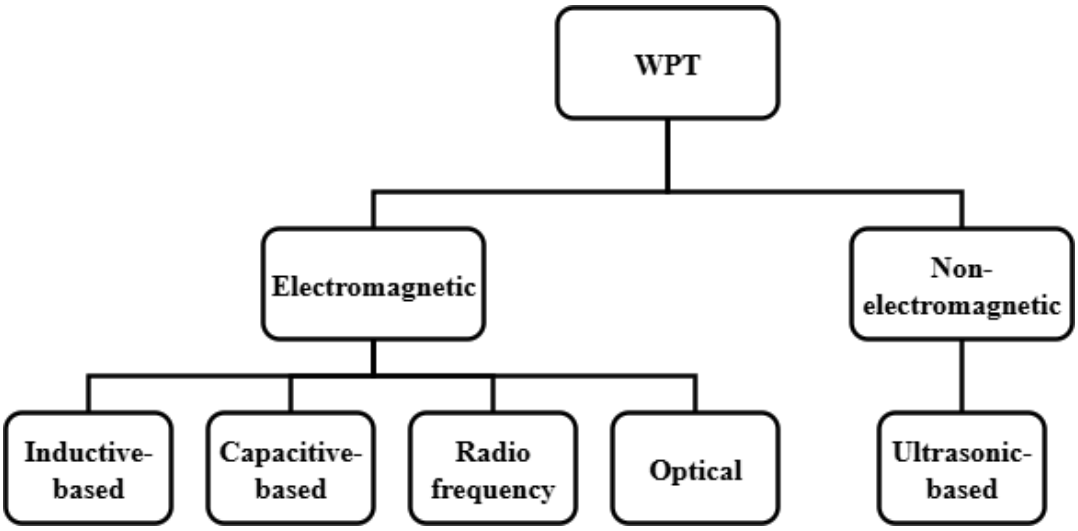


Figure 1.4: Classification of WPT

The following Table 1.1 summarizes the key advantages and disadvantages of each WPT technology. For WPT systems used in brain implants, several critical requirements must be met to ensure their effectiveness and safety. First, the system must prioritize safety, avoiding harmful electromagnetic radiation and ensuring that the specific absorption rate (SAR) complies with international safety standards to prevent any potential harm to human tissues [10]. Similarly, ultrasound and optical power transfer are also subject to strict safety limits, as excessive acoustic or light energy may damage neural tissue. Secondly, the system must possess good penetration capabilities, allowing energy to pass effectively through the skull and brain tissue, ensuring the deep delivery of power [11]. Additionally, the system needs to be compact and non-invasive, minimizing interference with surrounding tissues while fitting within the small constraints of brain implants [12]. Lastly, the system must be efficient in power transmission, providing sufficient energy to the implant while avoiding excessive heat generation, which could damage sensitive brain tissue.

Ultrasonic-based WPT is considered a promising approach for brain implants because it relies on acoustic rather than electromagnetic energy, thereby eliminating electromagnetic radiation concerns and minimizing interference with other devices. It also exhibits strong penetration and good directionality, which enable effective transcranial energy delivery. Furthermore, when operated within established acoustic safety limits, ultrasonic WPT demonstrates high

Table 1.1: Advantages and Disadvantages of Different WPT Systems

WPT System	Advantages	Disadvantages
Inductive-based WPT	Reliable, safe	Short range, misalignment reduces efficiency
Capacitive-based WPT	Simple, low cost	Short range, low efficiency
RF WPT	Long-range, efficient energy transfer	Health risks, low efficiency, energy attenuation in tissue
Optical WPT	Long-range, high directionality	Low efficiency, attenuation and heating in tissue
Ultrasonic-based WPT	Safe, deep tissue penetration, no EMI	Limited efficiency

biocompatibility and a favorable safety profile, making it a strong candidate for medical implant applications.

The scope of this study is limited to the design and optimization of the RX circuit in the WPT system. Based on the technical boundaries of the research objectives, all subsequent discussions will focus on RX modules. It should be noted that uplink system components such as the transmitter topology, excitation source design, and electromagnetic field coupling characteristics are not within the scope of this study and will therefore not be discussed in detail.

1.3 Ultrasonic Receiver

The process of receiving and converting ultrasonic energy is a key factor affecting the overall efficiency of the ultrasonic WPT system. The ultrasonic receiver transducer is a core component developed in this context. It primarily uses piezoelectric materials to convert ultrasonic energy passing through tissue into electrical energy to power devices inside the body. Figure 1.5 shows the working principle of piezoelectric material.

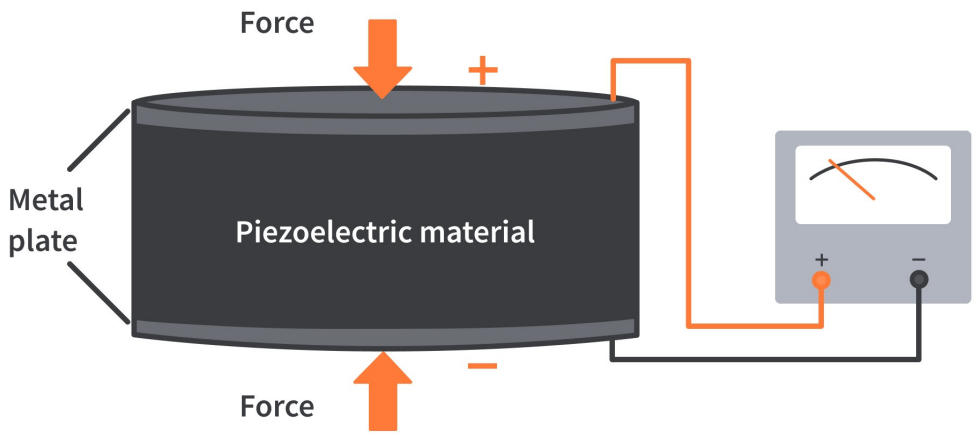


Figure 1.5: Schematic of the working principle of piezoelectric material power generation under force

To accurately describe the electrical response of piezoelectric elements at operating frequencies, equivalent circuits are typically used for modeling. The Butterworth-Van Dyke (BVD)

model is one of the most widely used modeling methods today [13, 14].

As depicted in Figure 1.6, the model consists of two parallel branches: one containing a shunt capacitor C_0, and the other comprising a series RLC circuit formed by a resistor R_1, a capacitor C_1, and an inductor L_1. The right branch is also called the electrical branch, it consists of a capacitor C_0 representing the static capacitance of the quartz crystal and associated parasitics. The left branch, referred to as the motional branch, includes a series combination of R_1, L_1, and C_1, which models the electromechanical dynamics and acoustic resonances of the system.

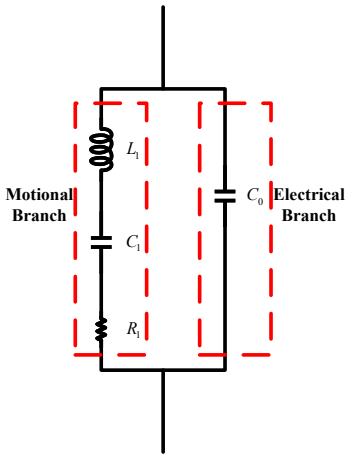


Figure 1.6: BVD model of piezoelectric material

This BVD model is commonly used to describe the behavior of piezoelectric resonators operating in the vicinity of their resonance frequency. The values of the equivalent circuit elements are determined by the transducer's width w, thickness d, and the intrinsic properties of the piezoelectric material. These properties include the relative permittivity ε_{33}^T, the electromechanical coupling coefficient k_{33}, the acoustic impedance of the material Z_C, and the acoustic loading impedances on the front and back surfaces, denoted by Z_F and Z_B, respectively. As described in [15], under the assumption of a rectangular transducer, the expressions for the circuit components are obtained as follows:

$$C_0 = \varepsilon_0 \varepsilon_{33}^T \left(1 - k_{33}^2\right) \frac{w^2}{d} \tag{1.1}$$

$$C_1 = \frac{8 C_0 k_{33}^2}{\pi^2 - 8 k_{33}^2} \tag{1.2}$$

$$L_1 = \frac{1}{4\pi^2 f_{sc}^2 C_1} \tag{1.3}$$

$$R_1 = \frac{1}{8k_{33}^2 f_{sc} C_0} \cdot \frac{Z_F + Z_B}{Z_C} \tag{1.4}$$

Here, f_{sc} denotes the short-circuit resonance frequency, and v represents the acoustic velocity of the piezoelectric material. The open-circuit resonance frequency f_{oc} is determined by the material's sound velocity and thickness t, and is given by:

$$f_{oc} = \frac{v}{2t} \tag{1.5}$$

The relationship between the short-circuit and open-circuit resonance frequencies is expressed as:

$$f_{sc} \approx \sqrt{1 - \frac{8k_{33}^2}{\pi^2}} \cdot f_{oc} \tag{1.6}$$

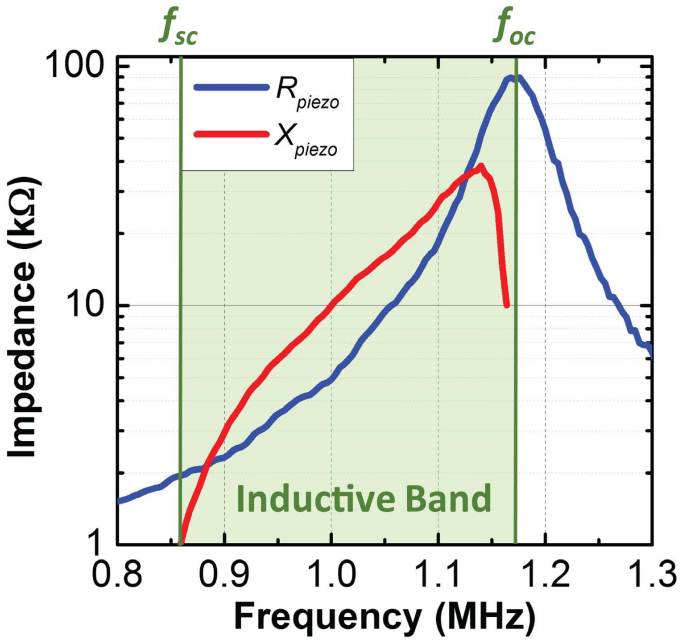


Figure 1.7: Inductive band [15]

The open-circuit resonance frequency f_{oc} corresponds to the frequency at which the output voltage reaches its maximum as the load resistance approaches infinity. Conversely, the short-circuit resonance frequency f_{sc} is the frequency at which the output current becomes maximum as the load resistance approaches zero. When the operating frequency of the ultrasonic receiver falls between the short-circuit resonance frequency f_{sc} and the open-circuit resonance frequency f_{oc}, the device exhibits an inductive impedance characteristic. This frequency range

is known as the inductive band (IB) [15]. As shown in Figure 1.7, the green region represents the IB region, where the reactance is positive.

1.4 Research Question

The main research question: How could maximum power transfer be achieved for brain implants?

Question 1:Which wireless power transfer method is most suitable for brain implants?

Question 2:How to choose the rectifier and DC-DC converter?

Question 3:What MPPT algorithms are suitable for brain implants?

Question 4:How can the MPPT algorithm be implemented in the circuit design?

1.5 Thesis Outline

In Chapter 1, the background of the thesis is presented, followed by an overview of the classification of WPT systems. The advantages and disadvantages of various WPT systems are analyzed, which leads to the selection of ultrasonic WPT.

In Chapter 2, various topologies of WPT systems reported in the literature are introduced, providing examples and insights for selecting appropriate system architectures.

In Chapter 3, the current-mode rectifier is introduced in detail. It is promising due to various advantages. However, it is not suitable for ultrasonic WPT.

In Chapter 4, an analysis of various rectifier topologies and DC-DC converters, as well as conventional MPPT techniques used in WPT systems, is presented. This chapter also details the overall system design.

In chapter 5, the PCB design of the receiver circuit is presented.

In Chapter 6, the thesis is concluded, and the contributions of the work are summarized. Additionally, directions for future work are discussed.

Chapter 2

Literature Review

In [16], a far-field microwave WPT system was demonstrated, featuring a retrodirective phased array transmitter and a receiver equipped with an impedance-matched antenna array and a full-bridge Schottky diode rectifier. The rectifier performs RF-to-DC conversion, followed by a low-pass filter to deliver a stable DC supply to the load. Through careful impedance network optimization, the system achieved a conversion efficiency of 75%–86% across varying load conditions, maintaining high performance even under elevated input power. However, the efficiency exhibits a noticeable drop at lower input power levels, primarily due to the threshold voltage and loss characteristics of the full-bridge diodes.

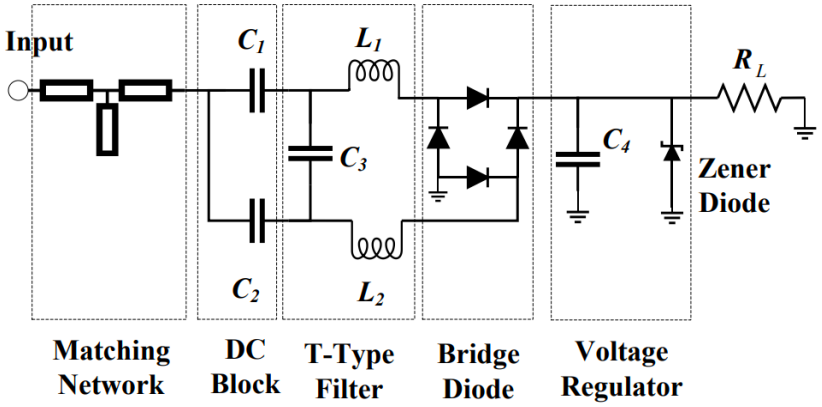


Figure 2.1: A receiver using full bridge rectifier [16]

In [17], a 13.56MHz reconfigurable resonant regulating (R^3) rectifier with 1X/2X mode was proposed. This architecture can give a stable output without implementing an LDO or a DC-DC converter. The schematic of the R^3 rectifier is shown in Figure 2.2(a). It has four switches: M_{P1},M_{P2},M_{N1}, and M_{N2}. Except for M_{P2}, all other switches are active and controlled by comparators. This configuration significantly reduces the voltage drop compared to a full

bridge rectifier. It has two working modes: 1X mode and 2X mode.

- **1X Mode**
  - S_1 and S_2 are turned on. S_3, S_4 and S_5 are turned off. Work as a full bridge rectifier
- **2X Mode**
  - S_1 and S_2 are turned off. S_3, S_4 and S_5 are turned on. Work as a voltage doubler.

1X and 2X modes can accommodate different load and coupling conditions. When the distance between coils is short or coupling conditions are favorable, the rectifier can meet output voltage requirements using the 1X mode; however, when the distance between coils increases or load demands grow, the rectifier must switch to the 2X mode to maintain stable output voltage by increasing the output voltage level. The mode switch is based on the error between the secondary-side output voltage and the target voltage, controlled by the local pulse width modulation (PWM) loop. The PWM controller detects the difference between the output voltage and the reference voltage, and achieves precise voltage regulation by adjusting the duty cycle of the rectifier between 1X and 2X modes.

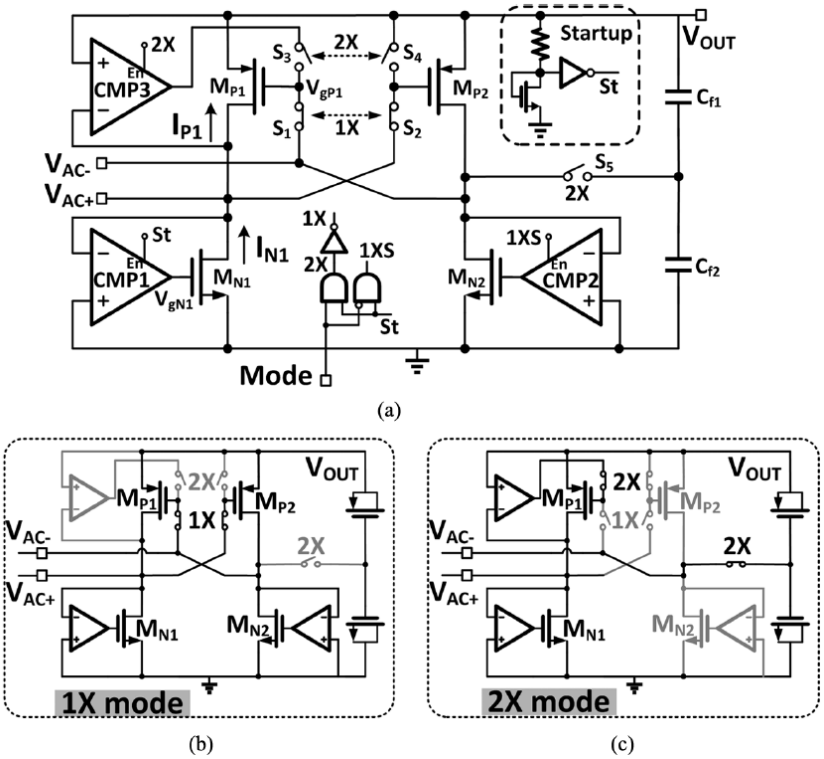


Figure 2.2: (a) Schematic of R^3 rectifier; (b) 1X mode of R^3 rectifier; (c) 2X mode of R^3 rectifier [17]

In [18], a cross-coupled rectifier structure is employed, as illustrated in Figure 2.3. The topology comprises two pairs of cross-connected transistors and incorporates an active threshold

voltage (V_{th}) compensation mechanism. This mechanism dynamically adjusts the gate bias of the MOS transistors connected to the diodes via differential signals, thereby reducing on-resistance during forward bias and suppressing leakage current during reverse bias, resulting in a significant improvement in power conversion efficiency (PCE).

During the negative half-cycle of V_X, the complementary node V_Y simultaneously rises to a positive voltage, applying a forward-enhancing gate bias to M_{N1}, which substantially reduces its conduction resistance. At the same time, M_{P2} turns on due to the negative voltage at V_X, creating a low-resistance path for current flow. Conversely, during the positive half-cycle of V_X, M_{N2} and M_{P1} conduct, forming a complementary conduction path. This symmetrical operation ensures balanced charge transfer in both half-cycles, maintaining continuous power delivery and leveraging the efficiency benefits of active V_{th} compensation. As a result, the rectifier achieves a reported PCE of 67.5% at 953 MHz with an input power of -12.5 dBm.

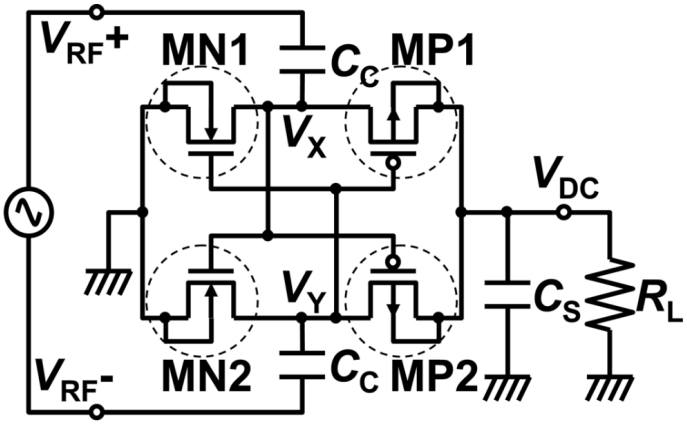


Figure 2.3: Schematic of cross-coupled rectifier [18]

When the TX and RX coils are far apart or weakly coupled as is often the case in implanted devices, voltage-mode (VM) receivers become inefficient because they fail to gather sufficient energy to complete each charging cycle. To address this issue, [19] proposed a current mode rectifier(CMR). This rectifier enhances energy efficiency by alternating between two distinct operating phases. In the build-up phase, the switch controlled by $\Phi_{build-up}$ is turned on, while the switch controlled by $\Phi_{charging}$ remains off, forming an LC tank circuit. During this phase, energy accumulates within the LC tank over several resonance cycles. Once sufficient energy is stored, the system transitions to the charging phase: $\Phi_{build-up}$ is opened and $\Phi_{charging}$ is closed, enabling the energy stored in the LC tank to be transferred efficiently to the battery. This architecture can not only perform rectification but also boost the voltage.

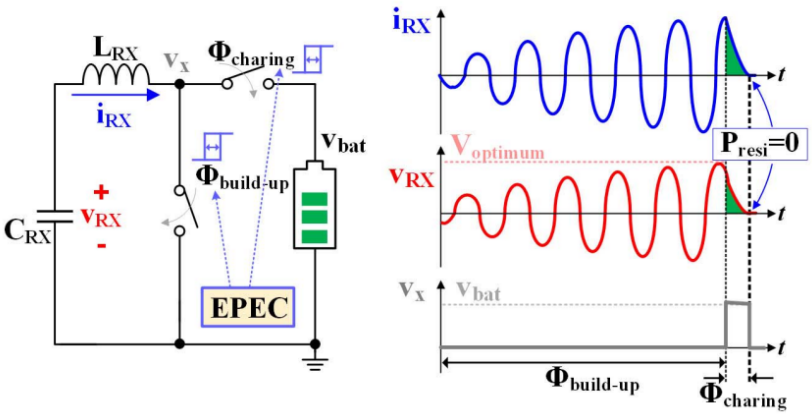


Figure 2.4: Working principle of current mode rectifier [19]

The intelligent mode-switching criteria are realized by the efficient power-extracting controller (EPEC). The working concept of EPEC is shown in Figure 2.5. By adaptively adjusting the build-up and charging durations based on the resonant voltage and current, EPEC ensures that both reach zero at switch-off, thereby achieving full energy transfer without residual loss.

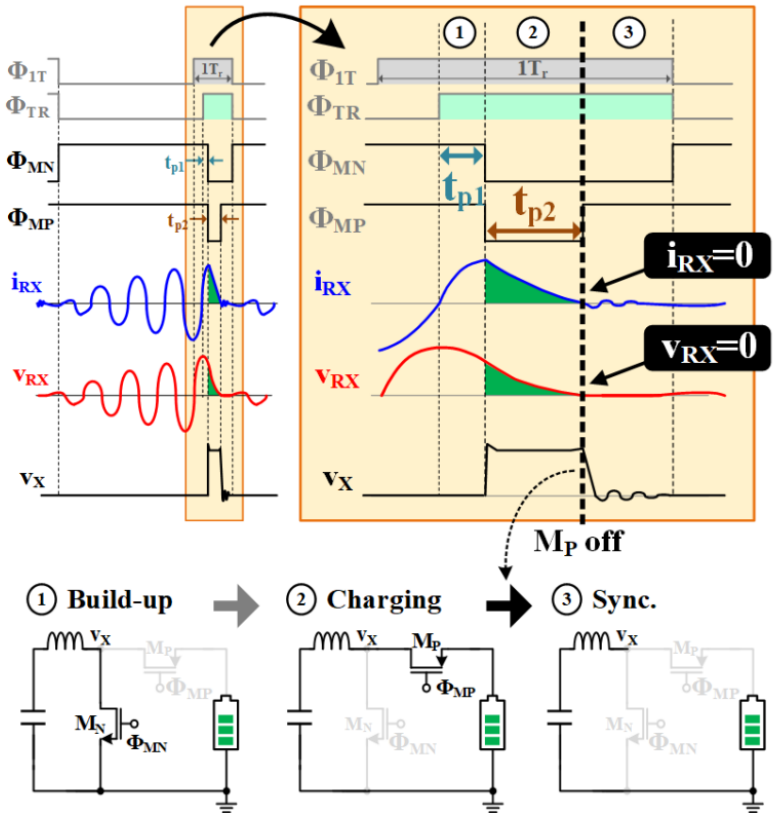


Figure 2.5: Concept of EPEC [19]

Similar to the CMR, a voltage doubler (VD) can simultaneously perform rectification and

voltage boosting. In [20], a highly efficient 13.56 MHz CMOS inductive-based WPT system specifically tailored for IMDs was proposed. The received alternating current (AC) signal is first rectified into a direct current (DC) signal via a VD, after which it undergoes further processing through low dropout regulators (LDOs) to minimize ripple. The schematic of the system is shown in Figure 2.6. The system is designed to deliver an output current of 20 mA for IMDs, employing a spiral-shaped inductive coil combined with a ferrite core to enhance efficiency and reduce spatial requirements. Experimental results demonstrate that the inductive coil achieves a transmission efficiency of 76.3% at the resonant frequency of 13.56 MHz.

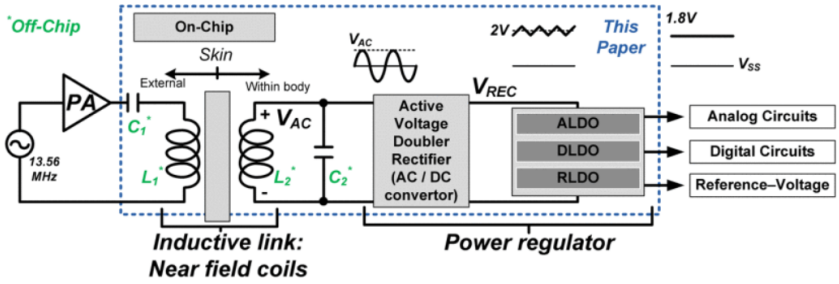


Figure 2.6: Inductive-based WPT with voltage doubler + LDO [20]

To further optimize power conversion efficiency (PCE), [20] designs a CMOS power regulator comprising an active VD and multiple LDOs. The schematic of VD is shown in Figure 2.7.

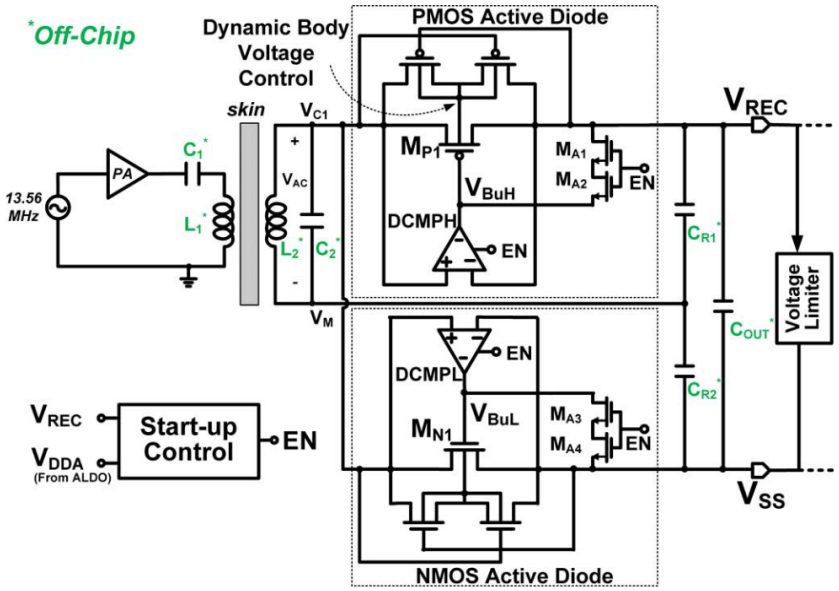


Figure 2.7: Schematic of VD [20]

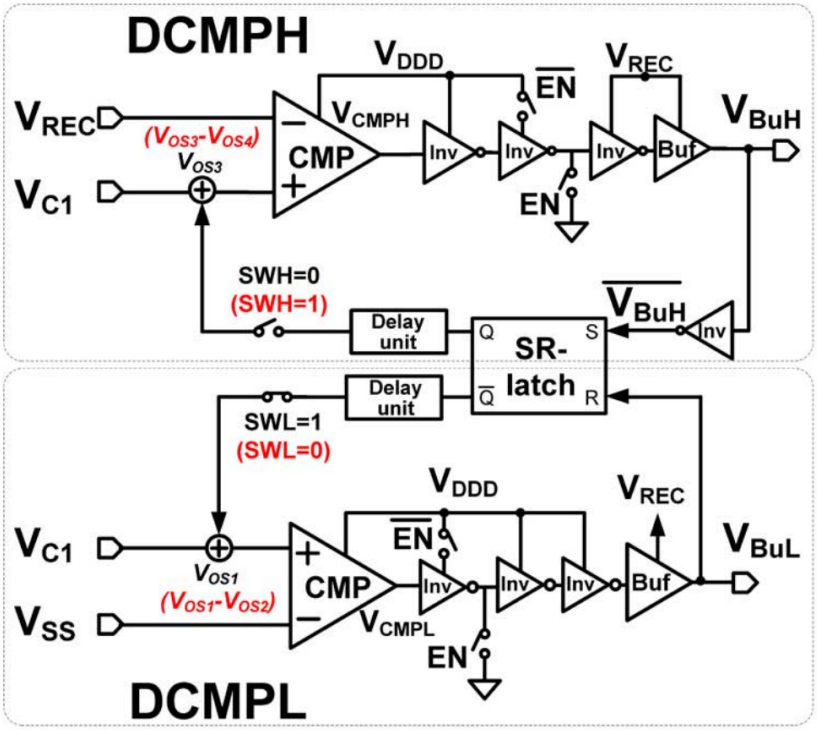


Figure 2.8: Schematic of delay compensation comparator [20]

Traditional diodes, due to their high forward voltage drop and reverse current, can significantly reduce system efficiency. To address this issue, the VD employs an active diode, which can significantly reduce the forward voltage drop. However, the operation of the active diode relies on comparator control. Due to the limited speed of the comparator, there may be cases where the diode fails to turn on or off in a timely manner during conduction or blocking, leading to reverse current or system instability. To handle this, the VD design utilizes a delay compensation comparator, which uses SR latches and delay units to compensate for the turn-on/turn-off delay of power MOSFETs. The detailed implementation of the delay compensation comparator is shown in Figure 2.8. Dynamic body voltage control can connect the body terminal of the power MOSFET to the appropriate potential automatically to eliminate body effects and substrate leakage. The voltage limiter can restrict the rectified voltage V_{REC} to 2.5 V in case the input voltage is too large. The system can achieve 85% peak PCE.

While the above studies contribute to the understanding of WPT RX architectures, they are generally not tailored for ultrasonic WPT. To address this, several RX designs dedicated to ultrasonic WPT have been proposed, as discussed in the following.

In [21], a millimeter-scale implantable medical device based on an ultrasound power supply and a hybrid bidirectional data link was developed, with the system architecture shown in Figure 2.9.

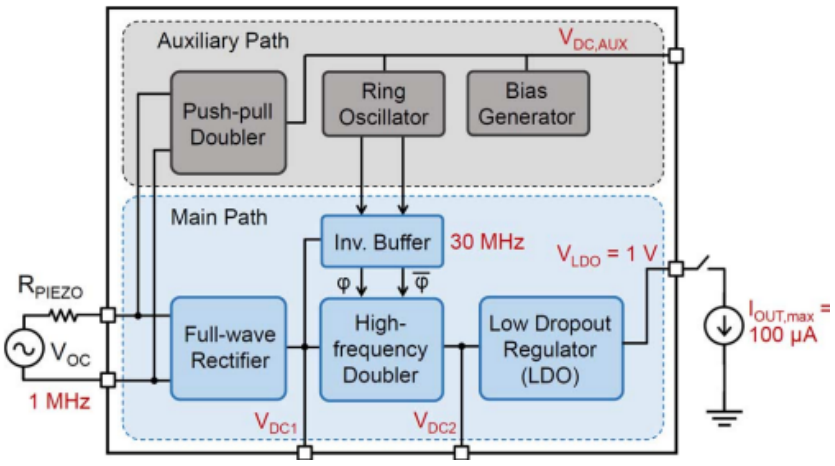


Figure 2.9: Two-path power recovery circuit[21]

Ultrasonic energy is converted into AC by a PZT piezoelectric receiver with dimensions of 1 mm $\times$ 1 mm $\times$ 1.4 mm. This AC is then rectified by an active full-wave rectifier to generate a DC voltage V_{DC1} with an input range of 0.6–1.2 V, achieving a measured voltage conversion efficiency of 97.5%. The schematic of the active rectifier is shown in Figure 2.10 (a). This voltage is subsequently boosted to V_{DC2} by a 30 MHz high-frequency voltage multiplier, as illustrated in Figure 2.10(b), with a simulated efficiency of 88%. Finally, an LDO regulator, as shown in Figure 2.10, outputs a 1.0 V DC rail, which can support a maximum load of 100 μW while maintaining a static current of 3.2 μA.

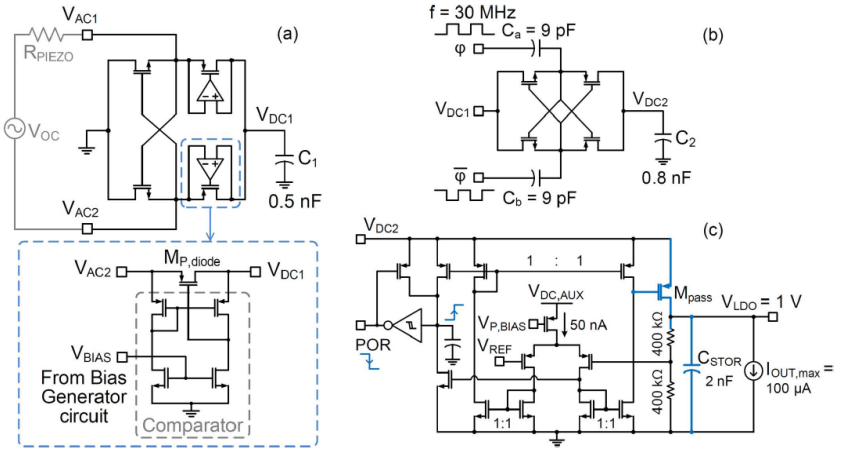


Figure 2.10: Power recovery circuit in main path (a) active rectifier; (b) voltage doubler; (c) LDO. [21]

To overcome the capacitor size limitations imposed by the low input frequency of 1 MHz, a dual-path hybrid architecture is employed: the main path architecture is specifically designed for a 100 μW load, integrating a rectifier, voltage doubler, and LDO; the auxiliary path generates a measured voltage of 0.69 V $V_{DC,AUX}$ via the push-pull voltage doubler, supplying power

to the bias circuit and 30 MHz ring oscillator to ensure low-power startup. The key innovation in the rectifier design lies in the reuse of PMOS diode comparators for ultrasonic envelope detection, generating precise 2 ns pulse width trigger signals to directly drive the uplink.

In [22], a millimeter-scale implantable neural stimulation device based on an ultrasound power supply and a hybrid data link was proposed, with the system architecture shown in Figure 2.11.

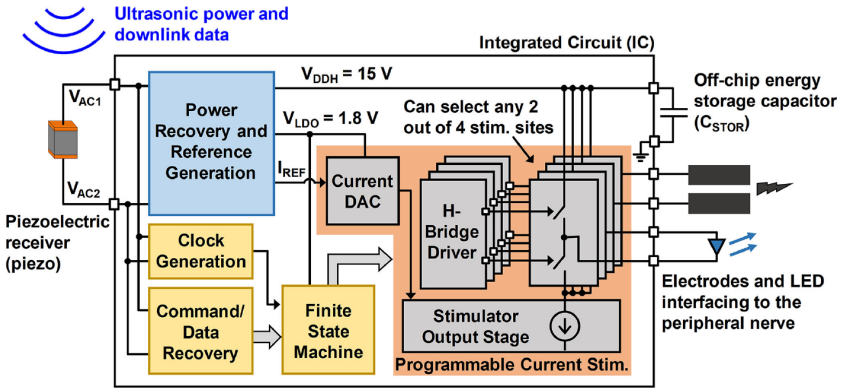


Figure 2.11: Ultrasonic receiver with power recovery and data link [22]

The piezoelectric receiver receives 1 MHz ultrasonic energy and downlink data signals through its dual-ended inputs V_{AC1} and V_{AC2}. The power recovery and reference voltage generation module converts the AC signal into a 15 V high voltage V_{DDH} to power the off-chip energy storage capacitor C_{STOR}, while generating a 1.8 V low voltage V_{LDO} to power the digital circuits and producing the reference current I_{REF}. The clock generation module extracts the clock signal from the ultrasonic carrier, instructing the data recovery module to parse the downlink commands. The finite state machine configures the parameters of the current digital-to-analog converter (DAC) based on the commands. The system supports selecting any two out of four stimulation sites for output, driving electrodes and LEDs via an H-bridge driver to interface with peripheral nerves, thereby achieving programmable current stimulation. The entire IC chip integrates ultrasonic power supply, data processing, and neural stimulation functions, utilizing a dual-power supply architecture with a 15 V high-voltage V_{DDH} and a 1.8 V V_{LDO}.

The detailed power recovery circuit is shown in Figure 2.12. The operating principle can be divided into three main stages: energy conversion, voltage boosting, and voltage regulating. In the energy conversion stage, the piezoelectric receiver first converts the AC signal from the V_{AC1} and V_{AC2} differential inputs into a DC voltage V_{RECT} via an active rectifier. This DC voltage then enters the voltage-boosting stage, where it is boosted through a three-stage charge pump. The switching operation of the charge pump is precisely controlled by the CLK clock signal, ultimately establishing a stable output V_{DDH} on the storage capacitor C_{STOR}. The clock generation section employs a current-limited ring oscillator structure, whose oscillation

frequency is precisely regulated by V_{REF} generated by the bandgap reference circuit. The resulting complementary clock signals CLK and $CLKB$ are shaped by inverters and buffers to provide high-quality clock drive for the system. In the voltage regulating stage, an LDO converts the high voltage into a stable low-voltage power supply to give supply to subsequent circuits.

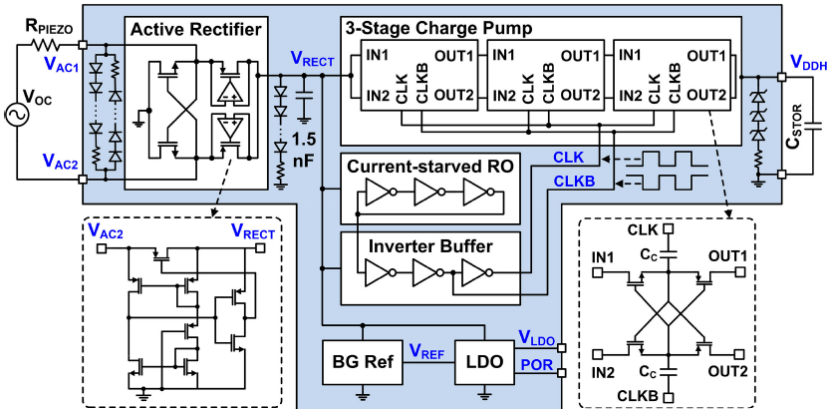


Figure 2.12: Schematic of power recovery circuit and reference generation [22]

In [23], an ultrasonic wireless power transfer system for deep tissue implants is proposed, featuring a single-chip integrated power extraction circuit with innovative designs in the voltage detectors and charge pump. The system employs a two-stage energy extraction architecture, as shown in Figure 2.13 (a). The first stage is a passive rectifier based on a two-stage Dickson charge pump, capable of autonomous startup from a 48 mV peak AC input, and optimized for charge transfer using low-threshold transistors. The second stage is an active two-stage charge pump.

Voltage detector VD1 continuously monitors the voltage across the output capacitor V_{CL} using a current comparator-based architecture. When V_{CL} exceeds 0.42 V, VD1 outputs a high signal to activate the charge pump; when V_{CL} falls below 0.38 V, it outputs a low signal to deactivate the pump. This enables precise control of pump operation with an ultra-low quiescent current of only 8.8 nA. Concurrently, voltage detector VD2 dynamically monitors the output capacitor voltage V_{CH} of the charge pump. When V_{CH} exceeds 1 V, switch SW1 is closed to deliver power to the load; when V_{CH} drops below 0.8 V, SW1 opens to halt power delivery and allow energy accumulation. The operation of this logic is shown in Figure 2.13 (b).

By employing dual-threshold hysteresis control (0.8 V–1 V), the system enables on-demand energy allocation. As a result, the total power consumption is maintained below 130 nW during a 7.9 μW short pulse output.

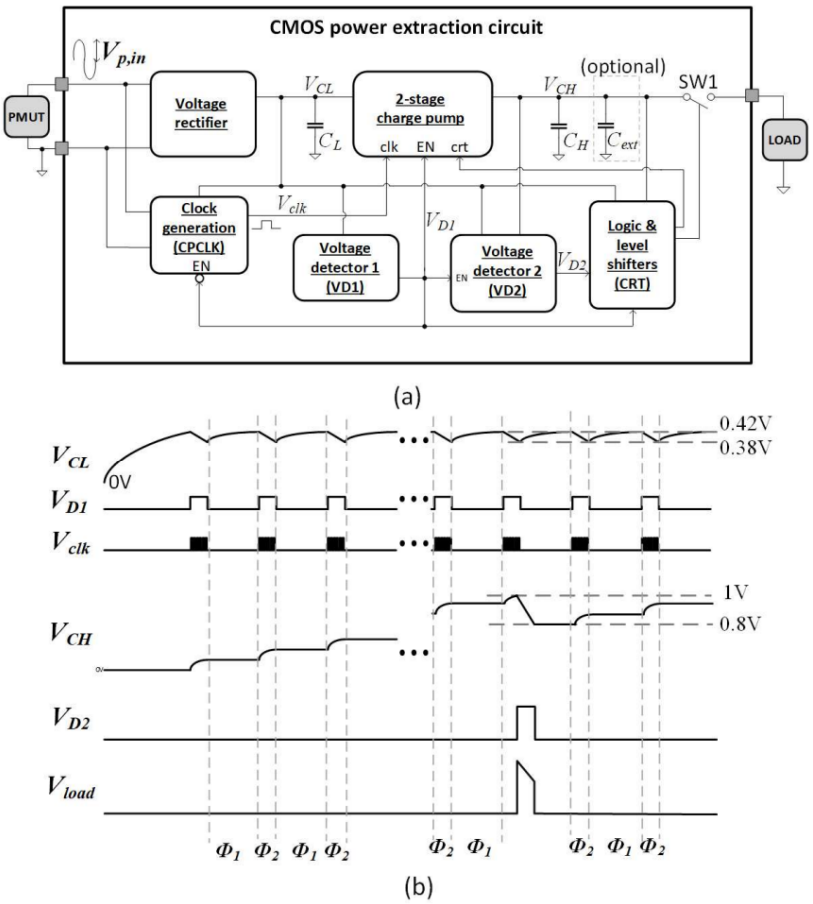


Figure 2.13: (a) Power extraction circuit with dickson charge pumps (b) its operation [23]

Based on the above literature review, commonly used rectifier structures include voltage doublers, active rectifiers, cross-coupled rectifiers, current-mode rectifiers, and Dickson charge pumps. For stabilizing the rectified DC voltage, the most common approach is to use an LDO; however, an LDO can only step the DC voltage down. Some studies employ Dickson charge pumps to boost the DC voltage, but their efficiency is generally low. Among them, the current-mode rectifier emerges as a promising candidate because it enables simultaneous rectification and voltage boosting. Therefore, the next chapter is devoted to a detailed discussion of current-mode rectifier design and its advantages.

Chapter 3

Current Mode Rectifier

CMRs have attracted increasing attention as an alternative to conventional voltage-mode rectifiers, since they can simultaneously perform rectification and voltage boosting without being constrained by threshold voltage limitations. These features make CMRs a promising candidate for efficient power transfer, particularly in applications such as ultrasonic WPT systems where both high efficiency and compact integration are critical. This chapter introduces the operating principle of the CMR, highlights its key advantages over traditional approaches, and presents a theoretical circuit analysis. Furthermore, simulations are conducted to evaluate the performance of the CMR and verify its suitability for ultrasonic systems.

3.1 Operation of Current Mode Rectifier

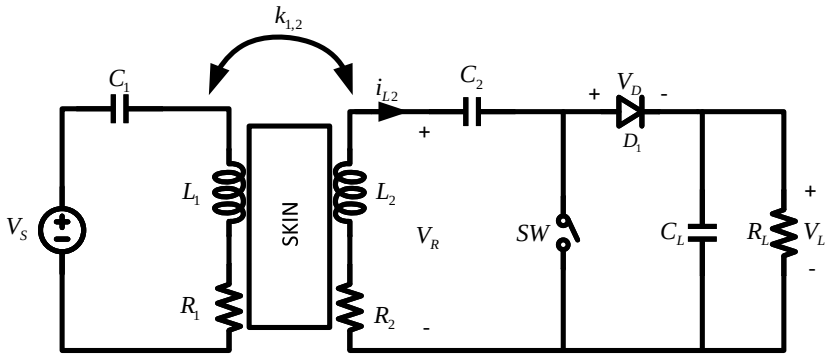


Figure 3.1: Schematic of current mode rectifier with inductive link

Figure 3.1 illustrates the schematic of a CMR with an inductive power link. On the receiver side, the circuit consists of an LC tank, a switch (SW), and a diode (D_1). The load voltage V_L

is developed across a load composed of a capacitor (C_L) and a resistor (R_L). V_R is the voltage across L_2 and R_2, V_D is the voltage on D_1, i_{L2} is the current in L_2.

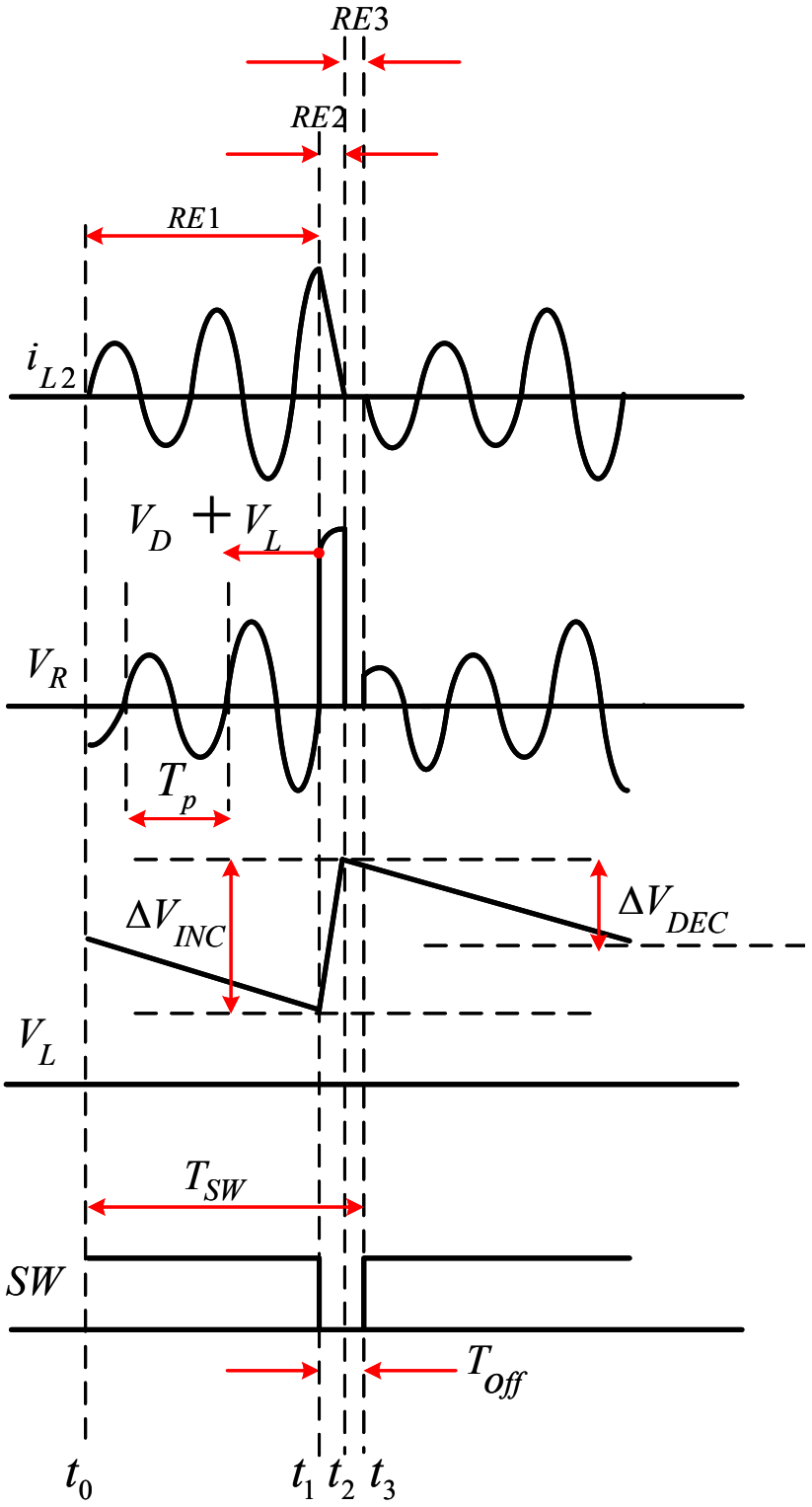


Figure 3.2: Key waveforms of current mode rectifier

The operation of the current-mode rectifier (CMR) can be divided into three distinct regions, as illustrated in Figure 3.2. During Region RE1 ($t_0 < t < t_1$), the switch (SW) remains closed over multiple power carrier cycles, allowing the high-Q LC tank circuit to accumulate energy from the inductive link. A critical transition occurs at t_1, when the inductor current i_{L2} reaches its optimal value, signaling the onset of Region RE2 ($t_1 < t < t_2$). At this precise moment—when the capacitor voltage V_{C2} crosses zero and all energy is stored in L_2, SW opens to deliver the stored energy to the load within a short duration. Region RE3 ($t_2 < t < t_3$) begins when i_{L2} decays to zero. During this period, SW remains open until t_3, resulting in a total switch-off time of $T_{\text{off}} = t_3 - t_1 = 0.25T_p$, where T_p is the power carrier period. The cycle recommences at t_3, when SW closes again to initiate a new energy transfer phase.

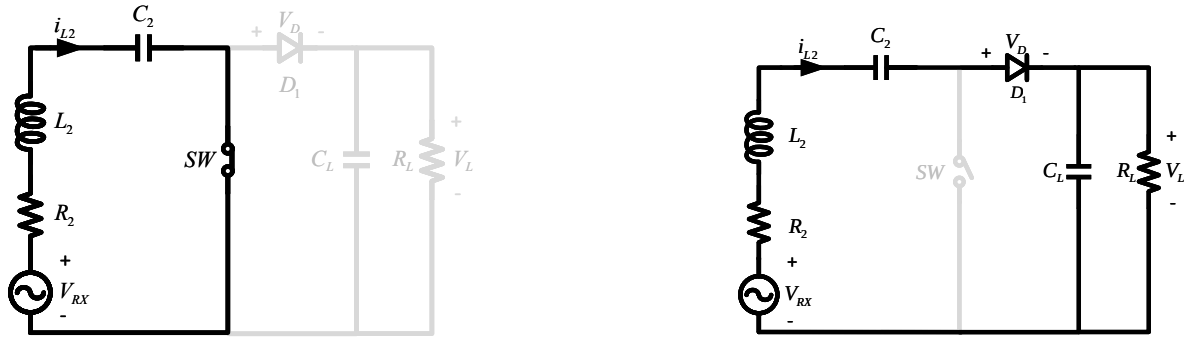
It is important to highlight the dynamic behavior of V_R. At time t_1, V_R is zero, and the only discharge path for L_2 is through diode D_1. However, V_R quickly rises to exceed $V_D + V_L$, where V_D is the voltage drop on D_1. This structure enables high voltage conversion efficiency, as the peak V_R does not need to surpass V_L and L_2 is working as a current source. The resonant behavior is primarily governed by region $RE1$, since regions $RE2$ and $RE3$ are of short duration—during which L_2 resonates in parallel with C_L and R_L, and C_L is much larger than C_2. As a result, their contribution to the overall quality factor Q is negligible.

The high sensitivity of CMRs enables the detection of ultra-low-power signals, rendering them particularly suitable for energy-constrained applications such as IMDs. Unlike conventional voltage-mode rectifiers, CMRs facilitate direct energy transfer, thereby avoiding the need for multi-stage conversion processes, minimizing energy loss, and improving overall power conversion efficiency. Furthermore, CMRs eliminate the requirement for complex compensation networks and additional voltage regulation circuitry, which contributes to reduced system complexity. Notably, their operation is not constrained by the threshold voltage, further enhancing their applicability[24]. These advantages collectively make CMRs a highly promising solution for IMD applications.

3.2 Theoretical Analysis

The two operating modes of the CMR receiver model are illustrated in Fig. 3.3. In the first mode, shown in Fig. 3.3a, the switch SW is closed, allowing energy to accumulate in the L_2C_2 tank. In the second mode, shown in Fig. 3.3b, the switch SW is open, and the stored energy is delivered to the load through diode D_1, which also serves to block reverse current.

Because the duration of $RE1$ is significantly longer than that of $RE2$ and $RE3$, the L_2C_2 tank in the CMR can be regarded as operating at resonance. Consequently, the steady-state values of i_{L2} can be determined using the $RE1$ circuit model shown in Figure 3.3a. According to



(a) CMR in $RE1$ with closed SW

(b) CMR in $RE2$ and $RE3$ with open SW

Figure 3.3: Two modes of CMR

Kirchhoff's voltage law, we could get the equation below.

$$\left(\frac{1}{j\omega_p C_2} + j\omega_p L_2 + R_2 + R_{sw}\right) i_{L2} - V_{RX} = 0 \tag{3.1}$$

Where R_{sw} is the resistance of SW when it is closed. $\omega_p = 2\pi/T_p = 2\pi f_p$. V_{RX} is the amplitude of the receiving voltage.

Maximizing V_{RX} while minimizing $R_2 + R_{SW}$ leads to a maximum i_{L2}, which in turn allows V_L to reach its highest possible value.

Since C_L is typically selected to be sufficiently large to minimize voltage ripple across R_L, the impedance of the load can be reasonably neglected.

The transient i_{L2} of Figure 3.3a can be found from the equation below.

$$V_{RX}(t) = L_2 \frac{di_{L2}(t)}{dt} + \frac{1}{C_2} \int i_{L2}(t)\, dt + (R_2 + R_{sw}) i_{L2}(t) \tag{3.2}$$

The solution of the equation above for $t_0 < t < t_1$ can be written as this:

$$i_{L2}(t) = e^{\alpha(t-t_0)} \left[A_1 \cos(\omega_d(t-t_0)) + A_2 \sin(\omega_d(t-t_0))\right] - A_3 \sin(\omega_p(t-t_0)) \tag{3.3}$$

Where $\alpha = -\frac{R_2+R_{sw}}{2L_2}$, $\omega_d = \sqrt{\frac{1}{L_2C_2} - \alpha^2}$. To get A_1 and A_2, we need initial conditions of i_{L2}. A_3 can be found from particular solution (3.1). So A_1, A_2 and A_3 can be expressed as

$$A_1 = i_{L2}\,(t_0) = 0 \tag{3.4}$$

$$A_2 = \frac{(-V_{C2}(t_0)/L_2 - \alpha A_1 + A_3\omega_p)}{\omega_d} \tag{3.5}$$

$$A_3 = \frac{V_{RX}}{R_2 + R_{sw}} \tag{3.6}$$

Where $V_{C2}(t_0)$ denotes the initial voltage on C_2 at the beginning of each cycle, implying that $V_{C2}(t_0) = V_{C2}(t_3)$. To maximize i_{L2}, it is necessary to maximize A_3. So we need larger V_{RX} and smaller $R_2 + R_{SW}$.

During the period $t_0 < t < t_1$, only C_L charges R_L, so V_L slowly decreases as shown in Figure3.2. The decreased amout ΔV_{DEC} can be expressed as:

$$\Delta V_{DEC} = V_L\left(t_0\right)\left(1 - e^{\frac{-T_{sw}+T_{off}}{R_L C_L}}\right) \tag{3.7}$$

where $T_{sw} = \frac{1}{f_{sw}}$ and $T_{off} = 0.25T_p$.

The transient i_{L2} of Figure 3.3b can be found from the equation below.

$$V_{RX}(t) - V_D = L_2\frac{di_{L2}(t)}{dt} + \frac{1}{C_2}\int i_{L2}(t)\,dt + \frac{1}{C_L}\int i_{L2}(t)\,dt + (R_2 + R_D)i_{L2}(t) \tag{3.8}$$

Where R_D is the resistance of diode D_1. The solution of (3.8) can be written as below:

$$i_{L2}(t) = Be^{\alpha(t-t_1)}\cos\left(\omega_d(t-t_1) - \theta\right) + A_3\cos\left(\omega_p(t-t_1)\right) \tag{3.9}$$

where

$$\begin{aligned}
A_3 &\approx \frac{V_{RX}}{R_2 + R_D}, \\
B &= \sqrt{\left(\frac{\frac{di_{L2}(t_1)}{dt} - \alpha\left(i_{L2}(t_1) - A_3\right)}{\omega_d}\right)^2 + \left(i_{L2}(t_1) - A_3\right)^2}, \\
\theta &= \tan^{-1}\left(\frac{\frac{di_{L2}(t_1)}{dt} - \alpha\left(i_{L2}(t_1) - A_3\right)}{\omega_d\left(i_{L2}(t_1) - A_3\right)}\right).
\end{aligned}$$

If using i_{L2} in equation (3.3), the time t_2 at which i_{L2} in (3.9) reaches zero can be approximated by the following expression:

$$t_2 - t_1 = \frac{\pi/2 - \theta}{\omega_d} \tag{3.10}$$

During $RE2$, when i_{L2} is nonzero and the L_2C_2 resonant tank is connected to the load, the inductor L_2 transfers energy to the parallel combination of C_L and R_L. As a result, the voltage V_L increases due to the energy released from L_2 into C_L. The voltage increment ΔV_{INC},

illustrated in Figure 3.2, can be calculated using the following integral expression:

$$\Delta V_{INC} = \int_{t_1}^{t_2} \frac{i_{L2}(t)}{C_L} dt \tag{3.11}$$

$RE3$ is deliberately introduced with a duration of $t_3 - t_1 = T_{off} = 0.25T_p$ to guarantee that the inductor L_2 fully discharges its energy into the capacitor C_L. This approach eliminates the need to detect the zero-crossing point of i_{L2}, thereby reducing sensing complexity.

Based on (3.7) and (3.11), V_L decreases during $RE1$ and increases during $RE2$ in each switching cycle, as illustrated in Figure 3.2. Therefore, the final value of V_L can be obtained from:

$$V_L(t = nT_{sw}) = \sum_{i=1}^{n} [\Delta V_{INC}(i) - \Delta V_{DEC}(i)] \tag{3.12}$$

At resonance, L_2 resonates with C_2 and is effectively canceled out. Therefore, the power transfer efficiency (PTE) of the CMR can be calculated as

$$PTE = \frac{P_{\text{load}}}{P_{\text{received}}} = \frac{V_L^2/R_L}{\left(V_{RX}/\sqrt{2}\right)^2/R_2} \tag{3.13}$$

3.3 Difference Between Ultrasonic Receiver and Inductive Receiver

For inductive receivers employing a CMR, the receiver inductor typically has an inductance in the range of several microhenries, and the quality factor Q is often greater than 30 [25, 26, 27]. A large inductance enables the LC tank to store more magnetic energy during each switching cycle, which can be subsequently transferred to the load. Meanwhile, a high quality factor Q indicates lower resistive losses, meaning that a smaller proportion of the stored energy is dissipated as heat in the coil resistance and associated parasitics. These characteristics—high inductance and high Q—are desirable in wireless power transfer systems because they enhance the system's energy efficiency and voltage gain. Specifically, a higher Q results in a sharper resonance peak, which improves power transfer capability and selectivity, while the increased energy storage of the inductor supports stronger coupling and more stable operation under load variations.

For ultrasonic receivers, operating within the IB is advantageous, as the transducer can effectively behave like an inductor in inductive power transfer systems. This enables the integration of an external capacitor to form a resonant tank circuit, thereby enhancing energy transfer ef-

ficiency.

Although the impedance appears inductive within this band, the equivalent inductance is typically quite small—on the order of several hundred nanohenries. Unlike inductive coils used in conventional wireless power transfer systems, ultrasonic transducers do not store energy magnetically. Instead, their impedance characteristics are predominantly determined by their mechanical structure and piezoelectric material properties.

Figure 3.4 shows the measured impedance of a specific PZT ultrasonic receiver. At an operating frequency of 4.6 MHz, the input impedance is approximately $50 + j22.5\ \Omega$, indicating a predominantly resistive characteristic with a relatively small inductive component. To achieve resonance, a compensation capacitor is required to form an LC tank with the equivalent inductance L_{eq}, which can be calculated as

$$L_{\text{eq}} = \frac{X_L}{2\pi f} = \frac{22.5}{2\pi \times 4.6 \times 10^6} \approx 779\text{nH} \tag{3.14}$$

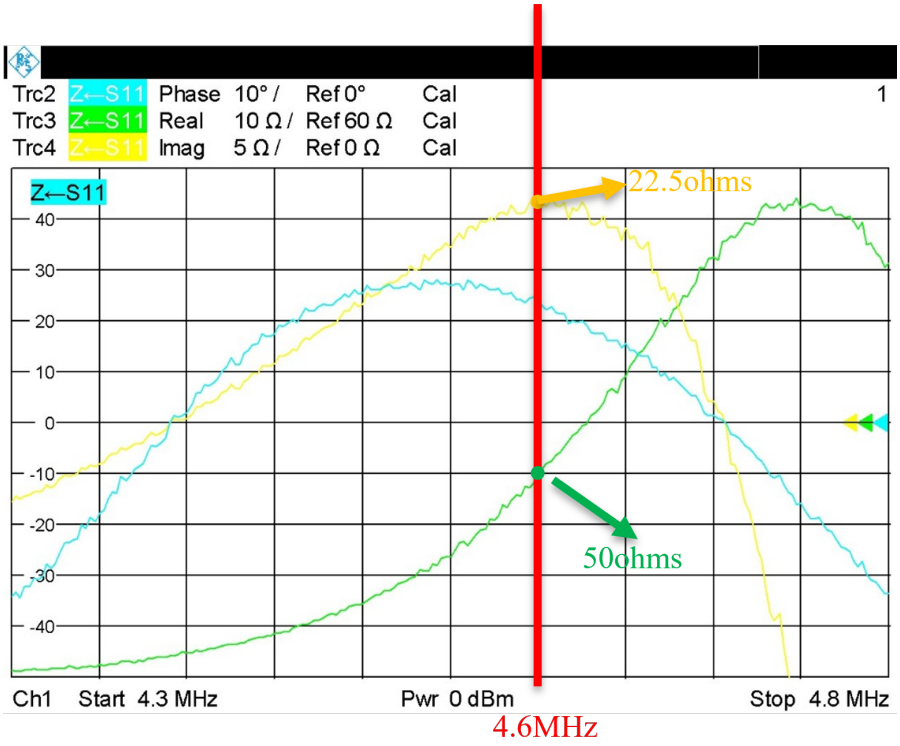


Figure 3.4: Impedance measurement result of ultrasonic receiver at 4.6 MHz

The required series capacitor for resonance at this frequency is:

$$X_C = X_L \Rightarrow C = \frac{1}{2\pi f X_C} = \frac{1}{2\pi \times 4.6 \times 10^6 \times 22.5} \approx 1.54\text{nF} \tag{3.15}$$

The quality factor Q of the resulting resonant circuit is given by:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{50}\sqrt{\frac{779 \times 10^{-6}}{1.54 \times 10^{-9}}} \approx 0.45 \tag{3.16}$$

The combination of small inductance and relatively high input resistance results in a low quality factor for ultrasonic receivers—significantly lower than that of conventional inductive coils. This inherently weak resonance poses challenges for achieving high power transfer efficiency using CMR technique.

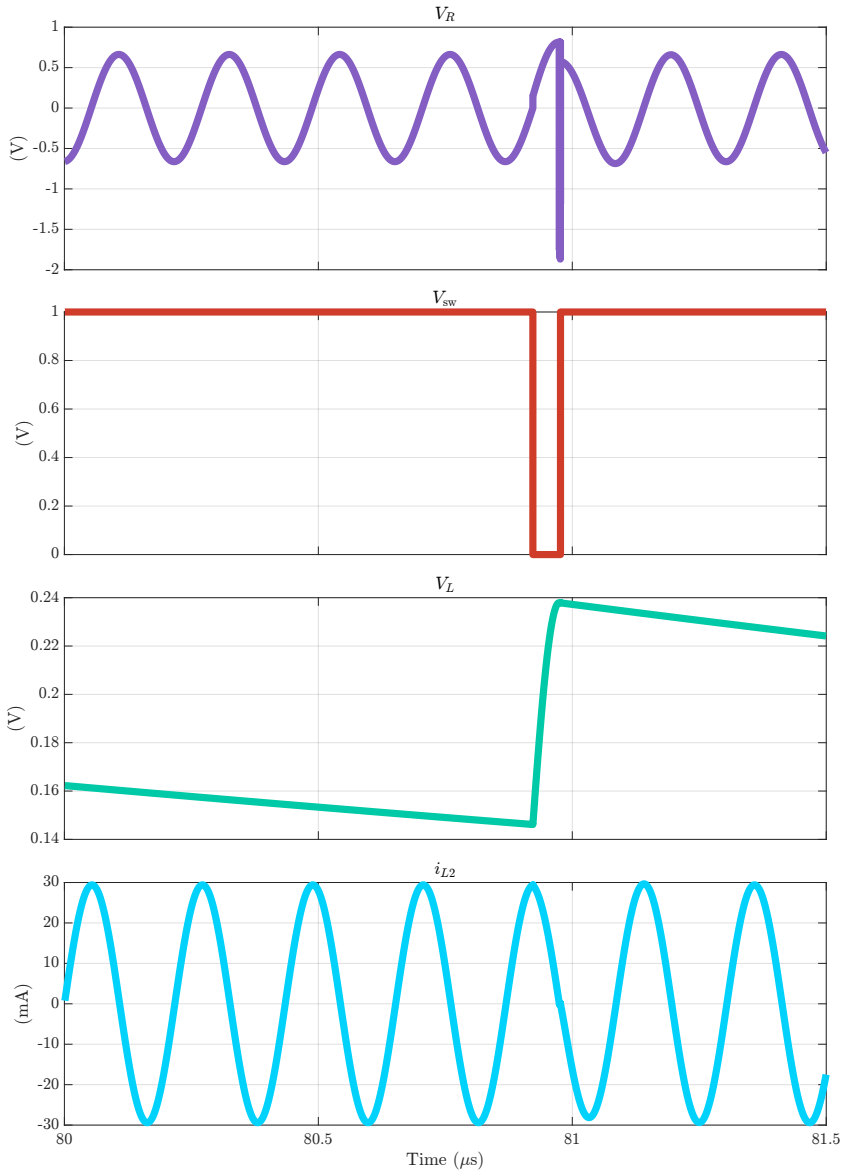


Figure 3.5: Simulation result of CMR using a PZT transducer

Based on the above calculations, a CMR circuit was implemented and tested through simulation. The number of accumulating cycles is set as 20. The simulation results are presented in

Figure 3.5. It can be observed that the inductor current i_{L2} remains nearly constant and does not increase as expected with the CMR configuration. This behavior is primarily attributed to the small inductance, which limits the amount of energy that can be stored in the LC tank, and the relatively large resistance, which leads to significant energy dissipation during each cycle.

One common approach to improving the quality factor Q is to increase the value of the inductor. Theoretically, a higher inductance allows for greater energy storage, leading to a higher Q. However, since the impedance characteristics are intrinsic to the transducer, altering the inductance effectively requires modifying the transducer itself. To emulate the behavior of a different transducer with higher inductance and same resistance, a extra inductor was connected to the transducer.

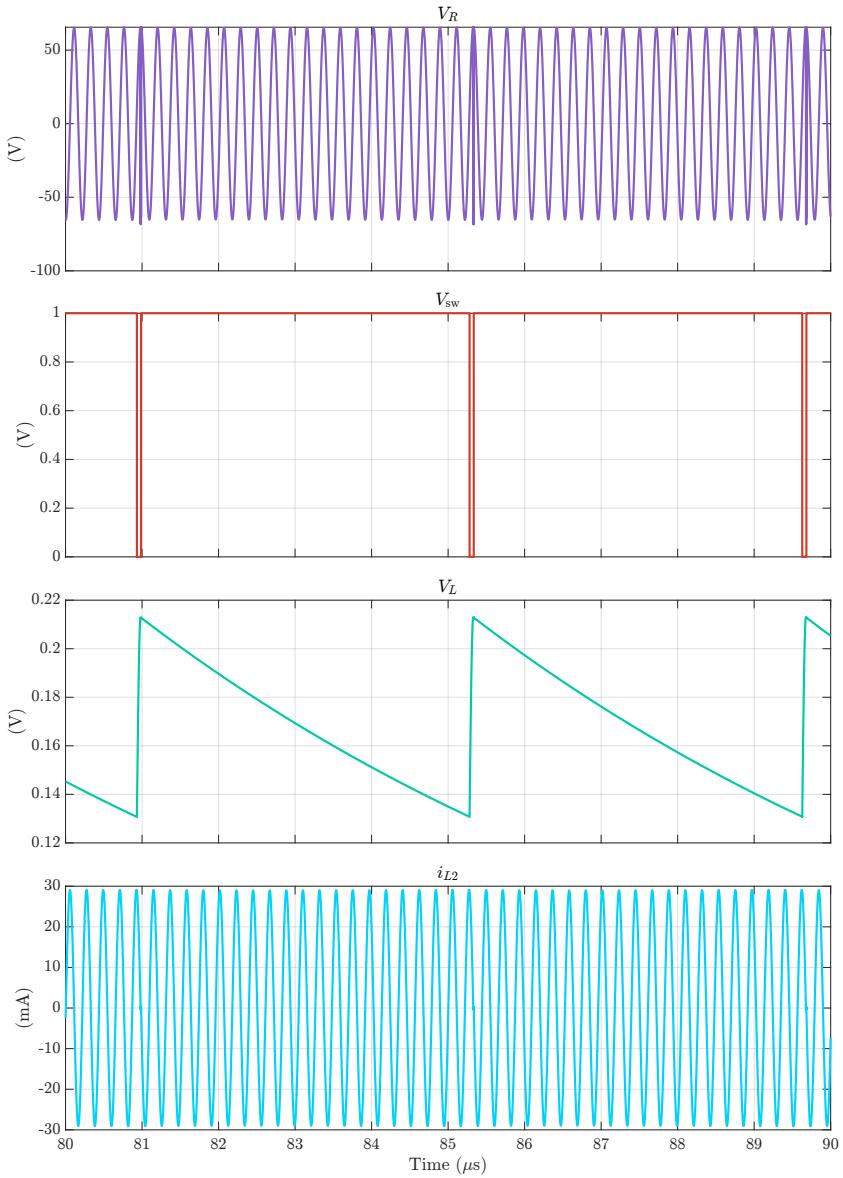


Figure 3.6: Simulation result of CMR with 100x inductance

The simulation result for a case where the inductance is increased by a factor of 100 is shown in Figure 3.6. Through (3.16), we can know now the Q is around 45, so this LC tank can restore much energy. However from simulation result, the output voltage doesn't get boosted as expected.

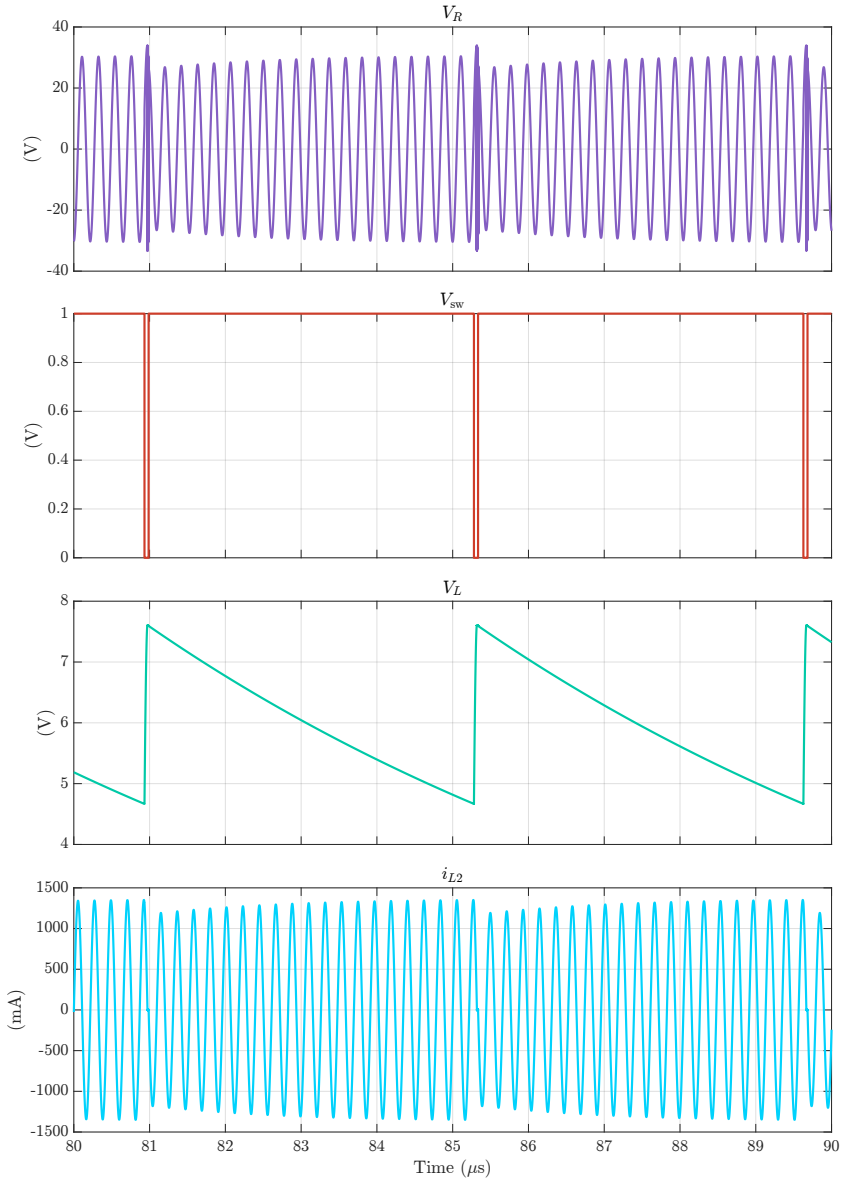


Figure 3.7: Simulation result of CMR with 0.1Ω resistor

Another approach to improving power transfer efficiency is to reduce the resistance of the ultrasonic receiver, thereby increasing the maximum inductor current. However, since resistance is an intrinsic property of the receiver, it cannot be easily modified in practice. A simulation was performed in which the receiver resistance was set to 0.1 Ω instead of its actual value of 50 Ω. The result, shown in Figure 3.7, illustrates the impact of reduced resistance on circuit performance. It should be noted, however, that the theoretical available power, given by

$P_{av} = {V_{ac}}^2/8R$ (where V_{ac} is the amplitude of the AC input and R is the source resistance), also increases as the source resistance decreases. Therefore, with the same input amplitude, a lower source resistance leads to a larger available power, making the higher voltage observed at the load reasonable.

Due to the large source resistance and small inductance of the PZT ultrasonic transducer, its quality factor at the resonant frequency of 4.6 MHz is extremely low, i.e., below unity. This indicates that the accumulated power is smaller than the power loss, rendering CMR unsuitable for direct application in PZT ultrasonic transducers. Although increasing the inductance could theoretically improve the quality factor at the same resonant frequency, this approach fails to provide the expected performance. Similarly, reducing the resistance may offer a theoretical benefit, but the intrinsic resistance of the transducer cannot be practically modified. Therefore, alternative solutions such as voltage-mode rectifiers and DC–DC converters are explored in the following section.

Chapter 4

System Design

Figure 4.1 illustrates the block diagram of the ultrasonic receiver system. Based on the impedance characteristics shown in Figure 3.4 and the advantages of operating the transducer in the IB region, the receiver is modeled as an AC voltage source in series with a resistor and an inductor. The system consists of two main power conversion stages. First, the received AC voltage is rectified by an AC/DC converter to produce a DC voltage. This DC voltage is then processed by a DC/DC converter, which makes it to the desired output level. Finally, an output capacitor C_L ensures voltage stability.

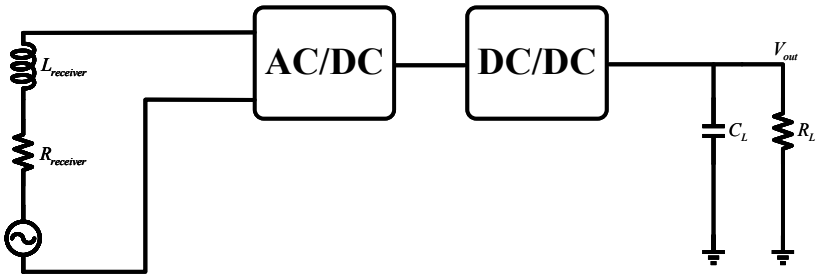


Figure 4.1: Blocks of ultrasonic RX working in IB

4.1 Rectifier

Rectifiers are essential for ensuring reliable and efficient operation of various on-chip analog and digital components, especially in energy-constrained environments.

4.1.1 Half Wave Rectifier

The half-wave rectifier is one of the most fundamental configurations employed in AC to DC power conversion. It operates by permitting current to flow through the load during only one

half-cycle of the input alternating voltage, effectively blocking the other half. This unidirectional conduction is achieved using a single diode.

In the standard configuration, one terminal of the AC voltage source is grounded, and the other terminal is connected in series with the anode of a diode. During the positive half-cycle of the AC input—when the instantaneous potential of the non-grounded terminal (V_{IN1}) exceeds that of the grounded terminal (V_{IN2})—the diode becomes forward-biased once V_{IN1}) surpasses the output DC voltage (V_{OUT}). Under this condition, the diode conducts, and current is delivered to the load, resulting in a pulsating DC voltage at the output.

Conversely, during the negative half-cycle—when $V_{IN1} < V_{IN2}$—the diode is reverse-biased, and no current flows through the load. Thus, the rectifier delivers energy to the load only during alternate half-cycles of the AC waveform.

However, the topology inherently exhibits poor power conversion efficiency and pronounced output voltage ripple, owing to its utilization of only a single half cycle of the AC input.

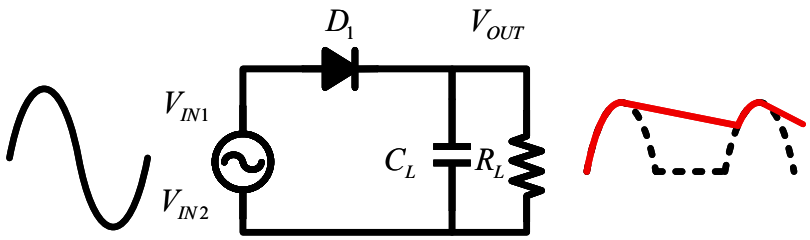


Figure 4.2: Schematic of half wave rectifier

4.1.2 Full Wave Rectifier

To overcome the limitations of the half-wave rectifier, the full-wave rectifier was introduced. This fundamental topology converts an AC input into a DC output by utilizing both the positive and negative half-cycles of the AC waveform, thereby achieving higher power-conversion efficiency and significantly reduced output-voltage ripple.

Full Bridge Rectifier

A full bridge rectifier is a commonly used full wave rectifier. As shown in Figure 4.3, the full-bridge rectifier consists of four diodes, a load capacitor, and a load resistor. It can convert a AC voltage to a DC voltage. The capacitor serves to minimize the ripple in the output voltage, thereby improving voltage stability. Nevertheless, the significant forward voltage drop across the diodes leads to reduced conversion efficiency. In addition, the presence of a threshold voltage prevents the rectifier from functioning properly under low input voltage conditions.

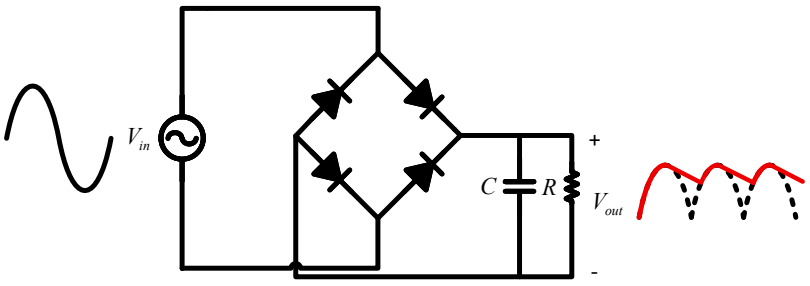


Figure 4.3: Schematic of full bridge rectifier

A full-wave rectifier can supply current to the load during both the positive and negative halves of the AC voltage cycle, whereas a half-wave rectifier only conducts during one half-cycle. Therefore, under the same load conditions, the charging time interval of a full-wave rectifier is only half that of a half-wave rectifier. Under the same load current and output capacitor conditions, the output voltage ripple amplitude of a half-wave rectifier is approximately twice that of a full-wave rectifier. This is because the charging frequency of a half-wave rectifier is lower, resulting in a greater drop in capacitor voltage. Additionally, the peak pulse current flowing through the diode in a half-wave rectifier is approximately twice that of a full-wave rectifier. Higher peak currents not only increase the electrical stress on the components but also lead to greater conduction losses.

Active rectifier

To minimize voltage drop, an active diode configuration can be utilized. This circuit typically consists of a comparator and a MOSFET, where the comparator continuously monitors the drain and source terminals of the MOSFET and accordingly controls its conduction state, thereby achieving a low forward voltage drop. The active rectifier builds upon the concept of active diodes and comprises a pair of cross-coupled PMOS transistors, along with two NMOS transistors that are driven by comparators. The schematic diagram of the active rectifier is presented in Figure 4.4.

The operating principle of an active full-wave rectifier can be interpreted as follows. Consider an AC cycle in which the voltage input V_{AC1} is decreasing while V_{AC2} is increasing. When the condition $V_{AC2} - V_{AC1} > |V_{THP}|$ is satisfied, where V_{THP} denotes the threshold voltage of PMOS transistors M_{P1} and M_{P2}, transistor M_{P1} is activated, thereby pulling V_{AC2} to the DC output level:$V_{AC2} = V_{DC}$. As V_{AC1} continues to drop below the ground potential (0 V), the comparator CMP1 detects this transition and switches on NMOS transistor M_{N1}, allowing the AC source to supply current I_{AC1} that charges the output node V_{DC}. This process persists until V_{AC1} reaches its minimum and begins to increase again. Once $V_{AC1} > 0$,the comparator

CMP1 turns off M_{N1}, thereby completing one half-cycle of the full-wave rectification process.

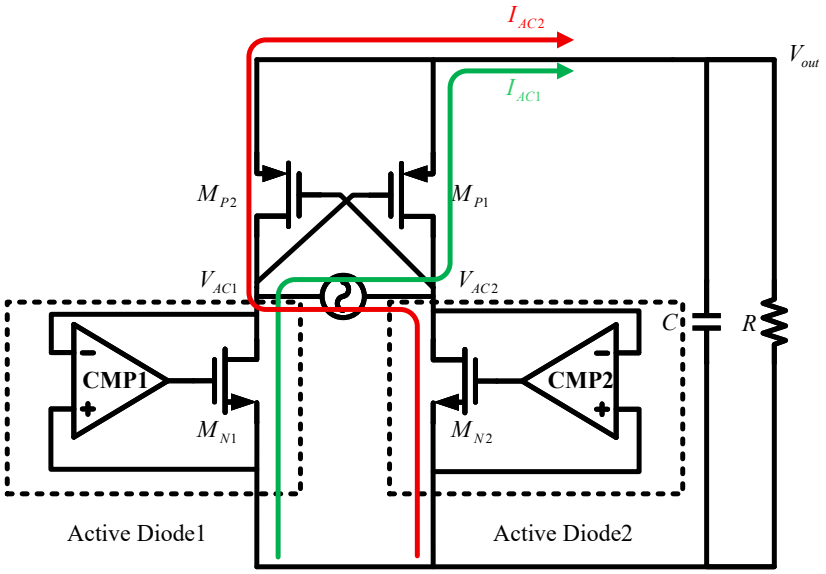


Figure 4.4: Schematic of active rectifier

During the subsequent half-cycle of the AC input, the complementary half of the rectifier circuit operates in an similar manner. By substituting the conventional four-diode full-wave rectifier with a set of active power transistors, the voltage conversion ratio can be significantly improved, particularly under low input amplitude conditions.

Nevertheless, when the circuit operates at high frequencies, performance degradation may occur due to the inherent propagation delay of the comparator and gate driver stages. As revealed in the simulated waveforms of I_{AC1}, reverse current is observed if the power transistors are not promptly turned off when V_{AC1} or V_{AC2} rises above ground. This delay-induced conduction leads to efficiency losses, increased power dissipation, and potential reliability issues, thereby underscoring the need for high-speed control circuitry in high-frequency rectification systems.

To mitigate the adverse effects of propagation delay, delay compensation techniques can be introduced to minimize the duration of unwanted conduction. However, the effectiveness of such compensation strategies is highly sensitive to the layout. Parasitic capacitances, interconnect mismatches, and signal routing irregularities introduced at the layout level can distort the timing characteristics, potentially offsetting or degrading the accuracy of delay compensation.

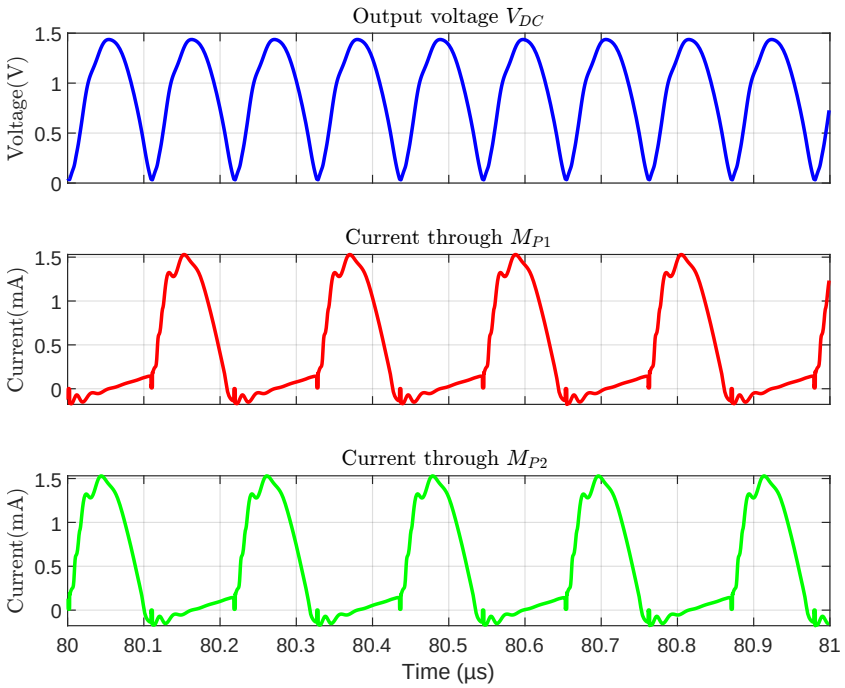


Figure 4.5: Simulation results of active rectifier

To evaluate the performance of the active rectifier, simulations were carried out using a source impedance identical to that shown in Figure 3.4, i.e., $50 + j22.5\ \Omega$. The circuit was implemented in TSMC 65-nm CMOS technology, with both the NMOS and PMOS transistors sized equivalently at $4.8\,\text{mm}/0.26\,\mu\text{m}$. The input signal was a sinusoidal waveform with an amplitude of $1.5\,\text{V}$. The load only has a capacitor of 10 nF. The simulation results of the active rectifier are shown in Figure 4.5. In this simulation, an ideal comparator is used to generate the switching signals. Although a small amount of reverse current is still observed, its magnitude remains negligible, indicating effective rectification performance.

Cross-coupled Rectifier

Another type of rectifier is the cross-coupled rectifier [28], whose schematic is shown in Figure 4.6. This configuration consists of a pair of cross-coupled NMOS transistors and a pair of cross-coupled PMOS transistors. Its operation can be described as follows: when the differential input satisfies $V_{IN+} > V_{IN-} + V_{th}$, the NMOS transistor M_{N2} and the PMOS transistor M_{P1} are turned on, establishing a current path from V_{IN+} through M_{P1} to charge the output capacitor C_L, and then returning to V_{IN-} via M_{N2}. In this manner, the high-frequency AC signal is effectively rectified into a DC output voltage V_{DC}. Simultaneously, M_{N1} and M_{P2} remain off due to insufficient gate-to-source voltage.

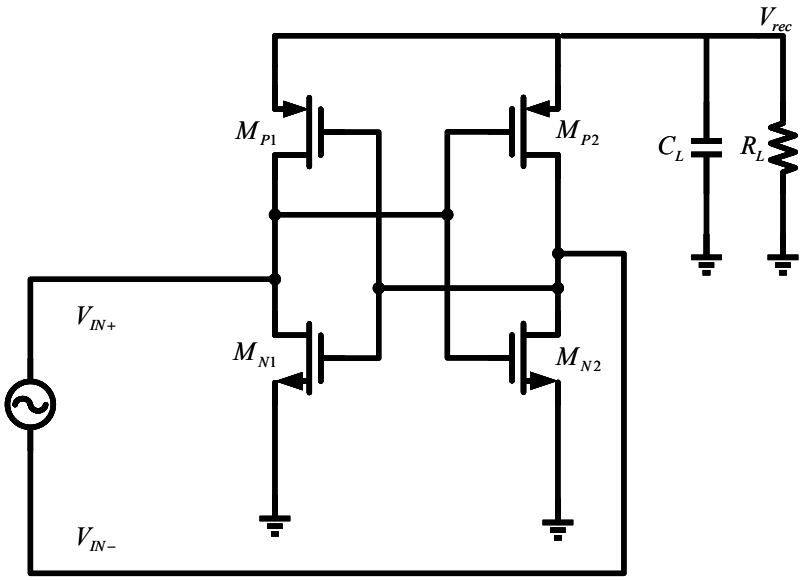


Figure 4.6: Schematic of cross-coupled rectifier

When the input polarity reverses, i.e., $V_{IN-} > V_{IN+} + V_{th}$, the conduction roles are inverted: M_{N1} and M_{P2} turn on, allowing current to flow from V_{IN-} through M_{P2} to the output, and then return to V_{IN+} through M_{N1}. By alternating conduction in this way, the cross-coupled topology enables efficient, passive synchronous rectification.

An additional advantage of this topology is its inherent active threshold voltage cancellation scheme: thanks to the cross-coupled differential configuration, the effective threshold voltage V_{th} of the transistors can be dynamically minimized during forward conduction, thereby reducing the turn-on resistance, while it can be increased during reverse bias, suppressing reverse leakage. This mechanism enhances both power conversion efficiency and minimum input voltage that can be rectified [29].

However, similar to other rectifier circuits that use diode-connected MOS transistors, the cross-coupled rectifier suffers from poor startup performance when the amplitude of the input signal is lower than the threshold voltage of the MOS transistors. This limitation arises because the static bias voltage required for MOS conduction in the cross-coupled configuration is internally generated during rectifier operation, which prevents the circuit from initiating conduction under low input amplitudes [18].

To further evaluate rectifier performance, simulations were conducted for the cross-coupled rectifier using the same operating conditions and parameters as those applied in the active rectifier case. As shown in the simulation results, the reverse current behavior of the cross-coupled rectifier closely resembles that of the active rectifier.

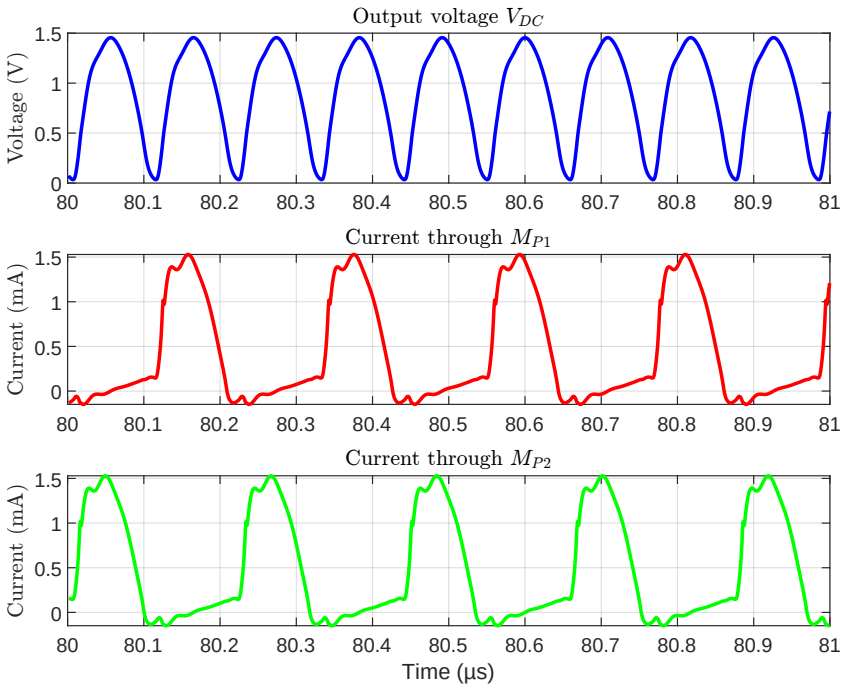


Figure 4.7: Simulation results of cross-coupled rectifier

However, it should be emphasized that the active rectifier simulations employed an ideal comparator, which does not account for the non-idealities typically present in practical implementations. As a result, the actual reverse current in a real-world active rectifier is expected to be larger than that observed in the simulation.

Taking into account both the comparable performance and the simpler control requirements, the cross-coupled rectifier is selected as the preferred solution for this design.

Voltage Doubler

In addition to the rectifier topologies discussed above, another circuit capable of simultaneously achieving rectification and voltage boosting is the voltage doubler. Voltage doublers are typically categorized into two types: half-wave and full-wave configurations. Among them, the full-wave voltage doubler is more widely adopted in practical applications due to its ability to deliver a more stable output voltage with reduced ripple. Consequently, the following discussion will focus exclusively on the full-wave voltage doubler.

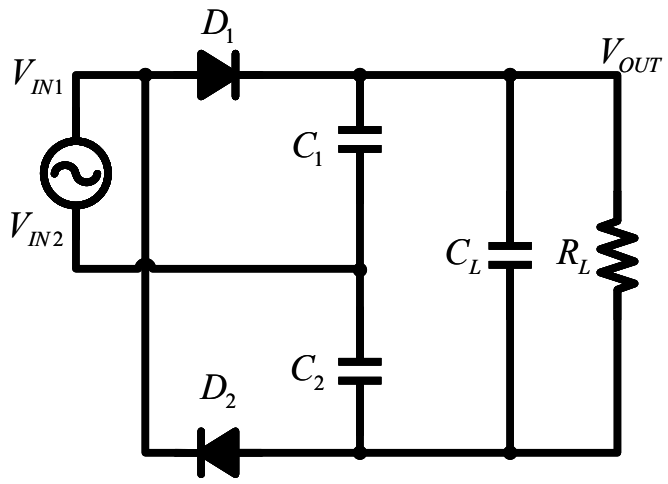


Figure 4.8: Schematic of full wave voltage doubler

The full wave voltage doubler represents a symmetrical configuration that can be regarded as the combination of two half-wave rectifier stages. By adding an additional diode and capacitor to the output of a standard half-wave rectifier, the output voltage can be effectively increased.

During the positive half-cycle of the input sinusoidal voltage($V_{IN1} > V_{IN2}$), capacitor C_1 charges through diode D_1. Conversely, during the negative half-cycle($V_{IN1} < V_{IN2}$), capacitor C_2 charges through diode D_2. Because the two capacitors are connected in series at the output, their voltages add together, producing an output voltage that theoretically reaches approximately $2V_{\text{IN}}$.

The voltage doubler circuit offers several advantages, including a simple topology, a VCR of two, and the ability to simultaneously perform rectification and voltage boosting. However, it provides only a fixed output voltage. Moreover, achieving high efficiency typically requires the use of active diodes. While active diodes can improve performance, they also introduce additional problems, as discussed in detail in the section *Active Rectifier*.

4.2 DC-DC Converter

In this project, the desired output voltage is higher than the input voltage, necessitating voltage boosting. Among various DC-DC converter topologies, the boost converter was selected to fulfill this requirement.

One of the key reasons for not using a switched-capacitor DC-DC converter lies in its fundamental limitation: the voltage conversion ratio is discrete and fixed, typically determined by the network topology [30]. In contrast, inductor-based converters—such as the boost converter—

enable continuous adjustment of the voltage conversion ratio through tuning the duty cycle, making them significantly more suitable for applications requiring fine-grained control.

In this design, the DC-DC converter not only serves to boost voltage but more critically, acts as an impedance matching element. Achieving precise impedance transformation requires the ability to continuously adjust the converter's VCR. This continuous tunability is inherently supported by inductor-based converters, but not by switched-capacitor types.

In a conventional boost converter topology, a single switch and a diode are employed to alternate the conduction paths. However, the diode introduces a relatively high forward voltage drop, leading to considerable conduction losses and reduced overall efficiency [31]. To address this issue, the diode can be replaced with an active diode, which reduces the voltage drop and improves conduction efficiency. Nonetheless, this modification introduces the risk of simultaneous conduction between the MOSFET and the active diode. As discussed in Section *Active Rectifier*, due to the comparator delay inherent in the active diode circuit, conduction may begin earlier than intended. This timing mismatch can lead to shoot-through currents, ultimately degrading the overall efficiency.

An alternative and more efficient approach involves replacing the active diode with a dedicated MOSFET switch and driving both the high-side and low-side switches using a non-overlapping signal generator. This circuit produces two complementary gate signals that are inherently separated by a dead-time interval. As a result, it prevents shoot-through without the need for comparators or complex timing logic, simplifying the control structure and reducing on-chip circuit complexity while still achieving high efficiency. This dual-switch boost converter configuration is also commonly referred to as a synchronous boost converter [32].

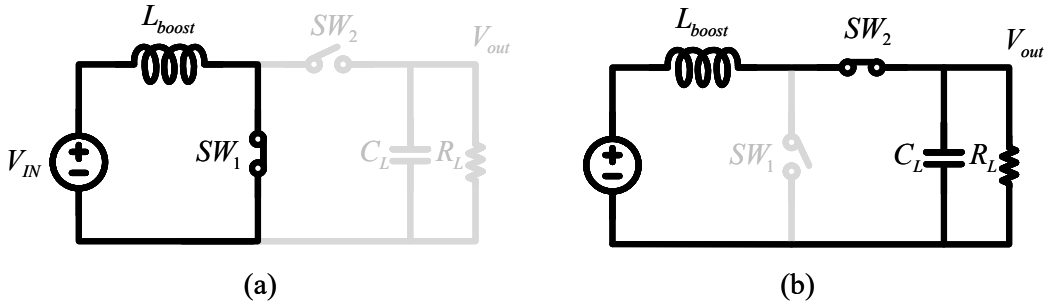


Figure 4.9: Schematic of a synchronous boost converter: (a) Phase 1, SW_1 is on and SW_2 is off; (b) Phase 2, SW_1 is off and SW_2 is on.

Figure 4.9 illustrates the two operational phases of a synchronous boost converter. During Phase 1, depicted in Figure 4.9a, the voltage across the inductor equals the input voltage V_{in}, and this phase lasts for a time interval known as the on-time, t_{on}. In Phase 2, shown in Fig-

ure 4.9b, the voltage across the inductor becomes $V_{out} - V_{in}$, corresponding to the off-time duration, t_{off}. The boost converter's behavior can be described using the volt-second balance principle, which relies on the steady-state condition. This principle asserts that, for a stable operation, the average voltage across the inductor over a complete switching cycle must be zero; otherwise, the inductor current would increase without bound.

In a synchronous boost converter operating under steady-state conditions, the volt-second balance principle ensures that the average voltage across the inductor over one full switching cycle is zero. Mathematically, this is expressed as

$$\overline{V_L} \cdot T = 0, \tag{4.1}$$

where $\overline{V_L}$ is the average voltage across the inductor over a switching period $T = t_{on} + t_{off}$. During the on-time t_{on}, as shown in Figure 4.9a,the switch is closed, and the inductor is directly connected to the input voltage V_{in}, so the voltage across the inductor is V_{in}. During the off-time t_{off}, as shown in Figure 4.9b, the switch is open, and the inductor voltage becomes $V_{in} - V_{out}$. Applying the volt-second balance yields

$$V_{in} \cdot t_{on} + (V_{in} - V_{out}) \cdot t_{off} = 0. \tag{4.2}$$

Rearranging this expression allows us to isolate the input-output voltage relationship:

$$V_{in} \cdot t_{on} = (V_{out} - V_{in}) \cdot t_{off}. \tag{4.3}$$

Dividing both sides by $V_{in} \cdot t_{off}$ gives

$$\frac{V_{out}}{V_{in}} = \frac{T}{t_{off}}, \tag{4.4}$$

and since the duty cycle D is defined as the ratio of the on-time to the total period, i.e., $D = t_{on}/T$, it follows that $t_{off} = T(1 - D)$. Substituting this into the equation results in

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D}. \tag{4.5}$$

This final expression represents the VCR of an ideal boost converter in continuous conduction mode (CCM).

Beyond the voltage conversion characteristics, the current behavior of a boost converter can be thoroughly examined through the inductor's current-voltage relationship during each phase of the switching cycle. In CCM, the inductor current never drops to zero, and its variation within each cycle can be analyzed to derive important design parameters.

During the on-state of the switch, corresponding to Phase 1, the inductor is directly connected to the input voltage source. As a result, a constant voltage of V_{in} is applied across the inductor over the time interval t_{on}. According to the fundamental inductor relation $V = L\frac{di}{dt}$, the inductor current increases linearly during this interval. The change in inductor current ΔI_1 over t_{on} is given by

$$\Delta I_1 = \frac{V_{in}}{L} \cdot t_{on} = \frac{V_{in}}{L} \cdot T_s D, \tag{4.6}$$

In the off-state or Phase 2, the switch opens and the inductor releases stored energy to the load via the output diode and capacitor. During this phase, the voltage across the inductor becomes $(V_{out} - V_{in})$, leading to a linear decrease in current. The corresponding current change ΔI_2 over the off-time $t_{off} = T_s(1 - D)$ is described by

$$\Delta I_2 = \frac{V_{out} - V_{in}}{L} \cdot t_{off} = \frac{V_{out} - V_{in}}{L} \cdot T_s(1 - D) \tag{4.7}$$

Under steady-state conditions, the net change in inductor current over one full cycle must be zero to ensure periodic operation. This implies that the increase in current during the on-phase must equal the decrease in current during the off-phase, i.e., $\Delta I_1 = \Delta I_2$. Equating Equations (4.6) and (4.7) again leads to the voltage conversion ratio previously derived in Equation (4.5), confirming internal consistency of the boost converter model.

When analyzing an ideal boost converter—i.e., one that neglects all parasitic resistances, switching losses, and voltage drops—the conservation of power principle applies. This means that the input power equals the output power:

$$V_{in} \cdot I_{in} = V_{out} \cdot I_{out} \tag{4.8}$$

Substituting the voltage ratio $V_{out}/V_{in} = 1/(1 - D)$ from Equation (4.5) into the above power equation allows for the derivation of a corresponding current relationship:

$$\frac{I_{in}}{I_{out}} = \frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{4.9}$$

which can be inverted to obtain the ratio of output current to input current:

$$\frac{I_{out}}{I_{in}} = 1 - D \tag{4.10}$$

4.2.1 Conduction Loss in Boost Converter

In practical boost converter designs, parasitic resistances present in components such as the inductor windings and switching devices lead to conduction losses. These losses originate from the flow of current through resistive elements, resulting in undesired power dissipation and decreased efficiency. Conduction losses are particularly significant when the converter operates under high load conditions, where elevated current levels exacerbate resistive power dissipation.

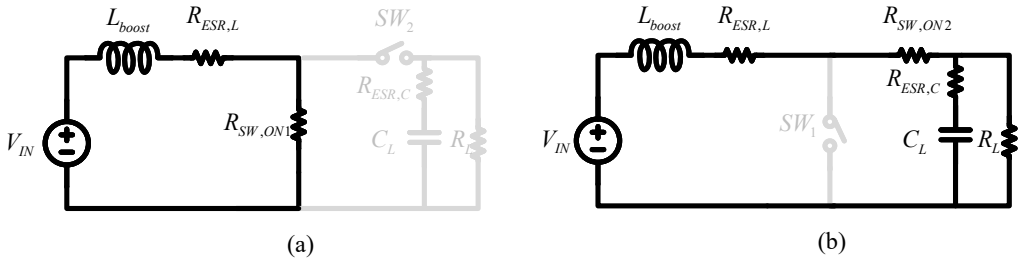


Figure 4.10: Schematic of more realistic boost converter: (a) Phase 1; (b) Phase 2.

Figure 4.10 illustrates a boost converter model incorporating parasitic resistive elements during its two operating phases. Specifically, the conduction losses in each phase arise from different resistive paths: in Phase 1, when switch S_1 is on, the current flows through the equivalent series resistance of the inductor ($R_{ESR,L}$) and the on-resistance of the switch ($R_{SW,ON1}$). In Phase 2, when the switch is off and the diode conducts, current passes through $R_{ESR,L}$ and the diode's equivalent on-resistance ($R_{SW,ON2}$).

The conduction loss for Phase 1 and Phase 2 can be expressed:

$$P_{loss1} = I_{rms}^2 \cdot (R_{ESR,L} + R_{SW,ON1}) \cdot D \tag{4.11}$$

$$P_{loss2} = I_{rms}^2 \cdot (R_{ESR,L} + R_{SW,ON2}) \cdot (1 - D) \tag{4.12}$$

, where $I_{rms}^2 = I_{avg}^2 + I_{rip\_rms}^2$ and D represents the duty cycle.

For a periodic waveform with a triangular shape, the general RMS definition,

$$I_{rms\_general} = \sqrt{\frac{1}{T_2 - T_1} \int_{T_1}^{T_2} I^2(t)\, dt} \tag{4.13}$$

simplifies to the well-known expression for triangular waveforms:

$$I_{rip\_rms} = \frac{I_{pp}}{2\sqrt{3}} \tag{4.14}$$

where I_{pp} is the peak-to-peak ripple current.

From Equations (4.6) and (4.7), it is evident that the magnitude of ripple current depends on both the inductance value and the switching frequency. Higher switching frequencies or larger inductances reduce the ripple, leading to lower AC losses.

These expressions clearly illustrate the quadratic dependence of conduction losses on current, emphasizing that even a small increase in either the average or ripple component of the current can result in a disproportionately large increase in power dissipation.

4.2.2 Switching Losses in Boost Converter

In a boost converter, switching losses are a major contributor to total power dissipation, especially at high switching frequencies. These losses primarily occur during the MOSFET's turn-on and turn-off transitions, due to both the overlap of voltage and current and the charging and discharging of parasitic capacitances.

The physical structure of a MOSFET includes unavoidable parasitic capacitances between the gate, drain, and source terminals—namely C_{gs}, C_{gd}, and C_{ds}. During each switching cycle, these capacitances must be charged or discharged, resulting in gate-drive losses. Since the gate capacitance is largely determined by the overlap area between the gate and the source/drain regions, it increases linearly with the MOSFET's width. As a result, the required gate charge Q also increases. The energy required to charge the gate to a voltage V_g is given by:

$$E_{\text{gate}} = Q \cdot V_g \tag{4.15}$$

Over time, this translates into a power loss due to gate charging:

$$P_{\text{gate}} = Q \cdot V_g \cdot f_s \tag{4.16}$$

where f_s is the switching frequency. Hence, the gate-drive loss increases linearly with switching frequency and MOSFET size.

In addition to gate charging loss, the MOSFET also incurs *hard-switching loss* due to the finite rise and fall times of voltage and current during transitions. During these periods, the drain-to-source voltage V_{DS} and the drain current I_D overlap, causing switching energy loss, which can be approximated by:

$$P_{\text{sw}} \approx \frac{1}{2} V_{DS} \cdot I_D \cdot (t_{rise} + t_{fall}) \cdot f_s \tag{4.17}$$

Here, t_{rise} and t_{fall} are the MOSFET's switching rise and fall times, respectively, which depend on the gate charge and the gate driver's current capability.

After determinng the topology of the rectifier and DC-DC converter, the overall system is shown in Figure 4.11. It consists of a cross-coupled rectifier and a boost converter. The received AC voltage is initially rectified into DC, which is subsequently stepped up to a higher level by the boost converter.

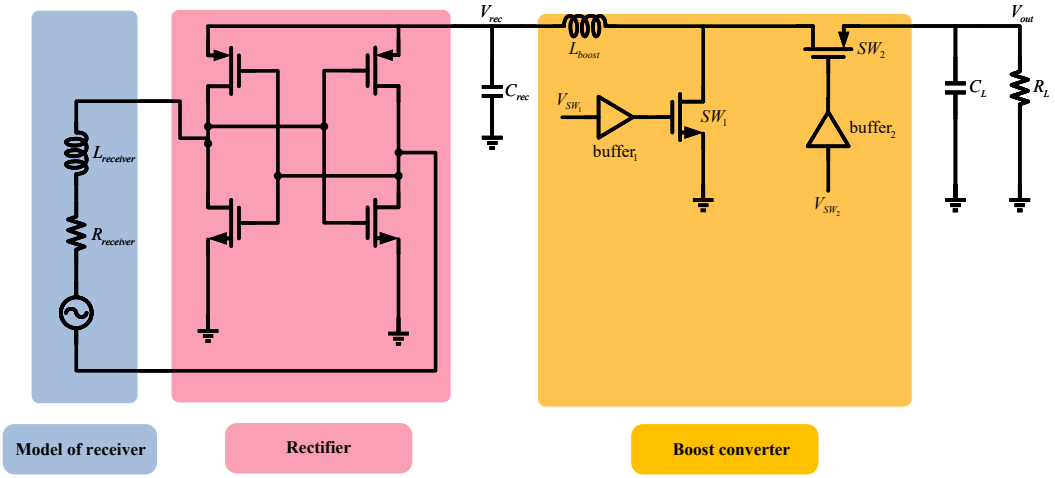


Figure 4.11: Schematic of overall system

4.3 Non-overlapping Signals Generator

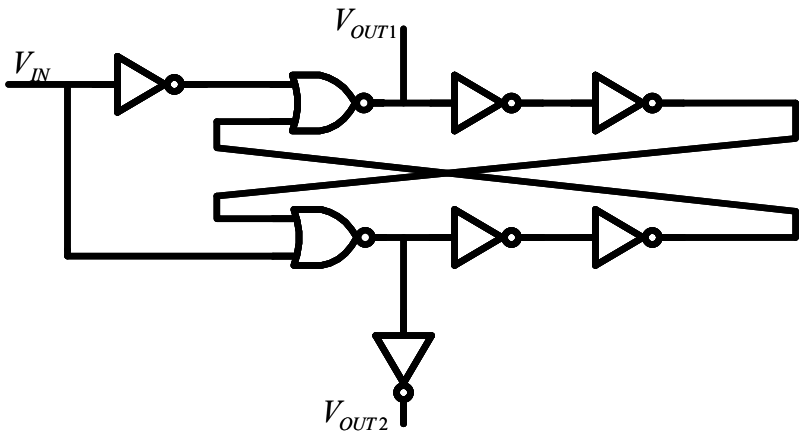


Figure 4.12: Schematic of non-overlapping signals generator

To address issue of shoot-through, a dead-time interval must be inserted between the two switching signals of SW_1 and SW_2. A non-overlapping signals generator can do this. The schematic of the non-overlapping signal generator is shown in Figure 4.12. Given a single input signal, it generates two non-overlapping output signals. The circuit consists of five inverters and two NOR gates. The two pairs of inverters on the right introduce a deliberate delay to enforce the dead-time. The main advantages of this design are its simplicity, robustness, and ease of integration into compact control architectures.

The dead time t_{dead} is a critical design parameter in boost converters: if it is too short, the high-side and low-side switches may overlap in conduction, resulting in shoot-through; if it is too long, excessive conduction losses occur. As shown in [33], the power loss attributable to dead time can be expressed as

$$P_{\text{loss}} = V_D \, I_{OUT} \left(t_{D_r} + t_{D_f} \right) f_{\text{SW}} \tag{4.18}$$

where

- V_D denotes the forward voltage drop of the body diode,
- I_{OUT} is the steady-state output current,
- t_{D_r} and t_{D_f} are the rising and falling dead-time intervals, respectively,
- f_{SW} is the switching frequency.

To ensure that the two switches do not conduct simultaneously, a minimal dead time is required. Through testing, we determined that a dead time of approximately 1.9 ns yields optimal results. Based on this requirement, we adjusted the sizes of the inverters to achieve the desired delay. According to [34], the delay of inverter can be expressed as:

$$t_p = 0.69 R_{ref} C_{iref} \left(1 + \frac{C_{ext}}{S C_{iref}} \right) \tag{4.19}$$

where:

- S: Inverter sizing factor, defined as the ratio of the MOSFET width in the current inverter to that in the minimum-size inverter;
- R_{ref}: Equivalent resistance of the minimum-size inverter;
- C_{iref}: Intrinsic capacitance of the minimum-size inverter;
- C_{ext}: External load capacitance;

From Equation (4.19), it can be observed that increasing the inverter size S leads to a reduction in propagation delay. The simulated relationship between S and delay is illustrated in Figure 4.13.

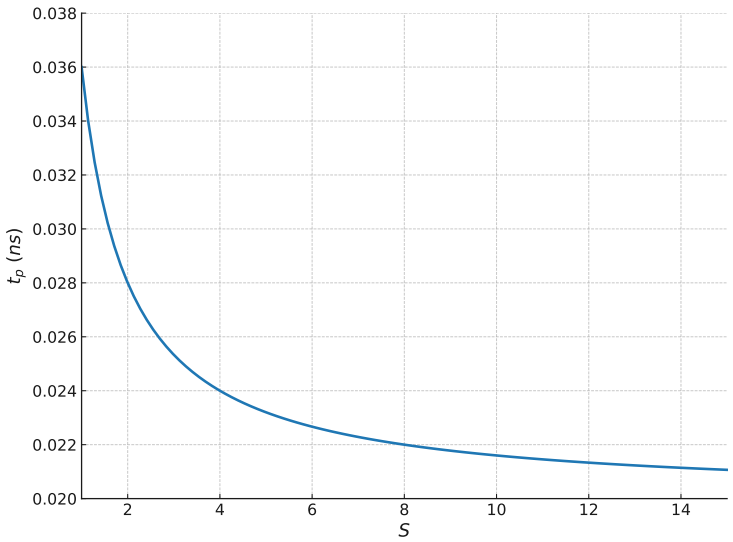


Figure 4.13: Simulation result of S on delay [34]

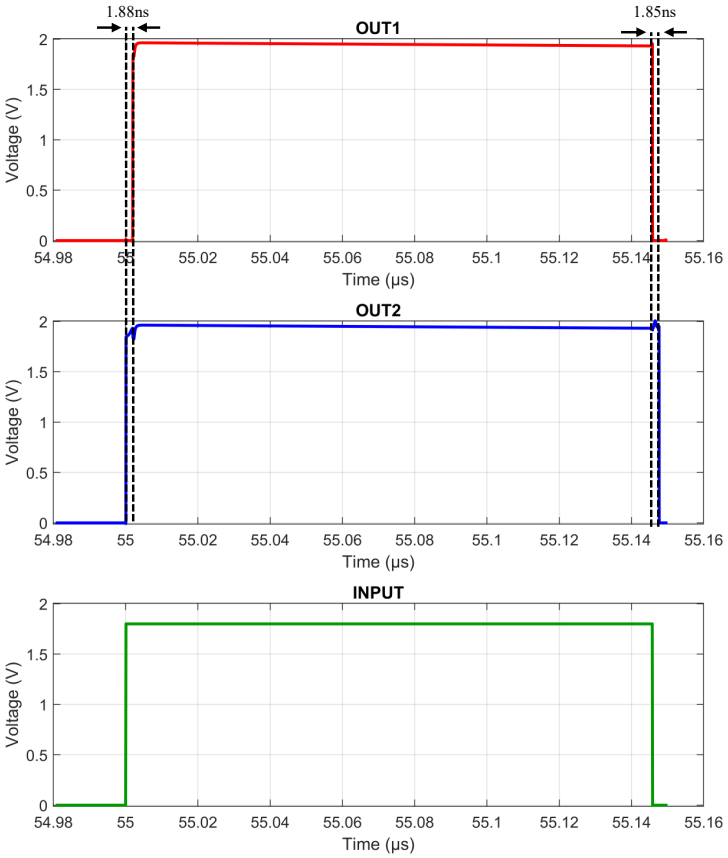


Figure 4.14: Simulation results of non-overlapping signals generator

The final simulation results are presented in Figure 4.14. The lower part of Figure 4.14 presents enlarged views of the two regions marked by dashed boxes in the upper part of the figure.

To verify that the selected dead time effectively prevents simultaneous conduction of the two switches (one PMOS and one NMOS), we also plotted the waveforms of V_{GS} and V_{SG}, as shown in Figure 4.15.

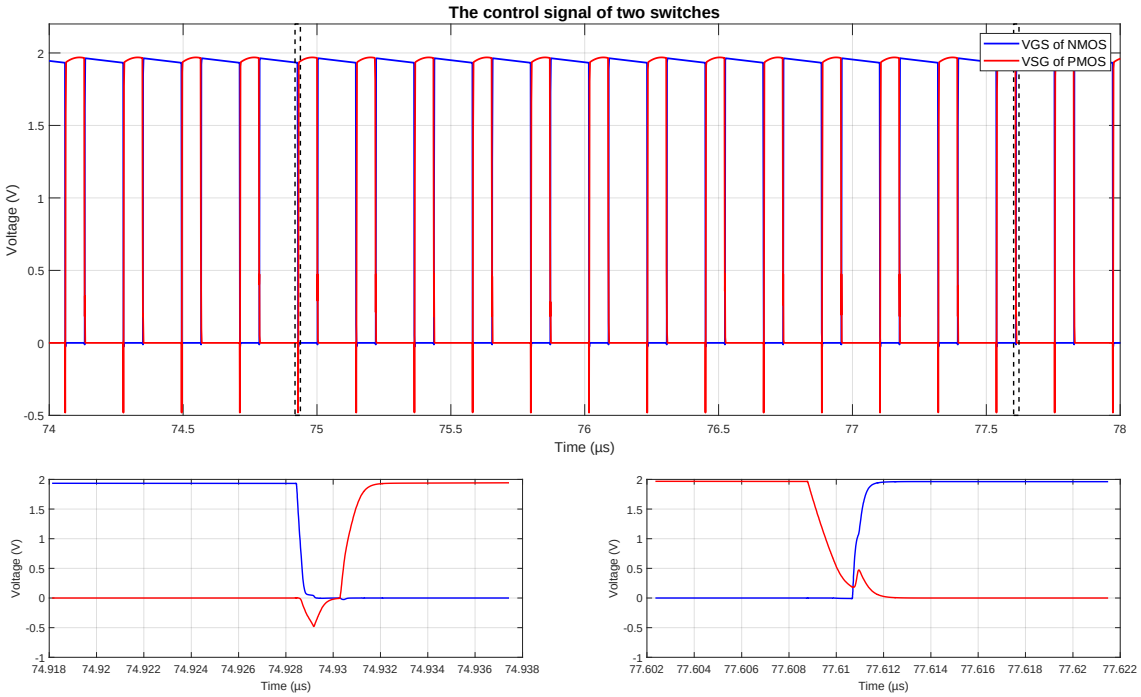


Figure 4.15: The V_{GS} of NMOS and V_{SG} of PMOS

4.4 Maximum Voltage Selector

Usually, during start-up, due to the body diode of PMOS of boost converter, energy can be passed to the load with a voltage drop of that body diode, but we observed that during the start-up phase, the system may fail to operate properly because the supply voltage of the buffers (buffer 1 and buffer 2 in Figure 4.11) is insufficient to overcome the threshold voltages of the boost converter switches. As a result, the boost converters cannot start, and since the buffer supply voltage is derived from the output voltage, this leads to a self-sustaining failure: the boost converter does not operate because the output voltage does not rise, and the output voltage does not rise because the boost converter is not operating. However, we also observed that during start-up, the voltage at the output of the rectifier is sufficient to overcome the threshold voltages of the boost converter switches. Therefore, to address this start-up issue, a maximum voltage selector is required to ensure reliable system initialization.

The schematic of the maximum voltage selector is shown in Figure 4.16. The left section

consists of a constant-g_m circuit, which provides a stable bias current for the transistors.

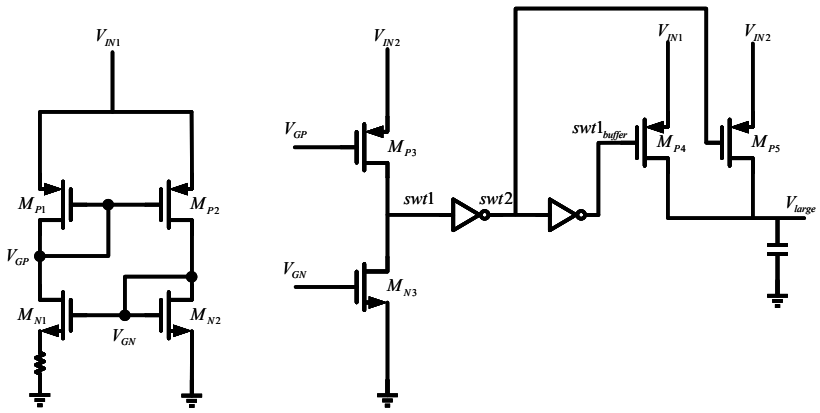


Figure 4.16: Schematic of maximum voltage selector

In this circuit, the transistor pairs M_{P2}–M_{P3} and M_{N2}–M_{N3} are designed to be matched. When the voltage at V_{IN2} exceeds that of V_{IN1}, the gate–source voltage of M_{P3} becomes greater than that of M_{P2}. Although the drive strength of M_{N3} remains equal to that of M_{N2} and M_{P2} due to matching, M_{P3} gains an advantage under this condition and drives the signal $swt1$ to a high level (close to V_{IN2}). Conversely, when V_{IN2} is lower than V_{IN1}, the drive capability of M_{P3} diminishes relative to M_{N3}, resulting in $swt1$ transitioning to a low level.

For simulation, V_{IN1} is connected to the rectifier output V_{rec}, and V_{IN2} is connected to the boost converter output V_{out}. As shown in Figure 4.17, the simulation results demonstrate that the maximum voltage selector effectively identifies the larger voltage between V_{out} and V_{rec}.

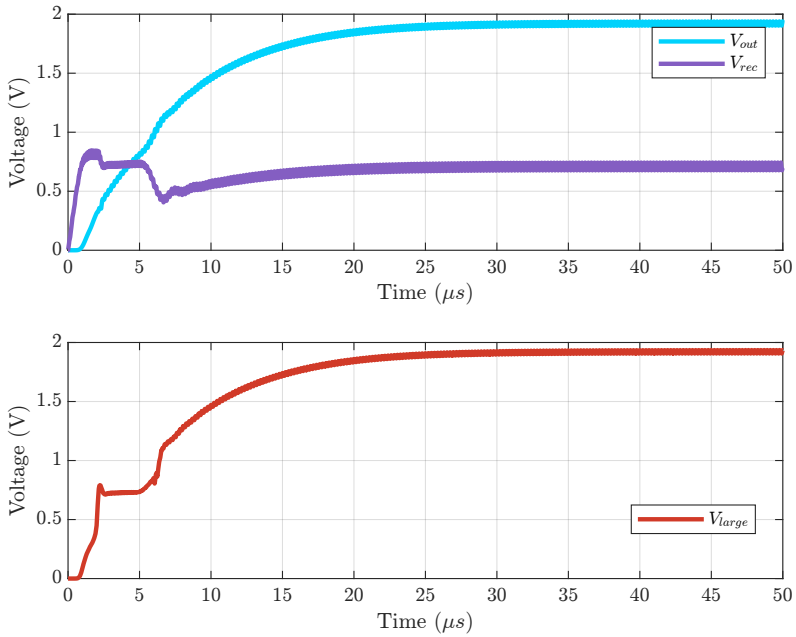


Figure 4.17: Simulation results of maximum voltage selector

4.5 Maximum Power Point Tracking

4.5.1 Maximum Power Transfer Theorem

The Maximum Power Transfer Theorem states that, in a linear network, maximum power is transferred from a source to a load when the load resistance R_L is equal to the internal resistance of the source R_S.

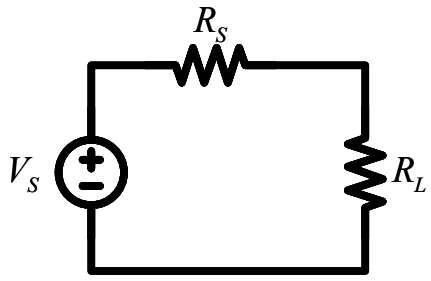


Figure 4.18: Schematic of model for analyzing maximum power transfer theorem

Consider a DC circuit in which a voltage source V_S has a series internal resistance R_S and is connected to a load resistance R_L. The power delivered to the load is given by:

$$P_L = \frac{{V_S}^2 R_L}{(R_S + R_L)^2} \tag{4.20}$$

To determine the condition for maximum power transfer, differentiate (4.20) with respect to R_L and set the derivative to zero:

$$\frac{dP_L}{dR_L} = 0 \quad \Rightarrow \quad R_L = R_S \tag{4.21}$$

Substituting (4.21) into (4.20) yields the maximum power:

$$P_{\text{max}} = \frac{V^2}{4R_S} \tag{4.22}$$

For an AC voltage source with peak amplitude V_{ac}, the RMS voltage is:

$$V_{\text{RMS}} = \frac{V_{ac}}{\sqrt{2}} \tag{4.23}$$

The condition for maximum power remains $R_L = R_S$, and the power delivered to the load

becomes:

$$P_{\text{max}} = \frac{V_{\text{RMS}}^2}{4R_S} = \frac{1}{4R_S} \cdot \left(\frac{V_{ac}}{\sqrt{2}}\right)^2 = \frac{V_{ac}^2}{8R_S} \tag{4.24}$$

In general situations where the source impedance is complex, the condition for maximum power transfer is different from the purely resistive case. Let the source impedance be expressed as $Z_S = R_S + jX_S$, and the load impedance as $Z_L = R_L + jX_L$. The current flowing through the load is given by

$$I = \frac{V_S}{Z_S + Z_L} = \frac{V_S}{(R_S + R_L) + j(X_S + X_L)}. \tag{4.25}$$

The average power delivered to the load is

$$P_L = \frac{1}{2}|I|^2 R_L = \frac{1}{2} \cdot \frac{|V_S|^2}{(R_S + R_L)^2 + (X_S + X_L)^2} \cdot R_L. \tag{4.26}$$

,where $|I|$ denotes the amplitude of I and $|V_S|$ denotes the amplitude of V_S.

To maximize P_L, first the denominator needs to be minimized. This occurs when the reactive components cancel, i.e., $X_L = -X_S$. Substituting this into the

$$P_L = \frac{1}{2} \cdot \frac{|V_S|^2}{(R_S + R_L)^2} \cdot R_L. \tag{4.27}$$

Differentiating with respect to R_L and setting the derivative to zero. According to (4.21), the maximum occurs when $R_L = R_S$. Therefore, the load impedance that maximizes power transfer must satisfy

$$Z_L = Z_S^*, \tag{4.28}$$

which is known as conjugate matching. This condition ensures that the total impedance seen by the source is purely resistive, maximizing the current and thereby maximizing real power delivered to the load.

4.5.2 Impedance Transformation of Rectifier

To simplify the analysis, a FBR is modeled using an ideal sinusoidal current source with amplitude I_p. The DC component of the rectified current is calculated as

$$I_{dc} = \frac{\int_0^{T/2} I_p \sin\left(\frac{2\pi}{T}t\right) dt}{\frac{T}{2}} = \frac{2}{\pi} I_p \tag{4.29}$$

where I_p is the peak value of the sinusoidal input current.

Accordingly, the output DC voltage is

$$V_{dc} = \frac{2}{\pi} I_p \cdot R_L \tag{4.30}$$

Assuming the current source operates at frequency f_p, the average power delivered over one cycle only includes the contributions from the components of voltage and current at the same frequency f_p. Higher-order harmonics in the square waveform V_p do not contribute to average power [35]. Thus, only the fundamental component of V_p is considered.

The average input power P_{in} can therefore be expressed as

$$P_{in} = \frac{1}{2} V_{p,\text{fund}} I_p \tag{4.31}$$

where $V_{p,\text{fund}}$ is the fundamental component of V_p, given by

$$V_{p,\text{fund}} = \frac{4}{\pi} V_{dc} \tag{4.32}$$

The waveforms of V_p, $V_{p,\text{fund}}$, and i_p are illustrated in Fig. 4.19.

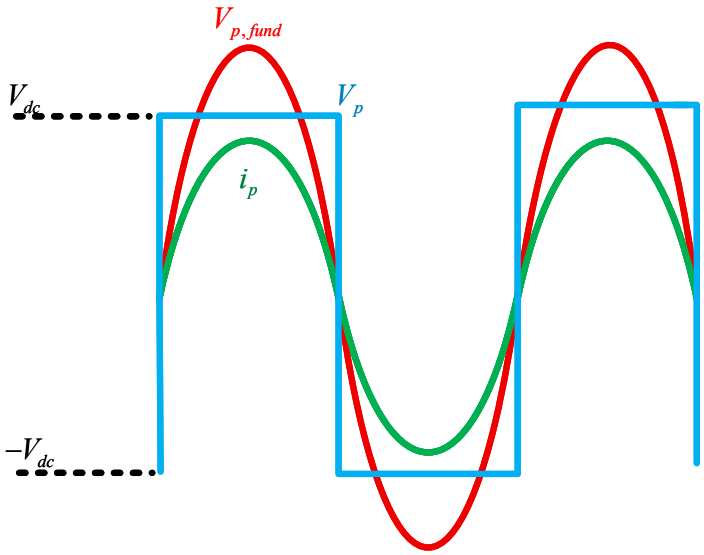


Figure 4.19: Waveforms of V_p, i_p, and $V_{p,\text{fund}}$

Substituting (4.32) into (4.31), the input power becomes

$$P_{in} = \frac{1}{2} V_{p,\text{fund}} I_p = \frac{1}{2} \cdot \frac{4}{\pi} V_{dc} I_p = \frac{1}{2} \cdot \frac{8}{\pi^2} R_L I_p^2 \tag{4.33}$$

Alternatively, since R_{in} represents the equivalent input resistance seen by the source, the input power can also be written as

$$P_{in} = \frac{1}{2} R_{in} I_p^2 \tag{4.34}$$

This equivalent transformation is illustrated in Figure 4.20.

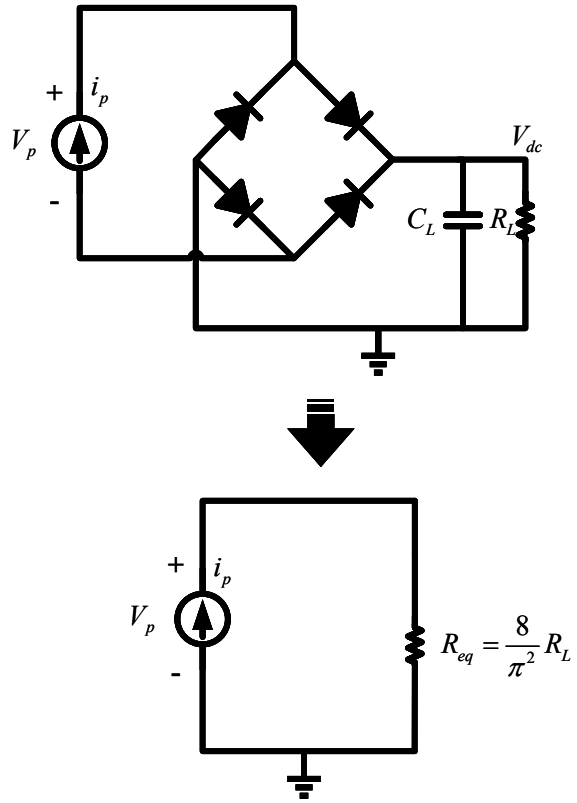


Figure 4.20: Equivalent input model of the rectifier

4.5.3 Impedance Transformation of Boost Converter

DC-DC converter can also do the impedance transformation, Under ideal CCM operation, the power delivered to the load is equal to the power drawn from the source, i.e.,

$$P_{in} = P_{out} = \frac{V_{out}^2}{R_L} = V_{in} \cdot I_{in}, \tag{4.35}$$

where V_{in} and V_{out} are the input and output voltages, I_{in} is the input current, and R_L is the resistive load, as shown in Figure 4.21.

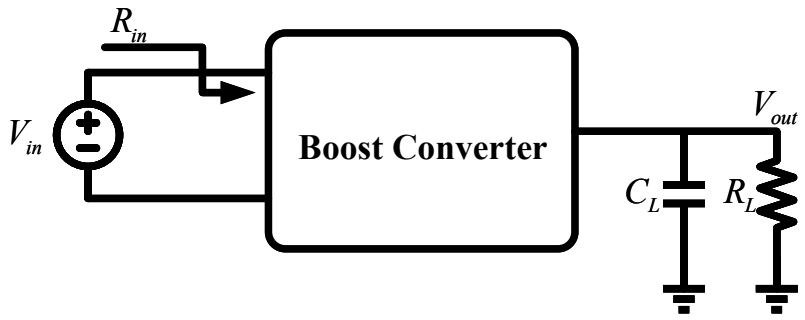


Figure 4.21: R_{in} of boost converter

As shown in Figure 4.21, the equivalent input resistance R_{in} observed from the source can be expressed as

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}^2 R_L}{V_{out}^2}. \tag{4.36}$$

Considering the ideal voltage conversion ratio of a boost converter,

$$V_{out} = \frac{V_{in}}{1 - D}, \tag{4.37}$$

where D is the duty cycle, the input resistance becomes

$$R_{in} = R_L(1 - D)^2. \tag{4.38}$$

This result indicates that a boost converter performs impedance transformation, effectively reflecting the load resistance to the input side scaled by the square of the complement of the duty cycle. As the duty cycle increases, the input impedance decreases nonlinearly.

4.5.4 Algorithms for Maxmium Power Point Tracking

Conventional maximum power point tracking (MPPT) techniques are typically employed to maximize the power output of the transducer. However, the objective of this project is to ensure maximum power delivery to the load. As discussed above, both the rectifier and the boost converter influence the load resistance as perceived from the source. To achieve maximum power transfer, the load impedance must be matched to the source impedance. Since the impedance transformation introduced by the rectifier is fixed, only the duty cycle of the boost converter can be tuned to adjust the equivalent load impedance seen from the source. Considering that the load is a fixed resistor, the voltage across it can serve as an indicator of power transfer. When this voltage reaches its maximum, the power delivered to the load is also maximized.

The common techniques employed in energy harvesting systems include fractional open-circuit

voltage (FOCV) and perturb and observe (P&O) [36]. The FOCV technique exploits the near-linear relationship between the open-circuit voltage (V_{oc}) of transducer and its maximum power point voltage (V_{mpp}), expressed as:

$$V_{mpp} = K_{trans} \times V_{oc} \tag{4.39}$$

where K_{trans} (typically 0.7–0.9) is determined from the transducer module's I–V characteristics or manufacturer data [37].

FOCV offers simple implementation and low cost, making it suitable for resource-constrained systems [38]. However, it requires periodic open-circuit measurements, leading to brief power loss and reduced tracking accuracy under rapidly changing conditions.

The P&O algorithm incrementally adjusts the rectified output power toward the maximum power point (MPP) in a stepwise manner [39].When the measured power at the current perturbation step exceeds that of the preceding step, the algorithm continues perturbing in the same direction toward the MPP; otherwise, the perturbation direction is reversed. Under steady-state conditions, it oscillates within a narrow range around the MPP, thereby enabling robust and sustained MPPT operation. This approach is independent of the specific characteristics of the energy harvester and maintains continuous tracking capability.

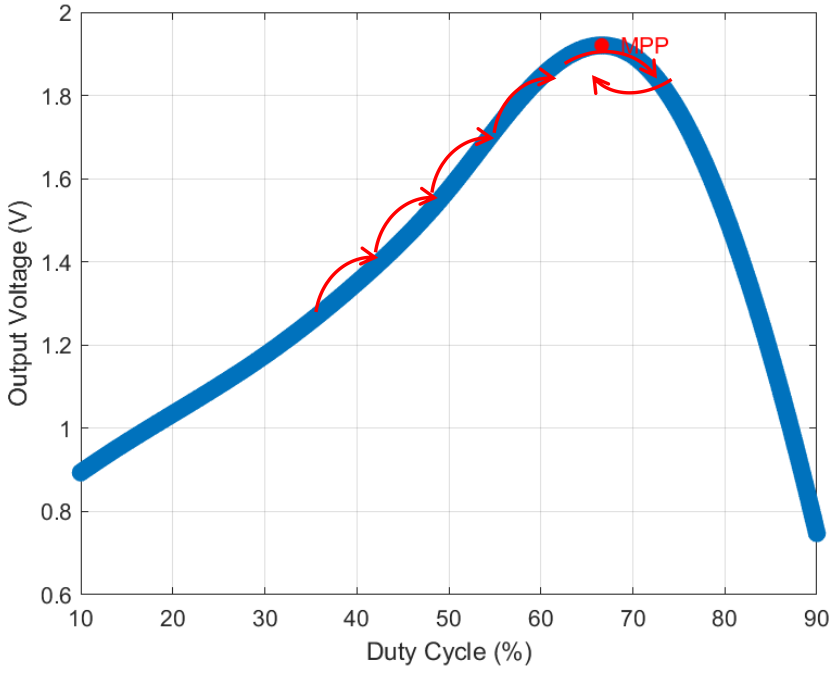


Figure 4.22: Adapted P&O algorithm

As previously stated, the objective of this thesis is to maximize the power delivered to the load rather than to maximize the power output of the transducer. Therefore, the use of the FOCV

method is considered unsuitable for the present case. Instead, P&O algorithm is adapted to meet the requirements. Maximum power transfer to the load is achieved when the source impedance is matched to the equivalent load impedance, which is regarded as the MPP for the load. In the proposed approach, the voltage across the load is monitored, and the duty cycle is adjusted based on this feedback in a manner consistent with the P&O algorithm, as illustrated in Fig.4.22. When an increase in the duty cycle is observed to result in a higher voltage across the load, the tuning direction is regarded as correct, and the duty cycle is further increased. Conversely, when a decrease in the voltage across the load is observed, the tuning direction is regarded as incorrect, and the duty cycle is reduced accordingly. Furthermore, when an increase in the duty cycle is observed to result in a lower voltage across the load, the tuning direction is again regarded as incorrect, and the duty cycle is decreased. The specific operation of this adapted P&O algorithm is illustrated in Figure 4.23.

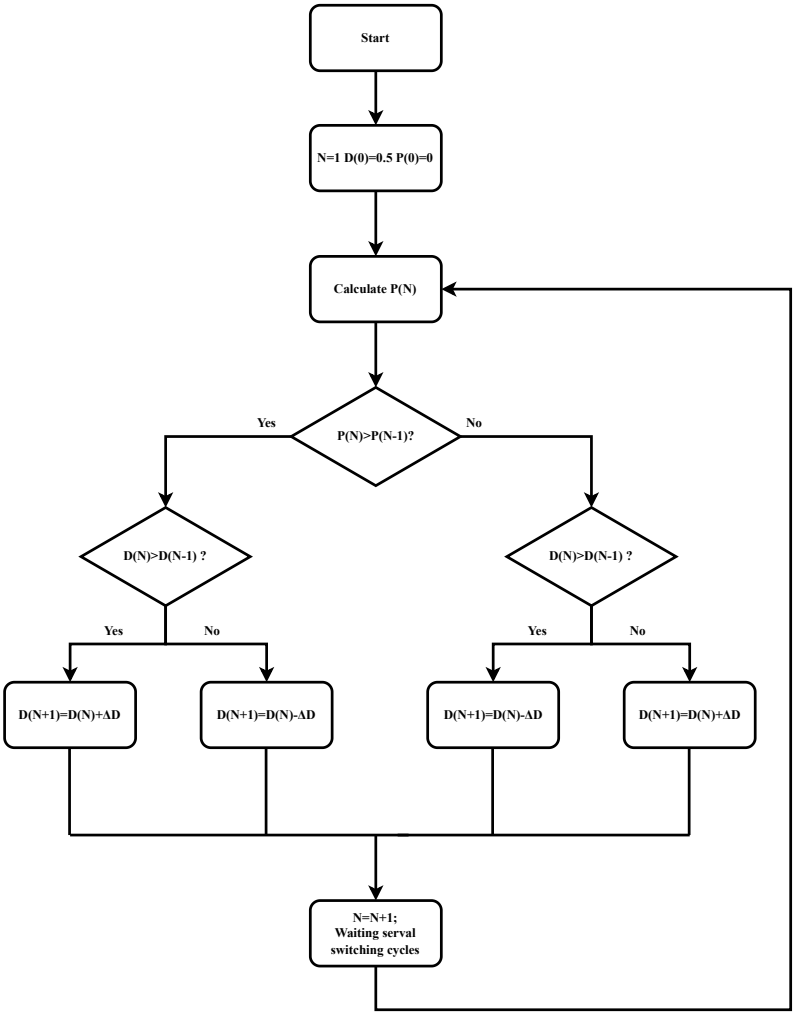


Figure 4.23: Flow of adapted P&O algorithm

The implementation of the adapted P&O algorithm is illustrated in Figure 4.24. The system's

output voltage, V_{out}, is sampled by a Sample and Hold (S&H) circuit. The voltage stored in the S&H circuit is then compared with V_{out} in the subsequent sampling cycle. A comparator generates a signal, V_{Dir}, which indicates whether V_{out} is increasing or decreasing. This signal, V_{Dir}, is then fed into the adapted P&O logic, along with $V_{tunedir}$ from the previous cycle, to determine the new value of $V_{tunedir}$. Based on the updated $V_{tunedir}$, the value of a 6-bit register is adjusted and compared with a digital counter to generate square waves with a specific duty cycle.

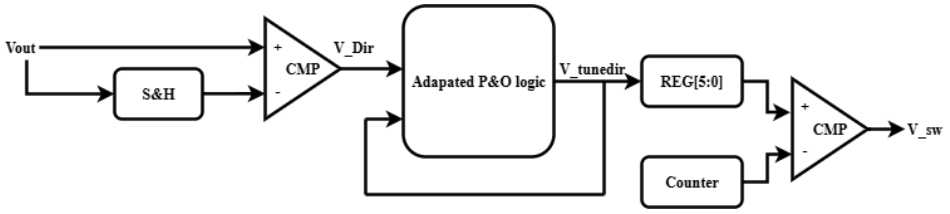


Figure 4.24: Realization of adapted P&O algorithm

For instance, if V_{out} is increasing during the current cycle, V_{Dir} will be at a high level. Assuming that the $V_{tunedir}$ from the previous cycle was at a high level, this would indicate that the duty cycle for the current cycle is higher than that of the previous cycle. The adapted P&O logic then determines that the $V_{tunedir}$ for the current cycle should remain at a high level, thus increasing the duty cycle. Consequently, the value of the register is incremented by 1, leading to an increase in the duty cycle of the switching signal, V_{sw}.

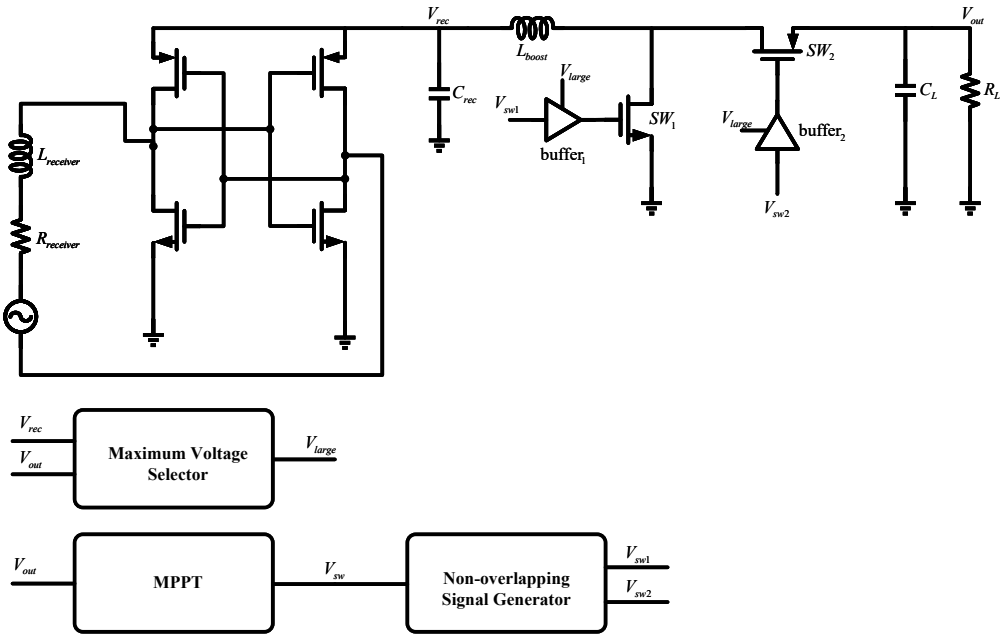


Figure 4.25: Schematic of completed system

The complete system is depicted in Figure 4.25. It comprises a cross-coupled rectifier, a synchronous boost converter, a maximum voltage selector to supply buffers within the circuit to address the start-up issue, a MPPT block to ensure the load receives the maximum power, and a non-overlapping signal generator to prevent simultaneous conduction of the two switches in the boost converter.

In the simulation, a 4.6 MHz AC voltage source with an amplitude of 1.5 V (3 V_{pp}) is applied. The load resistor is set to 882 Ω to emulate the actual load conditions. The duty-cycle adjustment step size is set to 1%, and the waiting time parameter, T_{wait}, is configured as 20 times the ultrasonic cycle.

The simulation results of the complete system are shown in Fig. 4.26. As the system requires sufficient time to reach steady-state operation, the MPPT logic is initiated at 100 μs. A waiting period T_{wait}, indicated in Fig. 4.26, is required after each duty-cycle adjustment to allow the system to stabilize. Once the maximum power point (MPP) is reached, the duty cycle oscillates around this point, resulting in oscillations in V_{out}. A larger T_{wait} increases the convergence time but reduces oscillation, whereas a smaller T_{wait} accelerates convergence but may prevent proper MPPT operation and increase oscillations.

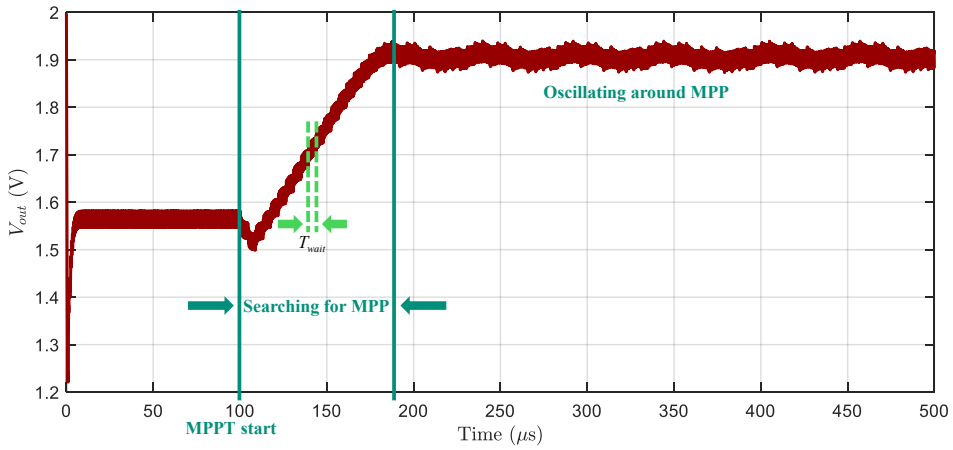


Figure 4.26: Simulation result of adapted P&O algorithm

The duty-cycle adjustment step size is also a critical parameter. A large step size reduces the MPP search time but may yield a suboptimal operating point, resulting in a significant deviation between the estimated and true MPP. Conversely, a smaller step size improves accuracy but increases convergence time.

The simulation results for three cases with different T_{wait} values and duty-cycle tuning step sizes are shown in Figs. 4.27 and 4.28. These results are consistent with the aforementioned analysis regarding the impact of T_{wait} and the duty-cycle tuning step size.

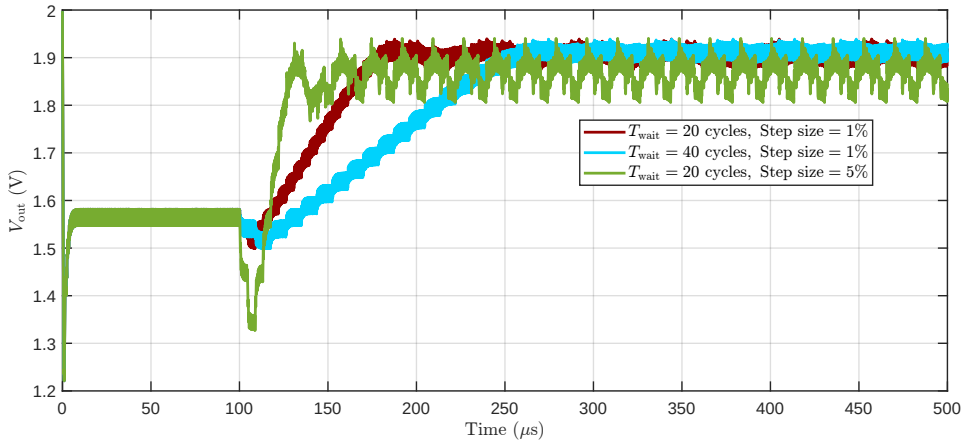


Figure 4.27: Comparison of adapted P&O algorithm with different parameters

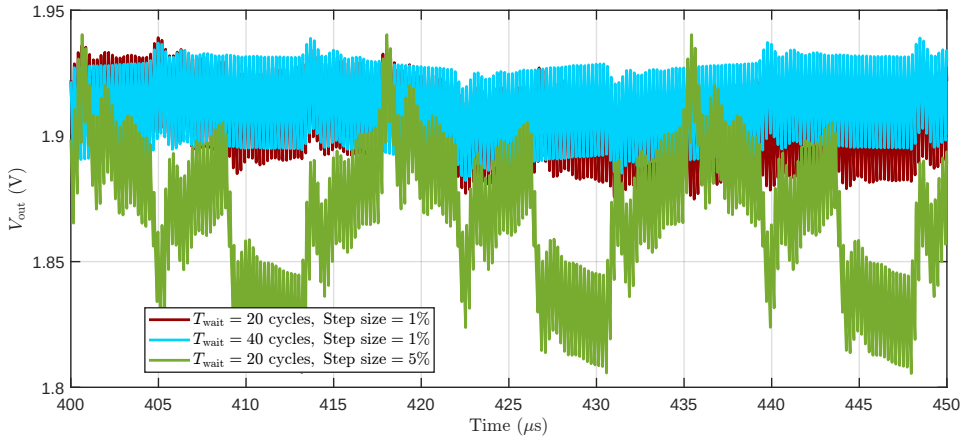


Figure 4.28: Enlarged view of the oscillation period in the MPPT simulation of Fig. 4.27

The system efficiency is defined as

$$\eta = \frac{P_L}{P_{\text{av}}}, \tag{4.40}$$

where P_L denotes the power delivered to the load and P_{av} represents the available power from the ultrasonic transducer. Simulation results indicate that the proposed design achieves an overall system efficiency of 83.09%, with the cross-coupled rectifier and the boost converter achieving efficiencies of 91.57% and 90.74%, respectively.

Figure 4.29 compares the system performance with and without MPPT. For the case without MPPT, the cross-coupled rectifier is configured as in the previous simulation, with two NMOS and two PMOS transistors, each sized at $4.8\,\text{mm}/0.26\,\mu\text{m}$. In the boost converter, the inductor value is set to $5\,\mu$H, and the switching frequency is matched to the ultrasound frequency of 4.6 MHz. The sizes of the switching devices are $400\,\mu\text{m}/0.26\,\mu\text{m}$ for PMOS SW_1 and $1.6\,\text{mm}/0.26\,\mu\text{m}$ for NMOS SW_2. For the case with MPPT, T_{wait} is set to 20 cycles of the 4.6 MHz ultrasound frequency, the step size for duty-cycle tuning is 1%, the initial duty cycle

is 0.5, and the initial output voltage V_{out} is 0 V. All other parameters remain the same as in the case without MPPT.

It is evident that the MPPT algorithm significantly increases V_{out}. The MPP determined by the adapted P&O algorithm is very close to the optimal MPP obtained by sweeping the duty cycle. Specifically, the peak V_{out} achieved using the adapted P&O algorithm is 1.939 V, whereas sweeping the duty cycle yields a peak V_{out} of 1.941 V. These results indicate that the MPPT algorithm achieves a high accuracy.

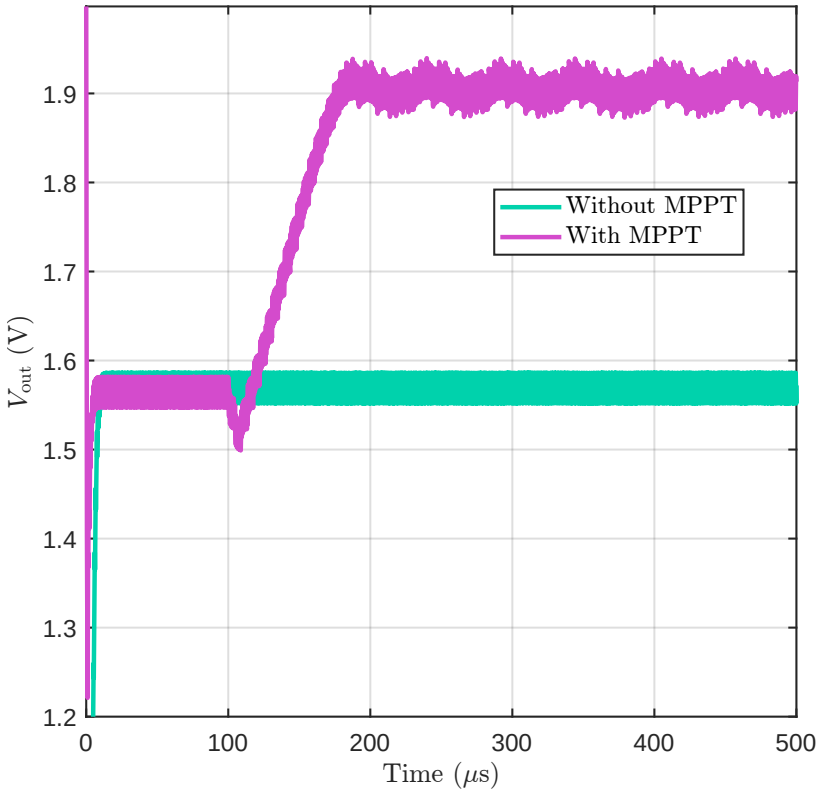


Figure 4.29: Comparison of output voltage with MPPT and without MPPT

Figure 4.30 shows the output power for different load resistances, R_L. Over a wide range of load resistances, the output power remains approximately 4.2 mW when the adapted P&O logic is applied.

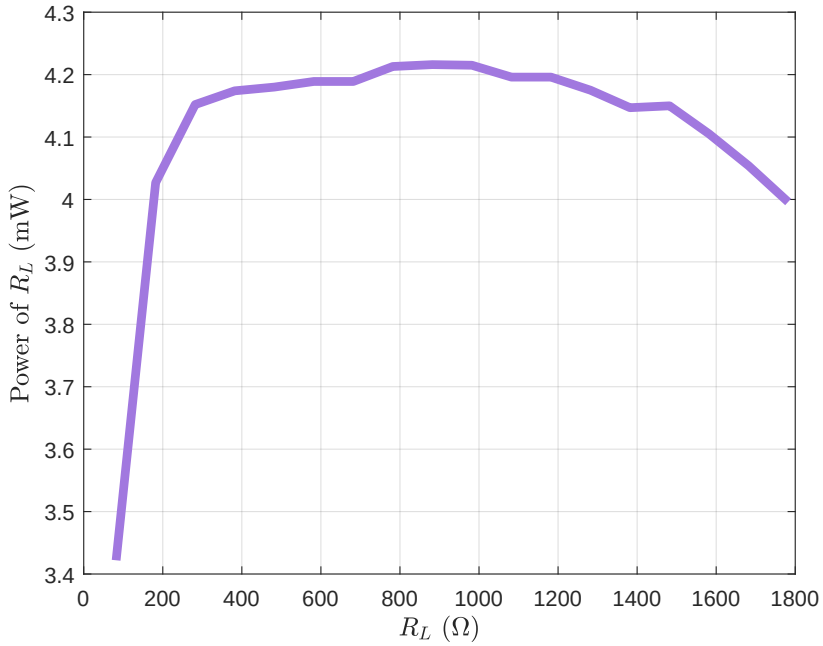


Figure 4.30: Output power vs load resistor

Figure 4.31 shows the system efficiency for various load resistances. It can be observed that, over a wide range of load resistances, the system maintains an efficiency greater than 82%.

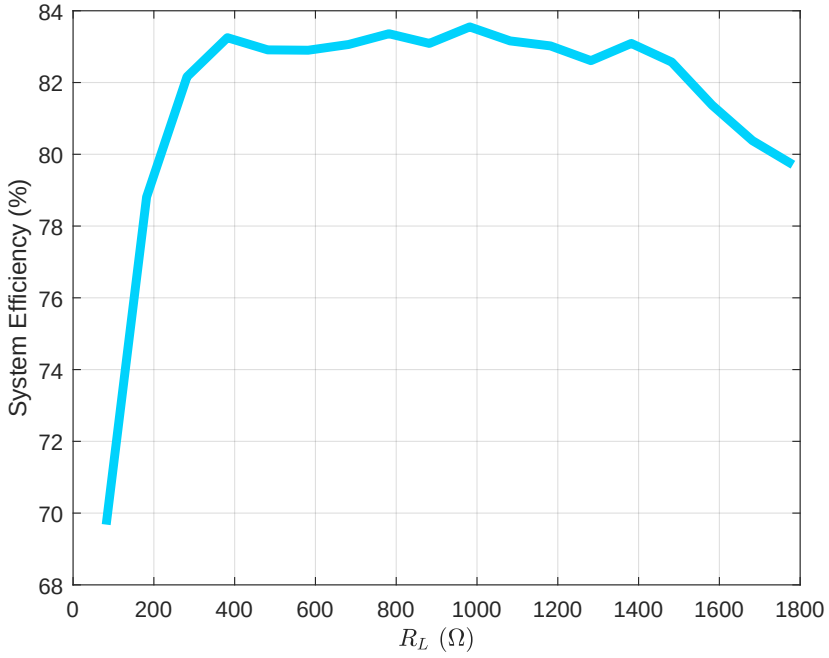


Figure 4.31: System efficiency vs load resistance

Figure 4.32 illustrates the system efficiency for various input voltage amplitudes V_{in} while R_L keeps constant. As previously noted, when V_{in} is too low, the rectifier cannot operate fully,

resulting in reduced efficiency. The figure shows that once V_{in} is sufficiently high to enable full rectifier operation, the efficiency stabilizes at approximately 83%.

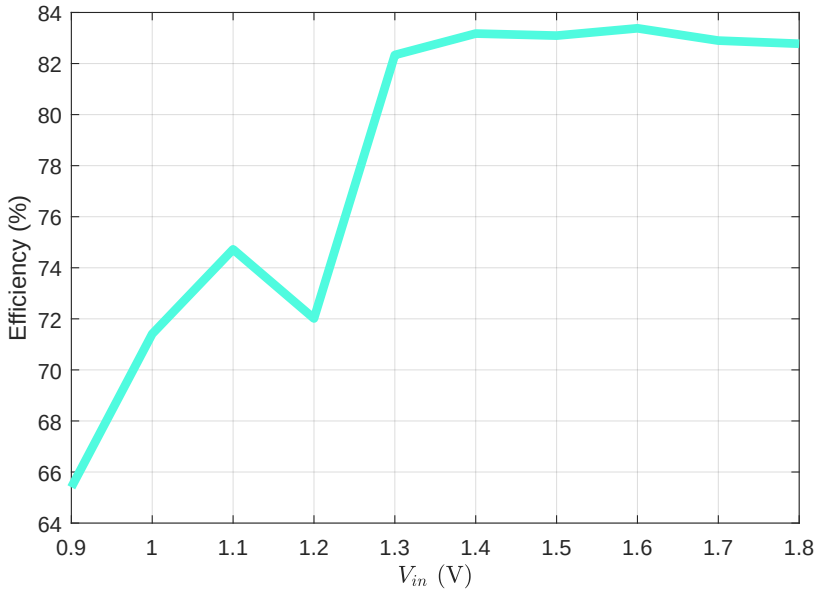


Figure 4.32: System efficiency vs V_{in}

Chapter 5

PCB Design

Compared with tape-out, PCB implementation provides a simpler and faster approach to verify the system designed in this thesis, and it can be more easily integrated with an ultrasonic transmitter to form a complete WPT system. The discrete component version of the design was also proposed. It has three SMA connectors, a cross-coupled rectifier, a synchronous boost converter. The right SMA connector is used for connecting to input voltage. The left two SMA connectors are used for connecting to gate signals of two switches of boost converter. The load resistor will be added externally. For the adapted P&O MPPT logic, the implementation is carried out on an STM32 development board STM32L476RGTX.

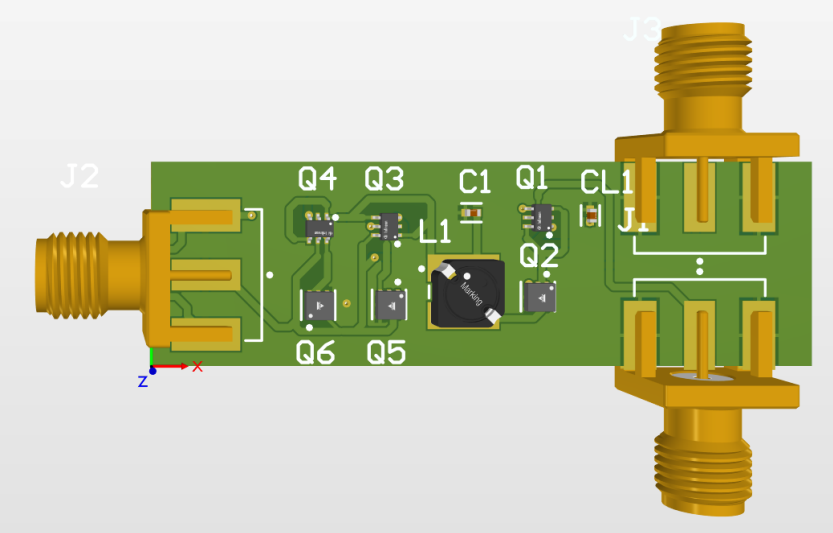


Figure 5.1: PCB board appearance

The components of this PCB is listed in Table 5.1.

Table 5.1: Bill of Materials

Name	Description	Quantity
CL05B103KO5NNNC	10nF Ceramic Capacitor	2
142-0701-801	SMA Connector	3
74408941050	5μH Inductor	1
BSD223P	PMOS	3
SIB452DK-T1-GE3	NMOS	3

To evaluate the cross-coupled rectifier in the PCB design, simulations were performed in LTSpice using the manufacturer's SPICE model of the device. The source impedance was set to $50 + j22.5\ \Omega$, identical to the previous configuration. The load was a 10 nF capacitor, and the input was a 4.6 MHz AC signal with an amplitude of 1.5 V. The simulation result is shown in Figure 5.2.

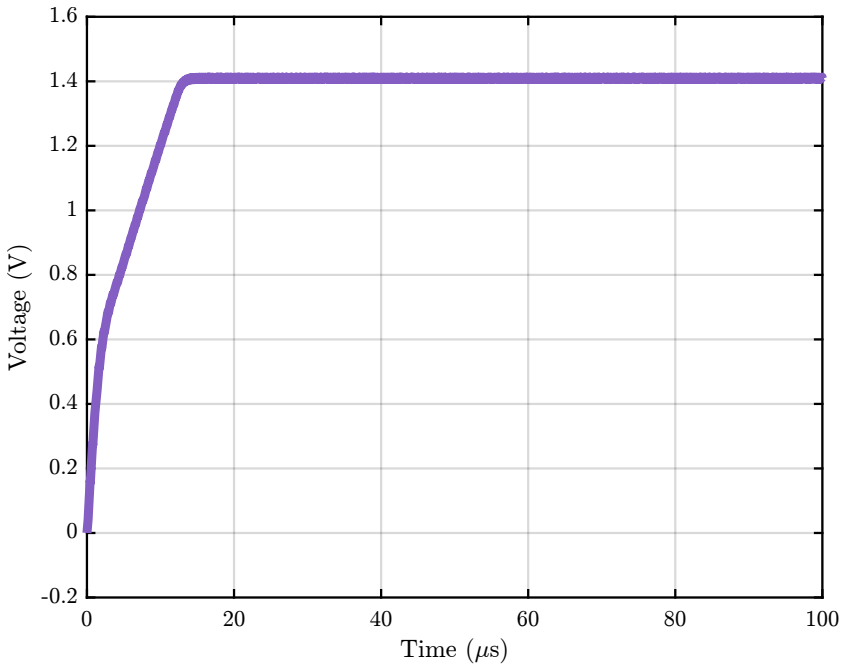


Figure 5.2: Simulation result of cross-coupled rectifier in PCB design

A similar simulation was also performed for the boost converter. The input was a 1 V DC source, and the switching frequency was set to 4.6 MHz, identical to the ultrasound frequency. The duty cycle was fixed at 50%. The load consisted of a 10 nF capacitor in parallel with an 882 Ω resistor. The simulation result is shown in Figure 5.3.

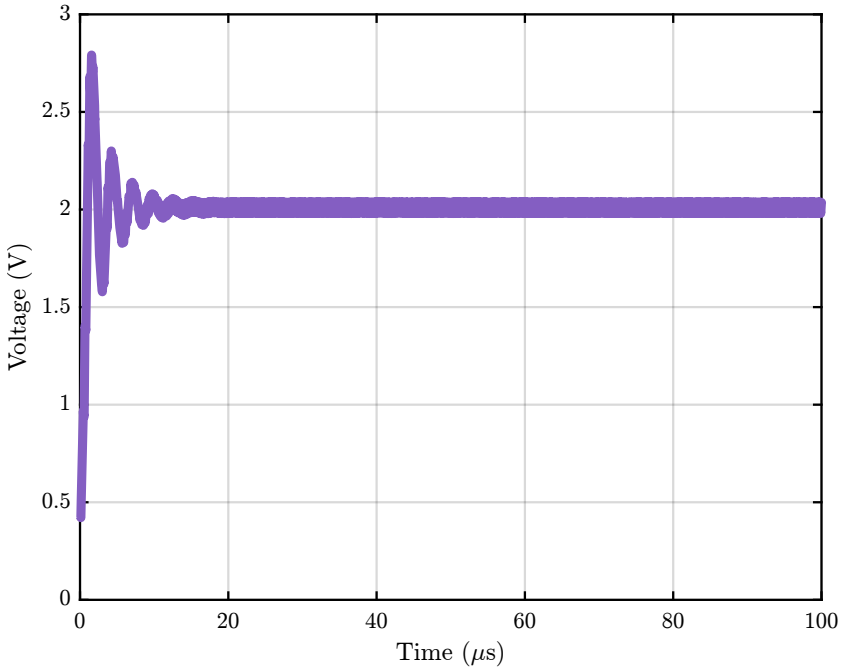


Figure 5.3: Simulation result of boost converter in PCB design

However, due to time constraints, the PCB has not been tested in the laboratory. As a result, the adapted P&O MPPT logic could not be verified, since no simulation environment is available for testing the STM32 code.

Chapter 6

Conclusion

6.1 Conclusions

This thesis presents a receiver circuit suitable for ultrasonic WPT. The system is designed to maximize power delivery to the load by mitigating impedance mismatch between the source and the load. Several rectifier topologies are analyzed, and the cross-coupled rectifier is ultimately selected due to its simplicity and superior performance. A boost converter is incorporated to further increase the rectified voltage. Moreover, both the rectifier and the boost converter can transform the equivalent load resistance seen by the source; however, the duty cycle of the boost converter is the only parameter that can be tuned. According to the maximum power transfer theorem, adjusting the duty cycle allows the equivalent load impedance to match the source impedance. Unlike conventional MPPT techniques, which aim to maximize the power output of the transducer rather than the power delivered to the load, the proposed adapted P&O MPPT algorithm focuses on maximizing the load power. By dynamically adjusting the duty cycle, the algorithm achieves automatic impedance matching, thereby ensuring optimal power transfer to the load. The influence of MPPT parameters is also analyzed and verified through simulations. The proposed system is validated through simulations, demonstrating its capability to efficiently supply power to a brain implant. Simulation results indicate that, under constant input amplitude and frequency, the system achieves a peak efficiency of 83.55%, with the cross-coupled rectifier and the boost converter achieving efficiencies of 91.55% and 91.26%, respectively. Under varying load and input conditions, the proposed design can also consistently maintain high efficiency.

6.2 Contributions

The main contributions of this thesis are summarized as follows:

- Relevant overview of the state-of-the-art receiver circuits
- Investigation on the applicability of CMR in ultrasonic WPT
- Design of a high-efficiency receiver circuit with MPPT for ultrasonic WPT.
- Resolve the start-up issue using a maximum-voltage selector.
- PCB design of receiver circuit with MPPT implemented by STM32 development board.

6.3 Future Works

6.3.1 Voltage regulator integrated with MPPT

In the proposed design, the output doesn't have a regulation. However, the RX circuit is intended to power other implants, such as devices for recording nerve signals or transferring data from brain implants. Therefore, it requires a stable and specific supply voltage. While MPPT can provide maximum available power, this power may exceed the actual requirement. To address this, a comparator can be used to compare the output voltage with the rated voltage. When the two are equal, the MPPT algorithm freezes the duty cycle and is disabled, ensuring that the subsequent implants receive the rated voltage. If the output voltage exhibits significant ripple, an LDO can be implemented. However, since an LDO introduces a voltage drop, the comparison voltage should be set slightly higher than the rated voltage.

6.3.2 Debug PCB board and MPPT implemented by STM32

As mentioned in Chapter 5, the PCB has not yet been tested in the laboratory. In future work, both the PCB and the code programmed into the STM32 development board will need to be debugged and tested in combination, in order to verify the functionality of the complete system.

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