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MICROELECTRONICS

An Energy-Efficient and Robust Cryo-CMOS Smart Temperature Sensor

A Capacitively-Biased Diode-Based Cryo-CMOS Temperature Sensor with Hybrid Voltage-Time Domain Readout

By

Zenghui Li(5592425)

Supervisor: F. Sebastiano
Thesis committee: M. A. P. Pertijs
Department: Quantum and Computing Engineering
Faculty: Electrical Engineering, Mathematics and Computer Science

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Delft University of Technology

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Abstract

Quantum computers, mainly rely on quantum bits (qubits), which need to be operated at cryogenic temperatures. With the need for systems with thousands or even millions of qubits, the challenges of wiring and scalability become more apparent.

To address this, several studies focused on the idea of fully integrated cryogenic controller systems. It operates in close proximity to qubits in a deep cryogenic environment. In order to ensure operation over a specific temperature range, accurate temperature monitoring by temperature sensors (TS) is critical in this type of setup. Such sensors should operate efficiently at low temperatures and should operate over an extremely wide temperature range (from 4K to 300K) with high accuracy and energy efficiency. Current TS still faces performance challenges in such applications, especially in temperatures below 200K.

CMOS-based smart temperature sensors have the advantages including low cost, compact size, and ease of use. Among the various CMOS sensing elements, Capacitively Biased Diodes (CB-Ds) were chosen for this project. Therefore, in this project,a CB-D-based temperature sensor with a novel hybrid voltage-time domain readout in Intel 16nm FinFET technology is proposed with the capability of operating within a range from 4.2K to 300K.

Based on this topology, a further over-ranging technique is employed, thereby energy efficiency and accuracy are improved. From simulated data, with the supply $V_{DD} = 0.90V$, an accuracy of $+0.5/-0.3K$ with a conversion time of 44.1 μs is achieved. Furthermore, it consumes 21.9 μW, which has a competitive performance with room temperature prior art smart temperature sensors. Based on measurements, a customized smart temperature sensor can be designed. This will allow cryo-CMOS thermal monitoring system to be designed, which will provide an important milestone in the realization of scalable quantum computing.

Acknowledgements

First of all, I would like to thank my supervisor, Dr. Fabio Sebastiano, for providing me with this chance to work on this very challenging project. Special gratitude for the discussions, valuable comments, and encouragement over the past year. He taught me not only the basics of being a circuit designer but also the importance of looking at things critically. Next, I would like to thank my daily supervisor, Job, for all the support he has given me. I appreciate his kind greetings when he stops by the office each week, and I have thoroughly enjoyed our discussions, and also special thanks for his continued mental support when I have encountered various difficulties. Next, I would like to thank dr.ir. M.A.P. Pertijs for being on the committee for my thesis, and your outstanding achievements in smart temperature sensors have been a great influence and help for us to start our temperature sensor design. In addition, I would like to thank CoolGroup for all the help during the past year and the happy time we had.

Finally, I would like to thank my girlfriend and family for their love and support.

Contents

1. Introduction

This thesis presents the design of a specialized smart temperature sensor tailored for the thermal monitoring of cryogenic quantum computing applications.

In this chapter, we first give a brief overview of the motivation behind the cryo-smart temperature sensor design in the quantum integrated circuit (IC). This is followed by the design challenges that need to be met for cryogenic applications. Then, we compare the various sensing elements available in CMOS technology, leading us to our selection: on-chip diodes with a capacitively-biased principle. Finally, the organization of the rest thesis is introduced.

1.1 Motivation

Quantum computers hold the promise to address specific intractable problems —such as prime factorization, quantum simulations for drug and material synthesis, and intricate optimizations —which are unsolved even by today's largest supercomputers [1]. It has the potential to revolutionize computing by providing exponential speedups for technologically important problems.

The operation of quantum computers relies on processing the information stored in quantum bits (**qubits**) [2]. So far, there are already several physical implementations proposed for qubits, such as electron spins in quantum dots, superconducting circuits, and nitrogen vacancies in diamond lattices [3]–[9]. Regardless of such diversity, a shared requirement among the leading techniques is the need for cooling at tens of mK, for proper operation [10]. In its fundamental embodiment, the quantum processor consists of a set of qubits operating at ultra-low temperatures, while the classical electronic controller is used to read out and control the quantum processor

at **room temperature (RT)** [11], see Fig.1.1.

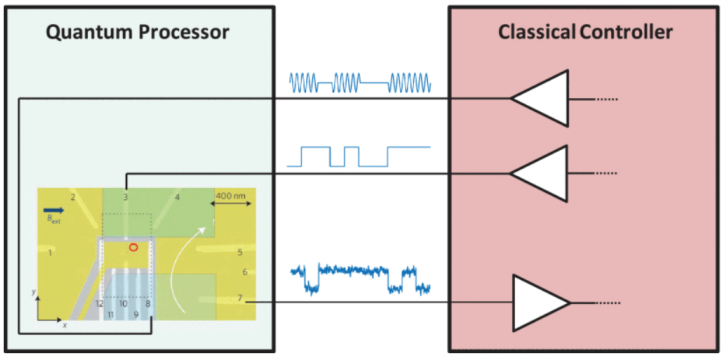

Figure 1.1: Quantum processor and the classical controller connected in a control/readout configuration [3]

While RT controllers have been effective for systems with fewer than 100 qubits [12], their architectural constraints limit the number of qubits they can manage efficiently. This is mostly due to wiring challenges [13]. As the need for qubits escalates into the thousands or millions, this approach becomes less feasible, more complex, and less cost-efficient [14], [15].

To support the scaling of qubit arrays, researchers have proposed and actively explored fully integrated cryogenic controller systems. It brings the functionality of the RT equipment into the deep-cryogenic environment, close to the qubits [16]. By co-integrating the controller system with advanced "hot" qubits operating on the same die or package, thus eliminating the wiring issue and offering a compact solution toward the realization of large-scale quantum computers [2]. In this context, the deep-cryogenic environment typically refers to temperatures ranging from 10 mK to 4.2 K, residing in dilution refrigerators.

Given that the systems will operate at temperatures close, ideally equal, to those of the qubits, one of the important challenges is the power dissipation of classical circuits. Dilution refrigerators offer limited cooling capacity at deep-cryogenic levels, such as 14 μW at 20mK in devices like the Bluefors XLD, severe power constraints are posed upon the cryogenic controller [17]. In other words, it has to be budgeted to be within the limits of thermal absorption by the refrigeration system used in the setup in order not

to destroy the qubit states by raising their temperature [12]. **Therefore, to ensure operation within a secure thermal range, precise monitoring of the temperature is crucial.**

Given this context, **Temperature Sensors (TS)** capable of operating efficiently in cryogenic conditions are essential. Furthermore, since the readout and control endpoints for the quantum processor are situated at room temperature, the sensor should have the flexibility to operate both at cryogenic levels (4K) and at room temperature (300K). In sum, it needs to work within an **ultra-wide temperature range** (4K to 300K) while maintaining **both high accuracy and high energy efficiency**.

1.2 Existing work of Smart TS at Cryogenic

From the most basic level, a temperature sensor is a device that produces a measurable output that varies based on temperature changes. To reduce the cost of both a temperature sensor and a computer interface, efforts were made to integrate the temperature sensor on the same chip as the **Analog-to-Digital converter (ADC)**, known as **Integrated Smart Temperature Sensors (ISTS)** [18], see Fig.1.2.

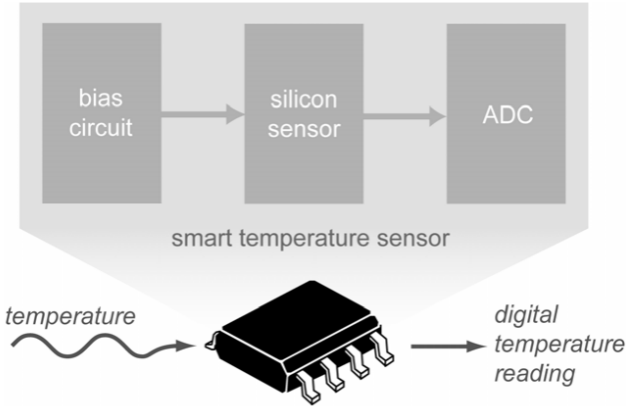

Figure 1.2: Block diagram of an integrated smart temperature sensor [19]

With the fast advancements in **CMOS** (complementary metal oxide semiconductor) and micro-fabrication technology, smart temperature sensors produced using standard CMOS technology have become popular in many application fields [19]. These sensors present benefits like low cost, small size,

and ease of use [20], which aligns with our design requirements. Besides, although several other technologies also show functionality at deep cryogenic temperatures, CMOS technology is the only one that can integrate billions of transistors on a single chip, while ensuring low-power consumption and sub-kelvin functionality [21].

So far, the existing CMOS-based smart temperature sensor can already monitor die or environment temperature over a temperature range from 200K to 300K [22]. In specific, it can achieve accuracy below 0.1 K, while keeping great efficiency in terms of cost, area and power consumption [19]. However, as of now, **there are no reports available for performance below 200K.** Here, one primary challenge is the measurement at cryogenic temperatures presents more complexities compared to room temperature measurements. Various experiment factors including the remote nature of the measurement system, difficult thermal problems of sensor mounting and heat sinking, etc. all contribute to these complexities. See Fig.1.3 as am example.

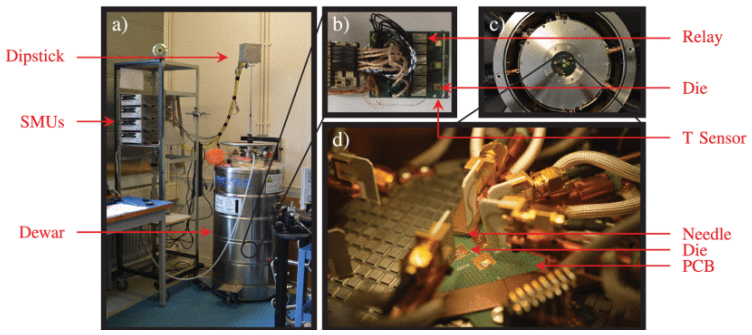

Figure 1.3: Example of measurement setup [23]

As the temperature decreases, the effort required to measure the temperature increases [24]. For instance, a task that might take minutes at room temperature could require months at 30 mK.

In summary, the CMOS-based smart temperature technique is the preferred choice for cryogenic temperature environments.

1.3 Design Challenges in CMOS-Based Smart TS

Implementing CMOS-Based Smart Temperature Sensors in cryogenic environments presents numerous challenges. Certain specific physical effects could cause some changes in the behaviour of devices at low temperatures, making the analogue circuit design a challenge in cryogenic environments. In specific,

- **Higher Threshold Voltage**
  The threshold voltage is expected to increase from 100mV to 200mV at 4K, which would lead to voltage headroom limitations [23]. Besides, designing a high-gain operational amplifier becomes challenging, which will make a high-accuracy sigma delta data converter less attractive.
- **Increased Mismatch**
  The Mismatch becomes larger in the cryogenic environment, see Fig.1.4.

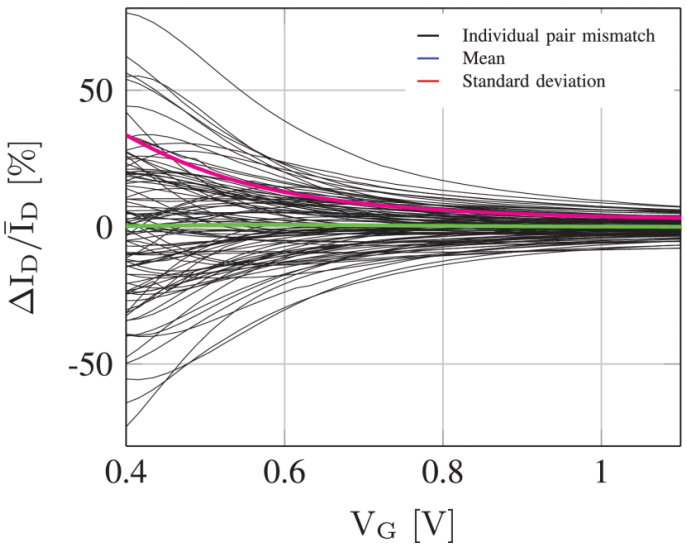

Figure 1.4: The drain-current mismatch of 99 NMOS device pairs [23]

Furthermore, compared with room temperature, the device will be working weak inversion more easily due to increased threshold voltage. This mismatch would degrade the performance of sensing elements, especially MOS-based diodes and related readout circuits di-

rectly. Details will be discussed in the following section.

Compared with analog/mixed-signal circuits, digital circuits are more robust in processing spread and environmental changes. However, its performance will also change significantly when extended to cryogenic temperatures, particularly in aspects such as speed and power consumption [25].

Moreover, a constrained power budget also needs to be considered due to the limited cooling power at cryogenic temperatures. Achieving energy efficiency for higher-performance design is always a challenge. Lastly, a significant challenge is the lack of available models and temperature-dependent measurement data. Smart temperature sensors with high performance are deeply dependent on accurate and reliable temperature-dependent models. When designing the specifications for readout circuitry, it's essential to have precise temperature models to take all possible non-ideal effects into account. Unfortunately, so far, there are no reliable models for cryogenic environments available. For this project, there is even no temperature-dependent measurement data for related intel 16nm FinFET sensing elements, making the project more complex and challenging.

1.4 CMOS Sensing Elements and Choice

So far, many studies has explored different sensing elements in CMOS technologies, such as bipolar junction transistors (BJTs), resistors, MOSFETs, diode, etc. It is the Temperature-based dependence of the sensing elements that enables temperature sensing.

In typical room temperature applications, the sensor front end of smart temperature sensors is wildly based on **Bipolar Junction Transistors (BJTs)**. However, Song et al. already demonstrated that the BJT does not operate properly at cryogenic, thus making a large number of existing sensor architectures unsuitable for cryogenic use [22].

Resistor-based temperature sensors are commonly implemented within RC networks [26], Wien-bridge [27], and Wheatstone-bridge. Previous stud-

ies have highlighted their superior resolution, but this usually comes at the cost of increased area and power consumption [28]. Besides, their reduced sensitivity at low temperatures prevents the full use of their capabilities.

The performance of sensors based on **thermal diffusivity** improves with advancements in technology scaling, as does the timing accuracy of their readout circuitry [29]. Yet, no design to date has shown a power consumption below 1.3 mW [30].

Compared with the diffusivity-based ones, **MOSFET-based** temperature sensors have the potential to keep a reasonable level of sensitivity without an extreme amount of power consumption [31]. However, even with multiple trimming points, they still struggle to achieve high resolution [32]. Additionally, they are affected by mismatch issues [33].

Traditional **Diodes** as well as **Metal-Oxide-Semiconductor (MOS)-based** Diodes use a current bias [34] for temperature sensing. J.Staveren et al. have already demonstrated an MOS-based Diode can enable reliable use over ultra-wide temperature ranges and maintain temperature linearity even at low temperatures [35]. However, their accuracy suffers in advanced CMOS technology nodes [36], for instance, FinFETs, which form the basis of this project. Therefore, **Capacitively Biased Diodes (CBDs)** were employed to enhance the performance of such sensors in advanced technology nodes [37], [38]. Its compatibility with digital designs aligns with the FinFET technology we employ [37]. More details analysis can be seen in the section.2.3.

Therefore, **we chose CBDs as the sensing elements in this project.**

1.5 Goal of this thesis

The goal of this project is to develop the first FinFET-based temperature sensor with an operating temperature range from 4.2K to 300K, using CB-D as the sensing element. Considering the self-heating limitations, we've set a power consumption threshold at 100 μW. The required accuracy is 1K, while the maximum conversion time is targeted at 100ms. See table.1.1 for the details.

Technology	Intel 16-nm FinFET
Nominal Supply Voltage	0.9V
Temperature Range	4.2 K - 300 K
Power	100 μW
Time per conversion	100 ms
+3 σ Accuracy	+1K

Table 1.1: Target specification

1.6 Thesis Organization

In the next chapter, CB-D-based sensor physics and its possible behavior at cryogenic with the various prior art readout architectures and their limitations at cryogenic are analyzed. To bridge the gap between the energy efficiency and ultra-wide temperature range target, a novel hybrid voltage-time domain readout architecture will be presented which results in low-power, digital friendly with a high robust readout. In Chap. 4, circuit realization of sensor prototype and its performance will be presented. Finally, the conclusion and future work of the thesis will be presented in Chap. 5

2. Capacitively-Biased-Diode-based Sensor and Readout Methods

This chapter discusses some general issues involved in the design of Capacitively-Biased-Diode(CB-D)-based temperature sensors. Firstly, the working principle of CB-D is described. This is followed by an overview of the prior art of CB-D-based temperature sensors. Next, two models are built up for understanding the physical behavior of CB-D at cryogenic. Finally, the limitations of prior-art architectures at cryogenic will be analyzed.

2.1 Operation Principle

First, we gave the operation principle of the CB-D, as shown in Fig. 2.1.

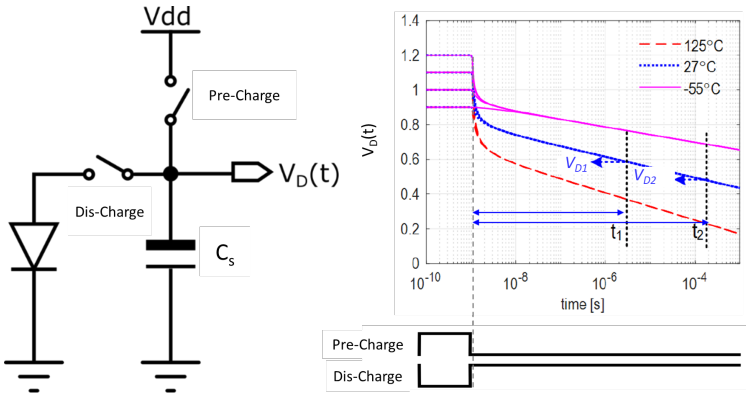

Figure 2.1: CB-D Operation Principle [39]

As we can see, the operation can be divided into 2 phases: Pre-charge and dis-charge. At the pre-charge phase, the capacitor is first charged to the supply voltage. After that, the capacitor is discharged through a diode.

If neglecting the series resistance of the diode at this point, combining the differential eq. 2.1 and standard $I - V$ characteristics of diode Eq. 2.2:

$$\frac{dQ}{dt} = C_s \frac{dV_D}{dt} \tag{2.1}$$

$$I = I_0 \left(\exp\left(\frac{qV_D}{nkT} \right) - 1 \right) \tag{2.2}$$

Here, k is the Boltzmann constant, q is the elementary charge, n is the non-ideal factor, and T is the temperature. nkT/q can be simplified as thermal voltage: V_T. I_0 is the reverse saturation current.

Then, the final differential equation can be obtained as:

$$-C_s \frac{dV_D}{dt} = I_0 \left(\exp\left(\frac{V_D}{V_T} \right) - 1 \right) \tag{2.3}$$

The differential equation describing the discharge process resolves to the term:

$$V_D(t) = -V_T \cdot \ln \left[1 - \left(1 - \exp \frac{-V_{DD}}{V_T} \right) \cdot \exp \frac{-I_0 \cdot t}{C_S \cdot V_T} \right] \tag{2.4}$$

Then three regions can be distinguished identified [40]:

1. **Fast Decay Region**($\sim$tens of nanoseconds)
   The decay voltage depends largely on the initial voltage (V_{DD}).
2. **Temp-dependent Decay Region**
   After the **Fast Decay** region, satisfying $t \cdot I_0 / (nV_T C) \gg \exp[-V_i / (nV_T)]$, the residual voltage V_D on the storage capacitor will be mainly decided by the $I - V$ characteristic and shows a supply-independent log relation of time. In this case, Eq. 2.4 can be simplified to:

$$V_D(t) = V_T \cdot \ln\left(\frac{C_s \cdot V_T}{I_0 \cdot t}\right) \tag{2.5}$$

3. **Dead Region** After a little time (the exact time is decided by the size of the diode and the capacitor, typically $\sim 10ms$), the voltage decay is no longer logarithmic, which also means there is little current($\sim pA$) left in the diode, and also impacted by leakage effects, while the voltage approaches 0 V.

Actually, With Eq. 2.5, we can also generate **CTAT** and **PTAT** voltage, as shown in Fig.2.3.

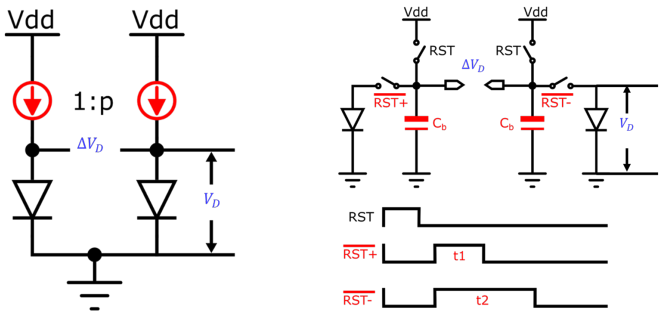

Figure 2.2: CS-D(left) v.s. CB-D(right)

It is similar to traditional Current-Source-biased-Diode(CS-D), see Fig.2.2.

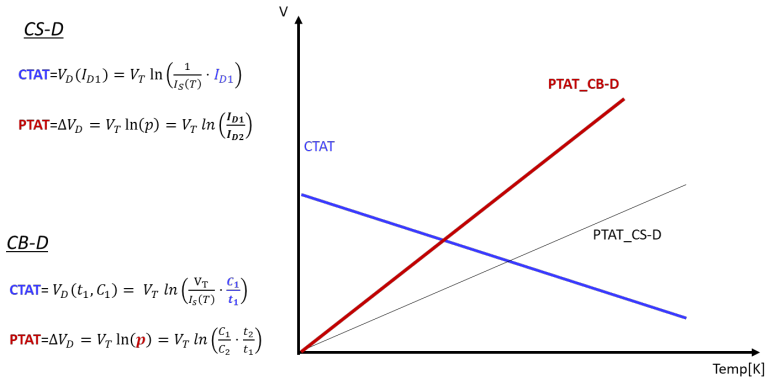

Figure 2.3: CTAT and PTAT Generator from CS-D and CB-D

The way of generating CTAT and PTAT are as follows:

- **CTAT Generator**: When biasing diode in the temp-dependent region, if fixing the discharging time $t = t_0$ in Eq.2.5, the resulting voltage $V_D(t_0) = V_T \cdot \ln\left(\frac{C_s \cdot V_T}{I_0 \cdot t_0}\right)$ will be CTAT.
- **PTAT Generator**: A PTAT voltage can then be generated by substracting the output of two CTAT($V_D(t_0) - V_D(t_1) = V_T \cdot \ln(t_1/t_0)$) with a fixed decay time ratio(t_1/t_0).

In this sense, the physical nature of CS-D and CB-D is the same. In traditional CS-D, the diode is biased by a fixed current, in which the current densities usually can be adjusted by current mirror ratios and diode areas. CB-D utilizes a capacitor with a fixed decaying time, which also provides the bias current. Besides, some unique benefits of the CB-D scheme also become obvious: the original CS-D scheme requirement for analog components, such as resistors, amplifiers, and current mirrors, can be waived.

Traditionally, the mismatch of the current mirrors and diodes/BJTs is usually the main error source of CS-D for temperature-dependent voltage generation. Meanwhile, transistor mismatch drastically increases at cryogenic temperature, which means a large error due to mismatch is expected in those current mirrors. However, digital is more robust to process spread and environmental changes. This robustness is verified to be extended to cryogenic temperatures [12], which provides an obvious benefit.

Last but not least, precise pulse timings can be more easily controlled in cutting-edge technology nodes (like FinFET technology), which makes CB-D more suitable for advanced technology nodes.

2.2 Prior Art of CB-D based temperature sensor

In the last section, the operation principle of the CB-D-based temperature sensor is well-explained. Several CB-D-based smart temperature sensors at room temperature(from 218.15K to 398.15K) range have been widely reported.

In [39] shown as Fig.2.4, the CB-D front end is directly combined with $\Sigma - \Delta$ADC.

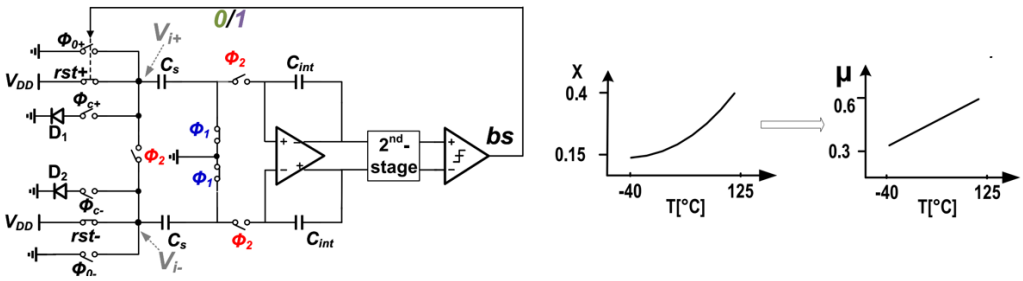

Figure 2.4: CB-D with $\Sigma - \Delta$ readout (left) and Temperature Sensing Principle(right)

Based on the description in the previous section, PTAT voltage, and CTAT voltage can be sampled separately by utilizing two different CB-D sensor cores and different discharging times. If the PTAT=ΔV_D voltage is treated as the input temperature sensing signal and the CTAT=V_D as the reference, based on the ratio measurement. X=$\Delta V_D / V_D$ can be digitally read out by the ADC.

This topology is improved in [41], the resolution FOM 0.34pJ $\cdot$ K^2 of this topology is achieved, which is one of the best reported at room temperature.

In [38], a novel time-domain readout for CB-D based temperature sensor is proposed, see Fig.2.5.

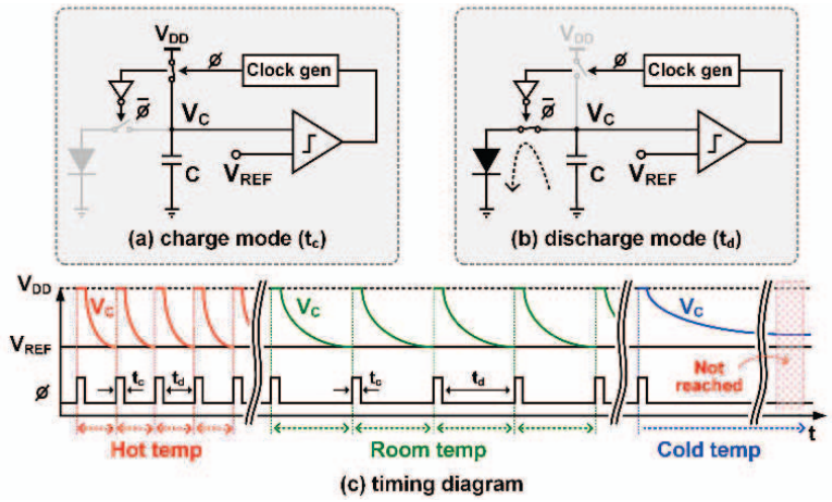

Figure 2.5: time domain readout with a temperature-independent V_{ref}[image reproduced from [38]

The working principle of this topology is that after pre-charging the capacitor to supply, the diode starts to discharge. The function of the compara-

tor is to detect when the decay voltage reaches a reference voltage(typically implemented by a BJT-based temperature-independent Voltage), which will toggle the states of the control logic.

However, the temperature readout range of this topology is limited. Since at low temperatures (even just below 283K at room temperature), V_C decaying speed is very slow and hard to reach V_{REF}. This problem is solved by replacing V_{REF} as a V_{CTAT}, see Fig.2.6.

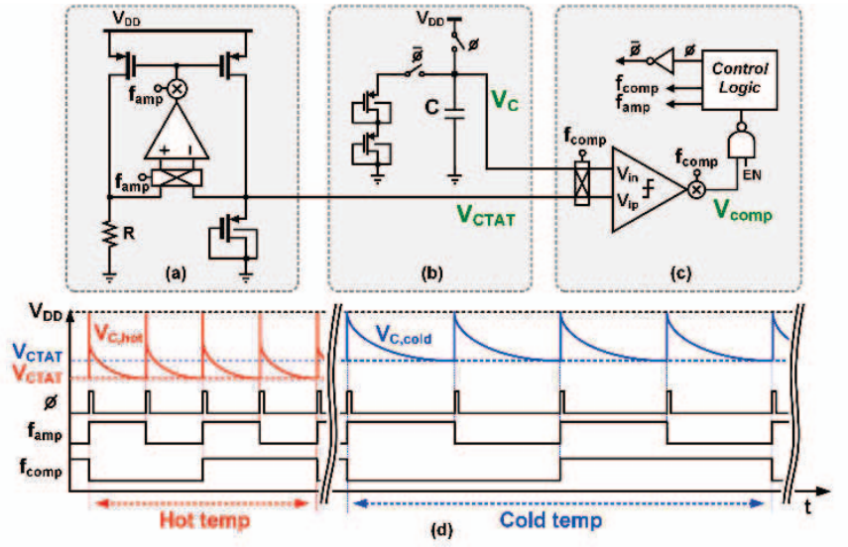

Figure 2.6: CTAT as V_{ref} scheme[impage reproduced from [38]]

An intel 16nm-FinFet process technology-based topology [42] is also reported, shown as 2.7. Here, CB-D is embedded with SAR-ADC, and a compact area is achieved.

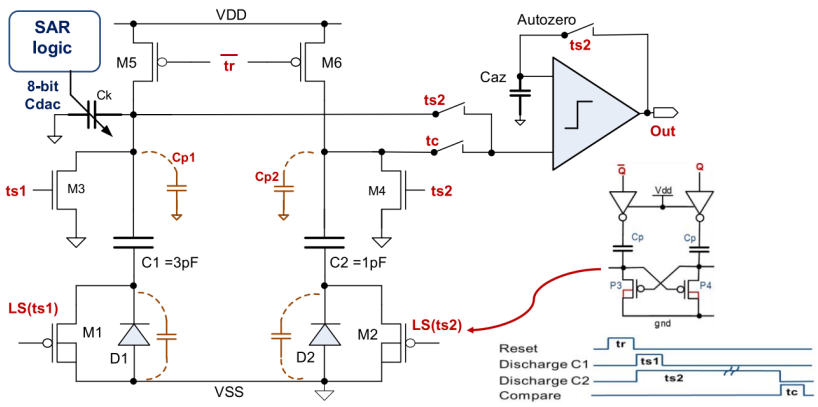

Figure 2.7: CB-D with SAR propotype

From the Tab. 2.1, we can find that time-domain readout is an energy-efficient(high Res FOM), a high accuracy(1k), and digital-friendly readout topology which is also suitable for advanced technology nodes(28nm CMOS).

	ISSCC'23	SSCL'21	SSCL'19	CICC'20
Technology	180nm	55nm	16nm	28nm
Type	PNP DT ΣΔ	PNP DT ΣΔ	Bulk Diode SAR	DTMOST OSC
Area $[mm^2]$	0.25	0.021	0.0025	0.017
Supply [V]	0.95-1.4	1-1.3	0.85-1	0.85-1.15
T. Range [°C]	-55 to 125	-55 to 125	-15 to 105	-10 to 90
3σ error [°C] (Trim point)	$\pm 0.45(0)$ $\pm 0.15(1)$	$\pm 1.4(0)$ $\pm 0.6(1)$	+1.5/-2.0 (0)	$\pm 2.0(0)$ $\pm 0.9(1)$
R.IA[%] (Trim point)	$0.5(0)$ $0.17(1)$	$1.6(0)$ $0.67(1)$	2.9(0)	$4(0)$ $1.8(1)$
Power [uW]	0.81	2.2	18	33.75
Tconv[ms]	128	6.4	0.013	0.1
Res. [mK]	1.8	15	300	10.2
Res. FoM* $[pJ \cdot K^2]$	0.34	3.1	21	0.36

Table 2.1: Prior-Art BenchMark [Table reproduced from [41]]

Before considering the application of these state-of-the-art readout architectures to cryogenic, we need to first have a reasonable prediction of the CB-D behavior at cryogenic. This will allow for a more quantitatively clear understanding of the read accuracy and requirements of the ADC. In the next section, the behavior of CB-D at cryogenic is discussed and analyzed.

2.3 CB-D at Cryogenic

This section investigates and predicts the possible physical behavior at cryogenic. With this aim, two different approaches are adopted for the prediction function.

2.3.1 Analysis of CB-D at Cryogenic

Although we do not have measured the CB-D behaviour and related dataset, due to the same physical essence as CS-D, CB-D is supposed to work at cryogenic. Fig.2.8 shows the I-V curves of TSMC 40-nm CMOS P+/Nwell Diode are measured as a function of temperature from 4K to 220K for self-heating measurement [43].

As aforementioned, during the second region of CB-D decay, voltage is fully decided by the I-V characteristics of the diode. From this perspective,

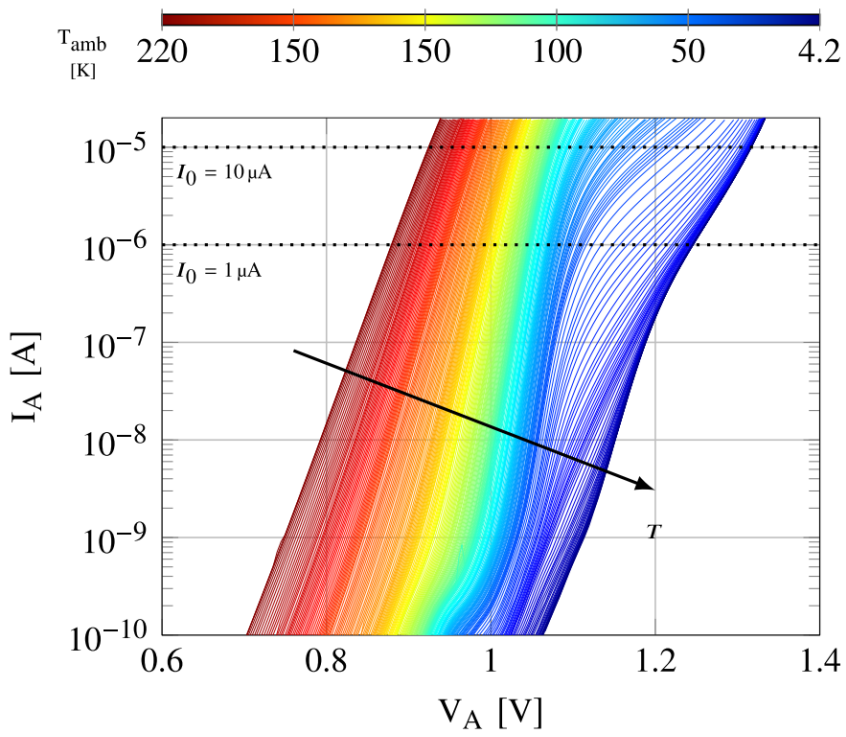

Figure 2.8: I-V curves of diode at ambient temperature ranging from 220K to 4.2K, image reproduced from [43]

based on the existing measurement dataset, we could build up a CB-D emulation model to predict the operating condition of CB-D at cryo to assist our design. Based on this, two different emulation models are built up, as will be explained in the following: an analytical model and a numerical model.

2.3.2 Analytical Model

In this section, an analytical CB-D emulation model is built up. The main idea is to fit the measured data with the standard I-V curve of the diode. Then, the physical parameters required by CB-D model can be obtained. With those parameters, CB-D behavior model can be reconstructed.

Since the minimum measured voltage $V_D = 0.69V >> n \cdot V_T$, the $I - V$ standard Eq. 2.2 can be simplified as:

$$I_D = I_0 \exp\left(\frac{qV_D}{nkT}\right) \tag{2.6}$$

The formula can be further modelled as:

$$V_D = a \cdot \log I_D + b \tag{2.7}$$

where,

$$\begin{cases} a = nkT/q, \\ b = f(a, I_0) \end{cases} \tag{2.8}$$

Here, f is the fitting function. Based on measured data I_D, V_D and corresponding temperature T, the required parameters I_0 and n can be obtained. Especially in the region of low current level(<10nA), n is well-fitted in n from I-V curve.

Then feed the calculated parameters into Eq. 2.4, the analytical CB-D can be obtained as Fig.2.9.

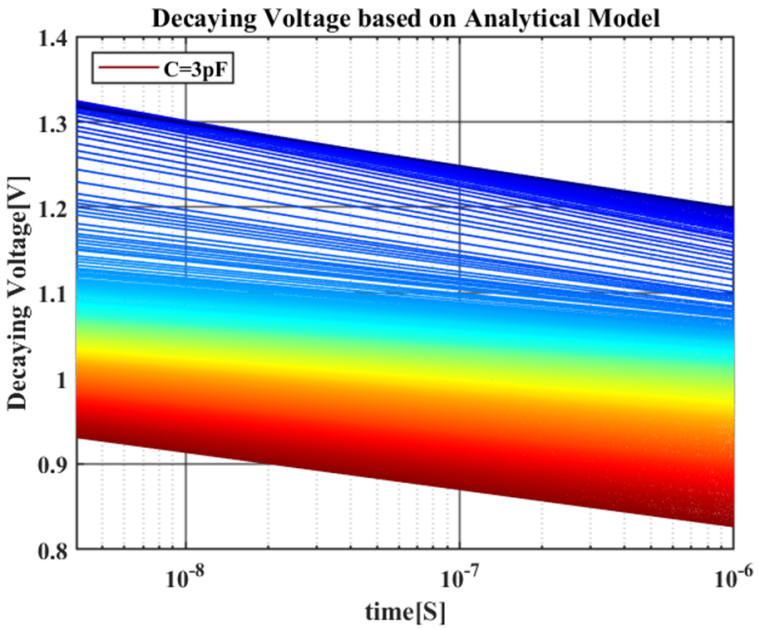

Figure 2.9: CB-D Analytical Behaviour Model at Cryo

2.3.3 Nurmercial Model built-up model

Another approach is more intuitive. We can build up a differential equation numerical model to model the CB-D behavior directly based on existing $I-V$ data.

The basic process is shown as follows:

1. Build look-up table of I-V curve of diode at different temperatures;
2. Model the differential equation:

$$\Delta V_D = -(I_D(V_D(t_i))/C_S \cdot \Delta t) \tag{2.9}$$

where

$$\begin{cases} \Delta V_D = V_D(t_i) - V_D(t_{i+1}), \\ \Delta t = t_{i+1} - t_i \end{cases} \tag{2.10}$$

With MATLAB modelling and simulation, the numerical CB_D model result is shown as Fig 2.10.

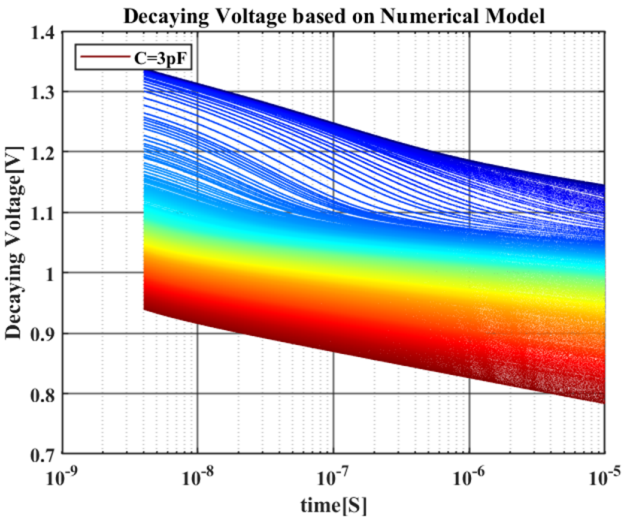

Figure 2.10: CB-D Numerical Model at Cryo

If biasing diode with a fixed time, the voltage across the diode is in-

trinsically a CTAT voltage shown as in Fig.2.11. If biasing diode with two different time interleaves t0 and t1 with the same diode and biasing capacitor size, a PTAT voltage is also generated. From here we could predict, the temperature dependence mechanism of CB-D is similar to traditional CS-D, which means it can also generate PTAT and CTAT voltage accordingly.

CTAT and PTAT from the CB-D data are shown as Fig.2.11 and Fig.2.12

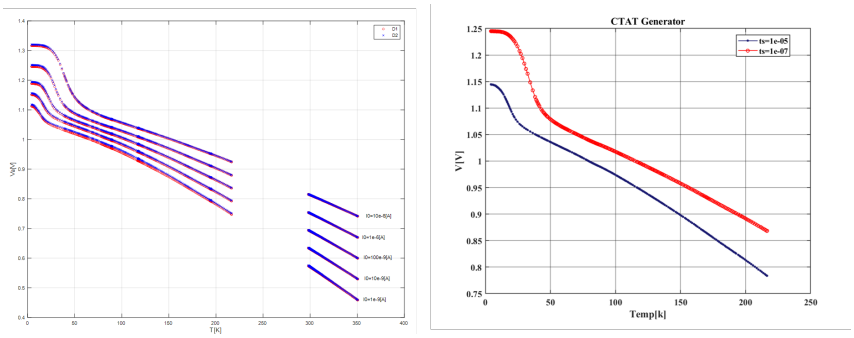

Figure 2.11: CTAT from CS-D at cryo(left) and CB-D at cryo(right)

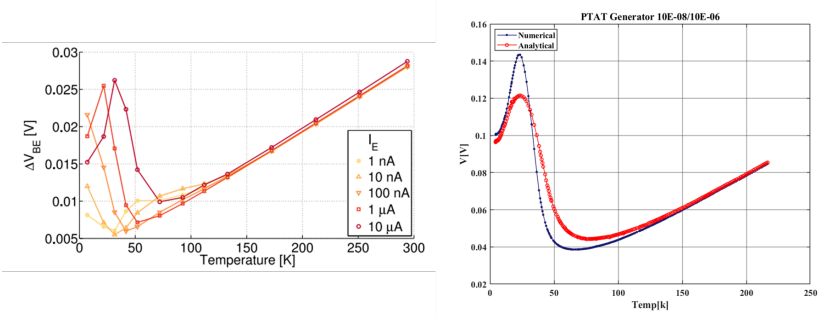

Figure 2.12: PTAT from current-source-biased BJT at cryogenic(left)(image reproduced from [44]) and CB-D at cryogenic(right)

From PTAT, we realized that CB-D may only work until $\tilde{5}$0K, the reason for which is similar to CS-D from [44].

Therefore, we may conclude that PN junction and BJT-based CB-D may not work properly–non-linear effects are accentuated, especially for PTAT voltage, even if not monotonic.

For predicting CB-D behavior at cryogenic, we find numerical is more useful as the non-ideal physical effect can also be reflected at a high current level.

2.3.4 MOS-based Diode model

Based on the conclusion of [45], the performance of MOS-based CS-D is better. It can provide more linear PTAT and CTAT voltage at cryogenic. As we do not have characterization data of intel-16nm transistor behavior so far at cryogenic, the approach we choose is to analyze the CB-D behavior based on the I-V transfer function and predict its feasibility.

For a diode-connected MOS, the current vs. voltage across MOS can be expressed as follows [45]:

$$\begin{aligned} I_D &= \mu C_{ox}(n-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \\ &= I_{Specs}\exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \end{aligned} \tag{2.11}$$

where W and L indicate the size of the transistors, μ is the mobility, C_{ox} indicates the oxide capacitance, n represents the non-ideal factor, V_T is the thermal voltage, and V_{Th} is the threshold voltage.

Associating this equation with Eq 2.1, we can derive a similar solution:

$$V_D = V_{th} + nV_T \ln\left(\frac{C \cdot V_T \cdot n}{t \cdot I_{\text{Specs}}}\right) \tag{2.12}$$

Different with P-N junction diode, $n \cdot V_T$ still shows PTAT relation until 4K, the CTAT of which is also decided by the V_{TH} similar to the traditional MOS-based CS-D. Although there is also temperature dependency on I_{specs}, its effect on the full equation is reduced by the log relation.

Since CB-D and CS-D have similar physical mechanisms, and MOS-based CS-D can exhibit a PTAT voltage with better linearity at cryogenic, we could predict that CB-D can also work properly at cryogenic as a promising candidate sensing element.

2.4 Limitation of Prior-Art at Cryogenic

In this section, the limitation of the Prior-Art readout at cryogenic will be described. First, the readout resolution is estimated by extrapolating the CTAT voltage linearly with the corresponding temperature transfer function. Based on this, the limitations will be analyzed.

2.4.1 Resolution Estimation at Cryogenic

In this section, We will first reconstruct the temperature principle of voltage-domain and time-domain Prior-Art Readout Architecture. Since there is no characterization data of used technology for cryogenic, we can only take the voltage data in the room temperature range and perform a linear extrapolation of it to cryogenic. After obtaining PTAT and CTAT, we construct the corresponding temperature sensing transfer function of Prior-Art, and based on this, we make a reasonable prediction of its expected resolution requirement at cryogenic.

Based on the sizing choice of [42], two CB-D (DTMOS) cores are reconstructed, with properly designed size W/L= $3.6\mu/0.45\mu$, time ratio t1=50ns and t2=1.45μs and capacitor ratio = 3. We can get the temperature-dependent voltage CTAT and PTAT with the voltage extrapolated to cryogenic as shown in Fig.2.13.

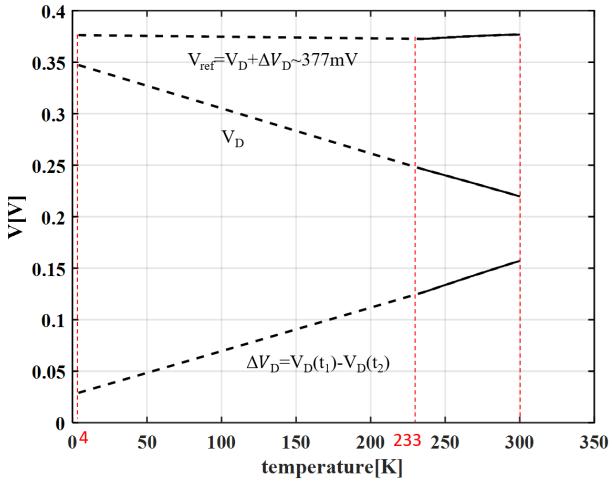

Figure 2.13: Temperature Dependent Voltage

For this temperature transfer function, deriving the resolution requirement on the X in paper [39], the minimum detectable step ΔX can be found as:

$$\Delta D_{out} = \Delta X \cdot \frac{\partial D_{out}}{\partial X} \Rightarrow \Delta X = \frac{\Delta D_{out}}{\left|\frac{\partial D_{out}}{\partial X}\right|} \tag{2.13}$$

Then the ADC's resolution can be calculated as follows:

$$\text{ENOB} \approx \log_2\left(\frac{X_{\text{FS}}}{\Delta X}\right) - 1 \tag{2.14}$$

For the target sensor in-accuracy 1K, the resolution should be at least x10 higher [46]. which means at least $\pm 0.1K$. The ADC's required resolution as a function of temperature is shown in Fig. 2.14.

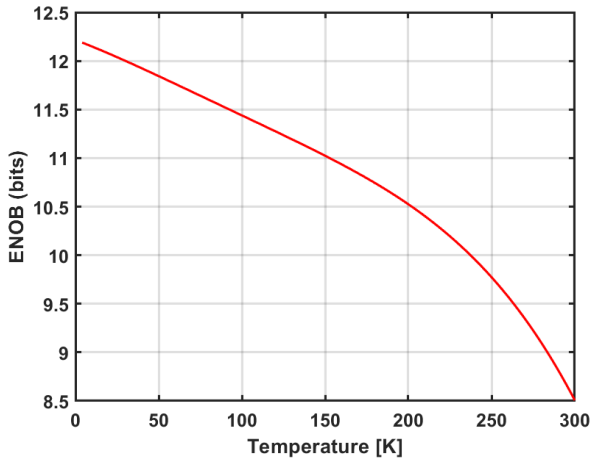

Figure 2.14: Voltage Domain Readout Resolution

From Fig 2.14, we can conclude that the voltage domain resolution at cryogenic should be designed at least for 12.5bits.

The derivation of the resolution requirement for the time domain in [47] is more tricky. We need to perform further analysis of the relationship in the time domain to obtain the temperature transfer function.

To revisit the time domain readout, the schematic is shown as Fig. 2.15.

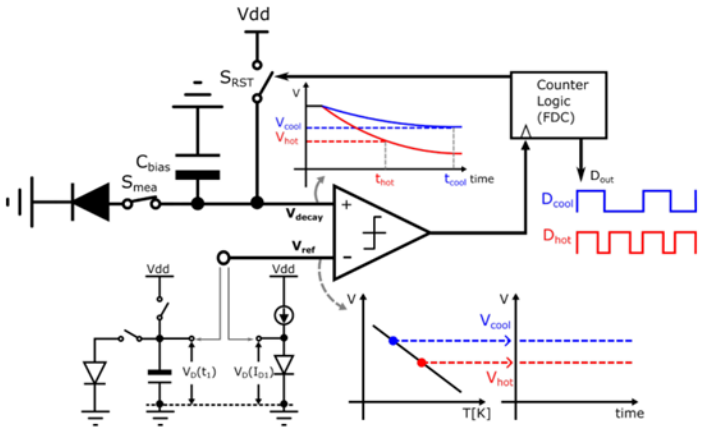

Figure 2.15: CB-D with Time Domain Readout

Essentially, the time starting to decay is like a start signal, the time when decay voltage crosses with V_{ref} is a stop signal, with both, the decay time t_d can be measured.

The discharge time t_d is temperature-dependent, which follows:

$$\begin{aligned} V_D(t_d) &= V_{ref} \\ t_d &\propto C \cdot V_T \cdot \exp(-\frac{V_{ref}}{V_T}) \end{aligned} \tag{2.15}$$

To mitigate the limited temperature readout range, a CTAT as the reference for the comparator V_{ref} is proposed [47], which makes the decay time the following:

$$\mathrm{t_d} \propto C \cdot V_T \cdot \exp\left(-\frac{V_{CTAT}}{V_T}\right) \tag{2.16}$$

For the CTAT generator, there are two ways to implement: the first is to use traditional CS-D like [47], and the other way is to use another CB-D sensor with a fixed biasing time as physical essence that is the same as traditional CS-D.

From the aforementioned operating principle, when the decay voltage $V_D(t)$ cross the reference voltage V_{CTAT}, which means that such equation is met with:

$$V_D\left(t_{mea}\right) = V_{CTAT} = \beta \cdot V_D\left(t_1\right) \tag{2.17}$$

where, β could be regarded as a scaling factor(β here is temperature-independent), which means that the temperature information is generated from the diode with different current densities.

The necessary condition to achieve time-domain readout is $\beta < 1$, in such case, Eq.2.17 can be reformed as:

$$\begin{aligned} V_D\left(t_1\right) - V_D\left(t_{mea}\right) &= (1-\beta)V_D\left(t_1\right) \\ V_T \log\left(\frac{t_{mea}}{t_1}\right) &= (1-\beta)V_D\left(t_1\right) \\ \mu = \frac{t_{mea}}{t_1} = \exp\left(\frac{(1-\beta)V_D\left(t_1\right)}{V_T}\right) &\propto \exp\left(\frac{1}{T}\right) \end{aligned} \tag{2.18}$$

The corresponding voltage relation between decay voltage at t_1: $V_D(t_1)$ and readout time t_{mea} is shown in Fig2.16.

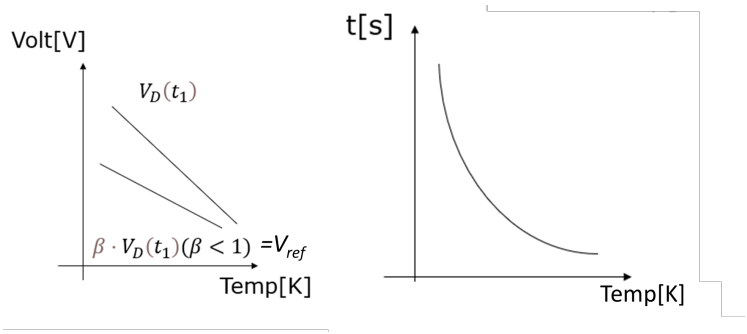

Figure 2.16: (left)Voltage relation between reference voltage and decay voltage at t_1;(right) readout time t_{mea} v.s. temperature

For the CTAT generator, there are two ways to implement: the first is

to use traditional CS-D like [47], and the other way is to use another CB-D sensor with a fixed biasing time as physical essence that is the same as traditional CS-D.

β can be easily generated by using either an individual CTAT generator as[47] or by charge-sharing with an extra reset capacitor after decaying with a fixed time t_1 where $\beta = \frac{C_1}{C_1+C_2}$, the working principle of this scheme is shown as Fig. 2.17.

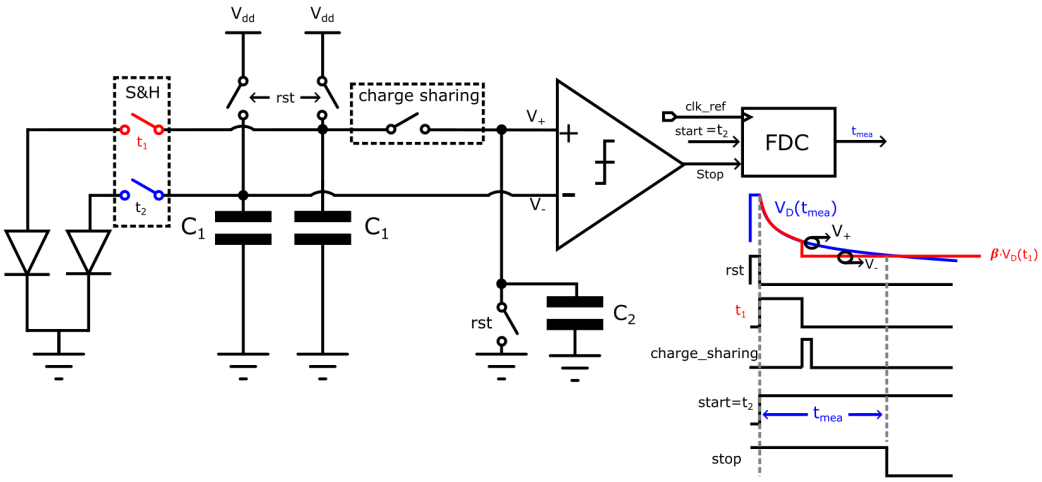

Figure 2.17: Time domain readout with a charge-sharing scheme

By adjusting different β, the possible simulation result based on intel-diode is obtained shown in Fig.2.18.

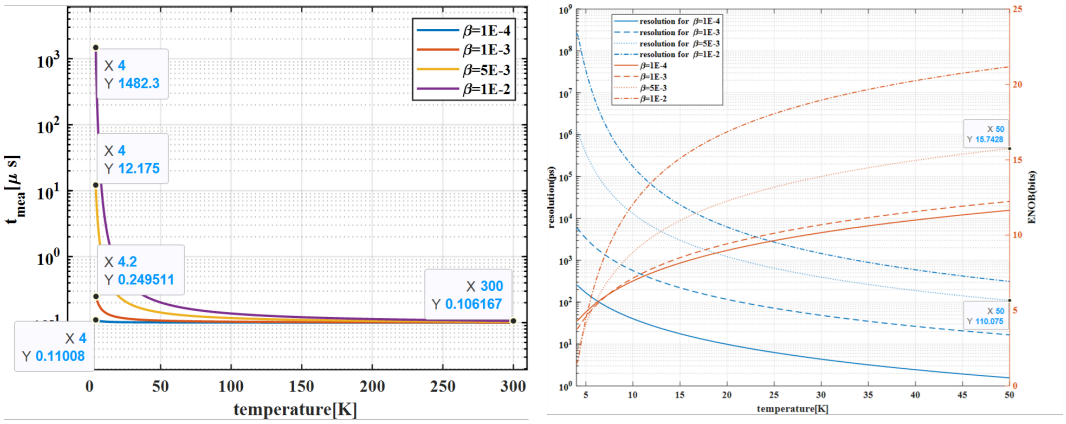

Figure 2.18: (left) Possible Readout Time vs Temperature;(Right) Possible Readout Resolution Requirement vs Temperature

Due to the exponential function, the readout time rises exponentially at deep cryogenic temperatures, and in order to read out such times, the cor-

responding time-to-digital converters that can achieve a 0.1K readout resolution required are shown in Tab.2.2.

	t_{max}	t_{range}	Resolution ((Δt[ps]))	#bits
$\beta' = 1E-4$	110ns	10.2ns	0.04	16
$\beta' = 1E-3$	261ns	160ns	0.4	17
$\beta' = 5E-3$	12.17us	12us	2.21	21
$\beta' = 1E-2$	1.48ms	1.48ms	4.5	27

Table 2.2: Possible Time-Domain Readout Resolution Requirement for 4K to 300K Temperature Range

Here, t_{max} is the maximum time supposed to be read at cryogenic, t_{range} is the range of readout time, resolution and bits indicate that resolution requirement.

This type of resolution in p̃s level and up to more than 15 bits time-to-digital converters is usually the application of frequency synthesis. The power consumption is usually up to m̃W, which is unacceptable at cryo because of the effect of self-heating, if the power reaches 100 μW, it will generate a temperature rise of nearly 50K.

2.4.2 Limitation at Cryogenic

In this section, the limitation of time domain and voltage domain readout at cryogenic is discussed.

For voltage domain readout, to achieve 13 bits, $\Sigma - \Delta$ ADC is usually used. However, due to at cryogenic, threshold voltage being higher, DC gain of the integrator in the $\Sigma\Delta$ modulator may be reduced, which will cause the charge to leak away which makes $\Sigma\Delta$ ADC not attractive at cryogenic.

For time domain readout, it is usually suitable for small range readout. The time provided is also an exponentially sensitive CTAT time. At cryogenic, the time is increasing with an exponential speed, which causes hard-achieved circuit requirement.

3. Energy-Efficient and Robust CB-D Readout

In this chapter, an energy-efficient voltage domain–SAR-based–readout and its design gap are analyzed detailedly, this is followed by the proposed hybrid voltage-time domain readout topology. Then, behavior model built-up and system-level considerations are discussed.

3.1 Energy Efficient Voltage Domain Readout

For energy-efficient purposes, in voltage domain readout, there is also an alternative to the aforementioned ΣΔ-ADC, which is SAR-ADC. The operating principle of this type of ADC is to employ a successive approximation algorithm in a feedback loop with a 1-bit quantizer. Besides, the simplicity of the hardware implementation of the SAR-ADC and its capacity for low-power with a digital-friendly property is also attractive for our target application field.

In the traditional charge-redistribution SAR ADC(shown in Fig.3.1), a temperature-independent reference voltage is necessarily required.

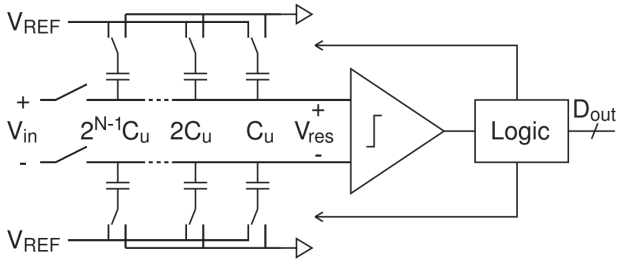

Figure 3.1: Charge-Redistribution SAR ADC Architecture (Image reproduced from [48].)

With a CB-D based sensor core, since the temperature-dependent voltage is already stored in the biasing capacitor before A/D conversion, one of the

input voltages could be served as V_{ref} and an extra step to generate V_{ref} is not required anymore.

Fig. 3.2 shows the working principle of the CB-D-based sensor with a charge-sharing-based SAR readout.

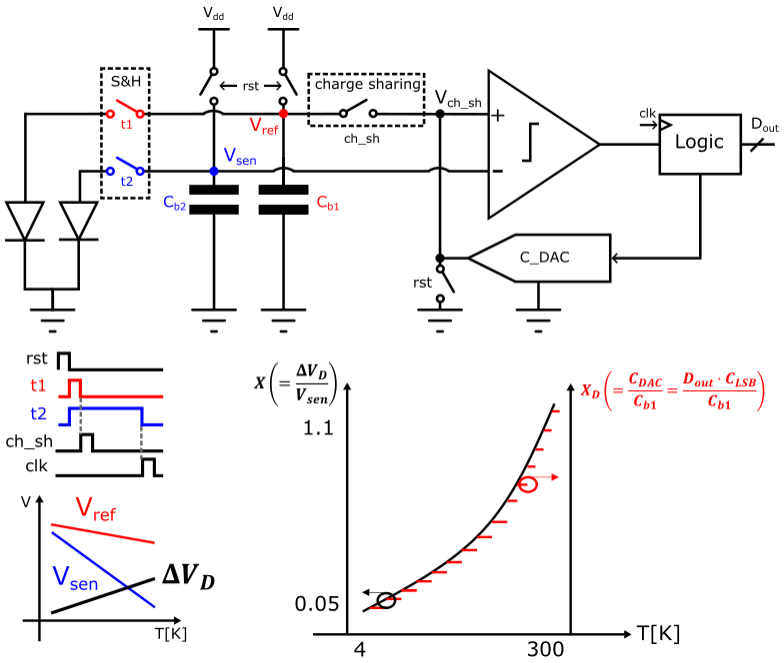

Figure 3.2: Working Principle of CB-D based Sensor with Charge-Sharing-based SAR Readout

By using two CB-D sensor cores with different discharging time t_1 and t_2, CTAT voltage $V_D(t_1)$ and $V_D(t_2)$ can be generated(here $t_2 > t_1$). Where a relative insensitive voltage $V_D(t_1)$ can serve as the reference voltage V_{ref}, while the low-bias sensitive voltage $V_D(t_2)$ can serve as targeting required readout voltage V_{sen}. This is followed by a charge-sharing operation(ch-sh), where the generated V_{ref} is charge-shared with C_{DAC}. During the rest phase, the top plate of C_{DAC} is discharged to 0V. After charge sharing, the input of the comparator yields:

$$V_{ch-sh} = \frac{C_{b1}}{C_{b1} + C_{DAC}} \cdot V_{ref} \tag{3.1}$$

Finally, C_{DAC} is updated by SAR logic. Therefore, temperature readout is

performed actually by comparing V_{sen} with V_{ref}, which is scaled by charge-sharing:

$$V_{sen} = \frac{C_{b1}}{C_{b1} + C_{DAC}} \cdot V_{ref} \tag{3.2}$$

$$\Delta V_D = V_{ref} - Vsen \tag{3.3}$$

Let us consider eq 3.3 and reformulate eq 3.2 as follows:

$$X \left(= \frac{C_{DAC}}{C_{b1}} = \frac{D_{\text{out}} \cdot C_{LSB}}{C_{b1}} \right) = \frac{\Delta V_D}{V_{sen}} \tag{3.4}$$

Although the ratio $X = \Delta V_D / V_{sens}$ is a nonlinear function of temperature, it can be post-linearized in the digital domain and converted to digital output of temperature with eq.3.5.

$$\begin{aligned} \mu &= \frac{\alpha \Delta V_D}{\alpha \Delta V_D + V_{sen}} = \frac{\alpha \cdot X}{\alpha \cdot X + 1} \\ D_{out} &= A \cdot \mu + B \end{aligned} \tag{3.5}$$

See Fig.3.3 as a showcase of Eq. 3.5.

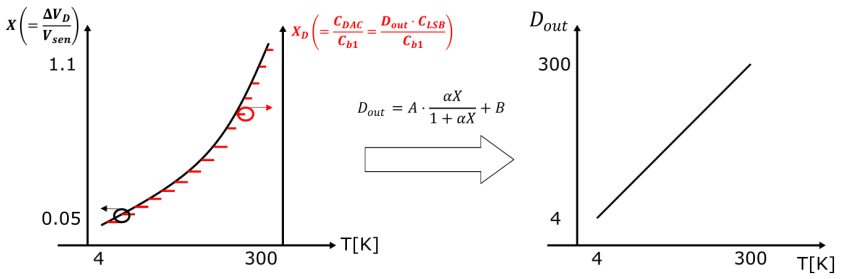

Figure 3.3: Nonlinear X with the linerization

Another point of view is illustrated in Fig. 3.4, where ΔV_D serves as a reference voltage level, and the crossing point defines the temperature to be measured (147K).

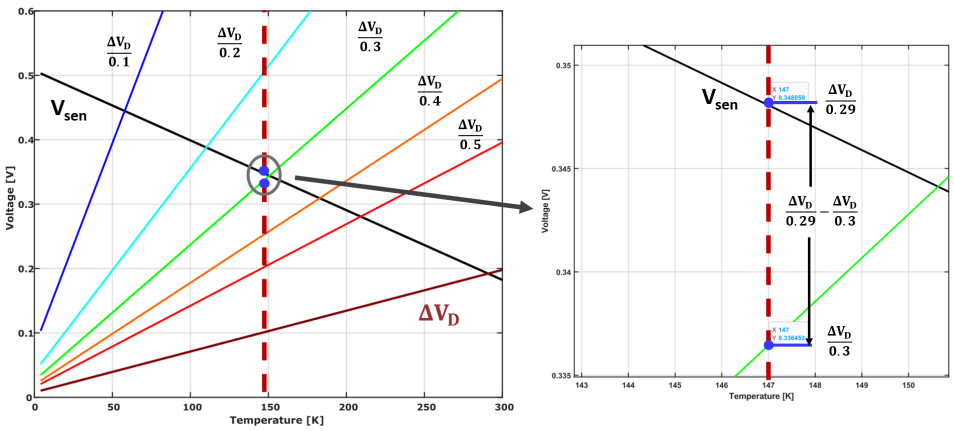

Figure 3.4: Temperature dependence of V_{sen} and take $\Delta V_D / X_D$ as a reference voltage level

The distance between $\Delta V_D/0.29$ and $\Delta V_D/0.30$ can be regarded as the limited readout resolution loss.

For this temperature transfer function, deriving the resolution requirement on the SAR-ADC requires an analysis of the ratio X. For the target sensor in-accuracy 1K, the resolution should be at least x10 higher [46], which means at least $\pm 0.1K$. The required resolution of ADC as a function of temperature is shown in Fig. 3.5.

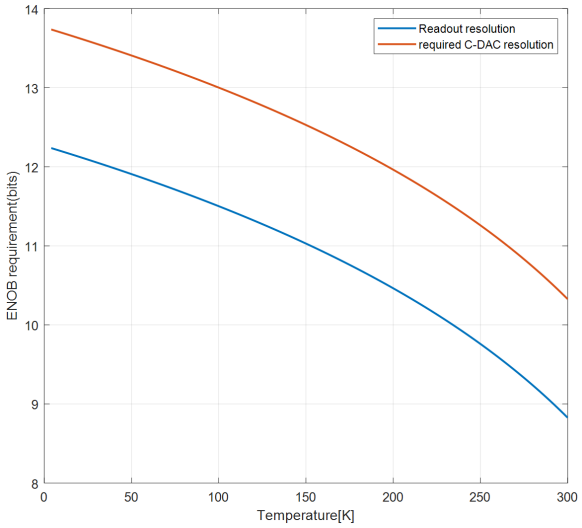

Figure 3.5: SAR ADC's resolution reuqirment

As shown, due to PTAT temperature-dependent property, the sensitivity of X is relatively poorer at cryo. Also due to PTAT insensitivity characteristics at cryo Fig.3.3, the readout resolution for the target accuracy budget requirement is even higher. Since the resolution of SAR-ADCs really depends on component matching, which means that extensive calibration is needed to achieve the ENOB of 15bits by target application field, this defeats the purpose of low cost. To sum up, the design of an energy-efficient, robust, high-resolution CB-D-based smart temperature sensor in a digital manner calls for architecture-level solutions.

3.2 Proposed Hybrid Voltage-Time Domain Readout Topology

As aforementioned in Chapter 2, time domain readout due to its intrinsic exponential relation is more sensitive to temperature range, in other way saying, it is more robust to circuit-introduced errors. However, it is not suitable for a wide temperature range. Therefore, clearly, a trade-off exists between the high resolution/robustness provided by the time domain and the energy efficiency of SAR-ADCs.

The process of temperature measurement can be regarded as reading out the voltage of V_{sens} in Eq. 3.2. Such readout can be accurately digitized by a hybrid voltage-time two-step way, in which a full-range voltage domain conversion first obtains a coarse estimate of the V_{sens}. This is followed by a low range, but high resolution, fine time domain conversion to obtain an accurate estimate of the input level. In the proposed hybrid voltage-time domain topology, the strengths of both SAR-ADC and time domain converters are combined into a two-step conversion, as will be explained in the following.

A block diagram of a Hybrid V(voltage)-T(time) ADC is shown in Fig. 3.6.

It consists of a coarse voltage domain SAR-ADC and time domain TDC (Time-to-Digital Converter). A schematic representation of the coarse volt-

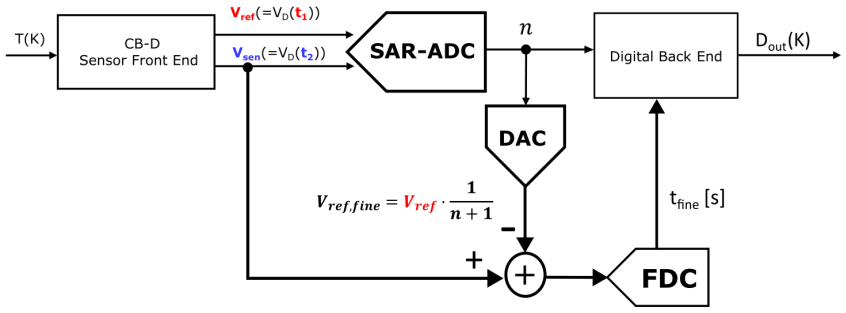

Figure 3.6: The system level block diagram of a hybrid voltage-time readout

age domain data converter's quantization levels and their relation to the zoomed-in voltage references of the time domain converter is shown in Fig. 3.7.

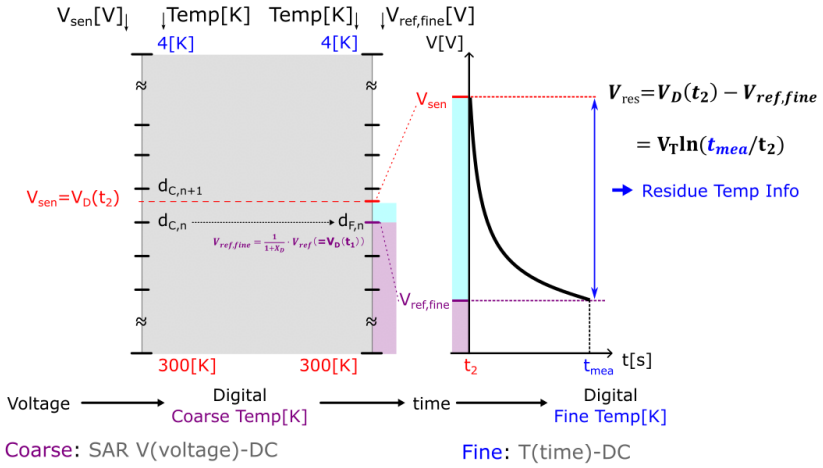

Figure 3.7: Working Principle of Hybrid voltage-time domain readout

The proposed topology is shown as Fig. 3.8. The corresponding timing is shown in Fig. 3.9. As for the detailed operation: firstly, **rst** is closed, biasing capacitors are precharged, while CDAC is discharged for charge-sharing preparation; secondly,**t1** and **t2** is closed for voltage decaying. After the time t1 and t2, the voltage $V_D(t_1)(= V_{ref})$, $V_D(t_2)(= V_{sen})$ is generated. After the decay phase, the voltage across C_{b1} is charge shared with CDAC during **charge-sharing**. This is followed by a comparator comparing the two inputs; After that, sar is updated.

With all SAR cycles, the voltage at the positive terminal of the comparator is updated as $V_{ref,fine}$. Then in the fine phase, CB-D2 start re-decaying until the voltage cross $V_{ref,fine}$. The full operation is shown as Fig. 3.10.

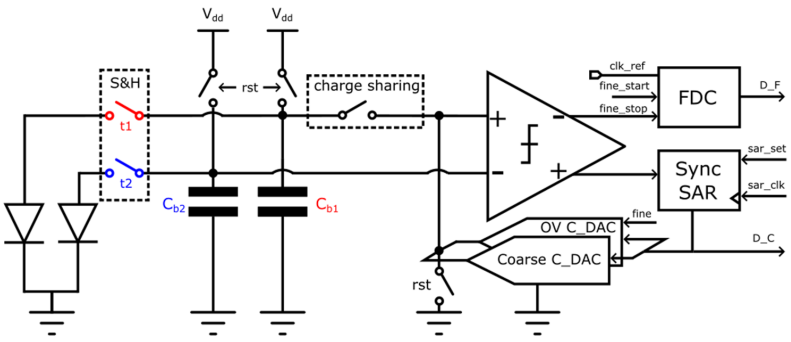

Figure 3.8: Proposed Architecture

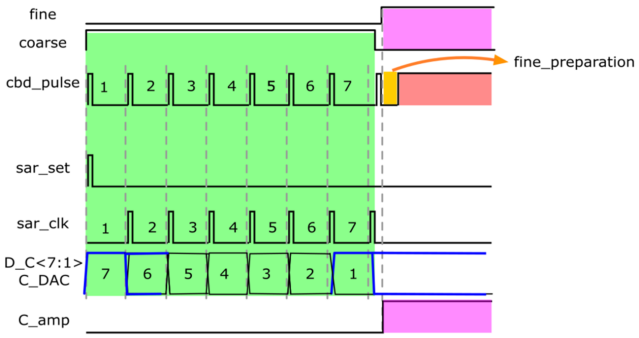

Figure 3.9: Readout Timing

In the proposed readout methods, the temperature readout process can be regarded as CTAT voltage V_{sen} readout in Eq. 3.2. In the coarse phase, the coarse estimation of V_{sen} is read out by the charge-sharing-based SAR algorithm. For the residue voltage information V_{res}, it can be read out by the time. The detailed process is that: during the fine phase readout, CB-D is decayed to cross the $V_{ref,fine}$–provided directly by the coarse converter. And then according to the CB-D voltage-time equation, the residue voltage information can be read out from the decay time t_{mea}. The mathmetical explanation is shown as below Eq.3.6.

$$\begin{aligned} V_{\text{sen}}\ (= V_D(t_2)) &= V_{\text{ref,fine}} + V_{\text{res}} \\ \text{Coarse: } V_{\text{ref,fine}} &= \frac{1}{1+X_D} V_{\text{ref}}\ (= V_D(t_1)) \\ \text{Fine: } V_{\text{res}} &= V_T \cdot \log\left(\frac{t_{mea}}{t_2}\right) \end{aligned} \tag{3.6}$$

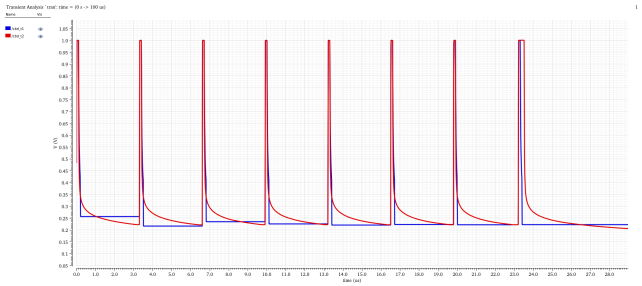

Figure 3.10: Hybrid V-T Operation

Another perspective for understanding the proposed topology is presented as follows: as described in Ch.2, the necessary condition for realizing a time domain readout is to generate a reference voltage($V_{ref,fine}$) which is relatively insensitive compared to the target readout voltage($V_{sen}(= V_D(t_2))$). This relation is shown in the Eq. 3.7.

$$V_{\text{ref,fine}} = \beta \cdot V_D\,(t_2)\,(\beta < 1) \tag{3.7}$$

The time information is obtained from the difference between $V_{ref,fine}$ and $V_{sen}(= V_D(t_2))$, see Fig.3.11.

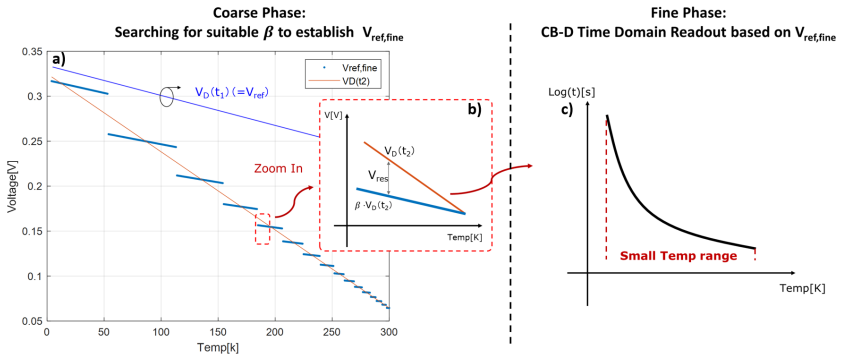

Figure 3.11: (a)temperature-dependent voltage in hybrid V-T readout; (b) Zoom-in voltage characteristics;(c) readout decay time in every fine range

Therefore, the process of this topology can be described from the point view of full-time domain readout as follows:

Firstly, with a coarse voltage domain converter, the suitable β is obtained for different coarse temperature ranges, which also means in the proposed

topology, the β factor in the initial scheme is changed from temperature-independent to temperature-dependent;

Then the temperature is obtained with a high-resolution time-domain method, which can be expressed in Eq. 3.8.

$$\frac{t_{\text{mea}}}{t_2} = \exp\left(\frac{(1-\beta)V_D\left(t_2\right)}{V_T}\right) \tag{3.8}$$

Here, $\beta = \frac{1}{1+X_D}$, which is same as Eq. 3.7.

With the proposed topology, the possible "Exponential Disaster" @4K and "Insane Hardware Requirement" @300K due to a single β in full range is thus possibly avoided, and also time-domain readout advantage would be possibly full-used, as will be explained in the next section.

3.3 Voltage-Domain Coarse Converter

Since the CMOS model at cryo is not available, an emulation model is necessary for us to predict the feasibility and reliability of the design choice at cryogenic.

A Charge-sharing-based SAR coarse converter model is built up for verification and design-assist purposes, shown as Fig 3.12.

Meanwhile, $V_{ref,fine}$ is also generated from the designed model for time-domain readout. See Fig.3.13 as the simulation result of Coarse Digital Output.

Simulation results of $V_{ref,fine}$ are shown and compared between the circuit schematic and Matlab can be seen in Fig.3.14.

3.4 Time-Domain Fine Converter

Based on the designed emulation model, readout time in the fine phase can also be obtained: the minimum readout time resolution at 300K(1/3ns$\approx$

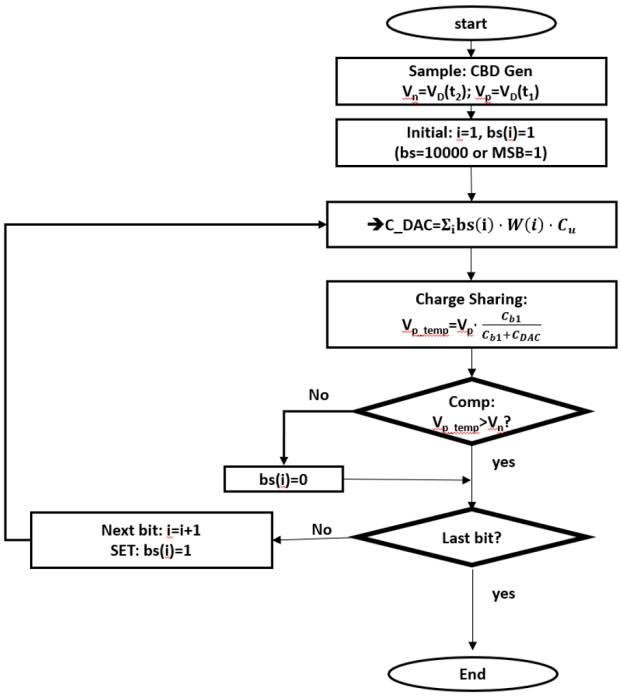

Figure 3.12: Charging-sharing based SAR algorithm

300MHz) is much relieved compared with the aforementioned time domain readout(p̃s) in the full range (4K-300K). Fine phase time domain readout is shown in Fig.3.15.

Fine-phase time domain output with full range(4K to 300K) is shown as Fig.3.16.

However, there are still several potential problems required to be optimized from a system level:

1. Fine phase measured time is still a bit long(1s) at cryo, which may allow the diode to reach the recombination region, as shown in Fig3.17.
2. In some temperature regions, for instance @∼50K shown, the readout time is shorter than t_2 due to $V_{ref,fine} > V_D(t_2)$ shown in Fig. 3.18.

   Such situations may lead to fine phase time domain readout reaching a fast decay region, causing supply sensitivity.
3. Fine phase readout resolution requirement for 0.1K is relatively high (∼x100MHz), which has room to reduce for further energy efficiency.
4. For fine phase readout, at high temperatures, the readout time region

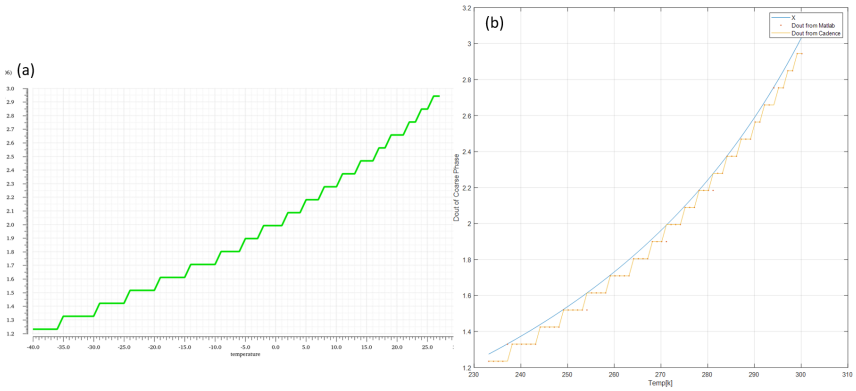

Figure 3.13: (a) Digital output in coarse phase D_C from circuit schematic @TT; (b) Digital output from Matlab emulation model

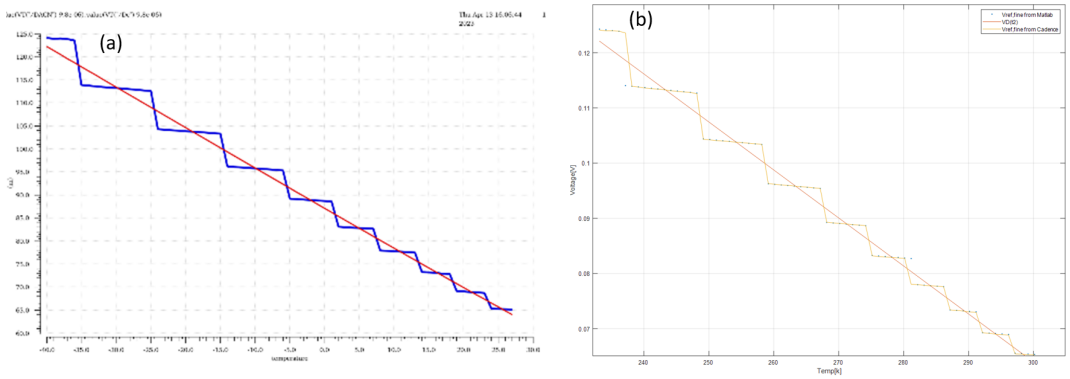

Figure 3.14: (a) $V_{ref,fine}$ obtained from circuit schematic @TT;(b) $V_{ref,fine}$ obtained from Matlab emulation model

is relatively short(x100 smaller than cryo), which will result in the fact that the designed FDC is not fully used, which could cause hardware waste.

To solve these problems, a full system-level emulation model is required. The emulation model built up and proposed over-ranging-based time-domain amplification solutions will be described in the following section.

3.5 System-Level Considerations and Optimization

In this section, the system-level design of hybrid V-T ADC is addressed, together with some considerations for its practical implementation. To ad-

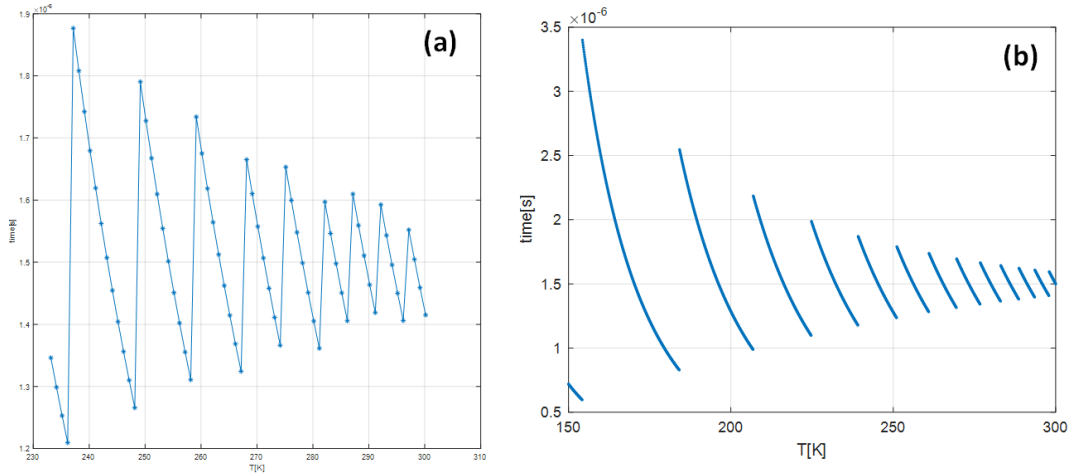

Figure 3.15: (a) Fine phase time domain digital output D_f from schematic @TT;(b) Fine phase time domain digital output from emulation model

dress this, a behavior model for the proposed topology was developed.

Fig 3.19 shows a simplified block diagram of the proposed topology, where various design parameters such as the current ratio, the resolution of coarse converter, the mismatch of DAC etc. can be adjusted. Detailed design process and related results are shown in Appendix.

Considering the aforementioned problems, the first one can be easily addressed by improving the coarse resolution from 5 bits to 7 bits. Then max decay time only 100μs is reached @cryo, shown in Fig.3.20.

All the rest problems can be addressed by the proposed over-ranging technique, which will be discussed in the subsection.

3.5.1 Over-ranging-based Fine-phase time-domain amplification

In practice, an over-ranging technique is often employed in two-step ADC, especially for zoom-ADC, which can be used to relax SAR ADC's required capacitive-DAC requirement.

In our case, the purpose of over-ranging is to improve the sensitivity and robustness of time domain readout further. To be sure the measured time is longer than t_2, 1 LSB over-ranging is employed specifically for the fine-phase time domain readout, which is shown in Fig. 3.21.

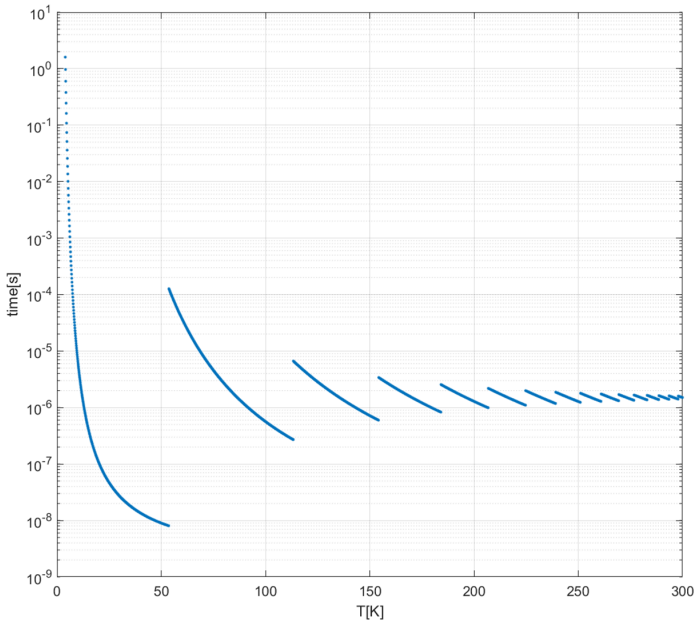

Figure 3.16: Fine phase time domain digital output from emulation model with full range[4K-300K]

In such a way, measured time in Fig.3.20 can be sure longer than t2 (=16us in our case).

This over-ranging can be used further to relieve the capacitive-DAC matching requirement. When observing the Eq.3.8, if we can make β smaller to β_{ov} in Eq.3.9.

$$\beta = \frac{C_{b1}}{C_{DAC} + C_{b1}} \Rightarrow \beta_{ov} = \frac{C_{b1}}{C_{DAC} + C_{b1} + C_{ov}} \tag{3.9}$$

Specifically in the fine phase, $V_{ref,fine}$ is lower. When crossing the reference voltage, the decay time is longer, and the current density of the diode at the crossing point is lower, which essentially means a more sensitive readout. Besides, other circuit components' error budget could also be relieved but still achieve 0.1K readout resolution.

With this concept, an over-ranging capacitor bank could be designed for amplifying readout time purposes. As in different coarse temperature ranges, the time amplification requirement is also different, so this over-

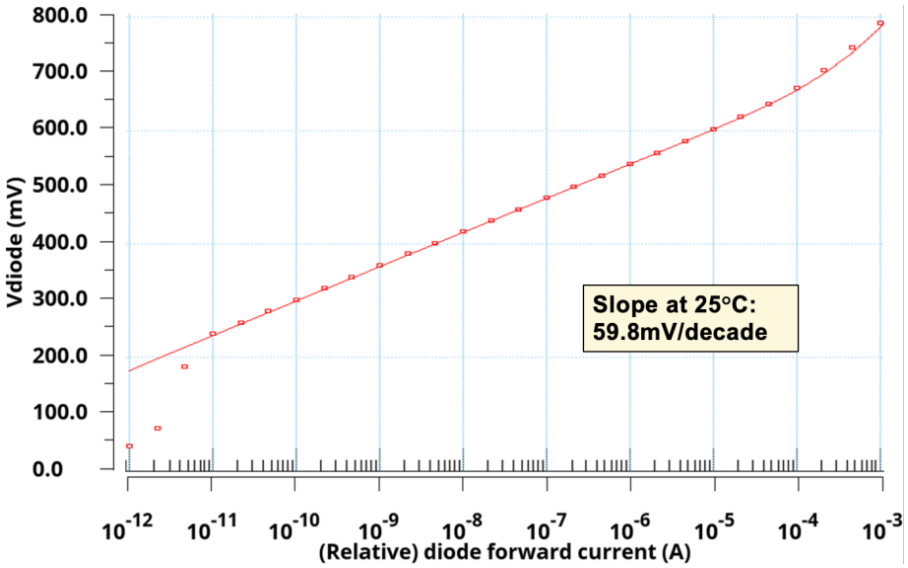

Figure 3.17: Transfer curve of the diode in Intel 16nm FinFET process[image reproduced from [42]]

ranging capacitor bank can be directly controlled by the digital output of the coarse SAR converter. One possible capacitor bank candidate is shown as Eq.3.10.

$$
\begin{aligned}
&C_{b1} = 4pF \\
&C_{b2} = 2pF \\
&C\_DAC = 40.9fF \\
&(\text{ with } 7bits \text{ and } 1LSB \text{ for over-ranging in fine phase }) \\
&[11b_5b_4b_3b_2b_1] \rightarrow C_{\text{ov }1} = 2pF \\
&[10b_5b_4b_3b_2b_1] \rightarrow C_{\text{ov }2} = 1.2pF \\
&[011b_4b_3b_2b_1] \rightarrow C_{\text{ov }3} = 380fF \\
&[010b_4b_3b_2b_1] \rightarrow C_{\text{ov }4} = 100fF
\end{aligned}
\tag{3.10}
$$

The corresponding fine phase readout time is shown in Fig.3.22. The required time domain resolution for 0.1K is also reduced from 300MHz without over-ranging to only 20MHz required, see Fig.3.23.

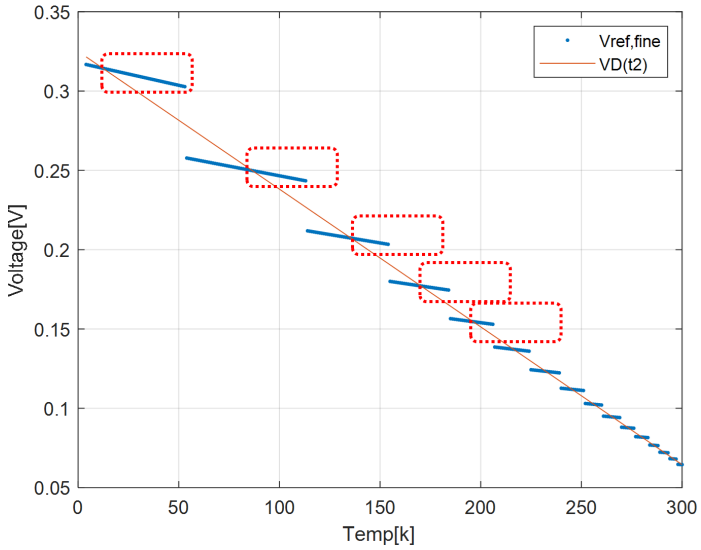

Figure 3.18: Red Region indicating where $V_{ref,fine}$>$V_D(t_2)$ leading to $t_{mea} < t_2$

3.5.2 Robustness Verification

In this SAR-based voltage domain readout, the matching requirement of capacitor DAC limits the readout resolution for 0.1K target ($\approx$ 13bits). With the proposed hybrid V-T readout scheme, the matching requirement is significantly relieved due to the intrinsic robustness and exponential transfer function between time and temperature. The calculated requirement is shown in Fig.3.24

The emulation model can also be used to investigate the effect of the mismatch between the unit elements of the feedback DAC.

Fig.3.25 shows the simulated temperature error(INL) of the proposed sensor with the random mismatch of feedback capacitive-DAC, assuming a normal distribution with mean=0 and $\sigma = 0.75\%$(same with intel PDK).

As shown, the resulting temperature errors can be as high as $\pm$0.3K. With over-ranging, the accuracy is improved to $\pm$0.05K due to higher sensitivity, representing a 5x improvement, which also verified an intrinsic robustness of time domain readout.

Another important observation can also be concluded from Fig.**??** is that at cryogenic temperatures, time domain readout, irrespective of with or without over-ranging capacitors, yields minimal temperature errors at cryo-

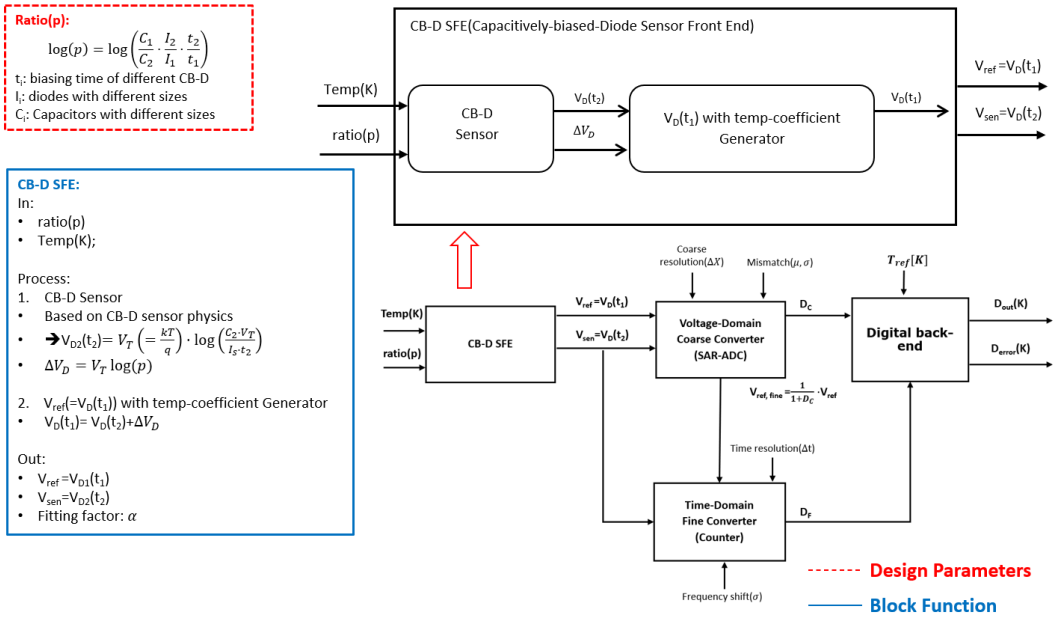

Figure 3.19: Hybrid V-T ADC Behaviour Model and corresponding parameters explanation

genic, which is attributed to the time-domain inherent "low-temperature but high-temperature-sensitivity" property.

3.6 Curve Fitting and Post-End Digital Processing

So far, a hybrid voltage-time domain readout method has been introduced. However, further digital signal processing is required before an output D_{out} in real temperature can be obtained.

Traditionally in CS-BJT-based temperature sensor with a Zoom-ADC readout [49], the ratio function X is obtained by summing the coarse and fine digital output directly. Whereas in the proposed topology, the temperature is obtained by fitting the fine phase time-domain digital output with temperature, shown as 3.26.

A coarse voltage domain converter provides only the temperature range information D_C during the fitting process and is not involved directly in the process of fitting the data to obtain the digital output.

In the shown block diagram, $\beta = t_{mea}/t_2$, for every range, A_f and B_f

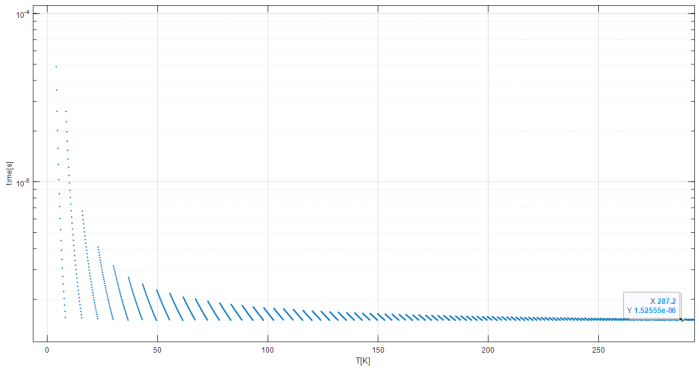

Figure 3.20: readout time in full temperature range(4K to 300K) with over-ranging technique

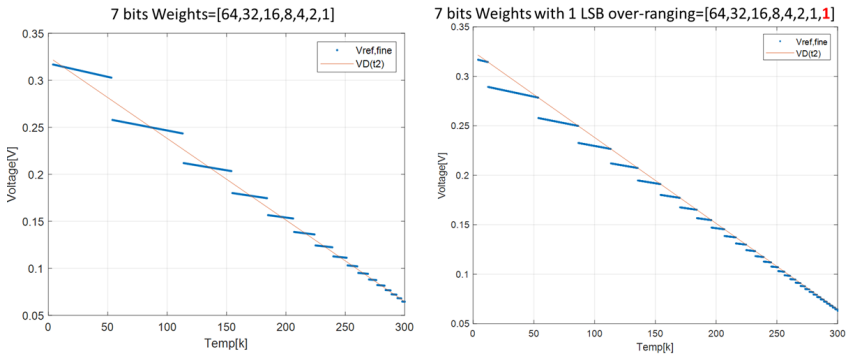

Figure 3.21: $V_{ref,fine}$ vs $V_D(t_2)$ without(left) and with(right) over-ranging

should be calculated as fitting parameters.

3.7 Concluding Remarks

In this chapter, a novel "Hybrid Voltage-Time(V-T) domain" readout method is introduced. This innovative readout method, which combines voltage and time information from the sensor, is also the first time proposed in the field of standard smart sensor design. Compared with traditional full-voltage domain Zoom Readout, fine conversion traditionally employed with a $\Sigma - \Delta$ Converter is replaced by counter-based time-domain readout in a digital-friendly way. Based on the proposed over-ranging technique in fine phase readout, the readout resolution is improved further. In the proposed Hybrid V-T readout, the digital strengths of both SAR-ADC and time-domain readout are combined into a two-step conversion, which is suitable for our cryogenic target applications with digital and compact purposes.

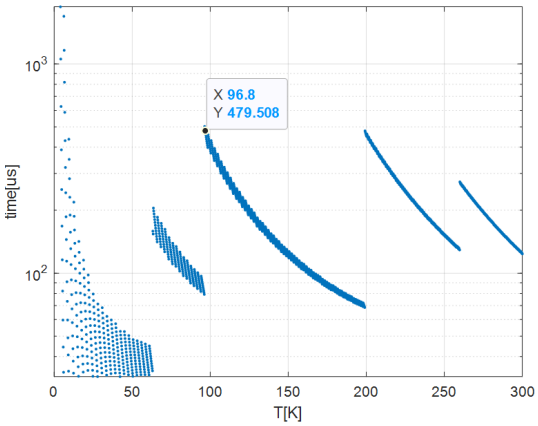

Figure 3.22: Fine phase readout time with over-ranging technique

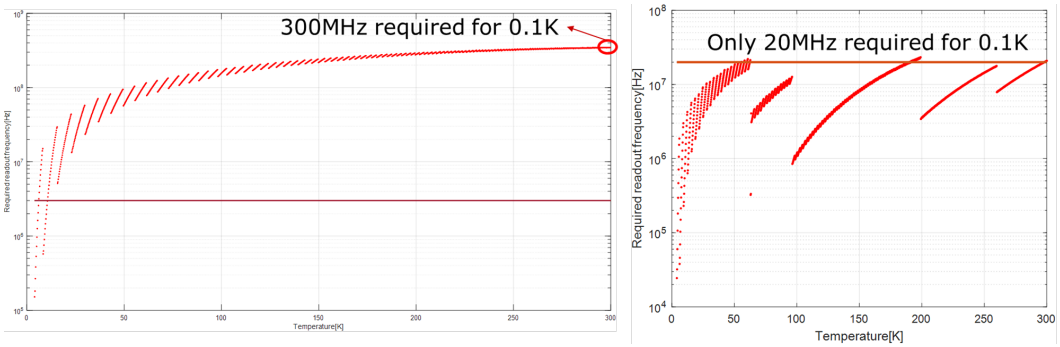

Figure 3.23: Fine phase time domain readout resolution requirement:(a) without over-ranging; (b) with over-ranging

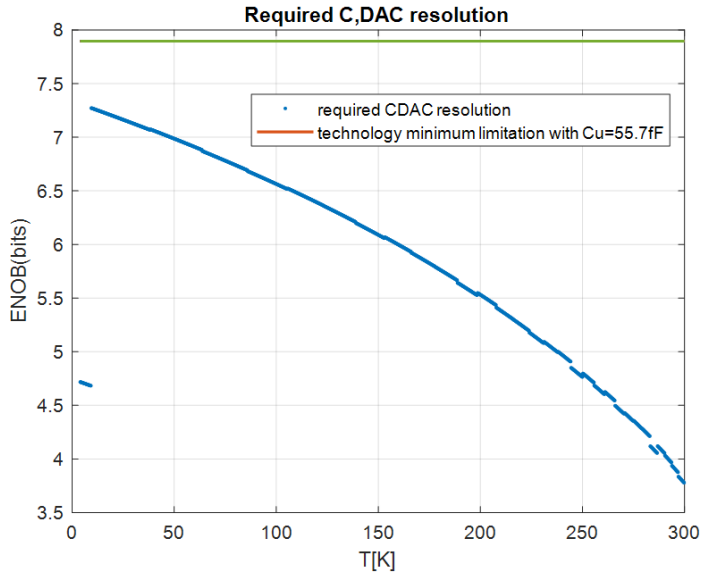

Figure 3.24: Matching Requirement of Proposed Topology

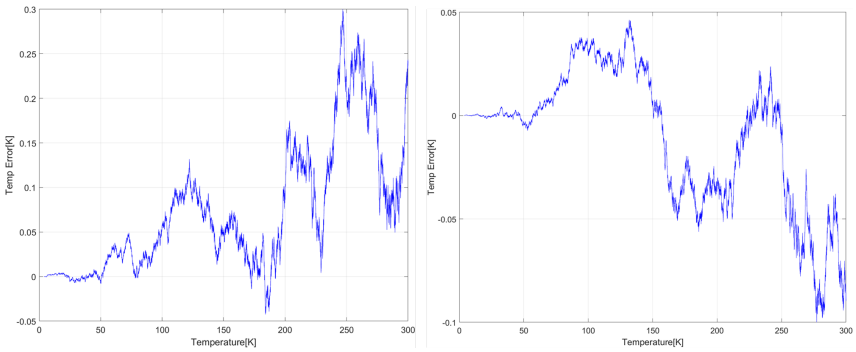

Figure 3.25: Simulated temperature error between DAC elements: without(left) over-ranging and with(right) over-ranging.

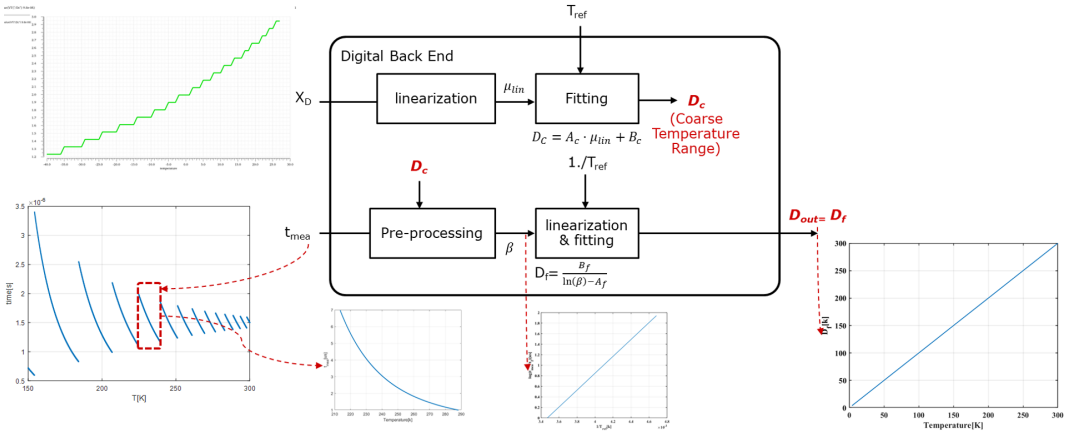

Figure 3.26: Digital-Back-End Block Diagram

4. Circuit Implementation and Performance

In the previous section (Ch.3), we proposed a novel capacitively-biased-based smart temperature sensor topology with a hybrid voltage-time domain readout method for cryogenic quantum computing with ultra-wide temperature range applications. In this section, we first provide the detailed circuit implementation of a CB-D-based fully programmable smart temperature sensor. This is followed by the performance of full system.

4.1 System Programmable Digital Controller

The overall architecture consists of analog core circuit and system programmable digital controller, see Fig:4.1.

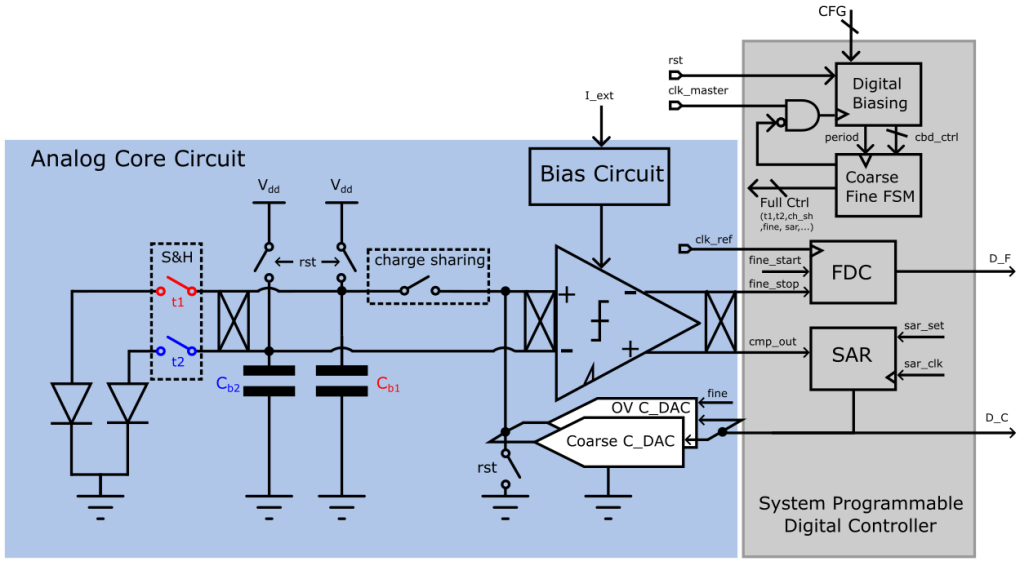

Figure 4.1: Architecture with Hybrid V-T Readout

The digital controller will be first introduced.

4.1.1 Overview

Regarding the sensing elements of the targeting technology–intel 16nm FinFET–there was no prior temperature-dependent and characterization measurement transistor behaviour data in group. Therefore, the motivation for designing this CB-D based smart temperature sensor, while ensuring that it meets the requirements of being able to characterize the behavior of CB-D sensor at cryogenic, is also required to be flexible and programmable enough to prove the concept of the readout we presented in Ch.3 is valid.

There are two different clocks for the inputs to the system. clk_{master} for control pulse generation and clk_{ref} for fine-phase time measuring frequency reference. Based on the configuration input bits, the initial pulses for CB-D behavior are generated. After this, these pulses are used in the Counter-based Coarse-Fine State Machine for further processing. The output of the Coarse–Fine FSM is employed to control the analog core circuits, update of sar phase and switch of coarse and fine. The Coarse SAR converter updates the CDAC based on the output of the Comparator and outputs the Coarse Voltage Domain digital output. The FDC is employed as the time domain readout of the fine phase based on the start and stop signal. The details will be shown in the following sub-sections.

4.1.2 Programmable Digital Biasing Network

A fully programmable digital bias network is designed shown as 4.2.

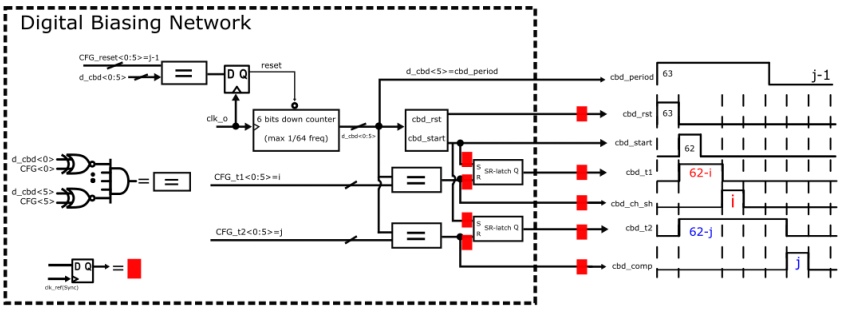

Figure 4.2: Fully Programmable Digital Biasing Network

It mainly includes:

1. A ripple down 6 bit counter up to 1/64 frequency division, where d_-cbd<0:5> is its binary digital outputs;
2. <cbd_rst / start> status generator: counting status(CNT)=63 is indicated as the reset signal at every first phase of CB-D core. CNT=62 is indicated as the start signal of decaying pulse t1 and t2.
3. Digital comparator: employed to compare the data from external with the d_cbd<0:5>
4. SR latch: for final decay pulse generator: t1, t2.

To way to generate clock t1 and t2 in CB-D phase with any duration, the specific biasing time is supposed to be controlled by external configuration bits. The input of the digital comprator are the counting status signal(d_-cbd<0:5>) and external configuration bits<CFG_tx<0:5»with the same bits number. This digital comparator define the stop signal of t1 and t2. This provides an important freedom to change temperature transfer function for ease cryogenic purposes. In this way, the maximum biasing time ratio between 2:63 is well defined.

In addition, signal "cbd_ch_sh" and "cbd_comp" can be used as the charge-sharing phase and comparison phase directly.

In order to reduce power consumption, the reset signal is also set as a configuration, which means in the case the time ratio we set is smaller than 63, after completing the bias and comparison, there is no need to waste additional power. In this way, the clock can directly switch to the next phase.

When using the ripple counter as the clock generator, it easily has glitches. To avoid these glitches influencing the timing, extra DFFs for synchronization are required shown as red region 4.2.

4.1.3 Counter-based Coarse-Fine State Machine

Since the required states in total are $coarse(7) + fine\_rdy(1) + fine\_start(1)$, which in total 9, this means at least a 4-bit ripple counter for state counting is required. The system diagram is shown in Fig.4.3.

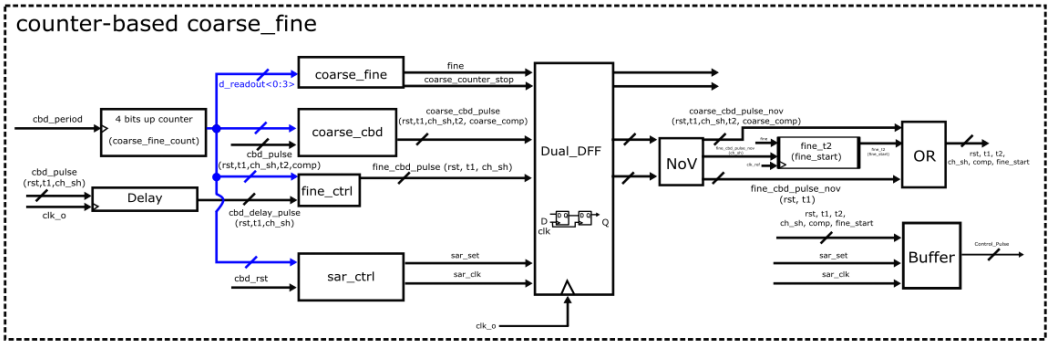

Figure 4.3: Counter-based Coarse-Fine State Machine

The input of the up ripple counter is the output: MSB (CBD_period here) of the digital biasing network, while the output is employed to define full control signal, like stop signal and rest control signal which are employed to control the circuit core, etc. When It reaches 9 it will stop full thing, for power saving purposes.

The function of the or gate chain is for combining the coarse and fine,*rst*, *t*1,*t*2 *ch_sh*. For example, *rst* in CB-D is used as either in coarse phase or in the $fine\_rdy$ phase, would be used as a OR gate to combine, then feed into the circuit core. Each clock passes through a Dual DFF to before it is fed into the core circuit. This is to avoid metastability.

Fig. 4.4 shows the timing of the coarse phase and CB_D pulse relation from Fig.4.3.

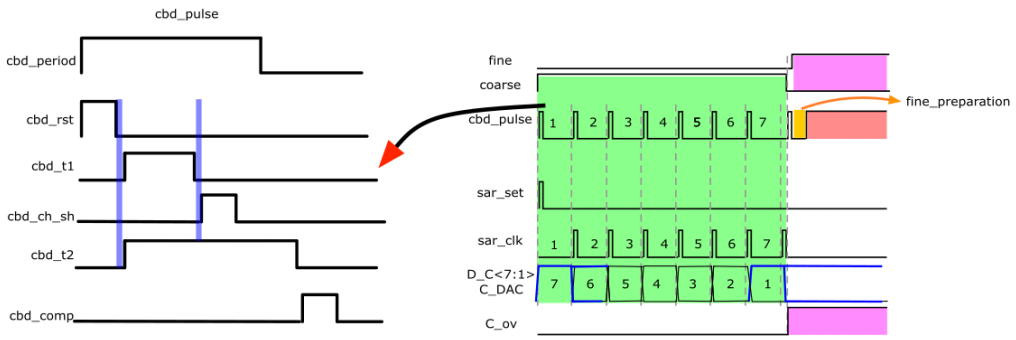

Figure 4.4: Coarse Phase timing(right) with CB_D pulse(left)

Each CB_D pulse is followed by a sar_clk (i+1 rst). sar_clk will update the coarse readout and DAC according to the comparator result. The sar clk does not require additional clk control, which effectively reduces the cost.

Fig. 4.5 shows the timing of the fine_rdy phase and fine phase time domain readout.

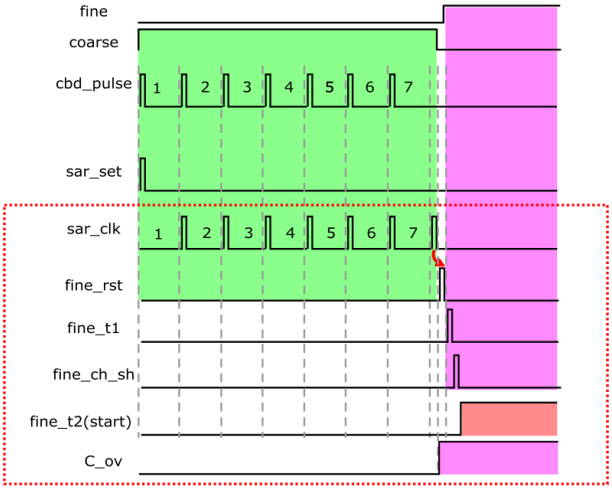

Figure 4.5: Fine-rdy and Fine phase time domain readout

The $fine\_rdy$ phase for building the $V_{ref,fine}$ begins immediately after the last sar update. This is thanks to the delay module in Fig.4.3. It is essentially a pipeline function that delays all *cbd_periods* by one "rst" so that the readout of the fine phase can start immediately, which reduces power consumption and improves the conversion efficiency. At the same time, the EN of the over-ranging capacitors will also be turned on to prepare for the generation of $V_{ref,fine}$.

Besides, we need to ensure non-overlapping between *rst*, $t1$, and *ch_sh* to avoid potential timing issues, To avoid affecting the time length of $t1$ and $t2$, therefore a customized non-overlapping block is designed, the schematic of which is shown below in Fig.4.6.

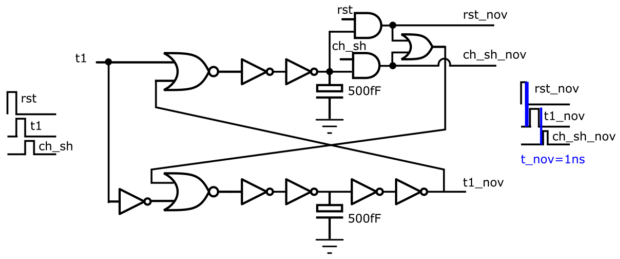

Figure 4.6: 3 phase non-overlapping

The clock gating path (see Fig.4.7) is also designed for energy efficiency and keeping functionality purpose.

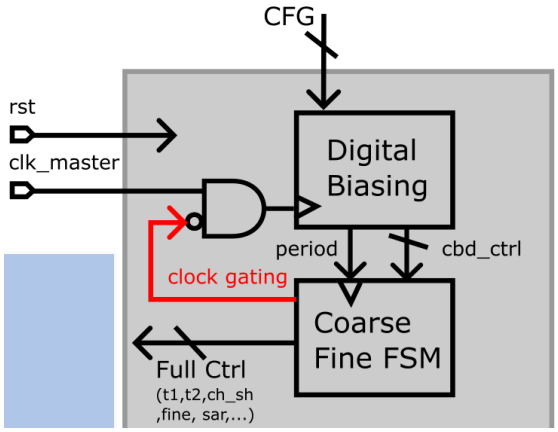

Figure 4.7: Clock Gating

The combination logic of it is when the state machine counts to 9, the full controller will be stopped. However, this is not common in digital design, as this stop signal will usually have some delay when other digital blocks use the same clock. But in our case, as we only use one clock for full system control, such an issue would be avoided. Also with such a design way, asynchronous DFF is necessary. Every time we need to redo the temperature measurement, a reset signal is required to start the function.

4.1.4 Coarse-Fine-Data-Conversion

For the coarse phase, a standard sar logic is employed shown in Fig. 4.8, in which it consists of one shifter register for counting with one data register for data storage and update.

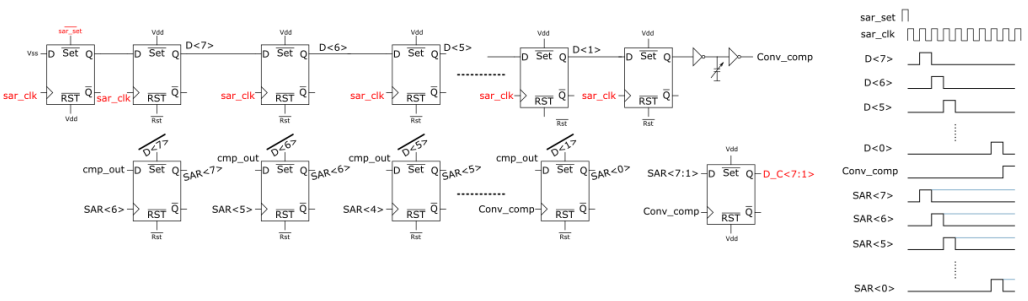

Figure 4.8: Coarse SAR Logic

For fine phase readout, a ripple 20 bits counter is over-designed since at cryogenic, the decay time may still be too long due to the exponential relation with temperature, shown in Fig.4.9.

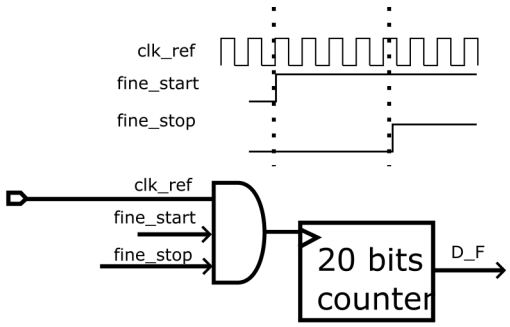

Figure 4.9: Fine phase Converter

4.2 MOS-based Diode Family Design

This section will provide a detailed analysis of the design considerations for sensor cores based on Finfet transistors. In FinFETs, unlike traditional bulk CMOS, altering W (width) and L (length) is not straightforward at the device level. To extend the transistor's length, one must stack transistors sequentially(increase S). Conversely, to increase the width, transistors should be positioned side by side(increase m). See Fig.4.10.

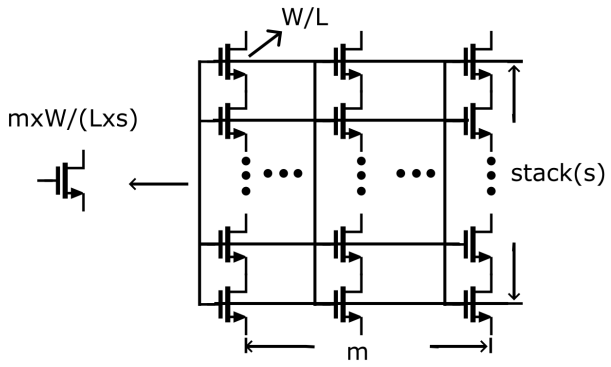

Figure 4.10: Finfet to increase W and L

The regulation of W and L has the following main considerations:

1. For the consideration of L, L cannot be short. in Finfet, a smaller L will cause a short device effect at cryogenic [50]. This in turn will lead

to a significant increase in n in SS. The increase of n will lead to the degradation of SS, which may affect the sensitivity of PTAT voltage.

2. The design consideration for W is mainly based on the mismatch, and we need to provide a large enough area so that the mismatch can be assumed negligible. Since there is no report on the measurement characterization of the Finfet mismatch. In this paper, based on the previous analyses of mismatch, we finally decided to choose the diode size of **W=360n, L=40n, m=30, s=50**, stack designed for 50 and m designed for 30 which can satisfy the good tradeoff between mismatch, short channel effect at cryogenic and area as much as possible. In addition, in order to minimize the intrinsic resistance, a good terminal contact between the gate/drain and Metal 1 is also necessary.

Due to the sensor core's chopping operation, these two diodes are chosen to be of the same size. The NMOS PMOS and DTMOS are designed to have the same dimensions in order to make a fair comparison during measurement later on when the chips come back from tape out.

4.3 Capacitor Bank Design

The capacitor banks involved in this sensor include Cb1 for high-biasing voltage($V_{ref} = V_D(t1)$), Cb2 for low-biasing voltage($V_{sen} = V_D(t2)$), coarse-sar cdac for coarse quantization, fine-over-ranging cdac for fine phase readout time amplification.

The main design considerations include: for Cb1 and Cb2, they need to provide as large a ratio as possible so that when at cryogenic it can be obtained while still providing sufficiently sensitive PTAT voltages to enable high-resolution readout. Maximum CDAC size should be decided by the PTAT function shown as Fig.4.11.

The actual size of the capacitor DAC is usually determined by the noise specification. However, in this design, the capacitance value is determined by the leakage allowed and the matching requirement, since leakage is the main source of error as described previously. The unit capacitance should

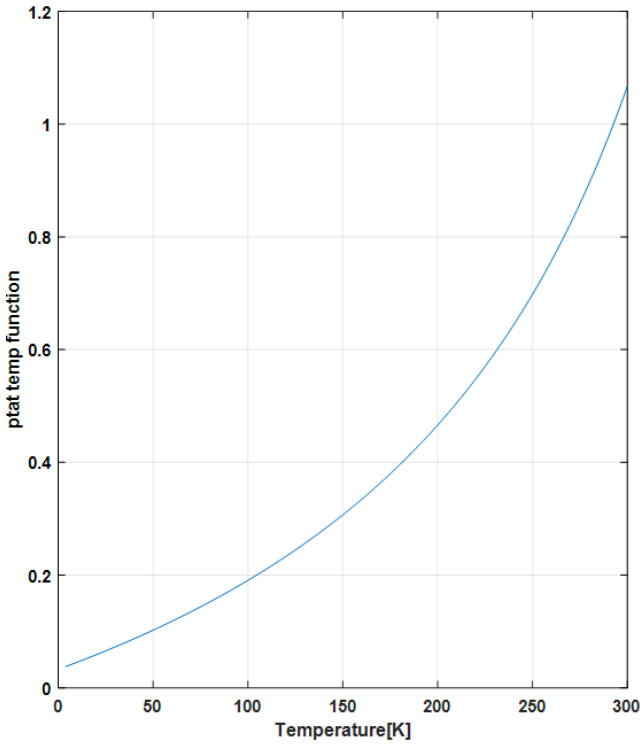

Figure 4.11: coarse phase ptat transfer function C_{DAC}/C_{b1}

be large enough to tolerate more leakage. Also, all capacitors need to be based on the same unit-size capacitor to optimize matching.

Based on the above analysis the capacitance values of each component and the logic for determining them are as Tab.4.1

	Size	Rational
Cu=54.57fF	1	leakage
Cb1	100	large ratio for high sensitivity
Cb2	20	large ratio for high sensitivity
CDAC_coarse=123 Cu	123	7 bits Coarse DAC
Cov=123 Cu	123	Over-Designed for Characterization Purpose

Table 4.1: CBANK Design

Unit capacitance based on higher capacitance density MOM capacitance double shielding between M3 and M5 for matching purposes. The maximum time ratio t2/t1=63/1 with Cb1/Cb2=5 can contribute to the ptat current density ratio=315; while the maximum value of the coarse CDAC is determined by the temperature PTAT temperature transfer function(shown as 4.11)at 300K 1.2, which can efficiently cover the large temperature range

required. For over-ranging capacitance, over-designed same with the coarse 7-bit C-DAC for flexibility and characterization purposes. It can also be controlled by external configuration signals for characterization and trimming purposes.

For the C-DAC driver (shown as 4.12), all switches used in the C-DAC are thick devices.

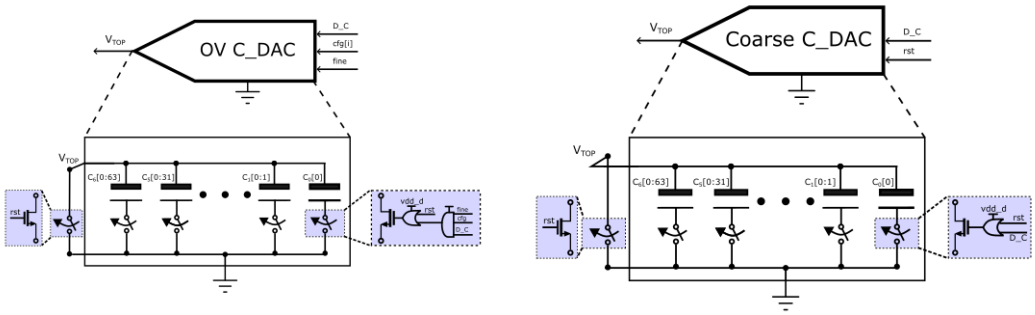

Figure 4.12: CDAC driver for (left) coarse CDAC and(right) Over-ranging CDAC

Since gate leakage causes potential issues for thin-oxide switches, and to prevent on-resistance from being too large at cryogenic, the gate of these switches is driven by a level shifter.

4.4 Comparator

In this section, we will explain design consideration and implementation of the comparator.

4.4.1 Architecture

The comparator, shown as Fig.4.13, as the only analog circuit module in the circuit, is the heart of the entire A/D conversion.

In this design, although the coarse and fine reads share a common comparator, the performance of the comparator mainly depends on the requirements of the fine stage time domain readout. For this reason, the classical two-stage continuous-time comparator is applied in this design. This topology consists of a current OTA with a cross-coupled pair for positive feed-

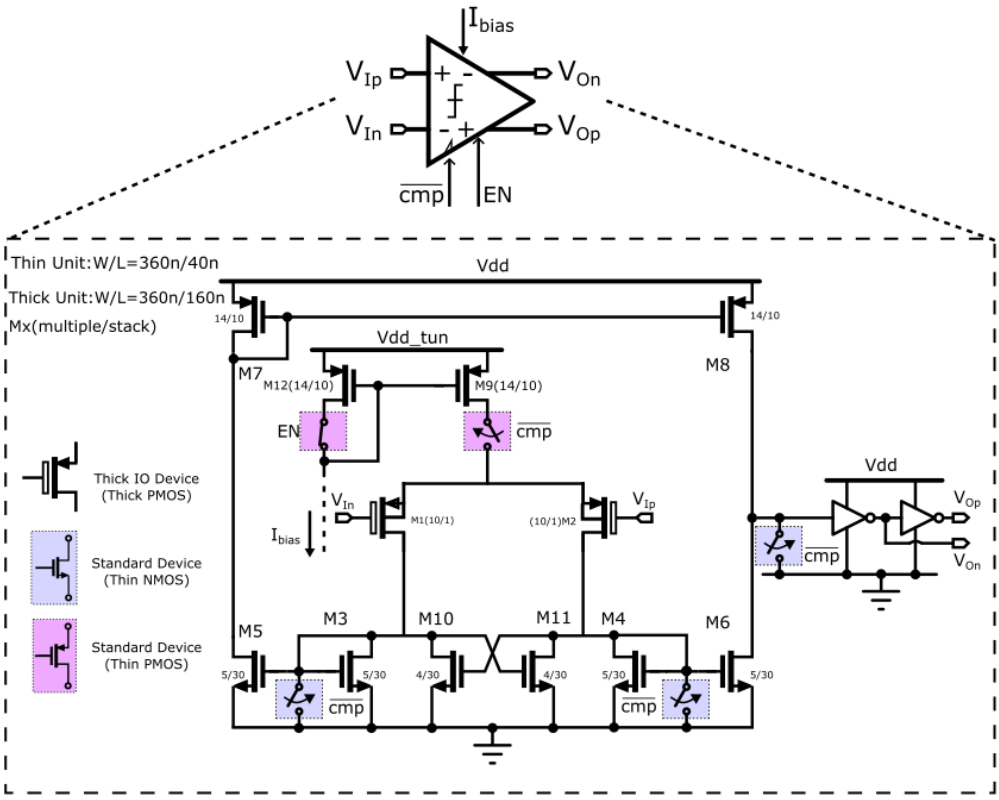

Figure 4.13: Two-stage Continuous Time Comparator

back to boost gain purpose. The gm11 is implemented with M11 and M10, whose gates are cross-coupled at the output. When gm11 value is close to gm6. The dc gain is increased. Thanks to the aforementioned Finfet high gm and rout intrinsic property, a DC gain >70dB with a 15 ns delay is achieved. The switches shown in the schematic: **Comp** is for comparator gating purpose during the coarse phase and **En** is for enable between different sensor candidates. Regarding the voltage domain offset, it will be reduced with a static chopper.

To accommodate the low input voltage of the MOS-based diode (range from 300 mV to 500 mV), PMOS devices are used for the input pair. Thick oxide devices are also used to reduce gate leakage.

Besides, there is a specific cryogenic concern analyzed. It is worth noting that for M9, as the current source, will introduce an offset if it enters the linear region, which can easily happen in the cryogenic case. The V_{dsat} of the M9 is measured to be 95 mV at -40 °C. So the stability of the M9 in

the saturation region is limited by the threshold voltage of the input pair. At cryogenic, the available margin of the M9 decreases due to the increase in threshold voltage. Since we currently do not have any cryogenic model for the thick model, the threshold voltage increase is difficult to predict reasonably. And this threshold voltage rise can easily exceed the expectations. The comparator is designed for biasing by adjusting the number of stacks so that it can cope with a nearly 200 mV boost. For safety, a separate M9 supply is provided to ensure that the M9 can be externally controlled to return to saturation at very low temperatures.

4.4.2 Biasing Current Generation

A current generator for the biasing comparator of different sensor candidates is designed and shown as Fig. 4.14.

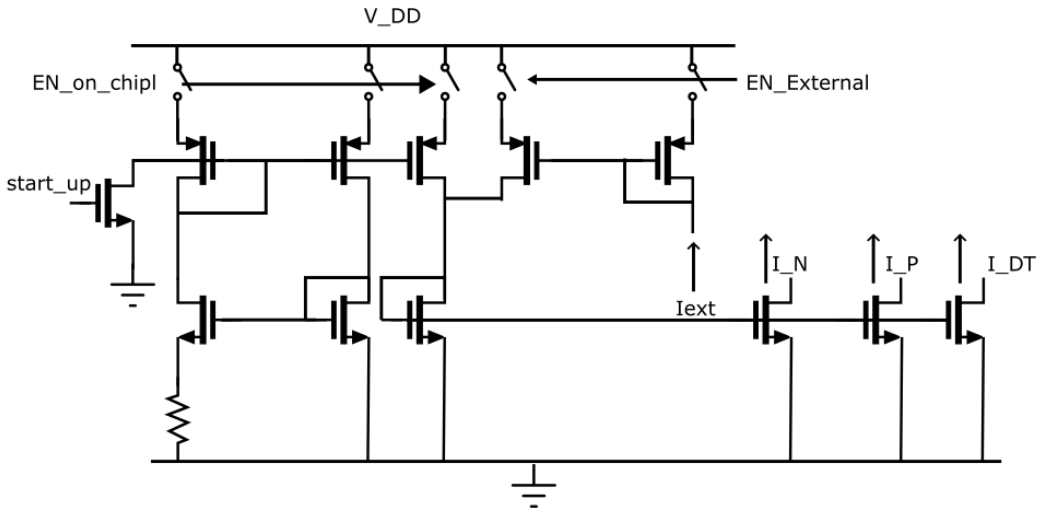

Figure 4.14: Bias Circuit for comparator

Especially for intel resistors, there is one resistor type, which may transfer to superconducting at cryogenic. Therefore, an external biasing current is required to avoid any unwanted potential issue,

The start-up pulse triggering the transistor is the same as reset in the digital controller.

4.4.3 Simulation Results

Fig. 4.15 shows the offset of the comparator. It can be seen that the comparator shows a worst-case offset of 0.7 mV.

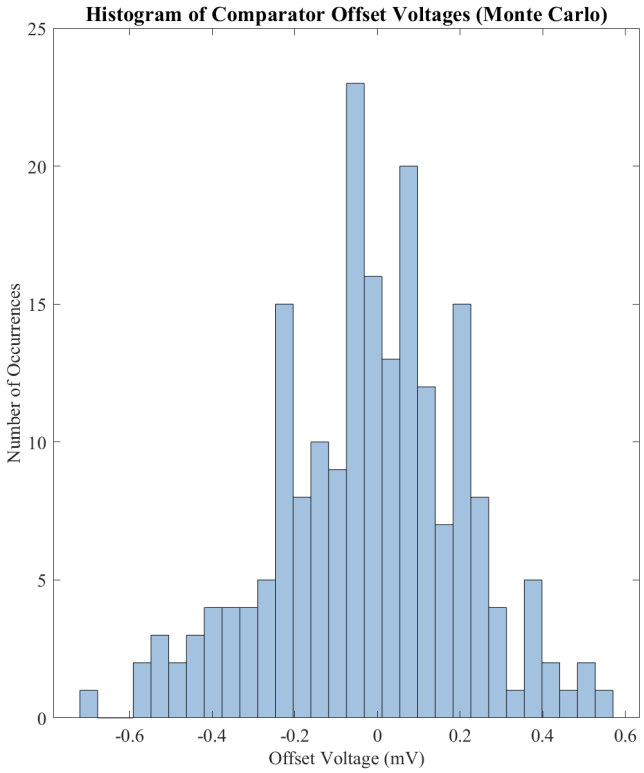

Figure 4.15: Offset Voltage of comparator

Fig.4.16 presents the AC response.

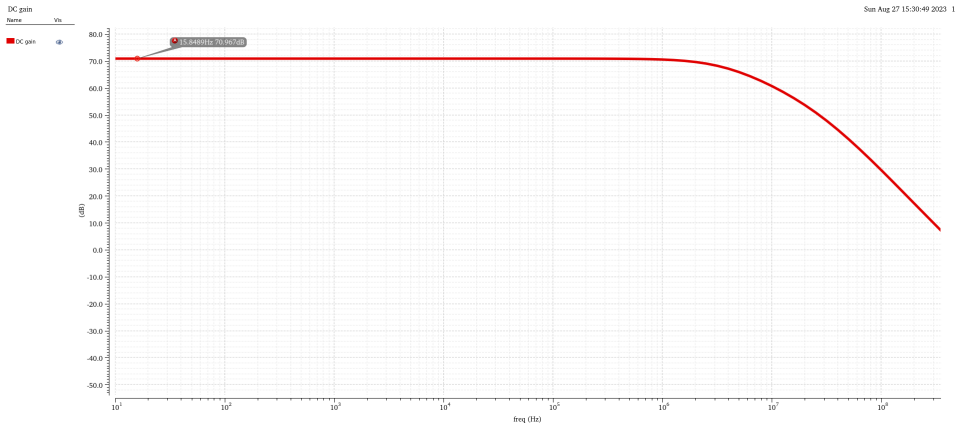

Figure 4.16: DC gain of Comparator

Fig. 4.17 and Fig. 4.18presents the robustness of the comparator to the corner.

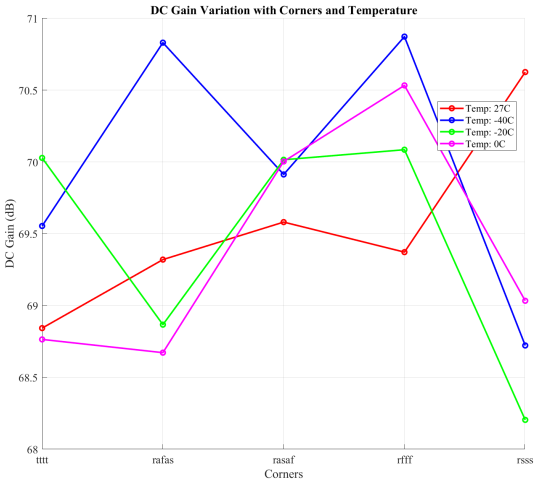

Figure 4.17: DC Gain variations with Corners

DC gain is slightly changing from 68dB to 71dB, showing a robust process variation.

Fig. 4.18 shows the comparator delay. The way to test delay is to directly test the delay between the decay voltage across the reference voltage and the transition time at the output of the comparator. The worst case is at -40 $\circ C$ and the corresponding delay is 11.5ns. The comparator consumes 12.5 μA and the bias circuit consumes 4.1 μA.

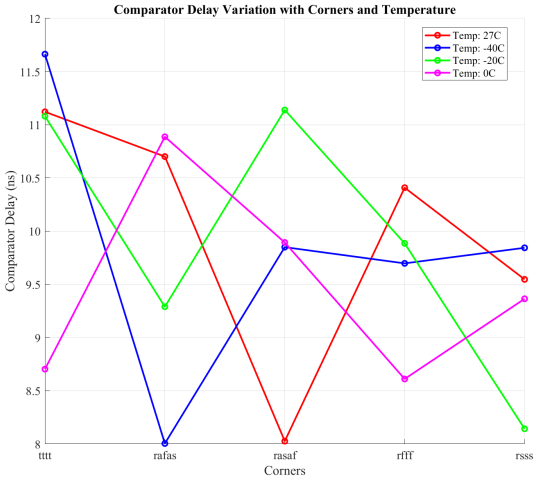

Figure 4.18: Compartor Delay

4.5 Switch and Chopper

To avoid gate leakage, all the switches are implemented as NMOS thick-oxide, only rst is PMOS thick-oxide. Therefore, before the pulses from the digital controller to the circuit core, all of these pulses are required to go through a level shifter to a voltage level of 1.8V for thick-oxide switch operation. The level shifter is re-used from the group, showing proper functionality at cryogenic. The delay of which is ≈100 ps, which translates to a negligible temperature error in time domain readout (<0.01mK).

To reduce the effect of offset of comparator as well as the potential increased mismatch of the diode at cryogenic, two choppers switches, shown as Fig. 4.19 with f_{comp} and f_{diode} are implemented.

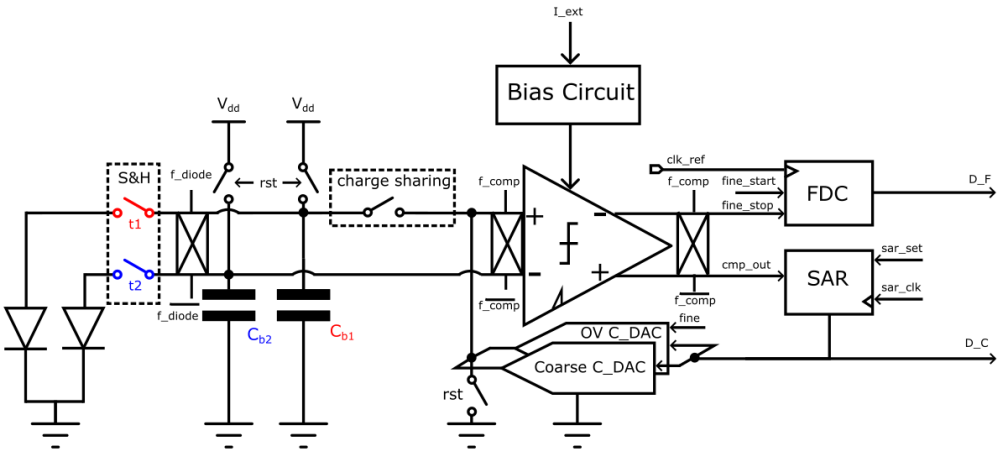

Figure 4.19: Switches and Choppers

Considering the reliability at cryogenic, the chopper of this sensor is a static configurable chopper.

Therefore, the sensor fine phase measured time can be determined by four different phases, which show less sensitivity to the offset of the comparator.

4.6 Full System Performance

The aim of this section is to show the performance of the proposed smart temperature sensor. Firstly, the functionality is tested again with the real

capacitors from the intel provided. Secondly, the accuracy is characterized for different corners and the resulting temperature error is reported. This is followed by the power budges between different circuit blocks. Finally, this work is compared to the state-of-the-art CB-D-based smart temperature sensor.

Due to the significant amount of simulation time, the following is based on DTMOS sensor candidate, and for fine phase readout only temperature ranging from 233.1K to 234K is reported.

4.6.1 Functionality test

4.6.1.1 Coarse Test

Fig.4.20 shows the coarse phase functionality between the schematic and Matlab emulation model. Comparing aforementioned Ch.2, ideal capacitors are used in the model in Chapter 3, which indicates a better fitting. However, when using the real capacitors, the diode-self capacitor will also involve charge sharing, which also causes a mismatch between the schematic and Matlab model.

4.6.1.2 Fine Test

The time readout from fine phase is shown as Fig.4.21 and Fig. 4.22 seperately. Both of them show a CTAT time, which also proves the concept. The advantage of over-ranging-based scheme is obvious, which shows much higher sensitivity.

4.6.2 Accuracy

Fig 4.23 shows the process spread simulation. By calculating the master curve with the emulation model introduced in chapter 3, the temperature error is obtained.

With the assistance of over-ranging technique, +0.5/-0.3K temperature error is achieved shown in Fig.4.25.

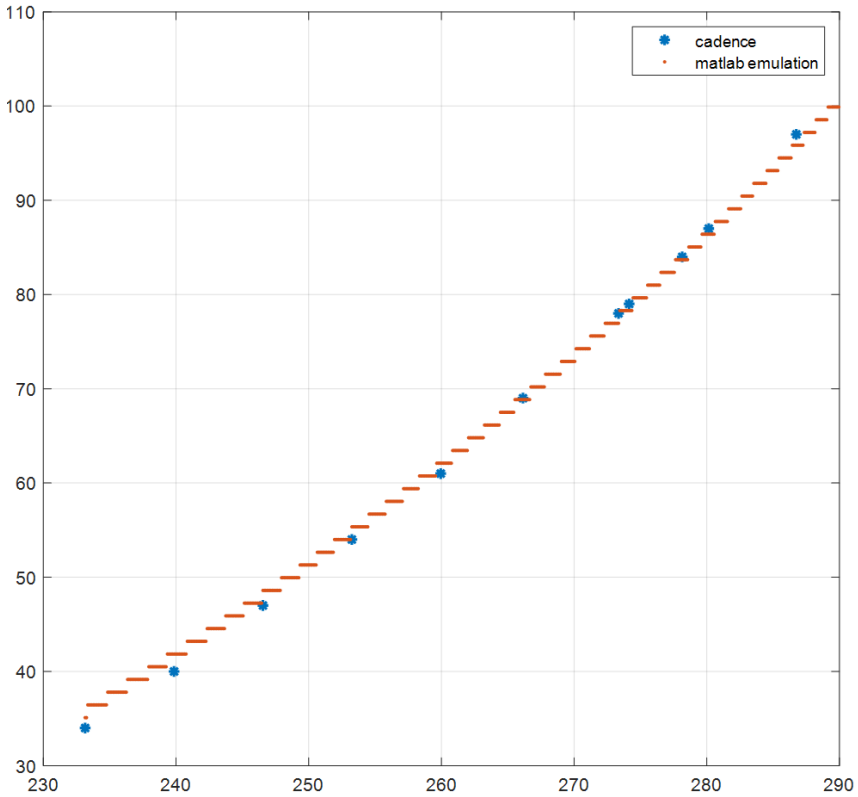

Figure 4.20: Coarse Readout Function Test

4.6.3 Power

Table 4.2 shows the power breakdown of simulated room temperature 300K. From the table, it can be seen that the comparator occupies the main power consumption, and the power consumption can be further reduced by replacing the coase phase comparator as a dynamic comparator.

	Power consumption
	300K (simulation)
Total	21.9 μW
CB-D core	1.38 μW
Full 1.1 V digital	2.92 μW
Comparator with bias circuit	16.6 μW
Level Shifter and Others	1.01 μW

Table 4.2: Power BreakDown

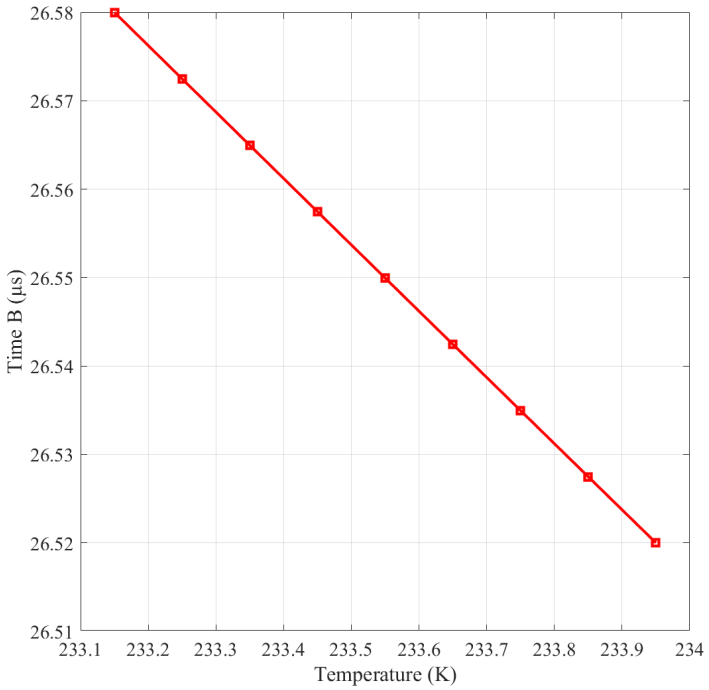

Figure 4.21: Fine Readout Function Test without over-ranging capacitor

4.6.4 Comparision to State-of-the-Art

Tab. 4.3 presents the comparison between this work and other prior art topologies. Especially compared with work [42], the Resolution FoM is improved x2, which also indicates the energy efficiency of the proposed readout method.

	This work	SSCL'21	SSCL'19	CICC'20
Technology	16nm	55nm	16nm	28nm
Type	MOS Hybrid $V-T$	PNP DT $\Sigma\Delta$	Bulk Diode SAR	DTMOST OSC
Area $[mm^2]$		0.021	0.0025	0.017
Supply [V]	0.9	1-1.3	0.85-1	0.85-1.15
T. Range [°C]	4K to 300K	-55 to 125	-15 to 105	-10 to 90
3σ error [°C] (Trim point)	$+0.5/-0.3$	$\pm 1.4(0)$ $\pm 0.6(1)$	+1.5/-2.0 (0)	$\pm 2.0(0)$ $\pm 0.9(1)$
Power [uW]	21.9	2.2	18	33.75
Tconv[ms]	0.044	6.4	0.013	0.1
Res. [mK]	100	15	300	10.2
Res. FoM* $[pJ \cdot K^2]$	9.6579	3.1	21	0.36

Table 4.3: Performance Summary and Comparision

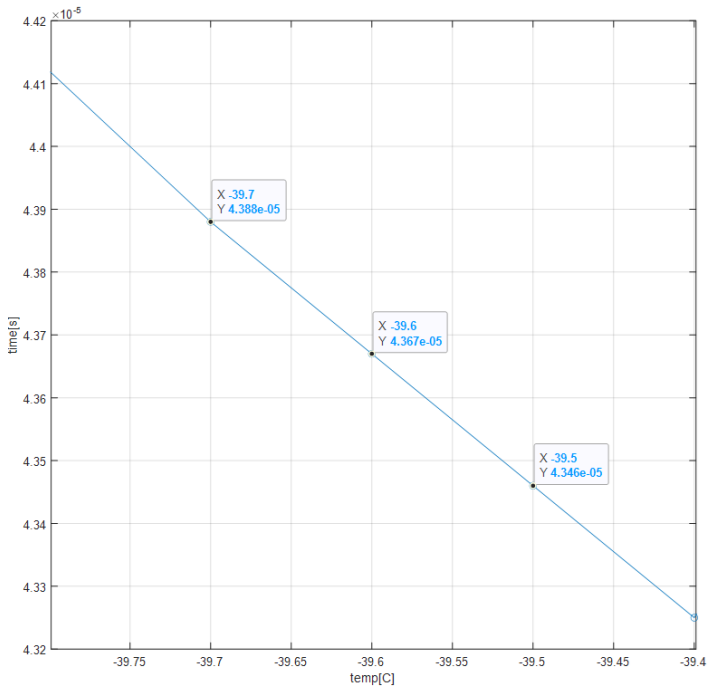

Figure 4.22: Fine Readout Function Test with the overranging capacitor

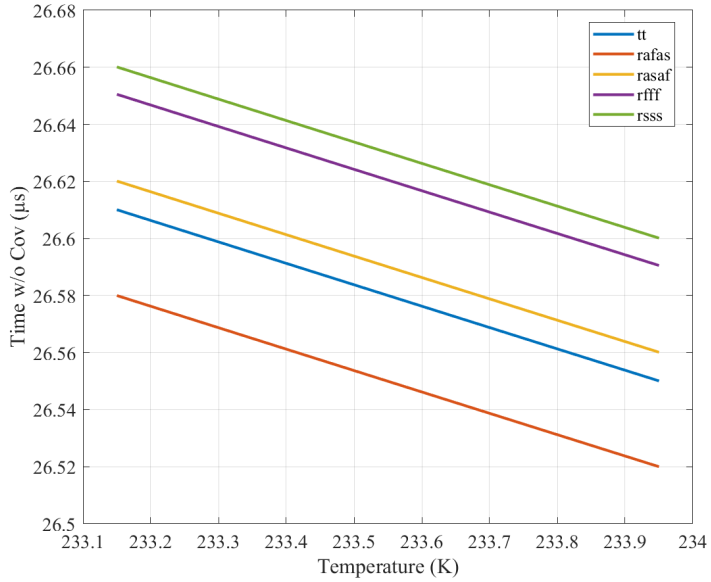

Figure 4.23: Process Spread without Cov

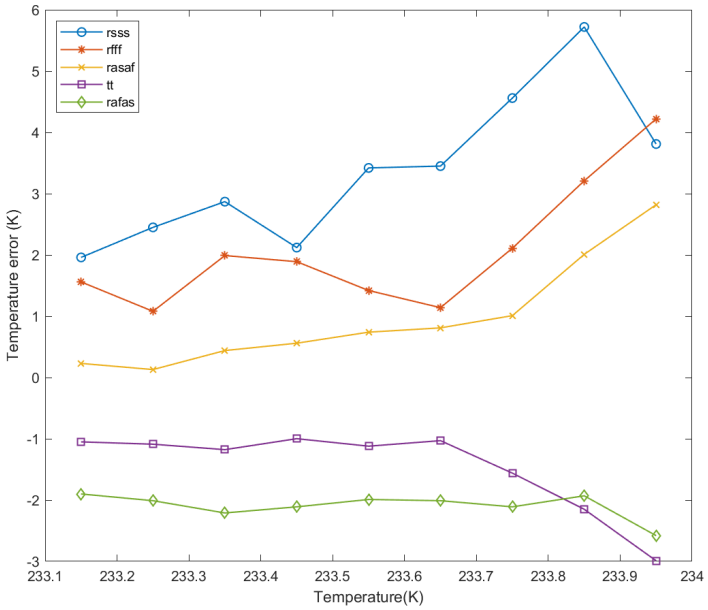

Figure 4.24: temperature error vs temperature without Cov

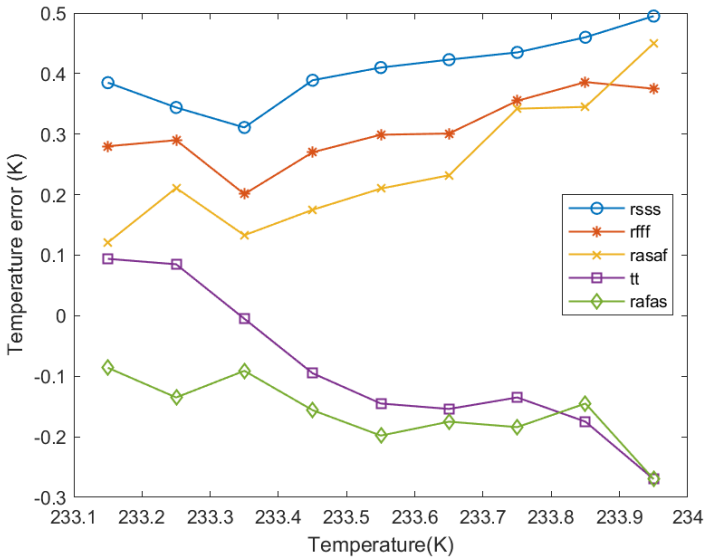

Figure 4.25: temperature error vs temperature with Cov

5. Conclusion and Future Work

5.1 Conclusion

This design presents the first FinFET-based temperature sensor capable of operating between 4K and 300K. The proposed temperature sensor overcomes the challenges of having no physical period or even temperature-dependent data. In this thesis, based on the existing diode current-voltage response characteristic curve, the possible performance of the target sensing element at cryogenic is obtained. Based on this, this thesis innovatively proposes a hybrid voltage-time domain readout scheme. At the same time, based on the proposed over-ranging technique, the temperature resolution can be effectively improved in any coarse range; the chopper-based technology can reduce the influence of device mismatch and comparator offset.

The proposed readout method is implemented by first reading the coarse voltage level by SAR ADC, and then based on the exponential relationship of the sensing element time with temperature, it fully utilizes and amplifies this advantage, giving this temperature sensor topology a chance to read accurately over the full range of 4K to 300K.

The coarse simulation of the sensor is carried out in this design for the full range of room temperature functions from -40C to 27C, showing the correct functionaliy of the PTAT.

The effective effect of over-ranging in fine phase readout is quantified. The flexibility of the methodology and its scalability is demonstrated.

The design ultimately requires only 20uW and can even provide 0.3 degrees of accuracy based on over-ranging, which is a very competitive sensor even in the smart temperature sensor at room temperature.

5.2 Future Work

1. The design is planned to be taped out in November. All schematics are ready. The next step will be a full layout for a final tapeout.
2. The proposed hybrid voltage-time domain readout has many advantages such as flexibility, scalability. As long as characterization behaviour is obtained through the first generation, the circuit design can be optimized only for deep cryogenic temperatures.
3. The technique of over-ranging is just to provide more fault tolerance margins for fine phase time-domain readout, which can also be achieved by biasing the CB-D for longer time before the fine phase reading without employing extra capacitor bank.

Appendices

A. Appendix title

.1 Algorithm from 2.2.2

Algorithm 1 CB-D Analytical Model Built-Up

procedure CB-D MODELING(IV_data, temperature)
  log_data ← log(IV_data)
  if measured_minimum_voltage(log_data) $\gg nVT$ **then**
    diode_IV_equation ← simplified-IV-Eq
  else
    diode_IV_equation ← original-IV-Eq
  end if
  (n, Id) ← fit_data_to_model(log_data, diode_IV_equation)
  CB-D_model ← substitute_parameters_into_CB-D(n, Id, C_s)
  return CB-D_Ana_model
end procedure

Algorithm 2 CB-D Numerical Model Built-Up

procedure CB-D MODELING(IV_data, temperature)
  LUT ← Diode IV_data, temperature
  CB-D_model ← Model capacitor I-V Eq with LUT
  return CB-D_Num_model
end procedure

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