Three-level Gate Driver for Latching Current Limiter in DC Microgrid Protection

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***Abstract*—The development of DC protection systems is an enabler of widespread adoption of DC microgrids. This paper introduces a three-level gate driver that provides the latching current limiter functionality in a solid-state circuit breaker with unidirectional protection. The proposed gate driver combines the output port description of a well-known, enabled gate driver with a soft turn-off network. The corresponding circuit can be adapted to well-established SSCBs, requiring few modifications which could allow for quick development. The concept, simulation, implementation and experimental validation of the gate driver are in the scope of the paper. The gate driver is implemented and tested in a solid-state circuit breaker prototype, showing the potential to develop further DC protection devices.**

***Index Terms*—DC protections, current limiter, solid-state circuit breaker**

I. Introduction

The development of modern DC microgrids aims to integrate complex systems into a single entity [1]. Both academia and industry have invested significant resources to define requirements, bring these definitions into practice, and exploit the potential benefits. These benefits include simplified integration of alternative energy sources and storage systems, increased control flexibility, and improved overall energy management [2]. As the benefits of this technology become clearer, its deployment has expanded across multiple applications, from grid-connected and isolated land-based DC systems to satellites, covering virtually every transportation technology suitable for electrification [3]–[6]. However, the diversity of applications necessitates a range of hardware solutions, which complicates standardization efforts.

One of the most sensitive subsystems in the design and operation of a DC microgrid is its protection scheme. Selecting a specific protection scheme is critical when system availability is closely tied to personnel safety or mission success. Time discrimination, a well-known approach for achieving selectivity, serves as a baseline in protection schemes for transportation microgrids (e.g., shipping) [7]. This method segments the microgrid into several sectors, prioritizing power availability based on fault location, and forms the core of breaker-based protection [8], [9]. Although this approach is popular in many DC applications due to its similarities with legacy AC protection technologies, it requires hardware modifications and offers limited performance. In contrast, solid-state circuit breakers (SSCB) and latching current limiters (LCL) have been developed to address areas where traditional protection components are ineffective.

For instance, aerospace DC microgrids use LCLs to protect against faults and their transients [10], [11], while maritime applications often employ a combination of high-speed fuses, mechanical disconnectors, and solid-state circuit breakers [12], [13]. Implementing the complex protection systems required in aerospace or maritime DC microgrids can be challenging with legacy components. In some cases, solid-state solutions are preferred despite their complexity, additional auxiliary subsystems, and higher cost. Furthermore, SSCBs are sometimes used as direct replacements for their AC counterparts, resulting in devices that do not fully exploit their potential and may lack cost-effectiveness in certain scenarios.

LCLs, primarily used in DC microgrids for aerospace applications, employ gate voltage modulation (e.g., hiccup modulation) to control a power switch that ultimately limits the current [10]. One LCL design [14], features a complex architecture with separate control, telemetry, and logic blocks constructed using photolithography. However, its millisecond-scale response time and requirement for custom chips render it impractical. A simpler design in [10] still faces challenges in analog design and magnetic isolation, with response times in the hundreds of microseconds, while the conventional LCL in [15], intended for low-voltage subsystems, provides limited control details and a $2\,\mathrm{ms}$ response time. Space-rated, off-the-shelf solutions such as the *Microchip LX7712* [10], [11] require advanced control and measurement circuits, as illustrated in the simplified block diagram in Fig. 1, although such

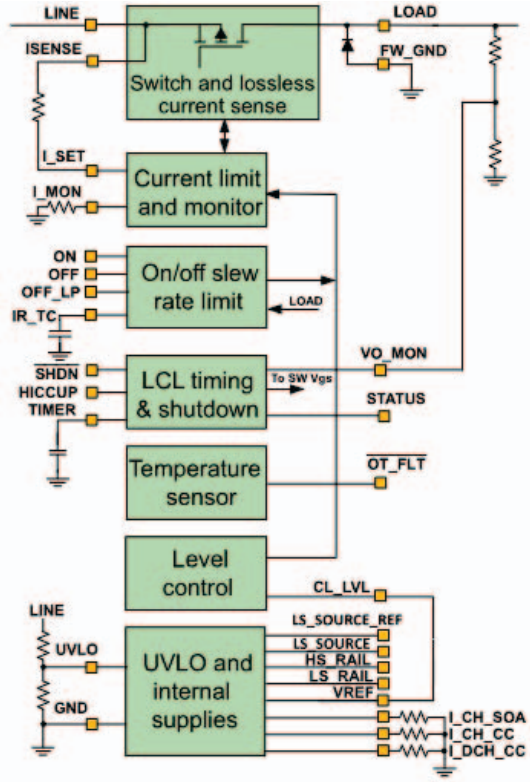

Fig. 1. LX7712 - Typical Power Switch System Programmable Current Limiting Power Switch For Space. *Extracted from [11].*

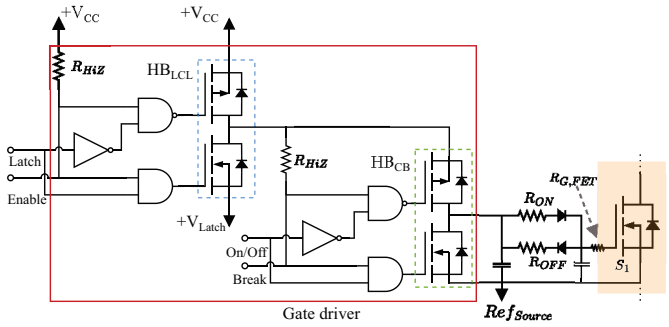

Fig. 2. Proposed three-level gate driver topology with soft turn-off network.

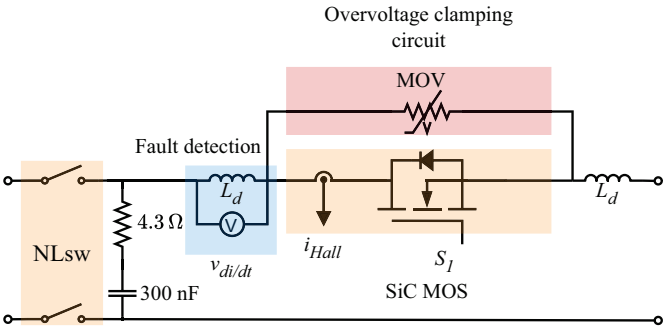

Fig. 3. Simplified schematic of a solid-state circuit breaker with unidirectional protection and bidirectional current flow.

features are often unnecessary for less demanding applications.

This work demonstrates a single-pole unidirectional SSCB that functions both as a circuit breaker and a latching current limiter with only minor modifications. The proposed three-level gate driver utilizes the SSCB's SiC MOSFET in the linear region to enable LCL functionality. The paper presents the concept, simulation, implementation, and experimental validation of this gate driver within a SSCB prototype. The proposed gate driver limits the to a safe level during temporary overloads, ensuring that the SSCB trips only when necessary (e.g., during solid short circuits). This strategy can significantly enhance the value of commercial SSCBs by improving both operational safety and system reliability in modern DC microgrids.

The remainder of this document is organized as follows. Section II discusses the gate driver topology and control logic, and includes relevant simulations; Section III covers the experimental validation; and Section IV presents the main conclusions.

II. Three-Level Gate Driver

The proposed gate driver integrates the output characteristics of a well-known enabled gate driver with a soft turn-off network. This section describes the three-level topology that enables the LCL in the SSCB, the required logic control, and the corresponding simulations.

A. Circuit Topology

Figure 2 illustrates the cascaded circuit topology used to achieve the three-level gate voltage. The LCL half-bridge (HB_{LCL}) serves as the power supply for the circuit breaker half-bridge (HB_{CB}), which ultimately drives the power switch S_1. HB_{LCL} is supplied with $+V_{CC}$ at the positive port, delivering the normal gate voltage to S_1. The low-side voltage applied to HB_{LCL} determines the latching voltage, as defined by (1), where V_{th} represents the threshold voltage of S_1.

$$+V_{CC} > +V_{Latch} > V_{th} \tag{1}$$

A high-impedance resistor (R_{HiZ}) prevents unintended gate signal activation when current limiting is disabled or the breaker is tripped. The soft turn-off network enhances the SSCB's dynamic performance during turn-off, reducing voltage ringing. Additional details can be found in [16], [17].

Figure 3 depicts the single-pole SSCB with unidirectional protection used in this study. The no-load switch (NLsw), shown in yellow, provides galvanic isolation after the SiC MOSFET interrupts current flow. An adjacent RC circuit modifies transient short-circuit characteristics to improve selectivity [16]. The series inductance L_d (blue) helps dampen the di/dt surge following a fault [18]. Monitoring the voltage across L_d enables high-speed short-circuit detection [19]. A metal-oxide varistor (MOV), highlighted in red, prevents voltage surges by acting as a resistor when the clamp voltage is reached. A Hall-effect sensor enables instantaneous current measurement

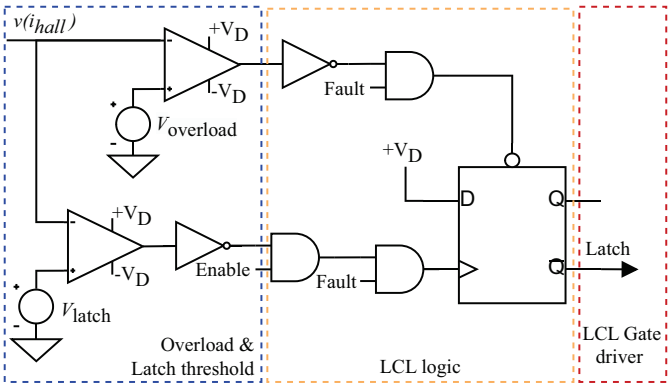

Fig. 4. Latching current limiter gate driver control stage. *Blue:* Rail-to-rail comparators and references, *yellow:* D-latch-based LCL logic, *red:* gate driver input signal.

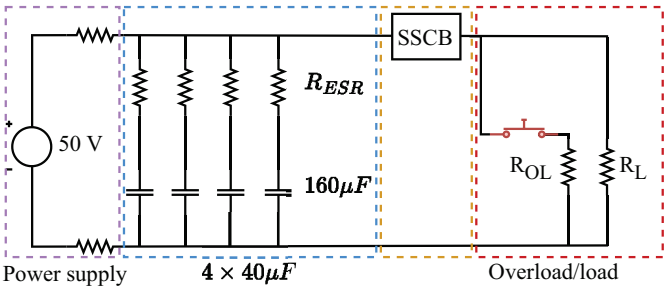

Fig. 5. Simplified schematic of the testing circuit incorporating the solid-state circuit breaker that features the three-level gate driver. *Purple:* power supply, *blue:* output filter capacitors, *yellow:* Solid-state circuit breaker with LCL, *red:* Load and overload resistances.

in series with the SiC MOSFET, supporting the breaking and LCL functions.

B. Latching current limiter control

The LCL operates independently from the circuit breaker's short-circuit logic. Several essential parameters must be defined based on the SSCB's characteristics and intended function.

- **Nominal current:** Rated current in normal operation.
- **Overload factor:** Maximum allowable overload current factor for a predefined duration.
- **LCL time:** Maximum acceptable accumulated time with active LCL.

These parameters form the basis of the LCL logic, illustrated in Fig. 4, which utilizes a D-latch. The measured current $v(i_{hall})$ compared against two reference set points, $v_{overload}$ and v_{latch}, where $v_{latch} > v_{overload}$, to classify the device's state as normal, overload, or overcurrent. These conditions are governed by (2a) to (2c).

$$i(t)\begin{cases} Nominal, & i(t) < I_{nom} \quad (2a) \\ Overload, & 1.2I_{nom} > i(t) > I_{nom} \quad (2b) \\ LCL, & i(t) \geq 1.2I_{nom} \quad (2c) \end{cases}$$

In this design, the LCL triggers when $i(t)$ exceeds $1.2I_{nom}$,where 1.2 represents the overload factor. This means $v(i_{hall}) > v_{latch}$, prompting an increase in the SiC MOSFET's channel resistance, which reduces $i(t)$. The LCL resets once $v(i_{hall})$ drops below $v_{overload}$, allowing $i(t)$ to return to nominal levels. This cycle repeats until the overcurrent condition is cleared or the LCL time is exceeded. To ensure proper operation, V_{latch} and $V_{overload}$ detection circuits must have similar propagation delays when connected to the D-latch. The external signal denoted as *Fault* is normally on indicating the breaker's status, whereas the Enable signal is also normally on and must be manually activated by the user or controller.

C. Operation simulation

The LCL functionality was simulated in LTSpice to validate its operation. The SSCB in Fig. 3, incorporating the three-level gate driver from Fig. 2, was tested usign the circuit in Fig. 5. The simulation was performed in two stages. 1) Validate the three-level gate driver operation and 2) confirm proper LCL functionality and control. Table I summarizes the implementation and simulation parameters. The maximum temperature rise follows *manufacturer recommendations* to keep a temperature margin of at least 20 K under the maximum of the component. In this case, the assumed ambient temperature is 45 °C. The maximum number of LCL cycles was estimated by extrapolating the temperature rise per cycle, determined by power losses in each cycle.

TABLE I
SSCB DESIGN PARAMETERS FROM THE PROPOSED DESIGN GUIDELINES.

Parameter	Value
Overload factor	1.2
Dampening inductance L_d	0.47 µH
Dampening capacitor	300 nF
Dampening resistance	4.3 Ω
On resistance R_{ON}	4.64 Ω
Off resistance R_{OFF}	9.28 Ω
LCL threshold	3.2 A
LCL maximum temperature rise	25 K
Maximum LCL cycles	22957000
Maximum LCL time $t_{LCL,max}$	22.7 s
Actual LCL time	20 µs
LCL delay*	250 ns
Commercial gate Driver	IXYS IXDD609SI
SiC MOSFET	Infineon IMW120R040M1H
High-speed D-Latch	TI SN74AHCT74DR

* Measured value

1) Three-level gate driver as LCL: Reducing the gate voltage to a preset V_{Latch} forces the SiC MOSFET into the linear region. According to (3), v_{GS} influences the semiconductor's parasitic capacitance, requiring charge removal to reach this state.

$$C_{gs} = \frac{Q_{gs}}{V_{GS}} \quad (3)$$

Figure 6 illustrates current paths during one LCL cycle and their impact on v_{GS}. Initially, v_{GS} (blue) is at $+V_{CC}$, requiring minimal on-state current for the power switch. When the LCL command (red) switches to logic one, a current overshoot occurs through the low-side switch of HB_{LCL} (dashed red), which is connected to $+V_{Latch}$.

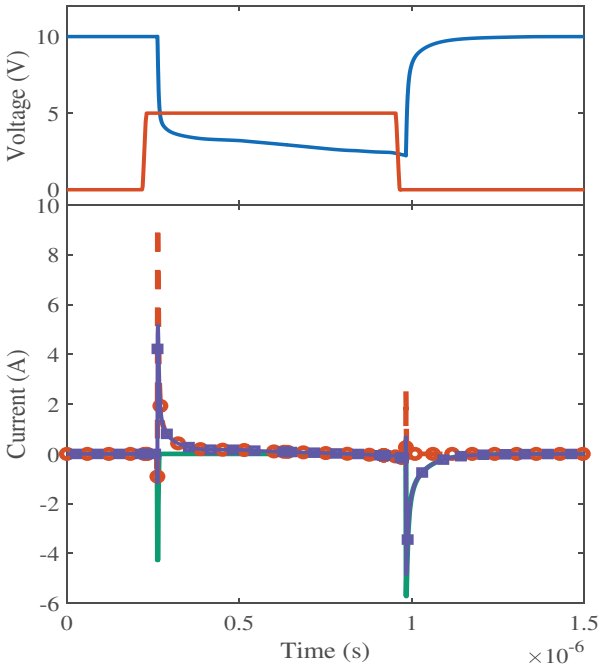

Fig. 6. Simulation of the gate driver current signals during one latching current limiting cycle, *top-blue:* gate-source voltage, *top-red:* LCL signal command, *bottom-green* current through the upper switch in HB_{LCL}, *bottom-red* current through the lower switch in HB_{LCL}, *bottom-purple* current through upper switch in HB_{CB}.

The simulation also shows a minor current undershoot through the top-side switch of HB_{LCL} (green), primarily due to turn-off processes, which are negligible. The top-side switch current in HB_{CB} (purple) follows a waveform similar to the low-side switch of HB_{LCL}, remaining active during the LCL operation. Upon LCL reset, a complementary effect is observed. The top-side switch of HB_{LCL} has a small current overshoot, while its low-side switch shows a clear undershoot. This confirms that the gate current direction changes during LCL operation, leading to the steady ramp-down of v_{GS} after the initial step-down.

2) LCL operation: This section further examines the role of the three-level gate driver in SSCB operation as an LCL. Fig. 7 presents simulated LCL cycles, controlled by the proposed gate driver. The current (blue) surpasses the LCL threshold of 3.7 A triggering the LCL command signal (green) after a delay of approximately 310 ns, followed by a drop in v_{GS} (yellow). The current initially continues to rise, peaking at around 4.7 A, before sharply decreasing due to increased resistance. When the current falls below 3.5 A, the system exits the overcurrent state, resetting the latch and restoring v_{GS} to normal. The simulation model accounts for the system line inductance, estimated at approximately 8.32 µH. This explains the substantial current oscillations and their rising characteristics observed during operation.

III. Experimental Validation

The three-level gate driver in Fig. 2 and its corresponding control (Fig. 4) were integrated into the SSCB (Fig. 3) for validation using the test circuit shown in Fig. 5. The prototype, visible in Fig. 8, consists of three boards. The gate drive board (blue), the LCL controller and safety board (red), and the SSCB power board (green). The experimental tests aimed to verify the functionality of the proposed gate driver and LCL controller by analyzing LCL operation. Fig. 9 presents the experimental validation results, showing the latching command signal (green), v_GS (yellow), and output current (blue). The test was conducted using a 50 V DC power supply and the current limit was set at 3.1 A. As observed in Fig. 9, when the LCL threshold is exceeded, the command signal switches to logic zero, causing the gate driver voltage to drop to $+V_{Latch}$. This, in turn, forces a current reduction, eventually restoring the command signal to logic one and resetting the latch, as expected from the designed logic.

The experimental results in Fig. 9 closely align with the

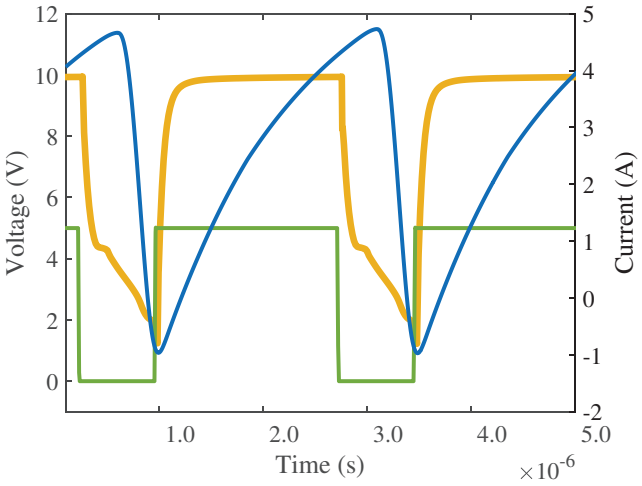

Fig. 7. Simulation of the latching current limiter functionality by using the proposed three-level gate driver. *Green:* LCL signal command, *yellow:* Gate-source voltage, *blue:* circuit breaker current.

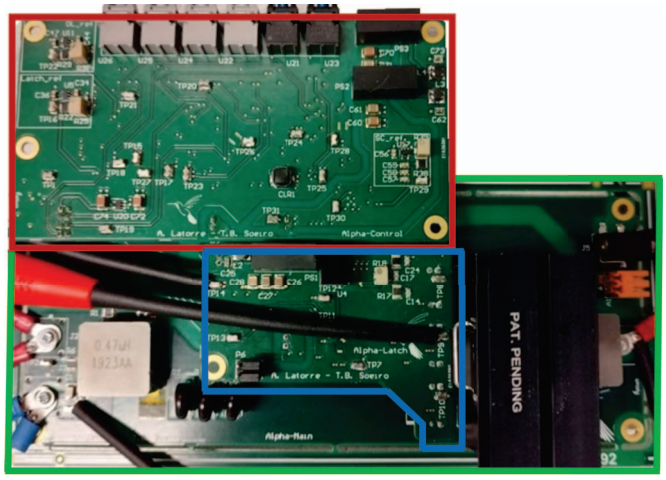

Fig. 8. Implementation of the solid-state circuit breaker with latching current limiter using the three-level gate driver. *Green:* Power board, *red:* control board, *blue:* three-level gate driver board.

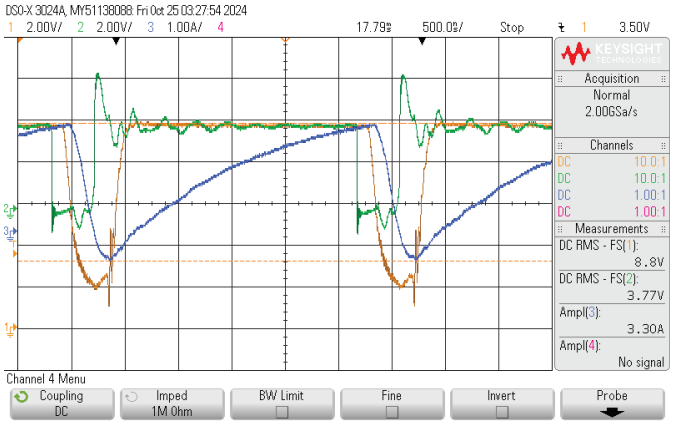

Fig. 9. Experimental results of the latching current limiter functionality by using the proposed three-level gate driver. *Green:* LCL signal command, *yellow:* Gate-source voltage, *blue:* circuit breaker current.

simulation results in Fig. 7. Some quantitative discrepancies are attributed to variations in impedance characterization, measurement constraints, and circuit limitations. The experiment recorded a peak current of 3.3 A with a propagation delay of approximately 250 ns. Both simulation and experimental data indicate that the current rise time is about 1 µs, mainly due to circuit and damping inductance effects.

To anticipate component failure, power losses in the SiC MOSFET during LCL cycles were estimated. However, no signs of immediate semiconductor degradation were observed in the experiments, given the selected components and test conditions. Additionally, as a precaution for exploratory studies, the LCL controller was programmed to interrupt and interlock the LCL after 20 µs, ensuring a conservative test.

IV. Conclusion

This paper presented a three-level gate driver designed for DC protection devices, which was successfully validated through experimental testing. The proposed approach enables the integration of latching current limiter functionality into existing solid-state circuit breakers with minimal modifications, making it adaptable to a wide range of DC applications. By combining current limiting and circuit breaking capabilities, the gate driver transforms SSCBs into multifunctional protection devices. The LCL adds meaningful value with low added complexity, enhancing SSCBs beyond mere replacements for traditional AC breakers. Importantly, the proposed solution can be implemented using off-the-shelf components, requiring only careful PCB layout, and no specialized hardware is needed. Future work will focus on refining the implementation guidelines and investigating long-term reliability, particularly the impact of repeated LCL cycling on SiC MOSFETs. The current scalability and the effects of LCL for high power DC systems must be investigated further.

Acknowledgments

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