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Yousefzadeh, Bahman; Makinwa, Kofi A.A.

DOI
10.1109/ISSCC.2017.7870311

Publication date
2017

Document Version
Final published version

Published in
2017 IEEE International Solid-State Circuits Conference, ISSCC 2017

9.3 A BJT-Based Temperature Sensor with a Packaging-Robust Inaccuracy of ±0.3°C (3σ) from -55°C to +125°C After Heater-Assisted Voltage Calibration

Bahman Yousefzadeh, Kofi A. A. Makinwa

Delft University of Technology, Delft, The Netherlands

This paper presents a BJT-based temperature sensor, which can be accurately trimmed in both ceramic and plastic packages, on the basis of purely electrical measurements at room temperature. This is achieved by combining the voltage-calibration technique from [1] with an on-chip heater, which can heat the sensing BJTs from room temperature to ~85°C in 0.5s. Measurements show that the sensor can then be trimmed to an inaccuracy of ±0.3°C (3σ) over the military range (–55 to +125°C). This is similar to the inaccuracy obtained after conventional *temperature calibration*, i.e., at well-defined temperatures, but requires much less calibration time and infrastructure.

A block diagram of the sensor is shown in Fig. 9.3.1. As in [2,3], an ADC is used to digitize the ratio $X_S = V_{BE}/\Delta V_{BE}$, where ΔV_{BE} is the difference in the base-emitter voltages of two BJTs biased at a fixed collector-current ratio p. In this design, p = 5 and so $\Delta V_{BE} = (\eta kT/q)\cdot\log(5)$, where η is the BJT's non-ideality factor. The use of dynamic techniques such as chopping and DEM ensures that the ADC's equivalent errors are negligible compared to BJT spread [2,3]. The ratio X_S can be converted into a linear function of temperature $\mu = \alpha/(\alpha+X)$, where α (~16) is a fitting parameter, after which the temperature can be expressed as $T_S = A\cdot\mu + B$, where A and B are also fitting parameters [2].

The accuracy of BJT-based sensors is limited by systematic variations in V_{BE} due to process spread and packaging stress [1-4]. This can be mitigated by *batch calibration*, during which the average values of A, B and α are determined by calibrating several samples at a number of known temperatures. Individual sensors can then be calibrated at one temperature and then trimmed by adjusting V_{BE} in a PTAT manner, e.g., by adding an offset to X_s [3]. Measurements on 20 samples packaged in ceramic (DIL-20) show that this results in ±0.1°C (3σ) inaccuracy over the military range (Fig. 9.3.2 (top)).

Compared to ceramic packages, plastic packages cause significantly more die stress, which, in turn, causes non-PTAT shifts in V_{BE} [4–6]. When the same "ceramic" fitting parameters are used, individual PTAT trimming of 20 samples packaged in plastic (SO-20) only leads to ±0.6°C (3σ) inaccuracy over the military range, (Fig. 9.3.2 (top)). This can be reduced to ±0.25°C (3σ) with new "plastic" fitting parameters obtained by a new batch calibration (Fig. 9.3.2 (bottom)). However, the need for a package-specific batch calibration followed by the temperature calibration of packaged devices (with minute-long thermal time constants) is logistically complex and time consuming, and so significantly increases manufacturing costs. Alternatively, die coatings can be used to reduce packaging stress [4], but this also increases cost.

Voltage calibration (VCal) has been used as a low-cost alternative to temperature calibration [1,2]. It exploits the fact that ΔV_{BE}, unlike V_{BE}, is robust to process spread and packaging stress and so can be used as an accurate measure of die temperature. VCal only requires electrical measurements and does not require a temperature-stabilized environment, making it well suited to volume production.

As shown in Fig. 9.3.1, VCal involves two ADC conversions. First, the ADC converts $X_s = V_{BE}/\Delta V_{BE}$, and second, it converts $X_{cal} = V_{ext}/\Delta V_{BE}$, where V_{ext} is a known external voltage. Die temperature (T_{cal}) can then be calculated from X_{cal}. Each conversion only lasts 20ms, and so T_{cal} can be assumed to be constant. As shown in Fig. 9.3.3 (top), the measured inaccuracy of VCal is less than ±0.1°C from 5 to 100°C in both packages, which agrees well with the 0.05°C error reported in [2]. The combination of package-specific batch calibration and low-cost VCal results in ±0.3°C (3σ) inaccuracy over the military range (Fig. 9.3.3 (bottom)), which is about the same as with temperature calibration (Fig. 9.3.2 (bottom)).

In this work, we propose a two-point calibration scheme, in which VCal is performed at room temperature and at an elevated temperature created by an on-chip heater. From this information, the fitting parameters A and B can be adjusted to correct for the effects of packaging stress. Due to its extensive use of dynamic techniques (e.g., CDS, chopping and DEM), the ADC is quite robust to on-chip temperature gradients, and so only the sensor's temperature-sensitive elements are heated, i.e., the BJTs and R_b, which sets their bias current. This can be done with a single heater, in contrast to [7], which used multiple heaters to minimize on-chip gradients during the calibration of a frequency reference. As shown by COMSOL simulations, however, the on-chip gradients under a small heater are quite large (Fig. 9.3.4). To mitigate their effect, a gradient-insensitive BJT layout is used, around which R_b is placed.

The sensor occupies 0.17mm² in 0.16µm CMOS (Fig. 9.3.7), and draws 4.6mA from a 1.8V supply. It achieves 7.5mK (rms) resolution in a 20ms conversion time. Prior to VCal, V_{ext} (=0.65V), is calibrated by a Keithley 2002A voltmeter. The 17Ω heater is implemented in metal 2 and occupies 0.017mm². Its terminals are connected to unprotected pads, thus allowing it to be safely pulsed by a 0.2A current (~0.7W) during VCal.

Measurements show that the heater can heat the BJTs from room temperature to ~85°C in less than 0.5s (Fig. 9.3.5 (top)), enabling a fast 2-point calibration. Rather than waiting several seconds for complete settling, two-point interpolation is used to rapidly estimate the die temperature T_S at which the X_S (=V_{BE}) conversion is made. This involves averaging T_{cal} before and after each X_s conversion. T_{cal} measurements made at 40ms intervals show that the resulting error is already less than 25mK (rms) after 0.5s (Fig. 9.3.5 (bottom)). With the heater on, however, a systematic PTAT error (~1.5°C at 85°C) is still observed between T_{cal} and T_S. This is probably due to the temperature gradient under the heater, which causes a systematic temperature difference between R_b and the BJTs, and thus causes a bias current shift. Being PTAT, this error is corrected by adding a fixed offset to X_S when the heater is on.

The results obtained after two-point heater-assisted VCal are shown in Fig. 9.3.6 (bottom) for both ceramic and plastic packages. The entire calibration takes less than a second, and after trimming, results in ±0.3°C (3σ) inaccuracy over the military range. This is comparable with the results obtained after two-point VCal at 25°C and 85°C in a temperature-stabilized oven (Fig. 9.3.6 (top)). It is also comparable with the results obtained after a package-specific batch-calibration followed by an individual voltage calibration (Fig. 9.3.3 (bottom)). Compared to VCal alone, heater-assisted VCal thus eliminates the need for batch calibration in the trimming of BJT-based temperature sensors.

Acknowledgements:
The authors would like to thank NXP semiconductors for chip fabrication, and Robert Van Veldhoven and Sha Xia (NXP) for their support.

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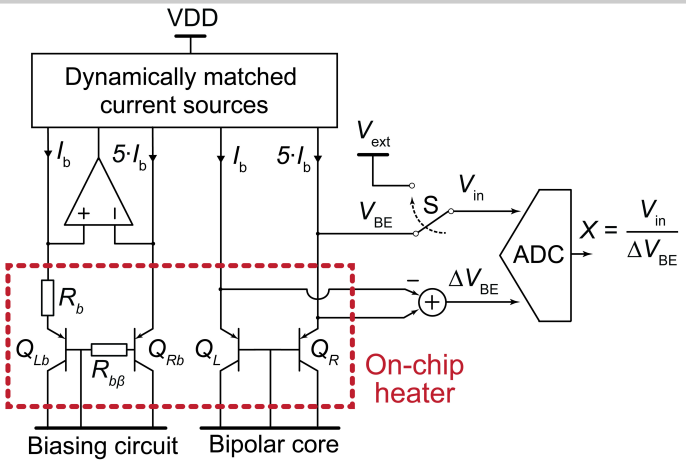

Figure 9.3.1: Sensor's operation, and heater-assisted voltage calibration. Biasing circuit generates a PTAT current ($I_b = \Delta V_{BE}/R_b$), which biases the sensing PNPs in Bipolar core. The indicated state of the switch (S) represents the normal mode of the temperature sensor.

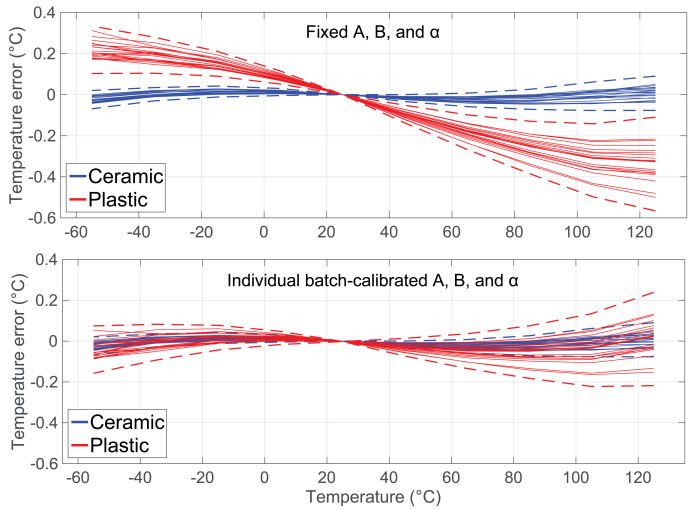

Figure 9.3.2: (Top) Measured inaccuracy after temperature calibration, with fixed fitting parameters, (Bottom) and with package-specific fitting parameters.

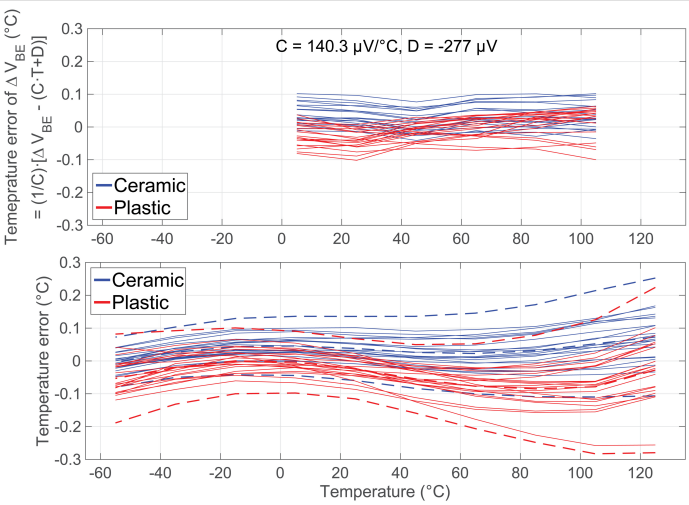

Figure 9.3.3: (Top) Measured inaccuracy associated with ΔV_{BE}. (Bottom) Measured inaccuracy after voltage calibration (at room-temperature), using package-specific fitting parameters.

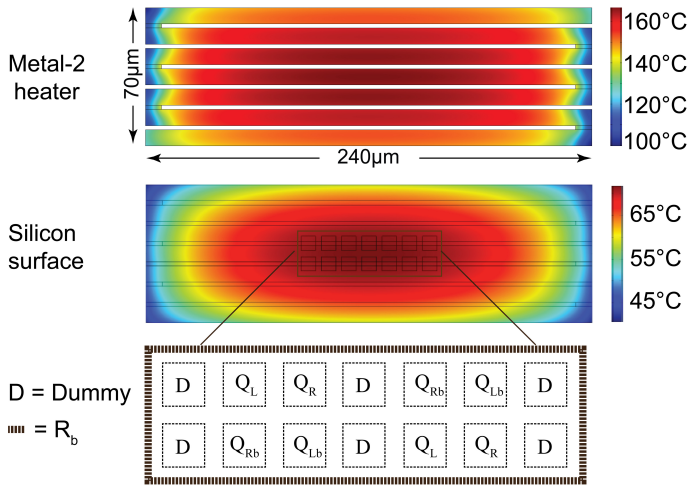

Figure 9.3.4: Simulated temperature gradient at steady-state, for 1A heater current, and gradient insensitive lay-out.

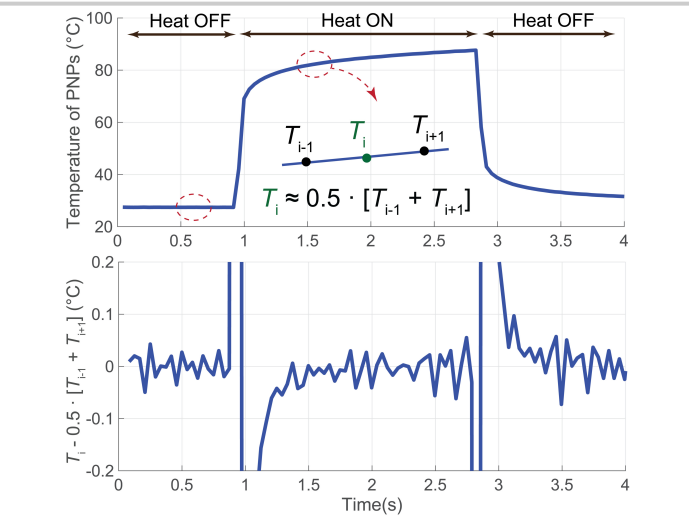

Figure 9.3.5: (Top) Measured die temperature, as a result of 2s exposure to heat (0.2A in the metal heater). (Bottom) Measured temperature error of T_{cal} interpolation.

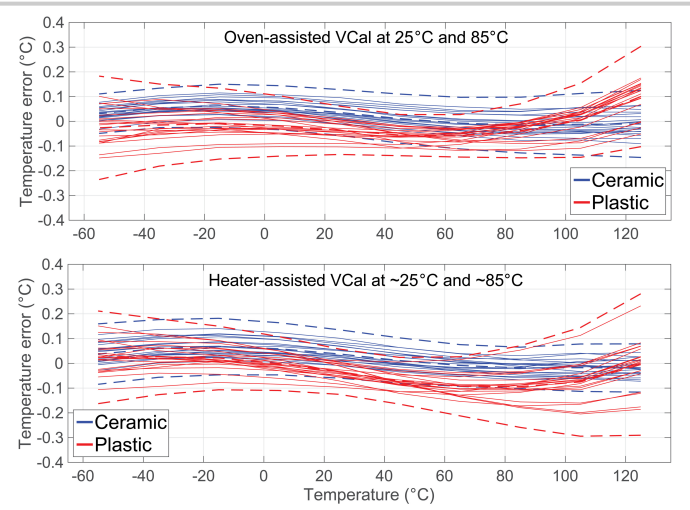

Figure 9.3.6: (Top) Measured inaccuracy after 2-point VCal in a stabilized oven. (Bottom) Measured inaccuracy after 2-point VCal with the on-chip heater. Dashed lines represent average and ±3σ bounds.

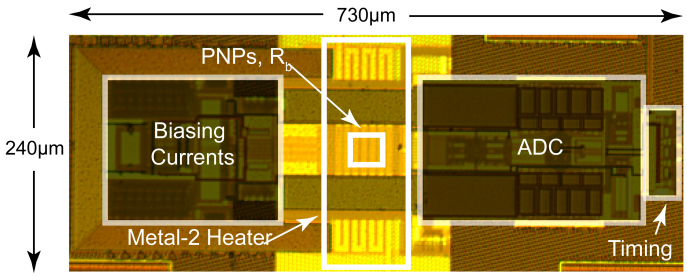

Figure 9.3.7: Chip micrograph.

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