A Compact Sub-1V Capacitively Biased Temperature Sensor in 65nm CMOS

By

Geng Chen

Supervisors:

Prof. dr. K. A. A. Makinwa

In partial fulfilment of the requirements for the degree of

Master of Science

In Electrical Engineering

At Delft University of Technology

Faculty of Electrical Engineering, Mathematics and Computer Science

To be defended on Month December 2025

Student Number: 5947278

Thesis Committee:

Prof. dr. K. A. A. Makinwa

Dr. D. G. Muratore

TU Delft Delft University of Technology

Abstract

In this thesis, a low-power, sub-1V, high-accuracy capacitively-biased-diode (CBD) based temperature sensor with excellent Power Supply Sensitivity (PSS) in a 65 nm LP process is proposed. The sensor consists of two main parts: a CBD front-end and a Delta-Sigma Modulator (DSM). The CBD front-end discharges the pre-charged capacitors via diode-connected BJTs to generate accurate proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) voltages. The ratio of these voltages is then digitized by a second-order switched-capacitor DSM, which employs energy-efficient inverter-based amplifiers capable of operating from a sub-1V supply. After a one-point temperature calibration, the BJT-based sensor achieves a simulated inaccuracy of ± 0.2℃ (3σ) over the temperature range from -55°C to 125°C. Over the entire temperature range, the BJT-based sensor achieves a PSS of 0.05℃/V from 0.9V to 1.4V. Compared to previous CBD-based temperature sensors, this design achieves $10\times$ better PSS.

Acknowledgements

The past two years have been a period of significant personal and academic growth. Looking back, I realize that this thesis would not have been possible without the support, patience, and encouragement of many people. Here, I would like to express my sincere gratitude to everyone who accompanied me throughout this journey.

First and foremost, I would like to express my deepest and most sincere gratitude to my supervisor, Prof. Dr. Kofi Makinwa. I am truly thankful for the opportunity he gave me to work on this project, as well as for the trust he placed in me throughout the entire process. His patient guidance and timely support helped me navigate the most difficult stages of the research, and his high standards continually encouraged me to grow. I am especially grateful for the academic exposure he provided, including the chance to attend conferences and observe the work of leading researchers in the field. Despite his busy schedule, he always took the time to teach me with great patience, and the lessons I learned from him—both in research and in how to conduct myself—will continue to benefit me in the future. Being part of this group under his supervision has been an inspiring and invaluable experience that I will always carry with me.

I would also like to express my sincere gratitude to my daily supervisors, Jida Peng and Nandor Toth, for their continuous support and guidance throughout this project. Their patience, clear explanations, and timely help allowed me to overcome many difficulties along the way. I truly appreciate the time they devoted to my work and everything I learned from them.

I would also like to thank Dr. Dante Muratore for taking the time and interest to serve as a member of my Thesis Committee. I truly appreciate his willingness to review my work and provide valuable feedback.

I am also grateful to the members of the EI group for the discussions, shared meals, and the many days and nights we worked through together. My sincere thanks go to Karimeldeen, Xiao, Sundeep, Alireza, and Floris for their help during my thesis, and to my peers Harland, Traian, Xujie, and Yi Mao for creating a supportive and energetic environment in the office.

I would like to express my profound love and heartfelt gratitude to my girlfriend, Sherry, for her constant love and support throughout this journey. During the most challenging moments, she brought me warmth, patience, and encouragement, making my life in the Netherlands feel far less lonely. Her presence gave me strength and comfort when I needed them the most, and I am truly grateful for everything she has done for me.

Finally, I would like to express my deepest gratitude to my family for their unconditional love, trust, and support. Their encouragement has always been my strongest source of strength, and their belief in me gave me the courage to pursue every step of this journey. No matter the distance, their constant support accompanied me throughout my time abroad. I would not have reached this point without everything they have given me.

Contents

List of Figures

List of Tables

List of Abbreviations

ADC	Analog-to-Digital Converter
AZ	Auto-Zero
BJT	Bipolar Junction Transistor
BS	Bitstream
CBD	Capacitively-Biased Diode
CHL	Chopping Low-frequency
CMFB	Common-Mode Feedback
CTAT	Complementary-To-Absolute-Temperature
DEM	Dynamic Element Matching
DSM	Delta-Sigma Modulator
DTMOST	Dynamic-Threshold MOSFET
EA	Error Amplifier
ETF	Electro-Thermal Filter
FE	Front-End
FoM	Figure of Merit
GBW	Gain Bandwidth Product
LDO	Low-Dropout Regulator
MIM	Metal-Insulator-Metal
OTA	Operational Transconductance Amplifier
PSS	Power Supply Sensitivity
PTAT	Proportional-To-Absolute-Temperature
RCP	Regulated Charge Pump
RIA	Relative Inaccuracy
RTD	Resistance Temperature Detector
SoC	System-on-Chip
VBE	Base-Emitter Voltage
VDD	Supply Voltage
VGS	Gate-Source Voltage

1 Introduction

Temperature is one of the most frequently measured physical quantities, as it affects the behavior of almost all biological, chemical, environmental, and physical systems. Traditionally, temperature has been measured using thermocouples, thermistors, and resistance temperature detectors (RTDs). In recent decades, advances in semiconductor technology have enabled the development of silicon-based temperature sensors. Such on-chip sensors are now widely integrated into microprocessors and other ICs for thermal monitoring.

With the rapid growth of IoT applications, temperature sensors face increasing performance requirements. They must provide high accuracy across a wide temperature range and operate with ultra-low power consumption, since they are often powered by small batteries or energy-harvesting units. Moreover, in advanced sub-65 nm CMOS technologies, sensors must operate from sub-1 V supplies. In modern SoCs that adopt dynamic voltage scaling for thermal management, low power-supply sensitivity (PSS) is also essential.

1.1 Types of CMOS temperature sensors

In CMOS technology, several devices exhibit temperature-dependent behavior and so can be used for temperature sensing, such as bipolar junction transistors (BJTs), resistors, electro-thermal filters (ETFs), and MOSFETs. The best choice usually depends on the trade-offs between accuracy, power consumption, power-supply sensitivity, supply-voltage headroom, and calibration cost.

BJTs are widely used in precision temperature sensors and in bandgap references. When a BJT is biased at a constant current, its base-emitter voltage V_{BE} exhibits CTAT behavior, while the base-emitter voltage difference between two BJTs biased at different current densities, ΔV_{BE}, is PTAT. By combining these two voltages, a temperature-dependent output can be generated. After a low-cost one-point calibration, state-of-the-art BJT-based sensors can achieve a 0.10°C (3σ) accuracy from −70°C to 125°C, corresponding to a relative inaccuracy (RIA) of 0.11%, with a PSS as low as $0.025°\mathrm{C}/V$, and a minimum supply voltage of 1.4 V [4].

Resistor-based sensors make use of the intrinsic temperature coefficient of on-chip resistors. With relatively high sensitivity (typically around 0.3°C/V) in a Wheatstone-bridge configuration, they offer excellent energy efficiency and can support sub-1 V supply operation [5]. However, they typically require multi-point calibration to achieve high accuracy, which increases production cost. Recent designs report an accuracy of 1°C (3σ) from −55°C to 125°C, corresponding to an RIA of 0.56% after one-point trim [6]. With two-point trimming, this improves to 0.03%.

ETF-based sensors rely on the well-defined thermal diffusivity of silicon. In these sensors, a heater generates thermal pulses, and a thermopile placed at a fixed distance s measures the resulting delay, which appears as a temperature-dependent phase shift. Because the accuracy is primarily determined by lithographic precision, high absolute accuracy can be achieved without trimming. A state-of-the-art design reports a ±0.20°C (3σ) error from −55°C to 125°C [7], corresponding to a RIA of approximately 0.2%. ETF sensors can

also operate below 1 V [8], although their energy efficiency is limited by the low thermopile sensitivity and the relatively high heater power required.

MOSFETs biased in the subthreshold region can be used as an alternative to BJTs because their current–voltage characteristics also follow an exponential temperature dependence. They support low-voltage operation since $V_{GS}(\approx 0.4\,\mathrm{V})$ is smaller than $V_{BE}(\approx 0.7\,\mathrm{V})$. However, their characteristics depend strongly on C_{ox} and V_{th}, which makes them more sensitive to process variations. As a result, MOSFET-based sensors usually show worse accuracy after one-point trimming. State-of-the-art designs report 0.3°C (3σ) accuracy from −20°C to 100°C, corresponding to an RIA of 0.45% after one-point trim [9]. With two-point trim, this improves to 0.13%, and the PSS can be as low as $0.02°\mathrm{C}/V$.

Considering the need for high accuracy after one-point trimming, low PSS and low power consumption, BJT-based temperature sensors are an ideal choice. However, operating them under a sub-1 V supply is still challenging. To address this limitation, the CBD technique introduced in [10] provides an effective solution.

1.2 Operating Principle of CBD

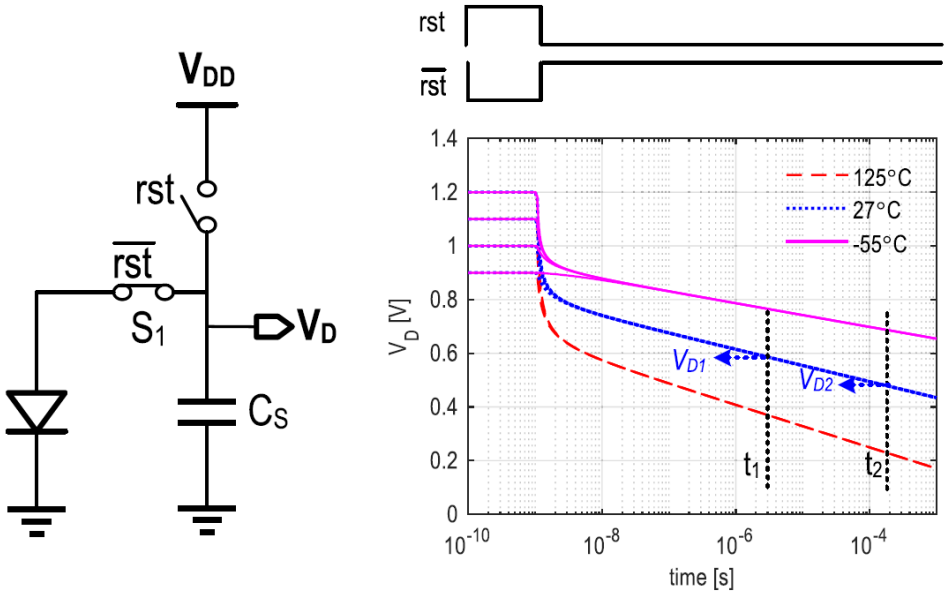


Figure 1: Working principle of the CBD technique [1].

As shown in Fig. 1, the CBD technique consists of two phases. In the first phase, a capacitor is precharged to V_{DD}. In the second phase, the capacitor is discharged through a diode. After a short time, the voltage across the capacitor becomes independent of the supply, due to the exponential discharge behavior. Sampling this voltage at time t_1 yields a CTAT value. Sampling again at a later time t_2 produces a second voltage, and their difference results in a PTAT term. With both CTAT and PTAT information, temperature can then be extracted in a manner similar to conventional BJT-based sensors.

In traditional temperature sensors, diode-connected BJTs are biased using current sources, which require additional voltage headroom (typically $> 0.4\,\mathrm{V}$). This limits their operation under low supply voltages. By replacing the current source with a charge-redistribution process, the CBD technique removes the need for such headroom, enabling sub-1 V operation.

1.2.1 Types of sensing diodes

As shown in Fig. 2, a diode is used as the sensing device in the CBD architecture. A diode-connected BJT or a diode-connected DTMOST can also serve as the sensing element, since all three devices exhibit similar exponential I–V characteristics.

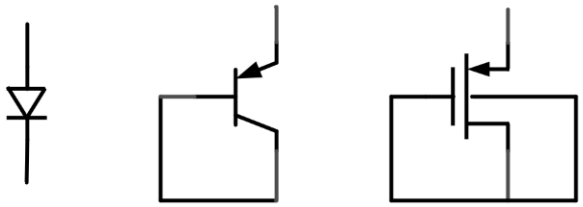


Figure 2: a) silicon diode; b) diode-connected BJT; c) diode-connected DTMOST.

Silicon diodes In the ideal case, assuming negligible carrier recombination in the depletion region, the diode I–V relationship is

$$I_D = I_S \left(\exp\left(\frac{qV}{kT}\right) - 1 \right) \tag{1.1}$$

where I_S is the saturation current, and V is the forward-bias voltage. Here, k is Boltzmann's constant, T is absolute temperature, and q is the electronic charge. When $V \gg kT/q$, the equation simplifies to:

$$V = \frac{kT}{q} \ln\left(\frac{I}{I_S}\right) \tag{1.2}$$

Since I_S is strongly temperature-dependent, the resulting voltage V exhibits a CTAT behavior. By biasing the diode at two different current densities, a PTAT voltage difference can be generated:

$$\Delta V = \frac{kT}{q} \ln\left(\frac{pI_1}{I_S}\right) - \frac{kT}{q} \ln\left(\frac{I_1}{I_S}\right) = \frac{kT}{q} \ln(p) \tag{1.3}$$

which ideally cancels I_S, making ΔV process-insensitive.

However, real diodes deviate from this ideal behavior. At low current densities, the recombination current dominates, whereas at high current densities, the diffusion current becomes dominant [11]. This results in a generalized I–V model

$$I_D = I_S \left(\exp\left(\frac{qV}{nkT} \right) - 1 \right), \tag{1.4}$$

where n is the ideality factor. When diffusion dominates, $n \approx 1$; when recombination dominates, $n \approx 2$. In the transition region, $1 < n < 2$, causing ΔV to depend on n and therefore on process variations [2]. This process dependence makes conventional silicon diodes unsuitable for high-accuracy temperature sensing.

Bipolar junction transistor The I_C–V_{BE} characteristic of a BJT follows the ideal exponential law much more closely than that of a silicon diode [2]. However, several nonideal effects still influence the collector current, such as carrier generation in the base–collector junction and minority carrier diffusion in the collector region. Using a diode-connected configuration, in which the base and collector are shorted, helps suppress these effects and makes the device behavior closer to the ideal model, with an ideality factor approaching 1.

The exponential I_C–V_{BE} relation can be expressed as:

$$I_C = I_S \left(\exp\left(\frac{qV_{BE}}{kT} \right) - 1 \right) \tag{1.5}$$

The PTAT voltage difference between two BJTs biased at current densities I_{C1} and pI_{C1} becomes:

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{pI_{C1} + I_S}{I_{C1} + I_S} \right) \tag{1.6}$$

If the collector current I_{C1} is chosen sufficiently larger than I_S, the saturation current term becomes negligible, yielding the well-known PTAT expression:

$$\Delta V_{BE} \approx \frac{kT}{q} \ln p \tag{1.7}$$

Similarly, the CTAT base–emitter voltage can be written as:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S} \right) \tag{1.8}$$

DTMOST When a MOSFET operates in the subthreshold region, the drain current I_D exhibits a quasi-exponential dependence on the gate–source voltage V_{GS}:

$$I_D \propto \frac{W}{L} \exp\left[\frac{q}{mkT} (V_{GS} - V_T^{\text{bulk}}) \right] \tag{1.9}$$

Here, $m = 1 + C_D/C_{OX}$ depends on the depletion-layer capacitance C_D and oxide capacitance C_{OX}. Both C_{OX} and the bulk threshold voltage V_T^{bulk} suffer from significant process variation and body-effect sensitivity [12], making MOSFET-based temperature sensors less accurate without trimming.

A more robust approach is to tie the gate and substrate together, forming a Dynamic-Threshold MOSFET (DTMOST) [13]. This configuration stabilizes the depletion region beneath the channel and yields a more predictable threshold voltage. The resulting current expression becomes:

$$I_D \propto \frac{W}{L} \exp\left[\frac{q}{kT}(V_{GS} - V_T^{\mathrm{DT}})\right] \tag{1.10}$$

Thus, a DTMOST diode exhibits a near-ideal exponential I–V relationship, with significantly reduced sensitivity to C_{OX}, C_D, and process spread compared to a bulk MOSFET. As a result, the process variation of V_{GS} in the DTMOST configuration is much smaller, making it attractive for temperature-sensing applications. Nevertheless, the spread of a DTMOST is still much larger than that of a BJT [14].

1.2.2 Temperature calculation

By forming an appropriate linear combination of V_{BE} or V_{GS} (CTAT) and ΔV_{BE} or ΔV_{GS} (PTAT), a reference voltage V_{ref} with a near-zero temperature coefficient can be generated. This is typically done by scaling ΔV_{BE} or ΔV_{GS} by a constant factor α such that the positive TC of $\alpha\Delta V$ cancels the negative TC of V_{BE} or V_{GS}:

$$V_{ref} = V_{BE} + \alpha\Delta V_{BE} \tag{1.11}$$

$$V_{ref} = V_{GS} + \alpha\Delta V_{GS} \tag{1.12}$$

As illustrated in Fig. 3, since ΔV_{BE} approaches zero at $T = 0\,\mathrm{K}$, the resulting V_{ref} for a BJT approaches the bandgap voltage of silicon ($\approx 1.2\,\mathrm{V}$). For a diode-connected DTMOST, V_{ref} is approximately $0.6\,\mathrm{V}$ [13], making it suitable for operation at lower supply voltages than BJT-based references.

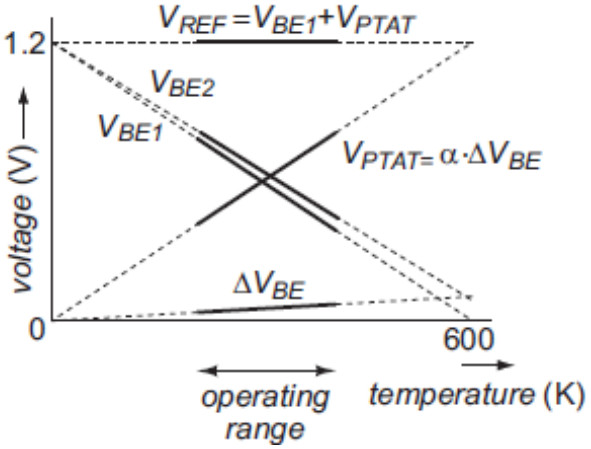


Figure 3: V_{ref} generation of a diode-connected BJT [2].

The readout ADC uses this reference voltage to normalize the PTAT voltage V_{PTAT}, producing a dimensionless output μ that is nearly linear with temperature:

$$\mu = \frac{V_{PTAT}}{V_{ref}} = \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}} \tag{1.13}$$

Finally, using fitting parameters A and B, μ can be mapped to the output temperature D_{out} in degrees Celsius:

$$D_{out} = A\mu - B \tag{1.14}$$

A similar transformation applies when using a DTMOST-based sensing core.

1.2.3 Capacitive Biasing

The voltage decay across a capacitor can be expressed as:

$$\frac{dQ}{dt} = C\frac{dV}{dt} \tag{1.15}$$

Combining (1.15) with the diode current relation in (1.4), the sampled voltage across the diode becomes [15]:

$$V = -n\frac{kT}{q} \ln \left[1 - \left(1 - \exp\left(\frac{-V_{DD}}{\frac{nkT}{q}} \right) \right) \exp\left(-\frac{I_S t}{\frac{nkTC}{q}} \right) \right] \tag{1.16}$$

where V_{DD} is the precharge voltage, n is the diode ideality factor, and t is the capacitor discharge time. For sufficiently long discharge intervals ($t \gg \frac{nkTC}{I_S q}$), the capacitor fully discharges to zero. For shorter intervals when ($t \ll \frac{nkTC}{I_S q}$), by using the first-order expansion, the exponential discharge-related exponent becomes:

$$\exp\left(-\frac{I_S t}{\frac{nkTC}{q}} \right) \approx 1 - \frac{I_S t}{\frac{nkTC}{q}} \tag{1.17}$$

Moreover, since typically $V_{DD} \gg \frac{kT}{q}$, (1.16) simplifies to the following form:

$$V = -n\frac{kT}{q} \ln \left[\exp\left(\frac{-V_{DD}}{\frac{nkT}{q}} \right) + \frac{I_S t}{\frac{nkTC}{q}} \right] \tag{1.18}$$

After a short discharge time $t \gg \frac{nkTC}{qI_S} \exp\left(-\frac{qV_{DD}}{nkT}\right)$, the first term becomes negligible compared to the second term, and the sampled voltage reduces to:

$$V \approx -n\frac{kT}{q} \ln \left(\frac{I_S t}{\frac{nkTC}{q}} \right) \tag{1.19}$$

Thus, once the transient has settled, the sampled voltage follows a logarithmic function of time and becomes independent of the initial capacitor voltage V_{DD}.

From equation (1.19), the dynamic current source generated by the charge-redistribution process in the CBD technique can be approximated as:

$$I_{\text{bias}}(t) \simeq \frac{nCkT}{tq} = \frac{nCV_T}{t} \tag{1.20}$$

To extract temperature, one sample is taken at t_1 to obtain a CTAT voltage. A second sample at $t_2 = p \cdot t_1$ yields a PTAT voltage difference:

$$\Delta V = n\frac{kT}{q} \ln\left(\frac{t_2}{t_1}\right) = n\frac{kT}{q} \ln(p) \tag{1.21}$$

If the diode is implemented with a diode-connected BJT or DTMOST, $n \approx 1$, making the PTAT voltage largely insensitive to process variations.

The CBD technique therefore enables sub-1 V operation and eliminates 1/f noise associated with current sources. However, it introduces kT/C sampling noise, imposing a trade-off between accuracy and capacitor size.

1.3 CBD-based temperature sensor in 180nm

Ideally, as shown in Fig. 1, the sampled diode voltage V_D is determined solely by the intrinsic I–V characteristic of the diode at the sampling moment, as described by (1.19). In practice, however, in addition to the process spread of the diode itself, another major error source arises from the voltage drop across the sampling switch S1.

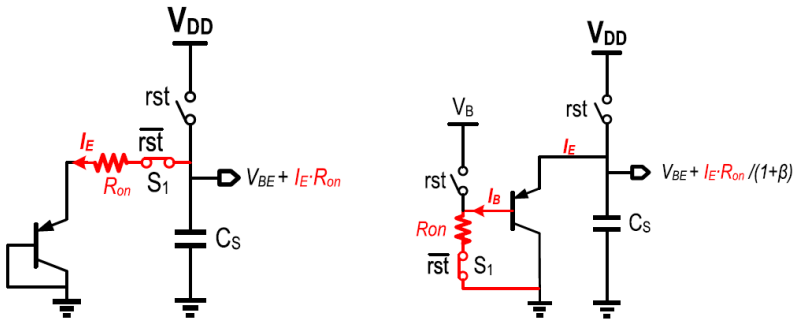


Figure 4: (a) Conventional CB p–n–p structure. (b) Base-switching CB p–n–p architecture [1].

To mitigate this effect, the CBD temperature sensor in [1] adopts a base-switching scheme that significantly reduces the effective ON-resistance R_{on}. As shown in Fig. 4(b), the discharge interval is controlled by switching the base terminal of the PNP transistor rather than its emitter. Since the current flowing through the switch becomes approximately $1+\beta$ times smaller, the associated voltage drop is greatly reduced. Moreover, because the switch is referenced to ground, the increased overdrive voltage further lowers R_{on}. The PNP is turned off by driving its base to a cutoff voltage V_B, which is a replica of V_{BE}.

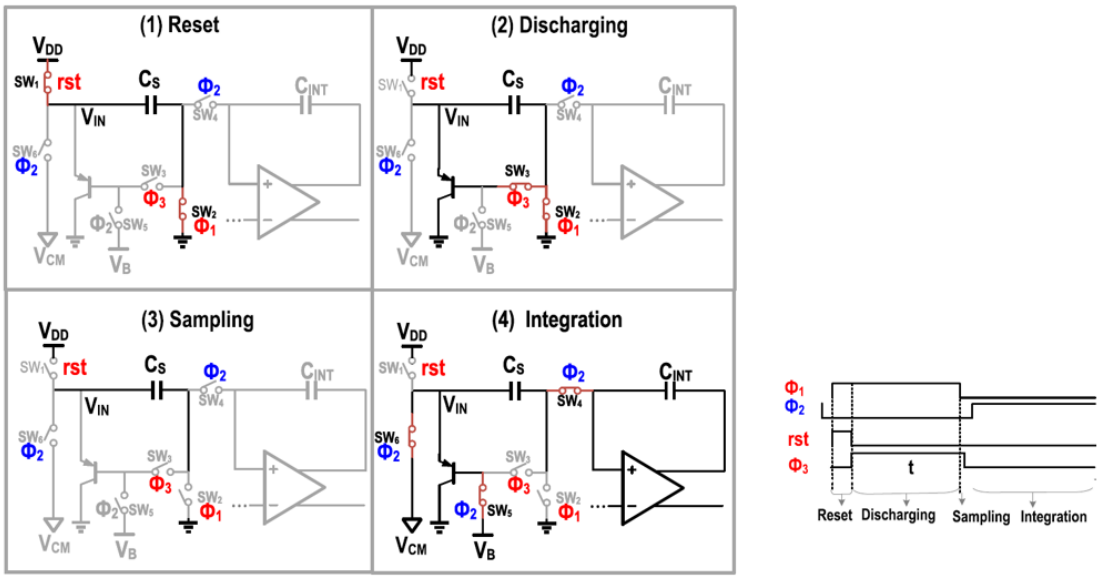


Figure 5: Single-ended operation of the CBD front-end together with the first integrator [1].

Fig. 5 illustrates the single-ended operation of the CBD front-end in combination with the first integrator. The sampling phase (Φ_1) is divided into two sub-phases: the precharge phase (*rst*) and the discharge phase (Φ_3). During *rst*, the sampling capacitor C_S ($C_S = 4\,\text{pF}$) is charged to V_{DD}.

When Φ_3 goes high, C_S is disconnected from V_{DD}, and the PNP transistor is enabled by grounding its base. This causes C_S to discharge through the diode-connected PNP for a controlled time interval t, determined by the Φ_1 and Φ_3 control signals. During this process, the voltage V_{BE} is stored on the sampling capacitor C_S.

Within the same Φ_1 phase, the integrator performs auto-zeroing to suppress offset and flicker noise while maintaining proper bias conditions. In the subsequent phase (Φ_2), the PNP transistor is disabled by tying its base to the bias voltage V_B. The front-end then connects to the integrator, transferring the stored charge from C_S to the integration capacitor C_{INT}.

1.3.1 Charge-balancing scheme

Using a differential CBD front-end pair, the sampled V_{BE2} and ΔV_{BE} values are obtained by applying two discharge intervals, t_1 and t_2 ($t_1 = 1\,\mu\text{s}$, $t_2 = 32\,\mu\text{s}$). Fig. 6 shows the simplified block level diagram of the CBD sensor in [1]. Under the control of the bitstream (BS) output, the clock signal driving three CBD pairs is adjusted every cycle so that they alternately generate V_{BE} or ΔV_{BE}, thereby realizing the charge-balancing scheme.

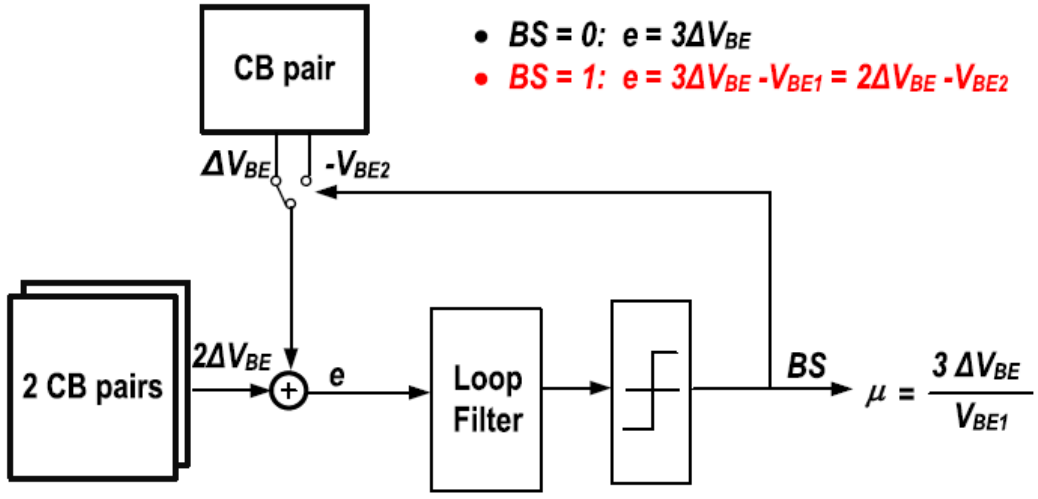


Figure 6: Simplified diagram of the proposed charge-balancing $\Delta\Sigma$ modulator [1].

For the two bitstream states, the corresponding expressions can be written as:

$$\text{BS} = 0: \qquad e = 3\,\Delta V_{BE}$$

$$\text{BS} = 1: \qquad e = 2\Delta V_{BE} - V_{BE2}$$

Applying the charge-balancing condition, the bitstream average μ is given by:

$$(1-\mu)3\Delta V_{BE} + \mu(2\Delta V_{BE} - V_{BE2}) = 0 \tag{1.22}$$

$$\mu = \frac{3\Delta V_{BE}}{V_{BE1}} \tag{1.23}$$

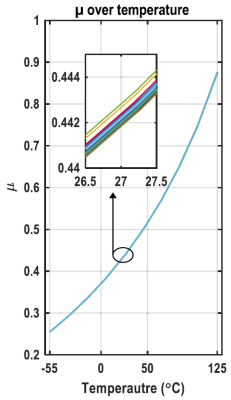


Figure 7: Measured bitstream average μ over temperature of chips in [1].

With the chosen discharge times, the resulting μ fully utilizes the ADC dynamic range (0.2–0.9), as shown in Fig. 7. To obtain a temperature-linear response as in (1.13), the decimated output μ is mapped to a linearized quantity μ_{lin}, given by:

$$\mu_{\text{lin}} = \frac{\alpha\,\Delta V_{BE}}{V_{BE} + \alpha\,\Delta V_{BE}} = \frac{\alpha\left(\frac{3\,\Delta V_{BE}}{V_{BE}}\right)}{3 + \alpha\left(\frac{3\,\Delta V_{BE}}{V_{BE}}\right)} = \frac{\alpha\,\mu}{\alpha\,\mu + 3}. \tag{1.24}$$

To compensate for the PTAT spread in V_{BE} (discussed in detail in Chapter 2.1.1), a one-point PTAT trimming [16] at room temperature can be applied:

$$\mu_{\text{lin}} = \frac{\alpha\,\mu}{(\alpha + \alpha_{\text{trim}})\,\mu + 3}. \tag{1.25}$$

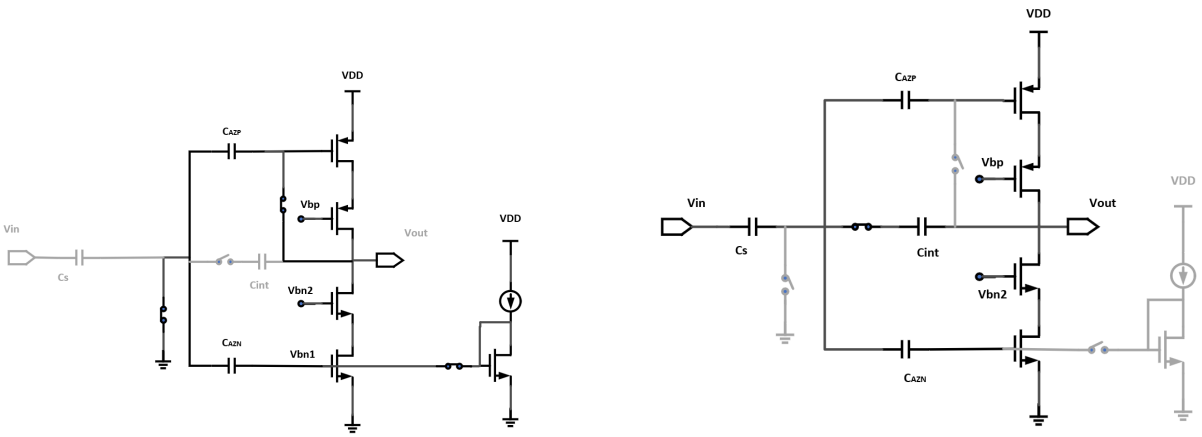
The linearized quantity is then processed digitally to generate the temperature output:

$$T = A\,\mu_{\text{lin}} - B, \tag{1.26}$$

where α, A, and B are fitting coefficients, and α_{trim} is the trimming coefficient used to correct the PTAT spread.

1.3.2 Error Correction Techniques

To accurately generate $3\Delta V_{BE}$, the mismatch between the charge-balancing pairs is minimized using a bitstream-controlled dynamic element matching (DEM) scheme, in which the CB pairs are rotated only when the bitstream (BS) output is '1'. Mismatch between the p–n–p devices and the sampling capacitors within each pair can introduce a residual offset in the generated ΔV_{BE}. This error is suppressed by a system-level low-frequency chopping (CHL) technique, whose period equals the conversion time.

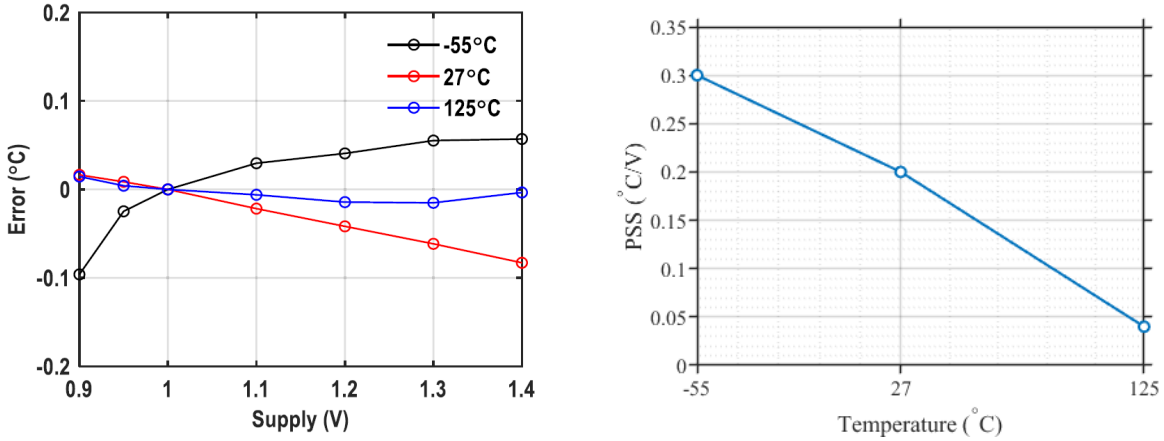


(a) Auto-zero phase.

(b) Integration phase.

Figure 8: Operation of the single-ended inverter-based amplifier.

To enable sub-1V operation and low energy consumption, the DSM employs auto-zeroed inverter-based pseudo-differential amplifiers, as shown in Fig. 8. During the auto-zero phase, the front-end is disconnected while the AZ switches are closed. The bias current (160 nA) is set by a constant-g_m bias generator through an NMOS current mirror, and the corresponding NMOS and PMOS bias voltages are sampled onto the capacitors C_{AZN} and C_{AZP}. In this unity-gain configuration, the input offset, bias voltages, and low-frequency noise are captured on the auto-zero capacitors. During the subsequent integration phase, these stored values are subtracted from the amplifier input, effectively cancelling offset and $1/f$ noise and ensuring a stable, low-offset output for the modulator.



(a) Temperature error over supply voltage [1].

(b) PSS over temperature.

Figure 9: PSS results in [1].

Fabricated in 180 nm CMOS, this design achieves an inaccuracy of ± 0.15°C after one-point trimming, with a PSS of 0.2°C$/V$ at room temperature and 0.3°C$/V$ over the full temperature range, as shown in Figure 9b. Its minimum supply voltage is limited to 0.95 V because the intrinsic V_{BE} at low temperatures (-55°C) is about 0.8 V.

1.4 CBD-based temperature sensor in 22nm

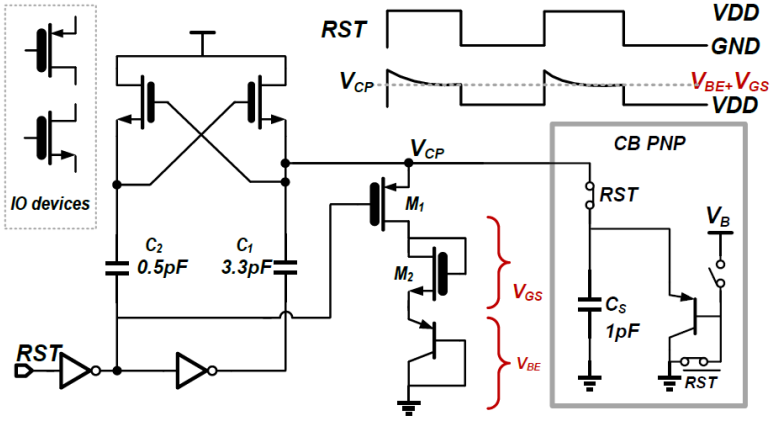


Figure 10: CB p–n–p structure with regulated charge pump (RCP) [3].

To address the supply-voltage limitation, [3] introduces a regulated charge-pump technique capable of boosting the internal supply above 1 V even when the external supply voltage is as low as 0.7 V. This provides sufficient headroom above the intrinsic V_{BE} at low temperatures (approximately 0.8 V at -55°C). As shown in Fig. 10, when the RST signal transitions high, the voltage on capacitor C_1 is first boosted to approximately $2V_{\mathrm{DD}}$. It is then discharged through a diode-connected PNP and a diode-connected NMOS, settling to a regulated level of $V_{BE} + V_{GS}$. After charge sharing between C_1 and the sampling capacitor C_s, the resulting voltage V_{CP} on C_s exceeds 1 V for $V_{\mathrm{DD}} > 0.7$ V, enabling reliable low-voltage operation.

This regulated node also reduces the dependence of the CB-biased PNPs' headroom (V_{GS}) on the supply voltage, thereby significantly improving the sensor's PSS.

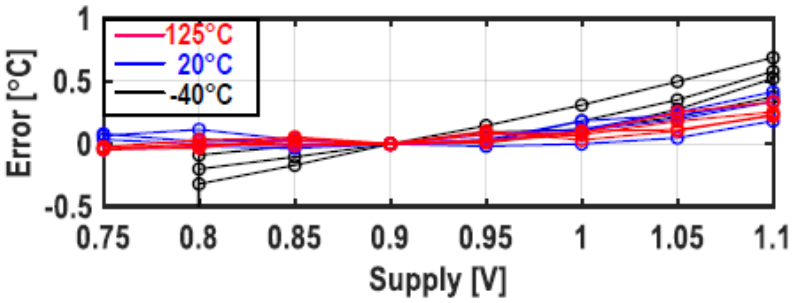


Figure 11: Temperature error over supply voltage [3].

Fabricated in 22 nm CMOS, this design achieves an inaccuracy of ± 0.4°C after one-point trimming. Although the RCP enables a lower supply voltage (0.8 V) and is expected to improve the PSS, the measured results in Fig. 11 show that the PSS remains relatively

high: 0.58–1.3 °C/V at room temperature and up to 3.67 °C/V at −40°C. This reveals a clear opportunity for further investigation and motivates a more detailed analysis and design approach aimed at achieving ultra-low and well-controlled PSS.

1.5 Project Goals

The performance of representative CBD-based temperature sensors is summarized in Table 1.

Table 1: Comparison of state-of-the-art CBD-based temperature sensors

Specification	**This Work**	**SSCL'19 [17]**	**JSSC'23 [1]**	**VLSI'24 [3]**
Process	65 nm	16 nm FinFET	180 nm	22 nm
Device Type	PNP	Diode	PNP	PNP
Supply [V]	< 1	0.85–1	0.95–1.4	0.8–1.1
Power [μW]	< 0.7	18	0.81	2.9
Temp. Range [°C]	–55 to 125	–15 to 105	–55 to 125	–40 to 125
Inaccuracy [°C]	±0.2 (1-pt)	$+1.5/-2$ (0-pt)	±0.45 (0-pt) ±0.15 (1-pt)	±1.25 (0-pt) ±0.4 (1-pt)
RIA [%]	0.23 (1-pt)	2.9 (0-pt)	0.5 (0-pt) 0.17 (1-pt)	1.5 (0-pt) 0.48 (1-pt)
PSS [°C/V]	< 0.05	1.5	0.2	0.58–1.3 (RT)
Resolution [mK]	3	300	1.8	4.7
Conv. Time [ms]	64	0.013	128	6.4
Res. FoM [pJ·K^2]	< 0.4	21	0.34	0.41

(0-pt = no individual trim; 1-pt = one-point trim.)
Resolution FoM = (Energy per conversion)·(Resolution)^2.

It can be observed that although CBD-based temperature sensors already demonstrate low-voltage capability and high energy efficiency, their PSS performance still leaves considerable room for improvement. Moreover, as technology scales down, the reported inaccuracy has worsened from ±0.15°C to approximately ±0.4°C, suggesting that the behavior of CBD-based temperature sensors in scaled technologies requires further examination.

Therefore, the primary objective of this work is to implement the CBD-based design presented in [1] in a 65 nm process. A secondary objective is to analyze the key contributors to PSS and develop techniques that can substantially reduce supply sensitivity without compromising accuracy.

The ultimate goal is to realize a CBD-based temperature sensor in 65nm process operating from a sub-1V supply, achieving a PSS below 0.05°C/V and an inaccuracy within ±0.2°C (1-point trim) over a temperature range of −55°C to 125°C, corresponding to approximately 0.23% RIA.

1.6 Thesis Organization

The remainder of this thesis is organized as follows. Chapter 2 presents the proposed system architecture and discusses design considerations for achieving high accuracy and low power-supply sensitivity. Chapter 3 describes the circuit-level implementation, including the CBD front-end and the DSM. Chapter 4 reports simulation results, covering accuracy, PSS, resolution, and power consumption. Finally, Chapter 5 concludes this thesis and outlines potential directions for future work.

2 Architecture Considerations

With the goals of achieving low PSS and high accuracy, this work builds on the state-of-the-art CBD-based temperature sensors presented in [1] and [3]. This chapter discusses the architecture of the proposed design and the key modifications made to enhance the performance compared with these previous designs.

2.1 Architecture of the Proposed CBD Front-End

2.1.1 Non-Idealities in the Front-End

Since we aim to achieve low PSS and high accuracy, the non-idealities that influence the intrinsic accuracy and PSS of the front-end need to be carefully studied.

For the ease of error budgeting, we will first investigate how the sampled voltage error is translated into a temperature error. Based on the equation (1.11), (1.13) and (1.14) , the sensitivity of the digital output D_{out} to errors in V_{BE} and ΔV_{BE} can be calculated by differentiating D_{out} with respect to each variable:

$$S_{V_{BE}}^{D_{out}}(T) = \frac{\partial D_{out}}{\partial V_{BE}} = A\frac{\partial \mu}{\partial V_{BE}} \simeq -\frac{T}{V_{REF}} \tag{2.1}$$

$$S_{\Delta V_{BE}}^{D_{out}}(T) = \frac{\partial D_{out}}{\partial (\Delta V_{BE})} = A\frac{\partial \mu}{\partial (\Delta V_{BE})} \simeq \frac{A-T}{V_{REF}}\alpha \tag{2.2}$$

where T is the temperature in Kelvin, and hence the approximation $\mu \simeq \frac{T}{A}$ has been used. In this design, a 5×5 μm^2 PNP is used and a current ratio of $p = 32$ is set to match the configuration in the previous work [1]. Parameters $A = 590$, $B = 280$, and $\alpha = 7.2$ are used for temperature calculation. The sensitivity of the digital output D_{out} to errors in V_{BE} and ΔV_{BE} is shown in Fig. 12. It can be seen that the sensitivity of the digital output D_{out} to errors in ΔV_{BE} is the most significant.

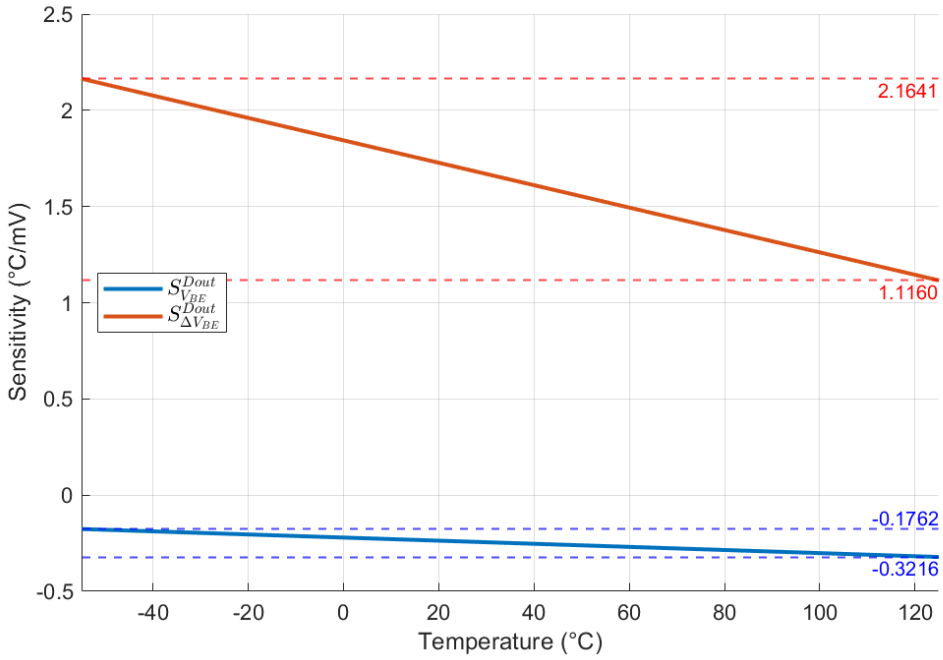


Figure 12: Sensitivity of D_{out} to V_{BE} and ΔV_{BE} errors.

Optimizing Accuracy The current-density ratio of the emitter currents in the diode-connected PNPs is well defined. However, the resulting base–emitter voltage V_{BE} is determined by the collector current I_C. The relationship between the collector current and the emitter current is governed by the common-base current gain α_0:

$$\alpha_0 = \frac{I_C}{I_E} = \frac{\beta}{\beta + 1}. \tag{2.3}$$

Since β is relatively low (approximately 0.5–1.5) in the 65 nm LP process, a β-dependent error is introduced. From equation (1.6), we can derive:

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{\frac{\beta_1}{\beta_1 + 1} p I_{E1} + I_S}{\frac{\beta_2}{\beta_2 + 1} I_{E1} + I_S} \right). \tag{2.4}$$

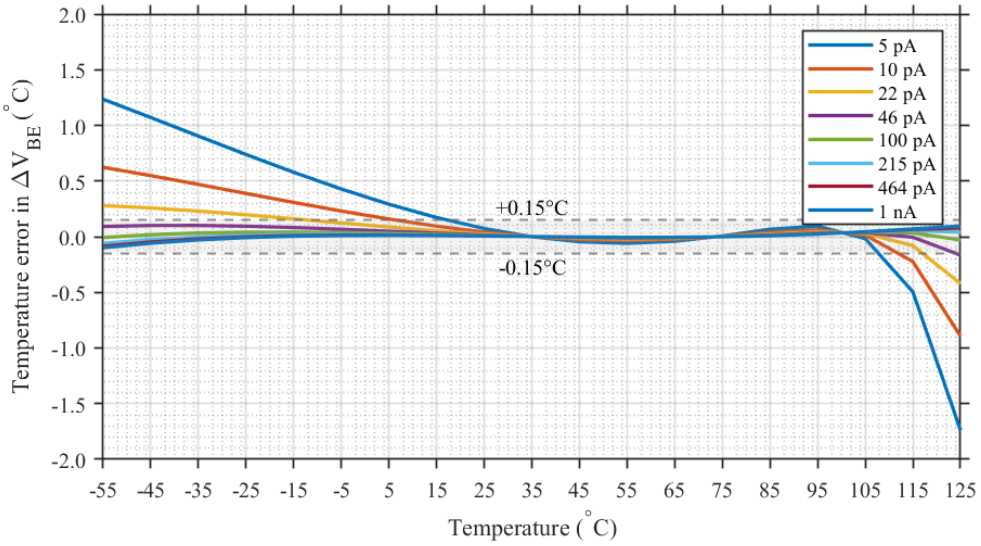


Figure 13: Temperature error caused by ΔV_{BE} variation from $-55°\mathrm{C}$ to $125°\mathrm{C}$ under different bias currents.

To minimize the I_S-related error in (2.4), the bias current I_E must be chosen much larger than I_S to obtain an accurate PTAT voltage. As shown in Fig. 13, when the PNP is biased with a small emitter current I_E, the saturation current I_S becomes comparable to I_E. Since I_S is strongly temperature dependent [2], this results in a pronounced ΔV_{BE}-related error at hot. When I_E is chosen sufficiently larger than I_S (typically $> 100\,\mathrm{pA}$), the influence of I_S becomes negligible, and the resulting ΔV_{BE}-related temperature error stays within an acceptable range (about $0.15°\mathrm{C}$ up to $125°\mathrm{C}$). In this regime, equation (2.4) reduces to:

$$\Delta V_{BE} \cong \frac{kT}{q} \ln \left(\frac{\frac{\beta_1}{\beta_1 + 1} p I_{E1}}{\frac{\beta_2}{\beta_2 + 1} I_{E1}} \right) \tag{2.5}$$

It can also be seen from Equation (2.5) that variations in β under different bias conditions introduce additional ΔV_{BE}-related errors. This becomes the dominant error source at low temperatures because of the limited β of the PNP at low temperature. As shown in Fig. 14, there is a range in which β remains relatively constant. When both BJTs are biased within this region, the β-related error can be minimized. This occurs when I_E is between approximately $0.1\,\mathrm{nA}$ and $10\,\mu\mathrm{A}$. In conclusion, to minimize the ΔV_{BE}-related errors caused by I_S and β, the emitter current I_E should be between $0.1\,\mathrm{nA}$ to $10\,\mu\mathrm{A}$.

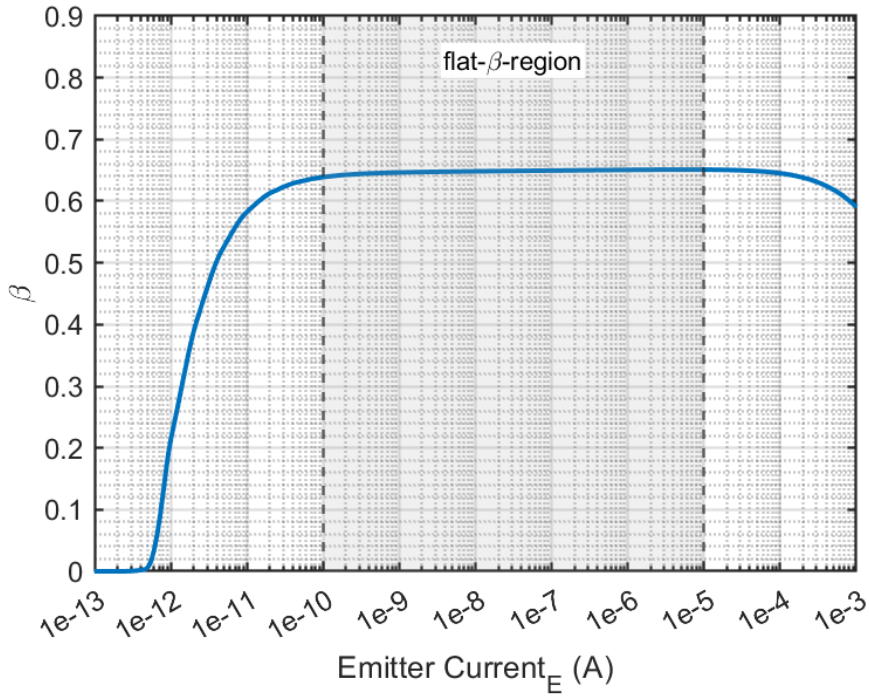


Figure 14: BJT's β variation over its emitter current I_E at $-55°\text{C}$.

Spread in V_{BE} is mainly due to the variation of I_S and β. If a given transistor has a saturation current that deviates by ΔI_S from its nominal value I_S, the base–emitter voltage can be expressed as:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S + \Delta I_S}\right) = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) - \frac{kT}{q} \ln\left(1 + \frac{\Delta I_S}{I_S}\right) \tag{2.6}$$

which can be approximated as

$$V_{BE} \simeq V_{BE}\big|_{\Delta I_S = 0} - \frac{kT}{q}\frac{\Delta I_S}{I_S}, \qquad (\Delta I_S \ll I_S) \tag{2.7}$$

Since this spread is PTAT [2], it can be compensated by a one-point PTAT trimming.

Although the β of the two BJTs are biased in the flat β region to minimize the β-related ΔV_{BE} error, the effect of β on V_{BE} still remains:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{\left(\frac{\beta_F + \Delta\beta_F}{\beta_F + \Delta\beta_F + 1}\right) I_E}{I_S}\right) \tag{2.8}$$

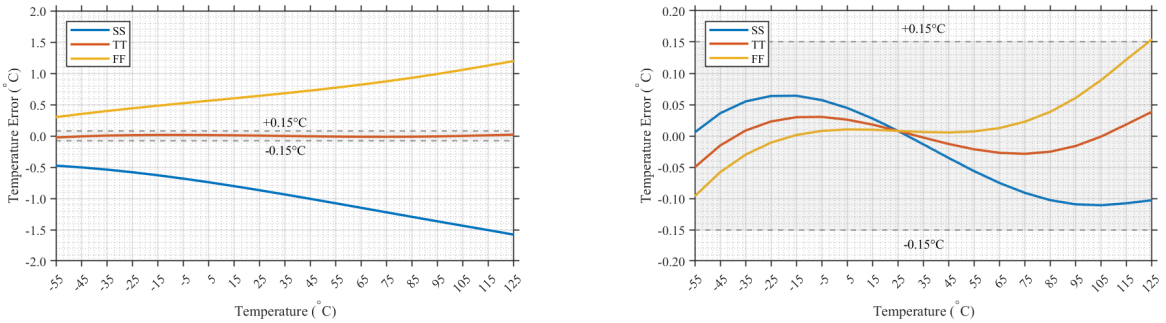
which can be approximated as

$$V_{BE} \simeq V_{BE}\big|_{\Delta\beta_F=0} + \frac{kT}{q}\frac{\Delta\beta_F}{\beta_F(\beta_F+1)}, \qquad (\Delta\beta_F \ll \beta_F) \tag{2.9}$$

This spread is not PTAT, since the second term is not temperature-independent [2]. However, because the sensitivity of the measured temperature to V_{BE} is much smaller than that to ΔV_{BE}, this source of spread can be tolerated after PTAT trimming.

In this design, the ΔV_{BE} spread over process and temperature is minimized by selecting a current-density ratio of 32 and a bias current of $I_{\text{bias}} = 1\,\text{nA}$ at room temperature. However, according to (1.20), this bias current is generated dynamically. Therefore, both the sampling-capacitor size and the discharge interval must be carefully selected. To keep the front-end kT/C noise comparable to that of the previous work [3], a sampling capacitor of 1 pF is used. With this choice and with $5 \times 5\ \mu\text{m}^2$ PNPs, the resulting asymmetric discharge intervals become approximately 500 ns and 16 μs.

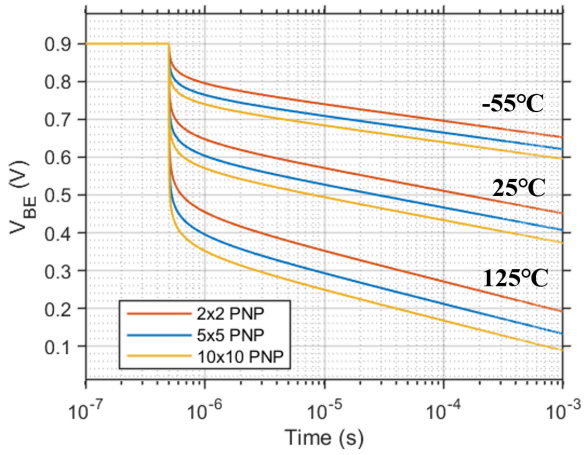
As shown in Fig. 15, the simulated intrinsic temperature spread of the PNP device is about 150 mK over all PVT corners. This leaves some margin for additional nonidealities—such as switch leakage and amplifier errors—to meet the overall inaccuracy target of 200 mK.



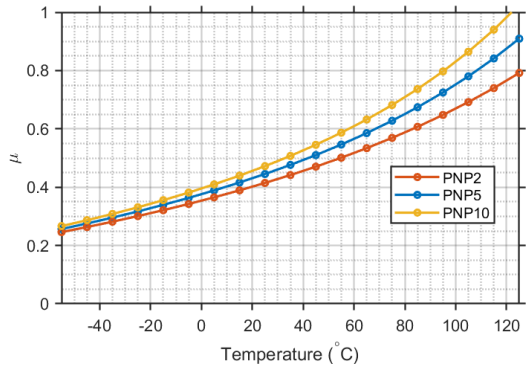
(a) Untrimmed (b) Trimmed

Figure 15: Simulated temperature error due to PNP corner variation: (a) untrimmed and (b) trimmed results.

Optimizing PNP Area In the 65 nm process, two additional PNP sizes are available: $2 \times 2\ \mu\text{m}^2$ and $10 \times 10\ \mu\text{m}^2$. A smaller device results in a lower I_s, which increases V_{BE} according to (1.19) and therefore reduces $\mu = \frac{3\Delta V_{BE}}{V_{BE1}}$, as illustrated in Fig. 16. Conversely, a larger $10\times10\ \mu\text{m}^2$ device causes the ADC output to clip at 125°C, while a smaller $2\times2\,\mu\text{m}^2$ PNP limits the ADC dynamic range and increases the required conversion time to achieve the same resolution.



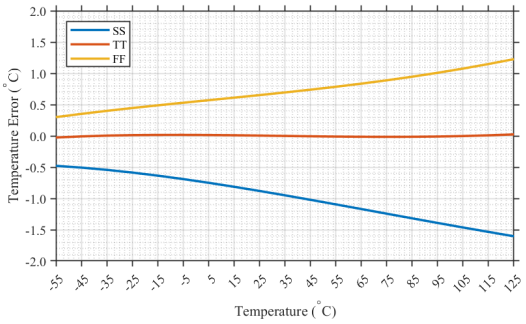
(a) V_{BE} vs. time for different PNP areas ($C_S = 1\,\text{pF}$, $V_{DD} = 0.9\,\text{V}$).



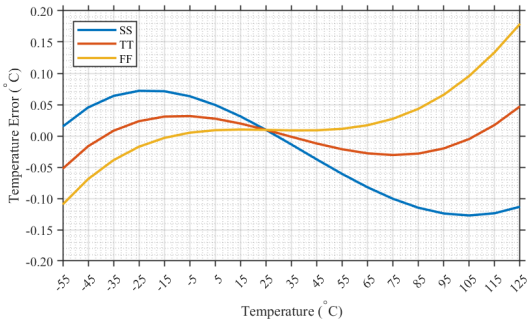
(b) Simulated μ over temperature for different PNP areas.

Figure 16: Variation of V_{BE} and μ for different PNP areas.

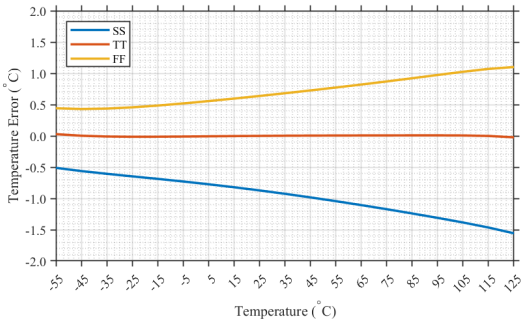
Because the dynamic biasing current in (1.20) is independent of PNP area, the same sampling capacitor and discharge intervals are used when comparing intrinsic accuracy across device sizes. Under these conditions, the simulated intrinsic spreads of the $2 \times 2\,\mu\text{m}^2$ ($\approx 170\,\text{mK}$) and $10 \times 10\,\mu\text{m}^2$ ($\approx 160\,\text{mK}$) devices are similar to that of the $5 \times 5\,\mu\text{m}^2$ PNP, as shown in Fig. 17. The larger device, however, exhibits a noticeable curvature in its temperature error. This behaviour can be explained by its current-gain characteristics: as shown in Fig. 18, the $10 \times 10\,\mu\text{m}^2$ PNP does not exhibit a flat β-region over current, whereas the $5 \times 5\,\mu\text{m}^2$ device does. As a result, the larger device introduces additional β-related ΔV_{BE} error.



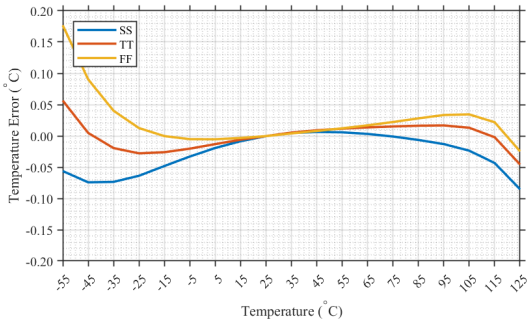
(a) Untrimmed error, $2 \times 2\,\mu\text{m}^2$.



(b) Trimmed error, $2 \times 2\,\mu\text{m}^2$.



(c) Untrimmed error, $10 \times 10\,\mu\text{m}^2$.



(d) Trimmed error, $10 \times 10\,\mu\text{m}^2$.

Figure 17: Simulated temperature error due to PNP corner variation for different device areas.

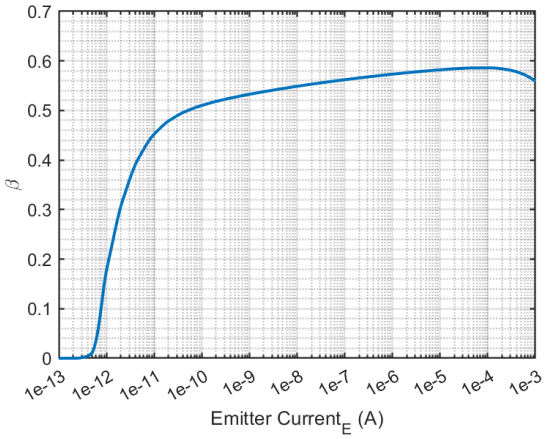


Figure 18: β variation of a $10 \times 10\,\mu\text{m}^2$ PNP at $-55°\text{C}$.

Conclusion on PNP size: Considering accuracy and ADC dynamic range, the $5 \times 5\,\mu\text{m}^2$ PNP is selected for the SC front-end.

Optimizing Discharge-Time Ratio The simulated μ values for discharge-time ratios $p = t_2/t_1 = 16, 32, 64$ are shown in Fig. 19. For $p = 64$, the ADC output clips at 125°C because ΔV_{BE} increases with p according to (1.21). A smaller ratio $p = 16$ reduces the ADC dynamic range and requires a longer conversion time to maintain resolution.

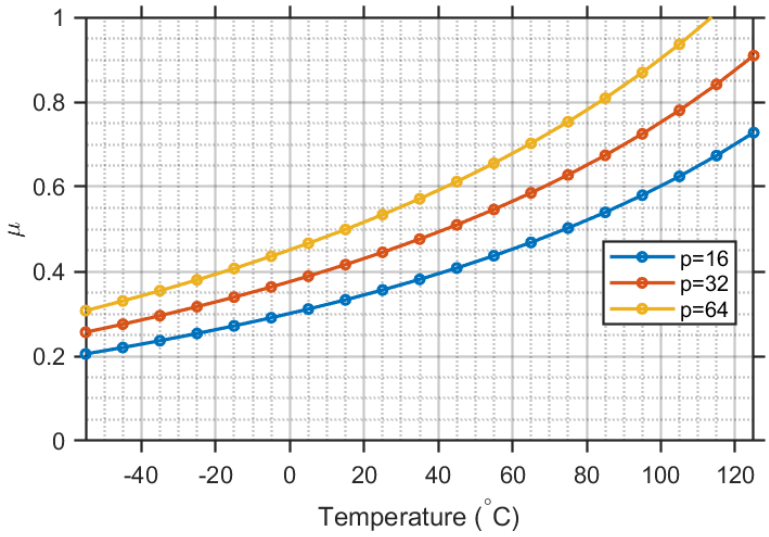
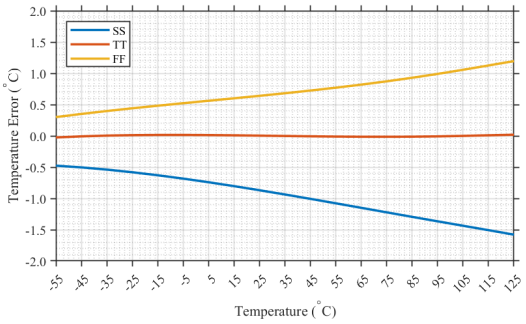
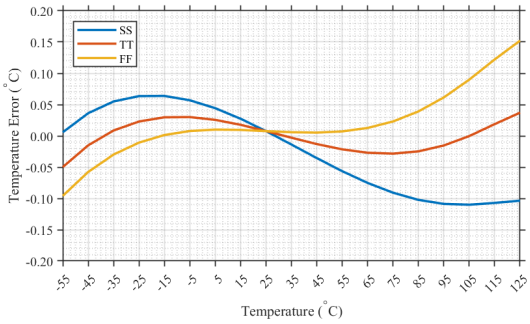


Figure 19: Simulated μ over temperature for time ratios $p = 16, 32, 64$.

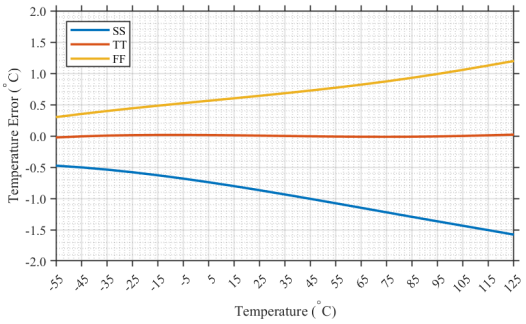
All three values of p exhibit similar intrinsic accuracy. Simulation results for $p = 16$ and $p = 64$ are shown in Fig. 20.



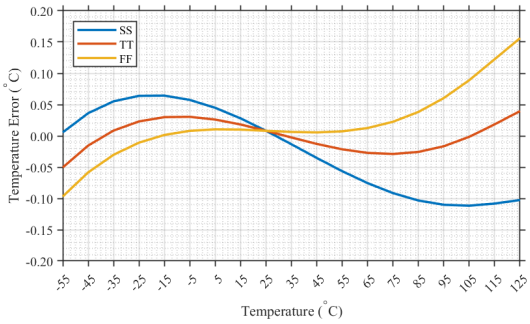
(a) Untrimmed error, $p = 16$.



(b) Trimmed error, $p = 16$.



(c) Untrimmed error, $p = 64$.



(d) Trimmed error, $p = 64$.

Figure 20: Simulated temperature error for different discharge-time ratios p under PNP corner variation.

Conclusion on discharge-time ratio: A discharge-time ratio of $p = 32$ provides the most balanced trade-off between ADC dynamic range and intrinsic accuracy.

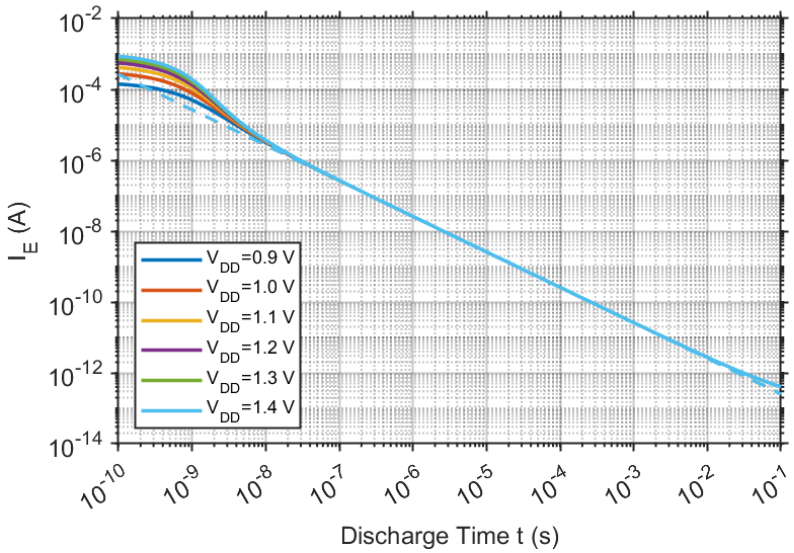


Figure 21: Current through the PNP over discharge time for different initial voltages.

Optimizing PSS The intrinsic PSS of the front-end must also be examined, as it represents the supply-voltage-related error over the VDD range of 0.9 V to 1.4 V.

As described in Section 1.2.3, the supply-independent bias current in (1.20) is generated dynamically and is only valid under the following two conditions:

$$t \ll \frac{nkTC}{I_S q}, \qquad t \gg \frac{nkTC}{qI_S} \exp\left(-\frac{qV_{DD}}{nkT}\right).$$

Outside this range, the VDD-dependent exponential term in (1.18) remains significant. As shown in Fig. 21, the simulated dynamic current converges to the modeled current source (dashed line) only when the discharge interval exceeds roughly 10 ns. For shorter discharge intervals, the deviation becomes non-negligible, resulting in a larger intrinsic PSS. In this region, the BJT operates in high injection and becomes strongly affected by series-resistance effects [2], which amplifies its sensitivity to supply-voltage variations.

At the other extreme, when the condition $t \ll \frac{nkTC}{I_S q}$ is no longer satisfied, the behavior of the dynamic current source starts to deviate from the ideal model. As shown in Fig. 21, this deviation becomes noticeable once the discharge time exceeds approximately 1 ms. Beyond this point, the exponential term in (1.16) can no longer be linearized, making the simplification to (1.18) invalid and introducing an additional VDD-dependent error.

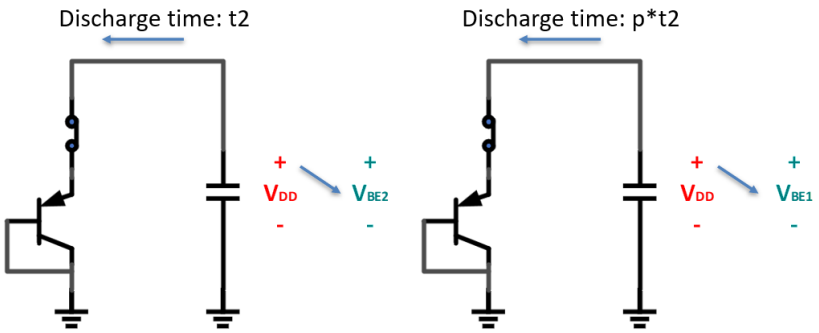
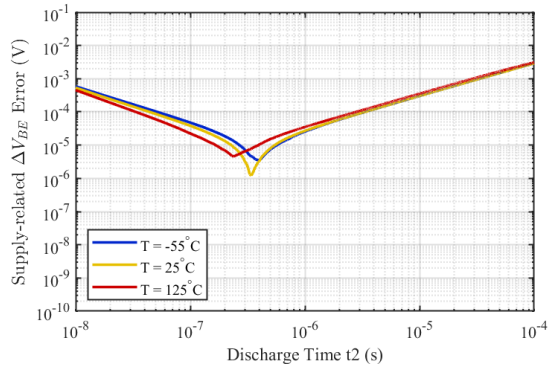
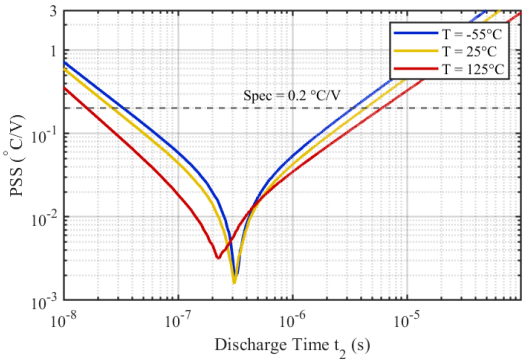


Figure 22: Testbench used to find the optimum PSS.

In conclusion, to ensure that the dynamic current source is independent of VDD, the discharge time should be neither too short nor too long. In the testbench shown in Fig. 22, the capacitors are precharged to different VDD values. The discharge switch is an ideal switch with $R_{on} = 1\Omega$. The left capacitor is discharged for t_2 seconds, while the right one is discharged for $p \cdot t_2$ seconds. With a fixed time ratio of $p = 32$, the simulated supply-related ΔV_{BE} error versus t_2 is shown in Fig. 23a. Using the sensitivity of measured temperature to ΔV_{BE} error, the PSS as a function of discharge time can be plotted in Fig. 23b. The optimum PSS is achieved when the discharge time t_2 is around 500 ns, corresponding to an intrinsic PSS of approximately 0.02 °C/V.



(a) Supply-related ΔV_{BE} error over discharge time.



(b) PSS over discharge time.

Figure 23: Simulated supply-related characteristics of the PNP-based front-end.

However, an ideal switch with $R_{\text{on}} = 1\,\Omega$ is not practical. When R_{on} is increased to a more realistic value of 500 Ω, Monte Carlo simulation in Fig. 24 shows that the resulting PSS exceeds the target specification of 0.05 °C/V across temperature, with the largest deviation occurring at −55°C. To further improve the PSS performance, a regulated charge pump architecture, as proposed in [3], is considered.

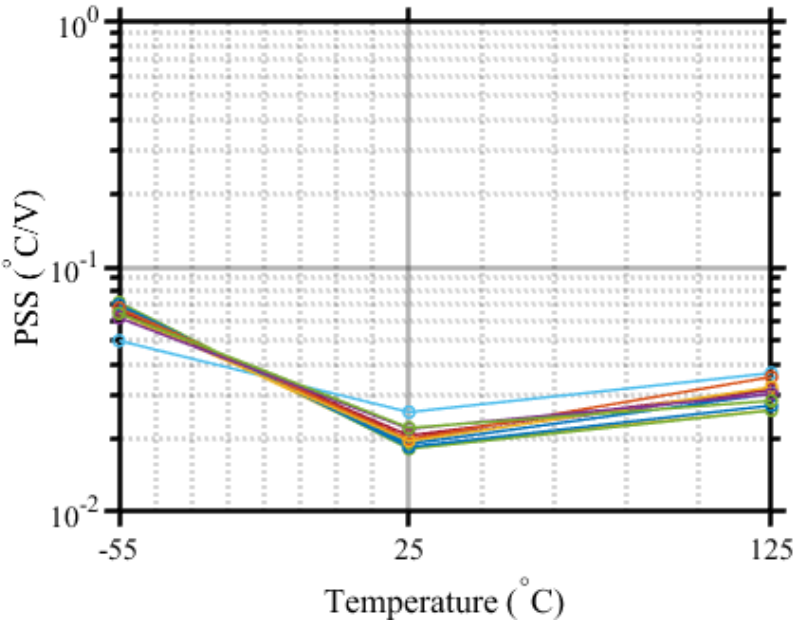


Figure 24: Monte Carlo PSS of the SC CBD front-end with an ideal discharge switch with $R_{on} = 500\Omega$.

2.1.2 Regulated Charge Pump

As discussed in Chapter 1.4, the design in [3] introduces a regulated charge pump that stabilizes the supply to $V_{GS} + V_{BE}$. However, during each cycle, its output has to swing from 0 to $2V_{DD}$ and then settle to $V_{GS} + V_{BE}$. As a result, accurately reaching the target voltage within the short reset phase becomes challenging. Therefore, a more stable and continuously regulated supply voltage is required.

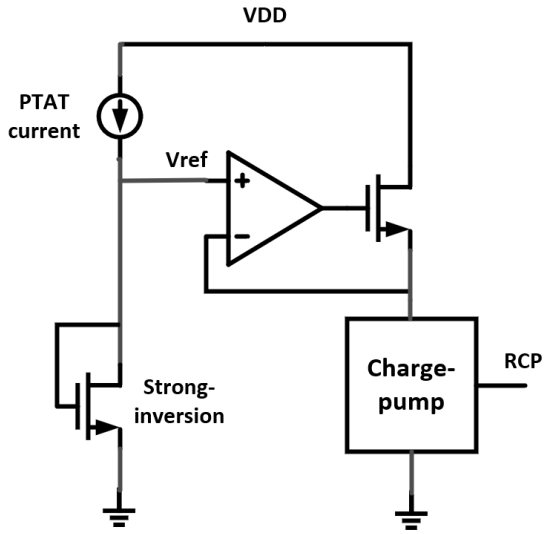


Figure 25: Proposed regulated charge pump with LDO-based reference generation.

In [18], a low-power regulated voltage doubler is presented. It consists of a reference-voltage generator that feeds a Low-Dropout Regulator(LDO), which then drives a charge pump to produce the boosted supply voltage. As shown in Fig. 25, a PTAT current biases a diode-connected NMOS transistor operating in strong inversion to generate a stable reference voltage. This PTAT current is provided by a constant-g_m biasing circuit.

Constant-g_m biasing circuit The low-voltage constant-g_m biasing circuit [19] used in this design is shown in Fig. 26. It generates a PTAT bias current of approximately 16 nA at room temperature, as shown in Fig. 27, which remains supply independent and enables reliable sub-1 V operation.

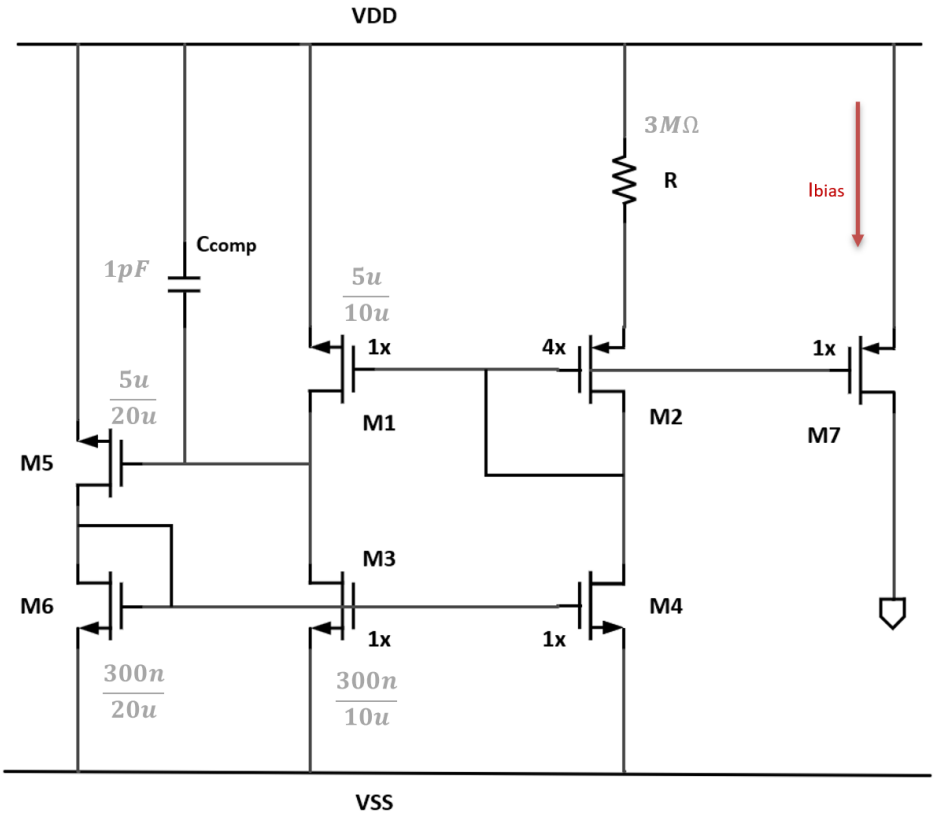


Figure 26: Low-voltage constant-g_m bias circuit.

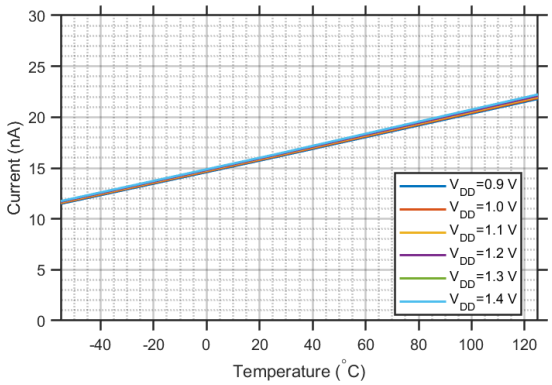


Figure 27: Generated PTAT biasing current over supply voltages.

Reference voltage generator When an NMOS diode is biased in weak inversion, the resulting reference voltage is CTAT, as illustrated in Fig. 28. However, by choosing an appropriate device aspect ratio and biasing the device in strong inversion (with an aspect ratio of 400 nm/100 μm), a nearly temperature-independent reference voltage of about 0.75 V

can be achieved, as shown in Fig. 29. Monte-Carlo simulations confirm that this reference voltage varies only from 0.72 V to 0.79 V across corners as shown in Fig. 30.

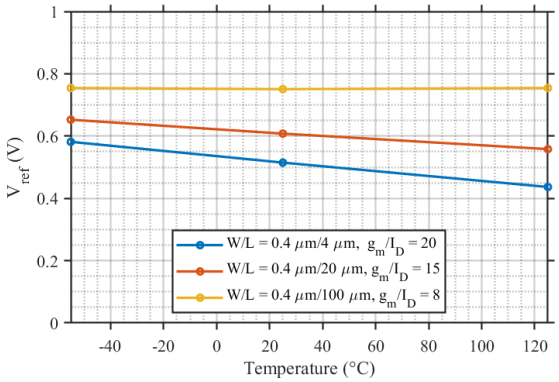
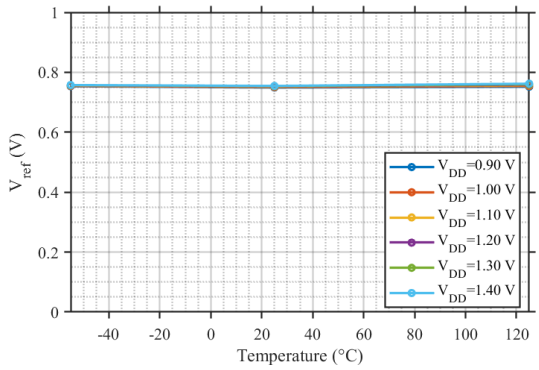
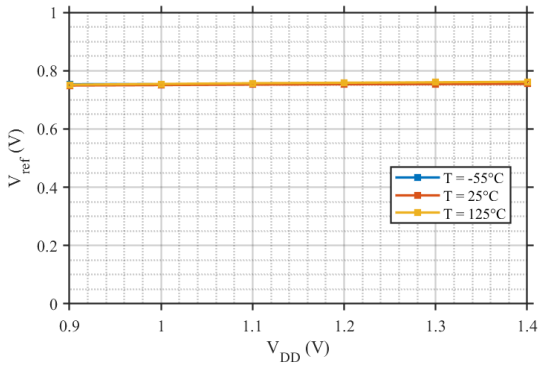


Figure 28: Reference voltage versus aspect ratio and $\frac{g_m}{I_D}$.



(a) Reference voltage versus temperature.



(b) Reference voltage versus supply voltage.

Figure 29: Simulated reference voltage stability over temperature and supply voltage.

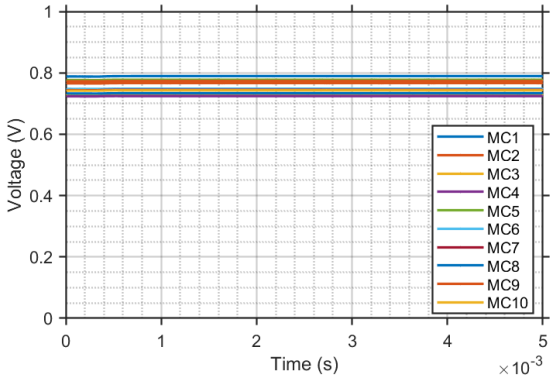


Figure 30: Monte Carlo simulation of the reference voltage.

Error amplifier The error amplifier (EA) used in the LDO is a simple five-transistor OTA, as shown in Fig. 31. It consumes only 16 nA of current while achieving a DC gain of 40 dB and a gain–bandwidth product (GBW) of 500 kHz. A native NMOS transistor is selected as the output driver due to its low threshold voltage, which ensures adequate output swing at low supply levels.

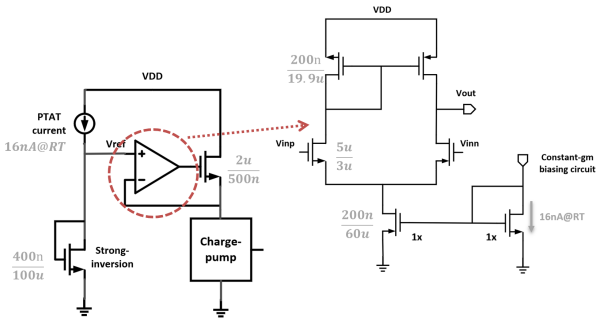


Figure 31: Circuit diagram of the error amplifier (EA).

Charge pump After buffering, this reference voltage is boosted by a charge pump, as shown in Fig. 32, to generate a regulated 1.5 V supply that remains stable across temperature and supply variations throughout the entire operating range.

The operation of the charge pump is as follows: ϕ_1 and ϕ_2 are rail-to-rail, non-overlapping, inverting clock signals. After being driven by inverters powered from the reference voltage, the resulting ϕ_1' and ϕ_2' become non-overlapping inverting signals that swing from 0 to V_{ref}. When ϕ_2' transitions from 0 to V_{ref}, node V_2 is driven from V_{ref} to $2V_{\text{ref}}$, while node V_1 transitions from $2V_{\text{ref}}$ to V_{ref}.

The cross-coupled NMOS pair and the PMOS switches are implemented using I/O devices to tolerate the higher voltages generated within the charge pump. The pump capacitors are realized using large MOS capacitors (about 10 pF), significantly larger than the sampling capacitors, to minimize charge-sharing effects.

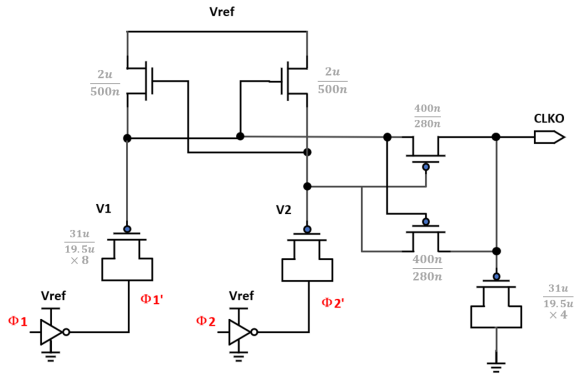


Figure 32: Circuit diagram of the reference-voltage charge pump.

3 Circuit Implementation

This chapter discusses the detailed circuit implementation of the proposed system.

3.1 CBD Front-End

3.1.1 Sensing Core and Sampling Capacitor

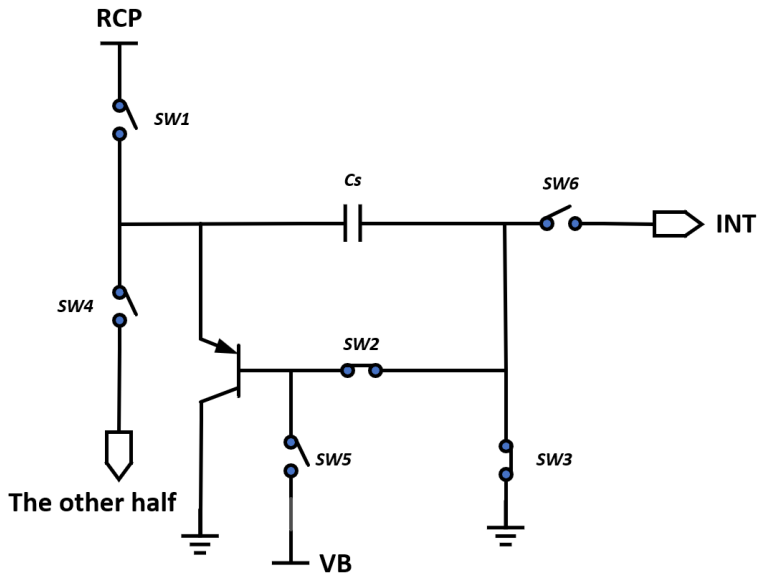
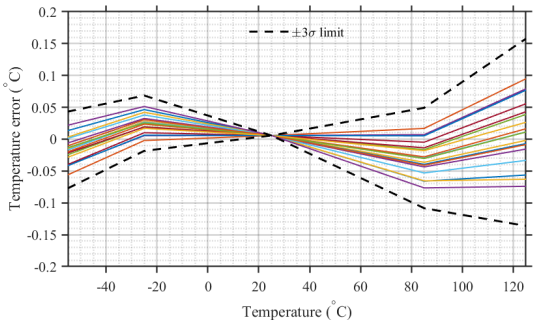


Figure 33: Simplified diagram of the single-ended front-end with switches.

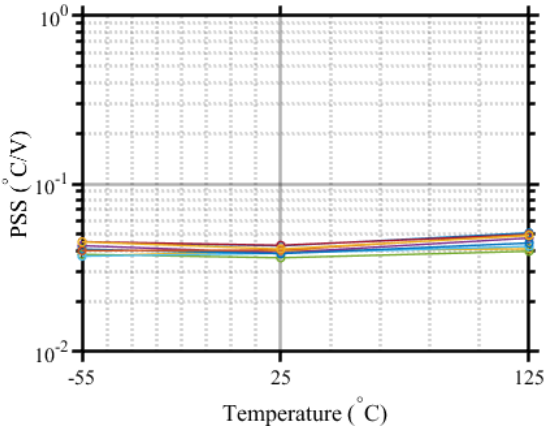
As discussed in the previous chapter, the CBD front-end is implemented using a sampling capacitor of $C_S = 1\,\text{pF}$ and a $5 \times 5\ \mu\text{m}^2$ PNP transistor, as shown in Fig. 33. The sampling capacitor is charged to a well-controlled RCP voltage. At this stage, ideal switches and an ideal readout circuit are assumed for initial analysis.

Considering both accuracy and PSS, the discharge intervals are chosen as $t_1 = 500\,\text{ns}$. With a time ratio of 32, t_2 is chosen as $16\,\mu\text{s}$. A metal–insulator–metal (MIM) capacitor is selected for C_S due to its excellent stability against process variations and temperature fluctuations.

Monte Carlo simulations indicate that this configuration achieves a 3σ inaccuracy of 0.15°C and a PSS of around 0.03°C/V, as shown in Fig. 34.



(a) Monte Carlo inaccuracy of the SC CBD front-end with ideal switches after a one-point PTAT trim at 25°C.



(b) Monte Carlo PSS of the SC CBD front-end with ideal switches at −55°C, 25°C, and 125°C.

Figure 34: Monte Carlo simulation results of the SC CBD front-end with ideal switches.

3.1.2 Switch Design

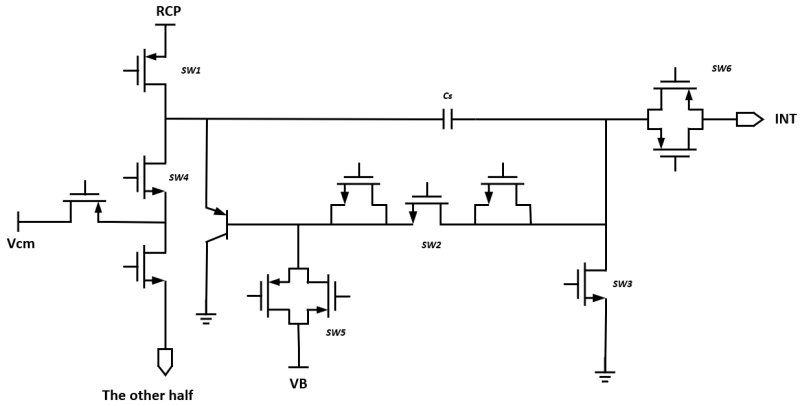


Figure 35: Transistor-level implementation of the front-end switches.

The ideal switches in Fig. 33 are replaced by transistor-level implementations, as shown in Fig. 35. The CBD front-end employs six pairs of switches, whose nonidealities—including R_{on}, leakage, charge injection, and clock feedthrough—directly influence the accuracy of the sampled V_{BE} and ΔV_{BE}. Furthermore, because all switches are driven from the supply, their supply-dependent behaviour also contributes to the overall PSS of the sensor.

The requirements for these switches are summarized in Table 2 and the detailed considerations are discussed below.

Table 2: Switch error budget and corresponding error contribution.

Switch	Error Budget	Error Contribution
SW1	$R_{\text{on}} < 200\ \text{k}\Omega,\ \ I_{\text{leak}} < 1.7\ \text{pA}$	0.03°C
SW2	$R_{\text{on}} < 550\ \Omega$	0.02°C
SW3	$R_{\text{on}} < 8\ \text{k}\Omega$	
SW4	$R_{\text{on}} < 13\ \text{k}\Omega,\ \ I_{\text{leak}} < 3.5\ \text{pA}$	0.05°C
SW5	$R_{\text{on}} < 8\ \text{k}\Omega$	–

SW1 (Reset Switch):

Since the two front-end branches use different discharge intervals during Φ_1, leakage through SW1 causes an asymmetric charge loss of approximately $\frac{I_{\text{leak}}\Delta t}{C_s}$, which appears as a ΔV_{BE}-related error between the sampling paths. To keep this error below 30 mK, the leakage current must remain below 1.7 pA.

SW1 also determines the settling behaviour, since the sampling capacitor is charged through this switch. With a minimum reset time of 500 ns, a low R_{on} of 200 kΩ is required to ensure accurate ($\sim 5\tau$) settling. Therefore, an I/O PMOS with $W/L = 400\,\text{nm}/560\,\text{nm}$ is used. A boosted clock is applied to simultaneously achieve low R_{on} and high R_{off}, improving both settling and leakage performance.

SW2 (Discharge Switch):

As discussed in Chapter 1.3, IR-drop introduces a supply-dependent ΔV_{BE}-related error component. To limit this error below 20 mK, R_{on} must remain below 550 Ω. Thus, SW2 is implemented with a wide I/O NMOS ($W/L = 4\,\mu\text{m}/560\,\text{nm}$) and driven by a boosted clock.

However, because of the large device size, charge injection and clock feedthrough become significant, and these effects degrade both accuracy and PSS. Two half-sized dummy switches are therefore added to both sides of the switch to compensate these errors.

SW3 (Grounding Switch):

Implemented using a small I/O NMOS ($W/L = 400\,\text{nm}/560\,\text{nm}$), SW3 benefits from relaxed R_{on} requirements [1]. Its leakage is negligible across PVT because both of its terminals remain close to ground (or virtual ground) during operation.

SW4 (Sampling Switch):

Leakage in SW4 introduces error through the same mechanism as in SW1. To keep this error below 50 mK, its leakage must be under 3.5 pA. A minimum-size NMOS T-switch is therefore used, achieving a maximum leakage of about 3.3 pA across PVT while keeping charge injection and clock feedthrough small.

SW5 (Base-Biasing Switch):

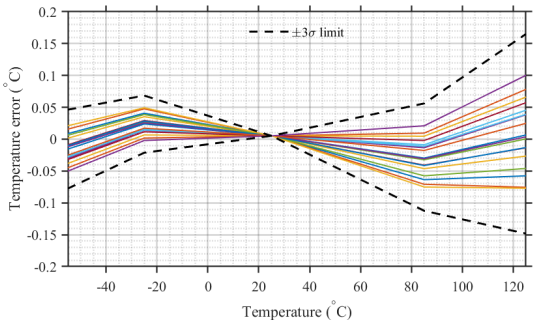
Since the PNP cutoff voltage V_B is approximately 0.75 V, a PMOS ($W/L = 600\,\text{nm}/280\,\text{nm}$) is used to achieve low R_{on}. An NMOS ($W/L = 400\,\text{nm}/280\,\text{nm}$) is added in parallel to balance charge injection and reduce clock feedthrough.

SW6 (Integrator Interface Switch):

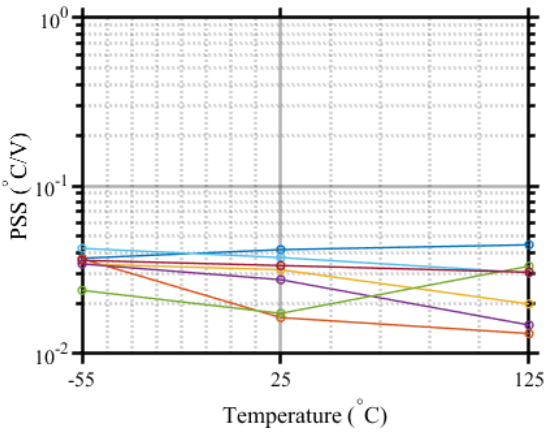
To preserve integrator transconductance while minimizing charge injection, SW6 uses a parallel combination of a minimum-size NMOS ($W/L = 200\,\text{nm}/60\,\text{nm}$) and PMOS

($W/L = 320\,\text{nm}/60\,\text{nm}$).

By ensuring all switches meet the specified R_{on} and leakage requirements in Table 2, the real front-end achieves an inaccuracy of 0.16°C after a one-point PTAT trim. This performance is obtained at a 0.9 V supply voltage. The corresponding PSS results are shown in Fig. 36, confirming that the design meets the accuracy specification.



(a) Monte Carlo inaccuracy of the SC CBD front-end with real switches after one-point PTAT trim at 25°C.



(b) Monte Carlo PSS of the SC CBD front-end with real switches at −55°C, 25°C, and 125°C.

Figure 36: Monte Carlo simulation results of the SC CBD front-end with real switches.

3.1.3 Biasing Voltage Generator

During the integration phase (Φ_2), the base of the PNP must be tied to a biasing voltage V_B to ensure complete cutoff. In the previous design, this bias voltage was generated by a simplified replica of the front-end that produced a voltage approximately equal to V_{BE2}.

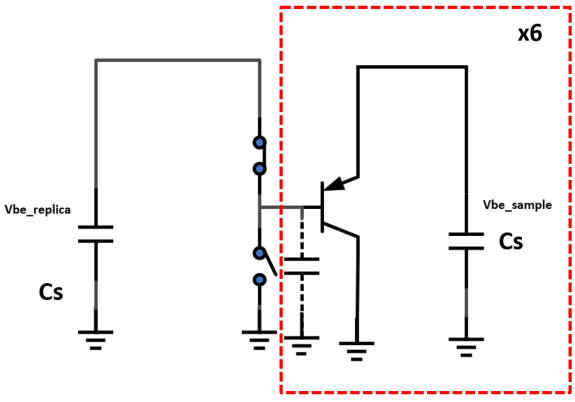
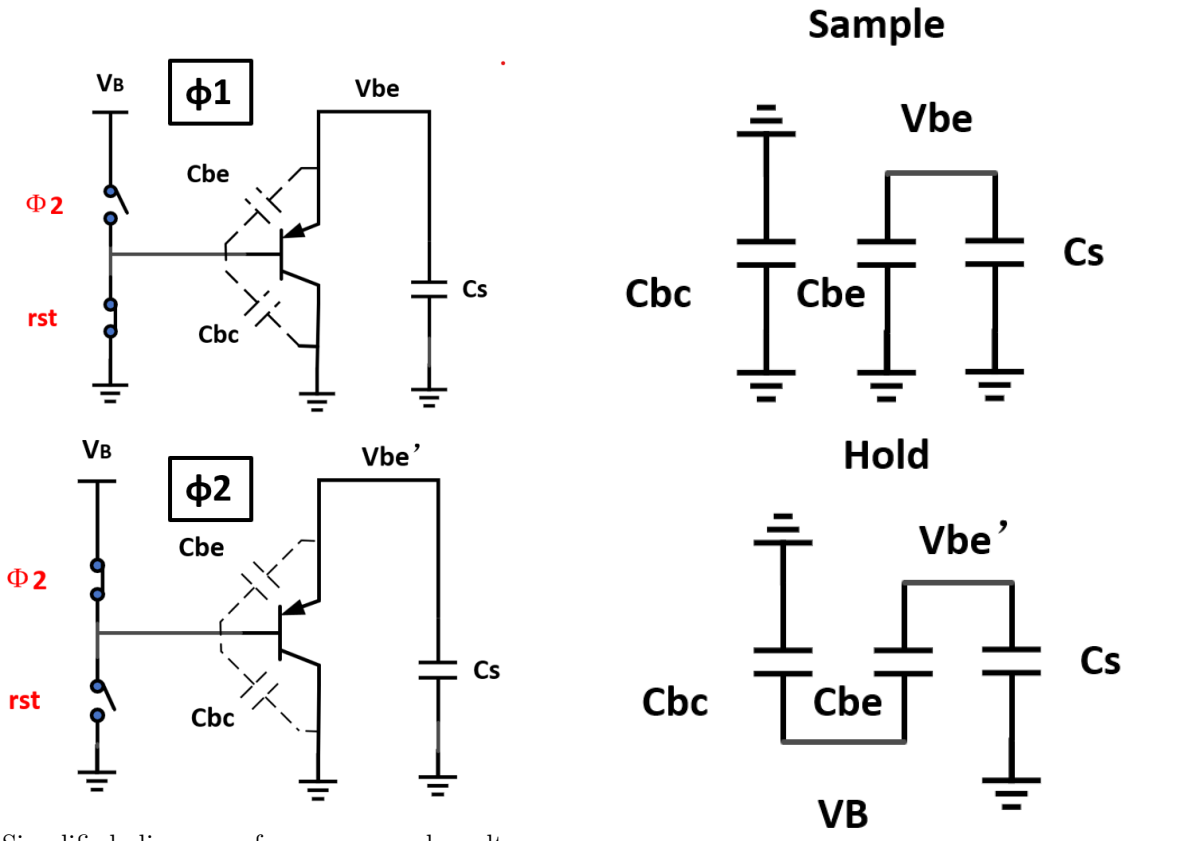


Figure 37: Simplified diagram illustrating base voltage generation and charge sharing.

As shown in Fig. 37, charge sharing between the replica sampling capacitor and the

parasitic base capacitances of the six PNPs lowers the actual base voltage below the intended $V_{BE,\text{replica}}$. This reduced cutoff voltage is insufficient to fully turn off the PNPs at high temperatures. Even when V_{BE1} is used as the cutoff level, the sampled V_{BE} still drops by approximately 120 μV during the hold phase (Φ_2), corresponding to a temperature error of roughly 0.12°C.



(a) Simplified diagram of common-mode voltage drift.

(b) Voltage across C_S and parasitic capacitances.

Figure 38: Front-end common-mode voltage drift caused by charge sharing.

However, increasing the base voltage excessively is also undesirable. As shown in Fig. 38, when switching from Φ_1 to Φ_2, a voltage jump occurs due to charge sharing, resulting in a modified base-emitter voltage:

$$V'_{BE} = V_{BE} + \frac{C_{BE}}{C_{BE} + C_S} V_B \tag{3.1}$$

For PNP5, C_{BE} is approximately 28 fF. If V_B were set equal to V_{DD}, the resulting voltage jump would be around 32 mV. This causes a common-mode voltage drift of about 32 mV across the differential front-end, complicating the common-mode feedback (CMFB) gain requirement, which will be explained in the CMFB section.

To balance these trade-offs, a static bias voltage $V_B \approx 0.75$ V is selected to ensure reliable cutoff while minimizing input common-mode variation around 24 mV. This bias voltage is conveniently available from the LDO reference block and reused during Φ_2, without requiring additional circuitry.

3.2 DSM Readout

3.2.1 Topology and Sizing

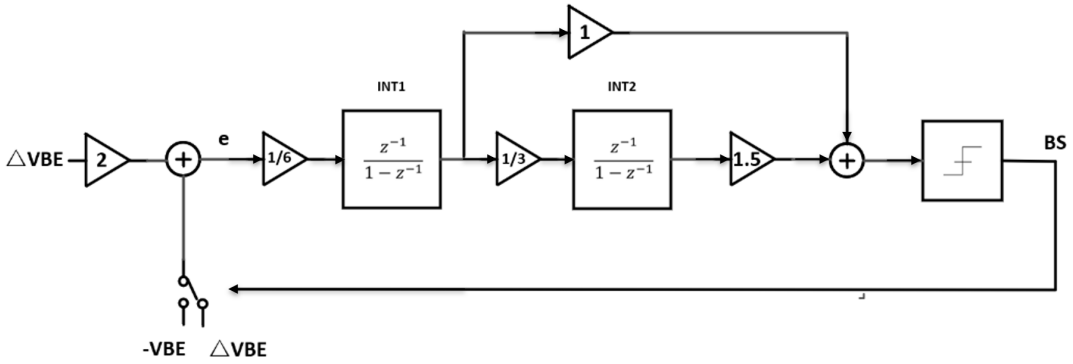


Figure 39: Block diagram of the second-order feed-forward DSM readout circuit.

As proposed in [3], this work employs a second-order feed-forward sigma–delta modulator to digitize the ratio between the PTAT and CTAT voltages generated by the front-end. A feed-forward topology is selected to minimize the signal swing at the output of the first integrator, thereby improving linearity and stability. The loop coefficients are optimized according to the integrator output swing constraints obtained from behavioral simulations.

The corresponding single-ended capacitor values are summarized in Table 3.

The output swing of the first and second integrators, as well as the adder, across temperature and process corners is shown in Table 4. The variations over temperature arise from the temperature dependence of the sampled input voltages, ΔV_{BE} and V_{BE}. Since V_{BE} increases at low temperatures, the corresponding integrator output swings become larger in the cold corner.

3.2.2 Implementation of Integrators

The first integrator plays a critical role in balancing the charge provided by the front-end while introducing minimal additional noise. To meet these requirements, it must provide sufficiently high DC gain, adequate speed for accurate settling, and enough drive strength for the capacitive load. This subsection details the corresponding design considerations and implementation.

Table 3: Chosen capacitor values for single-ended DSM implementation.

Capacitor	**Value [pF]**
C_{S1}	3×1
C_{INT1}	6
C_{S2}	0.1
C_{INT2}	0.3
C_{FF1}	0.2
C_{FF2}	0.3
C_{cm1}	2×0.8
C_{cm2}	2×0.1
C_{AZ1}	2×4
C_{AZ2}	2×0.6
Total capacitance	**20.1**

Table 4: Output swings of the first integrator, second integrator, and the SC adder across corners and temperature.

		Max swing [mV]	**Min swing [mV]**
FF 125°C	INT1	45	-45.9
	INT2	59.6	-2.2
	Adder	55.4	-13.6
TT 27°C	INT1	68	-66.7
	INT2	18.3	-24.8
	Adder	48.7	-54.3
SS -55°C	INT1	102.8	-112.0
	INT2	13	-78.8
	Adder	40.5	-80.6

An open-loop gain of approximately 80 dB across PVT is targeted for the first-stage amplifier to match the design requirements in [1].

The next key requirement is speed. The total load capacitance seen at the output of the first integrator is approximately 4.7 pF. To achieve the desired settling accuracy within the integration time of 16 μs, the gain–bandwidth product of the first-stage amplifier is set to about 250 kHz, i.e., roughly eight times the sampling frequency. The effective time constant is given by:

$$\tau = \frac{1}{\mathrm{BW}} = \frac{1}{\beta \cdot \mathrm{GBW}}, \tag{3.2}$$

where β is the feedback factor. With this choice, the output settles within approximately 8τ, corresponding to a residual error of e^{-8}, which translates into a V_{BE} settling error of about 27 μV, i.e., less than 5 mK over the full input range. The Monte Carlo open-loop Bode plot in Fig. 40 confirms that the designed amplifier achieves a mean gain of about

80 dB and a GBW exceeding 250 kHz across PVT, thus meeting these requirements.

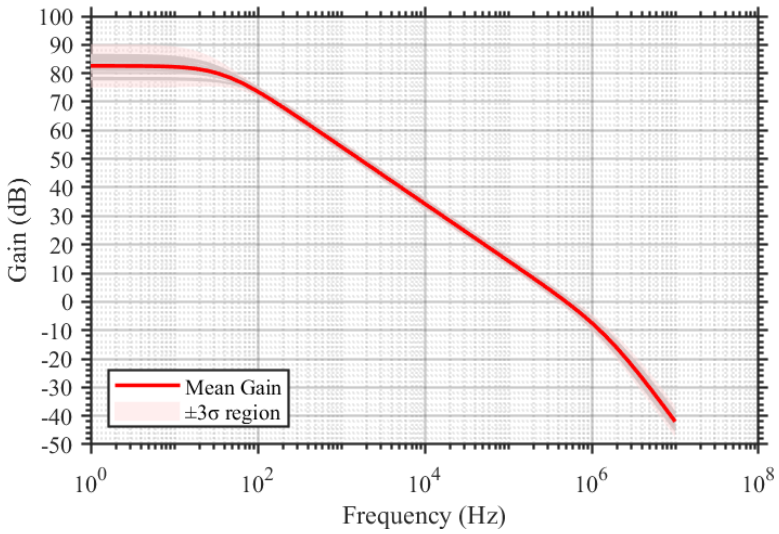
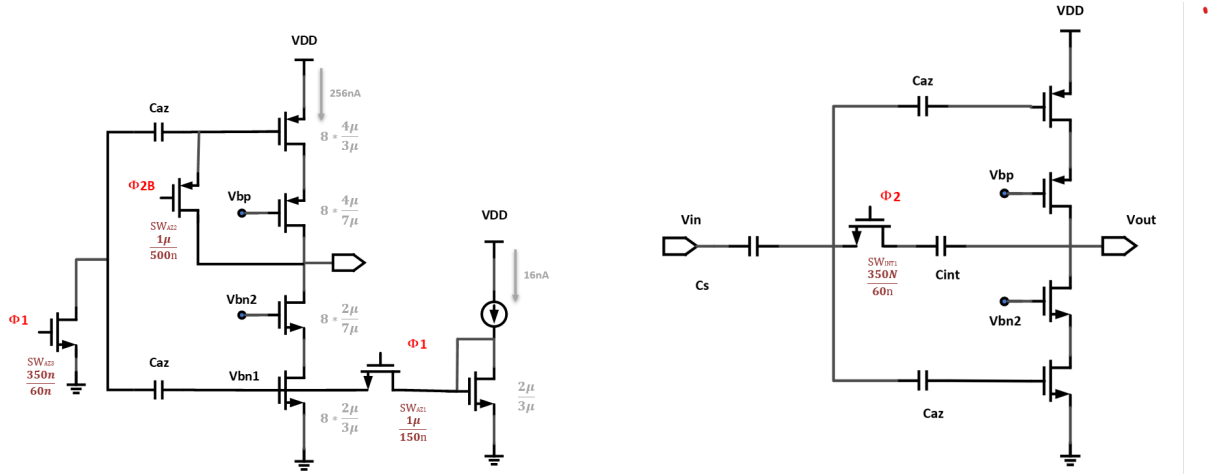


Figure 40: Monte Carlo simulated open-loop gain and GBW of the amplifier.

The operation of the auto-zeroed inverter-based amplifier was discussed in Chapter 1.3.2 and is detailed schematically in Fig. 41.



(a) Auto-zero phase.

(b) Integration phase.

Figure 41: Circuit schematics of the inverter-based amplifier in auto-zero and integration phases.

From a noise perspective, the input-referred noise of the integrator should be kept below the kT/C noise of the front-end sampling capacitor. This motivates the use of a relatively large auto-zero capacitor C_{AZ}. Furthermore, since the input transistors' bias

voltage, offset, and 1/f noise are sampled onto C_{AZ}, the effect of charge sharing with the parasitic gate capacitance C_{gg} must be minimized. To ensure that this effect is negligible, C_{AZ} is chosen to be at least ten times larger than C_{gg}. For the wide input devices used, C_{gg} is approximately 320 fF, leading to the choice of $C_{\mathrm{AZ}} = 4$ pF.

Leakage currents during the auto-zero phase can cause a common-mode drift in the voltages stored on C_{AZ}, resulting in a residual offset after subtraction. In a 65-nm process, the dominant contributors are the gate leakage of the large input devices (approximately 2.5 pA) and the leakage of the auto-zero switch (approximately 400 fA). The resulting voltage error can be estimated as

$$\Delta V_{\mathrm{AZ}} \approx \frac{I_{\mathrm{leak}} \cdot t_{\mathrm{AZ}}}{C_{\mathrm{AZ}}}, \tag{3.3}$$

which remains below approximately 10 μV, i.e., within about 2 mK equivalent temperature error, and is therefore acceptable.

The second integrator employs a scaled version of the same inverter-based, auto-zeroed amplifier. Its device dimensions are reduced by a factor of eight, resulting in approximately eight times lower bias current and power consumption. Its biasing is shared with the first integrator.

3.2.3 Common-Mode Feedback

The implemented common-mode feedback circuit is shown in Fig. 42.

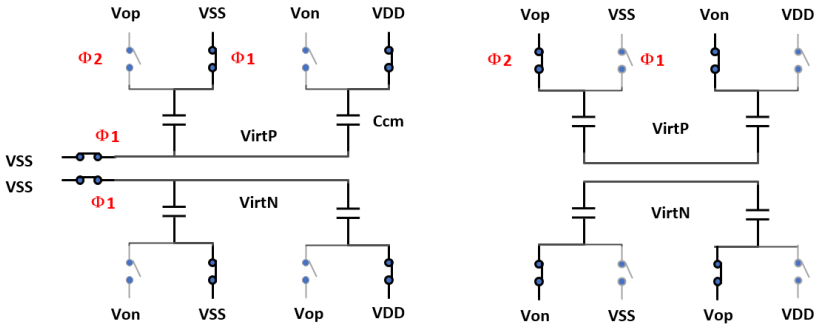


Figure 42: Circuit schematic of the CMFB design [1].

During phase Φ_1, the common-mode feedback capacitors C_{cm} are connected between the supply voltage and ground. For one half of the differential circuit, the total charge stored on the two capacitors can be expressed as:

$$Q_{\Phi_1} = C_{\mathrm{cm}} V_{\mathrm{DD}}. \tag{3.7}$$

During the integration phase Φ_2, the C_{cm} capacitors are reconnected between the amplifier outputs ($V_{\mathrm{OP}}, V_{\mathrm{ON}}$) and the virtual ground nodes ($V_{\mathrm{irtP}}, V_{\mathrm{irtN}}$). Considering one side of the circuit, the total charge becomes:

$$Q_{\Phi_2} = C_{\mathrm{cm}}(V_{\mathrm{OP}} - V_{\mathrm{irtP}}) + C_{\mathrm{cm}}(V_{\mathrm{ON}} - V_{\mathrm{irtP}}). \tag{3.8}$$

This can be simplified to:

$$Q_{\Phi_2} = C_{\text{cm}}(V_{\text{OP}} + V_{\text{ON}} - 2V_{\text{irtP}}). \tag{3.9}$$

By applying charge conservation between (3.7) and (3.9), the virtual input node voltage settles to:

$$V_{\text{irtP}} = \frac{V_{\text{OP}} + V_{\text{ON}}}{2} - \frac{V_{\text{DD}}}{2}. \tag{3.10}$$

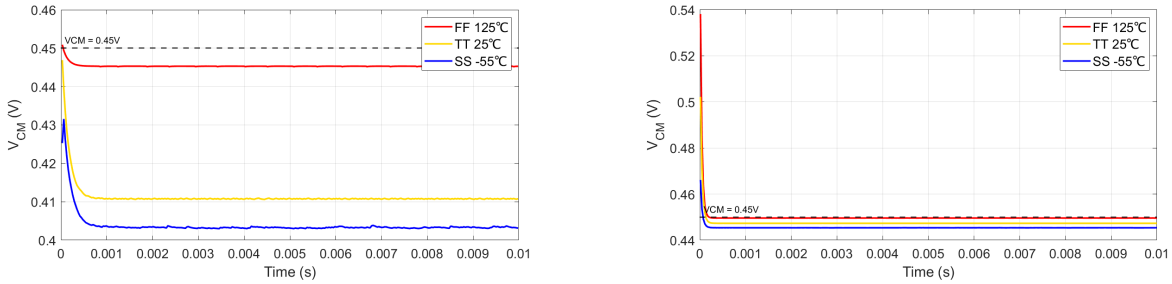
In this way, the CMFB circuit drives the output common-mode voltage $V_{\text{CM,out}}$ toward the target reference $\frac{V_{\text{DD}}}{2}$ by adjusting the charge stored at the amplifier inputs.

As discussed in Section 3.1.3, any drift of the input common-mode voltage affects the sizing of the common-mode capacitors through the feedback gain relationship:

$$3 \cdot C_S \cdot \Delta V_{\text{CM,in}} = 2C_{\text{cm}} \cdot \Delta V_{\text{CM,out}}. \tag{3.4}$$

To tolerate a maximum output common-mode drift of 50 mV, C_{cm} must be no smaller than 800 fF. This value ensures sufficient CMFB gain while maintaining a low noise contribution.

The output VCM deviation of the first integrator and second integrator over temperature and corner is shown in Figure 43. The output VCM shifts by 46mV at most in the SS corner at $-55°$C as calculated. In the FF corner at 125°C present a VCM output deviation since the leakage on the autozero capactors will cause a common-mode voltage deviation and the leakage is the most in this corner.



(a) Output VCM of the first integrator.

(b) Output VCM of the second integrator..

Figure 43: Output VCM of the first and second integrator.

3.3 Clock Boosters and Level Shifters

Several switches in the front-end require clock signals with amplitudes exceeding the nominal supply voltage (V_{DD}) in order to meet the stringent leakage and settling-time specifications. To support this requirement, a boosted clock voltage of approximately $2V_{\text{DD}}$ is generated. In [1], each of these signals was generated by its own charge pump. Although this works well, it becomes less efficient when a large number of boosted signals are required. Therefore, in this design, a constant $2V_{\text{DD}}$ supply is generated using a single

pair of non-overlapping inverting clocks. Level shifters are then employed to translate standard logic levels to the boosted domain, ensuring correct operation of all high-swing switches.

The implemented charge pump is shown in Fig. 32, where the reference supply V_{ref} is replaced by the actual V_{DD}. The level-shifter design is shown in Fig. 44. A total of 26 level shifters are distributed across the system to up-convert control signals from the V_{DD} logic domain to the boosted $2V_{\text{DD}}$ domain. Each level shifter consists of a differential input pair and cross-coupled pull-up devices, all implemented using I/O transistors to ensure safe operation under the boosted voltage. This topology enables full-swing transitions at $2V_{\text{DD}}$ while maintaining negligible static current.

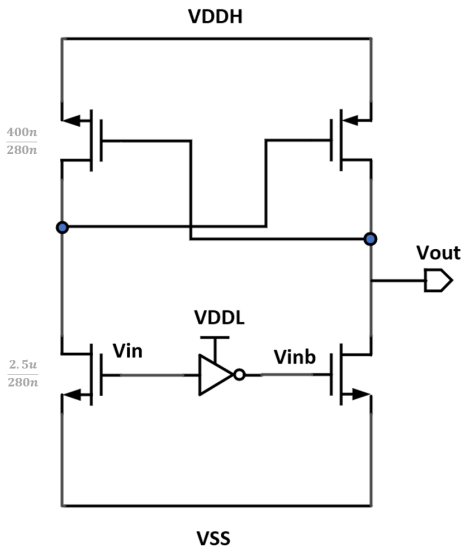


Figure 44: Circuit schematic of the level shifter.

The combination of a centralized charge pump and distributed level shifters ensures that all critical switches receive the required boosted drive signals across temperature and process corners.

3.4 Digital Controller

The digital controller is reused from the previous design [1] and is responsible for generating all the required control signals. The functionality of these signals is summarized in Table 5.

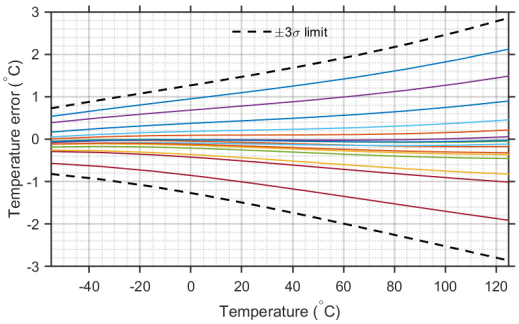
Table 5: Input and output signals of the digital controller

Signal name	**Signal type**	**Description**
SYS_CLK	Input	2-MHz System clock
SYS_RST	Input	System reset signal
BS	Input	Comparator's output bitstream
CPIN	Input	CHL input
DEM_EN	Input	Enable BS-controlled DEM
BS0	Output	Output bistream
CLK_VAL	Output	Comparator's clock
PH0N<2:0>	Output	CBD FE control signals –SW4
PH0P<2:0>	Output	CBD FE control signals –SW4
PH1	Output	DSM's phase signal
PH1E	Output	Autozero signal
PH2	Output	DSM's phase signal
PH3N<2:0>	Output	CBD FE control signals –SW2
PH3P<2:0>	Output	CBD FE control signals –SW2
RSTNB<2:0>	Output	CBD FE control signals –SW1
RSTPB<2:0>	Output	CBD FE control signals –SW1
RST_ANA	Output	Reset signal for the modulator

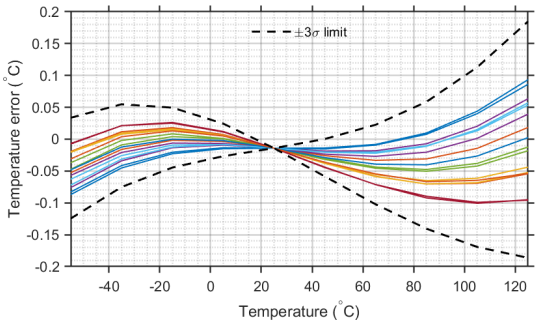
4 Simulation Results

4.1 Accuracy

In Chapter 3, the front-end with real-device implementation achieves an inaccuracy of 0.16°C after a one-point trim at 25°C when evaluated with an ideal readout stage. This leaves a margin of approximately 40 mK for the readout circuitry. The transient Monte Carlo inaccuracy (20 samples) over mismatch and process spread for the combined real front-end and real readout is shown in Fig. 45. After a one-point trim at a supply voltage of 0.9 V, the resulting inaccuracy is 0.18°C, which meets the design target.



(a) Monte Carlo inaccuracy of the SC CBD front-end with real readout without trimming.



(b) Monte Carlo PSS of the SC CBD front-end with real switches at −55°C, 25°C, and 125°C.

Figure 45: Monte Carlo inaccuracy of the SC CBD front-end with real readout with one-point trimming at 25°C.

The resulting decimated bitstream average, μ, over temperature is shown in Fig. 46. Across the full temperature range, μ varies from approximately 0.2 to 0.9.

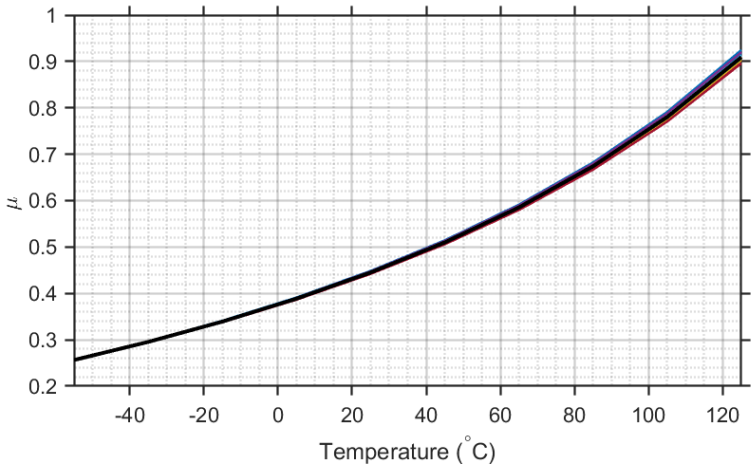


Figure 46: Monte Carlo simulated μ over temperature.

4.2 Power Supply Sensitivity

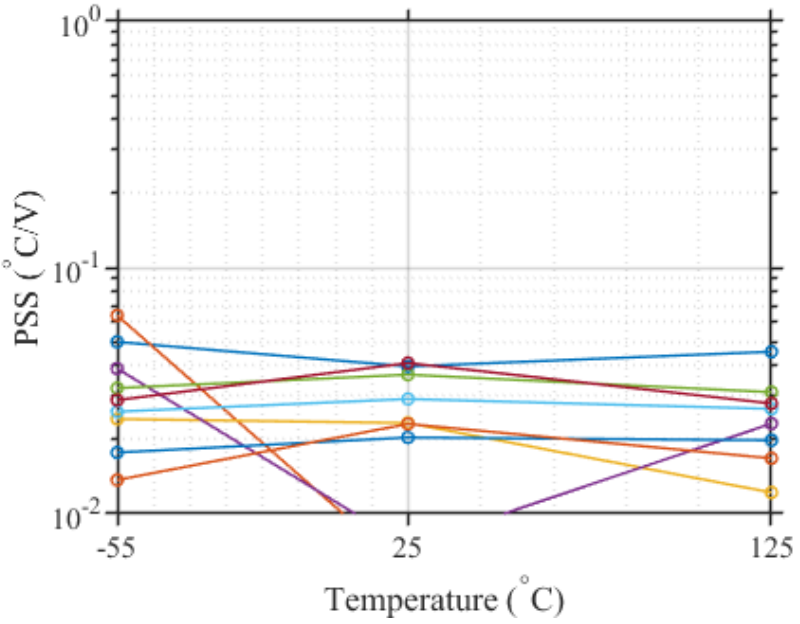


Figure 47: Monte Carlo PSS of the SC CBD front-end with real readout from −55°C to 125°C .

Monte Carlo simulations (10 samples) over mismatch and process spread were performed at three temperatures: −55°C, 25°C, and 125°C, with the supply voltage swept from 0.9 V to 1.4 V. As shown in Fig. 47, the sensor achieves a PSS of 0.05°C/V across the entire temperature range. Thanks to the use of an LDO-based RCP, the PSS is effectively controlled over the full PVT space. The remaining PSS error is primarily attributed to switch non-idealities.

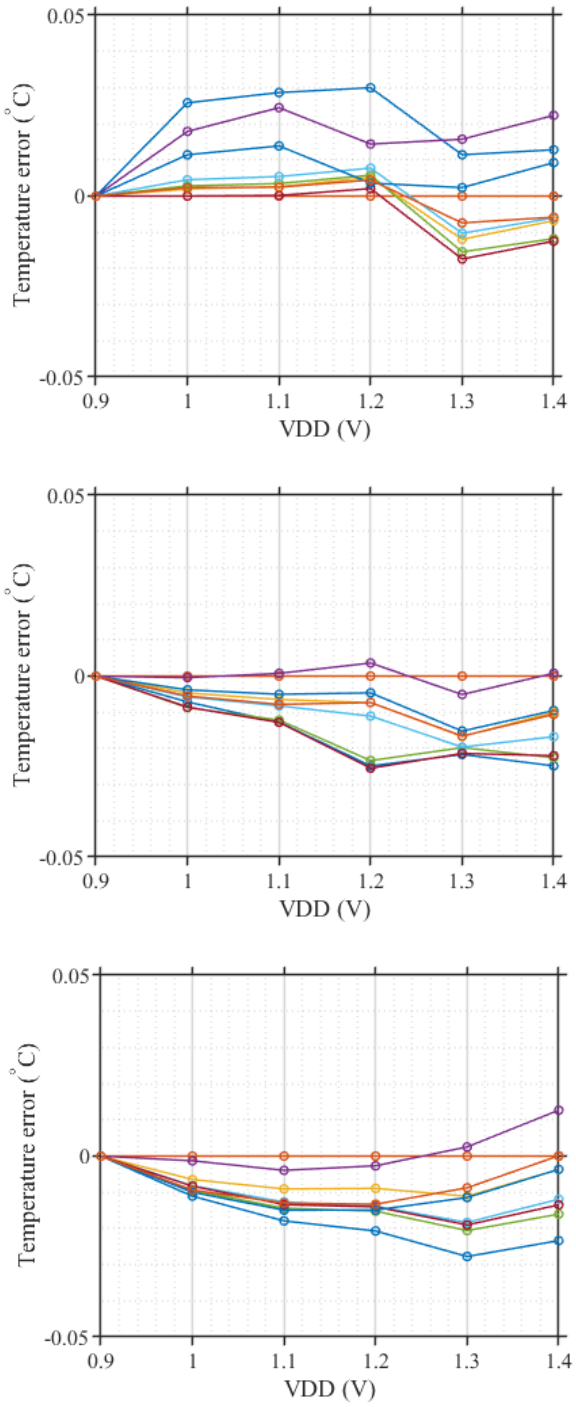


Figure 48: Monte Carlo simulation of temperature error over supply voltage for $-55°C$,$25°C$ and $125°C$.

4.3 Power Dissipation

Figure 49 shows the simulated power breakdown at a supply voltage of 0.9 V. The digital circuitry consumes approximately 110 nW. The analog circuitry accounts for the remaining 475.3 nW, with the first integrator being the dominant contributor at roughly 210 nW.

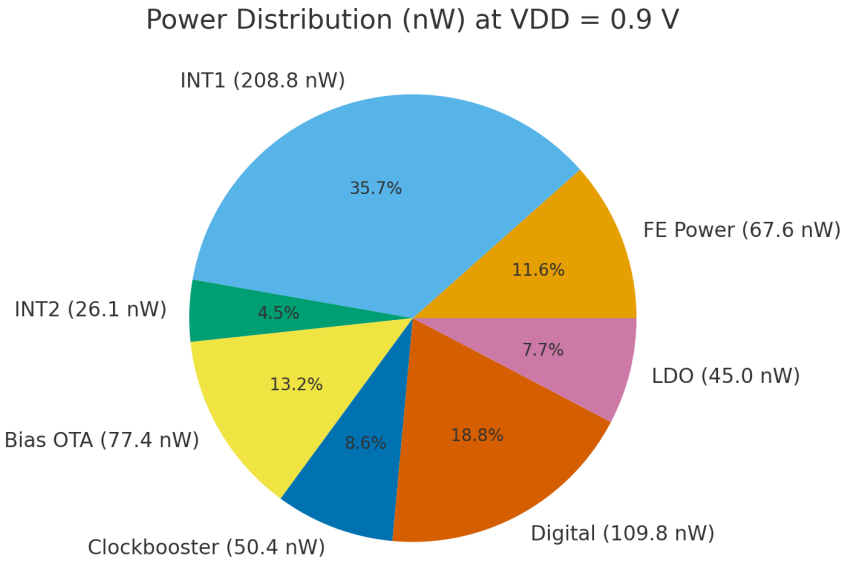


Figure 49: Simulated total power consumption breakdown at 0.9V supply.

4.4 Resolution

The FFT of the modulator's bitstream output at room temperature is shown in Fig. 50. The expected second-order noise shaping is clearly visible.

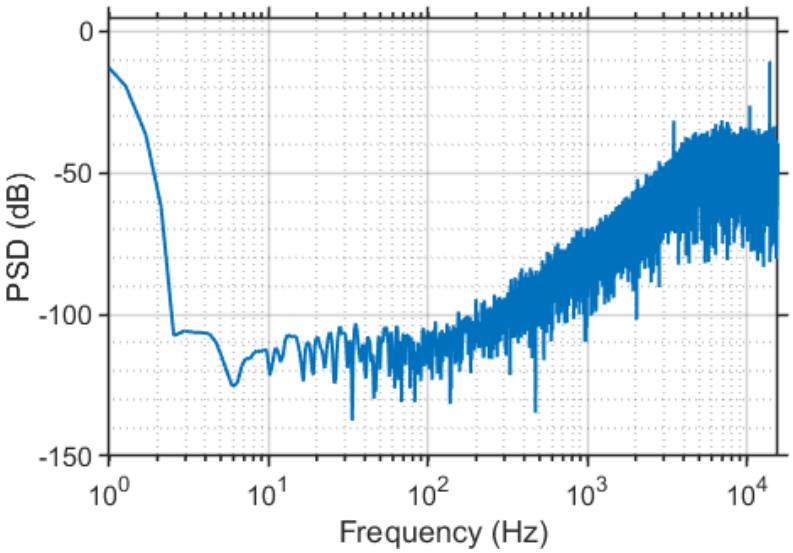


Figure 50: FFT of the sensor's bitstream at 25 °C.

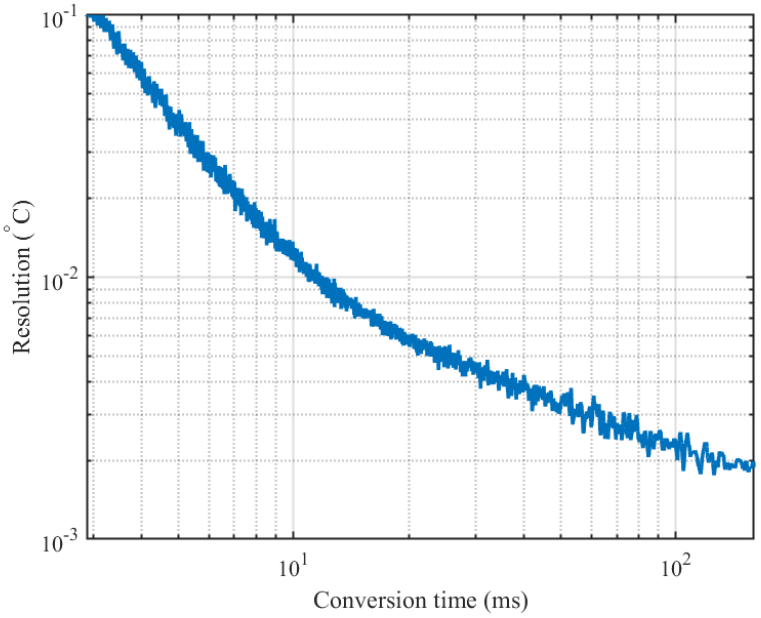


Figure 51: Resolution versus conversion time.

The simulated resolution as a function of conversion time is shown in Fig. 51. For short conversion times (< 20 ms), the resolution is limited by quantization noise. Beyond approximately 20 ms, thermal noise becomes dominant. At a conversion time of 64 ms—corresponding to an OSR of 1000 and 2000 modulator cycles—it achieves a resolution of 2.8 mK.

4.5 Figure of Merit

The figure of merit for a temperature sensor can be calculated as:

$$\text{FoM} = \text{Resolution}^2 \times T_{\text{conv}} \times \text{Power} \tag{4.1}$$

As mentioned in the previous section, the sensor consumes 585.1 nW and achieves a resolution of 2.8 mK at a conversion time of 64 ms. This corresponds to a FoM of approximately $0.3\,\text{pJ} \cdot \text{K}^2$, which is of the same order as the previous design.

4.6 Summary

Table 6 summarizes the performance of the CB BJT-based temperature sensor and compares it with previous work. The simulated results show that the proposed 65-nm design achieves the best reported PSS (0.05 °C/V) while maintaining a FoM comparable to earlier designs.

Table 6: Performance summary and comparison to the state-of-the-art.

Specification	**This Work**	**SSCL'19 [17]**	**JSSC'23 [1]**	**VLSI'24 [3]**
Process	65 nm	16 nm FinFET	180 nm	22 nm
Device Type	PNP	Diode	PNP	PNP
Supply [V]	0.9	0.85–1	0.95–1.4	0.8–1.1
Power [μW]	0.59	18	0.81	2.9
Temp. Range [°C]	–55 to 125	–15 to 105	–55 to 125	–40 to 125
Inaccuracy [°C]	±0.2 (1-pt)	+1.5/ − 2 (0-pt)	±0.45 (0-pt) ±0.15 (1-pt)	±1.25 (0-pt) ±0.4 (1-pt)
RIA [%]	0.23 (1-pt)	2.9 (0-pt)	0.5 (0-pt) 0.17 (1-pt)	1.5 (0-pt) 0.48 (1-pt)
PSS [°C/V]	0.05	1.5	0.2	0.58–1.3 (RT)
Resolution [mK]	2.8	300	1.8	4.7
Conv. Time [ms]	64	0.013	128	6.4
Res. FoM [pJ·K^2]	0.3	21	0.34	0.41

(0-pt = no individual trim; 1-pt = one-point trim.)
Resolution FoM = (Energy per conversion)·(Resolution)^2.

5 Conclusion

5.1 Conclusion

A 0.59 μW, 0.9-V operable capacitively-biased BJT-based temperature sensor has been designed in a 65-nm CMOS process. This work presents an enhanced version of the temperature sensors reported in [1,3], with two key contributions: (1) evaluating the feasibility of implementing a capacitively-biased BJT temperature sensor in a scaled 65-nm technology, and (2) improving the PSS performance by identifying the intrinsic PSS limit of the CB-BJT structure, introducing a new RCP architecture, and carefully optimizing the switch design. As a result, the proposed design achieves a tenfold improvement in PSS, reaching 0.05 °C/V. After one-point calibration, the sensor attains a simulated inaccuracy of ± 0.2 °C (3σ) over the -55°C to 125°C range. These results demonstrate that capacitively-biased BJT-based temperature sensing can be effectively realized in a 65-nm process while maintaining accuracy comparable to 180-nm implementations, making it well suited for ultra-low-power IoT applications.

5.2 Future Work

5.2.1 Reducing the conversion time

Compared with previous CBD-based temperature sensors [1,3], this work employs an OSR of 1000, resulting in a conversion time of approximately 64 ms. However, as shown in Fig. 52, the optimal FoM is achieved at a shorter conversion time corresponding to a smaller OSR. Operating the modulator at this point would increase the sensor's speed while still maintaining near-optimal energy efficiency.

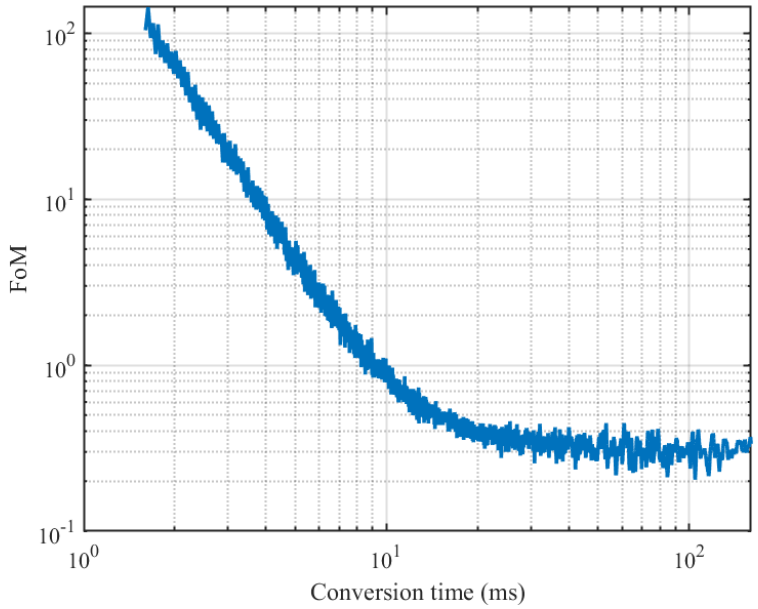


Figure 52: Figure of Merit versus conversion time.

Another way to reduce the conversion time while maintaining the same OSR is to shorten the discharge interval of the front-end BJTs. To preserve both accuracy and PSS performance, the discharge time must be carefully optimized based on Fig. 23b and Fig. 13. These figures illustrate the strong dependence of accuracy and PSS on the chosen discharge interval and biasing conditions, highlighting the need to carefully balance these parameters in future designs.

5.2.2 Increasing the energy efficiency

The integrators are the most power-hungry blocks in this design. Due to the auto-zero (AZ) nature of the amplifier, they do not operate continuously throughout the conversion cycle. The AZ capacitor acts as a level shifter, and, ideally, if no leakage occurs, the amplifier could remain active after the AZ capacitor samples the required bias, offset, and $1/f$ noise information, without requiring further auto-zeroing.

However, in a 65-nm process, capacitor leakage can reach approximately 2.5 pA at high temperatures. An interesting direction for future work is therefore to investigate how long the AZ capacitor can reliably maintain its stored voltage, and whether this would allow the amplifier to operate in a more continuous manner.

Since the switched-capacitor nature of the front-end does not provide continuous-time V_{BE} or ΔV_{BE} information, a ping-pong architecture becomes a promising alternative. In such an approach, two CBD front-end sections operate in an alternating fashion. During Φ_1, the first section performs reset and discharge, capturing ΔV_{BE} or V_{BE}, while the second section transfers the sampled charge to the integrator. During Φ_2, the roles are reversed.

This architecture introduces several design challenges. First, the digital clock-generation and error-correction logic becomes more complex. Second, AZ-capacitor leakage requires a carefully designed reset phase to ensure accurate level shifting. Finally, continuous operation of the integrator may cause crosstalk between the two CBD sections, potentially introducing additional errors.

5.2.3 Decreasing the area

The auto-zero capacitor in the integrator is sized large to minimize KT/C noise and to avoid charge sharing with the input pair's gate parasitics. However, with chopping as described in [3], the KT/C noise generated during each auto-zero phase is effectively averaged out. As a result, the sizing requirement of the AZ capacitor can be relaxed significantly. In future designs, the capacitor only needs to be sufficiently larger than the input transistor parasitic capacitance, allowing a substantial reduction in area.

References

[1] Z. Tang, S. Pan, M. Grubor, and K. A. Makinwa, "A sub-1 v capacitively biased bjt-based temperature sensor with an inaccuracy of±0.15 c (3 σ) from- 55 c to 125 c," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 12, pp. 3433–3441, 2023.

[2] M. A. Pertijs and J. Huijsing, *Precision temperature sensors in CMOS technology*. Springer Science & Business Media, 2006.

[3] Z. Tang, H. Wang, X. Yu, K. A. Makinwa, and N. N. Tan, "A 0.8v capacitively-biased bjt-based temperature sensor with an inaccuracy of ±0.4°c ($\mathbf{3}\sigma$) from 40°c to 125°c in 22nm cmos," in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2024, pp. 1–2.

[4] N. G. Toth and K. A. A. Makinwa, "27.4 a bjt-based temperature sensor with an 80fj.k2 resolution fom," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 476–478.

[5] S. Pan, "Resistor-based temperature sensors in cmos technology," Dissertation, Delft University of Technology, 2021. [Online]. Available: https://doi.org/10.4233/uuid:28108302-2d9b-4560-a806-8ba6d381812e

[6] S. Pan, J. A. Angevare, and K. A. A. Makinwa, "5.4 a hybrid thermal-diffusivity/resistor-based temperature sensor with a self-calibrated inaccuracy of ±0.25° c(3) from -55°c to 125°c," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 78–80.

[7] C. P. van Vroonhoven, D. d'Aquino, and K. A. Makinwa, "A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of ±0.2°c (3s) from 55°c to 125°c," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 314–315.

[8] U. Sönmez, F. Sebastiano, and K. A. Makinwa, "11.4 1650µm2 thermal-diffusivity sensors with inaccuracies down to ±0.75°c in 40nm cmos," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 206–207.

[9] W. Wang, L. Jiang, S. Dutta, Y. Su, Z. Chen, Z. Yu, C. Kemere, and K. Yang, "A 36nw cmos temperature sensor with ¡0.1k inaccuracy and uniform resolution," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2023, pp. 1–2.

[10] M. Eberlein, G. Panagopoulos, and H. Pretl, "A 40nw, sub-iv truly 'digital' reverse bandgap reference using bulk-diodes in 16nm finfet," in *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2018, pp. 99–102.

[11] D. A. Neamen and D. Biswas, *Semiconductor physics and devices*. McGraw-Hill higher education New York, 2011.

[12] K. Souri and K. A. Makinwa, *Energy-efficient smart temperature sensors in CMOS technology*. Springer, 2017.

[13] M. Terauchi, "Temperature dependence of the subthreshold characteristics of dynamic threshold metal–oxide–semiconductor field-effect transistors and its application to an absolute-temperature sensing scheme for low-voltage operation," *Japanese Journal of Applied Physics*, vol. 46, no. 7R, p. 4102, 2007.

[14] K. Souri, Y. Chae, F. Thus, and K. Makinwa, "12.7 a 0.85v 600nw all-cmos temperature sensor with an inaccuracy of ±0.4°c (3) from 40 to 125°c," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 222–223.

[15] E. H. Hellen, "Verifying the diode–capacitor circuit voltage decay," *American Journal of Physics*, vol. 71, no. 8, pp. 797–800, 2003.

[16] M. A. Pertijs, K. A. Makinwa, and J. H. Huijsing, "A cmos smart temperature sensor with a 3inaccuracy of 0.1 c from- 55 c to 125 c," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, 2005.

[17] M. Eberlein and H. Pretl, "A no-trim, scaling-friendly thermal sensor in 16nm finfet using bulk diodes as sensing elements," *IEEE Solid-State Circuits Letters*, vol. 2, no. 9, pp. 63–66, 2019.

[18] N. G. Toth and K. A. A. Makinwa, "A background-calibrated npn-based temperature sensor with 0.05°c (3σ) inaccuracy from –70°c to 125°c," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2026, to be published.

[19] J. Huijsing, *Operational amplifiers*. Springer, 2011.