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A Transformerless Single-Phase Symmetrical Z-Source HERIC Inverter with Reduced Leakage Currents for PV Systems

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Abstract— **A transformerless single-phase symmetric Z-source HERIC inverter featuring low leakage currents is presented in this paper. It is an attempt to utilize the Highly Efficient and Reliable Inverter Concept (HERIC) and an impedance source (Z-source) network to maintain a constant common mode voltage and thus low leakage currents in PV applications. The symmetric Z-source HERIC inverter requires two extra active switches. Nevertheless, the operation frequency of the two switches is the line frequency, leading to negligible losses. More importantly, the performance in terms of low leakage currents and harmonics is improved. Experimental tests are performed to validate the analysis and performance of the proposed system.**

I. INTRODUCTION

The energy industry has experienced a rapid change in the last decades. The energy paradigm has shifted from fossil fuels to environmentally friendly energy sources with a high growth rate. For instance, the capacity of the installed photovoltaic (PV) systems in 2015 (i.e., approximately 227 GW) was more than the double of that in 2012 (i.e., around 100 GW) [1]. This high penetration of PV sources is mainly driven by the continuous declination of PV module price and the increasing demand for renewable energy systems. At the same time, the power electronic technology is also advancing [2], enabling more flexible and reliable PV systems.

The development of PV systems is mainly efficiency- and reliability-driven. Thus, the DC-link voltage for PV systems is increasing (e.g., 1500 V). In addition, the elimination of isolation transformers, known as transformerless topologies, contributes to a better performance in terms of power density and efficiency. Transformerless PV systems nowadays are widely used [3], [4], which typically consist of a DC-DC converter and a DC-AC voltage source inverter. The first-stage is employed to track the maximum power point by regulating the low and varying voltage of the PV panels [5]-[7]. While the second-stage is utilized as an interface to deliver the power to the grid [8]-[10]. Recently, single-phase single-stage PV inverters, especially impedance source (Z-source) based inverters, draw much attention due to its high voltage-boosting capability [11]-[13], enabling a single-stage step-up DC-AC inversion. Although the Z-source inverter was firstly developed for motor drives [14], intensive research focusing on renewable energy applications has been reported in the past years, e.g., in terms of dc-link voltage shaping for reducing the requirement of large dc capacitors [15], high voltage gain for grid-connected PV applications [16], and reduced leakage currents for grid-tied inverters [17].

To reduce the leakage currents, the common mode voltage of PV inverters should be maintained constant through modulations or topological improvements [17]. Many PV topologies like the HERIC, H5, and H6 are modifications of the conventional H-bridge inverter can achieve constant common mode voltages [18]. Unfortunately, a boost DC/DC converter is normally adopted in such systems, leading to a relatively low efficiency, especially when the PV voltage is low. Furthermore, impedance source networks cannot be directly connected in-between the PV panels and the transformerless topologies due to the required shoot-through operation. Solutions to this challenge are to modify modulation strategies or switching patterns and therefore alleviate the variation of the common mode voltage [19], [20]. In addition, three-level impedance source inverters would be promising if the voltage gain is not sacrificed [21]. In all, it calls for advanced transformerless inverters with high voltage boost capabilities.

In light of the above, this paper proposes a single-phase symmetrical Z-Source HERIC inverter and the corresponding modulation strategy is also discussed. The proposed inverter features a constant common mode voltage without affecting the performance of the impedance source network, and thus the merit of low leakage currents remains. The steady-state operation principles and common mode voltage analysis are explained in § II. Following the analysis, two variations of the symmetrical Z-source HERIC inverter with clamping are discussed in § III. Simulations and experiments are conducted in § IV, where not only the proposed symmetrical Z-source HERIC inverter is tested but also the conventional Z-source H-bridge inverter to verify the performance. Finally, concluding remarks are provided in § V.

II. STEADY-STATE ANALYSIS OF THE SYMMETRIC Z-SOURCE HERIC INVERTER

Fig. 1 shows the schematic of the symmetrical Z-source HERIC inverter system, which consists of a symmetrical Z-source network, a HERIC inverter, and an L-filter network (two identical L_r). One modulation strategy is shown in Fig. 2.
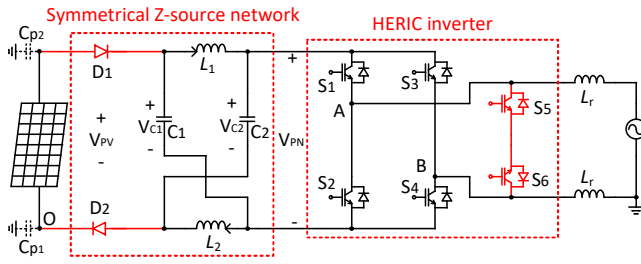
Fig. 1. Hardware schematic of the proposed symmetrical Z-source HERIC inverter system, where C_{p1} and C_{p2} are the parasitic capacitors.
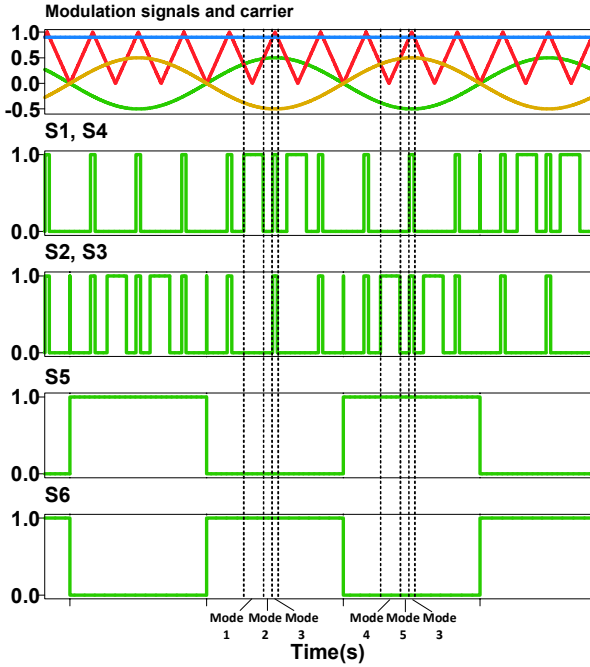

Fig. 2. Modulation signals, carrier, and gate driving signals of the proposed symmetrical Z-source HERIC inverter.
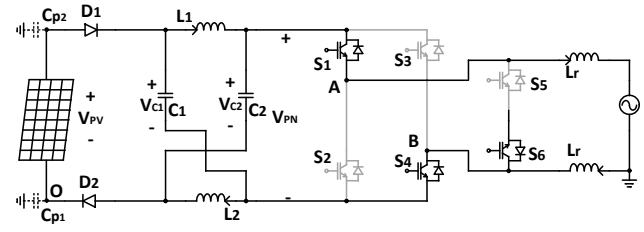

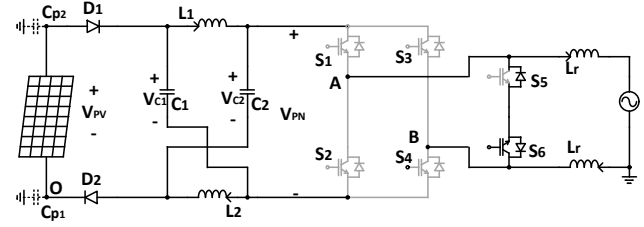Fig. 3. Switching states of the proposed inverter in Mode 1.

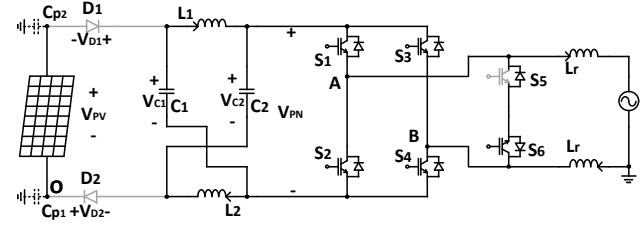Fig. 4. Switching states of the proposed inverter in Mode 2.

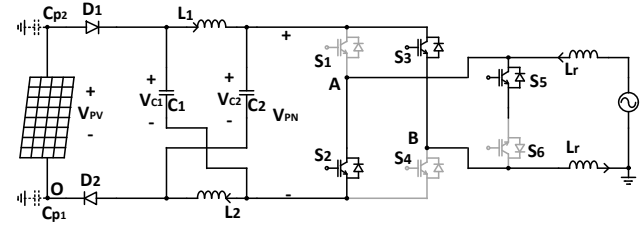Fig. 5. Switching states of the proposed inverter in Mode 3.

Fig. 6. Switching states of the proposed inverter in Mode 4.

Fig. 7. Switching states of the proposed inverter in Mode 5.

In the case of a unity power factor operation, two sinusoidal signals with 180° phase difference (yellow and green) for the AC output and a DC signal (blue) for the shoot-through state are utilized as the modulation signals, the inverter has five switching behaviors denoted as Mode 1 to Mode 5, as shown in Fig. 2. The switching modes depicted in Fig. 3 – Fig. 7 are used to elaborate the steady-state operation principle of the proposed inverter. In the steady-state operation, the voltage stress of switches $S_1 - S_4$ are equal, the voltages stresses of the diodes D_1 and D_2 are equal and the voltages of the capacitors V_{C1} and V_{C2} are equal as well.

A. Differential Mode and Common Mode Voltages in Mode 1

In this operation mode, the switches S_1, S_4, and S_6 are switched on while the rest are off (see Fig. 3). The inverter output is a positive vector during this period. Therefore, the differential mode (DM) voltage V_{AB} equals to the maximum dc-link voltage V_{PN}. The common mode (CM) voltage is calculated.

$$V_{DM} = V_{AO} - V_{BO} = V_{C2} + V_{in} - V_{C1} = V_{PN} \tag{1}$$

$$V_{CM} = \frac{V_{AO} + V_{BO}}{2} = \frac{V_{C2} + V_{in} - V_{C1}}{2} = \frac{V_{in}}{2} \tag{2}$$

where V_{DM} and V_{CM} are the inverter DM and CM voltages, respectively and the other voltage variables of the inverter are denoted in Figs. 1 and 3.

B. Differential Mode and Common Mode Voltages in Mode 2

In this period, only the switch S_6 is on while the rest switches are off, as shown in Fig. 4. Because of the continuous of the

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inductor current, the body diode of S_5 is conducted as well for freewheeling. Hence, the inverter output is a zero vector. Consequently, the DM voltage V_{AB} equals to zero. The CM voltage in this case is calculated as

$$V_{DM} = V_{AO} - V_{BO} = 0 \qquad (3)$$

$$V_{CM} = \frac{V_{AO} + V_{BO}}{2}$$
$$= \frac{1}{2}\left[\left(\frac{V_{C2} + (V_{in} - V_{C1})}{2}\right) + \left(\frac{V_{C2} + (V_{in} - V_{C1})}{2}\right)\right] = \frac{V_{in}}{2}. \qquad (4)$$

C. Differential Mode and Common Mode Voltages in Mode 3

In this interval, the switches S_1, S_2, S_3, and S_4 are on for charging the inductor L_1 and L_2 (see Fig. 5) as shoot-through stage. While the switch S_6 and the body diode of S_5 remain conducting for freewheeling. Accordingly, the DM and CM voltages can be written as

$$V_{DM} = V_{AO} - V_{BO} = 0 \qquad (5)$$

$$V_{CM} = \frac{V_{AO} + V_{BO}}{2}$$
$$= \frac{(-V_{D2} + V_{C2}) + (V_{in} + V_{D1} - V_{C1})}{2} = \frac{V_{in}}{2}. \qquad (6)$$

D. Differential Mode and Common Mode Voltages in Mode 4

In Mode 4, the switches S_2, S_3, and S_5 turn on, and the output voltage is negative voltage vector, as illustrated in Fig. 6. The analysis is similar to that shown in section II-A. Accordingly, the DM and CM voltages can be obtained as

$$V_{DM} = V_{AO} - V_{BO} = V_{C2} - V_{C1} + V_{in} = -V_{PN} \qquad (7)$$

$$V_{CM} = \frac{V_{AO} + V_{BO}}{2}$$
$$= \frac{(-V_{D2} + V_{C2}) + (V_{in} + V_{D1} - V_{C1})}{2} = \frac{V_{in}}{2}. \qquad (8)$$

E. Differential Mode and Common Mode Voltages in Mode 5

In this stage, only is S_5 turned on while the rest are off (see Fig. 7). Due to the grid current, the body diode of S_6 is conducted for freewheeling as well. The inverter output is a zero vector. Therefore, the DM voltage V_{AB} equals to zero. The CM voltage is calculated as

$$V_{DM} = V_{AO} - V_{BO} = 0 \qquad (9)$$

$$V_{CM} = \frac{V_{AO} + V_{BO}}{2}$$
$$= \frac{1}{2}\left[\left(\frac{V_{C2} + (V_{in} - V_{C1})}{2}\right) + \left(\frac{V_{C2} + (V_{in} - V_{C1})}{2}\right)\right] = \frac{V_{in}}{2}. \qquad (10)$$

It is clearly shown in the above analysis that the CM voltage of the proposed Z-source HERIC inverter remains constant
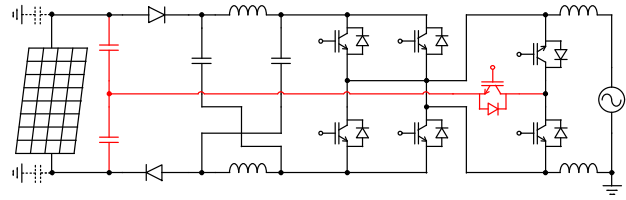

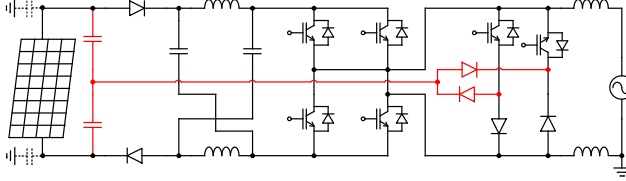Fig. 8. A symmetric Z-source HERIC inverter with an active clamping path.

Fig. 9. A symmetrical Z-source HERIC inverter with a passive clamping path.

during operation. In other words, the inverter features a constant CM voltage in steady state, and thus leading to reduced leakage currents. It is worth mentioning that the switching frequency of S_5 and S_6 is the line frequency, i.e., the same as that for the conventional HERIC inverter, resulting in extremely low switching losses. Thus, the high efficiency is maintained in the proposed inverter.

III. SYMMETRIC Z-SOURCE HERIC DERIVED TOPOLOGIES

HERIC inverters have topological derivations and are connected to the symmetrical Z-source network with minor modifications while still maintaining constant CM voltage. In Figs. 8 and 9, symmetrical Z-source HERIC inverters with an active clamping and passive clamping path are presented. Their operation principles are similar to that of the symmetrical Z-source HERIC inverter. The clamping point is benefitial to a more stable CM voltage, although two extral DC capacitors are adopted. These two solutions have their own pros and cons. In terms of power losses, the active clamping solution (see Fig. 8) features lower conduction losses because only one active clamping switch is used, while two calmping diodes are used in the passive solution (see Fig. 9). However, the passive solution is easier to use and more robust because no extra isolated gate driver is needed. The use of these two solutions depends on the requirement of the application.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The symmetric Z-source network is built by using two STW28N65M2 MOSFET as diodes, two Bourns 1140 inductors and two Nichicon UCP2G121MHD capacitors. The HERIC inverter is constructed by using six STW28N65M2 MOSFETs. The operation conditions are shown as follows: input voltage Vin is 60 V, and the maximum DC-link voltage VPN is approximately 280 V. Hence, the inverter output voltage is set as 110 V (root mean square), and the output power is 100 W with a resistive load, in which the two filter inductors L_r are of 3.3 mH. Comparisons with an Z-source H-bridge inverter, a symmetrical Z-source H-bridge inverter, and an Z-source HERIC inverter are carried out.
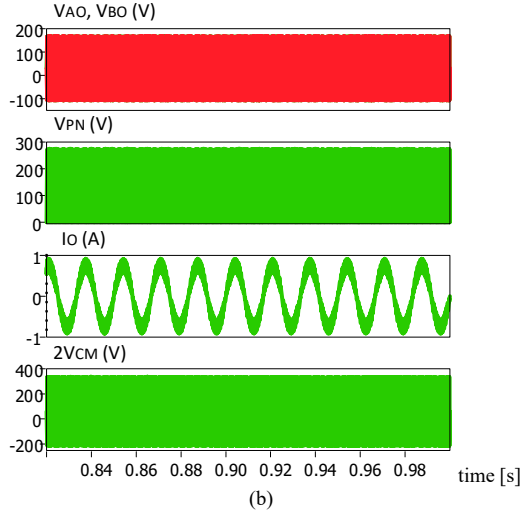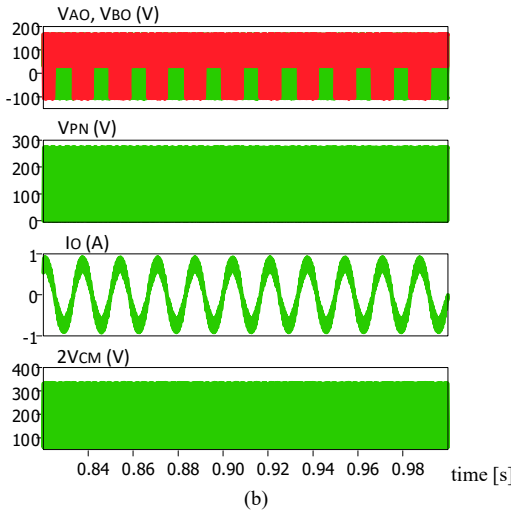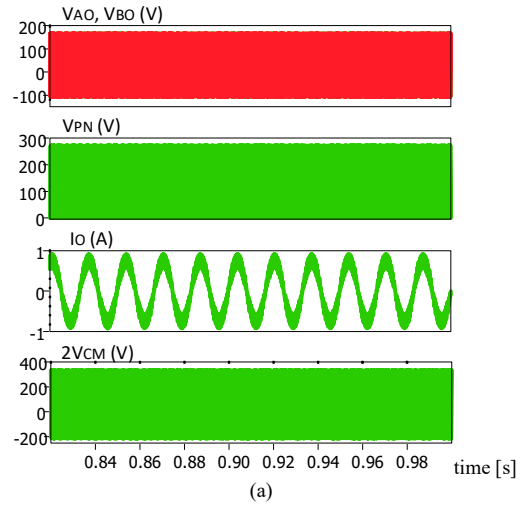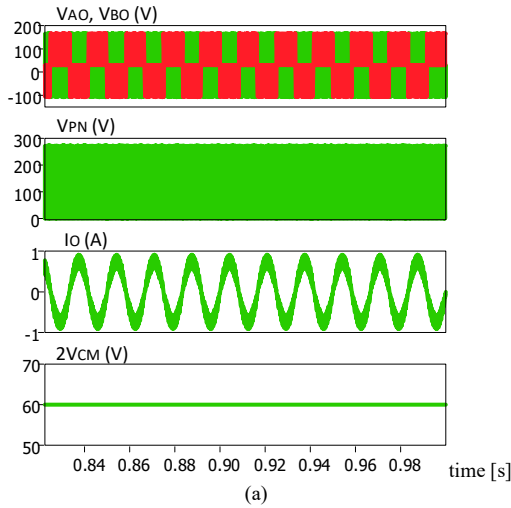
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Fig. 10. Simulation results of impedance source based inverters (V_{AO} and V_{BO}; V_{PN}; I_O; $2V_{CM} = V_{AO} + V_{BO}$): (a) the proposed symmetrical Z-source HERIC inverter and (b) the Z-source HERIC inverter.

Fig. 11. Simulation results of impedance source based inverters (V_{AO} and V_{BO}; V_{PN}; I_O; $2V_{CM} = V_{AO} + V_{BO}$): (a) the Z-source H-bridge inverter, and (b) the symmetrical Z-source H-bridge inverter.

A. Simulation results

Simulation results of the proposed symmetrical inverter and other Z-source topologies are shown in Figs. 10 and 11. It is observed in Fig. 10(a) that the proposed symmetrical Z-source HERIC inverter features a constant common mode voltage whilst the others (Fig. 10a and Fig. 11) show a large variation of the common mode voltage. The simulation results in Fig. 10(a) indicate that the symmetrical Z-source HERIC inverter has a better performance in terms of a constant common mode voltage and thus the leakage current is suppressed.

B. Experimental results

Experimental results are shown in Fig. 12. It is observed in Fig. 12(a) that the proposed symmetrical Z-source HERIC inverter presents a CM voltage with the least variation among these four inverters, and thus the corresponding leakage current is the lowest. These results verify the concept to reduce the leakage current with the proposed solution.

For a quantitative analysis, a 220-nF capacitor is connected between point O and the ground as an emulated capacitor. The

root mean square value of the capacitor are recorded as an indicator representing the suppression of leakage currents. The measured results with different output power of the simulation models is shown in Fig. 13. It is observed in Fig. 13 that the proposed symmetrical Z-source inverter has better performances compared to the other three configurations. It is further seen in Fig. 13 that an approximately 95% reduction of the leakage current (root mean square) compared with that of the conventional Z-source H-bridge inverter. The quantitative comparison results further confirm the proposed solution and show the superiority in terms of leakage current suppression in transformerless PV applications.

V. CONCLUSIONS

A symmetrical Z-source HERIC inverter has been presented and studied in this paper. Two symmetrical Z-source HERIC variants were also derived by adding the active and passive clamping path. The common mode voltage (indirectly reflects the leakage currents) for the proposed inverter has also been analyzed in details in this paper. The analysis indicates that the
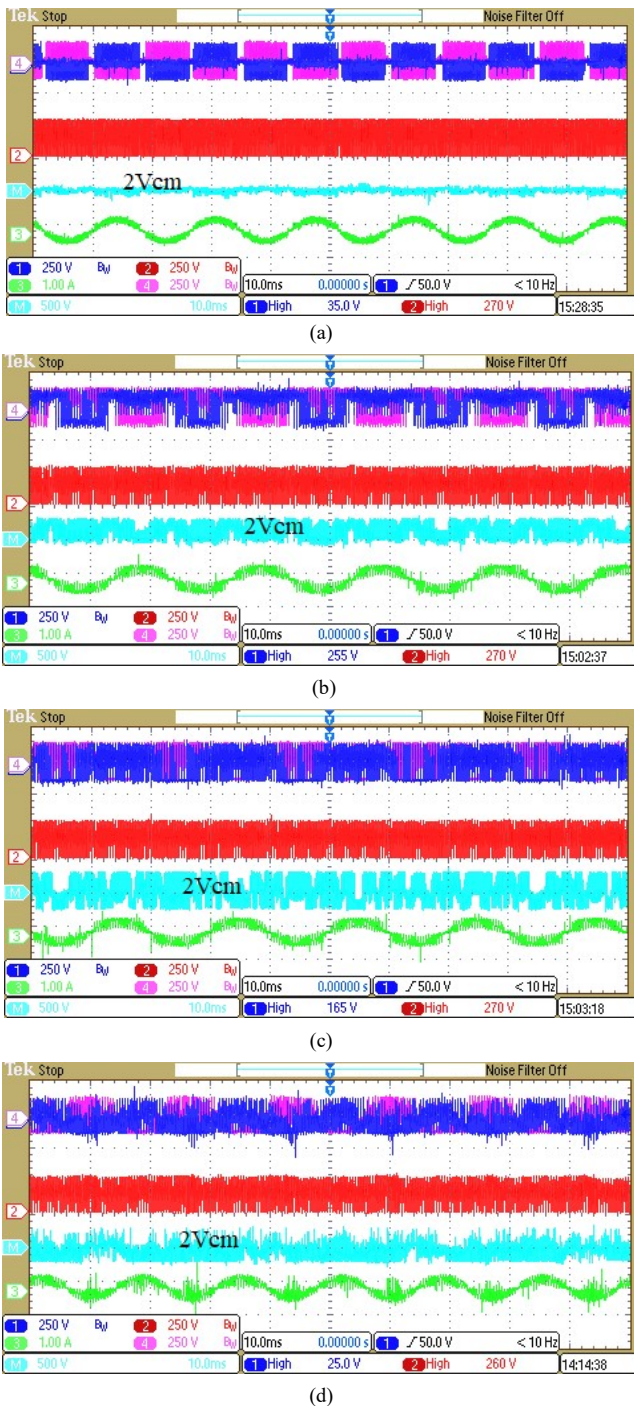
Fig. 12. Experimental results of impedance source based inverters (CH1: V_{AO} [250 V/div], CH2: V_{dclink} [250 V/div], CH3: I_o [1A /div], CH4: V_{BO} [250 V/div], CHM: $2V_{CM} = V_{AO} + V_{BO}$ [250 V/div], time [10 ms/div]): (a) the proposed symmetrical Z-source HERIC inverter, (b) the Z-source HERIC inverter, (c) the Z-source H-bridge inverter, and (d) the symmetrical Z-source H-bridge inverter.

symmetrical Z-source HERIC inverter maintains a constant common mode voltage during operation. Thus, the resultant leakage currents are low, and lower harmonics as well. Experimental results of the impedance source based inverters, including the proposed symmetrical Z-source HERIC inverter,
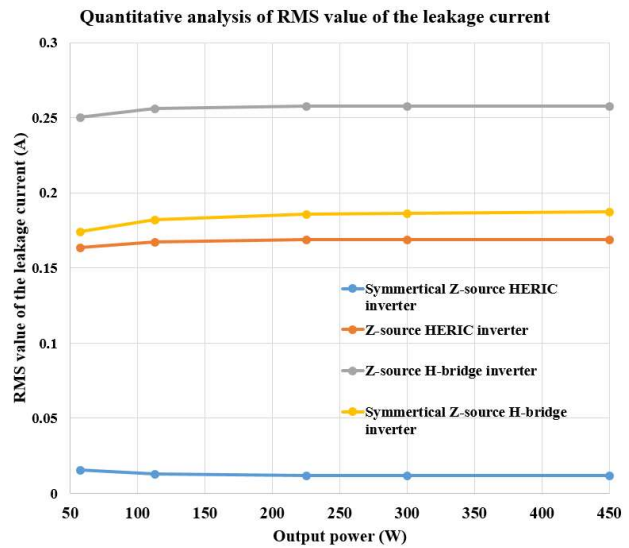

Fig. 13. Comparison of the leakage currents in four transformerless impedance source based inverters.

the Z-source HERIC inverter, the symmetrical Z-source H-bridge inverter and the Z-source H-bridge inverter have been provided. It has been demonstrated by the experiments that the proposed symmetrical Z-source HERIC inverter features an almost constant common mode voltage, which leads to low leakage currents.

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