Contents

Chapter 1

Introduction

In this chapter, background knowledge of the capacitive sensors will first be given in Section 1.1. followed by the motivation for this thesis project, which will be discussed in Section 1.2. Finally, the thesis organization will be presented in Section 1.3.

1.1 Capacitive Sensors

Accurate, relatively cost effcient, and suitable to be implemented in modern IC technology, capacitive sensor systems can be a good, even optimal solution for many different types of measurement and sensing problems. Capacitive sensor systems are being used in various types of applications, including industrial applications like displacement [1] and angular measurement [2], liquid level measurement [3], surface flatness measurement [4]and applications that are more related to our daily life, such as the accelerometers and gyroscopes used in car air-bags [5] and toys such as wii consoles [6] , the pressure sensors [7] used in our laptop fingerprint recognition systems and the electronic microphones [8] used by almost everyone.

1.1.1 Capacitive Sensor Basics

Capacitive sensors electronically measure the capacitance between two electrodes, which can be translated into the physical quantities we would like to know, such as displacement, material properties, etc. The most common type of configuration of capacitive sensor is simply capacitors with two parallel electrodes.

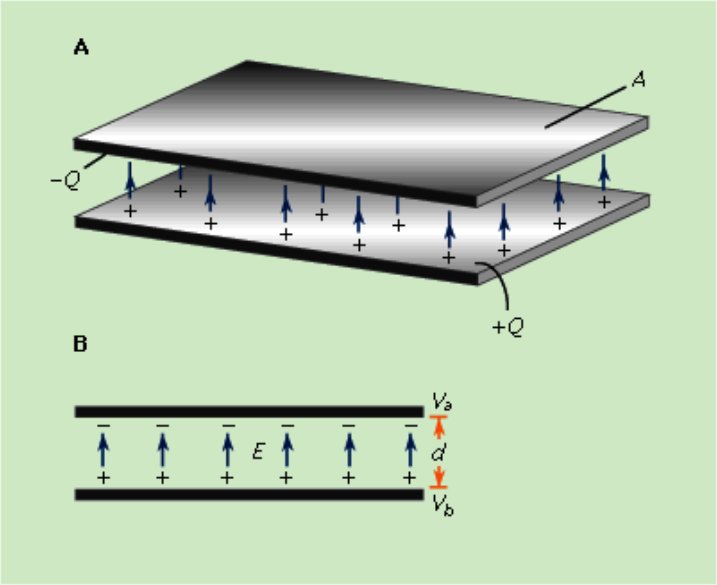

Figure 1.1: Parallel-plate capacitor. (A) This storage device consists of two flat conducting plates, each of area A. (B) These plates are parallel and separated by a small distance d

For this kind of structure, as shown in Fig 1.1, the capacitance C_0 between the two electrodes with surface area A, which is separated by a small distance d and a dielectric with permittivity ε, equals to:

$$C_0 = \varepsilon \frac{A}{d} \tag{1.1}$$

It should be noted that any imperfection of this electrode configuration, such as field bending effect or non-homogeneity of the dielectric, are not

Application	Input Non-electric signal	Intermediate variable
Angular Encoder	Rotation or Displacement	Overlapping Area
Pressure Sensor	Mechanical Force or Pressure	Distance
Humidity Sensor	Humidity	Permittivity
Motion Detection	Movement	All Possible

Table 1.1: Overview of capacitive sensor, their input signal, and sensing principle

shown in Eq 1.1.

As we can see, the capacitance is determined by three parameters: overlapping area, distance between the electrode, and permittivity. For this reason, if sensors in such a configuration are used to translate the nonelectrical signal into capacitance, all three parameters can serve as the intermediate variable, which makes it suitable for different kinds of applications:

Table 1.1 list a few applications of capacitive sensors, and their sensing principle. Sometimes several parameters could be used as the intermediate variable, and careful consideration should be applied to select the most appropriate one.

Other than two parallel plate capacitors, there are several other configurations of the electrodes, such as disks, two spheres, concentric cylinders, etc. The calculations of the capacitance are different in each case, thus providing more available intermediate variables, meaning that these structures can be used in various different applications. Detail of these calculations can be found in [9].

Depending on the application, capacitive sensors can be implemented as single ended or differential configuration, as shown in Fig 1.2

In signal ended configuration, the sensing capacitor changes with respect to the change of input non-electrical signal, and both ends of the capacitor are connected to the interface electronics (in some applications, one terminal of the sensing capacitor would be grounded). Alternatively, differential configuration, which are commonly used in MEMS accelerometers, make use

of two sensing capacitors with change in different direction with regards to the excitation. Such structures are beneficial with respect to sensitivity, and in some cases can provide linear output regarding the input signal, but are not widely used since it's difficult to build the differential structure in most of the applications.

1.1.2 Interfacing Capacitive Sensors

Capacitive sensors can translate the non-electrical signal to capacitance, but this is still not enough. What is usually needed is a signal that can be directly measured, for instance voltage, time, etc., and in most system level design the above mentioned parameters are used to communicate between the building blocks. This brings us to the issue of interfacing with capacitive sensors.

There are many ways to interface with capacitive sensors, and these can be classified by the parameters that capacitance is translated to, for example, [10] translates the change in capacitance into a voltage change, while [11] converts capacitance to frequency. There are other principles, which can be seen in Table 1.2

Another way to classify the interface is with respect to how the capacitive sensor is connected to the interface circuit. There are two basic configurations: "one-port measurement" and "two-port measurement" [13]. A very

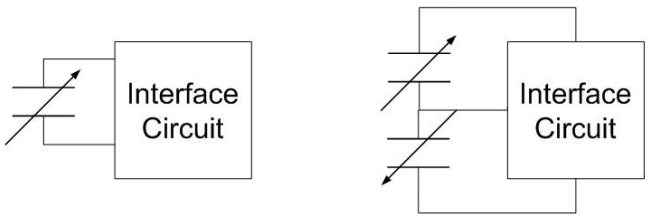

Figure 1.2: Single ended (Left) and differential (Right) configuration of capacitive sensors

Reference	Principle
[10]	Capacitance ⇒ Voltage
[11]	Capacitance ⇒ Frequency
[12]	Capacitance ⇒ Time Period

Table 1.2: Different principles of read out capacitance

important issue to consider for both configurations is the reduction, or even elimination of the negative effect of the parasitic capacitance around the capacitive sensor, which is mainly the result of the stray or cable capacitance Fig 1.3 shows the principle of operation of the one-port (left) and the two-port (right) solutions.

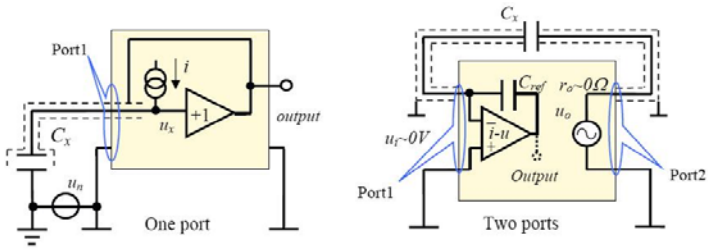

Figure 1.3: One-port (left) and two-ports (right) methods for capacitive sensor interfaces

In the configuration of the one-port measurement principle, only one terminal of the sensor is connected to the interface, and this electrode is called the sensing electrode. The other electrode is the target electrode, and in some applications can be grounded. Normally this target electrode can be connected to the already available (machine) ground, i.e. no special cable is needed, which is important for some applications, since connecting the target to the interface might not be feasible.

On the other hand, with the two-port principle, neither of the sensor electrodes is grounded. They are typically connected to the interface where the input impedance is low, which results in a reduced influence of the cable capacitance and other possible parasitic capacitors. In most cases, the two-port sensor interface demonstrates better performance with respect to

linearity and stability, but it is still not completely immune to the effects of long cables and high parasitic capacitance at the input of the interface electronics.

1.1.3 Effect of Long Connection Cables

Unlike the experimental set-up in lab conditions, most capacitive sensor systems are placed in industrial applications, where the sensor head is often located far away from the interface circuits. Such configuration brings the issue of long connection cables. Long connection cables may cause problems in two ways, as shown in Fig 1.4.

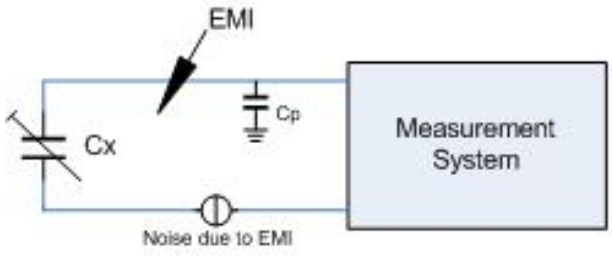

Figure 1.4: The effect and possible problems caused by long connection cables between the sensor and the interface

The first problem we have to deal with, or may want to prevent, is the parasitic capacitance C_p, due to the cable. Such parasitic capacitance is proportional to cable length and has the value of 100 pF per meter. In measurement systems using the two-port measurement principle, such parasitic capacitance appears as shunt capacitance around the sensor, where it may cause errors, since the sensing capacitor is much smaller. Things are even worse in applications using the one-port measurement principle, for example grounded capacitive sensor systems, where the parasitic cable capacitance is in parallel to the sensing capacitor, and will result in an error in accuracy. Considering the fact that the value of the cable capacitance is much larger (sometimes an order of magnitude) than the sensing capacitor, and

the uncertainty of its value (C_p may be different with different shapes of cable, even with the same length), the performance for the system could be completely jeopardized by such parasitic cable capacitance.

The other problem is related to the loop of cable, which may cause external interference, mostly electromagnetic (EMI), if the area of the loop is large. Such a closed loop will act as an antenna and pick up the nearby magnetic fields, which will cause unpredictable measurement errors. Such an issue is particularly important in industrial applications, where there's a combination of EMI source and long cabling.

1.2 Motivation

Thanks to the technique of shielding, the capacitive sensor and the interface circuit can be well-protected from the interference caused by external electromagnetic fields. What is more likely to cause a problem is the fact that the cables connecting the sensor with the electronic interface create a loop. As mentioned in the above section, such a loop acts as an antenna for magnetic fields, but creating a closed loop is unavoidable for all interface principles for capacitive sensors. The best solution for minimizing the sensitivity to external magnetic fields is to keep the area which is surrounded by the loop as small as possible, by using twisted wires for example. Unfortunately, this is not always possible, especially in industrial applications, as the routing of the two cables which connect the two sensor electrodes to the electronic interface may be different, due to other higher-priority requirements.

Therefore, the main purpose of this project is to investigate such issues, and finally to develop the interface principle and a capacitive sensor interface for use in industrial applications, where long cables have to be used. Since there's not yet any solution published regarding this issue, this thesis serves as an attempt to make a theoretical analysis and systematic approach to the development of such an interface principle.

1.3 Outline of the Thesis

This thesis is divided into six chapters to describe different aspects of the investigation and the design process. Following this introduction chapter, chapter two will introduce the investigation and a feasibility study of the problem where different possible measurement principles will be described and a comparison between them made. By studying and comparing such possible principles, the proposed principle will be determined.

Chapter three mainly deals with the behavior level analysis of the pro posed principle, where the proposed concept will be translated and converted into block diagrams, and a specification given. The design methodology that guides the whole design will also be introduced.

The circuit designs and implementation of the sensor interface will be presented in chapter four. In this chapter, detailed specifications of each building block will be calculated, and the selection of the components will also be presented. Next, the practical implementation issues of the system will be described.

In chapter five, emphasis will be placed on the initial measurement results of the system. The analysis of the results will also be presented.

Finally, in chapter six, the conclusion for this thesis will be given, including suggestions for future performance improvement work.

Chapter 2

Concept Development

This chapter presents the issue during the concept development phase of the capacitance measurement. It starts with a full and complete discussion of the problem (section 2.1), which has already been briefly described in section 1.2. After that, several possible solution in literature are presented and discussed, advantages and disadvantages are compared, and the reason why they are not suitable for this application, are given in section 2.2.

As the result of the literature study, the "two channel, out-of-phase measurement" concept is proposed in section 2.3, where the details of such concept is analyzed, including the pro's and con's. Finally the chapter is ended with a conclusion (section 2.4).

2.1 Problem Definition

As mentioned in the previous chapter, possible problems will occur when capacitive sensor systems are used in combination of long connection cables, where it is quite common in industrial applications. Actually, there are two types of problem presents with long cable: the parasitic capacitance caused by the "length" of the cable and the external interference picked up by the "shape" (loop area) of the cable, as shown in Fig 1.4

2.1.1 Possible Problems Caused by Cable Length

In industry, there's several way to solve, or to be exact, to prevent the possible problem caused by the length of the cable. One of the technique is named "Active shielding" [14], which force the voltage of the shield to track the voltage of the signal in order to prevent leakage caused by the parasitics. Detailed theory of operation about active shielding will be presented in later chapters.

2.1.2 Possible Problems Caused by the Loop Area

More investigation should be placed with respect to the second problem, since in most industrial applications, the capacitance measurement systems are placed in the environment where there's quite a few source of magnetic fields with in the cable loop. For example there may be motors, or even magnets. When the long cable and the loop presents with such source, the loop may act as antenna and the "interference" would be picked up. Such interference have two features:

Unpredictable The picked-up interference has an undefined frequency and magnitude, which may saturate the input stage and what's worse, cannot be calibrated.

Unavoidable Unfortunately, such issue is unavoidable for any measurement principles whenever big cabling loops is presented. What can be done is to minimize the loop area. But in most industrial application, where cabling routine is made by higher level specifications, it's not easy to minimize loop area if connections have to be made both to the target and to the probe.

In conclusion, there are existing solutions for the parasitic capacitance caused by the long cables, while there is not much research effort have been placed for the issue of large loops. This thesis attempts to place effort on

the investigation of such issue, in section 2.2, several possible solutions will be presented and analyzed.

2.2 Possible Solutions

As mentioned in the above section, the main cause of the external interference is the loop area created by the cable. In order to minimize such interference, effort should be made either to break the loop, or to keep the loop but make the effective loop area small. Both direction could provide possible solutions to such issue.

2.2.1 To Break the Loop

Investigation starts with the direction "to break the loop", which can be achieved by the several concepts.

Using Grounded Capacitive Sensors

A very straight forward way would be eliminate one connection cable to the target, which can be done by grounding the target electrode. Actually, there are applications where grounded capacitive sensors are being used [12] [15]. But such applications are based on the assumption or fact that the "ground" they are using are "clean ground", meaning that the ground potential of the sensor electrode is the same value as the ground potential of the electronic interface. Under such circumstances, there will be no "ground current" flowing to the sensor and introducing noise.

But this is not always the case in industrial applications, especially for sensors mounted inside complex machines, where the "machine ground" is likely to have different potential than the "clean ground". More importantly, since there are a lot of different electric components in the machine, the ground potential of the "machine ground" is likely to be changing over time, meaning that the "machine ground" is coupling to the "clean ground"

via a voltage source, whose value and frequency are unpredictable. As shown in Fig 2.1, connecting the target electrode to the machine ground is not beneficial since it will introduce "ground noise" (V_n), and more importantly, the loop still exists, but in a undefined pattern. Therefore, in these applications, ground the target electrode will not break the loop.

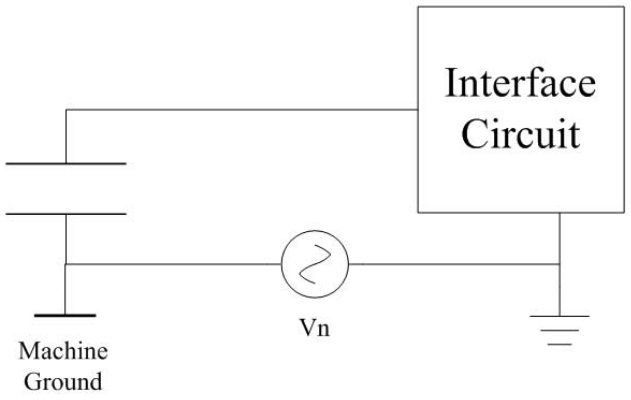

Figure 2.1: One electrode of the sensor connected to the machine ground, which will induce noise due to different ground potential

Using Optical Connections

Another way to break the loop is to focus on the alternatives of cables, one way to break the loop is to use optical connections somewhere in the loop, which will break the loop of current flow. The optical connection can be implemented by, for example, fiber optics, but the price to pay is the extra building block, which is to convert the electrical signal to optical signal and vise versa, as demonstrated in Fig 2.2.

Since in most cases such conversions are not 100 percent efficient, introducing such conversions between electrical and optical domain will not be beneficial regarding to system efficiency, let alone reliability and complexity issue. For these reasons, using optical connections is not a good idea regarding to such issue.

What if designing the entire measurement system in optical domain? It seems not a bad idea. Actually, in the application of positioning, one good alternative solution other than using capacitive sensor is to do the measurements in optical domain, i.e, using interferometers [16]. But to realize such principle, more complex system is needed compare with the principle of capacitive sensor. And the discussion of such principle is out of the scope of this thesis, therefore, we limit ourselves to the principle of capacitive sensor.

2.2.2 Make the Area Small

When there's a road block placed in the way where we are heading to, we have two options to deal with the situation. We either remove the road block and continue (direct way), or we find a way that the road block will not affect the situation we are facing (indirect way).

This is a similar situation to the problems caused by the big loop, where we could either "break the loop" (directly solve the problem), or live with the loop, but with an area that small enough (indirect way to avoid the problem).

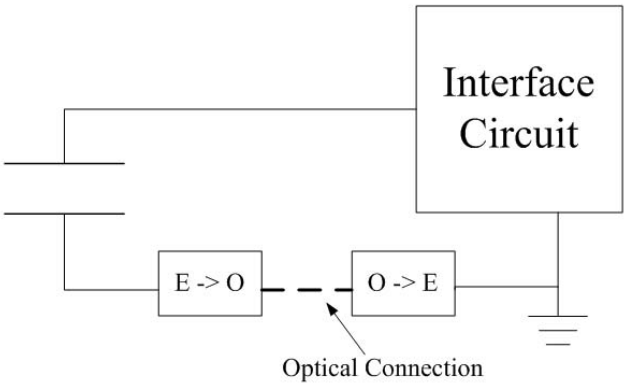

Figure 2.2: Using optical connection to break the current loop

Shielded and Twisted Cable

One common way to deal with electromagnetic interference would be using shielded and twisted cables for connection. It is true that this will greatly reduced the effect of electromagnetic interference since when twisted cable is used, the effective loop area reduced to a neglected level, as shown in Fig 2.3, but, this is not always possible for industrial application. Considering the fact that most industrial application where contactless measurement is used, the cable connecting the sensing element usually goes in a different route from the cabling connecting to the target, twisting the two cables is not feasible regarding to such situation.

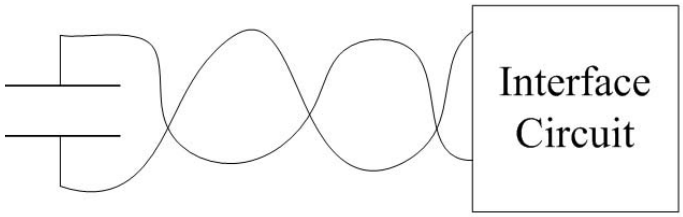

Figure 2.3: Minimizing effective loop area by means of twisting the cable

Wireless Sensing

Using the principle of wireless sensing would be one direct way to handle to issue of minimizing the loop area. To realize such principle, the interface circuit should be mounted in the sensing element and communicate with the data processing system using wireless communications. In principle such approach would not have the problem of external interference, but there are two issues to be considered.

First issue would be the distance between the sensor node (interface circuit) and the receiver, although long cable is not being used, still the distance between the sensor node and the receiver has not been changed, meaning that there is quite a long distance between the two. To conduct effective communication between the two, a large amount of power is expected to be consumed, which is acceptable for the receiver, but problems may occur to the sensor node. Driving a lot of power in the sensor node is always not a good idea, since it may cause self-heating effect thus increase the chance of misalignment.

The power management of the sensor node would be the other issue, compare to the principle where long cables are used, the sensing element used in the principle of wireless sensing is power consuming, which brings the issue of power management. As discussed above, the sensor node need certain amount of power to achieve effective communications to the receiver, therefore, how to provide such constant power supply will be an issue. Of course battery can be used, but that leads to the life time issue, etc.

In a nutshell, such principle can served as one possible way to solve the problem of big loop, but a lot of issues have to be considered. Regarding the the target application in this thesis, it's not a good idea since such principle is trying solve one problem with the cost of bringing more problems. It is a good idea to make further investigation effort on replacing the connection cables with high speed wireless communications, but regarding to the scope of this thesis, it is not the best option in this moment.

2.3 Proposed Concept for Solution

The above mentioned section described several possible ways to solve or to prevent the problem caused by the big loop area of the connection cable. Unfortunately they all have their own constrains and limitations regarding to the requirements of target application.

Amount such principles, using shielded and twisted cables (section 2.2.2) would be the best option with respect to complexity and economic consideration, and such principle has been widely proven in industry. Therefore, when we are looking for the concept for solving such problem, it will be nice to start from this principle.

2.3.1 Measurement with Floating Target Electrode

As discussed in section 2.2.2, what was preventing the use of shielded and twisted cable is the fact that the two cable connected to the interface are going with different route from the sensor. If there's solution for such issue, we can make use of the principle.

Actually, there is something that can be done to make the two wires in the same side, which is similar to [17]. In such structure, two sensing electrode are used to make one measurement, and the two wires connected to the electrodes can be twisted. But the question then becomes, where should the target be connected to? One answer would be to ground the

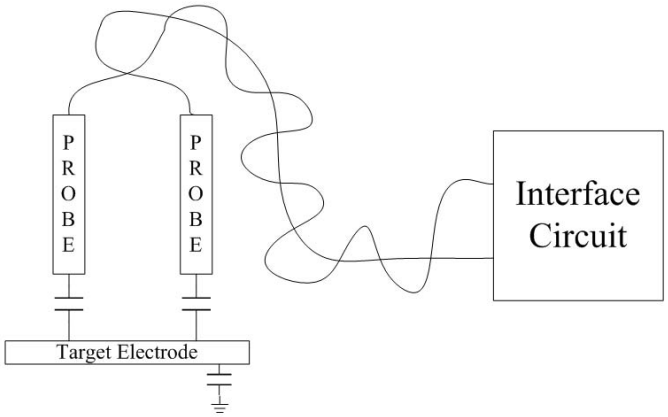

Figure 2.4: Measurement with floating target electrode

target, again, as discussed in section 2.2.1, the target electrode will likely to connected to "machine ground", which may directly introduce unpredictable

noise current.

Another way is to leave the target electrode floating. In such case, the target electrode, although not directly grounded, have a capacitance to ground (capacitive coupling), as demonstrated in Fig 2.4. Therefore, the sensing current will flow through the sensing capacitance (probe/target capacitance) and then through the target/ground capacitance (parasitic), which introduce measurement error.

To eliminate such error, a two-channel, out-of-phase measurement principle is introduced based on the proposed structure, which will be discussed in section 2.3.2.

2.3.2 Two-Channel Out-of-Phase Measurement Principle

If making measurements with the two channel configuration mentioned in Fig 2.4, where two probe channels are synchronized 180 degree out of phase, then in this configuration, the current path is out from one probe, and in to the other. Fig 2.5 shows the direction of the current flow, by such configuration, the loop of sensing current is constructed, then floating target (or grounding) is no longer an issue.

If the parasitic (target/ground) capacitance is changing in time, the variance of the induced current will result in time-variant noise at the output. Whenever the current changes, a small DC shift will occur in the output. Continuous changes in the capacitance will create a corresponding continuous change in the output which will appear as noise. Fortunately, the loop of noise current is different from the loop of sensing current (shown in Fig 2.6), and more importantly, such noise current I_n is split into two parts by the two channels, and appears as a common mode input signal for the interface circuit, while the current I_s in the measurement loop appears as differential signal. By using an interface circuit with a high input CMRR (common mode rejection ratio), the noise signal can be significantly suppressed.

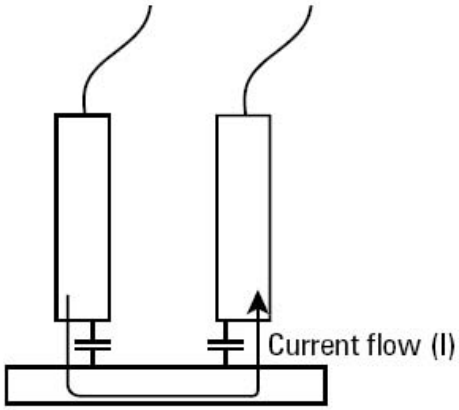

Figure 2.5: Two-channel measurements can build the current loop by providing a return path for the sensing current

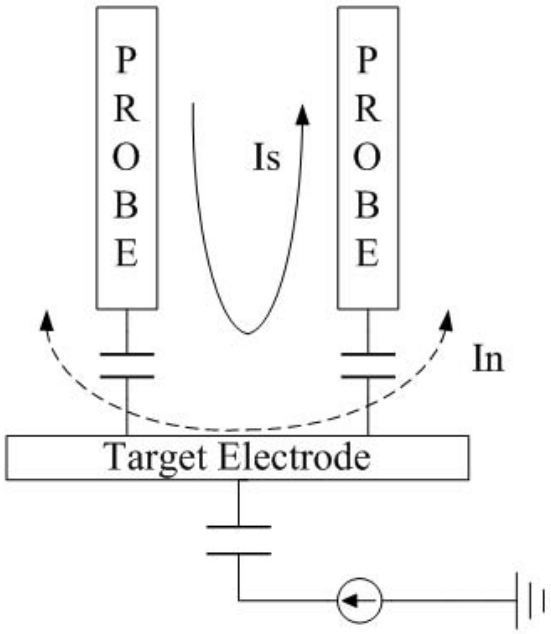

Figure 2.6: There are two current loops presented in such structure – the measurement loop and the noise loop

Further improvement can be done in such a way that the distance between the target and the machine ground is significantly larger than the distance between the target and the sensing electrodes, meaning that the parasitic (target/ground) capacitance is significantly small than the sensing (probe/target) capacitance, which will further reduce magnitude of the noise current, hence reduce measurement error.

2.3.3 Pro's and Con's

Section 2.3 has proposed a concept for dealing with the issue of external interference caused by the large loop. In principle, such configuration makes two loop, the measurement loop and the noise coupling loop. By twisting the two cable, the loop area of the measurement loop is small enough with respect to antenna effect, while the current of the noise loop is small due to the relatively large distance between the target and machine body and will appear as common mode input therefore can be suppressed. Therefore, in principle such concept of measurement is good enough to deal with the issue of external interference.

Every coin has two sides, there are "side effects" of such configuration. First, since two-channel measurement is being used, which makes at least four times sensitivity loss compare to single channel measurement using the same size of mounting. Second, such measurement principle requires the two channel to be 180 degree out of phase, which increases the design effort and requirement for the interface circuit. Finally, in order to achieve good accuracy, the issue of good separation of the two channel should be taken into account.

2.4 Conclusion

In this chapter, the problem we are facing has been clearly defined and analyzed. By understanding the essence and fundamental issue of the problem ,

A scientific and well reasoned approach to find proper measurement concept is shown. By studying different existing measurement concept, the advantage and disadvantage are analyzed, and the reason is given why it is not suitable for the target application. In section 2.3, the concept of two-channel, out-of-phase measurement with floating target is proposed, following by the detail feasibility analysis of such concept. Finally, the requirements for the interface electronics is also given.

However, in order to fully understand the performance of such concept and the related issue for the interface circuit, behavior level analysis must be done and building blocks of interface circuit can be found with well-defined specifications. This will be discussed in detail in Chapter 3.

Chapter 3

Behavior Level Analysis and Design

Behavior level analysis is always the first step toward a successful circuit design, since the results from such analysis provide a translation from requirements (usually stated in "general language" and not clear for engineers) to specifications, which is more engineering oriented language and can be precisely described. On the other hand, from a top-down design perspective, building blocks are used in behavior level analysis and design, which enables designers to be more concentrated on the performance of each block and the influence between different blocks without placing much of the effort on realization. This is extremely helpful in the stage of making specifications. And more importantly such analysis can give guidance to the circuit design.

This chapter discusses both the general issue and the insight during the phase of behavior level design. As a starting point, section 3.1 introduce the basic methodology used to conduct such analysis. It is followed by a detail discussion on the specifications for the interface circuit, which is coming from the performance of the sensor (section 3.2). When the specifications are fixed, the architecture level design of the interface is proposed in section 3.3, including the building blocks and functional analysis. According to such analysis, the design issue for the circuit realization is given in section 3.4

3.1 Methodology

Before the analysis and design in behavior level, it is necessary to introduce the design methodology being used through out the design. Similar discussion can be found in [18].

Do No Harm This is the very first thing should be kept in mind, since what is being designed is the interface circuit to "read-out" the signals (capacitance in this case) from the capacitive sensor that is built according to the principle mentioned in section 2.3. Therefore, it must be clearly aware that the interface circuit should not do any harm to the performance, meaning that the sensor should be the bottle neck of the performance, not the interface. For example,in order not to further lose the dynamic range, the noise floor of the interface should be lower in level than that of the sensor, which caused by the mechanical limitation.

Prevent Problem Although engineering is all about solving problem, sometimes it is more important to prevent problem, at least try to, rather than solving the problem when it occurs. In order to do so, a lot of thinking and analysis has to be done before the actual start of the design, in order to predict, and afterwards try to prevent possible problems. If problems seem to be unavoidable, then it would be nice to think of the reaction well in advance, which will ensure such issue will not jeopardizes the performance. For example, if long connection cable has to be used, there will be the issue of cable capacitance, proper technique should be included in the design in order to prevent the loss the performance due to such issue.

Be Systematic This is more or less the same in nature when we are talking about "team work" in groups, companies, etc. Sometimes the good

performance of the system does not necessarily require a good performance from all components in the system. Since the interaction between different components in the system can provide extra benefit to the system performance. In many cases, one component can be use to compensate the disadvantage of the other component, or the two components can be configured to such a way that the disadvantages in each of them cancels one another and therefore cannot be seen in groups. Make use of the advantage of one component can sometimes relax the design requirement of the other, making life more easy without sacrificing the overall performance.

3.2 Specifications

Keeping the design methodology in mind, the first step in a "top-down" design approach is to fix the specifications. Since the specifications of the interface electronics comes from the performance of the sensor, as well as the higher level system specifications, we have to know what the sensor is doing and the requirements from higher level system specifications.

Since this capacitive sensor interface, as well as the capacitive sensor, are going to serve as part of the control system. Since it's a close loop control system and certain amount of delay will be allocated to each block to ensure loop stability. Therefore, one specification coming from the higher level would be the conversion time, which would be below 100 μs in this case. And the measurement range is up to 10 pF, with a bandwidth of 10 kHz maximum. Another requirement coming from higher level system specification would be the tolerance of 10 meter connection cable and possible electromagnetic interference, the details of such issue has been discussed in chapter two and the proposed measurement concept is capable to handle the issue of electromagnetic interference. On the other hand, certain technique (active shielding) will be implemented in order to prevent possible problem

caused by the use of lang cable, details will be presented in chapter four.

What to be left before fixing the specifications is the performance of the capacitive sensor proposed in chapter two. Since the limited time and resource of this project, building the actual model of such sensor is not feasible and not completely necessary for validating the concept. Therefore, 2D FEM (finite element method) simulation result is used instead, as discussed in section 3.2.1. The finite element method (FEM) (sometimes referred to as finite element analysis) is a numerical technique for finding approximate solutions of partial differential equations (PDE) as well as of integral equations. The solution approach is based either on eliminating the differential equation completely (steady state problems), or rendering the PDE into an approximating system of ordinary differential equations, which are then numerically integrated using standard techniques. FEM is widely used in industrial applications since it allows entire designs to be constructed, refined, and optimized before the design is manufactured. More specificity, literature [19] has proofed that using FEM simulation is a feasible approach when designing capacitive sensors, therefore, using 2D-FEM simulation result to represent the performance of capacitive sensor is acceptable. The purpose for performing such modeling and simulation process, is to find out the inferences in mechanical issue to the capacitance value. This is a very complex process and it is not the main focus on this thesis, therefore, simulations done in these thesis only focus on the effect of tilting in electrodes.

3.2.1 FEM simulation result of the Sensor

A simple model has been built for conducting the FEM simulation, in order to have a rough idea about the specification, as can be seen as Fig 3.1. The dimensions are also included in the plot, which will make the two capacitances approximately 10 pF and a good isolation between the two. In such model, it is assumed the bottom electrode (target electrode) has a significantly larger area than the two sensing electrode, meaning that the effective

Mode	C_{x1}	C_{x2}
Without Tilt	9.6015 pF	9.6014 pF
With Tilt	9.5983 pF	9.6044 pF
Difference	0.0032 pF	0.0030 pF

Table 3.1: Simulated Capacitance Value, with and without electrode tilting

overlapping area of the two electrodes are the area of the sensing electrode. The part in red color is made of non-conducting material and the parts in blue are the electrodes. The non-conducting material serves as the holding of the two electrodes, which will ensure they are in the same level and have an acceptable isolation.

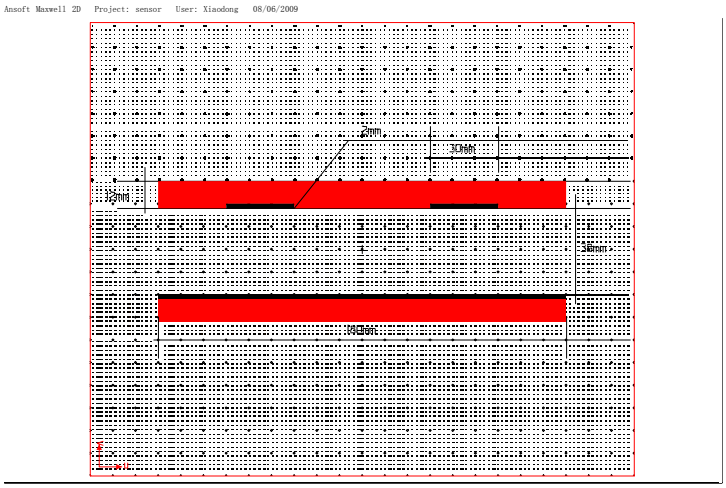

Figure 3.1: Simple FEM simulation model of the capacitive sensor

If the tolerance of tilting is 0.05 degree, then from the FEM simulation result given by the software Maxwell 2D, the simulated capacitance value of the two capacitance with and without the tilting of electrode can be found in table 3.1

The from such simulation result, the resolution of the sensor can be found.

Range	Bandwidth	Resolution
10 pF	up to 10 kHz	11.6 Bits

Table 3.2: Specifications of the sensor, using the principle proposed in chapter two

Range	Bandwidth	Resolution	Conversion Time	Other
10 pF	DC-10 kHz	12 Bits	Less than 100 us	10m Cable

Table 3.3: Specifications of the interface circuit

$$\Delta C_{min} = 0.0032pF \tag{3.1}$$

$$\Delta C_{max} = 10pF \tag{3.2}$$

$$Res = \log_2 \frac{\Delta C_{max}}{\Delta C_{min}} = 11.6bit \tag{3.3}$$

Therefore, the dynamic range of the simulated capacitive sensor is 11.6 bits.

The model and simulation made in this section is serve only as an initial attempt to conduct a complete systematic design approach. As further improvement, more issue should be considered when making such model. For example, the material of the electrodes and the holding, the dimensions of the electrode, and the detail parameter of the proposed capacitive sensor should be considered and included in the model.

3.2.2 Specifications for the Interface Circuit

As a combination of the higher level specifications, and the FEM simulation result, the sensor specification used in this investigation can be found in table 3.2.

The specification of the interface circuit is determined based on such information, as well as the higher level requirements. It can be found in table 3.3.

In conclusion, the interface circuit should achieve a specifications mention above. Due to the special configuration of the sensor, the interface circuit has to be configured in such a way that the signal in the two channels are out-of-phase with each other. This will be discussed in section 3.3.

3.3 Proposed Architecture

The electrical equivalent model of the proposed sensor structure can be seen in Fig 3.2,

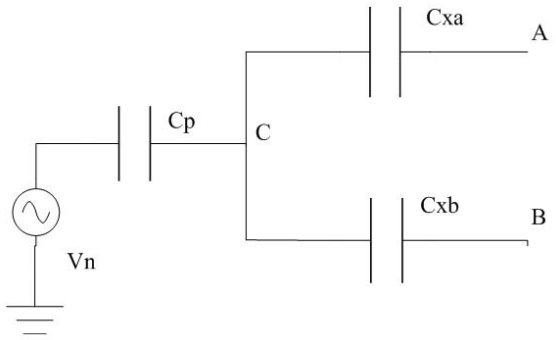

Figure 3.2: Equivalent model of the proposed sensor structure

The interface which implements the two-channel, out-of-phase measurement principle connects the two channel (C_{xa} and C_{xb}) in point A and B demonstrated in the model. If the two channel are matched with each other with different polarity, there potential in node C will be ground and there will be no injected noise caused by the parasitic capacitor C_p and noise V_n from machine ground.

Knowing such fact, the behavior of such model together with in interface can be seen as two grounded capacitive sensors and their interfaces, with ground potential on node C. Therefore, what have to be designed are

two grounded "synchronized" capacitive sensor interfaces, but with sensing current in different polarity.

3.3.1 Interfacing Grounded Capacitive Sensor

Capacitive sensors can be measured in several ways. In the book [9], a number of interfacing principle have been proposed with respect to different configurations of capacitive sensors. But for grounded capacitive sensor, since only one terminal can be accessed, not all the principle listed in [9] can be used, some very widely-used principle such as AC bridge cannot be used in grounded capacitive sensors. In general there are three major types of interfacing principle for such type of sensors.

DC Measurement Based

The simplest way of interfacing grounded capacitive sensor is the DC measurement method. With a operational amplifier with very high input impendence, the change of capacitance can be measured by the respective change of DC voltage.

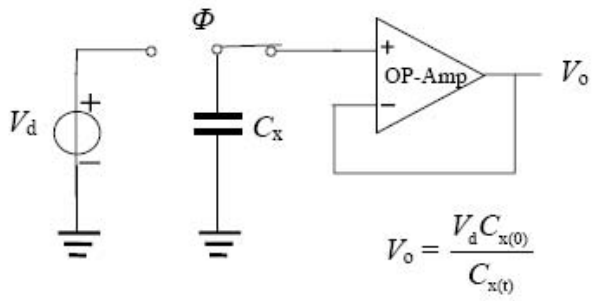

Figure 3.3: DC measurement based interface principle

Fig 3.3 shows the simple configuration of such interface. The sensing capacitor C_x is first charged by a voltage reference V_d, resulting in a constant

charge in the capacitor. Then the sensing capacitor is connected to the amplifier input, assuming ideal situation, the output voltage of the amplifier with change accordingly.

DC measurement based interface is susceptible to many disturbances, such as parasitic capacitance at the input node, slow variation of component parameters and finite DC gain of the op-amp. Errors will also be introduced if the switching time between to the phase is long enough to cause leakage of charge.

Oscillation Based

The second method is based on oscillation, it can be RC oscillation or LC oscillation, where the sensing capacitor serves as the tuning element and the frequency output signal is controlled by the value of such capacitor. Normally, RC oscillation method is preferred since in LC oscillation method, it is difficult to make accurate inductor. Fig 3.4 demonstrates a grounded capacitive interface based on RC relaxation oscillator, with a oscillation frequency of $\frac{1}{2\ln(2)RC_x}$

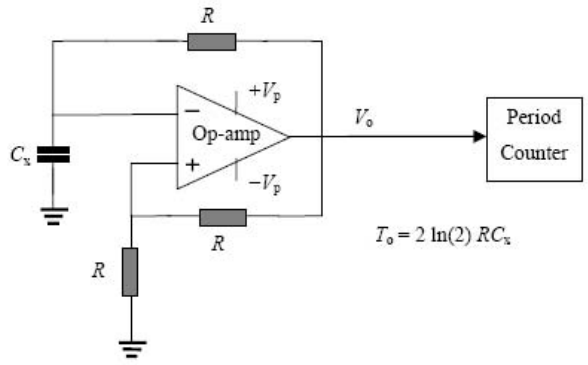

Figure 3.4: Simple relaxation oscillator to interface grounded capacitive sensor

Charge Transfer Based

One other possible solution is based on charge-transfer method, which is the improvement of the DC measurement method. Fig 3.5 describes a simple configuration of a Charge-transfer based method to interface grounded capacitive sensor. The operation of this interface consists of charging the sensing capacitance C_x using voltage V_c via switch S_1 then discharging it into a current integration amplifier to transfer the amount of charge to the output via a second switch S_2.

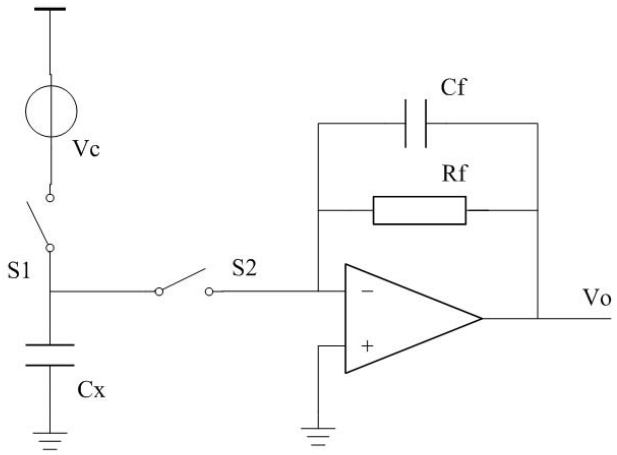

Figure 3.5: Charge-transfer based method to interface grounded capacitive sensor

The charge transferred from C_x to the output in a single charging/discharging cycle is

$$Q = V_c C_x \tag{3.4}$$

The charging and discharging operation is repeated at a clock frequency f. The discharging current pulse is intergraded in the current integration amplifier to give an current flow I_s, where:

$$I_s = V_c C_x f \tag{3.5}$$

And finally the output voltage V_o equals to

$$V_o = R_f V_c C_x f \tag{3.6}$$

where R_f is the feedback resistance.

3.3.2 Proposed Interface

With the knowledge of the possible ways to measure grounded capacitive sensors, the interface circuit for the sensor model can be designed. However, the special configuration of the sensor do give some limitation to the choice of architectures for the interface. Since the concept of the sensor requires the sensing current in the two channel to be different in polarity, therefore, interfacing principle that convert the capacitance into frequency seems not an option for this type of sensor since there's no way to built negative frequency, meaning that there's no way to make the sensing current in the two channel in reverse polarity.

However the principle of charge transfer seems to be a good option, since it works in a two phase approach. The sensing currents in the two channel can be easily configured into reverse polarity by using excitation signal in reverse polarity, which will convert the common mode capacitance (C_{xa} and C_{xb} changes in the same direction with the same amount) into differential charge (or current) and will bring huge beneficial to the interface.

The basic configuration of the front end can be seen in Fig 3.6, where the two sensing capacitors are first charged by two excitation signal $+V_c$ and $-V_c$, in ideal situation, the charged generated in node A and node B equals to

$$Q_a = V_c C_{xa} \tag{3.7}$$

$$Q_b = -V_c C_{xb} \tag{3.8}$$

If the two channels are matched , i.e

$$C_{xa} = C_{xb}, \tag{3.9}$$

then

$$Q_a = -Q_b, \tag{3.10}$$

meaning that differential charge is generated in the input node of the op-amp.

And then it switches to phase two, where the generated charge is transferred to the output via the feedback capacitors:

$$V_{outp} = R_f V_c C_{xa} f \tag{3.11}$$

$$V_{outn} = -R_f V_c C_{xb} f \tag{3.12}$$

Therefore, using charge transfer method, the interface for such sensor configuration can be designed. The details of the circuit design will be discussed in Chapter four. Before going into the detailed circuit design, it is necessary to first design the interface in behavior level to achieve better performance.

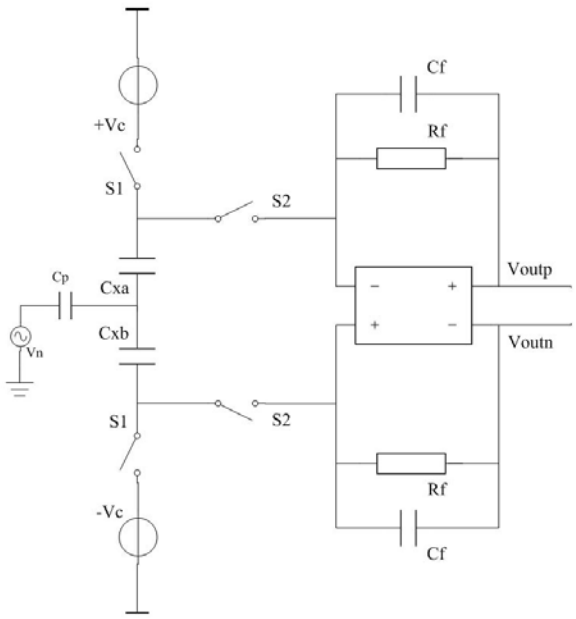

Figure 3.6: Modified charge transfer method for interfacing the proposed sensor

3.3.3 Building Blocks

The front-end is not the complete story of designing the interface, since the interface should be designed to have digital output and more importantly, it will be beneficial if the analog part and the digital part can somehow compensate each other in performance. Therefore, a complete block diagram of the interface is proposed, with respect to the specifications. As seen Fig, it can be seen that the proposed interface is based around a 12-bit ADC, which is interfaced to the controlling micro-controller or CPLD via simple digital buffer.

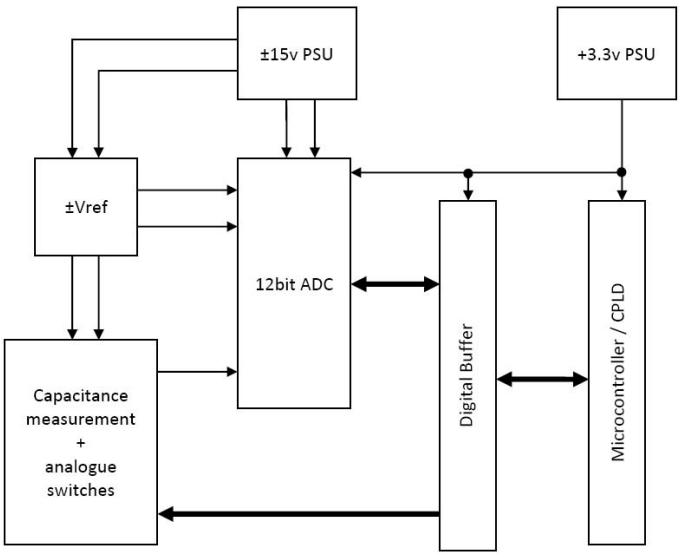

Figure 3.7: Building blocks of the complete interface circuit

Notice that as well as controlling the ADC, the CPLD controls the analogue switch configuration needed for the capacitance measurement operation. Two reference voltages are also generated locally ($\pm V_{ref}$), from the $\pm$15V regulated power supply. Again notice that these two references (also used for the capacitance measurement operation) are measured via the ADC,

in order to improve the overall transfer function measurement accuracy.

3.3.4 Functional Analysis

In section 3.1, the design methodology was discussed. This section presents the functional design considerations of the interface, with the purpose of maximizing performance by properly design the interaction between building blocks.

Knowing the structure of the sensor and the charge-transfer interfacing principle, it can be seen that the sensor needs bipolar excitation voltage to perform one single measurement. Since the sensor works in a relatively low frequency range, the offset and low-frequency noise will have a negative contribution to the performance, which can be improved by, of course, using the best components with respect to such performance. Actually, more can be done by just picking up the best available in the market. Since offset and low-frequency noise change slowly in time, it can be canceled by making one more measurement but with different polarity, then take the difference between the two. Therefore, if the final output (V_{out} in Fig 3.8) is only sensitive to the difference (but not accurate level) between the two sub-measurements ($V_{out,1}$ and $V_{out,2}$),the interface will not any more be sensitive to offset and low frequency noise, as demonstrated in Fig 3.8.

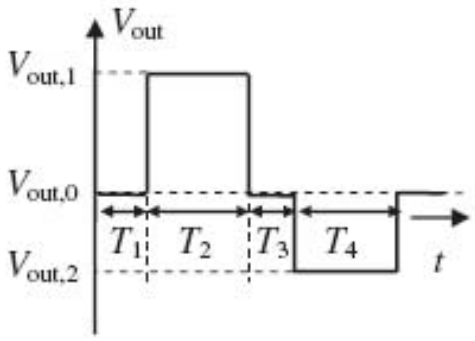

Figure 3.8: output of the interface with the presence of offset

Therefore, the interfacing principle can be slightly modified with respect to this issue. Each measurement now consist of two charge-transfer process. In the first half of the measurement, the two sensing capacitors C_{xa} and C_{xb} are charged by $+V_{ref}$ and $-V_{ref}$, while in the second half of the measurement, the excitation polarity is swopped, meaning that C_{xa} and C_{xb} are now charged by $-V_{ref}$ and $+V_{ref}$. By doing so, the output signal of the two half cycle have reverse polarity and performance with respected to offset and low-frequency noise can be improved by taking the difference.

The question is now become how to achieve such interfacing process, to be exact, how to "remember" the result from the first half and subtract the result from the second half. It can be done in analog domain by using sample and hold structure, but it will be complex and further introduce noise source. Providing that the output signal will be digitized via the ADC, it will be a good idea to make such substraction in digital domain, which is easy with respected to implementation, and more importantly, no extra circuit is needed. As a result, the requirement for offset and low frequency noise in the analog domain is relaxed with the help of proper digital signal processing.

On the other hand, as mentioned in section 3.3.3, two references voltage used for the capacitance measurement operation are also measured via the ADC. This will provide a "ratiometric measurement" with respect to the reference voltage, as discussed below.

Again using the circuit in Fig 3.5 for discussion, the reference voltage is V_c, and the final output voltage is $V_o = R_f V_c C_x f$. Using the "ratiometric measurement" principle, V_c is first measured via the ADC, resulting its digital representation D_c.

$$D_c \doteq V_c \tag{3.13}$$

Then the output voltage V_o is measured, resulting its digital representation

D_o.

$$D_o \doteq V_o = R_f V_c C_x f \tag{3.14}$$

Therefore,

$$\frac{D_o}{D_c} = R_f C_x f \tag{3.15}$$

$$C_x = \frac{D_o}{D_c R_f f} \tag{3.16}$$

And the digital output will not be affected by accuracy of V_c in the transfer function.

3.4 Conclusion

This chapter presents the design and discussion of the interface in behavior level, which serves as a preparation for the actual circuit design. Such discussion helps to gain further knowledge of the insight design issue of the interface. By using the methodology mentioned in section 3.1, the performance of the interface can be optimized without going into the details of each building blocks.

Providing the knowledge of the interface in behavior level, the building blocks of the interface are proposed. The function analysis and optimization process is also presented. And more importantly, during the phase of behavior level design, the principle is becoming more and more complete and the circuit is coming into the surface little by little. With a good understanding of the interface in behavior level, finishing the design in component level will be efficient and more repairable performance can be expected.

The component level design of the interface will be presented in Chapter four, where detail circuit design issue will be presented. And discussion on the component non-perfection will also be included, as well as the implementation issue.

Chapter 4

Circuit Design and Implementation

In chapter three, behavior level design and analysis to the interface has been performed. From such analysis, charge-transfer principle has been has been proposed to build the interface and the optimization process has also been introduced. What is left to be done is the circuit implementation for the building blocks mentioned in section 3.3.3, which is presented in this chapter.

This chapter starts with the discussion of front-end circuit design, since it is the most critical part of the interface. Detail designing issue is presented such as fixing the component specifications and how is effect of component non-perfection. Other than these, the technique of active shielding is also discussed, where detail design considerations will be analyzed.

After that the design process of the other building block will be presented as well as the issue and consideration for implementation. Finally, the chapter ends with a conclusion.

4.1 Proposed Circuit for Capacitance Measurement

With results from the analysis in chapter three, it can be seen that charge-transfer method would be a suitable principle for the front-end circuit. In order to achieve the behavior level performance optimization described in section 3.3.4, bipolar excitation signal is needed. The focus of this section is the detail design issue of the front-end, including calculations and analysis for device non-perfection.

4.1.1 Theory of Operation

Fig 4.1 demonstrates the circuit for the front-end of the capacitive sensor interface, only half circuit is shown for simplicity. It is a charge transfer based design and works in four phase.

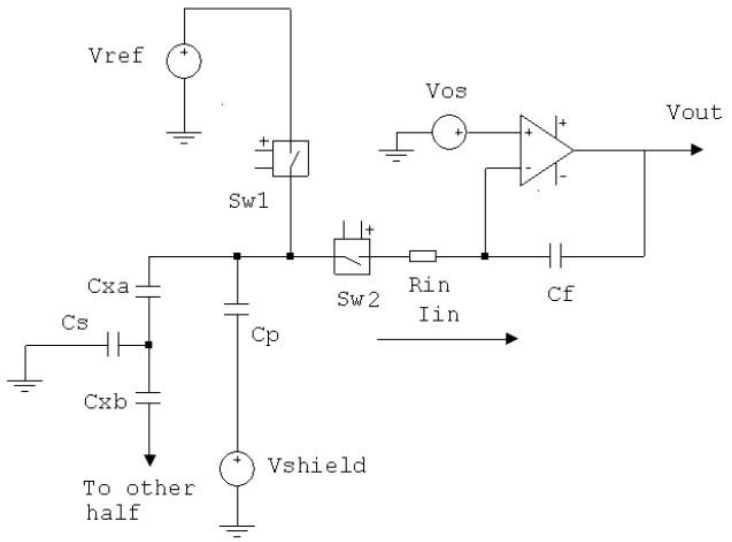

Figure 4.1: Half circuit of the capacitive sensor interface front-end

Basic Action and Tolerances

Analyzing Fig 4.1, it can be seen that the sensing capacitor is C_x , which illustrated by C_{xa} in Fig 4.1, and C_{xb} is for the identical second circuit and can therefore be ignored for this analysis. During the first quarter of a cycle, sw_1 is closed and C_x is charged to V_{ref}. During the second quarter of the cycle, sw_1 is opened and sw_2 closed and hence C_x is discharged into the integrator circuit consisting of R_{in} and C_f connected around an op-amp as shown Fig 4.1. The third and the fourth cycle are the same as previous two, with the only difference on changing the polarity of V_{ref}.

During the charging cycle, the integrator feedback capacitor C_f is discharged by a switch across it (which is not shown in Fig 4.1), so that the voltage across C_f starts at zero. Assuming that the op-amp is perfect, V_{os} can be neglected and $V-$ (i.e. the op-amps negative input) is maintained as a virtual earth by the feedback through C_f; then C_x will discharge toward ground through R_{in}, and C_f will charge so as to maintain $V-$ at ground potential.

During this charge transfer process, Charge balance implies:

$$C_x V_{ref} = -V_{out} C_f \tag{4.1}$$

or

$$V_{out} = -\frac{C_x}{C_f} V_{ref} \tag{4.2}$$

The current into the op-amp would be (from the formula for the discharge of a capacitor):

$$I_{in} = \frac{V_{ref}}{R_{in}} e^{\frac{-t}{C_x R_{in}}} \tag{4.3}$$

The output voltage slew rate follows as:

$$\begin{aligned} \frac{d(V_{out})}{dt} &= \frac{I_{in}}{C_f} \\ &= \frac{V_{ref}}{R_{in} C_f} e^{\frac{-t}{C_x R_{in}}} \end{aligned} \tag{4.4}$$

Therefore, assuming the initial voltage on the feedback capacitor is zero, the transfer function of the front-end can be seen as

$$V_{out} = \frac{C_x}{C_f} V_{ref} e^{\frac{-t}{C_x R_{in}}} \tag{4.5}$$

This is the ideal situation. However, if the op-amp is unable to meet the demands of the initial slew, the effect would be for $V-$ to move slightly more positive than ground, but as the transient proceeded, feedback would restore the virtual earth. Providing that the op-amp input impedance is large, all current must still pass through C_f, and hence the charge balance relationship would still hold.

The effect of V_{os} is to produce a measurement error. This can be reasoned by applying supposition to the input. Assume that the capacitor has zero voltage initially. Feedback would hold $V-$ at V_{os}, which would then attempt to charge C_x, by passing current through C_f.

This argument produces an initial error rate of:

$$\frac{d(V_{out})}{dt} = \frac{V_{os}}{C_f R_{in}} \tag{4.6}$$

This error would decay to zero as the voltage on C_x approaches V_{os} and current into C_x approaches zero.

From such analysis, we can see that there are several important parameters to consider:

1. Op-amp slew rate must be comparable with $\frac{V_{ref}}{R_{in}}$ in order to ensure no great deviations from virtual earth, i.e. charging of C_f keeps up with discharge of C_x in order to maintain $V-$ at zero volts.

2. Switch charge injection when sw_2 closes is small when compared with $C_x V_{os}$

3. Time constant $C_x R_{in}$ is sufficiently small such that C_x has sufficient time to discharge close to zero during the cycle time when sw_2 is closed, in order to ensure that adequate accuracy is obtained.

4. Any error due to V_{os} (or any other cause) is small during the time of measurement.

The Complete Circuit

Two halves of the circuit shown in Fig 4.1 are required, as the sensing capacitance is split into two identical halves C_{xa} and C_{xb}. The measurement cycle consists of two sub cycles, the first with C_{xa} charged to V_{ref}, and C_{xb} to $-V_{ref}$, the second with C_{xa} charged to $-V_{ref}$ and C_{xb} to V_{ref}. By using the such configuration, the current through stray capacitance C_s (parasitic capacitance between the floating electrode to ground) is held near zero. Also the two measurement sub cycles, with polarities reversed, help combat the error due to V_{os} and possible other factors.

The complete circuit diagram can be seen in Fig 4.2,which consist an instrumentation amplifier as a gain stage to provide enough signal swing for the ADC, whose input range is ±5V

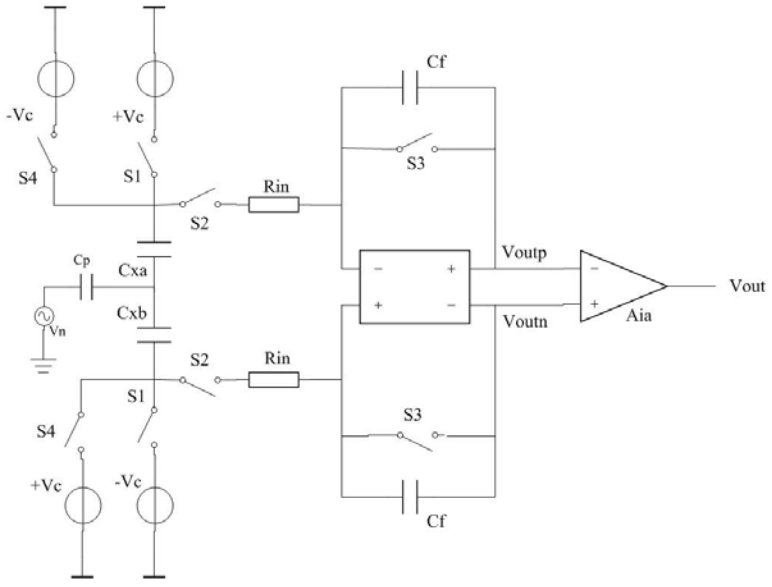

Figure 4.2: Complete analog front-end circuit of the interface

4.1.2 Detailed Design and Component Selection

Having the insight knowledge of the operation, the next step would be to choose the right components to meet the specifications and achieve the performance. Some hints for the components are already included in section 4.1.1, and here more detail would be included in discussed. Since the most important components are those in the analog part, discussions will be focusing on such components. Issue with R_{in}, C_f and the op-amp will be first discussed, then the focus will be turned to the issue for selecting the switches. Finally the discussion with other surrounding components will be presented.

Selection of R_{in}, C_f and the Op-amps

The first issue to discuss is the performance with respect to noise, which is directly related to the dynamic range of the interface. Keeping in mind the specifications of the sensor, and the design methodology (the sensor should be the limit, not the interface), it has to be assured that the dynamic range (DR) of the interface is better than that of the sensor.

Fig 4.3 is used to analysis the noise performance of the interface, where critical noise sources are demonstrated.

From the specification of the sensor:

$$C_{x,max} = 10\text{pF} \tag{4.7}$$

$$C_{x,min} = \frac{C_{x,max}}{2^{12}} = 0.002\text{pF} \tag{4.8}$$

Then the maximum and minimum value of the output voltage can be found:

$$V_{out,max} = \frac{C_{x,max}}{C_f} V_c \tag{4.9}$$

$$V_{out,min} = \frac{C_{x,min}}{C_f} V_c \tag{4.10}$$

And from the bandwidth requirement of $BW = 10kHz$, if only consider in-band noise power, the noise bandwidth can be found:

$$f_n = \frac{\pi}{2} BW = 15.7kHz \tag{4.11}$$

to leave some margin, it is set to 20 kHz.

According the Fig 4.3 the total noise power at the output can be calculated:

$$V_{n,out}^2 = (1 + \frac{C_x}{C_f})^2 V_{n,opamp}^2 f_n + \frac{KT}{C_x} + (4k_B T R_{in})(\frac{C_f}{C_x})^2 f_n \tag{4.12}$$

while the signal power equals to

$$V_{s,out}^2 = \frac{C_x}{C_f} V_s \tag{4.13}$$

Since the dynamic range is defined as the signal to noise ratio when the signal is at full scale, and V_c is 5V in this case, the dynamic range of the interface can be found:

$$DR = \frac{V_{s,out,max}^2}{V_{n,out,max}^2} > 80dB \tag{4.14}$$

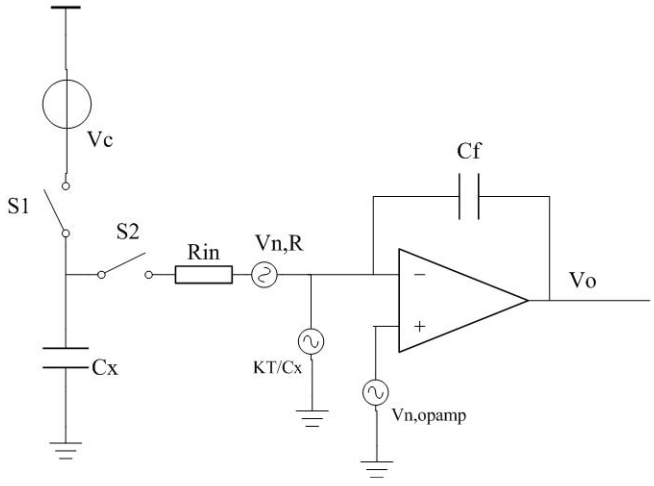

Figure 4.3: Noise analysis of the front end

and on the other hand, $V_{out,min}$ should be above the noise floor. These give the first requirement for selecting the right component. Amount such parameters the most important ones to fix are C_f and R_{in}

Another important issue is related to the input bias current of the op-amp. In ideal situation, there would be no current flowing into the op-amp, however, the input bias current do exists and it will cause measurement error. In order to achieve the require accuracy, and with some margin, the input bias current should satisfy:

$$I_{bias} < \frac{V_c}{R_{in}} \frac{1}{2^{13}} \tag{4.15}$$

with this condition, the leakage current to the op-amp will not cause out-of-spec errors.

Seen from the equation above, it seems that the smaller R_{in} is, the more relaxed for the requirements for I_{bias}. What's more, if R_{in} is small, the time constant $\tau = C_x R_{in}$ will be small and the discharging time of C_x is sufficient in the transfer phase, which can ensure the required accuracy. If full settling of 14-bit accuracy (an error ratio) is required, then,

$$V(t) = V_c e^{\frac{-t}{\tau}} \tag{4.16}$$

$$\frac{V(t)}{V_c} < 2^{-14} \tag{4.17}$$

$$\frac{-t}{\tau} < \ln(2^{-14}) \tag{4.18}$$

resulting in a need of 12τ fore such settling, therefore, small R_{in} will help with such process.

But there are another limitation for R_{in}, which is related to the slew rate of the op-amp, as mentioned in section 4.1. If R_{in} is becoming smaller, then the requirement for the slew rate will become higher. Therefore, the value of R_{in} should be optimized to obtain best performance amount the available components.

The value of C_f also has an influence on the settling issue, since in the charging phase, the switch across C_f is ON and C_f is discharged through the on resistance R_{on} of the switch . If the time constant $\tau = C_f R_{on}$ is not small enough to have a full settling, there would be errors in measurement. Or using the other way to interpret, this gives the limitation for the maximin working frequency of the interface.

One other issue regarding to C_f is the signal swing, it can be seen that the signal swing is decreasing with increasing value of C_f. It is true that the gain stage afterwards will amplify the signal to meet the range of ADC, but from noise point of view, a high gain in the second stage is not suggested. Since looking at the final output, the equivalent noise source at the output of the first stage will be amplified by the gain of the second stage.

Other than these, there are a few other requirements for the op-amp. Since the interface is aimed at a 12-bit resolution and to leave some safe margin, the DC gain of the op-amp should be higher than $6 \times 14 = 84$dB in order to have a settling with enough accuracy. And since one task of the op-amp, and the instrumentation amplifier is to reduce the influence of noise due to the capacitive coupling from the floating target, they should be able to provide enough CMRR in the working frequency. At this stage, a CMRR of 75 dB at working frequency is suggested.

The above mentioned constrains give the space for optimizing the value of R_{in} and C_f, with the target of achieving the specifications using the most relaxed requirements of the op-amp.

Selection of Analog Switches

Other than general parameter such as bandwidth, signal swing etc, charge injection and on resistance are the key parameters to look at when selecting analog switch, since these two parameters have a strong interaction with other circuit components and therefore should be well analyzed.

Charge injection usually occurs when the switch is about to turn OFF [20], and for switch implemented using CMOS (although discreet components are used in this case, the relation between charge injection and on resistance is still hold), the injected charge is equal to [21]:

$$Q_{inj} = \frac{L^2}{\mu R_{on}} \tag{4.19}$$

meaning that the cost of reducing charge injection is to have a switch with large on resistance, which will increase the time for settling to a certain accuracy when charging of discharging the capacitors, resulting in a decrease of the maximum operational frequency.

But fortunately, the issue of charge injection is not critical in some case. If the injected charge from a certain switch is signal independent, then such charge will only bring fixed error like offset and can be cancel out without affecting performance. On the other hand, if the injected charge from a certain switch is signal dependent, then it can not be cancel out and will introduce distortion.

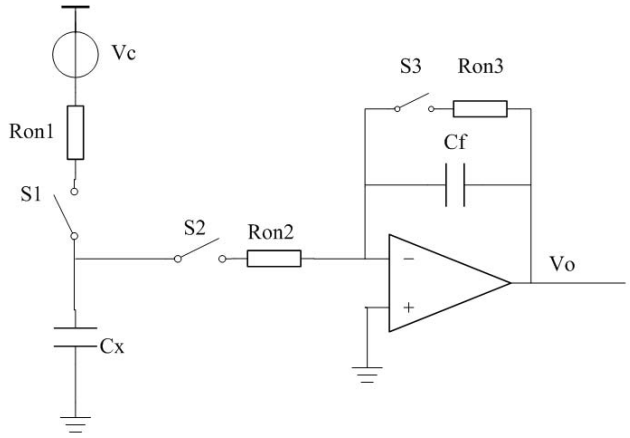

Figure 4.4: Discussion on charge injection and on resistance of the switches

Fig 4.4 is simplified circuit of the analog front end, which is used to analyze the effect of charge injection and on resistance of the switches. The

on resistance of these switches are modeled separately next to the switch and therefore the switches in Fig 4.4 have no on resistance.

When the interface works in charge and reset phase, S1 and S3 is ON while S2 is OFF. In this case, there will be injected charge from S2. But the charge injection of S2 is not important, because the injected charge will split and go to C_x and to C_f, where the sensor C_x in this phase is connected to a well known potential V_c and therefore the charge stored in C_x is fixed ($Q_x = C_x V_c$). On the other hand, the part that will go to C_f is not important since C_f is now in reset phase and the output voltage is not important for measurement.

Therefore, the charge injection of S2 is not important and S2 is not a critical switch, meaning that the switch can be made with relatively low on resistance compare with R_{in} to prevent errors.

However, on the next phase, which is the transfer phase, there are critical switches. On this phase, S1 and S3 is OFF while S2 is ON. There will be charge injection from switch S1 and S3. The injected charge from S3 is not critical, the reason is that the injected charge goes to both sides of C_f and therefore the error induced in the output voltage is always in one direction and similar to that of the offset voltage. This effect can be removed by the measurement principle.

The charge injection of switch S1 needs to have special attention, since the injected charge will directly go into the signal path and cause measurement error. Therefore it is suggested to choose low charge injection switch for S1, to make sure the require accuracy can be achieved. Also the break before make switching principle used in the front end will help reducing such problem.

The analog switches can be found using the result of such analysis. ADG1221/2/3 series is recommended since this device has the virtue of a break before make switching action, and by default has one switch that

is closed and other that is open. This device also has low capacitance and low charge injection and could be placed next the op-amps, simplifying the PCB layout and improving AC performance.

Selection of the Surrounding Components

Other than the key components, the surrounding components has to be carefully selected in order not to jeopardies the overall performance of the interface. A detailed description of such devices/components is now given below:

12bit ADC: In order to minimize measurement errors of the complete capacitance sensor interface, it is recommended to place an ADC on the PCB together with the analogue circuitry. This will ensure that any measurement errors and noise will be minimal on the processed result. Analyzing Fig 3.7, notice that a multichannel ADC has been proposed instead of a single channel ADC. The virtue of such a device allows for the exact measurement of the two reference voltages ($\pm V_{ref}$), and as such relaxed the design requirement for the voltage references. The device AD7323 12-bit + sign, 500kS/sec ADC is recommend for this application, noted that all four analogue inputs can be software configured and the device has the advantage of an internally generated reference voltage. This reference voltage (once activated in software) can be used to generate $\pm V_{ref}$, leading to lower design effort (no extra voltage reference needed). The re-configurable analog input range and 500kS/sec sampling rate will also allow for easy experimentation during the experimentation/evaluation stage.

Digital buffer: 74AC244 from TI would be a suitable choice here by virtue of its small propagation delay and input and output protection diodes.

Voltage references: If a multiplexed ADC were to be used in the design, then two op-amps (such as Nationals quad LM324) and a few resistors

and capacitors could be used to implement $\pm V_{ref}$. Where, the measurement of $\pm V_{ref}$ could be undertaken at power up or even between switching cycles. However, precision components would be required in the absence of a measurement medium.

+3.3V Power Supply: This could be supplied from the digital control board. However, adding a +3.3v regulator such as SGSs KF33 would be not be difficult.

±15V Power Supply: It is recommended that two low power linear voltage regulators be placed on the board for generating the ±15V for the analog front-end and ADC. This also has the advantage of providing over voltage protection and power supply noise reduction. Nationals LM78L15 and LM79L15 are both suitable for this application. However, the output current is limited to 100mA, which should be fine for this application.

As a result of such study and selection process, the key components can be seen in table 4.1. These are only the key components, and a lot of other components such as de-coupling capacitor, protection diodes, and other indicators are not included in table 4.1.

Component	Value (Model)
R_{in}	2.2 kΩ
C_f	100 pF
Integrator Op-Amp	AD8671
Instrumentation Amp	AD8221
Analog Switch	ADG1221/2/3
ADC	AD7323
Digital Buffer	74AC244
References Amplifier	LM324
+3.3v Power	KF33
±15v Power	LM78L15/LM79L15
Digital Control	From FPGA in another board

Table 4.1: List of components in the interface

4.1.3 Effect of Component Non-Perfection

The major non-perfection of the selected components are the op-amp offset, component mismatch, the switch charge injection, ON resistance of the switch and the input capacitance of the op-amp. In this section, the influence of these non-perfection will be discussed, except for the issue of switch charge injection and on resistance, which has already been discussed in section 4.1.2. The influence of cable capacitance will also discussed in this section.

Op-amp Offset

The influence of op-amp offset can be illustrated using Fig 4.5, which is represented by the two voltage source V_{os1} and V_{os2}. Noted that V_{os1} and V_{os2} represents only the absolute value of the offset voltages.

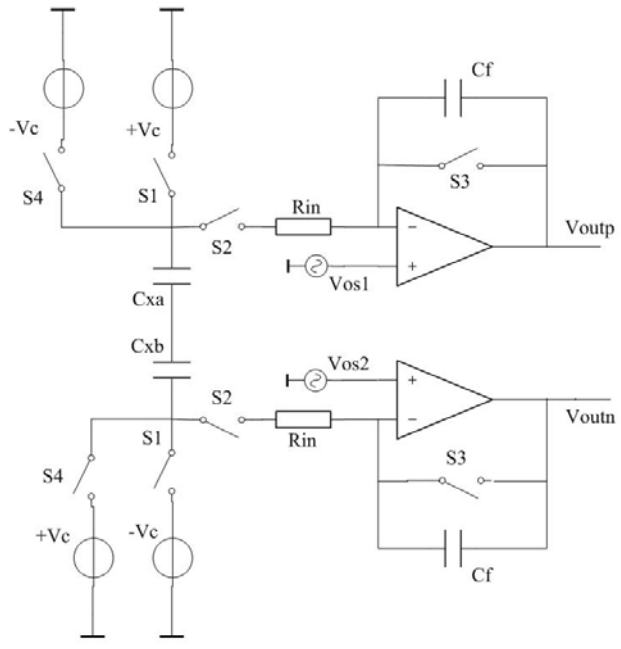

Figure 4.5: The analog front end circuit with the presents of offset in the op-amp

According the principle of operation, the sensors are first charged by the reference voltages in phase one, resulting in:

$$Q_{cxa} = C_{xa} V_c \tag{4.20}$$

$$V_{outp} = V_{os1} \tag{4.21}$$

and

$$Q_{cxb} = -C_{xb} V_c V_{outn} = V_{os2} \tag{4.22}$$

Then in the second phase, the amount of charge is transferred to the output voltage via C_f, but at the same time, there are offset charge due to V_{os1} and V_{os2}:

$$Q_{cxa} = C_{xa} V_c + C_{xa} V_{os1} \tag{4.23}$$

$$Q_{cxb} = -C_{xb} V_c + C_{xb} V_{os2} \tag{4.24}$$

$$V_{outp} = \frac{C_{xa} V_c}{C_f} + V_{os1}(1 + \frac{C_{xa}}{C_f}) \tag{4.25}$$

$$V_{outn} = -\frac{C_{xb} V_c}{C_f} + V_{os2}(1 + \frac{C_{xb}}{C_f}) \tag{4.26}$$

and therefore, consider the worst case

$$V_2 = V_{outp} - V_{outn} = \frac{(C_{xa} + C_{xb})V_c}{C_f} + V_{os1}(1 + \frac{C_{xa}}{C_f}) + V_{os2}(1 + \frac{C_{xb}}{C_f}) \tag{4.27}$$

Similar situation holds in phase three and four, except for swapping the sign of V_c, and the output voltage in phase four can be found as:

$$V_4 = V_{outp} - V_{outn} = -\frac{(C_{xa} + C_{xb})V_c}{C_f} + V_{os1}(1 + \frac{C_{xa}}{C_f}) + V_{os2}(1 + \frac{C_{xb}}{C_f}) \tag{4.28}$$

it seems that the offset voltage of the op-amp will directly introduce measurement error and taking difference of the output in the two channels will not help. However, according the operational principle of the interface, the output voltage V_2 and V_4 will be digitized and the final digital output of each measurement cycle equals to (analog representation is still used for obtain clear demonstration, although this will be done in digital domain):

$$V_{out} = V_2 - V_4 = \frac{2(C_{xa} + C_{xb})V_c}{C_f} \tag{4.29}$$

It can be seen that the offset voltage V_{os1} and V_{os2} is no longer in the expression, meaning that the final digital output does not sensitive to op-amp offset, it only sensitive to the difference(!) between the outputs of phase two and phase four.

Op-amp Input Capacitance

Fig 4.6 can be used to analyze the effect of op-amp input capacitance C_p. Again according to the operational principle, the output in phase two can be shown as:

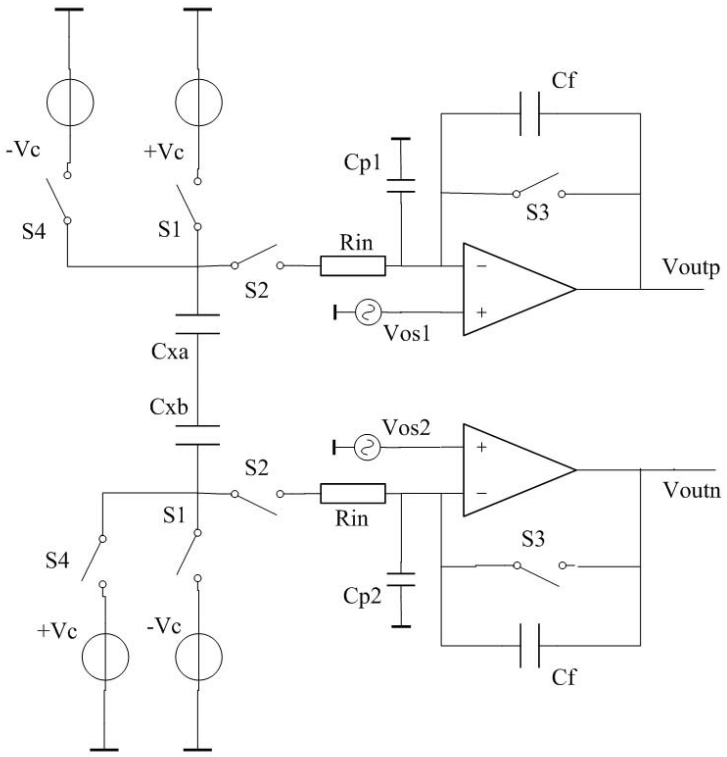

Figure 4.6: The analog front end circuit with the presents of op-amp offset and input capacitance

$$V_{outp} = \frac{C_{xa} V_c}{C_f} + V_{os1}(1 + \frac{C_{xa}}{C_f} + \frac{C_{p1}}{C_f}) \qquad (4.30)$$

$$V_{outn} = -\frac{C_{xb}V_c}{C_f} + V_{os2}(1 + \frac{C_{xb}}{C_f} + \frac{C_{p2}}{C_f}) \quad (4.31)$$

$$V_2 = V_{outp} - V_{outn} = \frac{(C_{xa} + C_{xb})V_c}{C_f} + V_{os1}(1 + \frac{C_{xa} + C_{p1}}{C_f}) + V_{os2}(1 + \frac{C_{xb} + C_{p2}}{C_f}) \quad (4.32)$$

and similarly, the output in phase four can be shown as:

$$V_4 = V_{outp} - V_{outn} = -\frac{(C_{xa} + C_{xb})V_c}{C_f} + V_{os1}(1 + \frac{C_{xa} + C_{p1}}{C_f}) + V_{os2}(1 + \frac{C_{xb} + C_{p2}}{C_f}) \quad (4.33)$$

therefore, when taking the difference in the digital domain:

$$V_{out} = V_2 - V_4 = \frac{2(C_{xa} + C_{xb})V_c}{C_f} \quad (4.34)$$

Again, C_p is not in the expression, meaning that C_p has no influence to the final output in digital domain.

Component Mismatch

Fig 4.6 can be used again to analyze the effect of mismatch between components. Studying the expressions of output voltages in the four phases, it can be conclude that with respect to component mismatch, the key parameters in the circuit are C_f and V_c. Luckily, as mentioned in the behavior level design (section 3.3.4), since the voltage references are first measured by the ADC, the effect of V_c mismatch can be cancel out by ratiometric measurement principle described in section 3.3.4.

What to be left the to study the influence of C_f mismatch. It can be calculated that the final digital output, with presence of C_f and V_c mismatch equals to

$$V_{out,mismatch} = \frac{2C_{xa}V_{c1}}{C_{f1}} + \frac{2C_{xb}V_{c2}}{C_{f2}} \quad (4.35)$$

It can be seen that the presence of C_f and V_c mismatch will not affect the feature with respect to op-amp offset and input capacitance. Since the effect V_c mismatch can be cancel out, the output voltage can now be expressed as:

$$V_{out,mismatch} = \frac{2C_{xa}V_c}{C_f} + \frac{2C_{xb}V_c}{C_f(1 + \delta)} \quad (4.36)$$

where δ represents the mismatch factor between the two C_f. Compare this with equation 4.34, the mismatch factor Δ of the output can be calculated:

$$\Delta = \frac{V_{out,mismatch}}{V_{out}} = \frac{(1+\delta)C_{xa} + C_{xb}}{(1+\delta)(C_{xa} + C_{xb})} \tag{4.37}$$

assuming $C_{xa} = C_{xb}$, then the effect of C_f mismatch will bring error to the final output. As long as such error is within one LSB of the ADC (with some safe margin), it will not be seen in the digital domain, therefore:

$$\Delta = 1 - \frac{\delta}{2+2\delta} \tag{4.38}$$

and the relative error equals to:

$$\varepsilon = \frac{\delta}{2+2\delta} < 2^{-13} \tag{4.39}$$

by this we can find the maximum tolerable mismatch between the two C_f:

$$\delta < 2^{-12} \tag{4.40}$$

Although the most accurate capacitors in lump element are around 0.1 percent, this is still achievable by using such precision capacitors since δ only represents the difference between the two C_f. Two capacitors with the error rate less than δ still can be found, and the absolute value is less important sense the shift of absolute value will only produce level shift in output voltage, as long as the error rate is small enough, such level shift will behave like offset, which has no influence to the final output. What's more, the effect of the mismatch can also be reduced by calibration.

Cable Capacitance and Coupled Noise

When long connection cables are used, the effect of cable capacitance will affect the performance since the cable capacitance in this case is directly in parallel of the sensing capacitance, shown as Fig 4.7.

From the theory of operation, it can be derived in the charge phase, the charge stored at the input of the op-amp equals to:

$$Q_{inp} = Q_{cxa} + Q_{cc} = (V_c - V_p)C_{xa} + V_cC_c \tag{4.41}$$

$$Q_{inn} = Q_{cxb} + Q_{cc} = -(V_c + V_p)C_{xb} - V_cC_c \tag{4.42}$$

When such amount of charge is transferred, the output voltage equals to

$$V_{outp} = \frac{Q_{inp}}{C_f} = \frac{(V_c - V_p)C_{xa} + V_cC_c}{C_f} \tag{4.43}$$

$$V_{outn} = \frac{Q_{inn}}{C_f} = \frac{-(V_c + V_p)C_{xb} - V_cC_c}{C_f} \tag{4.44}$$

At the input of the instrumentation amplifier, the differential signal equals to:

$$V_{diff} = V_{outp} - V_{outn} = \frac{V_c}{C_f}(C_{xa} + C_{xb} + 2C_c) \tag{4.45}$$

while the common mode signal can be seen as:

$$V_{comm} = \frac{V_{outp} + V_{outn}}{2} = \frac{V_p}{C_f}(C_{xa} + C_{xb}) \tag{4.46}$$

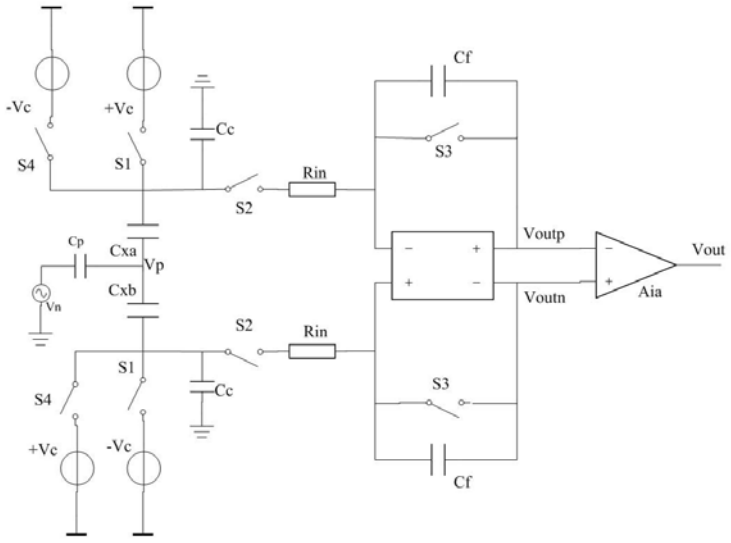

Figure 4.7: Circuit diagram for investigating the effect of cable capacitance and coupled noise on the floating target

Therefore, high common mode rejection ratio of the instrumentation amplifier will help suppress the effect cause by V_p, which is exactly as expected. On the other hand, however, the feature of high CMRR will not gain any beneficial effect with respect to the cable capacitance since it remains in the differential signal and cannot be distinguished by the interface. As a result, active shielding technique will be used to take care of such problem, which will be discussed in the next section.

4.2 Prevent Problem Caused by Cable Capacitance: Active Shielding

The basic idea of active shielding, is to drive the outer conductor at the same potential as that of the inner conductor by using certain circuit [22] [23]. By doing so, there will be no potential difference between the two ends of C_p, meaning that there will be no leakage current flowing through and therefore no error is generated.

According to the different method for the driven circuit, active shielding can be divided in continues-time based implementation and switch-capacitor implementation.

4.2.1 Continuous-Time Type

The driver circuit in continuous time type active shielding is implemented by a buffer amplifier, which can be demonstrated in Fig 4.8

In such configuration, the interference from outside are driven to ground since the low output impedance of the amplifier. More importantly, C_p ideally does not affect the measurement result of C_x because both cable conductors are at the same potential.

Therefore, in principle, using this technique can prevent the problem of cable capacitance. However, due to the parasitic components of the coaxial cable, the buffer amplifier has a positive feedback path that can cause stabil-

ity issue. In addition, due to the limited bandwidth of the buffer amplifier, the inner and outer conductors of the coaxial cable are not at exactly the same potential. As a result, the effect of Cp is still exists, thus limiting the accuracy of the measurement. More detail about the stability and accuracy issue can be found in [24].

4.2.2 Switch-Capacitor Type

An alternative way to have both potentials equal is by means of switch capacitor circuits. The core idea of such type of active shielding would be if the potential applied to the cable are known in advance, these can also be applied to the shield without the need of feedback.[14]

Seen from Fig 4.7, the voltage applied to the cable (signal conductor) will only be one of the three voltages: $+V_c$, $-V_c$, and virtual ground. This is exactly suitable for implementing active shielding in switch capacitor type, what is only needed to add, is three switches connected to the shield, which are operating in phase with S1, S2 and S4 in order to provide the right voltage level. This configuration ensures a shield potential equal to the inner potential and is stable since there is no feedback.

This type of active shielding technique has been used in the proposed interface and detail analysis is presented in section 4.2.3

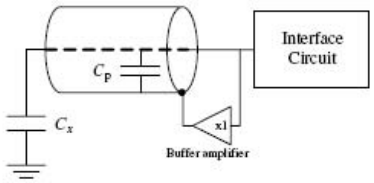

Figure 4.8: Continuous time type active shielding technique used in measurement of grounded capacitor

4.2.3 Performance Analysis

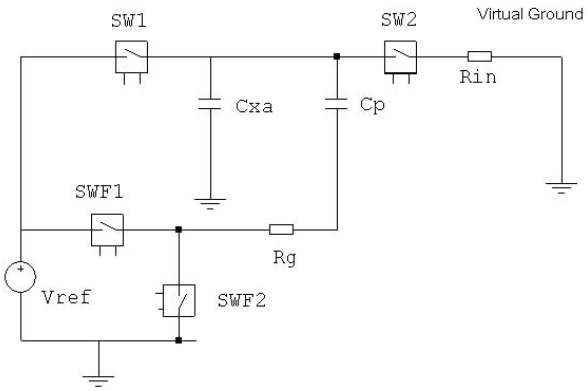

Figure 4.9: Analysis of the effect of switch capacitor type active shielding

Fig 4.9 consists of the essential part of the interface to investigate the effect of switch capacitor type active shielding. C_{xa} is the sensing capacitance and C_p the capacitance to shield. C_{xa} is pre-charged to V_{ref} by closing SW1, and the cable capacitance is held at zero volts with respect to C_{xa} by closing SWF1. During the measurement cycle, SW1 is opened and SW2 is closed so that C_{xa} is discharged into the virtual ground. Where, SWF2 is closed in an attempt to maintain zero volts across V_{ref}. U

Unfortunately, C_{xa} will also discharge into C_p which is now grounded through SWF2 and R_g, which represents the resistance of the discharge path into SWF2. Thus, part of the charge on C_{xa} will initially be lost to C_p. The voltage across C_p will still be discharged into R_{in}, and eventually both C_p and C_{xa} will reach zero volts.

Let us assume that $R_{in} >> R_g$, so initially C_{xa} discharges into C_p rapidly. Therefore, calculating the voltage (V2) across the shield capacitance, C_p:

$$\Delta Q = C_{xa} V_{ref} = (C_{xa} + C_p)V2 \qquad (4.47)$$

and therefore

$$V2 = \frac{C_{xa} V_{ref}}{C_{xa} + C_p} \tag{4.48}$$

On the other hand, The discharge of C_p into the virtual ground is also a charge transfer process, so for the integrator section:

$$(C_{xa} + C_p)V2 = V_{out}C_f \tag{4.49}$$

resulting in the output voltage:

$$V_{out} = \frac{C_{xa} V_{ref}}{C_f} \tag{4.50}$$

It can be seen that the value of output voltage is unchanged. However, the time constant for the transient does change, and consists of the time constant for $C_{xa} + C_p$ in order to settle to the desired accuracy, by discharging through R_{in}. However, the voltage V2 is of the order of 50mV, providing that C_p is approximately 100 times larger than C_x. So the input signal discharging into the integrator is also fairly small. This makes the effect of V_{os} (offset voltage of the op-amp) much more relevant.

4.3 Implementation and Practical Issue

This section focus on the implementation and piratical issue of the proposed interface. The proposed interface has been prototyped into a printed circuit board using lump components. The practical issue regarding to the components will be first described and afterwards the PCB layout will be presented.

4.3.1 Practical Consideration

The complete schematic of the circuit can be found in appendix. Practical and functional considerations for each components are described below:

Voltage Reference

$\pm V_{ref}$ are generated from the ADCs +2.5v reference. At power up the ADCs internal reference is disabled and must be therefore configured via the SPI interface. Finally, the possibility for altering the reference voltages is reserved by just modifying R3 and R6 without losing the op-amp stability.

Power Supplies

The design has three linear regulators providing 15v and +3.3v respectively.

a) The ±15v supplies (U3 and U4) are used for the analog circuit (powering the op-amps and ADC), and should never be connected to any digital circuitry.

b) The +3.3v supply (U5) is used for the digital section of the design and may be taken off the board (via J1) in order to power other digital devices.

c) Notice that the ±15v supplies are made available on J2 allowing the possibility to connect extra analog circuit to the board if required.

d) The input voltages to the voltage regulators should always be in the range 18-25v dc respectively.

Damping and ESD protection

A 100R 1206 resistor (R13/R14) has been placed in series with each shield in order to provide damping when switching between $\pm V_{ref}$. A BAV99 diode pair (D1 and D2) serve to protect the input of the analog switch from ESD/RFI. However, care should be exercised when handling the shield of the SMB connector, as static discharge or short circuits could damage the analog switches.

Instrumentation op-amp

A precision Analog devices AD8221 instrumentation op-amp (U7) has been configured for a closed loop gain of 4.98.

Analogue Switches

There are three types of analog switches present in the design needed for the default state when a logic 0 is applied to the control inputs (G1/G2), e.g. the power up state.

a) The ADG1221 (U11, U13, U14 and U16) is normally open and is used for switching between $\pm V_{ref}$.

b) The ADG1222 (U15) is normally closed and is used to hold the shield at ground at power up and during the capacitors (C_{xa} and C_{xb}) discharge.

c) The ADG1223 (U9 and U12) has one switch that is normally closed and one that is normally open. Notice that the normally closed switch is placed around the integrator in order to hold the op-amp (U8/U10) at ground when not in use.

The valid switch positions for each phase are shown in Fig 4.10, Fig 4.11, Fig 4.12, Fig 4.13 and Fig 4.14 for a single channel. Please refer to section 4.1.1 and section 4.1 for detailed overview of the theory of operation.

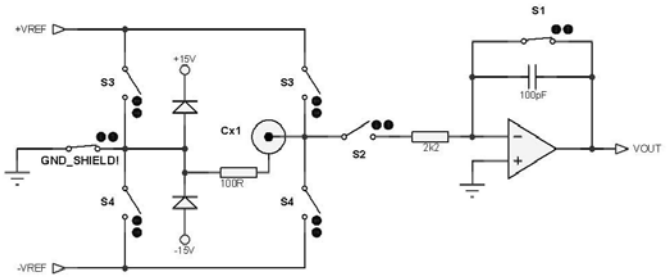

Figure 4.10: Switching position at power up state

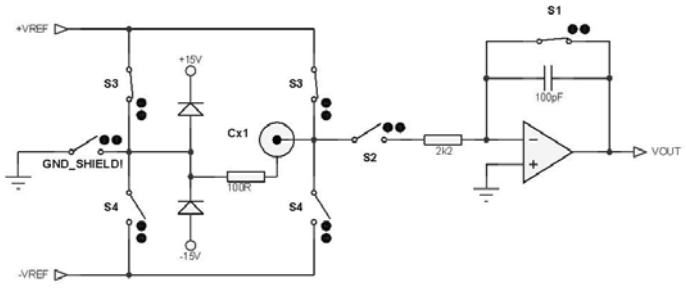

Figure 4.11: Switching position at phase one during operation

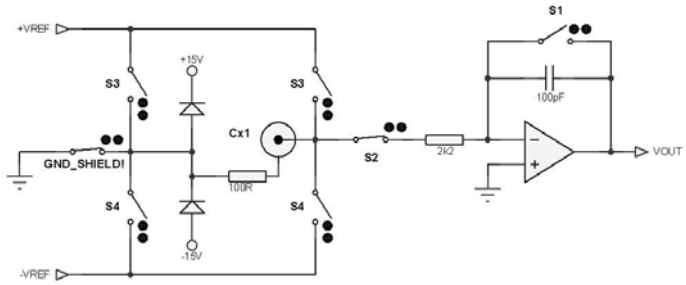

Figure 4.12: Switching position at phase two during operation

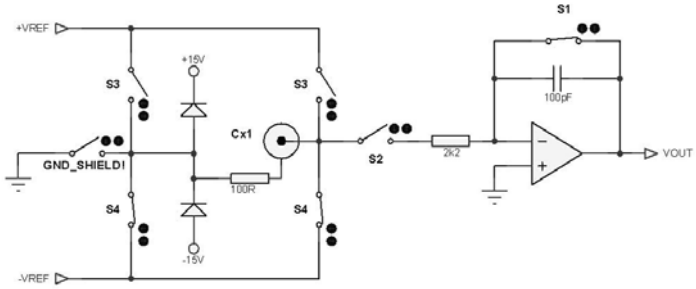

Figure 4.13: Switching position at phase three during operation

General components and comments

There are also some general issue applied for all components,

a) Several low ESR 10 uF tantalum capacitors have been placed on the power supply lines in order to overcome any low/mid frequency interference.

b) All ICs are decoupled with a single X7R 100nF capacitor.

c) All signals to and from the digital interface (J1) have been buffered via a 74AC244 digital buffer (U2) in order to provide protection and ensure consistent start-up behavior.

d) Two LEDs (D3 and D4) have been placed across the 15v power supplies in order to provide a visual reference of the presence of power.

e) Two guard rings have been etched onto the surface of PCB (layer 1) around the integrators (U8 and U10) in order to prevent leakage into the virtual earths and associated R and C.

f) A single unbroken ground plane has been implemented on layer 3, as shown in Fig. Also a partial +3.3v power plane has been implemented for the digital section on layer 4, as shown in Fig 4.19.

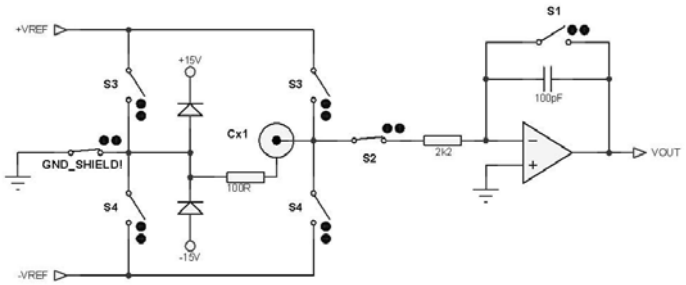

Figure 4.14: Switching position at phase four during operation

4.3.2 PCB Layout Overview

The proposed interface circuit has been implemented on a four layer PCB. The details of which are given below:

Layer 1: signal, power (±15v) and references ($\pm V_{ref}$)

Layer 2: power (±15v) and references ($\pm V_{ref}$)

Layer 3: ground

Layer 4: signal (digital only) and +3.3v power.

By placing all digital signals underneath the ground plane (i.e. on layer 4) it is hoped that a shield between the sensitive analogue signals and the digital signals can be formed. However, notice that in digital region some digital signal traces appear on layers 1 and 2 (see Fig 4.16 and Fig 4.17). Due to the relatively large physical separation between the majority of analogue and digital signals it is not anticipated that any digital return currents from the digital region will significantly manifest themselves on the analog signals.

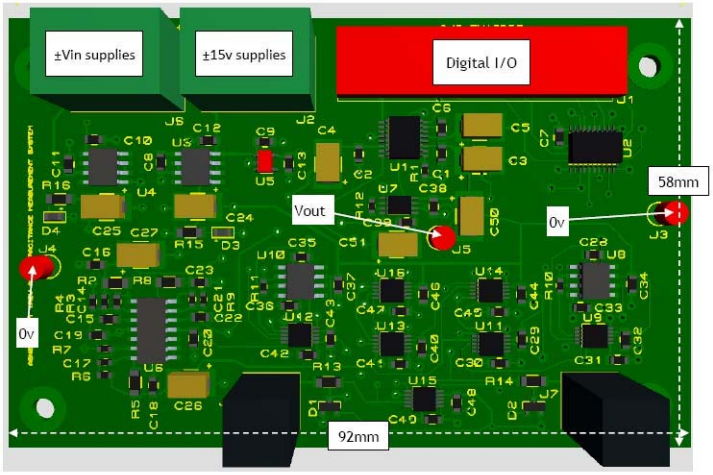

Figure 4.15: 3D front view of the PCB layout

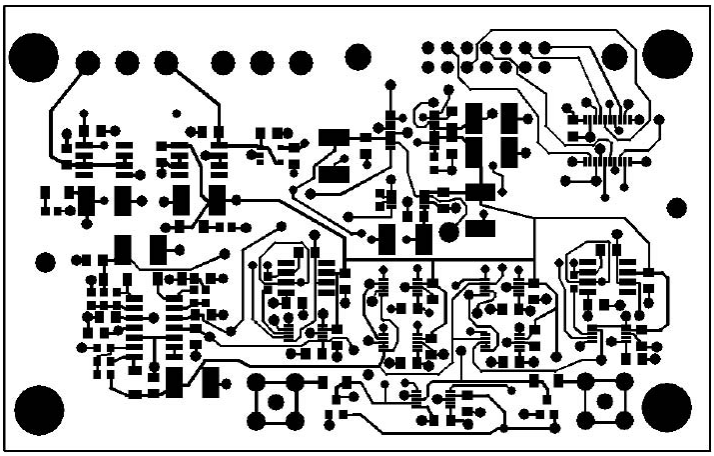

Figure 4.16: Layer 1 (top layer) of the PCB layout

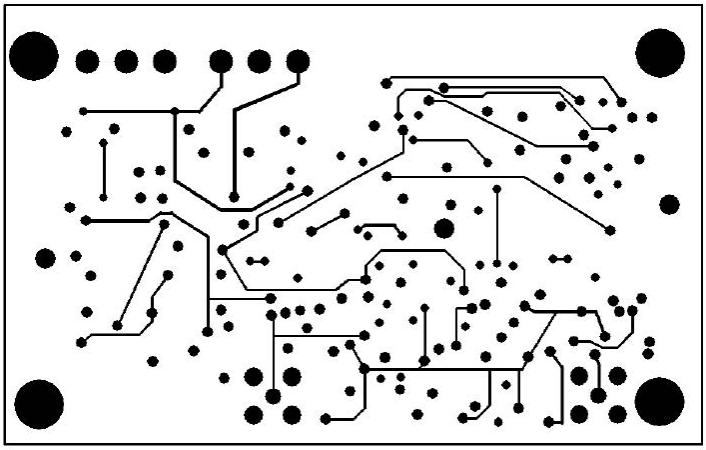

Figure 4.17: Layer 2 of the PCB layout

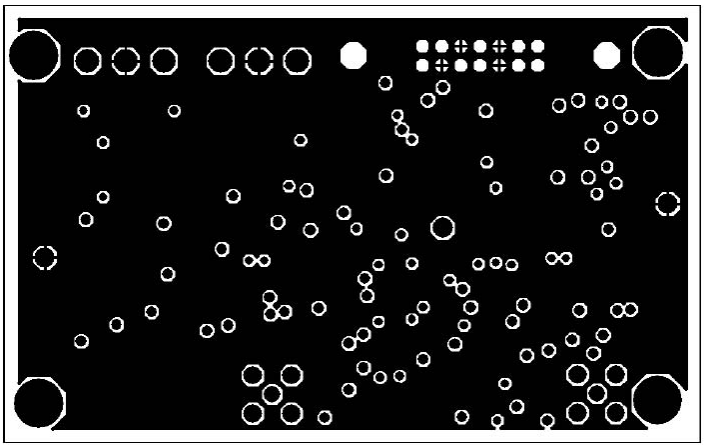

Figure 4.18: Layer 3 (ground plane) of the PCB layout

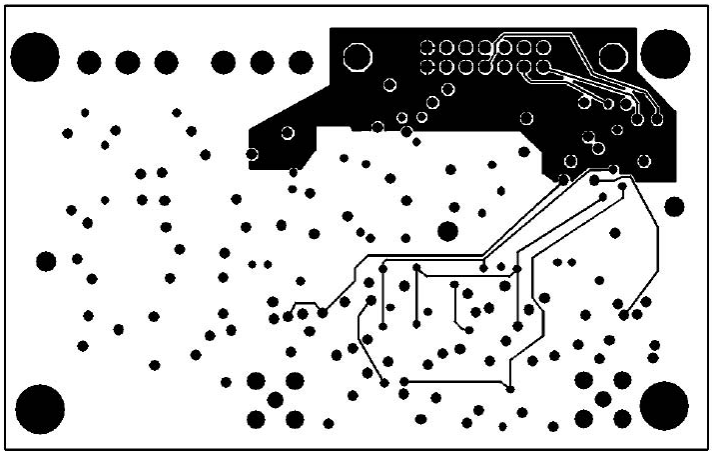

Figure 4.19: Layer 4 (bottom layer) of the PCB layout

4.4 Conclusion

This chapter discussed the issue for the interface circuit, from a design perspective. After proposing the most suitable interfacing principle, a detail analysis of the key issues have provided a clear guidance for selecting the right components. The performance of the interface has been well studied by means of identification and discussion and the key component nonperfection.

Other than theocratical study and calculation, the issue for practical experimentation has also been raised. And finally, the PCB layout has been introduced.

The interface has been properly designed and implemented in printed circuit board, chapter five will present the measurement stately and measurement results of the interface.

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