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A 10 bit 5 MS/s column SAR ADC with digital error correction for CMOS image sensors

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***Abstract*— This paper proposes a SAR ADC whose readout speed is improved by 33%, through applying a digital error correction (DEC) method, compared to an alternative without using the DEC technique. The proposed addition-only DEC alleviates the ADC's incomplete settling errors, hence improving conversion rate while maintaining accuracy. It is based on a binary bridged SAR architecture with 4 redundant capacitors and conversion cycles, which ensure the ADC's linearity of 10 bit within a 5 bit accuracy's settling time. The proposed SAR keeps the same straightforward timing diagram as that in a conventional SAR ADC, incurring no offset to the ADC. Measurement results of 15 columns of SAR ADCs, sampling at 5 MS/s on the same CMOS image sensor (CIS) chip, show integral nonlinearity (INL) around 3 LSB (1LSB = 1mV), when sampling at 5 MHz, after a proposed swift digital background calibration that incurs no additional hardware complexity. The CIS array read out by the proposed column-level SAR ADCs is measured reasonable photoelectron transfer characteristics.**

***Index Terms*— CMOS image sensor, digital error correction, successive approximation register, analog-to-digital converter, SAR, ADC, DEC, digital background calibration**

I. Introduction

Industrial applications such as machine vision requires a CIS to have continuous readout speed between 100 fps and 10 Mfps [1]–[4]. In theory, the maximum achievable readout speed is constrained by the voltage-to-digital conversion. 128 analog memories per pixel have been implemented on-chip to achieve a burst readout speed of 1T pixel/s in [4], for 128 burst instead of continuous video outputs, and 780 Mpixel/s (or, 2 mega columns/s) continuous outputs. In [1], the pixel source-follower (SF) and correlated double sampling (CDS) circuits have been optimized, achieving a continuous column readout speed of approximately 2 MHz. The column rates in [2][3] are around 150 kHz. On the other hand, despite being a crucial component in the voltage to digital conversion, the column ADC has seldom been optimized to further improve the continuous readout speed in previous publications. In contrast, this paper aims to explore the maximum achievable continuous readout speed without incurring additional area (e.g., on-chip memories), in a standard CIS technology process. This aim is achieved by employing DEC for column-level bridged SAR ADC featuring a conversion rate of 5 MHz. This translates to a higher continuous column conversion rate, compared to previous publications [1]–[4]. SAR ADCs are known for their medium resolution, prominent area and power and they have been recently used for high speed applications ranging from a few tens to a few hundred megahertz [5]–[8], using DEC. An *N* bit accurate conventional SAR ADC operates as both an *N* bit ADC and an *N* bit charge balancing DAC, both of which have to meet the accuracy of *N* bit [8].

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In contrast, in SAR ADCs with DEC [5][6]–[8], the DAC settling time could be less than $-ln(1/2^{(N+1)})\cdot\tau$ [9], which is required for a conventional counterpart, while τ being the product of *RC* of the DAC. DEC is generally based on the principle that if a comparator misjudges in a step, either due to comparator dynamic offset or incomplete settling, the following steps could correct for the misjudge: given that in each step, the DAC increases or decreases the charge balancing node voltage in an amount (Δ %) proportionally less than that in a conventional counterpart. The value of Δ % and the DEC logic determines the amount of settling errors that could be compensated for (e.g., up to 37 % in [7]) or the comparator offset that could be tolerated (e.g., $\pm V_{REF}/8$ in a 1.5 bit/stage pipelined ADC while V_{REF} is its full range voltage), without incurring linearity penalties. This paper introduces 4 additional unit sized capacitors and conversion cycles, the required settling time required for each step is reduced by 55 % (from 7.6 τ *to* 3.4 τ). The input voltage sampling time is 10.6 τ (this number is obtained through simulation when the input switch size is designed with regard to the charge injection). So using the conventional approach, the total conversion time would be 7.6 τ ×10 + 10.6 τ=86.6 τ. In contrast, using the proposed approach, the total conversion time would be 3.4 τ ×14 + 10.6 τ = 58.2 τ, saving 33 % time compared to the conventional alternative. Normally, the sampling switch size can be increased for minimizing τ, and when the increment of the switch size reaches a limit due to parasitic or other restrictions, the proposed DEC method reduces the total conversion time by an additional 33 %. Compared to previously published SAR ADCs with DEC, this paper has the following features: (1) The straightforward timing logic as that in a conventional SAR is kept; (2) No offset compensation is required for the digital output codes; (3) A swift digital background calibration is proposed to further improve the ADC's linearity. Our DEC approach is different from that presented in [6], where correlated-reversed instead of straightforward switching is employed. Furthermore, we use single step instead of the multiple step addition-only DEC described in [7]. Besides, our approach does not require the digital offset compensation employed in [8], which uses straightforward timing DEC. This paper is organized as follows. Section II explains the operating principles of the DEC method. Experimental results of 15 columns of SAR ADCs and the CIS read out by the proposed ADCs are shown in Section III. Section IV concludes this paper.

II. Operating Principles

Fig. 1 [10][11] shows the proposed bridge SAR schematic: Initially all the capacitors' bottom plates are connected to V_{CM}. Each time a bit switches, a voltage of $\pm V_{REF}\cdot C_i/2C_{TOTAL}$ is added or subtracted from the charge balancing node *Vx*, which is successively approximated toward $V_{CM}=V_{REF}/2$, depending on the logic value of Bi (1 or 0).

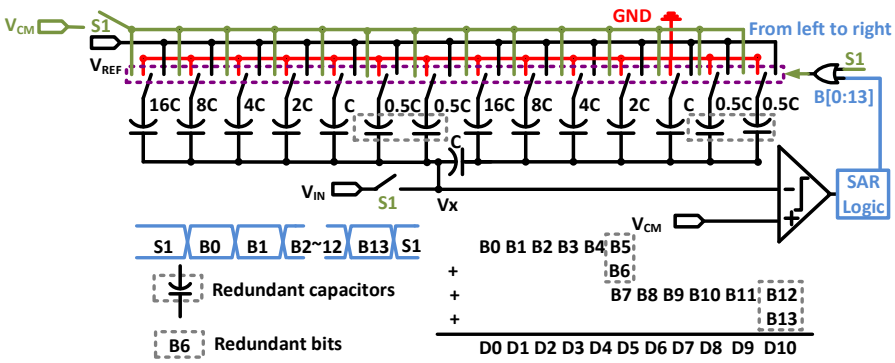

Fig. 1 Proposed bridged SAR ADCs, its timing diagram and DEC logic.

where *Ci* and C_{TOTAL} are the capacitance of the bit Bi (i=1~10) and the total ADC. For instance, if $V_{IN} < V_{CM}$, B0 will switch to V_{REF}, so that $Vx = V_{IN} + 1/2\cdot(V_{REF} - V_{CM}) = V_{IN} + 1/4V_{REF}$, $V_{CM}=V_{REF}/2$; otherwise if $V_{IN} > V_{CM}$, B0 will switch to ground (*GND*), and $Vx = V_{IN} + 1/2\cdot(0 - V_{CM}) = V_{IN} - 1/4V_{REF}$. In this way, *Vx* is successively approximating (switching toward) V_{CM}, and this (successive approximation) also applies to the following bits. In Fig. 1, the weight of the two redundant capacitors B5 and B6 adds approximately another 1/32 of the total capacitance to the left side capacitor array. In this way, each time a bit switches, the voltage added or subtracted is scaled by a factor *Scale_factor*=31/32, approximately. For instance, if B0 incurs an incomplete settling error of 1/32, and causes the comparator to misjudge for the logic value of B1, the maximum error accumulated after B1's switching is $(V_{REF}/(4\cdot32)+V_{REF}/8)\cdot Scale\_factor$ (assuming that B1 is fully settled to simplify the discussion at this moment), which is the sum of B0's settling error $(V_{REF}/(4\cdot32))\cdot Scale\_factor$ and B1's weight $(V_{REF}/8)\cdot Scale\_factor$. The maximum weight of the remaining capacitors are $(V_{REF}/8+V_{REF}/64)\cdot Scale\_factor$, which can fully quantize and compensate for the incomplete settling errors resulting from switching the first two bits. The bit value of B5 and B6 can be 01, 10, 11 and 00. Since initially both capacitors (of B5 and B6) are connected to V_{CM}, for the first two cases (01 and 10), one capacitor is connected to V_{REF} and another is connected to ground, and as $V_{CM}=V_{REF}/2$, these two capacitors can be seen as one parasitic capacitor that is always connected to V_{CM} and only shrinks the ADC's gain as a whole, but incurring no offset. For the case 11 and 00, B5 and B6 functions as one capacitor of the unit capacitor size *C*, adding or subtracting a voltage of $V_{REF}/64$ from the node *V*x. This would compensate for up to the same amount of incomplete settling errors ($\pm V_{REF}/64$) from earlier bits. The settling errors of B5~B11 can be corrected by B12 and B13, in a similar manner. As a result, the settling time per step required for the SAR ADC will be $-\ln(1/32) \approx 3.4\ \tau$, in theory, compared to $7.6\ \tau = (ln(1/2^{(N+1)})\cdot\tau,\ N = 10)$ for aonventional SAR. Taking into consideration the 4 redundant cycles, the proposed DEC method improves the conversion rate (or reducing the total conversion time) by 33%, without incurring penalties in the ADC's linearity. The proposed DEC algorithm is also able to tolerate dynamic comparator offsets, given their effects when combined with that from incomplete settling, are less than $\pm V_{REF}/64$. This capability to tolerate dynamic comparator offset (less than a certain level), is similar to that in a pipelined ADC with DEC [9]. The reasons are that, the charge/voltage is processed in the DAC, and the sub-ADC's misjudge can be corrected by the following stages (steps), as long as the misjudge does not cause overflow. The redundant capacitors in this work are designed to guarantee that the consequent capacitors can cover any previous step's misjudge within a certain limit, either due to unsettling or comparator offset. Comparator dynamic offset can be caused by drain-source voltage variations of the input transistors and the parasitic capacitors [12], which are related to plate voltages. From the DEC logic illustrated in Fig. 1, the bridged SAR is mathematically analogous to a two-step one, where DEC makes the accuracy requirement of the first ADC 5 bit instead of 10 bit. The reasons are that in a SAR without redundancy, the settling errors, in a similar way as the quantization errors, will lead to overflow to the latter bits, and thus can never be corrected. In contrast, in the proposed design shown in Fig. 1, a 10 bit's ADC's accuracy requirement is $\pm 1/2^{11}\cdot V_{REF}$ and the 6-bit second stage (B6~B13) can quantize up to a total of $\pm 1/2^{5}\cdot V_{REF}$, which could cover the non-ideal 5-bit first stage (B1~B5)'s quantization error ($\pm 1/2^{5}\cdot V_{REF}$). B5 and B6 shrinks the ADC gain by 31/32 and introduces no nonlinearity; and the same applies to B12 and B13. Simulation results (Fig. 4) will be shown in Section III to support the above statement. Digital background calibration is employed and described in Section II.B, to calibrate the ADC gain and to compensate for static comparator offset.

III. Experimental Results and Discussions

Fabricated using 0.18 µm CIS technology, a micrograph of the prototype chip is shown in Fig. 2. Each of the 16 column SAR ADCs occupies an area of 18 µm × 830 µm, among which 18 µm × 430 µm is taken by its capacitor array. The unit capacitor size and value are 4.5 µm × 5 µm and 24.59 fF, respectively. It is a MIM (metal-insulator-metal) capacitor. The CIS pixel pitch is 11 µm × 11 µm. With a power supply voltage of 3.3 V, the comparator and the capacitor array in the SAR consume 429 µW of power.

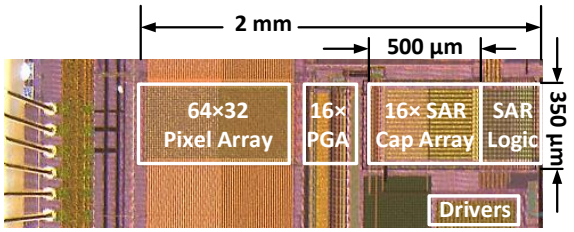

Fig. 2 Micrograph of the chip, with each block (pixel array, SAR ADC capacitor array, etc.) labelled, with its dimensions.

A. *Effectiveness of the proposed DEC method*

The proposed SAR ADC with DEC, as shown in Fig. 1, was measured. The input signal is a 700 mVp-p (-3 dB of full scale), 1.9 kHz sine wave, generated by an Agilent 3220A function generator. The reference voltage range of the ADC is 1 V (0.7 V and 1.7 V). The digital outputs are captured by SignalTap imbedded in Altera Quartus II FPGA.

Fig. 3 shows the measurement results of the ADC's DNL and INL, with and without using DEC, at the same conversion rate. It can be seen that the proposed DEC method effectively improves the ADC's INL from ±12 LSB to ±4 LSB, before being calibrated by the digital background calibration.

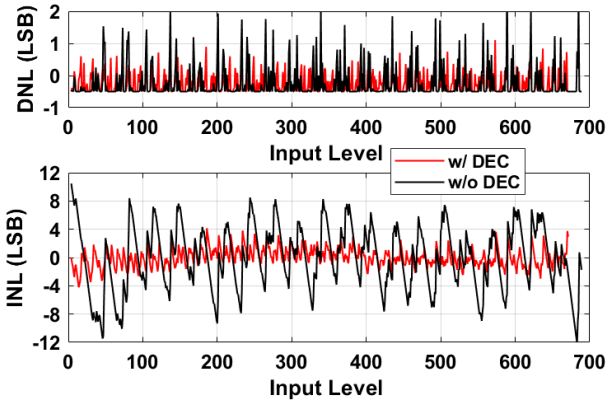

Fig. 3 Measurement results of DNL and INL, with and without DEC for the ADC, at the same conversion rate.

B. *Digital Background calibration*

The proposed digital error correction (DEC) method described in Section II was implemented on-chip using the 4 redundant capacitors, as shown in Fig. 1. In addition, a digital background calibration was employed off-chip to further improve the ADC's INL and SNR, by calibrating the gain mismatches of each capacitor. The method requires no additional hardware on-chip and works as follows. First of all, the ADC outputs are captured and stored in a software tool (e.g., MATLAB in this design). Secondly, the largest (MSB) capacitor is calibrated by supposing all the remaining bits are ideal, as follows: a number (e.g., 1000) of different values of MSB capacitor weight are used to construct the measured outputs, along with the remaining bits with ideal values. Then the one (value of MSB) that enables the best linearity (in the generated outputs) is selected as the calibrated MSB capacitor weight. Thirdly, the calibrated weight of the MSB capacitor is taken into account when calibrating the 2nd largest capacitor, and so on. Finally, the ADC outputs are re-calculated using the calibrated capacitor weights of all bits. Simulations are performed with random capacitor mismatches and then calibrated by the proposed digital background calibration, as shown in Fig. 4. It can be seen that the digital background calibration effectively removes errors caused by random capacitor mismatches.

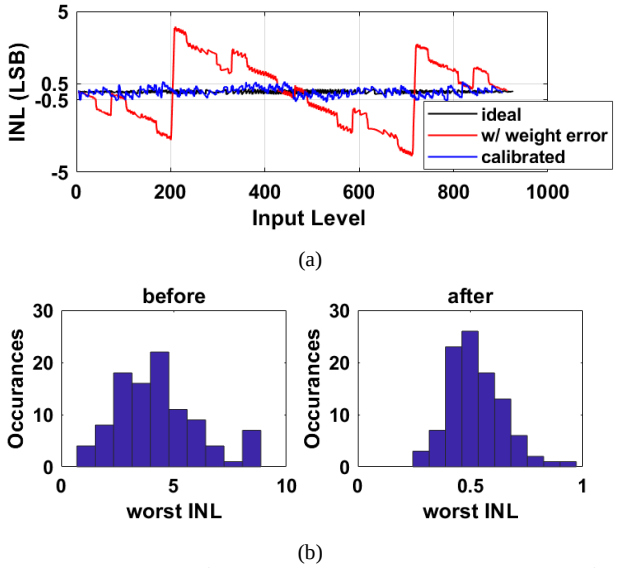

Fig. 4 Simulation results of the digital background calibration. (a) INL for the cases with (w/ weight error) and without (ideal) capacitor mismatches, and after calibration. (b) 100 Monte Carlo simulations of the case with capacitor mismatches before and after the digital background calibration.

C. *The linearity and speed of the proposed SAR with DEC*

The INL and signal-to-noise ratio (SNR) of the proposed SAR ADC in column #8 are measured, at a conversion rate of 5 MHz and post-processed with the proposed digital background calibration described in Section III.B. The measurement results are shown in Fig. 5 and Fig. 6, respectively. Fig. 5 shows that using the digital background calibration, the worst case INL is reduced from around 4.5 LSB to 2.5 LSB. In Fig. 6, the 2nd and 3rd order harmonic distortions (nonlinearity) have been suppressed, where the digital background calibration is applied. The reasons for the noise floor not to show visible decrease with the digital background calibration, is because the calibration corrects for nonlinearity but does not increase resolution. Furthermore, the ADC's worst case INL and SNR are also measured with increasing conversion frequency, between 1 MHz and 6 MHz and are shown in Fig. 7, upon digital background calibration. It can be seen that the measured INL becomes worse as the conversion frequency rises; however, slope (of degrading) becomes sharper when the frequency goes up from 5 MHz to 6 MHz. Fig. 8 shows the worst case INL and SNR of all 15 columns measured on the same CIS chip, without and with the digital background calibration. It indicates that without the digital background calibration, almost all columns have largest absolute INL around 4.5 LSB, while with the digital calibration all the columns' INL are reduced to around 3 LSB and their SNR are improved by approximately 3 dB.

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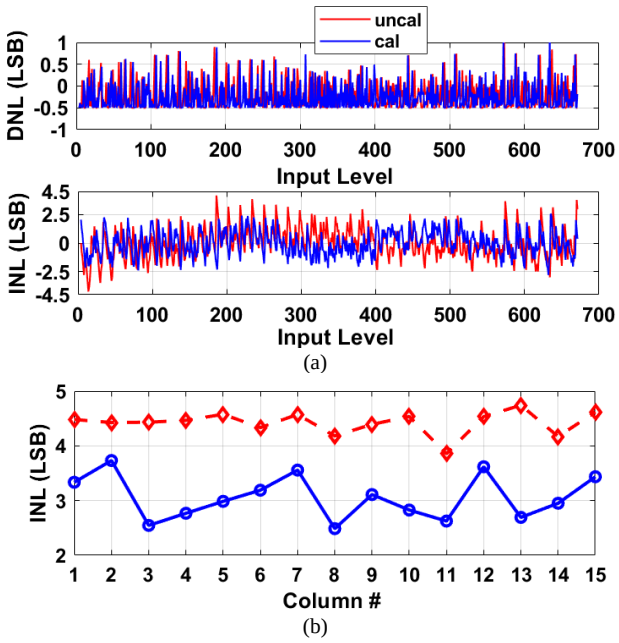

Fig. 5 (a) Measured DNL (top) and INL (bottom) of column #8 at a conversion frequency of 5 MHz, without (red) and with (blue) digital background calibration. (b) Measured INL of all the columns before (red) and after (blue) the digital background calibration.

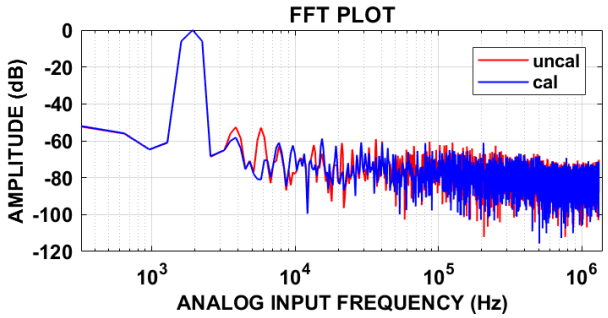

Fig. 6 Measured FFT spectral response of column #8 at a -3 dB 3.66 kHz sine wave input, and a conversion frequency of 5 MHz, without (red) and with (blue) digital background calibration.

The reasons that limit the performances of the proposed SAR ADC are as follows. First of all, although the proposed DEC can reduce the minimum required settling time of the capacitor array, it cannot do the same for the input signal sampling. In this design, the time reserved for the sampling switch S1 (shown in Fig. 1) is 3 times as long as that for each capacitor switching step. The reasons are that as our SAR is single-sided (as the output from a CIS pixel is single-ended), it is more sensitive to charge injection (compared to a fully differential alternative), so the input switch S1 is transmission gate rather than bootstrap based. Secondly, the comparator employed is of conventional pre-amp and comparator architecture, similar to the one presented in [6]. However, to improve the speed and to save the power further, the pre-amp can be biased by a clock signal as in [6], instead of a voltage bias as in the current design. Auto-zeroing technique that can get rid of the comparator offset [11] will be employed for the next prototype (not used in the current design due to speed considerations).

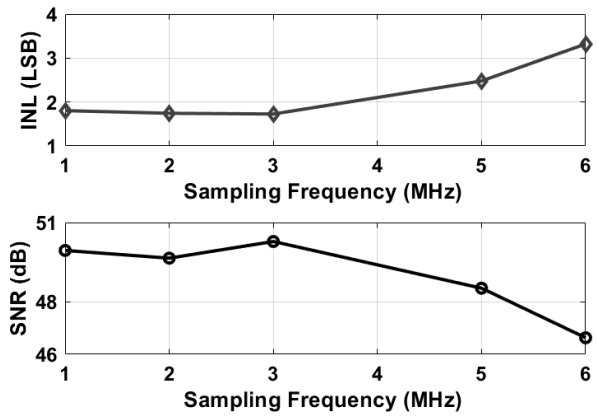

Fig. 7 Measured INL and SNR of column #8 at conversion frequencies between 1 MHz and 6 MHz, at -3 dB analog input level. The results are after digital background calibration.

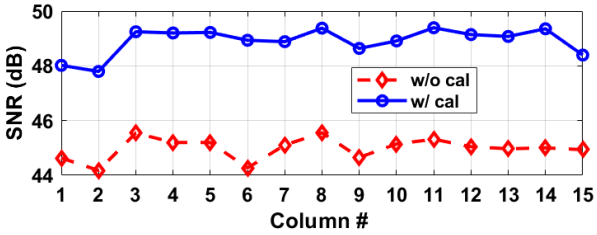

Fig. 8 Measured SNR of all columns at a convresion frequency of 5 MHz and test analog input level of -3 dB, without (w/o cal) and with (w/ cal) digital background calibration.

D. Photoelectron conversion of CIS

The CIS as a whole, equipped with 64×32 conventional 3T APS image pixel array and 16 column level cascade PGAs and SAR ADCs. Architectures of the PGA and the 3T image pixel can be found in [13]. Double sampling is used on the PGA, for the pixel output, to mitigate offset mismatches among the pixels, as shown in Fig. 9, where the signal and the reset voltages of the same pixel are sampled. Two cascade opamps instead of only one are employed in the PGA to optimize the speed, as unity-gain-bandwidth (UBW) of a feedback system is proportional to its feedback factor. For instance, in this design each PGA has a feedback factor of 1/4 (by cascading they have a total closed loop gain of 1/16), compared to 1/16 in a conventional PGA. They consume a current 145 µA at a power supply of 3.3 V. The reason for using 3T instead of 4T image pixel is to get rid of the electron charge transfer time on the transmission gate (TX). This (by using a 3T instead of 4T pixel) enables us to explore the maximum achievable continuous readout speed limited by the column readout circuits. On the other hand, the ultimate solution for the pixel would be based on a pixel that has high-sensitivity, as the one presented in [14], in which the charge transfer time is less than 10 ns. Indicated in Fig. 10, the photoelectron transfer curve of the CIS at 5 MHz has a bit worse linearity, compared to the case when the CIS operates at 1 MHz's column rate. Fig. 11 shows the measured column FPN versus the readout rate of the CIS, indicating that

when the conversion rate increases to the point that the settling errors begin to occur, the column FPN deteriorates.

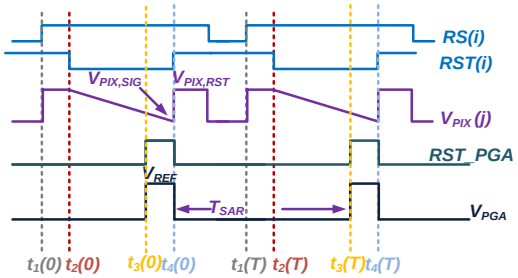

Fig. 9 The timing diagram of the pixel and its PGA in the proposed CIS.

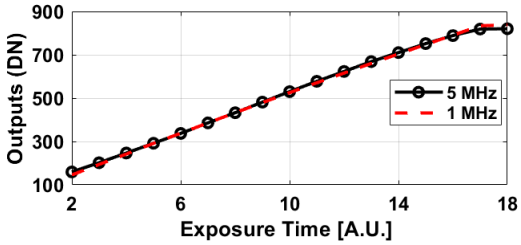

Fig. 10 The photoelectron transfer charateristics: the averaged digital outputs form the CIS chip versus the exposure time of the CIS, at a column readout frequency of 5 MHz and 1 MHz, respectively. A.U. refers to arbitary unit.

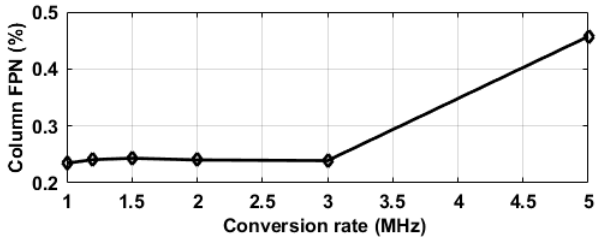

Fig. 11 The measured column FPN versus the conversion (readout) rate.

IV. Conclusions

This paper proposes a DEC that improves the conversion rate of a bridged SAR ADC by 33 %. The DEC method incurs minimum hardware complexity and no offset to the ADC, while maintaining the straight forward timing logic. The measurement results demonstrate all 15 column ADCs have INL around 3 LSB (1 LSB=1 mV) when converting at 5 MHz. The CIS array read out by the proposed SAR ADC is measured to have reasonable photoelectron transfer characteristics. Compared to the state-of-the-art column ADCs in high speed CIS in literature, as listed in Table I, this work has higher column ADC speed, despite using a larger technology node, while maintaining reasonable FOM. This work has the potential for higher speed if using clocked comparator or larger switch size and better ENOB/INL with auto-zeroed comparator.

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Table I Comparison with other column ADCs in high speed CISs

	This work	[1]	[2]	[3]
Process	0.18 µm	0.15 µm	90 nm	0.13 µm
Column ADC speed	5 MHz	2 MHz	125 kHz	150 kHz
ADC ENOB	8	8	9.3	11
Power (single ADC)	429 µW	N/A	437 µW	90 µW
Pixel Count	64×32	3.7 M	2.8 M	640×480
Power (CIS)	9.5 mW	N/A	64 mW	72 mW
FOM[a] (pJ/conv), ADC	0.33	N/A	5.5	0.29

[a]FOM=P/2^ENOB/f, where P and f are the power consumption and the sampling frequency of the ADC

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